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Page 15: Miscellaneous (MISC.SCH)


# Am186CC/CH/CU Customer Development Platform Schematics

# Main Board

**Rev 1.0:** Original design

**Rev 1.1:** TMROUT0[PIO28] changed to SRDY[PIO35].
Nets on DS34C86T's changed.
Pull-ups and pull-downs added to MACH.
Pinouts corrected on diode and MOSFET on USB page.
RXDC[PIO42] changed from TMRIN0[PIO27].
5V power changed to a switching regulator.
Fuse changed to 2A.
Pinouts corrected on diode and flyback transformer on power page.

**Rev 2.0:**
Sheet 2: Add series terminators in 0603 package.
Removed TP1, TP4 and TP5.
Sheet 3: Removed C42, C45, C48, C52, R106 and removed CAP TH-2 drawing.
Changed R32 to C123.
Updated tables and noted.
Removed R38-R44.
Sheet 4: Changed JP7 to 2x2 removing FLASHCS#.
Removed R30, R31, R36, R37.
Sheet 5: Changed JP4 & JP5 to JP18 & JP13, respectively.
Sheet 6: Changed HDLC DCE LED's circuit.
Changed LED part drawing.
Changed label for C1.
Sheet 7: Changed HDLC DCE LED's circuit.
Changed LED part drawing.
Changed label for C6.
Sheet 8: Modified tables.
Added series terminators.
Sheet 9: Changed UART LED's circuit.
Added series resistance to UART.
Changed capacitors to 1000pf.
Changed label for C21.
Sheet 10: Replaced U21 with TN0200T
Added 100K Pull-down to USB detect circuit.
Changed USB LED to PIO8 (ARDY).
Removed C46 and C47.
Added unpopulated 0 Ohm resistors to USB lines from transceiver.
Modified LED part drawing.
Sheet 11: Corrected picture to reflect analyzer configuration.
Sheet 12: Removed R45 & R48.
Removed P29 and fixed illustration.

**Rev 2.0:**
Sheet 13: Added net to VCC5 at P31, pin 55 for 186SEL.
Changed TIPSEL to ENETAEN on P31.
Changed SWIRQ to SHIRQ on P31.
Removed ARDYP on P31.
Removed TIP IRQ Jumpers and replace with 0 Ohm resistors.
Sheet 14: Changed fuse part specification.
Moved C64 and C65 and changed C65 to 0.01uF.
Changed U26 to a different part.
Changed C59 and C119 to 10uF, Y5V, 1210, 25V.
Changed C63 to two 330uF, E-CASE, 10V caps.
Changed C120 to three 330uF, E-CASE, 10V caps.
Sheet 15: Added 10K resistor to Sw6, pin 1 for DCE Multidrop Mode.
Removed RXDHU from SW2.
Rearranged connections to SW2.

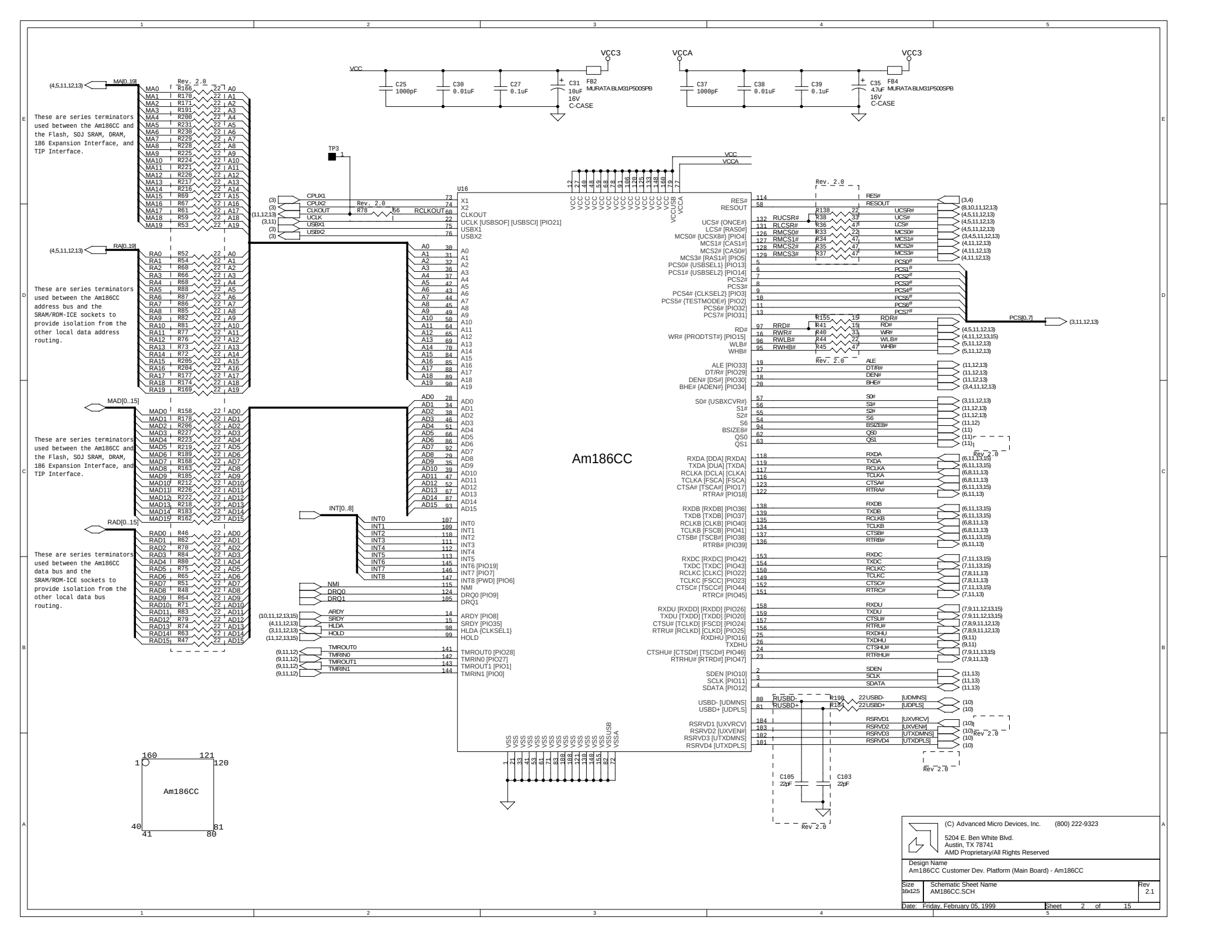
**Rev 2.1:**
Sheet 3: Added UCSX8# pinstrap control
Sheet 9: Changed RS232 DCE UART transceivers circuitry to support full flow control
Sheet 10: Changed USB attach/detach circuit
Sheet 13: Changed TIP ethernet chip select
Added ARDY to TIP connector



Design Name
Am186CC Customer Dev. Platform (Main Board)

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | COVER.SCH | 2.1 |

Date: Tuesday, March 30, 1999 Sheet 1 of 15

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Design Name
Am186CC Customer Dev. Platform (Main Board) - Am186CC

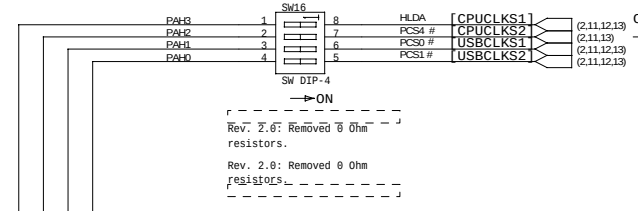
| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | AM186CC.SCH | 2.1 |

Date: Friday, February 05, 1999 Sheet 2 of 15

## Pinstrap Configuration

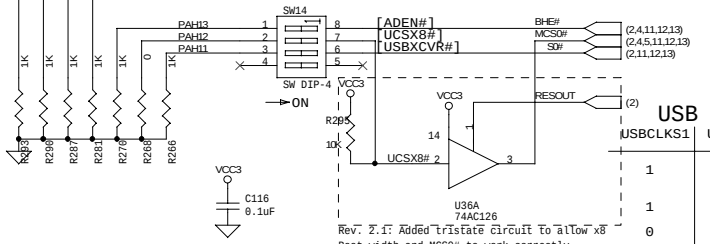
NOTE: Pinstraps default high. Set switch to 'ON' position to enable alternate pinstrap function.

Rev. 2.0: Removed 0 Ohm resistors.




Rev. 2.0: Removed 0 Ohm resistors.

Rev. 2.0: Removed 0 Ohm resistors.




Rev. 2.1: Added tristate circuit to allow x8 Boot width and MCS0# to work correctly.

### CPU PLL CLK MODES

| CPUCLKS1 | CPUCLKS2 | CPU PLL MODE |
|---|---|---|
| 1 | 1 | 2X PLL (DEFAULT) |
| 1 | 0 | 4X PLL |
| 0 | 1 | 1X PLL |
| 0 | 0 | PLL BYPASS |

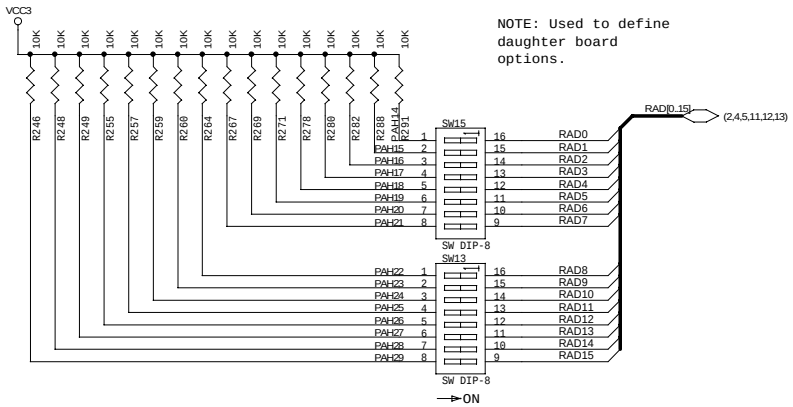
### USB PLL CLK MODES

| USBCLKS1 | USBCLKS2 | USB PLL MODE |
|---|---|---|
| 1 | 1 | USE CPU CLK, USB PLL DISABLED (DEFAULT) |
| 1 | 0 | 4X PLL |
| 0 | 1 | 2X PLL |

Rev. 2.0: Removed PLL Bypass

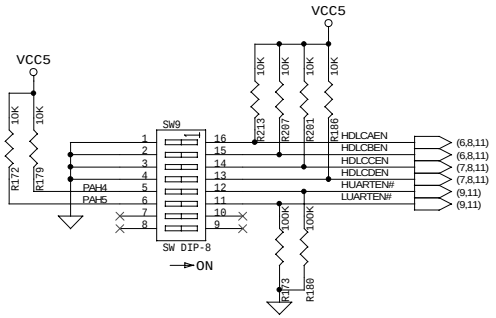
## Reset Configuration

NOTE: Used to define daughter board options.

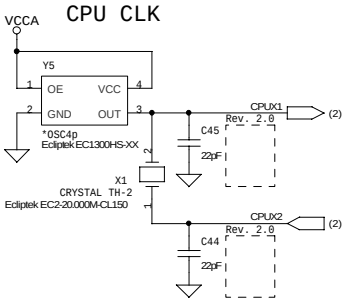



## HDLC / UART SHUTDOWN

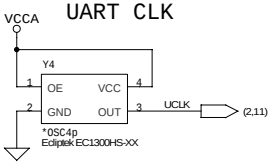
NOTE: To disable all HDLC and UART transceivers set all switches to 'ON'.



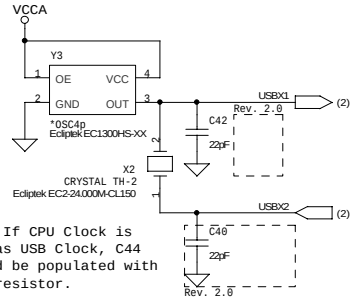

## CPU CLK



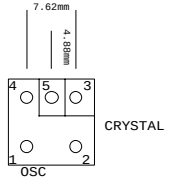

## UART CLK




## USB CLK




NOTE: If CPU Clock is used as USB Clock, C44 should be populated with a 1K resistor.

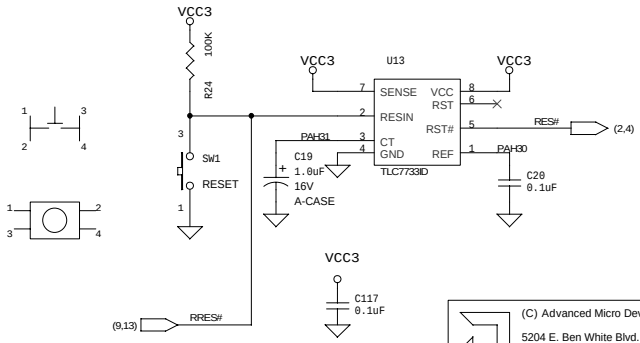



NOTE: Populate oscillator or crystal. Capacitors populated only when the crystal is used.

### CPU and USB Clocking Options

| Clock | 1x | 2x | 4x | PLL Bypass | Oscillator |
|---|---|---|---|---|---|
| CPU Clock | 16-40MHz | 8-25MHz | 8-12.5MHz | 0-24MHz | 0-24MHz |
| USB Clock | X | 24MHz | 12MHz | X | X |
| Shared CPU / USB Clock | X | 24MHz | 12MHz | X | X |
| High Speed / Low Speed UART Clock | X | X | X | X | 0-50MHz |

## Reset Circuit

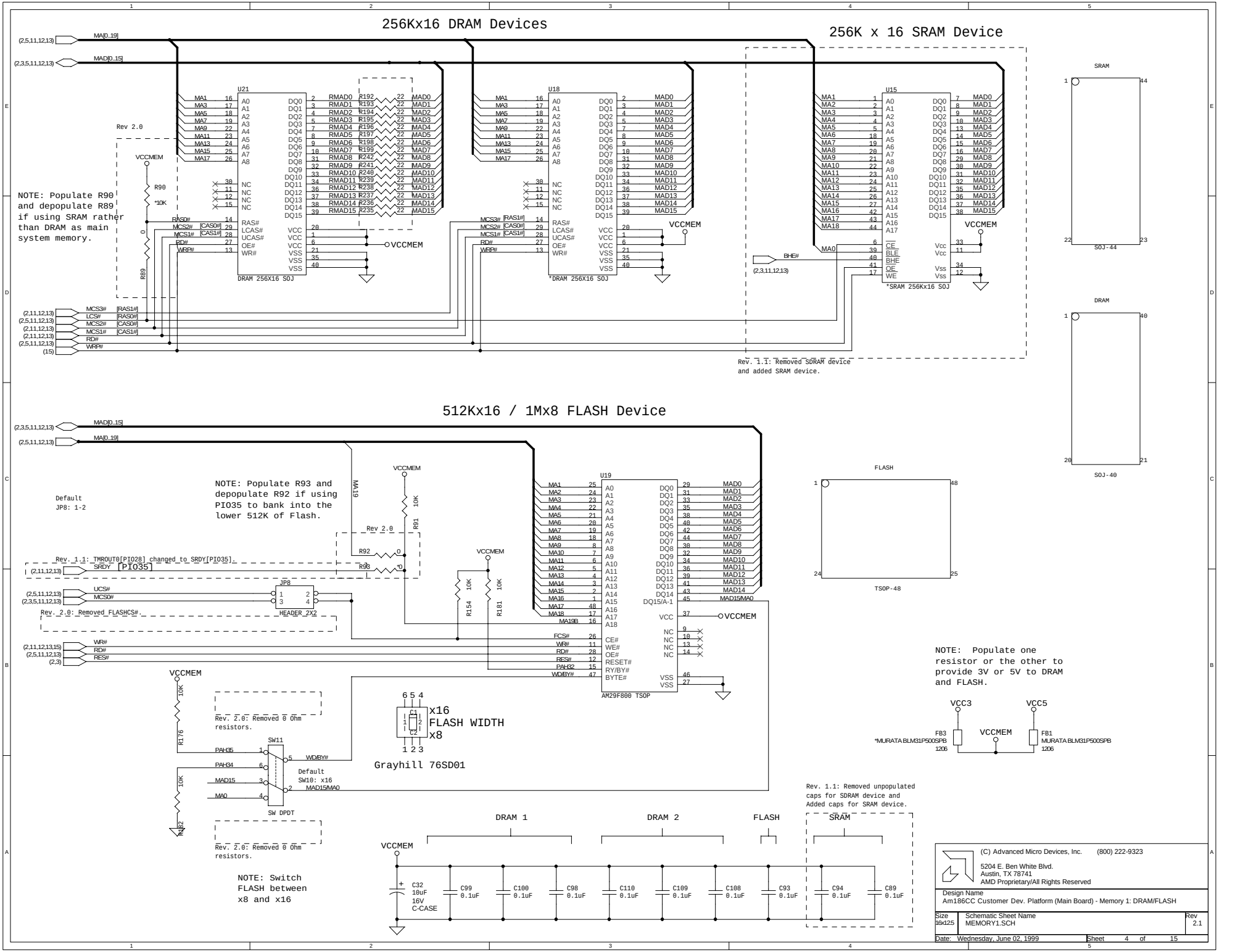





Design Name
Am186CC Customer Dev. Platform (Main Board) - Configuration

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | CONFIGURATION.SCH | 2.1 |

Date: Friday, February 05, 1999 Sheet 3 of 15


256Kx16 DRAM Devices
256K x 16 SRAM Device
U21
U18
U15
DRAM 256x16 SOJ
*DRAM 256x16 SOJ
*SRAM 256Kx16 SOJ
NOTE: Populate R90 and depopulate R89 if using SRAM rather than DRAM as main system memory.
Rev 2.0
R90
*10K
R89
0
VCCMEM
Rev. 1.1: Removed SDRAM device and added SRAM device.
SRAM
SOJ-44
DRAM
SOJ-40
512Kx16 / 1Mx8 FLASH Device
U19
AM29F800 TSOP
NOTE: Populate R93 and depopulate R92 if using PIO35 to bank into the lower 512K of Flash.
Default
JP8: 1-2
Rev. 1.1: TMROUT0[PIO28] changed to SRDY[PIO35].
Rev. 2.0: Removed FLASHCS#.
HEADER 2X2
R92
R93
R91
R154
R181
10K
FLASH
TSOP-48
x16
FLASH WIDTH
x8
Grayhill 76SD01
SW11
SW DPDT
Default
SW10: x16
Rev. 2.0: Removed 0 Ohm resistors.
NOTE: Switch FLASH between x8 and x16
NOTE: Populate one resistor or the other to provide 3V or 5V to DRAM and FLASH.
VCC3
VCC5
FB3
FB1
*MURATA BLM31P500SPB
1206
Rev. 1.1: Removed unpopulated caps for SDRAM device and Added caps for SRAM device.
DRAM 1
DRAM 2
FLASH
SRAM
C32
10uF
16V
C-CASE
C99
C100
C98
C110
C109
C108
C93
C94
C89
0.1uF
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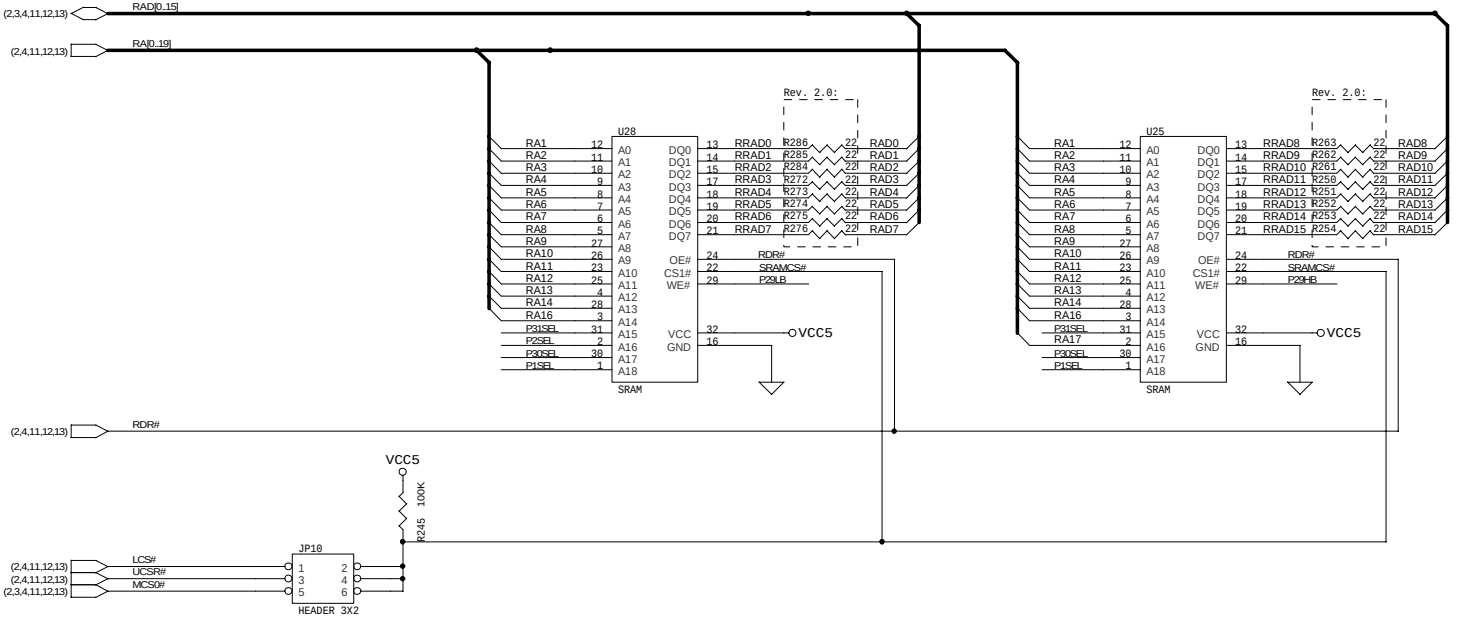
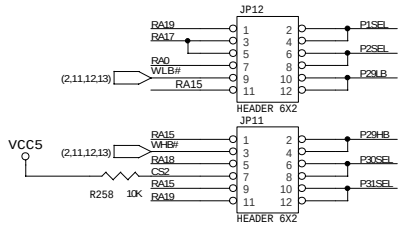
Design Name
Am186CC Customer Dev. Platform (Main Board) - Memory 1: DRAM/FLASH
Size 16x125
Schematic Sheet Name
MEMORY1.SCH
Rev 2.1
Date: Wednesday, June 02, 1999
Sheet 4 of 15

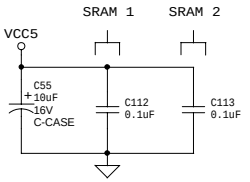
# x8 / x16 SRAM Device, ROM ICE




Rev. 2.0:

| | JP12 | | | JP11 | | |
|---|---|---|---|---|---|---|
| | P1SEL | P2SEL | P29LB | P29HB | P30SEL | P31SEL |
| SRAM 128Kx8 | NC | 7-8 | 9-10 | 3-4 | 7-8 | 9-10 |
| 128Kx16 | NC | 5-6 | 9-10 | 3-4 | 7-8 | 9-10 |
| 512Kx8 | 3-4 | 7-8 | 9-10 | 3-4 | 5-6 | 9-10 |
| 512Kx16 | 1-2 | 5-6 | 9-10 | 3-4 | 5-6 | 9-10 |
| ROM 128Kx16 | NC | 5-6 | 11-12 | 1-2 | NC | NC |
| 512Kx16 | NC | 5-6 | 11-12 | 1-2 | 5-6 | 11-12 |



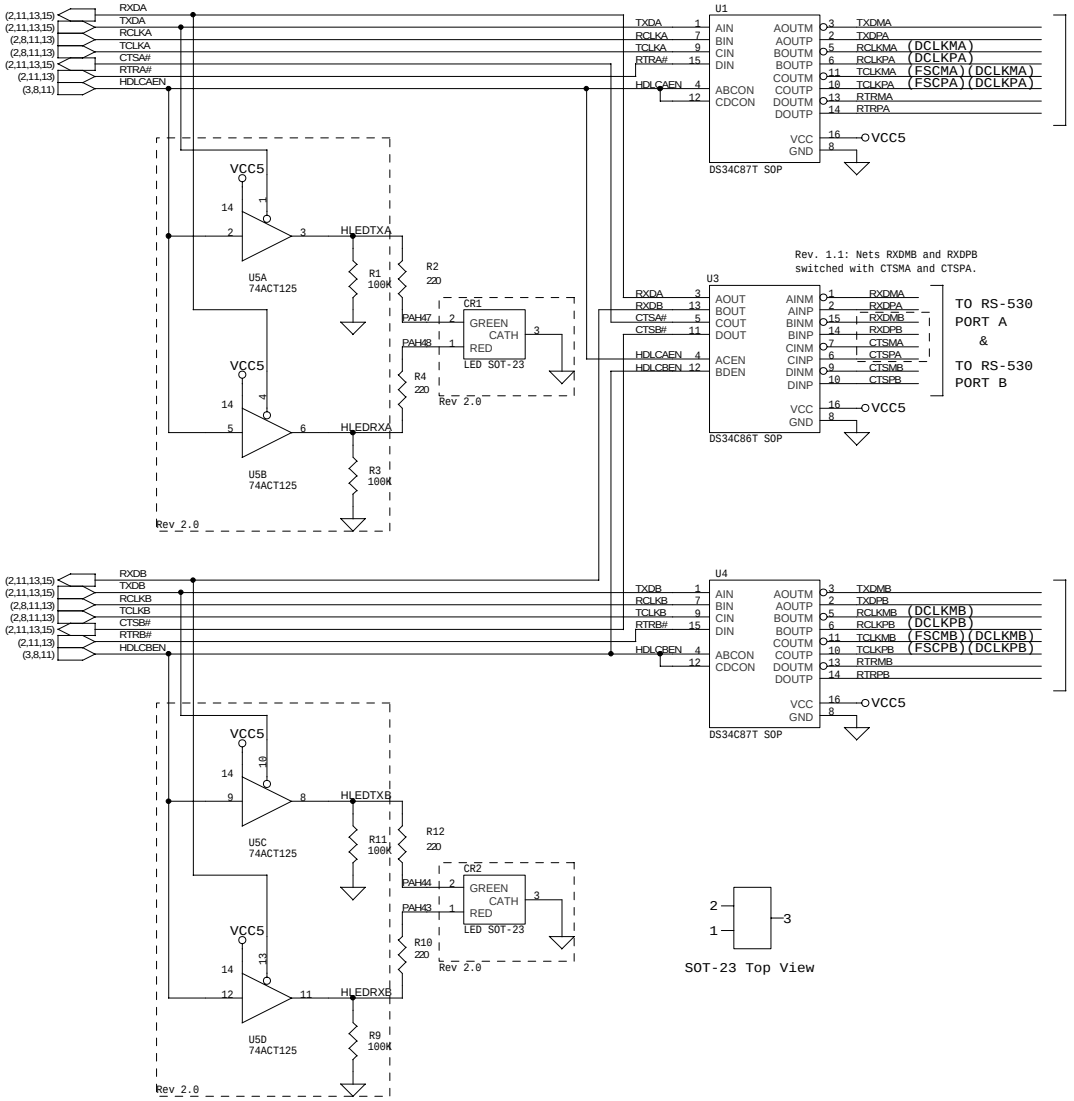



Design Name
Am186CC Customer Dev. Platform (Main Board) - Memory 2: SRAM/ROM

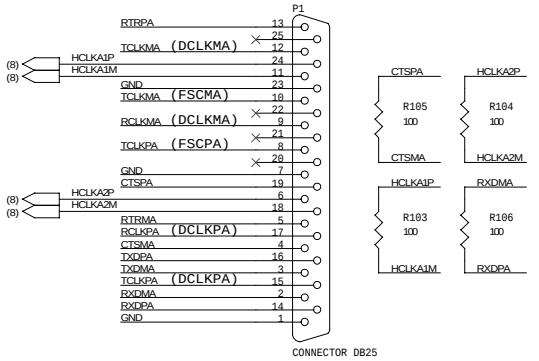
| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | MEMORY2.SCH | 2.1 |

Date: Friday, February 26, 1999 Sheet 5 of 15

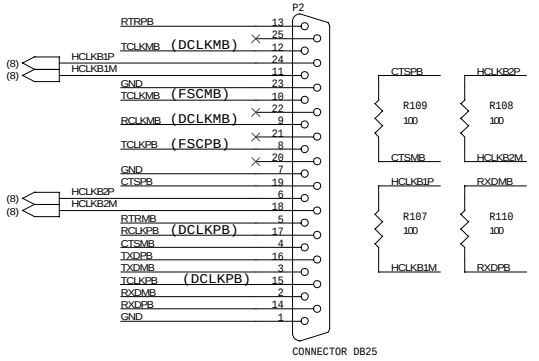
## RS-422 TRANSCEIVERS

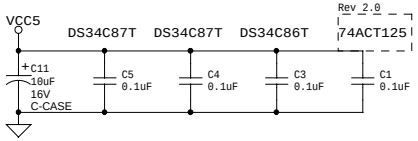



## RS-530 PORT A




## RS-530 PORT B







SOT-23 Top View

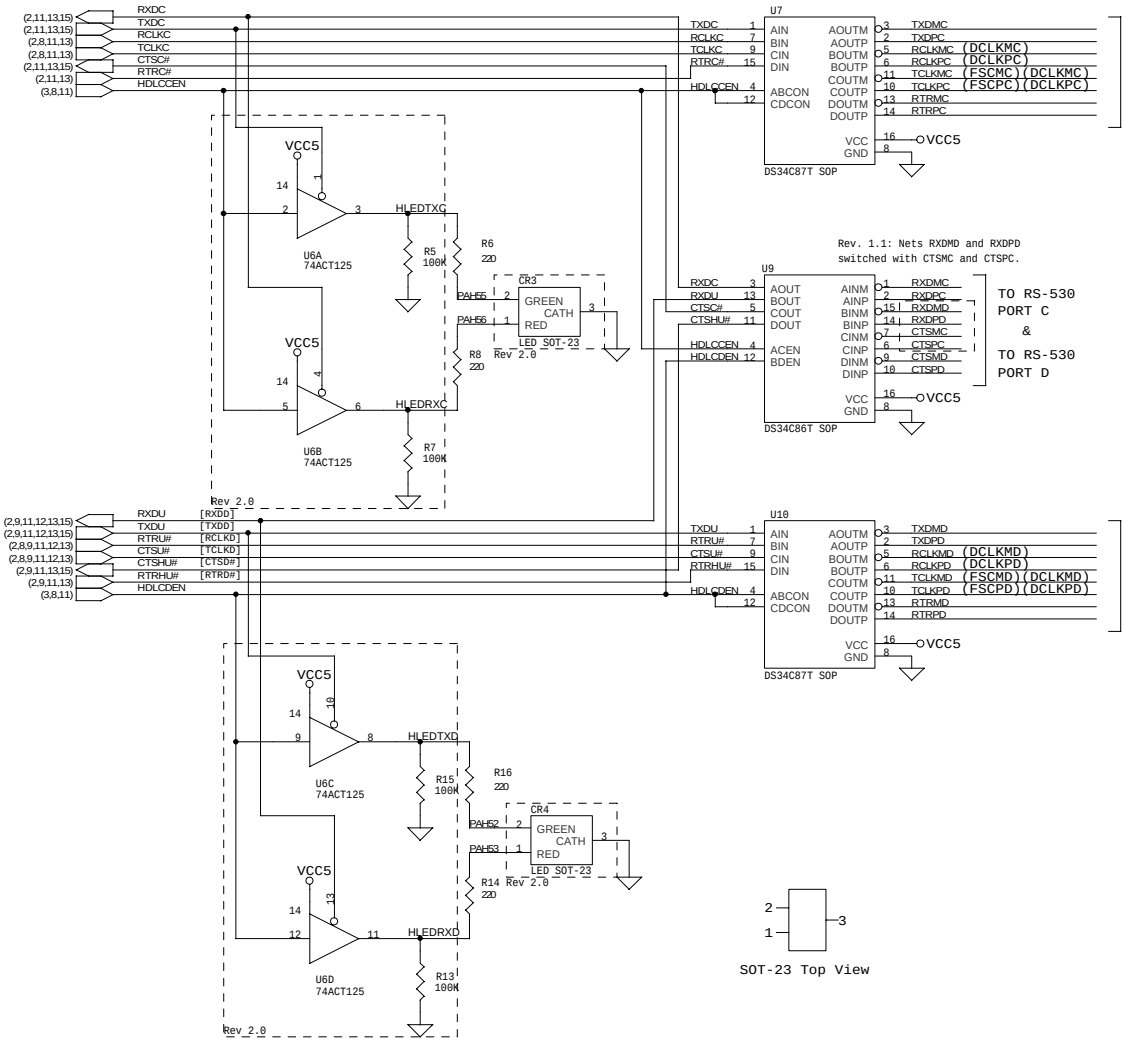


Design Name
Am186CC Customer Dev. Platform (Main Board) - HDLC Transceivers (Page 1)

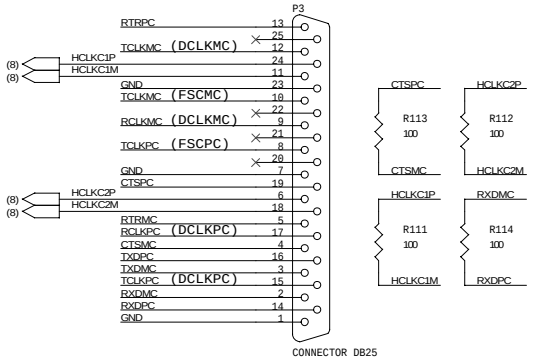
| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | HDLC1.SCH | 2.1 |

Date: Friday, February 05, 1999 Sheet 6 of 15

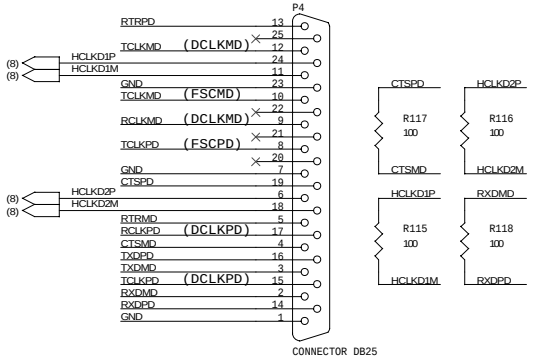
## RS-422 TRANSCEIVERS

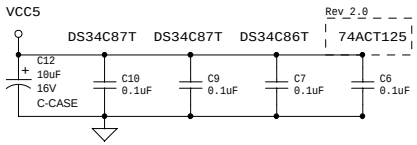



## RS-530 PORT C




## RS-530 PORT D



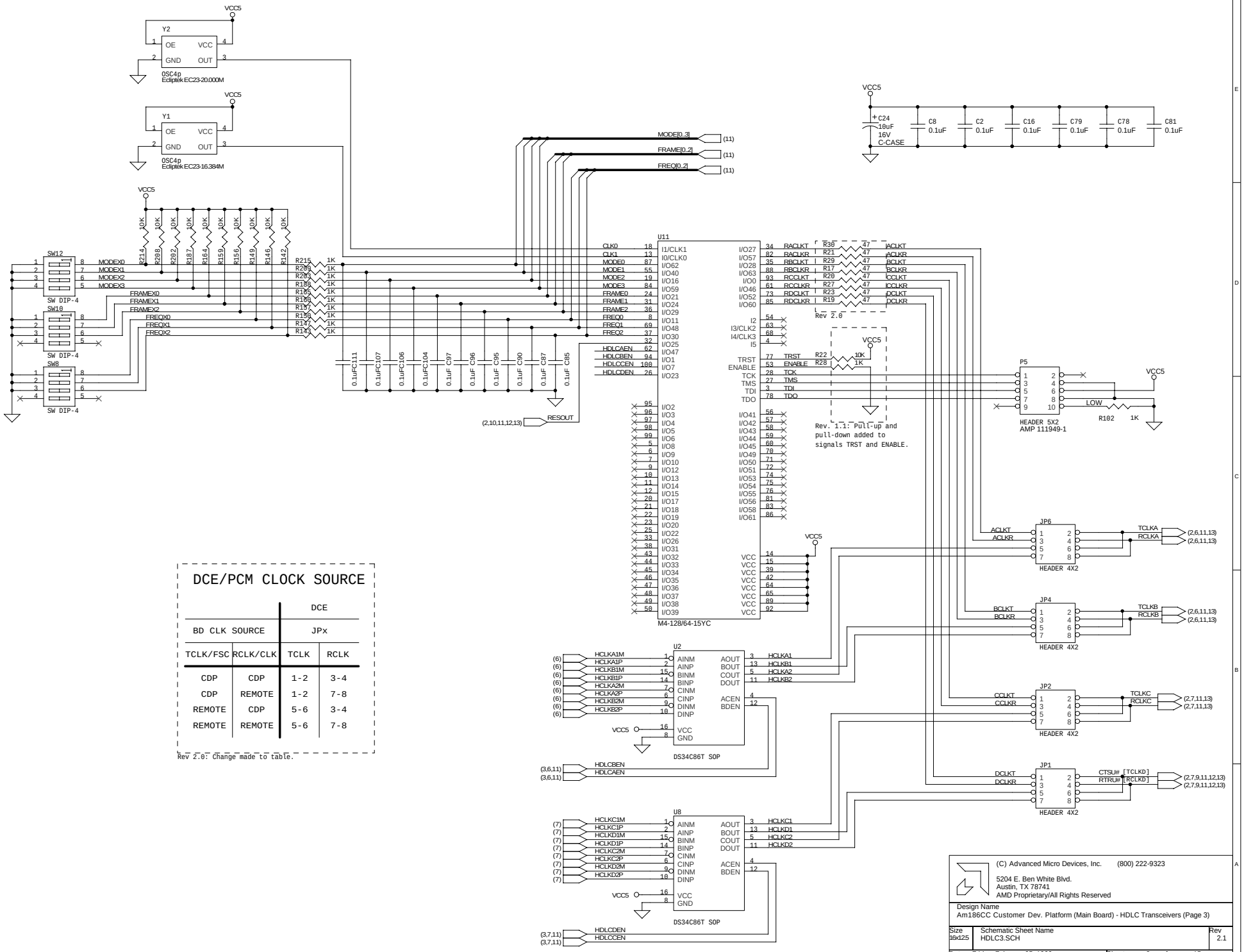






Design Name
Am186CC Customer Dev. Platform (Main Board) - HDLC Transceivers (Page 2)

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | HDLC2.SCH | 2.1 |

Date: Friday, February 05, 1999 Sheet 7 of 15




## DCE/PCM CLOCK SOURCE

| | DCE | |
|---|---|---|
| BD CLK SOURCE | JPx | |
| TCLK/FSC RCLK/CLK | TCLK | RCLK |
| CDP CDP | 1-2 | 3-4 |
| CDP REMOTE | 1-2 | 7-8 |
| REMOTE CDP | 5-6 | 3-4 |
| REMOTE REMOTE | 5-6 | 7-8 |

Rev 2.0: Change made to table.



Design Name
Am186CC Customer Dev. Platform (Main Board) - HDLC Transceivers (Page 3)

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | HDLC3.SCH | 2.1 |

Date: Friday, February 05, 1999 Sheet 8 of 15

CTSC# (PIO44) and RTRC# (PIO45) can be used to provide HSUART hardware flow control in case CTSHU# is needed as its TSCD# alternate function.

## High Speed UART

Rev 2.1: Changed Part

SP207HB
Sipex SP207HBCT

NOTE: PIO's may be used as additional hardware flow control signals for the high or low speed RS232 port if needed. These are defined as:
PIO0 - DCD
PIO1 - DTR
PIO27 - RI
PIO28 - DSR

NOTE: SIPEX XCVR'S HAVE 400K PULLUPS ON DRIVER INPUTS AND 5K PULLDOWNS ON RECEIVER INPUTS

SOT-23 Top View

## Low Speed UART

Rev 2.1: Changed Part

SP207B
Sipex SP207BCT

VCC5 SP211H SP211 74ACT02

CONNECTOR DB9



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Design Name
Am186CC Customer Dev. Platform (Main Board) - High Speed UART

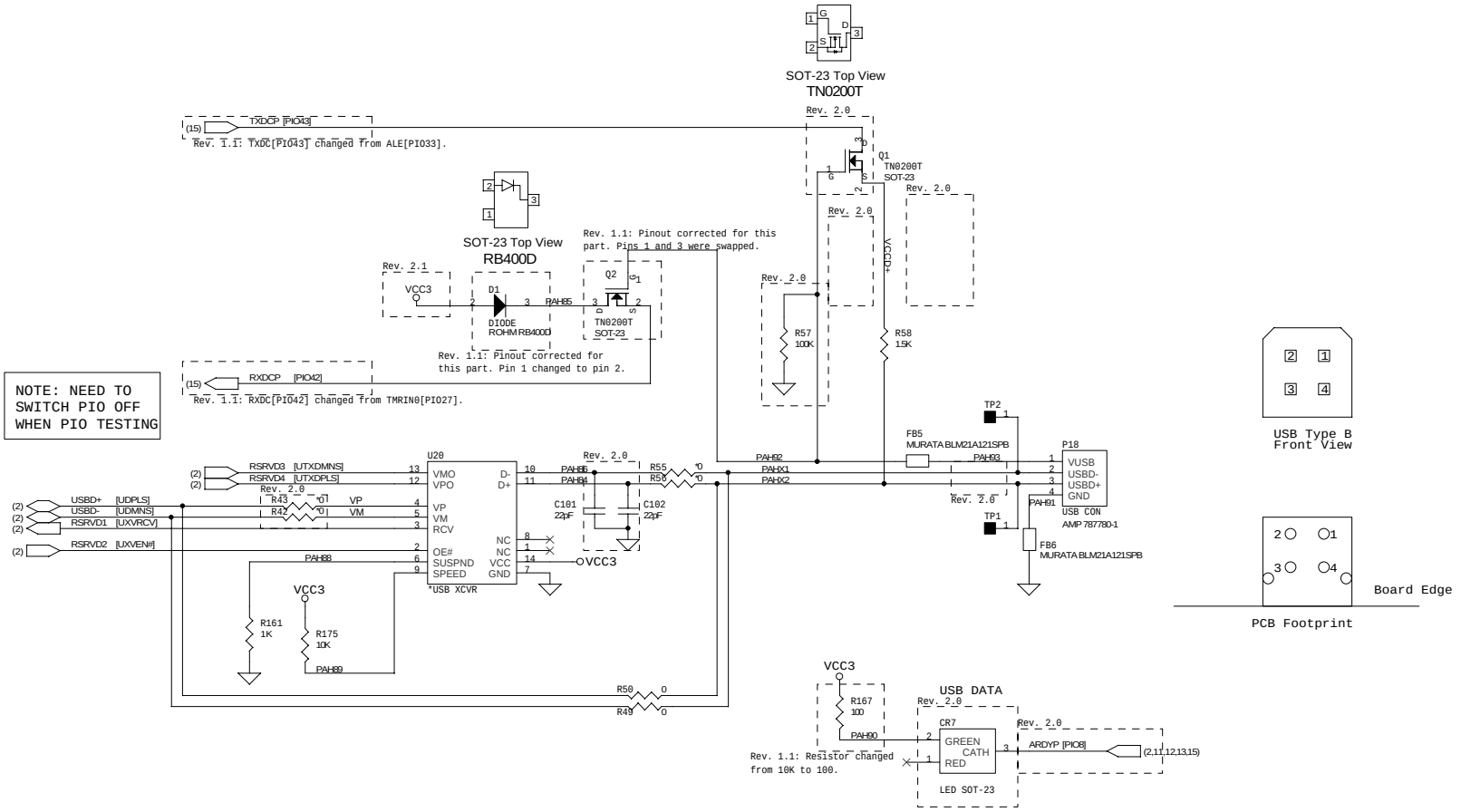
| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | UART.SCH | 2.1 |

Date: Thursday, February 11, 1999 Sheet 9 of 15

## Am186CC USB Attach/Detach

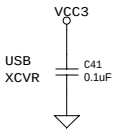
Attach: 1) Am186CC polls RXDCP [PIO42] for high edge to determine when VCCusb becomes active.
2) Am186CC drives TXDCP [PIO43] for LDO enable high after VCCusb presence detected.

Detach: 1) VCCusb goes away: Am186CC polls RXDCP [PIO42] for low edge.
2) Am186CC tristates USBD+/D-.
3) Am186CC VCC goes away: Q1 isolates VCCusb from RXDCP [PIO42].




### USB Transceiver Population Option

| Internal | External |
|---|---|
| R28 | R33 |
| R29 | R34 |
| | R231 |
| | R232 |

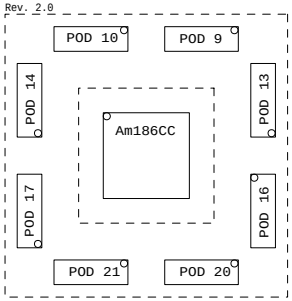


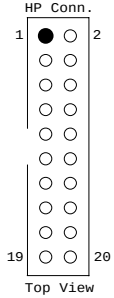


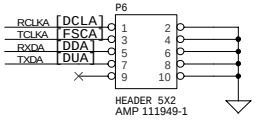

Design Name
Am186CC Customer Dev. Platform (Main Board) - USB Transeiver

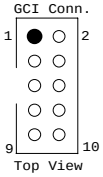
| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | USB.SCH | 2.1 |

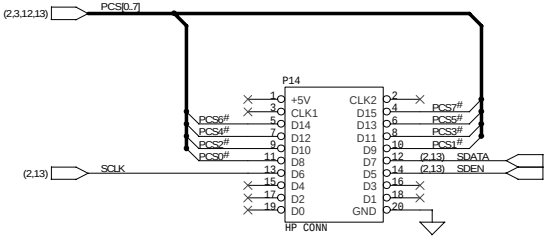
Date: Thursday, February 11, 1999 Sheet 10 of 15

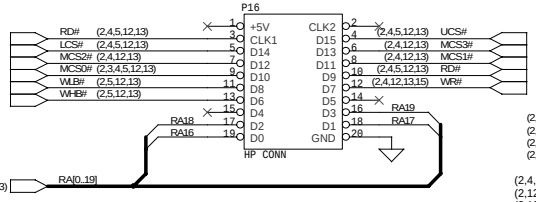


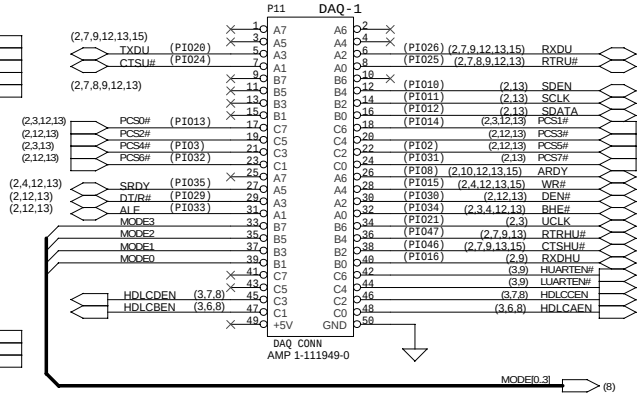



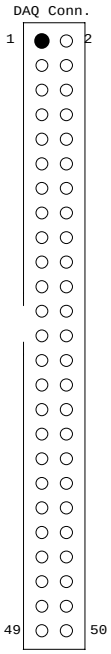



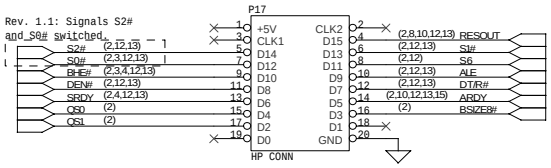



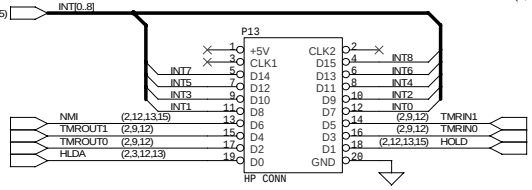



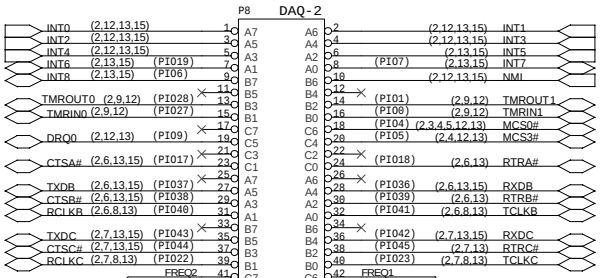



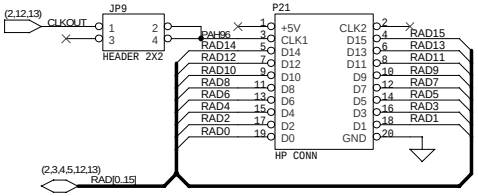



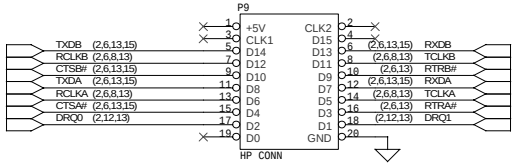



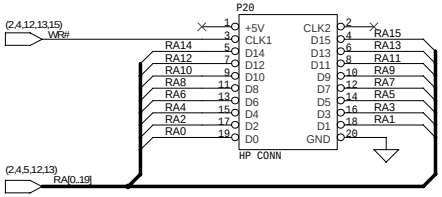



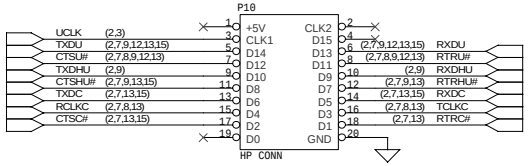



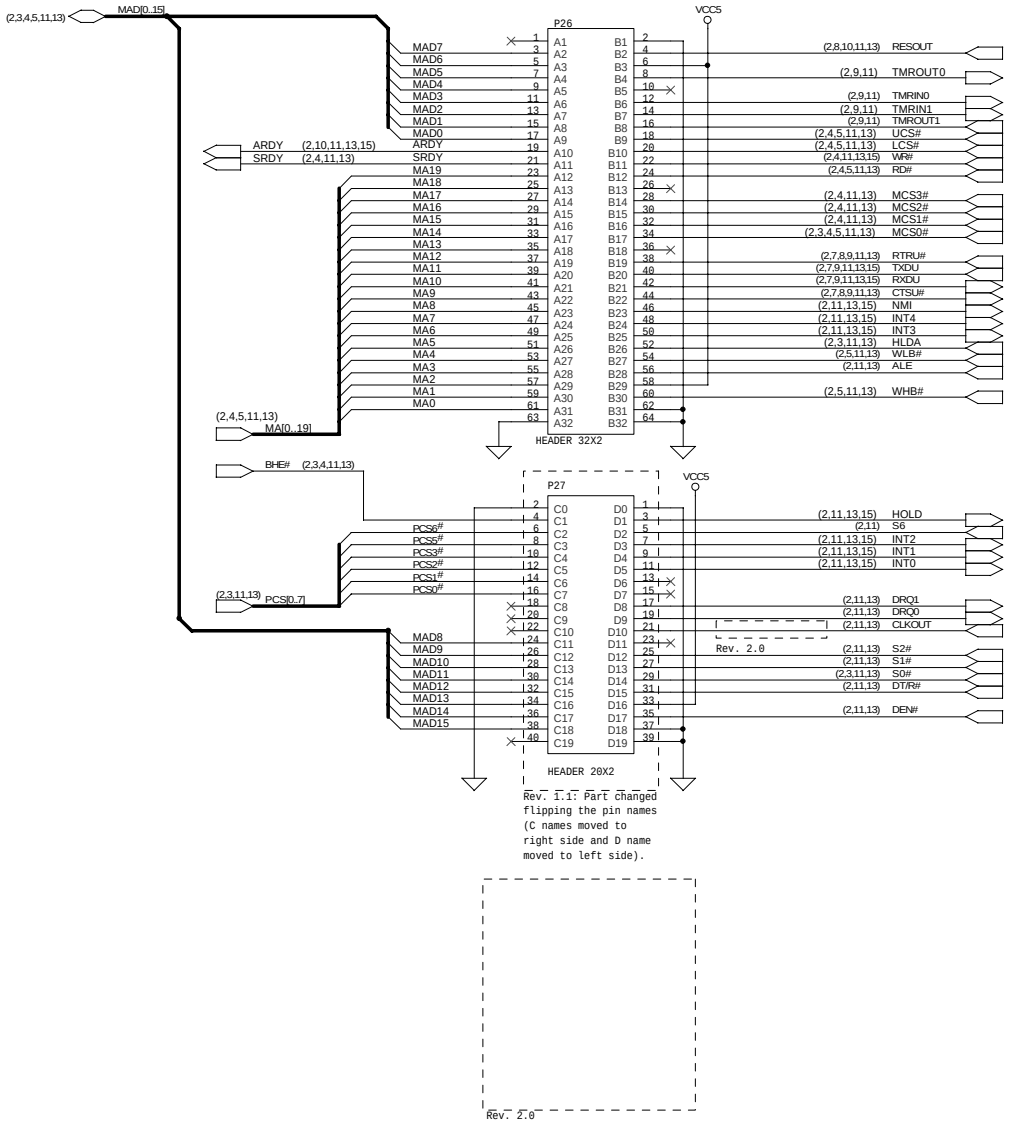


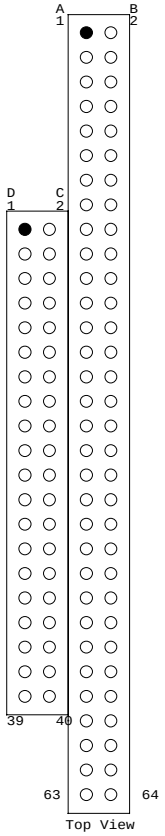

Design Name
Am186CC Customer Dev. Platform (Main Board) - DEBUG/DAQ

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | DEBUG/DAQ.SCH | 2.1 |

Date: Friday, February 05, 1999 Sheet 11 of 15

# 186 Local Bus Interface





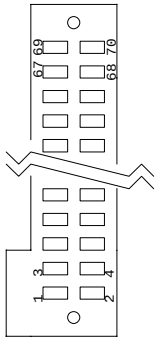

Design Name
Am186CC Customer Dev. Platform (Main Board) - 186 Local Bus Interface

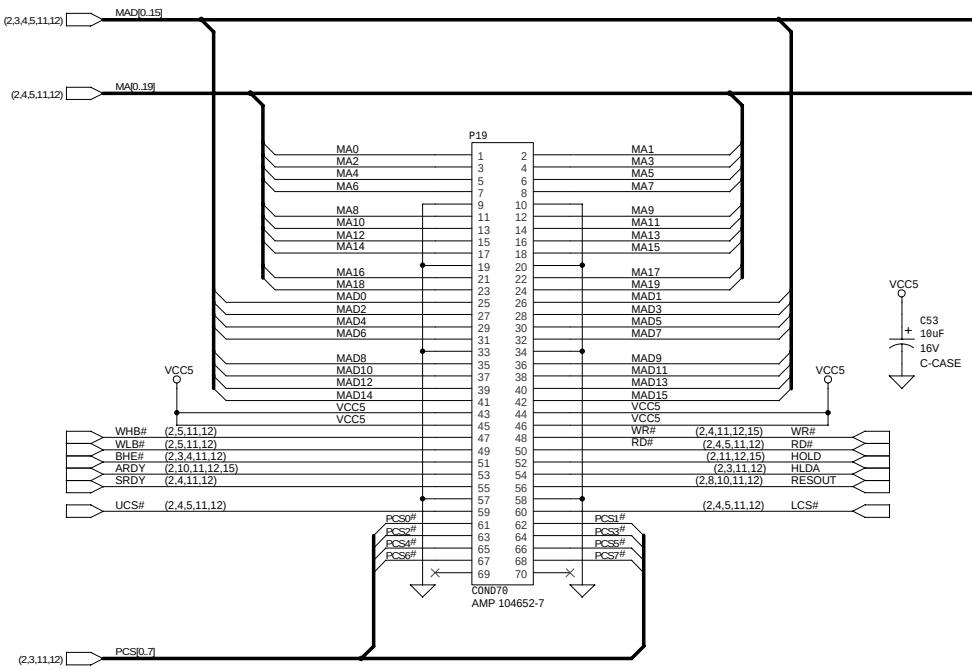
| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | 186EXP.SCH | 2.1 |

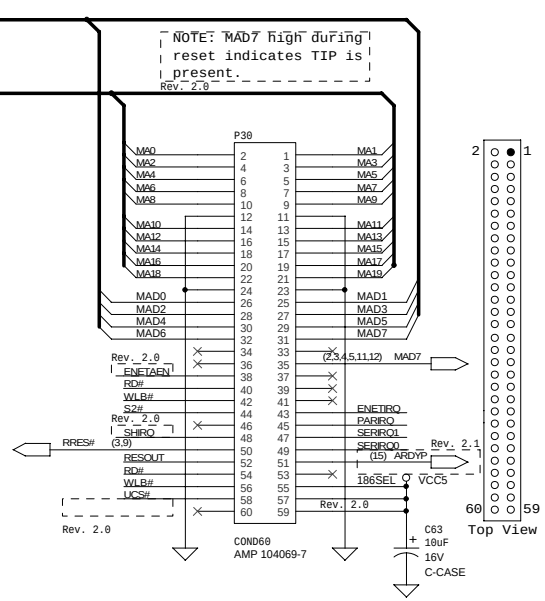
Date: Friday, February 05, 1999 Sheet 12 of 15

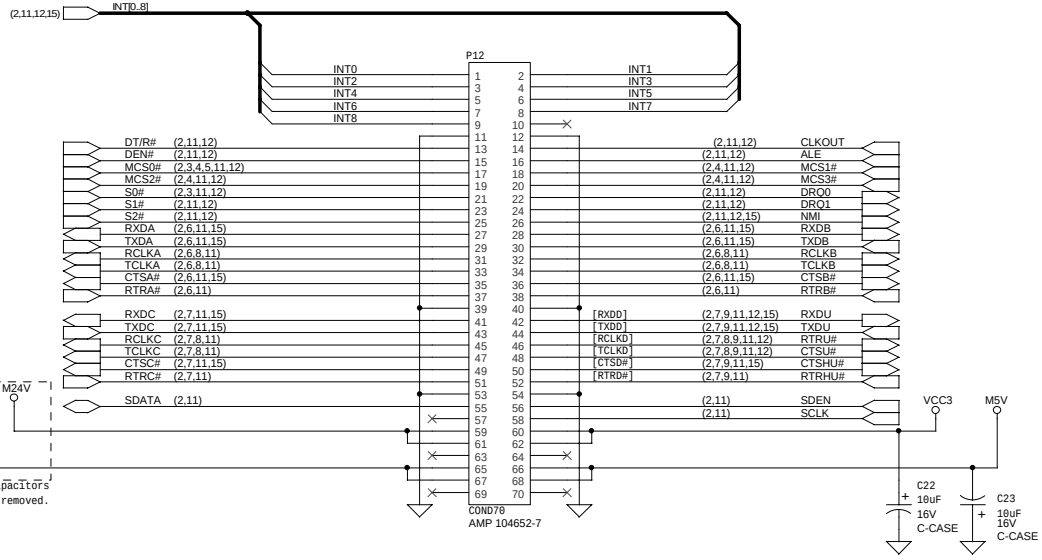
Module Connectors

Tip Conn.

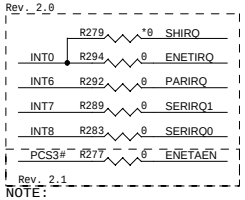



NOTE: ROUTES TIP IRQ'S TO Am186CC/CH/CU



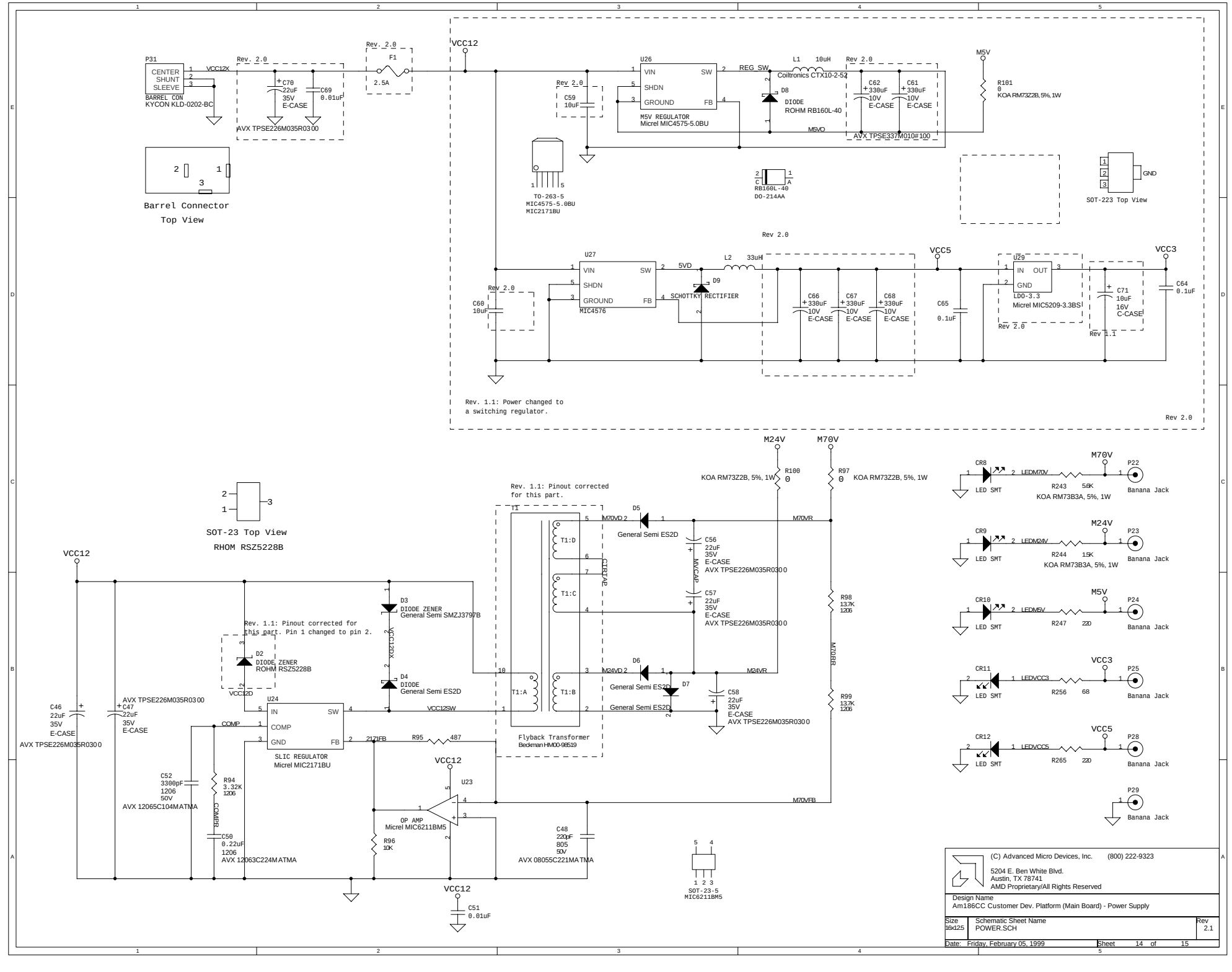

NOTE:
(1) SHIRQ is all IRQ's logically OR'ed on TIP and configured as level triggered high.
(2) MAD7 is TIP present indicator in RESCON register.
(3) PCS3# is the TIP ethernet chip select.
(4) S2# is the MEM/IO cycle detect to TIP.



Design Name: Am186CC Customer Dev. Platform (Main Board) - Module and TIP Connectors

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | MODULE/TIP.SCH | 2.1 |

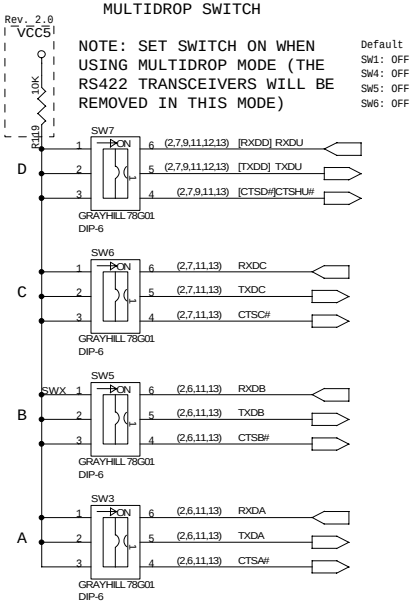
Date: Wednesday, June 02, 1999 Sheet 13 of 15


P31
CENTER
SHUNT
SLEEVE
BARREL CON
KYCON KLD-0202-BC
VCC12X
Rev. 2.0
C70
22uF
35V
E-CASE
C69
0.01uF
AVX TPSE226M035R0300
Rev. 2.0
F1
2.5A
VCC12
U26
VIN
SHDN
GROUND
SW
FB
M5V REGULATOR
Micrel MIC4575-5.0BU
REG_SW
L1 10uH
Coiltronics CTX10-2-52
Rev 2.0
D8
DIODE
ROHM RB160L-40
C62
330uF
10V
E-CASE
C61
330uF
10V
E-CASE
M5VO
AVX TPSE337M010#100
M5V
R101
0
KOA RM73Z2B, 5%, 1W
C59
10uF
Rev 2.0
TO-263-5
MIC4575-5.0BU
MIC2171BU
RB160L-40
DO-214AA
SOT-223 Top View
GND
Barrel Connector
Top View
Rev 2.0
U27
VIN
SHDN
GROUND
SW
FB
5VD
L2 33uH
MIC4576
D9
SCHOTTKY RECTIFIER
C60
10uF
Rev 2.0
C66
330uF
10V
E-CASE
C67
330uF
10V
E-CASE
C68
330uF
10V
E-CASE
VCC5
C65
0.1uF
U29
IN
OUT
GND
LDO-3.3
Micrel MIC5209-3.3BS
Rev 2.0
C71
10uF
16V
C-CASE
Rev 1.1
VCC3
C64
0.1uF
Rev. 1.1: Power changed to
a switching regulator.
Rev 2.0
M24V
M70V
R100
0
KOA RM73Z2B, 5%, 1W
R97
0
KOA RM73Z2B, 5%, 1W
SOT-23 Top View
RHOM RSZ5228B
Rev. 1.1: Pinout corrected
for this part.
T1
T1:D
T1:C
T1:A
T1:B
CTRTAP
D5
General Semi ES2D
M70VD
M70VR
C56
22uF
35V
E-CASE
AVX TPSE226M035R0300
MVCAP
C57
22uF
35V
E-CASE
AVX TPSE226M035R0300
D6
General Semi ES2D
M24VD
M24VR
D7
General Semi ES2D
C58
22uF
35V
E-CASE
AVX TPSE226M035R0300
R98
13.7K
1206
M70RR
R99
13.7K
1206
Flyback Transformer
Beckman HM00-98519
VCC12
D3
DIODE ZENER
General Semi SMZJ3797B
VCC12DX
Rev. 1.1: Pinout corrected for
this part. Pin 1 changed to pin 2.
D2
DIODE ZENER
ROHM RSZ5228B
VCC12D
D4
DIODE
General Semi ES2D
VCC12SW
U24
IN
SW
COMP
GND
FB
SLIC REGULATOR
Micrel MIC2171BU
C46
22uF
35V
E-CASE
AVX TPSE226M035R0300
C47
22uF
35V
E-CASE
AVX TPSE226M035R0300
2171FB
R95
487
C52
3300pF
1206
50V
AVX 12065C104MATMA
R94
3.32K
1206
COMPR
C50
0.22uF
1206
AVX 12063C224MATMA
U23
OP AMP
Micrel MIC6211BM5
R96
10K
C48
220pF
805
50V
AVX 08055C221MATMA
C51
0.01uF
SOT-23-5
MIC6211BM5
CR8
LED SMT
LEDM70V
R243
5.6K
KOA RM73B3A, 5%, 1W
P22
Banana Jack
CR9
LED SMT
LEDM24V
R244
1.5K
KOA RM73B3A, 5%, 1W
P23
Banana Jack
CR10
LED SMT
LEDM5V
R247
220
P24
Banana Jack
CR11
LED SMT
LEDVCC3
R256
68
P25
Banana Jack
CR12
LED SMT
LEDVCC5
R265
220
P28
Banana Jack
P29
Banana Jack
(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved
Design Name
Am186CC Customer Dev. Platform (Main Board) - Power Supply
Size
16x125
Schematic Sheet Name
POWER.SCH
Rev
2.1
Date: Friday, February 05, 1999
Sheet 14 of 15

## MULTIDROP SWITCH

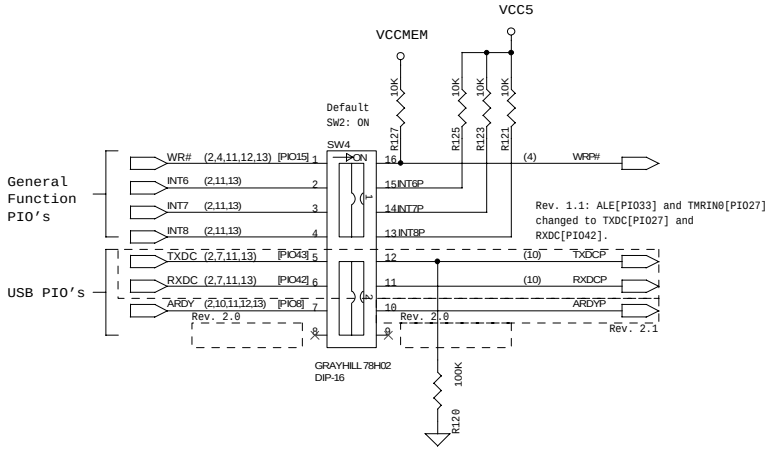
NOTE: SET SWITCH ON WHEN USING MULTIDROP MODE (THE RS422 TRANSCEIVERS WILL BE REMOVED IN THIS MODE)

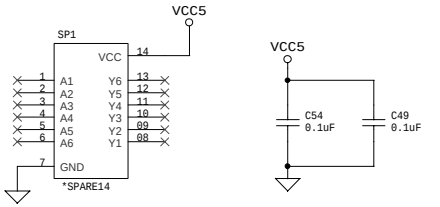
Default
SW1: OFF
SW4: OFF
SW5: OFF
SW6: OFF

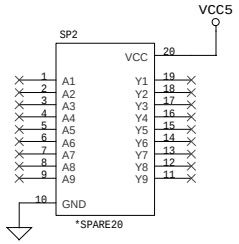


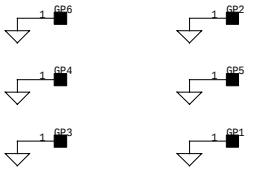

## PIO ISOLATION SWITCH

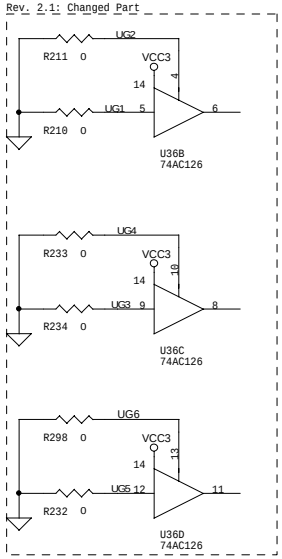
NOTE: TURN SWITCH TO OFF POSITION IF PIO ISOLATION IS DESIRED.

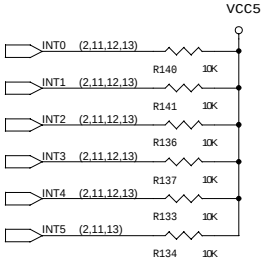


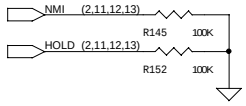






Design Name
Am186CC Customer Dev. Platform (Main Board) - Miscellaneous

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | MISC.SCH | 2.1 |

Date: Friday, February 05, 1999 Sheet 15 of 15

**Table of Contents**


Page 1: Cover Sheet (COVER.SCH)
Page 2: Main Board Connectors (CONNECTOR.SCH)
Page 3: Ethernet Page 1 (ETHERNET1.SCH)
Page 4: Ethernet Page 2 (ETHERNET2.SCH)
Page 5: ISDN S Interface (ISDN_S.SCH)
Page 6: ISDN U Interface (ISDN_U.SCH)
Page 7: RSLIC Page 1 (POTS_RSLIC1.SCH)
Page 8: RSLIC Page 2 (POTS_RSLIC2.SCH)
Page 9: DSLAC (POTS_DSLAC.SCH)
Page 10: Miscellaneous (MISC.SCH)


# Am186CC/CH/CU Customer Development Platform Schematics

# Router/ISDN Development Module

**Rev 1.0:** Original design

**Rev 2.0:**
Sheet 2: Change buffer control
Sheet 4: Change Packet SRAM to 64Kx16
Change PAL routing for Ethernet and Buffer control
Add Ethernet LED0 and delete LED2
Sheet 5: Correct S/T interface RJ45 pinout
Add S/T protection circuitry
Change S/T transceiver to 16-bit addressing
Remove ISDN diagnostic LED
Sheet 6: Add S/T interface names to U transceiver
Sheet 9: Add Time Slot Control buffering

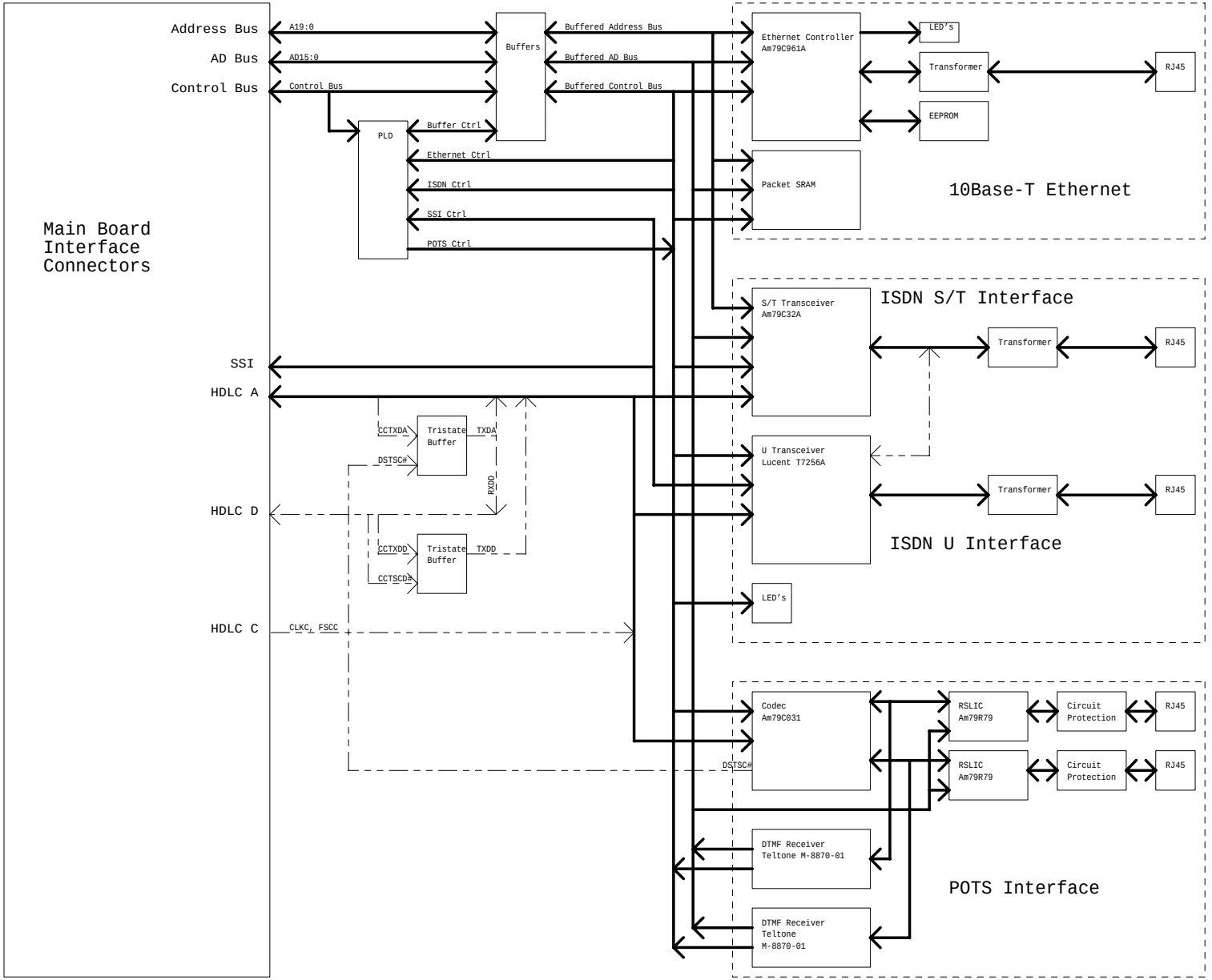
**Rev 2.1:**
Sheet 3: Change data buffer control
Added RING_IN PIO's thru buffer
Sheet 5: Change PAL for DTMF and Data Buffer control
Changed Packet SRAM select circuitry
Sheet 6: Change S/T Interrupt to INT6
Sheet 10: Added DSLAC clocking jumper select
Swapped DTMF data bit order



Design Name
Router/ISDN Development Module - Cover Page

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | COVER.SCH | 2.1 |

Date: Friday, June 04, 1999 Sheet 1 of 11

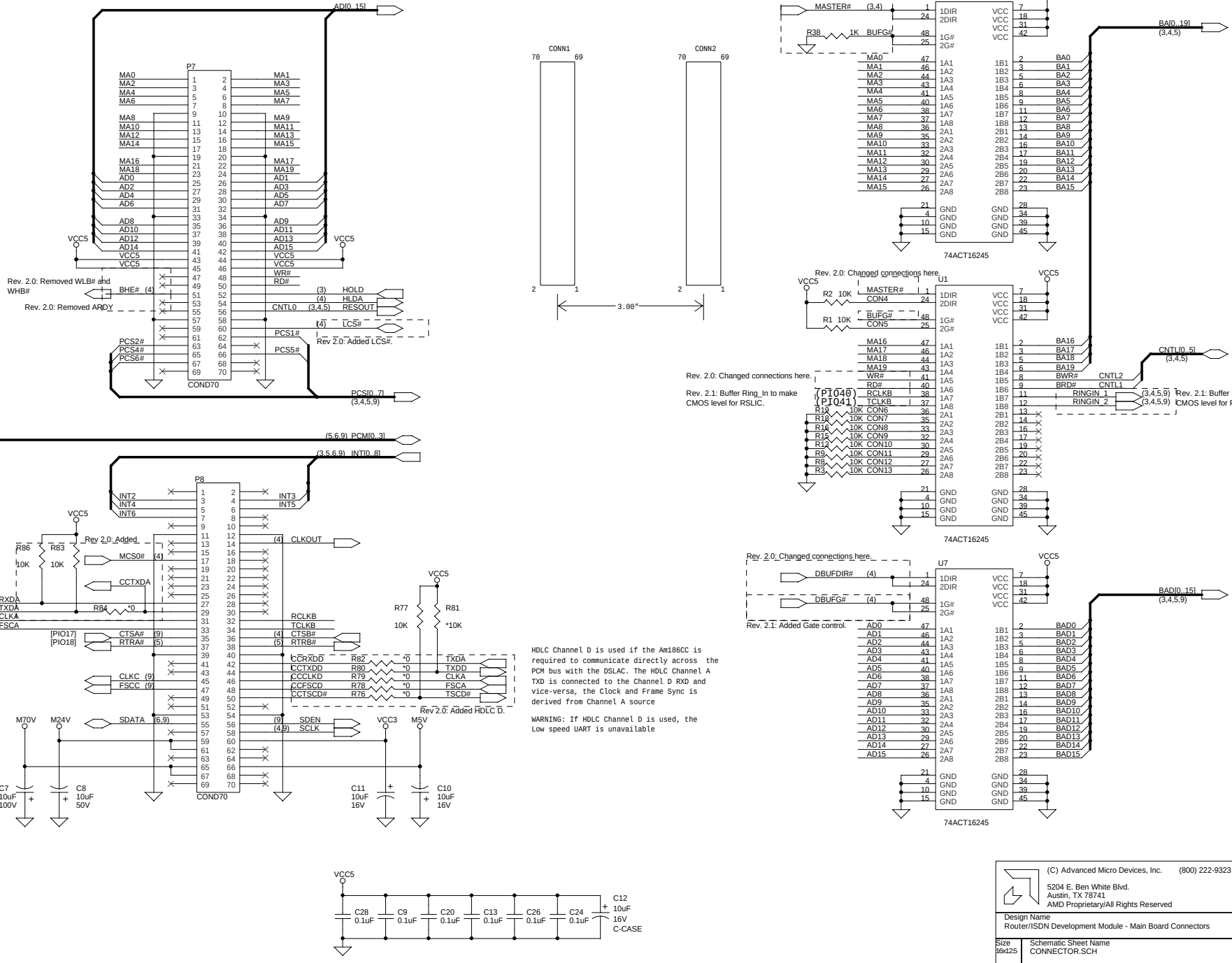





Design Name
Router/ISDN Development Module - Block Diagram

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | BLOCK DIAGRAM | 2.1 |

Date: Monday, May 31, 1999 Sheet 2 of 11

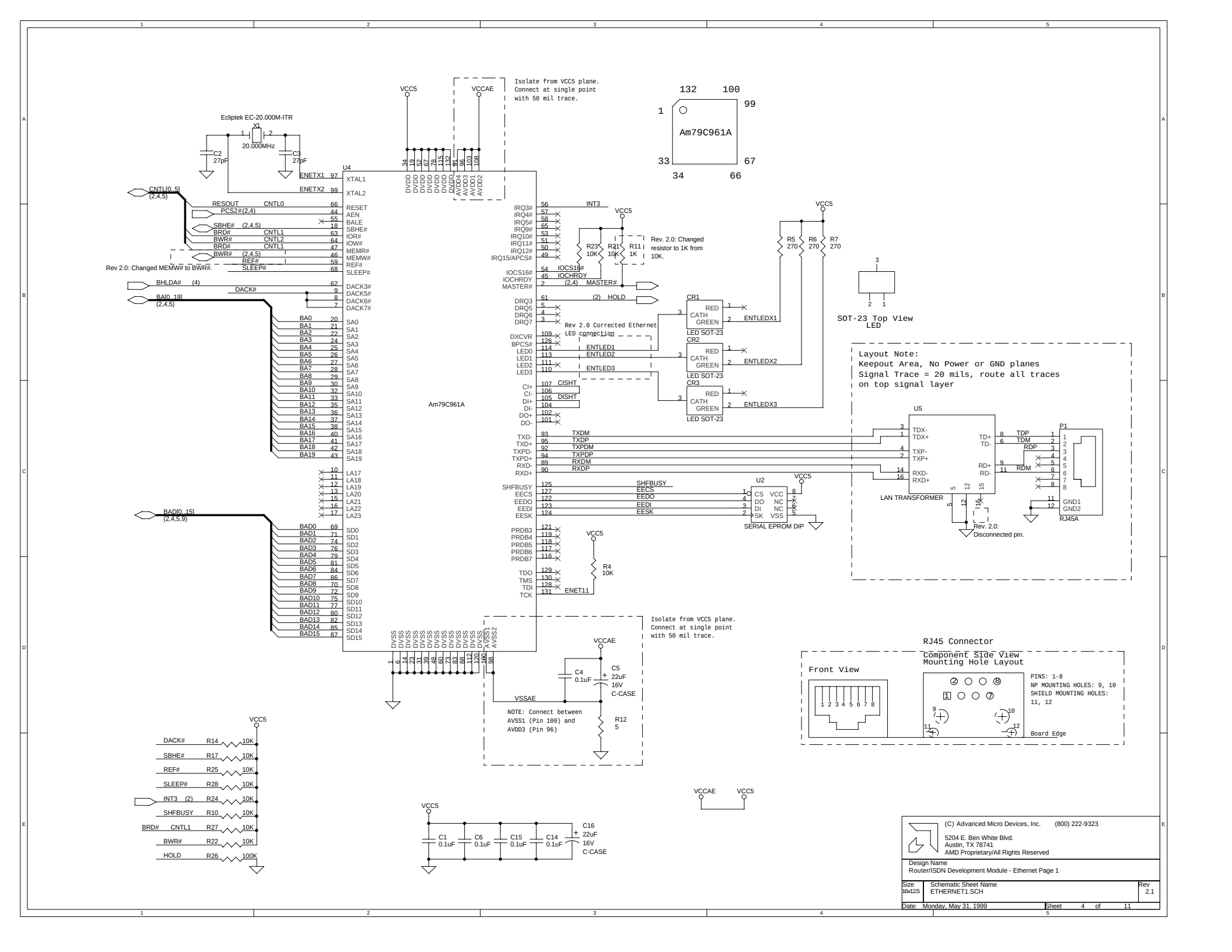




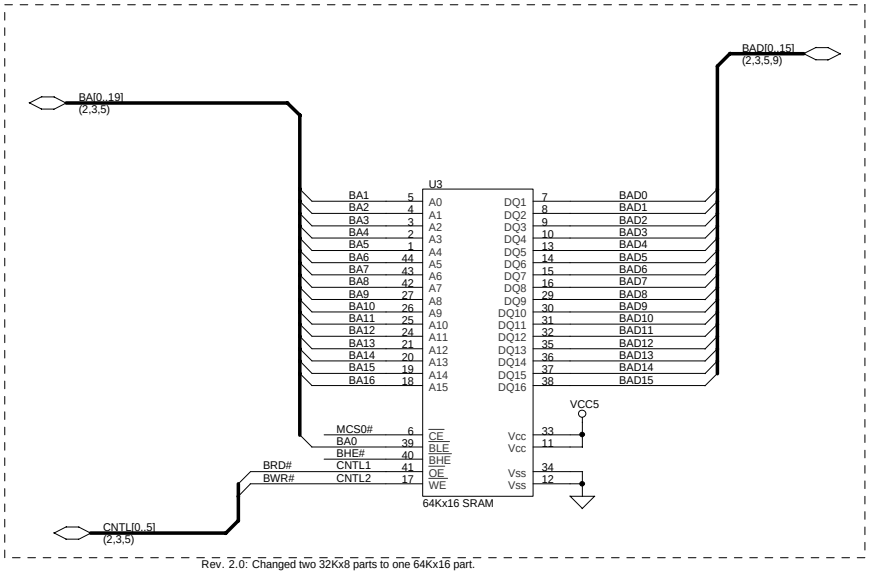

Design Name
Router/ISDN Development Module - Main Board Connectors

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | CONNECTOR.SCH | 2.1 |

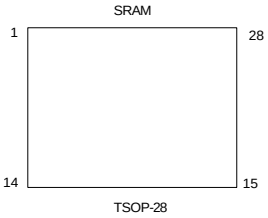
Date: Monday, May 31, 1999 Sheet 3 of 11

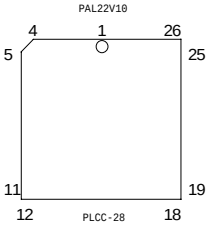

Ecliptek EC-20.000M-ITR
X1
20.000MHz
C2
27pF
C3
27pF
U4
Am79C961A
ENETX1
ENETX2
XTAL1
XTAL2
CNTL[0..5]
(2,4,5)
RESOUT
PCS2#(2,4)
SBHE# (2,4,5)
BRD# CNTL1
BWR# CNTL2
BRD# CNTL1
BWR# (2,4,5)
REF#
SLEEP#
RESET
AEN
BALE
SBHE#
IOR#
IOW#
MEMR#
MEMW#
REF#
SLEEP#
Rev 2.0: Changed MEMW# to BWR#.
BHLDA# (4)
DACK#
BA[0..19]
(2,4,5)
DACK3#
DACK5#
DACK6#
DACK7#
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
SA18
SA19
LA17
LA18
LA19
LA20
LA21
LA22
LA23
BAD[0..15]
(2,4,5,9)
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
DVDD
DVSS
AVDD1
AVDD2
AVDD3
AVDD4
AVSS1
AVSS2
VCC5
VCCAE
Isolate from VCC5 plane.
Connect at single point
with 50 mil trace.
132
100
1
99
Am79C961A
33
67
34
66
IRQ3#
IRQ4#
IRQ5#
IRQ9#
IRQ10#
IRQ11#
IRQ12#
IRQ15/APCS#
INT3
R23
10K
R21
10K
R11
1K
Rev. 2.0: Changed
resistor to 1K from
10K.
IOCS16#
IOCHRDY
MASTER#
IOCS16#
IOCHRDY
(2,4) MASTER#
DRQ3
DRQ5
DRQ6
DRQ7
(2) HOLD
Rev 2.0 Corrected Ethernet
LED connection
DXCVR
BPCS#
LED0
LED1
LED2
LED3
ENTLED1
ENTLED2
ENTLED3
CI+
CI-
DI+
DI-
DO+
DO-
CISHT
DISHT
TXD-
TXD+
TXPD-
TXPD+
RXD-
RXD+
TXDM
TXDP
TXPDM
TXPDP
RXDM
RXDP
SHFBUSY
EECS
EEDO
EEDI
EESK
PRDB3
PRDB4
PRDB5
PRDB6
PRDB7
TDO
TMS
TDI
TCK
ENET11
R4
10K
CR1
CR2
CR3
RED
CATH
GREEN
LED SOT-23
ENTLEDX1
ENTLEDX2
ENTLEDX3
R5
270
R6
270
R7
270
SOT-23 Top View
LED
Layout Note:
Keepout Area, No Power or GND planes
Signal Trace = 20 mils, route all traces
on top signal layer
U5
TDX-
TDX+
TXP-
TXP+
RXD-
RXD+
TD+
TD-
RD+
RD-
TDP
TDM
RDP
RDM
LAN TRANSFORMER
P1
GND1
GND2
RJ45A
Rev. 2.0:
Disconnected pin.
U2
CS
DO
DI
SK
VCC
NC
NC
VSS
SERIAL EPROM DIP
Isolate from VCC5 plane.
Connect at single point
with 50 mil trace.
C4
0.1uF
C5
22uF
16V
C-CASE
VSSAE
NOTE: Connect between
AVSS1 (Pin 100) and
AVDD3 (Pin 96)
R12
5
RJ45 Connector
Component Side View
Mounting Hole Layout
Front View
1 2 3 4 5 6 7 8
PINS: 1-8
NP MOUNTING HOLES: 9, 10
SHIELD MOUNTING HOLES:
11, 12
Board Edge
DACK# R14 10K
SBHE# R17 10K
REF# R25 10K
SLEEP# R28 10K
INT3 (2) R24 10K
SHFBUSY R10 10K
BRD# CNTL1 R27 10K
BWR# R22 10K
HOLD R26 100K
C1
0.1uF
C6
0.1uF
C15
0.1uF
C14
0.1uF
C16
22uF
16V
C-CASE
VCCAE
VCC5
(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved
Design Name
Router/ISDN Development Module - Ethernet Page 1
Size
16x125
Schematic Sheet Name
ETHERNET1.SCH
Rev
2.1
Date: Monday, May 31, 1999
Sheet 4 of 11

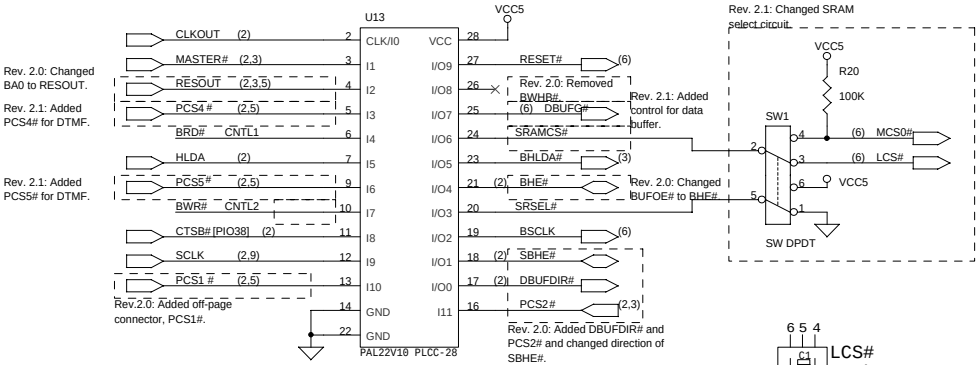
# PCNetISA SRAM - Packet Buffer
# 64K x 16

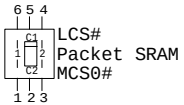



Rev. 2.0: Changed two 32Kx8 parts to one 64Kx16 part.

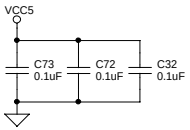



Grayhill 76SD01




## PAL DESCRIPTION

```
BHLDA# = HLDA + MASTER;
```

BHLDA# is an inverted HLDA and must remain active while MASTER is asserted (If DRAM is used as main system memory, the 186CC will deassert HLDA when requesting a refresh).

```
SBHE# = BHE + DBHE;
(ENABLED_BY /MASTER#)
```

SBHE# is an output which is delayed to extend after the rising edge of the command when 186CC has bus, and is an input which drives BHE# when PCNETISA has the bus. It is clocked by CLKOUT.

```
DBUFG = [PCS1 + PCS2 + PCS4 + PCS5]
      + [MASTER * SRAMCS * MAIN]
      + [/MASTER * SRAMCS * /MAIN]
```

DBUFG enables the gate of the tristate data buffer only when data is being transferred between the CDP main and module.

```
DBUFDIR# = MASTER * BWR
         + /MASTER * BRD
```

DBUFDIR# points the data buffer towards the 186CC on reads from PCNETISA and 79C32 when the 186CC has the bus and during PCNETISA writes when PCNETISA has the bus.

```
BSCLK = SCLK;
(ENABLED_BY PIO38)
```

BSCLK is the 186CC SCLK which is controlled by PIO38 to tristate BSCLK when the T7256 is not being accessed.

```
SRAMCS# = 1
(ENABLED_BY /MASTER#)
```

SRAMCS# is ACTIVE when PCNETISA has bus.

```
BHE#
(ENABLED_BY MASTER#)
```

BHE# is a gated SBHE# output from PCNETISA.

```
RESET# = RESOUT
```

RESET# is an inverted RESOUT.



Design Name
Router/ISDN Development Module - Ethernet Page 2

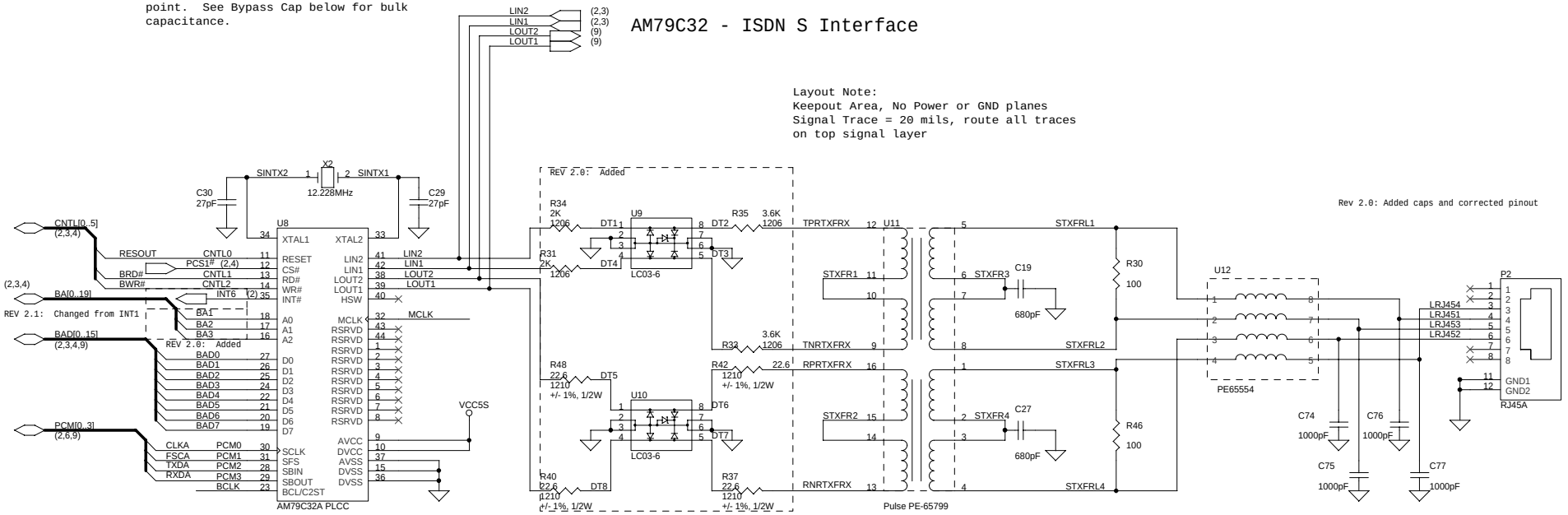
| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | ETHERNET2.SCH | 2.1 |

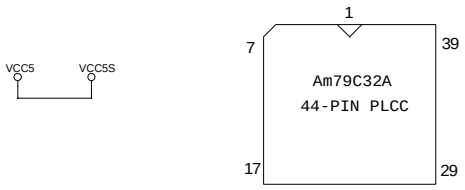
Date: Monday, May 31, 1999 Sheet 5 of 11

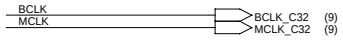
Layout Note:
79C32 is a single substrate device.
Separate Vcc plance for this area,
connected to System Vcc through single
point. See Bypass Cap below for bulk
capacitance.

# AM79C32 - ISDN S Interface

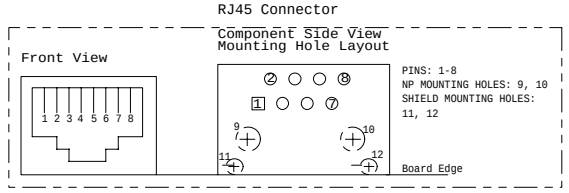
Layout Note:
Keepout Area, No Power or GND planes
Signal Trace = 20 mils, route all traces
on top signal layer

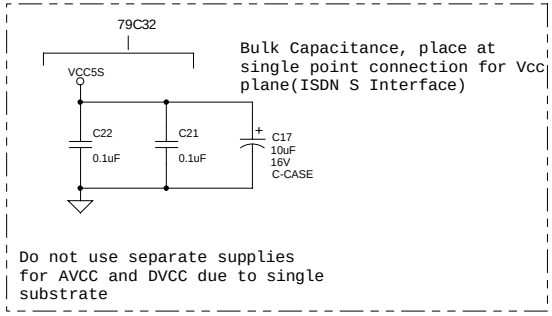


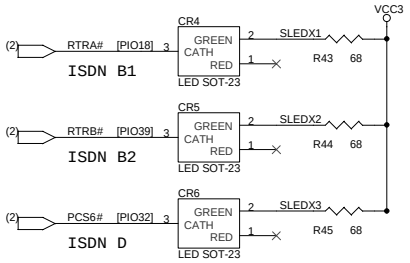




MCLK_C32 drives MCLK_DSLAC when ISDN S
Interface is functional. Alternate
source for MCLK_DSLAC is T7237/U
Interface.
Note - MCLK_C32 is controlled by the
PAL22V10




## LEDs Connected to PIOs





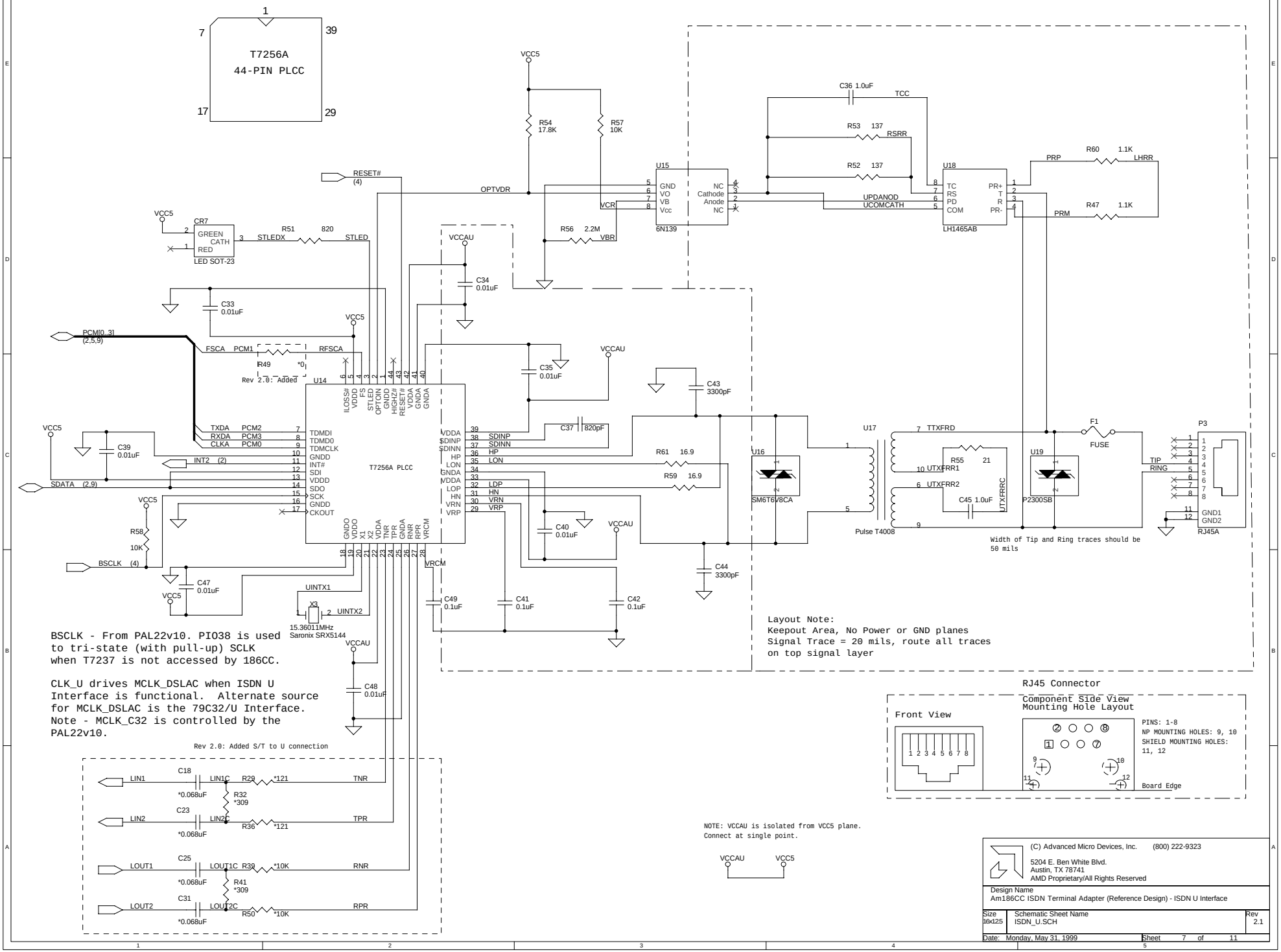


Design Name
Router/ISDN Development Module - ISDN S Interface

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | ISDN_S.SCH | 2.1 |

Date: Monday, May 31, 1999 Sheet 6 of 11

# U Interface




BSCLK - From PAL22v10. PIO38 is used to tri-state (with pull-up) SCLK when T7237 is not accessed by 186CC.

CLK_U drives MCLK_DSLAC when ISDN U Interface is functional. Alternate source for MCLK_DSLAC is the 79C32/U Interface. Note - MCLK_C32 is controlled by the PAL22v10.

Rev 2.0: Added S/T to U connection




Layout Note:
Keepout Area, No Power or GND planes
Signal Trace = 20 mils, route all traces
on top signal layer

RJ45 Connector
Component Side View
Mounting Hole Layout




NOTE: VCCAU is isolated from VCC5 plane.
Connect at single point.

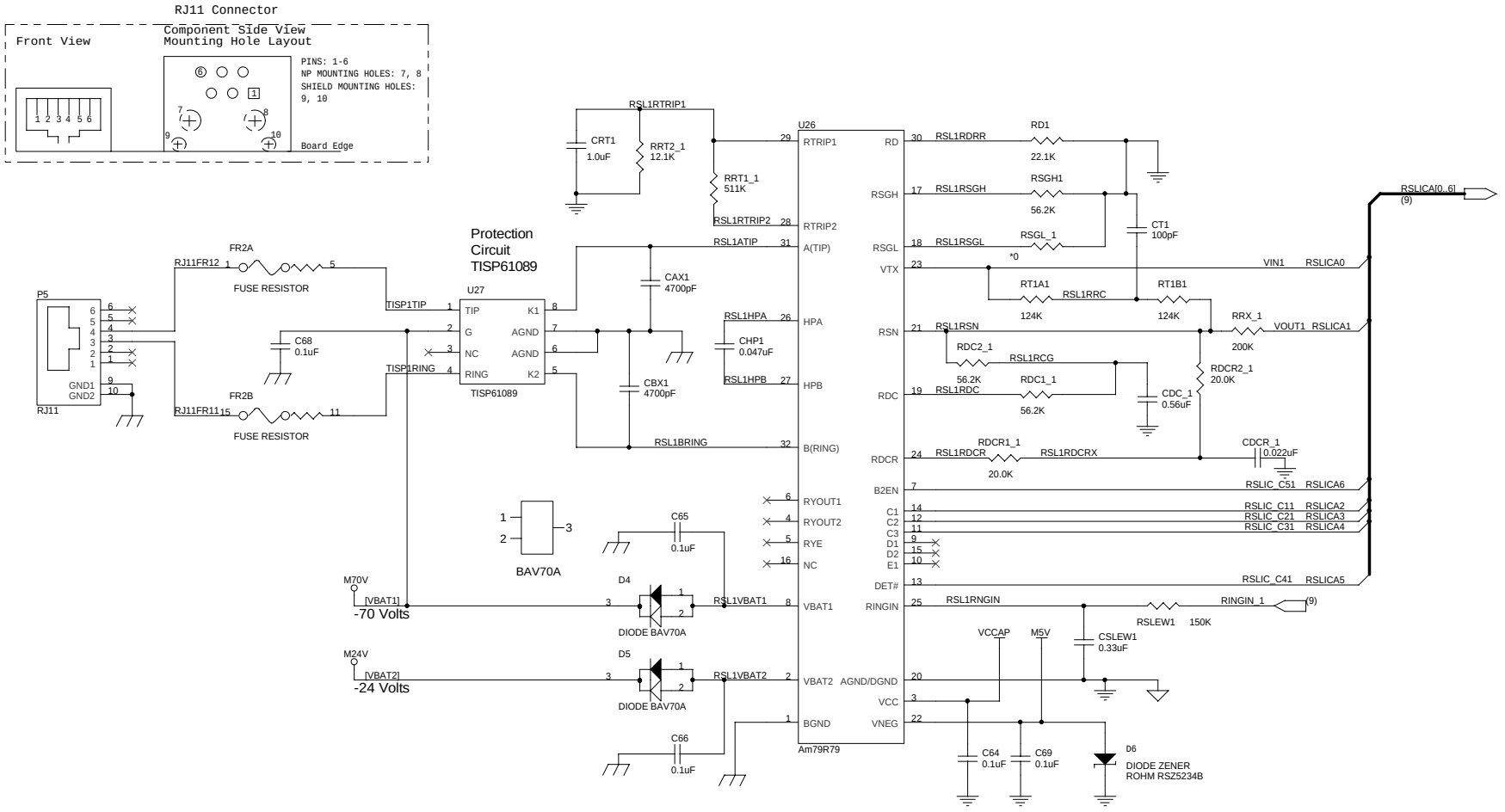
VCCAU VCC5



Design Name
Am186CC ISDN Terminal Adapter (Reference Design) - ISDN U Interface

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | ISDN_U.SCH | 2.1 |

Date: Monday, May 31, 1999 Sheet 7 of 11

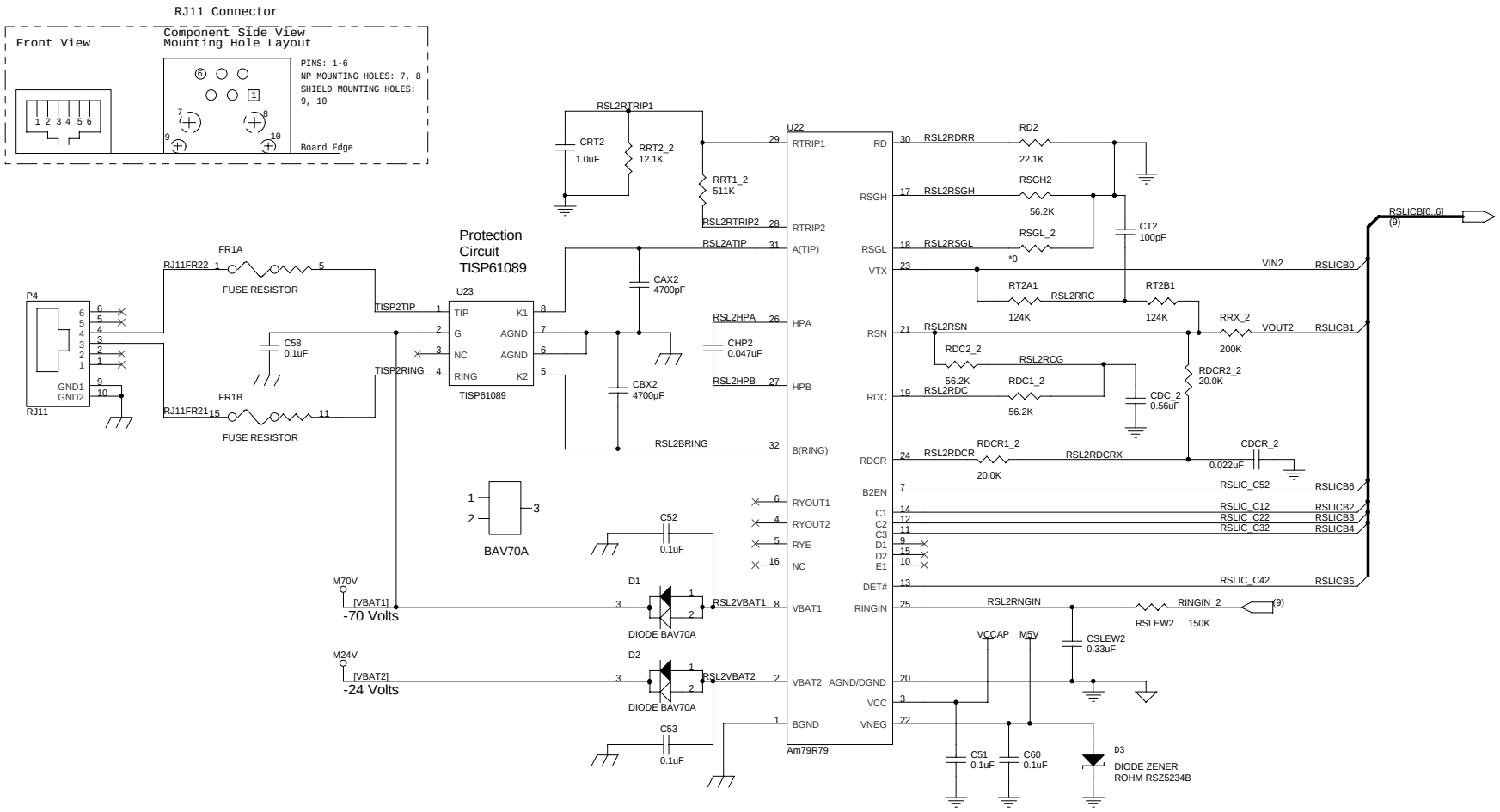





Design Name
Am186CC ISDN Terminal Adapter (Reference Design) - RSLIC Page 1

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | POTS_RSLIC1.SCH | 2.1 |

Date: Monday, May 31, 1999 Sheet 8 of 11



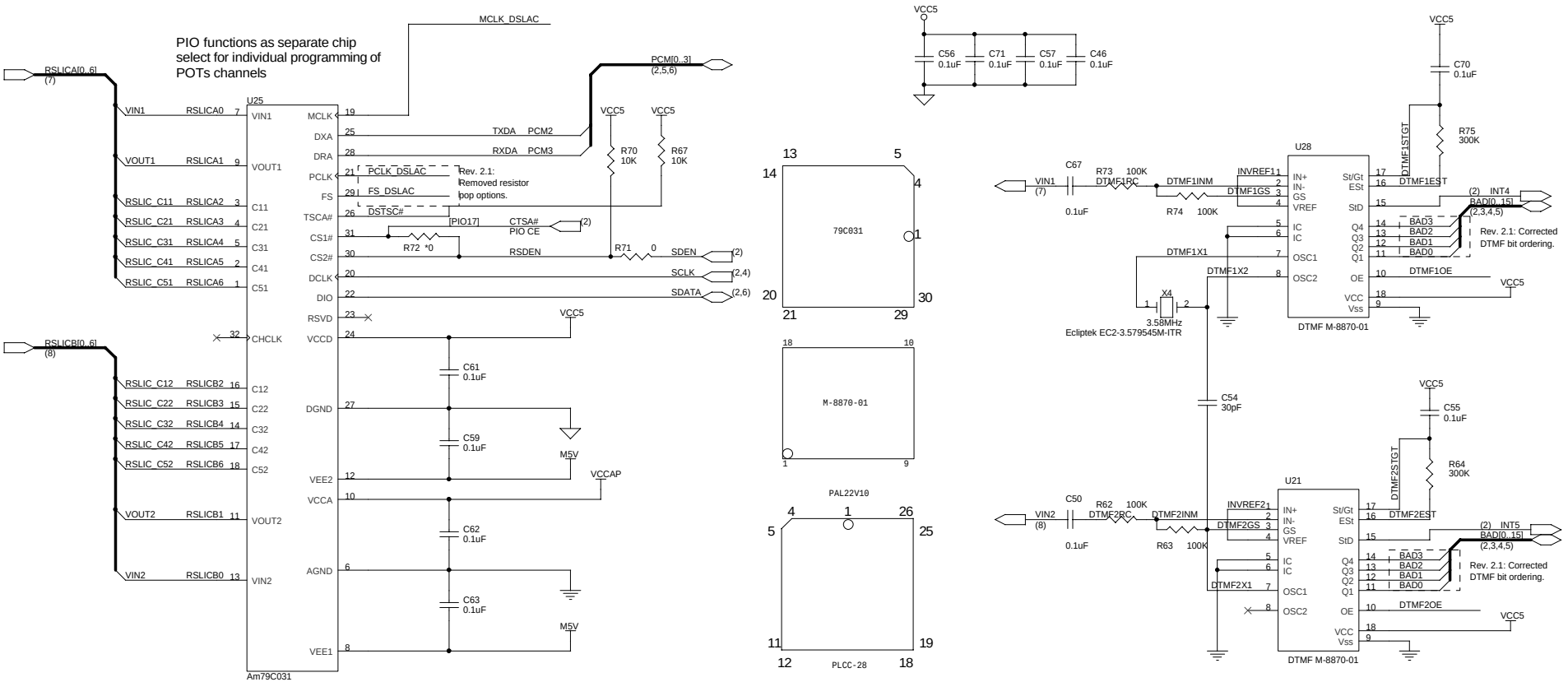

NOTE: VSSCP and VSSAP 50 mil traces connected to GND plane at single point.
No VCC or GND plane in this area.
M70V is a 50 mil trace.
M24V is a 50 mil trace.
M5V is a 50 mil trace.
VCCAP is a 50 mil trace connected to VCC5 at a single point.



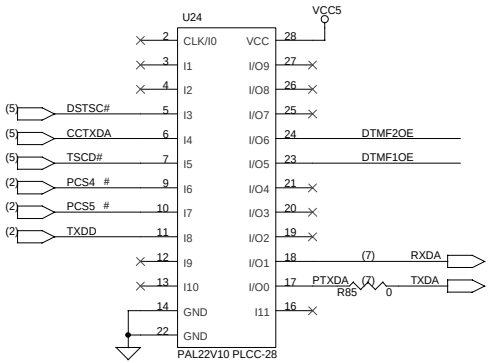
Design Name
Am186CC ISDN Terminal Adapter (Reference Design) - RSLIC Page 2

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | POTS_RSLIC2.SCH | 2.1 |

Date: Monday, May 31, 1999 Sheet 9 of 11

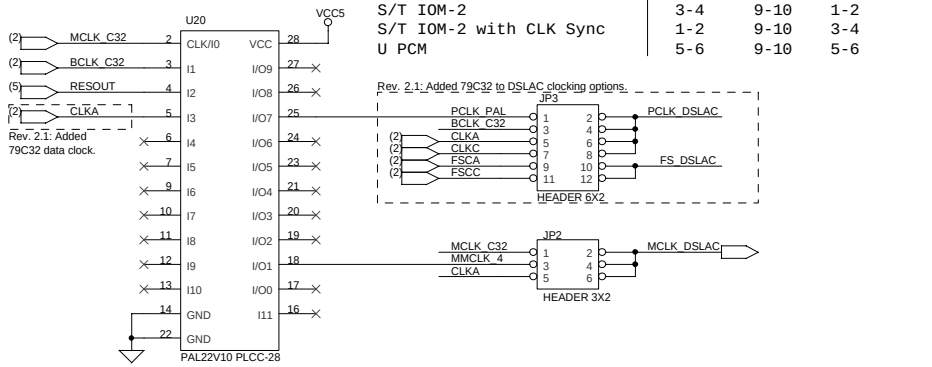



| DSLAC Clocking Options Mode | PCLK_DS | FS_DS | MCLK_DS |
|---|---|---|---|
| S/T SBP | 5-6 | 9-10 | 1-2 |
| S/T SBP with CLK Sync | 1-2 | 9-10 | 3-4 |
| S/T IOM-2 with GCI/PCM Conv. | 7-8 | 11-12 | 3-4 |
| S/T IOM-2 | 3-4 | 9-10 | 1-2 |
| S/T IOM-2 with CLK Sync | 1-2 | 9-10 | 3-4 |
| U PCM | 5-6 | 9-10 | 5-6 |




## U24 PAL DESCRIPTION

| | |
|---|---|
| DTMF2OE = PCS5; | DTMF2OE is an inverted PCS5#/PIO2 used for DTMF OE. |
| DTMF1OE = PCS4; | DTMF1OE is an inverted PCS5#/PIO2 used for DTMF OE. |
| TXDA = CCTXDA; ENABLED_BY DSTSC | TXDA is the Am186CC TXDA output when the DSLAC is NOT transmitting on the PCM bus. This is needed in case the HDLC TSA's are configured in muxed mode and a POTS line is needed. The Am186CC TXDA output will be tristated when the POTS interface is transmitting. |
| RXDA = TXDD; ENABLED_BY TSCD | RXDA is the Am186CC TXDD output when PCM channel D is transmitting. This is used if the Am186CC is required to transmit data to the DSLAC. |



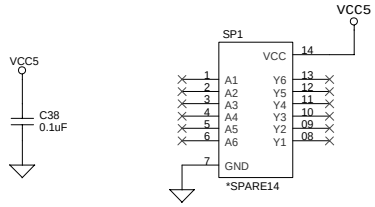

U20 is used to define the clocking used for the DSLAC device. The DSLAC is a PCM device only and may require clocking modifications for PCLK, FS, and MCLK, if PCLK is asynchronous to MCLK. Clocking options provided allow synchronous and asynchronous clocking based on clock masters running in PCM and GCI mode.
Options include :
1) GCI master - Use BCLK, FS, and MCLK outputs from master device.
2) GCI master - Use PAL to derive correct timing from GCI master for MCLK and PCLK. FS is a direct connection from GCI master.
3) GCI/PCM conversion - PCLK and FS are generated from the CLKC and FSCC outputs from the Am186CC device.
4) PCM master - PCLK ans FS are a direct connection from the PCM master device.



Design Name: Am186CC ISDN Terminal Adapter (Reference Design) - DSLAC

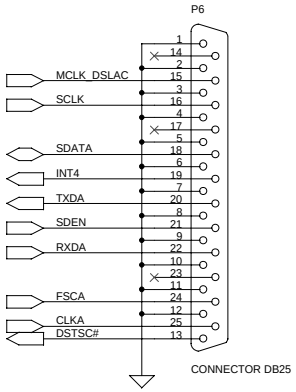
| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | POTS_DSLAC.SCH | 2.1 |

Date: Monday, May 31, 1999 Sheet 10 of 11





LNB Connection




If using the external LNB board to interface to a SLAC device, all connections on JP2 and JP3 must be removed.

## PIO RESOURCE ASSIGNMENTS

| PIO | SIGNAL | FUNCTIONALITY |
|---|---|---|
| PIO18 | RTRA | LED ISDN B1 |
| PIO39 | RTR_B# | LED ISDN B2 |
| PIO32 | PCS6# | LED ISDN D |
| PIO17 | CTSA# | CE FOR DSLAC |
| PIO38 | CTS_B | T7256 SCLK CNTL |
| PIO40 | RCLK_B | POTS LINE 1 RINGING SIGNAL |
| PIO41 | TCLK_B | POTS LINE 2 RINGING SIGNAL |

## CHIP SELECT ASSIGNMENTS

| CHIP SELECTS | DEVICE | INTERFACE |
|---|---|---|
| MCS0# | SRAM | 16 BIT |
| PCS1# | 79C32 | 16 BIT |
| PCS2# | PCNetISA II | 8 BIT |
| PCS4# | DTMF1 OE | 8 BIT |
| PCS5# | DTMF2 OE | 8 BIT |

## INTERRUPT ASSIGNMENTS

| INTERRUPT | DEVICE | POLARITY |
|---|---|---|
| INT2 | T7256 | ACTIVE LOW EDGE |
| INT3 | PCNetISA II | ACTIVE HIGH EDGE |
| INT6 | 79C32 | ACTIVE LOW EDGE |



Design Name
Router/ISDN Development Module - Miscellaneous

| Size | Schematic Sheet Name | Rev |
|---|---|---|
| 16x125 | MISC.SCH | 2.1 |

Date: Monday, May 31, 1999 Sheet 11 of 11