AMENDMENT

Am186™CC/CH/CU

Microcontrollers Register Set Manual

This document amends the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, order #21916B. It consists of these parts:

- "Documentation Defects and Corrections" on page 1 lists corrections to be made in page number order.
- "Changed Figure" on page 12 provides an improved version of Figure 5-1 of the manual.
- An Index is included at the end of this amendment.

DOCUMENTATION DEFECTS AND CORRECTIONS

Table 1 on page 2 lists defects that have been found in the *Am186™CC/CH/CU Microcontrollers Register Set Manual,* order #21916B. Defects are listed in page order. Each entry lists the following:

- page number
- item to be corrected
- original text (or description of text to change)
- corrected text (or description of change to make)
- comment explaining the change

Entries that correct text in a diagram or figure do not contain the entire diagram or figure. If graphical information is changed, the table refers to the page in this amendment where the changed figure can be found.

Square brackets ([ ]) are used to indicate a description of the text or change to be made, as opposed to the actual text to change.

Unchanged portions of a paragraph are replaced by an ellipsis (...) in entries where this might make the change easier to find. The whole paragraph is included if it is useful for understanding why the change was made.

Publication# **21916** Rev: **B** Amendment/**1**
Issue Date: **February 2000**

Table 1. Corrections to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, Rev. B

Page	Item	Original Text	Change To	Comment
Chapter 3 DMA Registers				
3-14	SmartDMA™ Channel Pair 0 Control (SD0CON) and SmartDMA Channel Pair 1 Control (SD1CON) registers, bit 3 POLL in bit diagram	POLL R/W C 0	POLL W C 0	The POLL bit always reads back as 0.
3-15	SmartDMA Channel Pair 0 Control (SD0CON) and SmartDMA Channel Pair 1 Control (SD1CON) registers, bit 1 TXST description, last paragraph	Clearing the TXST bit has no effect while a request is pending on the channel. Before clearing the TXST bit, make sure the requesting HDLC channel is stopped.	Clearing the TXST bit has no effect while a request is pending on the channel. Before clearing the TXST bit, make sure the requesting HDLC channel is stopped. If the requesting HDLC channel is stopped by an error status, the error handler should clear the TXST bit before clearing the error status bit. Otherwise the SmartDMA channel request might be reasserted before software can clear the TXST bit.	
	SmartDMA Channel Pair 0 Control (SD0CON) and SmartDMA Channel Pair 1 Control (SD1CON) registers, bit 0 RXST description, last paragraph	Clearing the RXST bit has no effect while a request is pending on the channel. Before clearing the RXST bit, make sure the requesting HDLC channel is stopped.	Clearing the RXST bit has no effect while a request is pending on the channel. Before clearing the RXST bit, make sure the requesting HDLC channel is stopped. If the requesting HDLC channel is stopped by an error status, the error handler should clear the RXST bit before clearing the error status bit. Otherwise the SmartDMA channel request might be reasserted before software can clear the RXST bit.	
3-17	SmartDMA Channel Pair 2 Control (SD2CON) and SmartDMA Channel Pair 3 Control (SD3CON) registers, bit 3 POLL in bit diagram	POLL R/W C 0	POLL W C 0	The POLL bit always reads back as 0.

Table 1. Corrections to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, Rev. B (Continued)

Page	Item	Original Text	Change To	Comment
3-18	SmartDMA Channel Pair 2 Control (SD2CON) and SmartDMA Channel Pair 3 Control (SD3CON) registers, bit 1 TXST description, last paragraph	Clearing the TXST bit has no effect while a request is pending on the channel. Before clearing the TXST bit, make sure the requesting peripheral (HDLC channel or USB endpoint) is stopped.	Clearing the TXST bit has no effect while a request is pending on the channel. Before clearing the TXST bit, make sure the requesting peripheral (HDLC channel or USB endpoint) is stopped. If the requesting peripheral is stopped by an error status, the error handler should clear the TXST bit before clearing the error status bit. Otherwise the SmartDMA channel request might be reasserted before software can clear the TXST bit.	
	SmartDMA Channel Pair 2 Control (SD2CON) and SmartDMA Channel Pair 3 Control (SD3CON) registers, bit 0 RXST description, last paragraph	Clearing the RXST bit has no effect while a request is pending on the channel. Before clearing the RXST bit, make sure the requesting peripheral (HDLC channel or USB endpoint) is stopped.	Clearing the RXST bit has no effect while a request is pending on the channel. Before clearing the RXST bit, make sure the requesting peripheral (HDLC channel or USB endpoint) is stopped. If the requesting peripheral is stopped by an error status, the error handler should clear the RXST bit before clearing the error status bit. Otherwise the SmartDMA channel request might be reasserted before software can clear the RXST bit.	
3-20 3-21 3-22 3-23	Programming Notes (for SDxTRCAL, SDxTRAH, SDxRRCAL, and SDxRRAH registers)	—	[Add new programming note:] The SmartDMA channel descriptor rings must reside in 16-bit memory. The buffers pointed to by the descriptors can be in either 8-bit or 16-bit memory.	

Table 1. Corrections to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, Rev. B (Continued)

Page	Item	Original Text	Change To	Comment
Chapter 4 USB Registers (Am186CC and Am186CU Microcontrollers Only)				
4-18	Control Endpoint Control/Status (CNTCTL) register, offset 200h, diagram bit 7 column and bit 7 description	[Bit diagram, bit 7 column:] *Res* R — 0 [Bit 7 description:] 7 Res **Reserved** For compatibility with future devices, always write this bit field with its chip reset default value.	[Bit diagram, bit 7 column:] HNDSHK R S/C 0 [Bit 7 description:] 7 HNDSHK **Data Handshake Indicator** The HNDSHK bit indicates the USB handshake phase for this endpoint for debugging purposes. 0 = DATA1 handshake token not present. 1 = DATA1 handshake token present. If a packet is being transferred when this bit is read, then the bit returns 1 if the packet had a USB handshake token of DATA1, and 0 if not. If no packet is being transferred, then this bit returns 1 if the next packet is to be transferred on DATA1, and 0 if not. This bit always changes state when a packet is acknowledged (IN direction) or when the hardware receives an acknowledgment (OUT direction). The HNDSHK bit is not available in parts released prior to revision C1. For processor revision information, see the PRL register description on page 16-4 [of the manual, and on page 11 of this amendment].	
4-27	Interrupt Endpoint Control/Status (IEPCTL) register, offset 210h, bit diagram bit 7 column and bit 7 description			
4-33	x Endpoint Control/ Status (xEPCTL) registers, offsets 220h, 230h, 240h, 250h,bit diagram bit 7 column and bit 7 description			

Table 1. Corrections to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, Rev. B (Continued)

Page	Item	Original Text	Change To	Comment
Chapter 5 Asynchronous Serial Port (UART) Registers				
5-3	High-Speed Serial Port Control 0 (HSPCON0) register, bit 12 RSIE description	The bits in the HSPSTAT register that generate receive status interrupts are MATCH, OERIM, IDLE, PER, OER, FER, AB, and BRK...	The bits in the HSPSTAT register that generate receive status interrupts are MATCH, BRKIM, OERIM, ABDONE, IDLE, PER, OER, FER, AB, and BRK...	Add BRKIM and ABDONE bits.
5-5	High-Speed Serial Port Control 1 (HSPCON1) register, bit 15 TFEN and bit 14 RFEN description	When setting the... [TFEN or RFEN] bit, software should also set the TFLUSH bit to ensure that the FIFO is initialized.	[Delete sentence.]	The FIFOs are automatically flushed when disabled.
	High-Speed Serial Port Control 1 (HSPCON1) register, bit 13 TFLUSH description	[Existing text.]	[Add the following paragraphs:] Flushing the transmit FIFO also clears the HSPTXD register, but not the transmit shift register. The transmit FIFO is automatically flushed when the TFEN bit is cleared, or when the TMODE bit is cleared in the HSPCON0 register.	
	High-Speed Serial Port Control 1 (HSPCON1) register, bit 12 RFLUSH description	[Existing text.]	[Add the following paragraph:] Flushing the receive FIFO also clears the HSPRXD register. The receive FIFO is automatically flushed when the RFEN bit is cleared, or when the RMODE bit is cleared in the HSPCON0 register.	

Table 1. Corrections to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, Rev. B (Continued)

Page	Item	Original Text	Change To	Comment
5-7	High-Speed Serial Port Status (HSPSTAT) register, bit diagram	[Bit 13 column:] *Res* R — 0	[Bit 13 column:] BRKIM R/W0 S 0	
		[Bit 11 column:] *Res* R — 0	[Bit 11 column:] ABDONE R/W0 S 0	
	High-Speed Serial Port Status (HSPSTAT) register, bit 13 description	13 Res **Reserved** For compatibility with future devices, always write this bit field with its chip reset default value.	13 BRKIM **Break Detected—Immediate** 0 = No break condition has been detected on the receive data line. 1 = The serial port has detected a break condition on the receive data line. The BRKIM bit must be cleared by software. If the receive FIFO is enabled, the BRKIM bit bypasses the FIFO to provide immediate notification of the break condition. In contrast, the BRK bit is not set until the HSPRXD register is loaded with the character on which the break was detected. If the receive FIFO is disabled, the BRKIM bit has no meaning, and software should use the BRK bit instead.	
	High-Speed Serial Port Status (HSPSTAT) register, bit 12 OERIM description	[Existing text.]	[Add the following paragraph:] If the receive FIFO is disabled, the OERIM bit has no meaning, and software should use the OER bit instead.	
	High-Speed Serial Port Status (HSPSTAT) register, bit 11 description	11 Res **Reserved** For compatibility with future devices, always write this bit field with its chip reset default value.	11 ABDONE **Autobaud Done** 0 = The autobaud operation is not complete, or no autobaud operation has been initiated. 1 = The autobaud operation has completed. The ABDONE bit must be cleared by software.	

Table 1. Corrections to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, Rev. B (Continued)

Page	Item	Original Text	Change To	Comment
5-8	High-Speed Serial Port Status (HSPSTAT) register, bit 6 THRE description	[Existing text.]	[Add the following note:] **Note:** If FIFOs are not used, software must verify that the THRE bit is set before writing to the HSPTXD register even if the TEMT bit was set before the previous write. If FIFOs are being used, software can omit polling the THRE bit only if it is certain there is space in the FIFO. The FIFO contains 16 empty slots if the TEMT bit is set. The FIFO contains at least eight empty slots if hardware sets the TTHRSH bit after software has cleared it.	
5-9	High-Speed Serial Port Status (HSPSTAT) register, Programming Notes	[Existing text.]	[Add the following paragraph:] The BRKIM and ABDONE bits are not available in parts released prior to revision C1. For processor revision information, see the PRL register description on page 16-4 [of the manual, and on page 11 of this amendment].	
5-10	High-Speed Serial Port Interrupt Mask (HSPIMSK) register, bit diagram	[Bit 13 column:] *Res* R — 0	[Bit 13 column:] BRKIM R/W — 0	
		[Bit 11 column:] *Res* R — 0	[Bit 11 column:] ABDONE R/W — 0	
	High-Speed Serial Port Interrupt Mask (HSPIMSK) register, bit 13 description	13 Res **Reserved** For compatibility with future devices, always write this bit field with its chip reset default value.	13 BRKIM **Break Immediate Interrupt Enable** 0 = The BRKIM bit in the HSPSTAT register does not generate interrupt requests. 1 = When the BRKIM bit is 1 and the RSIE bit in the HSPCON0 register is 1, the serial port generates an interrupt when the BRKIM bit in the HSPSTAT register is 1.	Also add BRKIM and ABDONE to bits affected by RSIE in Programming Notes on page 5-11 of manual.
	High-Speed Serial Port Interrupt Mask (HSPIMSK) register, bit 11 description	11 Res **Reserved** For compatibility with future devices, always write this bit field with its chip reset default value.	11 ABDONE **Autobaud Done Interrupt Enable** 0 = The ABDONE bit in the HSPSTAT register does not generate interrupt requests. 1 = When the ABDONE bit is 1 and the RSIE bit in the HSPCON0 register is 1, the serial port generates an interrupt when the autobaud operation completes.	

Table 1. Corrections to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, Rev. B (Continued)

Page	Item	Original Text	Change To	Comment
5-12	High-Speed Serial Port Interrupt Mask (HSPIMSK) register, Programming Notes	[Existing text.]	[Add the following paragraph:] The BRKIM and ABDONE bits are not available in parts released prior to revision C1. For processor revision information, see the PRL register description on page 16-4 [of the manual, and on page 11 of this amendment].	
5-23–5-27	High-Speed Serial Port Autobaud x (HSPABx) registers, new register description	[Four existing 16-bit register descriptions, HSPAB0–HSPAB3]	[Add a new register description for HSPAB4, offset 27E, and modify the other descriptions accordingly. The HSPAB4 register is identical to HSPAB0–HSPAB3, except as described in the following programming notes change.]	
	High-Speed Serial Port Autobaud x (HSPABx) registers, Programming Notes, second and third paragraphs	To always use the calculated baud divisor when autobaud is enabled, clear the ABTHRSH3 bit field in the HSPAB3 register, or leave the field at its default value (00h). Software must always program the HSPAB3 register with the largest value, program the HSPAB2 register with the next largest value, and so on. The HSPAB3 register must be programmed with the highest value even when using fewer than four valid divisor values. Software must clear the unused HSPABx registers (starting with HSPAB0) or leave them at their default values (00h).	To always use the calculated baud divisor when autobaud is enabled, clear the ABTHRSHx bit fields in the HSPAB3 and HSPAB4 registers, or leave the bit fields at their default value (00h). The HSPAB4 register is not available in parts released prior to revision C1. For processor revision information, see the PRL register description on page 16-4 [of the manual, and on page 11 of this amendment]. If the HSPAB4 register is used, it must contain the largest ABTHRSHx value. If the HSPAB4 register is not used, the ABTHRSH4 bit field must be 0, and the HSPAB3 register must contain the largest ABTHRSHx value. To enable the HSPABx registers, software must always program the HSPAB4 or HSPAB3 register's ABTHRSHx bit field. The other HSPABx registers must be programmed with successively lower threshold values, according to their numeric order. For example, if HSPAB4 contains the largest ABTHRSHx value, program HSPAB3 register with the next largest value, then HSPAB2, and so on. If any of the lower registers are to be left unused, software must clear the lowest-numbered ABTHRSHx bit fields or leave them at their default values (00h).	
5-24	Figure 5-1 Autobaud Enhancement	[Existing figure]	[Replace with Figure 5-1 on page 12 of this amendment.]	Update and clarify figure.
5-31	Serial Port Status (SPSTAT) register, bit 6 THRE description	[Existing text]	[Add the following note:] ***Note:*** *Software must verify that the THRE bit is set before writing to the SPTXD register even if the TEMT bit was set before the previous write.*	

Table 1. Corrections to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, Rev. B (Continued)

Page	Item	Original Text	Change To	Comment
5-32	Serial Port Status (SPSTAT) register, bit 1 IDLED description	[Existing text]	[Add the following paragraph:] The IDLED bit is included in the UART for compatibility with the High-Speed UART. In the absence of a FIFO (High-Speed UART only), the IDLED status bit is redundant and the RDR status bit should be used instead.	
Chapter 9 Interrupt Controller Registers				
9-41	Interrupt Request (REQST) register, Offset 32Ch; Software Read/Write field for bits 14–0	R	R/W0	
	Interrupt Request (REQST) register, Offset 32Ch; programming notes	**Programming Notes** [Existing text]	**Programming Notes** [Add the following paragraphs:] To clear a spurious edge-triggered interrupt that is pending, software can write 0 to the appropriate channel bit. Spurious edge-triggered interrupts can occur when software initially configures a PIO pin as an interrupt source. To clear level-triggered interrupts, the interrupt source must be cleared.	
Chapter 11 Chip Select Registers				
11-2	Upper Memory Chip Select (UMCS) register, Offset 3A0h, register description	[Existing paragraph]	[Insert a paragraph break before and after the following sentence:] This chip select is enabled immediately after an external or watchdog timer reset.	Clarify.
11-5	Lower Memory Chip Select (LMCS) register, Offset 3A2h, register description	[Existing paragraph]	[Insert a paragraph break before and after the following pair of sentences:] This chip select is not enabled immediately after an external or watchdog timer reset. This chip select can only be activated by system software performing a write operation to the LMCS register.	Clarify.
11-9	Peripheral Memory Chip Select (PACS) register, Offset 3A4h, register description	[Existing paragraph]	[Insert a paragraph break before the following pair of sentences:] The $\overline{\text{PCS}}$ chip selects are not enabled immediately after an external or watchdog timer reset. The $\overline{\text{PCS}}$ chip selects can only be activated by system software performing a write operation to both the PACS register and the MPCS register.	Clarify.
11-11	Midrange Memory Chip Select (MMCS) register, Offset 3A6h, bits 15–19 description, second paragraph, last sentence	The BA[19–13] bit field default value is 3Fh (i.e., the default base address is 3F000h).	The BA[19–13] bit field default value is 3Fh, which results in a default base address of 7E000h.	

Table 1. Corrections to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, Rev. B (Continued)

Page	Item	Original Text	Change To	Comment
Chapter 13 Programmable I/O (PIO) Registers				
13-4	PIO Mode 0 (PIOMODE0) register, Offset 3C0h, bits 15–0 description, first sentence of last paragraph	Terminated operation applies an internal 100-kΩ pullup or pulldown resistor, depending on the pin.	Terminated operation applies an internal 50-kΩ (approximate) pullup or pulldown resistor, depending on the pin.	
13-5	PIO Direction 0 (PIODIR0) register, Offset 3C2h, bits 15–0 description, first sentence of last paragraph			
13-7	PIO Set 0 (PIOSET0) register, Offset 3C6h, diagram Software Read/Write row (all bits)	R/W	R/W1	Writing 0 has no effect.
13-8	PIO Clear 0 (PIOCLR0) register, Offset 3C8h, diagram Software Read/Write row (all bits)			
13-9	PIO Mode 1 (PIOMODE1) register, Offset 3CAh, bits 15–0 description, first sentence of last paragraph	Terminated operation applies an internal 100-kΩ pullup or pulldown resistor, depending on the pin.	Terminated operation applies an internal 50-kΩ (approximate) pullup or pulldown resistor, depending on the pin.	
13-10	PIO Direction 1 (PIODIR1) register, Offset 3CCh, bits 15–0 description, first sentence of last paragraph			
13-12	PIO Set 1 (PIOSET1) register, Offset 3D0h, diagram Software Read/Write row (all bits)	R/W	R/W1	Writing 0 has no effect.
13-13	PIO Clear 1 (PIOCLR1) register, Offset 3D2h, diagram Software Read/Write row (all bits)			
13-14	PIO Mode 2 (PIOMODE2) register, Offset 3D4h, bits 15–0 description, first sentence of last paragraph	Terminated operation applies an internal 100-kΩ pullup or pulldown resistor, depending on the pin.	Terminated operation applies an internal 50-kΩ (approximate) pullup or pulldown resistor, depending on the pin.	
13-15	PIO Direction 2 (PIODIR2) register, Offset 3D6h, bits 15–0 description, first sentence of last paragraph			

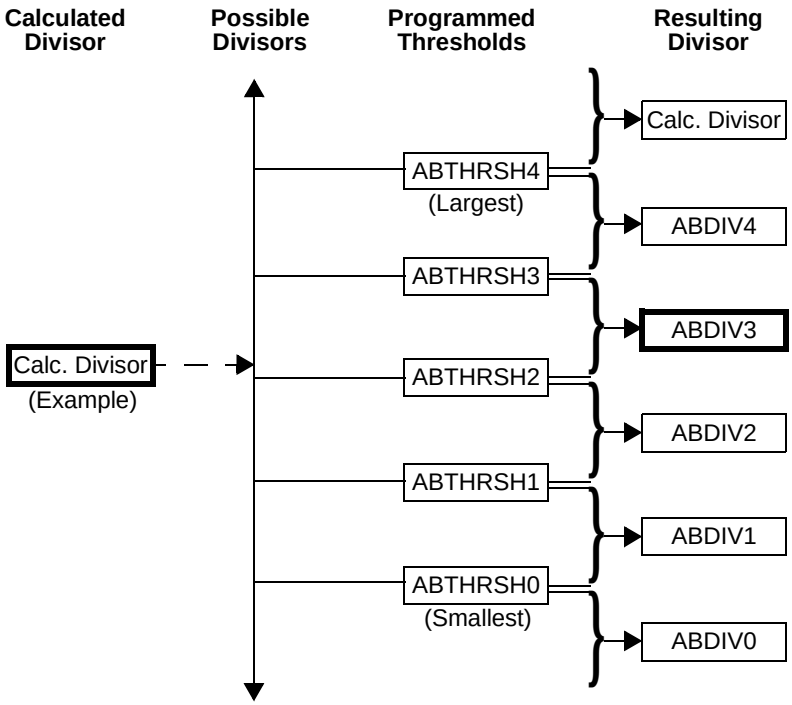
Table 1. Corrections to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, Rev. B (Continued)

Page	Item	Original Text	Change To	Comment
13-17	PIO Set 2 (PIOSET2) register, Offset 3DAh, diagram Software Read/Write row (all bits)	R/W	R/W1	Writing 0 has no effect.
13-18	PIO Clear 2 (PIOCLR2) register, Offset 3DCh, diagram Software Read/Write row (all bits)			
Chapter 16 Miscellaneous Configuration Registers				
16-4	Processor Revision Level (PRL) register, Offset 03F4h, bits 15–0 bit description	[Existing text.]	[Add the following paragraphs:] The PRL for Revision B1 is 4002h. The PRL for Revision B2 and B3 is 4003h. (B2 was not released. B2 and B3 are functionally identical.) The PRL for Revision C0 (not released) is 4004h. The PRL for Revision C1 is 4005h.	
Appendix A Register Summary				
A-8	CNTCTL register, bit 7	Res	HNDSHK	Add bit.
A-9	IEPCTL register, bit 7			
	AEPCTL register, bit 7			
	BEPCTL register, bit 7			
A-10	CEPCTL register, bit 7			
	DEPCTL register, bit 7			
A-11	HSPSTAT register, bit 13	Res	BRKIM	Add bit.
	HSPSTAT register, bit 11	Res	ABDONE	Add bit.
	HSPIMSK register, bit 13	Res	BRKIM	Add bit.
	HSPIMSK register, bit 11	Res	ABDONE	Add bit.
	HSPABx registers	[Existing rows]	[Add a row for the new HSPAB4 register, similar to the other HSPABx registers, with offset 27Eh, default location FE7Eh, default value 0h, and bit fields ABDIV4 and ABTHRSH4.]	Add register.

CHANGED FIGURE

Replace Figure 5-1 on page 5-24 of the manual with the following figure.

Figure 5-1 Autobaud Enhancement



Notes:

1. *If the calculated divisor is larger than the largest ABTHRSHx bit field value, the resulting divisor is the same as the calculated divisor.*
2. *The ABTHRSH4 or ABTHRSH3 bit field must contain the largest threshold value. If the ABTHRSH4 bit field is not the largest threshold, it must be 0. The remaining ABTHRSHx bit fields must be programmed with successively smaller thresholds for lower-numbered ABTHRSHx bit fields. If all five thresholds are not needed, the lowest-numbered ABTHRSHx bit fields (ABTHRSH0, ABTHRSH1, etc.) can be cleared or left in their default disabled state (00h).*

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