AMENDMENT

Am186™ER and Am188™ER Microcontrollers

User's Manual

This document amends the *Am186™ER and Am188™ER Microcontrollers User's Manual* (order #21684B).

This amendment contains several documentation changes to the *Am186™ER and Am188™ER Microcontrollers User's Manual* as described in Table 1.

The figures on page 3 and page 4 of this amendment contain notes that reference pages in the *Am186™ER and Am188™ER Microcontrollers User's Manual.* Refer to the referenced pages of the *Am186™ER and Am188™ER Microcontrollers User's Manual* for the related information.

Table 1. Corrections to the *Am186™ER and Am188™ER Microcontrollers User's Manual*, Rev. B

Subheading	Page	Original Text	Change To
1.2 Distinctive Characteristics	1-4	Figure 1-1 Am186ER Microcontroller Block Diagram. Arrow pointing from control register bus down to the "32-Kbyte RAM" box.	Replace "Figure 1-1 Am186ER Microcontroller Block Diagram" with the figure "Am186™ER Microcontroller Block Diagram" on page 3 of this amendment. Because control registers do not interface with RAM, the arrow is moved to originate from the "Bus Interface Unit" box to point to the "32-Kbyte RAM" box. The word "RAM" in the "32-Kbyte RAM" box is changed to "SRAM".
	1-5	Figure 1-2 Am188ER Microcontroller Block Diagram. Arrow pointing from control register bus down to the "32-Kbyte RAM" box.	Replace "Figure 1-2 Am186ER Microcontroller Block Diagram" with the figure "Am188™ER Microcontroller Block Diagram" on page 4 of this amendment. Because control registers do not interface with RAM, the arrow is moved to originate from the "Bus Interface Unit" box to point to the "32-Kbyte RAM" box. The word "RAM" in the "32-Kbyte RAM" box is changed to "SRAM".
3.4.2 Crystal-Driven Clock Source	3-24	Figure 3.5 Oscillator Configurations. In parts "a." and "b." of the figure, the arrow originates from "X1" and points to the callout "To PLL".	Replace "Figure 3-5 Oscillator Configurations" with Figure 1 on page 5 of this amendment. In parts "a." and "b." of the figure, the arrow is moved to originate from "X2", and the "To PLL" callout is moved to align horizontally with "X2" (under the "Oscillator" callout).
8.1 OVERVIEW	8-1	The WDT is active after reset.	The WDT is inactive after reset.
	8-1	After reset, the WDT is enabled and the timeout period is set to its maximum value.	[Delete sentence.]

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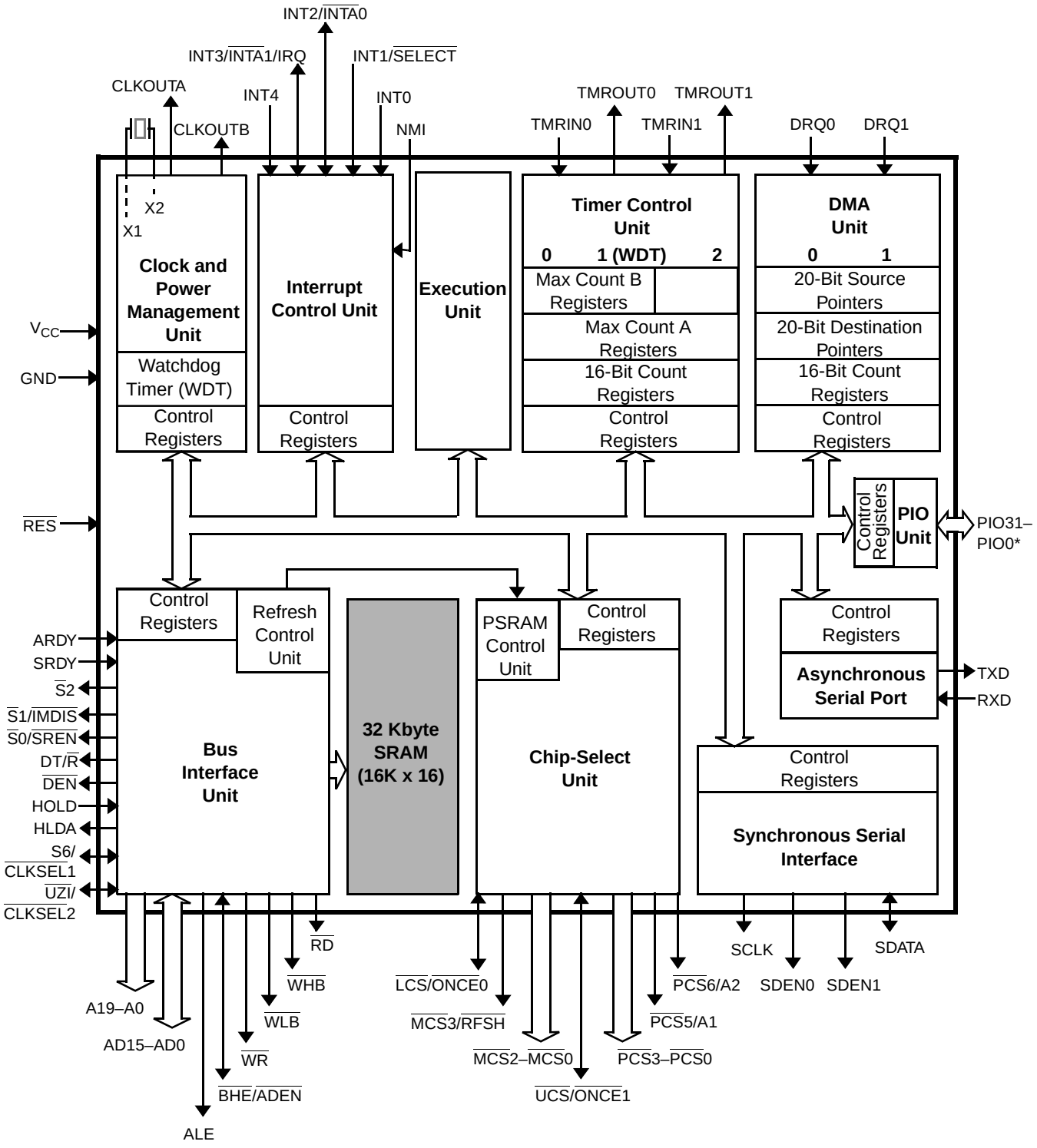
Table 1. Corrections to the *Am186™ER and Am188™ER Microcontrollers User's Manual*, Rev. B (Continued)

Subheading	Page	Original Text	Change To
8.1.1 Watchdog Timer Control Register (WDTCON, Offset E6h)	8-1	The watchdog timer is enabled out of reset and configured to system reset mode with a maximum timeout count.	[Delete sentence.]
	8-1	**Note:** *The Watchdog Timer (WDT) is active after reset.*	**Note:** *The Am186ER and Am188ER hardware watchdog timer is inactive after reset.*
	8-2	The value of the WDTCON Register at reset is C080h.	The value of the WDTCON Register at reset is 4080h.
	8-2	This bit is 1 after processor reset. [This sentence is in the **Bit 15: Watchdog Timer Enable (ENA)** description.]	After processor reset, this bit is 0.

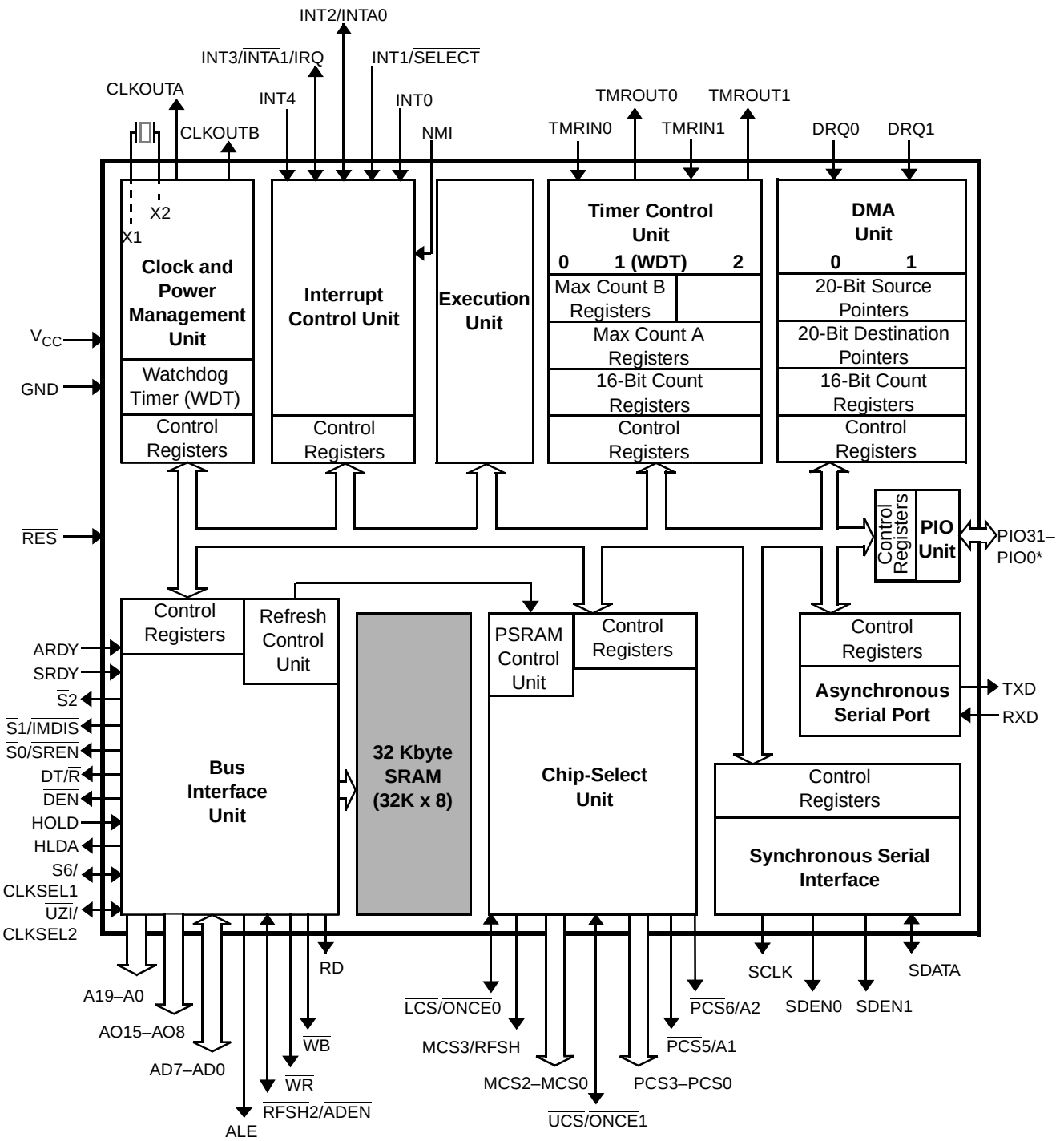
Am186™ER MICROCONTROLLER BLOCK DIAGRAM



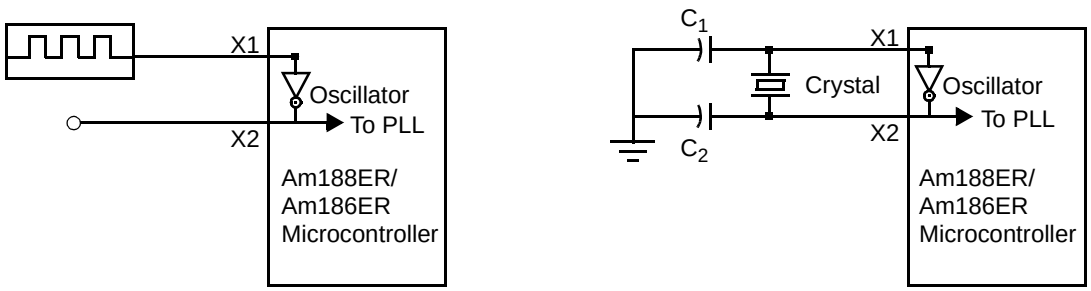
Note:

** All PIO signals are shared with other physical pins. See the pin descriptions beginning on page 26 and Table 3 on page 32 of the Am186™ER and Am188™ER Microcontrollers User's Manual for information on shared functions.*

Am188™ER MICROCONTROLLER BLOCK DIAGRAM



Note:
** All PIO signals are shared with other physical pins. See the pin descriptions beginning on page 26 and Table 3 on page 32 of the Am186™ER and Am188™ER Microcontrollers User's Manual for information on shared functions.*



a. External Clock Configuration **b. Crystal Configuration**

Note:
X1 and X2 are not 5-V tolerant. The X1 maximum input is V_{CC}.

Figure 1: Am186ER and Am188ER Microcontrollers Oscillator Configurations