Systems in Silicon

16 Bit Microcontroller Overview

Am186™ED, Am186EM, Am186ER, Am186ES

AMD

AMD Embedded Processor Division, 16-Bit Microcontroller Overview

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E86 Embedded Processor Family

Leverage the billions of dollars of research and development on the world's dominant architecture: x86

- Price
- Performance
- Software compatibility
- Broad, established set of tools
- Roadmap
- Integration
- Code compactness
- Familiarity

AMD

E86 Family of Microprocessors and Microcontrollers

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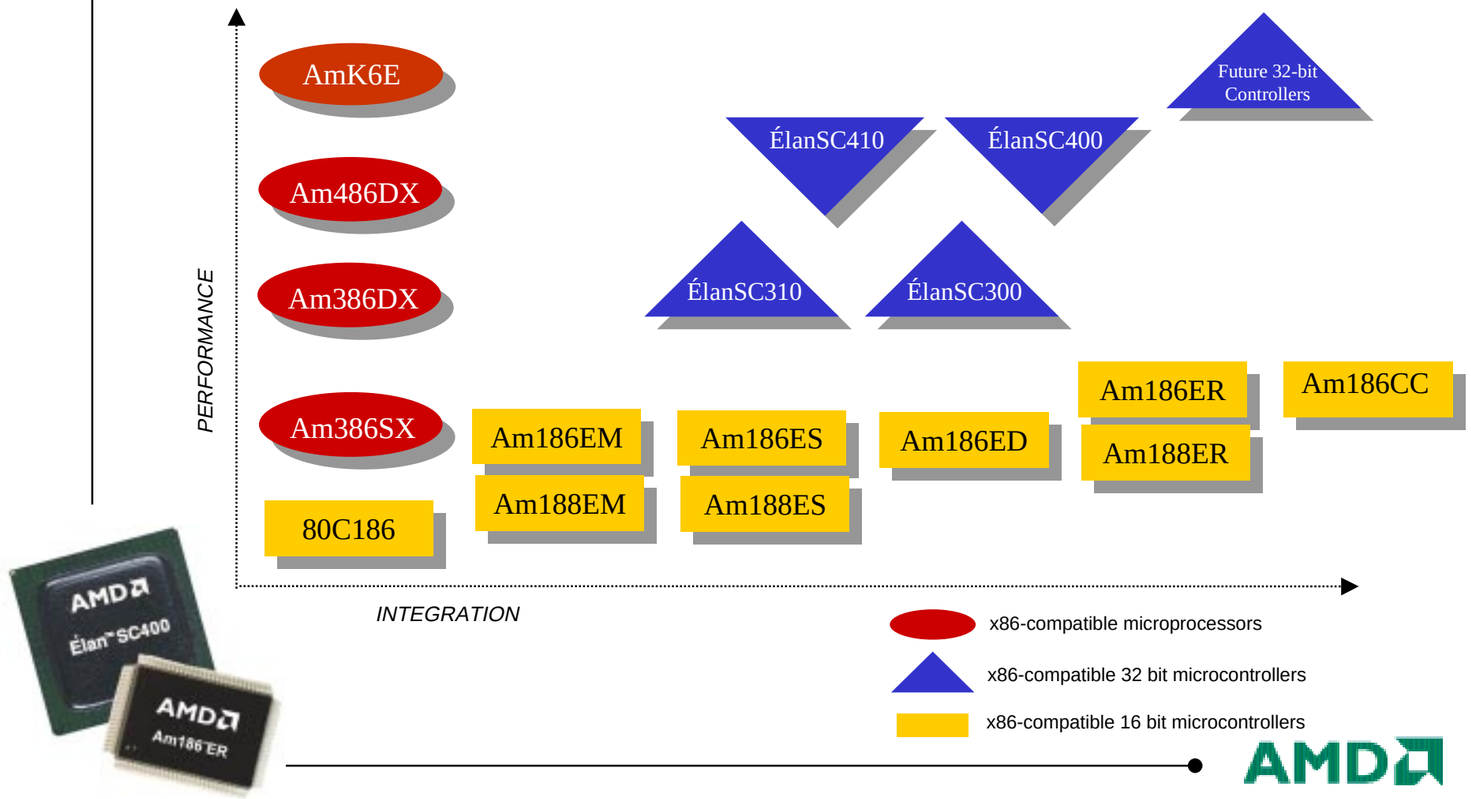

AMD Embedded Processor Division, 16-Bit Microcontroller Overview

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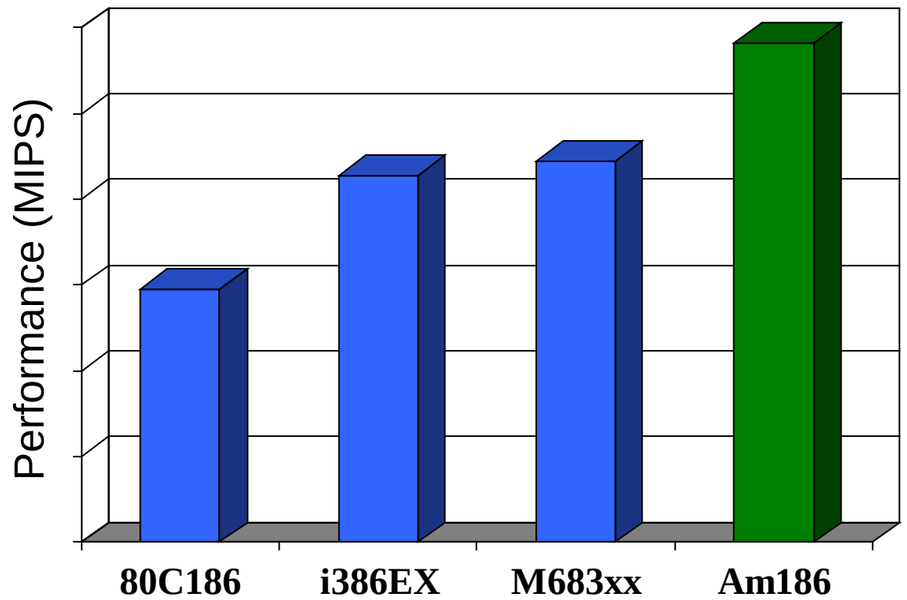
High Performance



"32-bit performance at a 16-bit price."

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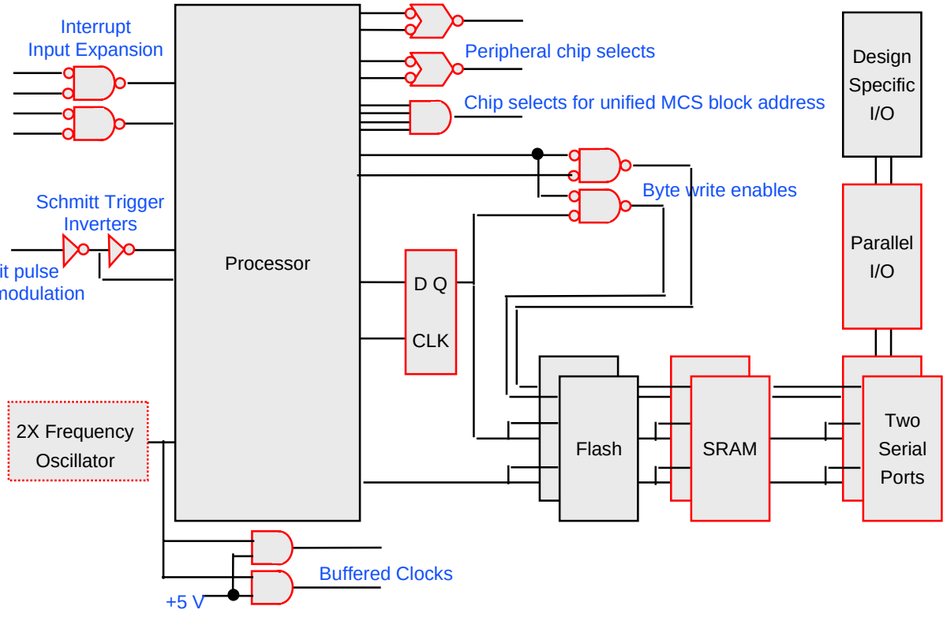
Low System Cost



"Everything in red is integrated into the Am186."

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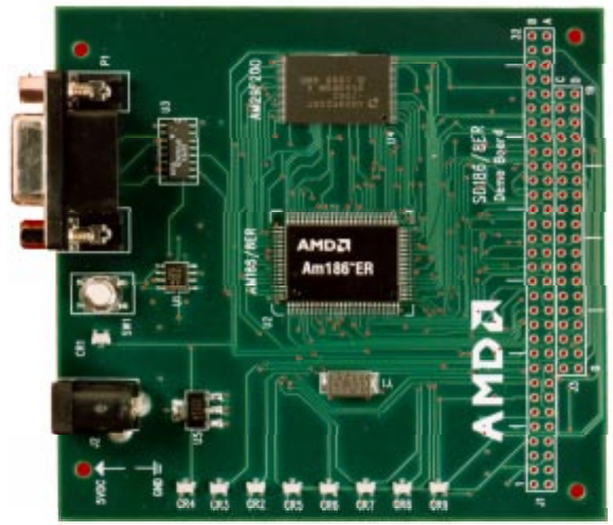
Low System Cost (Con't)



The Am186ER Evaluation Board

"1 Am186ER + 1 Flash = An easy high performance solution."

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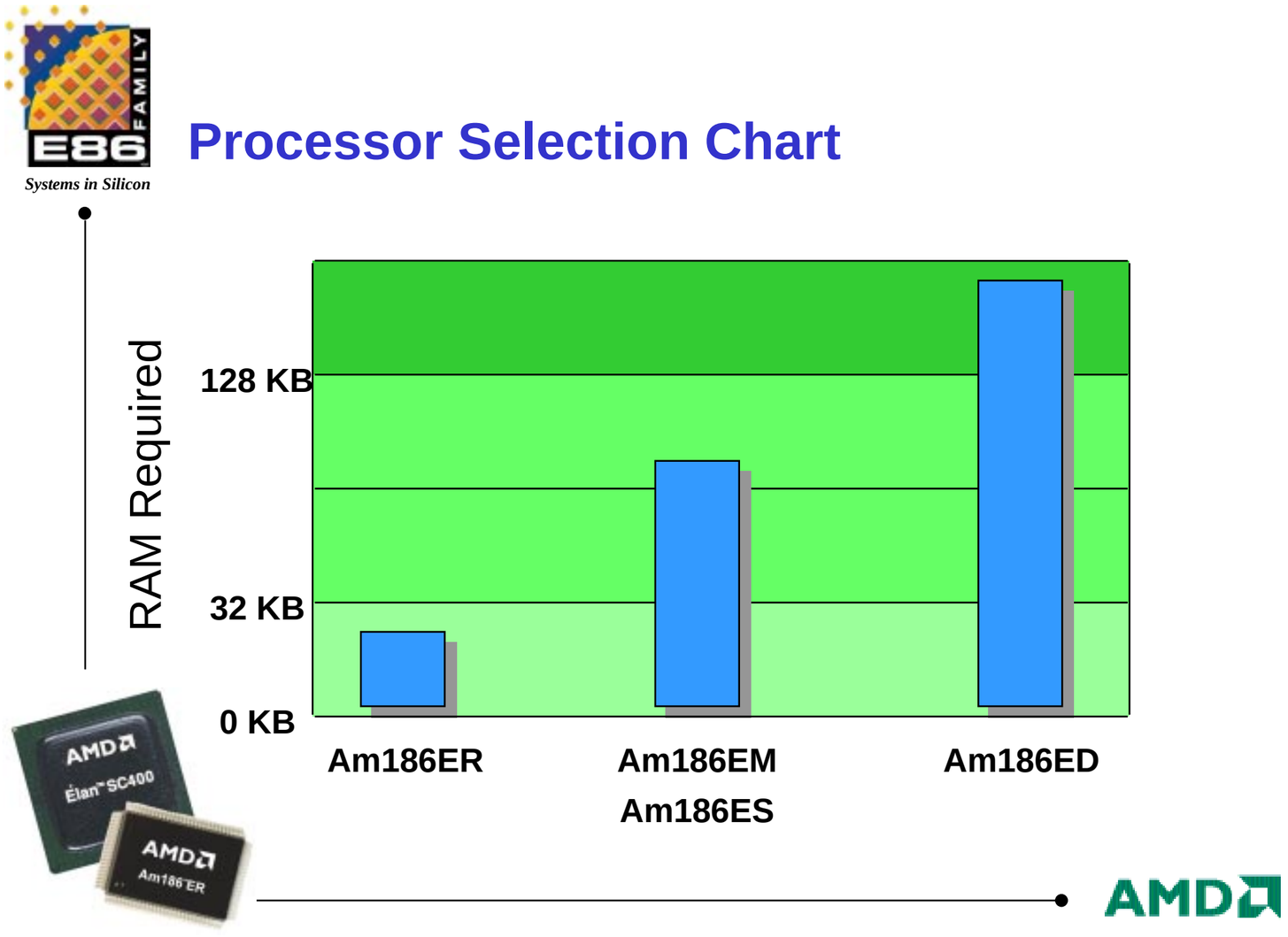
Processor Selection Chart



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E86 FAMILY

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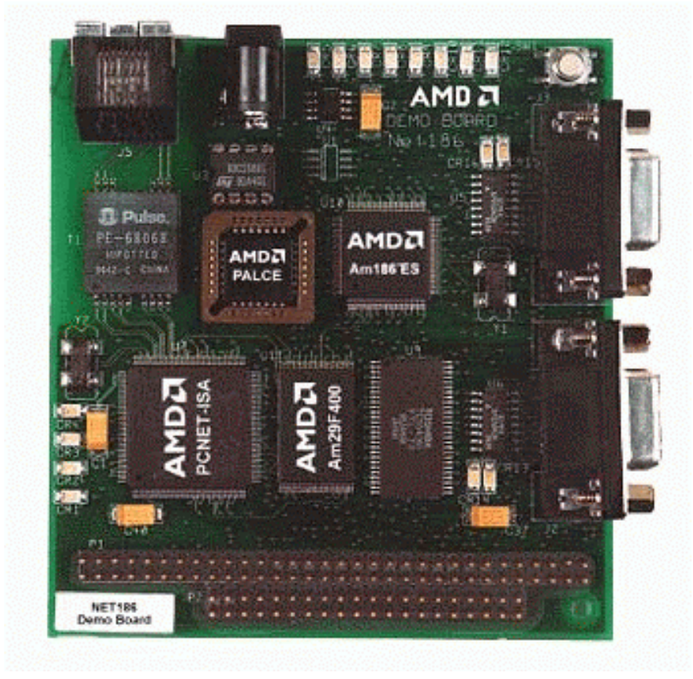
Ethernet Connectivity: Net186 Evaluation Board



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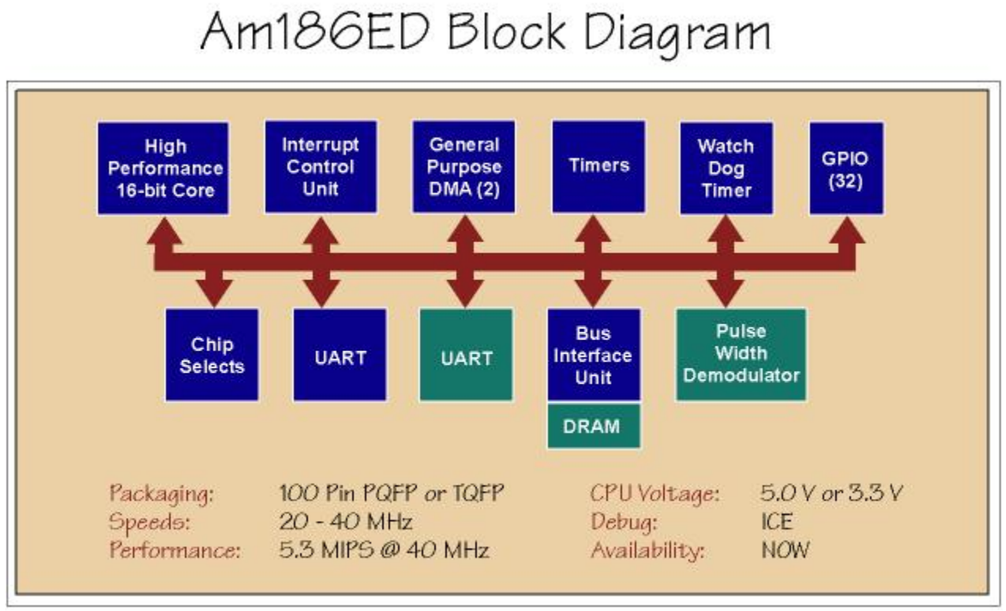

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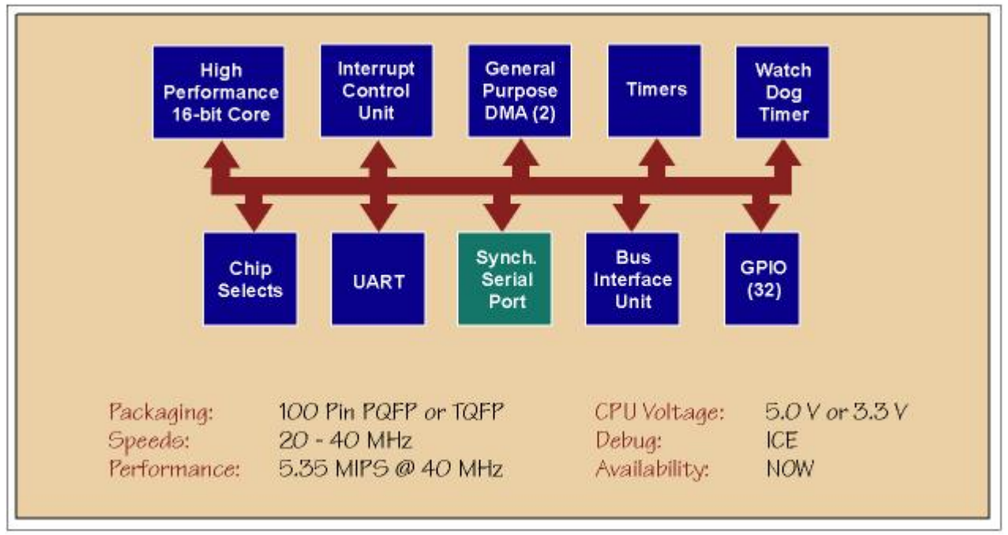
Am186EM Block Diagram



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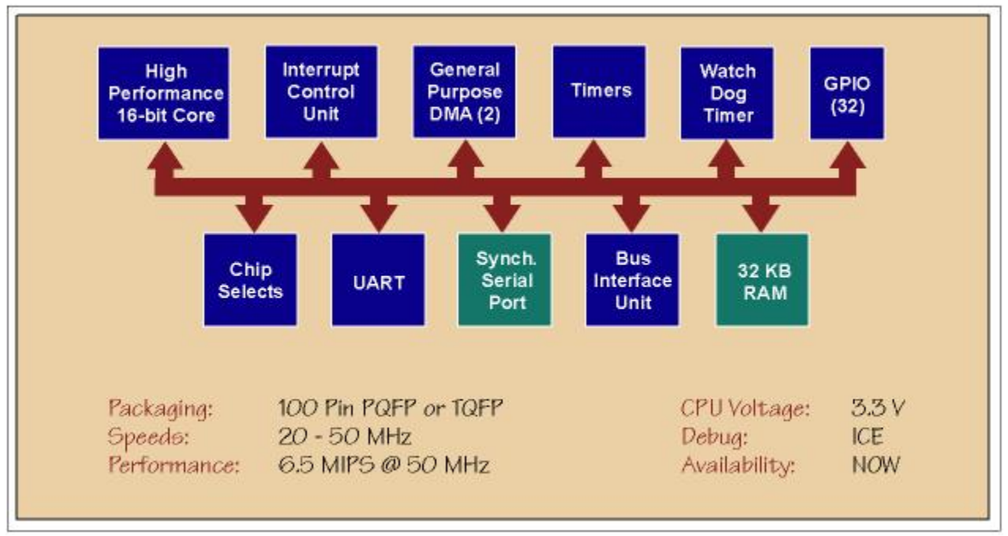
Am186ER Block Diagram



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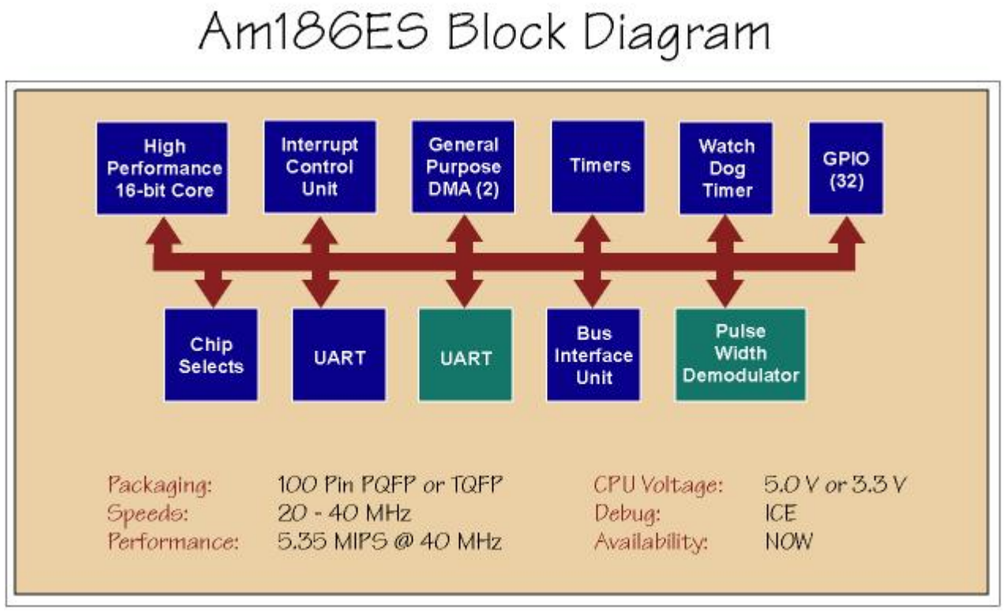

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Backup Slides
Peripherals

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CPU Core

- **16-Bit 80C186 CPU Core**
  - The Am186 version has a 16-bit external interface for maximum performance.
  - The Am188 version has an 8-bit external interface in order to minimize CPU and memory cost.
  - 1 MB memory address space, 64 KB I/O space.
  - Compatible with the large installed base of x86 software, development tools, and engineering know-how.

- **High clock frequencies yield high performance.**
  - *“32-bit performance at a 16-bit price.”*
  - The Am186ER has a 50 MHz maximum clock frequency which yields up to 6.6 MIPS.
  - The Am186ED, Am186EM, and Am186ES have a 40 MHz maximum clock frequency which yields up to 5.3 MIPS.

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DRAM Controller

- **DRAM Controller**
  - Supports fast-page mode or EDO DRAM.
  - Supports up to two banks of DRAM.
  - Has improved memory timing specifications which allow zero wait-state operation using commodity speed DRAMs:
    - Zero wait-state operation at 40 MHz using 50 ns DRAM.
    - Zero wait-state operation at 33 MHz using 60 ns DRAM.
    - Zero wait-state operation at 25 MHz using 70 ns DRAM.

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On Board RAM

- **32 KB of on board RAM**
  - Am186ER has a 16 K x 16 bit wide array (32 KB).
  - Am188ER has a 32 K x 8 bit wide array (32 KB).
  - The on board RAM can be located at any 32 KB boundary within the 1 MB address space.

- **Provides performance equivalent to 16-bit wide, external zero wait-state SRAM.**

- **There are two debug modes associated with the internal memory:**
  - The internal RAM can be disabled
  - One can drive data on the external data bus during the internal RAM read cycles.

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Asynchronous Serial Port

- **Asynchronous Serial Port**
  - Two pin interface that permits full-duplex bidirectional data transfer.
  - It supports 7 bit or 8 bit data; odd, even, or no parity; and 1 or 2 stop bits.
  - The Am186ED and ES also support 9-bit data transfers. This can be used in a multidrop serial port protocol.
- **Operation During Power Save Mode**
  - The asynchronous serial port(s) can be used while the processor is in power-save mode, but the software must adjust the transfer rate to correctly reflect the new internal operating frequency. The software must also ensure that the serial port does not receive any information while the frequency is being changed.

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Synchronous Serial Port

- **Synchronous Serial Port**
  - Four pin interface permits half-duplex bidirectional data transfer at speeds up to 20 Mbits/sec (peak).
  - Often used for communicating with ASICs that require programmability, but are short on pins.

- **Operation During Power Save Mode**
  - The synchronous serial port(s) can be used while the processor is in power-save mode, but the software must adjust the transfer rate to correctly reflect the new internal operating frequency. The software must also ensure that the serial port does not receive any information while the frequency is being changed.

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General Purpose I/O Pins

- **32 General Purpose I/O Pins**
  - Each of these pins can be used as a user-programmable input or output signal if the shared function of that pin in not needed.
  - The large quantity of PIO pins provides the flexibility to add a multitude of external peripherals or communications channels.
  - A PIO pin can be configured to operate as an input (with or without a weak internal pull-up or pull-down), as an output, or as as open-drain output.
  - **Notes on Usage**
  - The A19-A17 address pins default to normal operation at power-on reset, allowing the processor to correctly begin fetching instructions at boot address FFFF0h.
  - Note that emulators use A19, A18, A17, S6, and #UZI. System designers using these signals as PIOs should check with their emulator vendor for limitations on emulator operation.

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Clock and Power Management

- **Internal Phase-Locked Loop**
  - The internal PLL allows the CPU to operate at 0.5 times, 1.0 times, or (in the case of the Am186/188ER) at 4.0 times the crystal's frequency. *This allows a 40 MHz Am186ER (for example) to use a less expensive 10 MHz crystal.*

- **Power Save Mode**
  - The CPU and internal peripherals can operate at a frequency as slow as 1/128th the maximum operating frequency.
  - When the CPU is in power-save mode and a hardware interrupt occurs the microcontroller automatically returns to its normal operating frequency. The processor remains in power-save mode during software traps and interrupts.
  - Power-save operation requires that clock dependent peripherals be reprogrammed for clock frequency changes.

Systems in Silicon

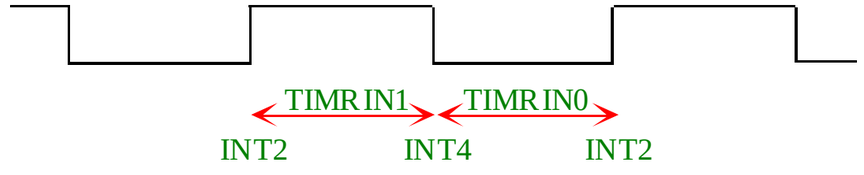
Bus Interface

- **Non-Multiplexed Address and Data Bus**
  - The original 80C186 / 80C188 microprocessors had a multiplexed address and data bus. This reduced system performance and required hardware (external latches) which increased system cost. In order to increase performance and decrease cost, the Am186 family offers non-multiplexed address and data busses.
  - *The Am186 family provides a glueless interface to SRAM, flash, and EPROMs*. The Am186ED also provides a glueless interface to DRAM.

- **Multiplexed Address and Data Bus**
  - Designers can also still use the original multiplexed A/D bus architecture, if they so desire.

Pulse Width Demodulator

- **Pulse Width Demodulator**
  - The PWD is useful in many applications, such as bar code reading, where it is necessary to measure the width of a signal in both its high and low phases.
  - Since the PWD's timers count at one quarter the processor's clock frequency, this determines the maximum resolution that can be attained.
  - In PWD mode TMRIN0, TMRIN1, INT2, and INT4 are configured internal to the microcontroller to support the detection of rising and falling edges on the PWD input pin.



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Interrupt Controller

- **Interrupt Controller Operation**
  - Interrupts can be received from both internal and external sources. The internal interrupt controller prioritizes these requests and presents them one at a time to the CPU.
  - Depending on the device, the Am186/188 family supports 7 - 8 internal interrupt sources and 6 - 8 external interrupt sources.
  - Interrupts are automatically disabled when an interrupt is taken. Interrupt-service routines (ISRs) may re-enable interrupts by setting the IF flag. This allows interrupts of greater or equal priority to interrupt the currently executing ISR.
  - Interrupts from the same source are disabled as long as the corresponding bit in the interrupt in-service register is set. INT0 and INT1 provide a special bit to enable a special fully nested mode. See data sheet for details.

Systems in Silicon

Timers

- **Timer Operation**
  - There are three 16 bit timers in the Am186 microcontrollers. Timers 0 and 1 are connected to external pins.
  - Timers can be used to count or time external events. They can also generate nonrepetitive or variable duty cycle waveforms.
  - Timer 1 can be used as a watchdog timer interrupt. This provides a mechanism for recovering if the system crashes or hangs.
  - Timer 2 is not connected to any external pins. It can be used for real-time coding and time-delay applications.
  - A timer can operate at a speed of up to ¼ the internal clock frequency.
  - Each timer has a maximum count register that defines the maximum value that timer can reach. Timers 0 and 1 also have a secondary maximum count register. This allows the timers to alternate between two different maximum values. Timer 2 can also be used as a DMA request source or a prescaler for timers 0 and 1.

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DMA Unit

- **Direct Memory Access (DMA) Unit**
  - A DMA Unit allows the transfer of data between memory and peripherals without CPU involvement. This effectively increases the performance of the CPU by freeing it to perform other tasks.
  - Data transfers can occur between memory and I/O spaces or within the same space (e.g. memory-to-memory or I/O-to-I/O). Bytes can also be transferred to or from even or odd addresses.
  - There are two DMA channels available in the Am186/188 microcontrollers. The DMA channels can be programmed so that one channel is always given priority over the other, or they can be programmed to alternate cycles when both have DMA requests pending.

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Chip Select Unit

- **Chip Select Unit Operation**
  - The Am186 microcontrollers contain logic that provides programmable chip select generation for both memories and peripherals.
  - The Am186/188 family provides 6 peripheral chip select outputs and 6 - 7 memory chip select outputs.
  - The logic can be programmed to provide external ready and wait-state generation and latched address bits A1 and A2.
  - The chip select lines are active for all memory and I/O cycles in their programmed areas, whether they are generated by the CPU or the integrated DMA unit.

Systems in Silicon

Backup Slides
FusionE86 Partners

Systems in Silicon

Third Party Support

- **Emulation Tools**
  - Applied Microsystems
  - Beacon Development Tools
  - CEIBO
  - Grammar Engine
  - HITEX
  - iSystem GmbH
  - Lauterbach Datentechnik
  - Microtek International
  - Softaid

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Third Party Support

- **Debugging and Testing Support**
  - Corelis, Inc.
  - Emulation Technology
  - Hewlett Packard
  - ITT Pomona

- **Software Support**
  - Aisys
  - Chronology
  - Eagle Design Automation
  - Synopsis (Logic Modeling)

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Third Party Support

- **DOS**
  - Datalight
  - General Software
  - IBM
  - Microsoft
- **RTOS**
  - Accelerated Technology
  - Integrated Systems
  - JMI Software
  - KADAK Products
  - Microtec Research
  - Pacific Softworks
  - US Software

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Third Party Support

- **Development Environments**
  - Borland
  - CAD-UL
  - Concurrent Sciences
  - Cygnus
  - MetaWare
  - Microsoft
  - Microtek Research
  - Paradigm
  - PharLap Software
  - Softaid
  - Systems and Software (SSI)
  - Watcom