AMENDMENT

80C186 and 80C188 Integrated 16-Bit Microprocessors

This document amends the *80C186 and 80C188 Integrated 16-Bit Microprocessors Data Book*, order #16514D, and replaces the discontinued *80C186/80C188 CMOS High-Integration 16-Bit Microprocessors Amendment* (specifications for the 20-MHz industrial operating range). This amendment consists of two parts:

- Clock generation information changes for the 80C186 and 80C188 microcontrollers. If the guidelines in this bulletin are not followed, you may experience problems with clock start-up.
- Industrial operating information at 20 MHz. This is the same information that was published in the discontinued *80C186/80C188 CMOS High-Integration 16-Bit Microprocessors Amendment*.

CLOCKING INFORMATION CHANGES

Crystal-Driven Clock Source

The internal oscillator circuit of the microcontroller is designed to function with a parallel resonant fundamental or third-overtone crystal. The 80C186 and 80C188 microprocessors use a crystal frequency that is twice the processor frequency. AMD does not recommend that you replace a crystal with an LC or RC equivalent for any member of the Am186™ family.

The X1 and X2 signals are connected to an internal inverting amplifier (oscillator) that provides, along with the external feedback loading, the necessary phase shift (Figure 1 on page 2). In such a positive feedback circuit, the inverting amplifier has an output signal (X2) 180 degrees out of phase of the input signal (X1). The external feedback network provides an additional 180 degree phase shift. In an ideal system, the input to X1 has 360 or zero degrees of phase shift.

The external feedback network is designed to be as close as possible to ideal. If the feedback network is not providing necessary phase shift, negative feedback dampens the output of the amplifier and negatively affects the operation of the clock generator. Values for the loading on X1 and X2 must be chosen to provide the necessary phase shift and crystal operation.

Selecting a Crystal

When selecting a crystal, you should always specify the load capacitance (C_L). This value can cause variance in the oscillation frequency from the desired specified value (resonance). The load capacitance and the loading of the feedback network have the following relationship:

$$C_L = ((C_1 \bullet C_2)/(C_1 + C_2)) + C_S$$

where C_S is the stray capacitance of the circuit. Placing the crystal and C_L in series across the inverting amplifier and tuning these values (C_1, C_2) allows the crystal to oscillate at resonance. This relationship is true for both fundamental and third-overtone operation. Finally, there is a relationship between $C_1$and C_2. To enhance the oscillation of the inverting amplifier, these values must be offset with the larger load on the output (X2). Equal values of these loads tend to balance the poles of the inverting amplifier.

The characteristics of the inverting amplifier set limits on the following parameters for crystals:

ESR (Equivalent Series Resistance) ..... 40 Ω Max

Drive Level..... 1 mW Max

The recommended range of values for C1and C2 are as follows:

C_1.....15 pF ± 20%

C_2.....22 pF ± 20%

You must determine the specific values for C_1 and C_2. The values are dependent on the characteristics of the chosen crystal and board design. The C_1 and C_2 values include the stray capacitances of the design.

Figure 1 on page 2 shows the correct connection of the oscillator configurations. Figure 1a shows the inverting amplifier configuration. This is the equivalent circuitry with the inverter integrated into the microcontroller. Figure 1b shows the crystal configuration. The diagram shows the correct connection for third-overtone crystals. The fundamental mode crystals do not require the L_1 or the 200-pF capacitor. Figure 1c shows the recommended crystal mode based on the crystal frequency. The 80C186 and 80C188 microprocessors use a crystal twice the CPU frequency and can use either fundamental or third-overtone mode crystals, depending on the CPU frequency.

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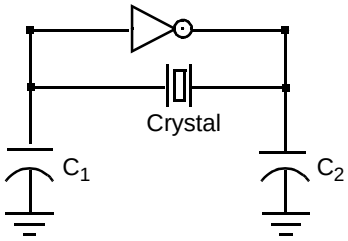
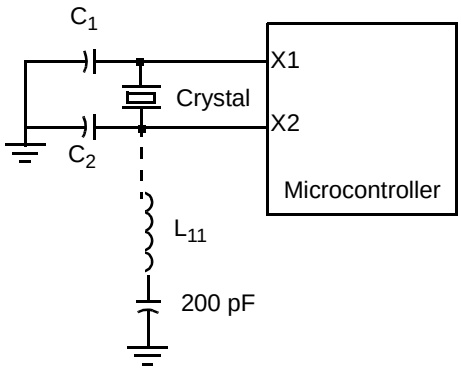


a. Inverting Amplifier Configuration

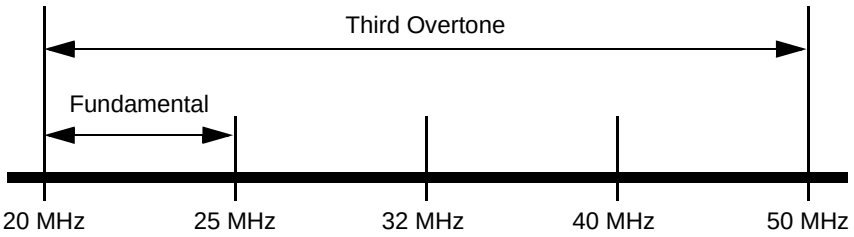


b. Crystal Configuration

Notes:

1. *Use for third overtone mode crystals. Fundamental mode crystals do not use L1 or the 200-pF capacitor.*

XTAL Frequency	***L1 Value (Max)***
20 MHz	*12 μH ±20%*
25 MHz	*8.2 μH ±20%*
32 MHz	*4.7 μH ±20%*
40 MHz	*3.0 μH ±20%*
50 MHz	*2.2 μH ±20%*



c. Recommended Crystal Mode

Figure 1. Oscillator Configurations and Recommended Crystal Modes

SWITCHING CHARACTERISTICS OVER INDUSTRIAL OPERATING RANGE AT 20 MHZ

This section includes the following timings and timing waveforms at 20 MHz:

Read-Cycle Timings[1]

$T_{A\text{-}IND}$=–40°C to +85°C, V_{CC}=5 V ±10%

Parameter			Preliminary 20 MHz		Unit
#	Symbol	Description	Min	Max	
General Timing Requirements (listed more than once)					
1	t_{DVCL}	Data in Setup (A/D)	10		ns
2	t_{CLDX}	Data in Hold (A/D)	3		ns
General Timing Responses (listed more than once)					
3	t_{CHSV}	Status Active Delay	3	29	ns
4	t_{CLSH}	Status Inactive Delay	3	29	ns
5	t_{CLAV}	Address Valid Delay	3	25	ns
6	t_{CLAX}	Address Hold	0		ns
7	t_{CLDV}	Data Valid Delay	3	25	ns
8	t_{CHDX}	Status Hold Time	10		ns
9	t_{CHLH}	ALE Active Delay		20	ns
10	t_{LHLL}	ALE Width	t_{CLCL}–15 = 35		ns
11	t_{CHLL}	ALE Inactive Delay		20	ns
12	t_{AVLL}	Address Valid to ALE Low[2]	t_{CLCH}–10 = 10		ns
13	t_{LLAX}	Address Hold from ALE Inactive[2]	t_{CHCL}–10 = 10		ns
14	t_{AVCH}	Address Valid to Clock High	0		ns
15	t_{CLAZ}	Address Float Delay	t_{CLAX} = 0	17	ns
16	t_{CLCSV}	Chip-Select Active Delay	3	25	ns
17	t_{CXCSX}	Chip-Select Hold from Command Inactive[2]	t_{CLCH}–10 = 10		ns
18	t_{CHCSX}	Chip-Select Inactive Delay	3	20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		ns
20	t_{CVCTV}	Control Active Delay 1[3]	3	22	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	3	22	ns
22	t_{CHCTV}	Control Active Delay 2[3]	3	22	ns
23	t_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	22	ns
Timing Responses (Read Cycle)					
24	t_{AZRL}	Address Float to $\overline{RD}$ Active	0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	3	27	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}$–20 = 80		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	3	25	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[2]	t_{CLCH}–10 = 10		ns
29	t_{RHAV}	$\overline{RD}$ Inactive to Address Active[2]	t_{CLCL}–15 = 35		ns

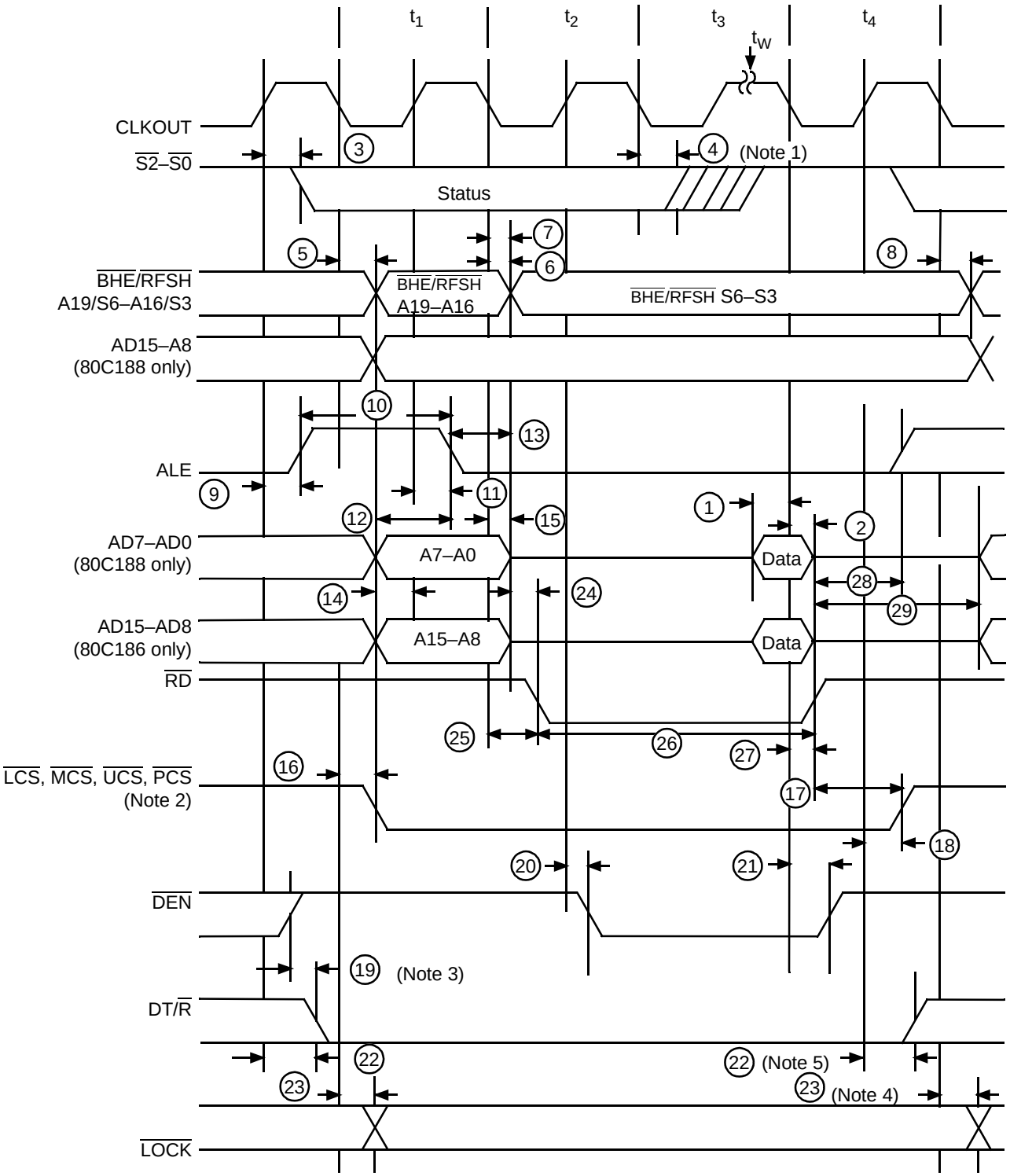
Notes:

1. All timings are measured at 1.5 V and 100-pF loading on CLKOUT unless otherwise noted. All output test conditions are with C_L = 50–100 pF (10–20 MHz). For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

2. Equal loading.

3. $\overline{DEN}$, $\overline{INTA}$, $\overline{WR}$.

Read-Cycle Waveforms



Notes:

1. *Status inactive in state preceding t_4.*
2. *If latched, A1 and A2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$; only t_{CLCSV} is applicable.*
3. *For write cycle followed by read cycle.*
4. *t_1 of next bus cycle.*
5. *Changes in t-state preceding next bus cycle if followed by write.*

Write-Cycle Timings[1]

$T_{A\text{-}IND}$ = –40°C to + 85°C, V_{CC} = 5 V ± 10%

Parameter			Preliminary 20 MHz		Unit
#	Symbol	Description	Min	Max	
General Timing Responses (listed more than once)					
3	t_{CHSV}	Status Active Delay	3	29	ns
4	t_{CLSH}	Status Inactive Delay	3	29	ns
5	t_{CLAV}	Address Valid Delay	3	25	ns
6	t_{CLAX}	Address Hold	0		ns
7	t_{CLDV}	Data Valid Delay	3	25	ns
8	t_{CHDX}	Status Hold Time	10		ns
9	t_{CHLH}	ALE Active Delay		20	ns
10	t_{LHLL}	ALE Width	t_{CLCL}–15 = 35		ns
11	t_{CHLL}	ALE Inactive Delay		20	ns
12	t_{AVLL}	Address Valid to ALE Low[2]	t_{CLCH}–10 = 10		ns
13	t_{LLAX}	Address Hold from ALE Inactive[2]	t_{CHCL}–10 = 10		ns
14	t_{AVCH}	Address Valid to Clock High	0		ns
16	t_{CLCSV}	Chip-Select Active Delay	3	25	ns
17	t_{CXCSX}	Chip-Select Hold from Command Inactive[2]	t_{CLCH}–10 = 10		ns
18	t_{CHCSX}	Chip-Select Inactive Delay	3	20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		ns
20	t_{CVCTV}	Control Active Delay 1[3]	3	22	ns
23	t_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	22	ns
Timing Responses (Write Cycle)					
30	t_{CLDOX}	Data Hold Time	3		ns
31	t_{CVCTX}	Control Inactive Delay[3]	3	22	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}$–20 = 80		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[2]	t_{CLCH}–14 = 6		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[2]	t_{CLCL}–15 = 35		ns
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive[2]	t_{CLCH}–10 = 10		ns

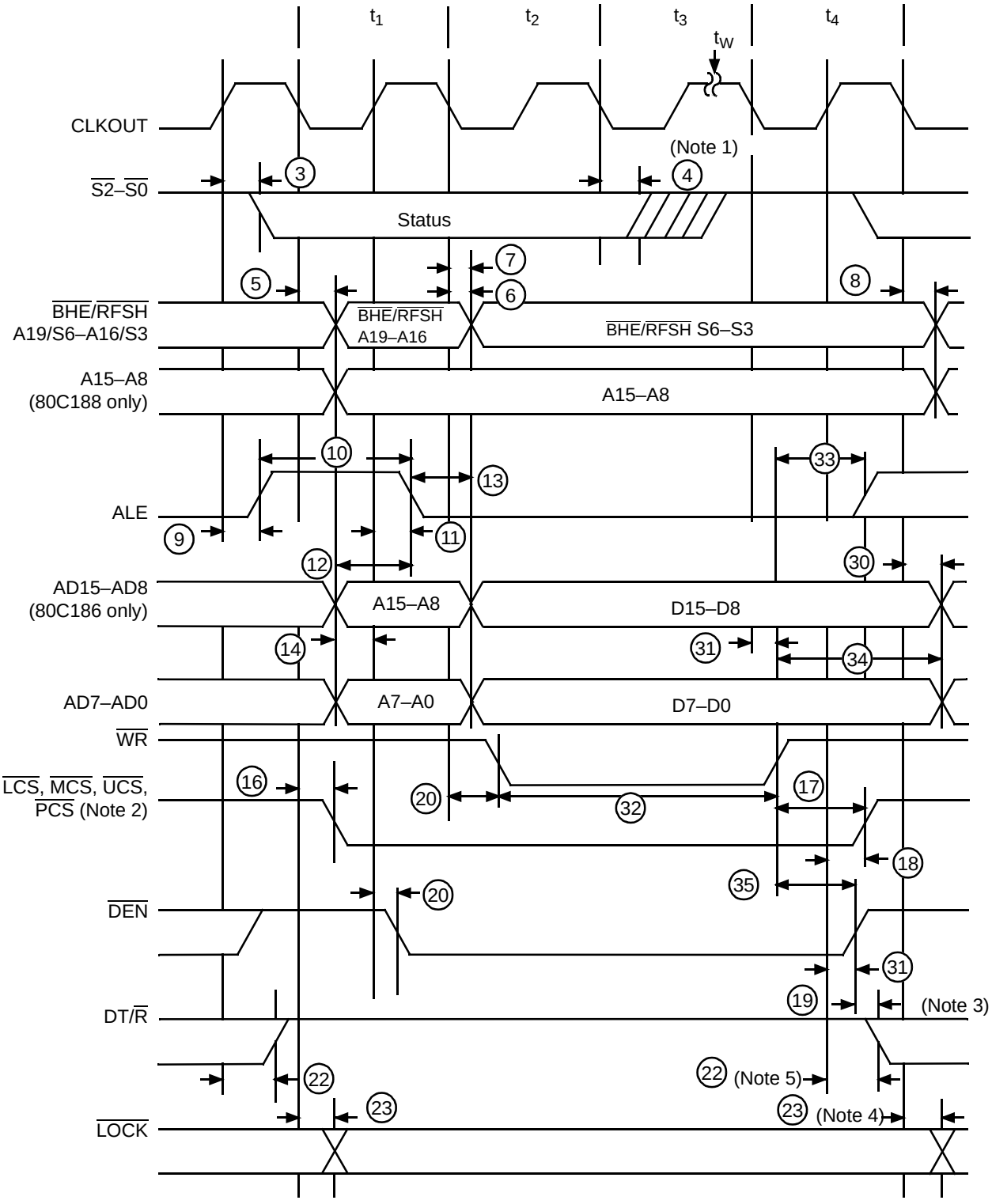
Notes:

1. All timings are measured at 1.5 V and 100-pF loading on CLKOUT unless otherwise noted. All output test conditions are with C_L = 50–100 pF (10–20 MHz). For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

2. Equal loading.

3. $\overline{DEN}$, $\overline{INTA}$, $\overline{WR}$.

Write-Cycle Waveforms



Notes:

1. *Status inactive in state preceding t_4.*
2. *If latched, A1 and A2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$; only t_{CLCSV} is applicable.*
3. *For write cycle followed by read cycle.*
4. *t_1 of next bus cycle.*
5. *Changes in t-state preceding next bus cycle if followed by read, $\overline{INTA}$, or halt.*

Interrupt Acknowledge Cycle Timings[1]

T_A = –40°C to +85°C, V_{CC} = 5 V ± 10%

Parameter			Preliminary 20 MHz		Unit
#	Symbol	Description	Min	Max	
80C186 General Timing Requirements (listed more than once)					
1	t_{DVCL}	Data in Setup (A/D)	10		ns
2	t_{CLDX}	Data in Hold (A/D)	3		ns
80C186 General Timing Responses (listed more than once)					
3	t_{CHSV}	Status Active Delay	3	29	ns
4	t_{CLSH}	Status Inactive Delay	3	29	ns
5	t_{CLAV}	Address Valid Delay	3	25	ns
6	t_{CLAX}	Address Hold	0		ns
7	t_{CLDV}	Data Valid Delay	3	25	ns
8	t_{CHDX}	Status Hold Time	10		ns
9	t_{CHLH}	ALE Active Delay		20	ns
10	t_{LHLL}	ALE Width	t_{CLCL}–15 = 35		ns
11	t_{CHLL}	ALE Inactive Delay		20	ns
12	t_{AVLL}	Address Valid to ALE Low[2]	t_{CLCH}–10 = 10		ns
13	t_{LLAX}	Address Hold from ALE Inactive[2]	t_{CHCL}–10 = 10		ns
14	t_{AVCH}	Address Valid to Clock High	0		ns
15	t_{CLAZ}	Address Float Delay	t_{CLAX} = 0	17	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[2]	0		ns
20	t_{CVCTV}	Control Active Delay 1[3]	3	22	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycles)	3	22	ns
22	t_{CHCTV}	Control Active Delay 2[3]	3	22	ns
23	t_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	22	ns
31	t_{CVCTX}	Control Inactive Delay[3]	3	22	ns

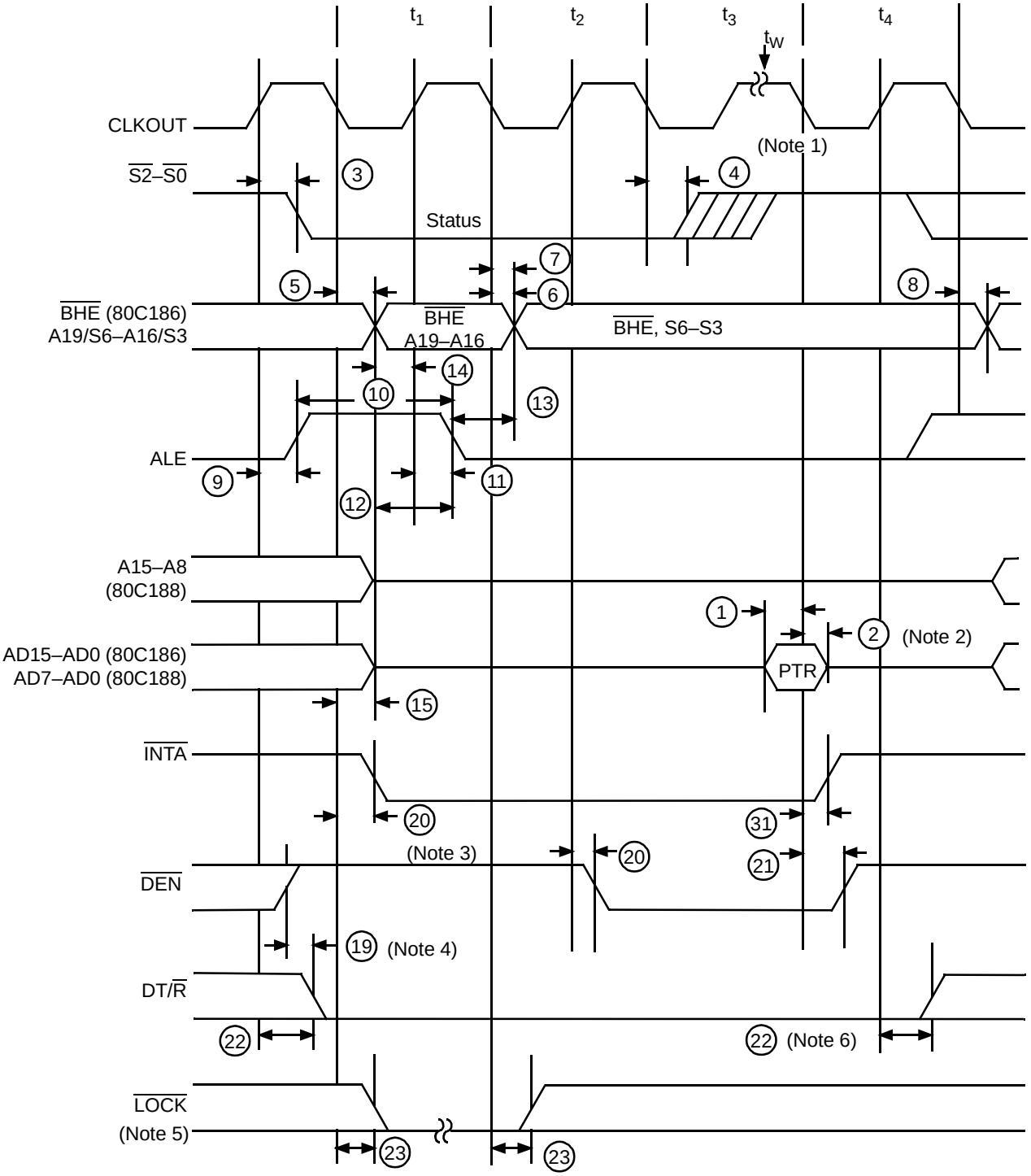
Notes:

1. All timings are measured at 1.5 V and 100-pF loading on CLKOUT unless otherwise noted. All output test conditions are with C_L = 50–200 pF (10 MHz) and C_L = 50–100 pF (12.5–20 MHz). For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

2. Equal loading.

3. $\overline{DEN}$, $\overline{INTA}$, $\overline{WR}$.

Interrupt Acknowledge Cycle Waveforms



Notes:

1. *Status inactive in state preceding t_4.*
2. *The data hold time lasts only until $\overline{INTA}$ goes inactive, even if the $\overline{INTA}$ transition occurs prior to t_{CLDX} (min).*
3. *$\overline{INTA}$ occurs one clock later in Slave mode.*
4. *For write cycle followed by interrupt acknowledge cycle.*
5. *$\overline{LOCK}$ is active upon t_1 of the first interrupt acknowledge cycle and inactive upon t_2 of the second interrupt acknowledge cycle.*
6. *Changes in t-state preceding next bus cycle if followed by write.*

Software Halt Cycle Timings[1]

T_A = –40°C to 85°C, V_{CC} = 5 V ± 10%

Parameter			Preliminary 20 MHz		Unit
#	Symbol	Description	Min	Max	
80C186 General Timing Responses (listed more than once)					
3	t_{CHSV}	Status Active Delay	3	29	ns
4	t_{CLSH}	Status Inactive Delay	3	29	ns
5	t_{CLAV}	Address Valid Delay	3	25	ns
9	t_{CHLH}	ALE Active Delay		20	ns
10	t_{LHLL}	ALE Width	t_{CLCL}–15 = 35		ns
11	t_{CHLL}	ALE Inactive Delay		20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[2]	0		ns
22	t_{CHCTV}	Control Active Delay 2[3]	3	22	ns

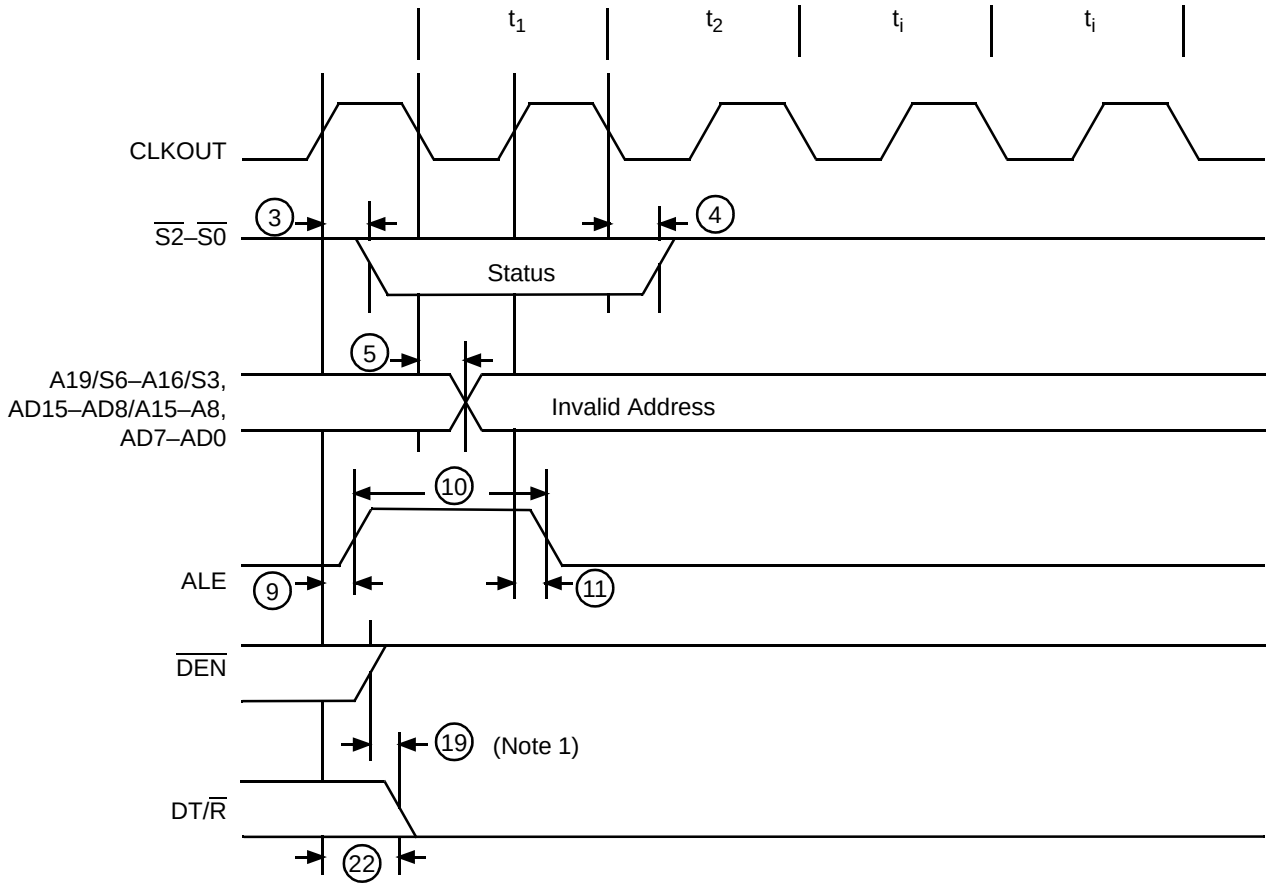
Notes:

1. All timings are measured at 1.5 V and 100-pF loading on CLKOUT unless otherwise noted. All output test conditions are with C_L = 50–200 pF (10 MHz) and C_L = 50–100 pF (12.5–20 MHz). For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

2. Equal loading.

3. $\overline{DEN}$, $\overline{INTA}$, $\overline{WR}$.

Software Halt Cycle Waveforms



Notes:

1. For write cycle followed by halt cycle.

Clock Timings[1]

$T_{A\text{-}IND}$ = –40°C to +85°C, V_{CC} = 5 V ± 10%

Parameter			Preliminary 20 MHz		Unit
#	Symbol	Description	Min	Max	
CLKIN Requirements—measurements taken with external clock input to X1 and X2 not connected (float)					
36	t_{CKIN}	CLKIN Period	25		ns
37	t_{CLCK}[2]	CLKIN Low Time 1.5 V[3]	7		ns
38	t_{CHCK}[2]	CLKIN High Time 1.5 V[3]	8		ns
39	t_{CKHL}	CLKIN Fall Time 3.5 – 1.0 V		5	ns
40	t_{CKLH}	CLKIN Rise Time 1.0 – 3.5 V		5	ns
CLKOUT Timing					
41	t_{CICO}	CLKIN to CLKOUT Skew		17	ns
42	t_{CLCL}	CLKOUT Period	50		ns
43	t_{CLCH}	CLKOUT Low Time C_L = 50 pF[4]	0.5 t_{CLCL} –5 = 20		ns
		C_L = 100 pF[3]	0.5 t_{CLCL} –7 = 18		
44	t_{CHCL}	CLKOUT High Time C_L = 50 pF[4]	0.5 t_{CLCL} –5 = 20		ns
		C_L = 100 pF[5]	0.5 t_{CLCL} –7 = 18		
45	t_{CH1CH2}	CLKOUT Rise Time 1.0–3.5 V		8	ns
46	t_{CL2CL1}	CLKOUT Fall Time 3.5 – 1.0 V		8	ns

Notes:

1. All timings are measured at 1.5 V and 100-pF loading on CLKOUT unless otherwise noted. All output test conditions are with C_L = 50–100 pF (10–20 MHz). For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

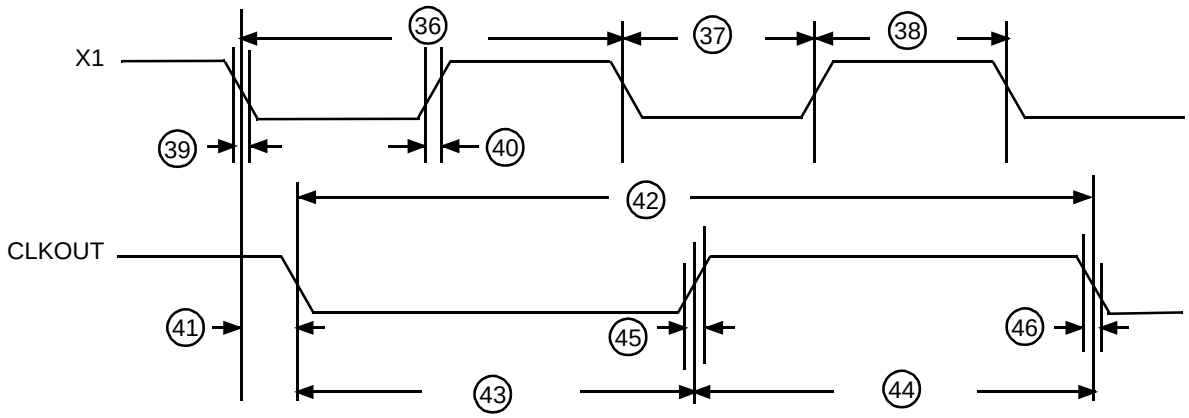
2. t_{CLCK} and t_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of t_{CKIN}.

3. Tested under worst case conditions: V_{CC} = 5.5 V @ 20 MHz, T_A = 70°C.

4. Not tested.

5. Tested under worst case conditions: V_{CC} = 4.5 V @ 20 MHz, T_A = 0°C.

Clock Waveforms



Ready, Peripheral, and Queue Status Timings[1]

$T_{A\text{-}IND}$ = –40°C to +85°C, V_{CC} = 5 V ± 10%

Parameter			Preliminary 20 MHz		Unit
#	Symbol	Description	Min	Max	
Ready and Peripheral Timing Requirements					
47	t_{SRYCL}	SRDY Transition Setup Time[2]	15		ns
48	t_{CLSRY}	SRDY Transition Hold Time[2]	10		ns
49	t_{ARYCH}	ARDY Res. Transition Setup Time[3]	10		ns
50	t_{CLARX}	ARDY Active Hold Time[2]	10		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	10		ns
52	t_{ARYLCL}	ARDY Setup Time[2]	20		ns
53	t_{INVCH}	Peripheral Setup[3]: INTx, NMI, TMR IN, $\overline{TEST}$/BUSY	15		ns
54	t_{INVCL}	DRQ0, DRQ1 Setup Time[3]	15		ns
Peripheral and Queue Status Timing Responses					
55	t_{CLTMV}	Timer Output Delay		22	ns
56	t_{CHQSV}	Queue Status Delay		23	ns

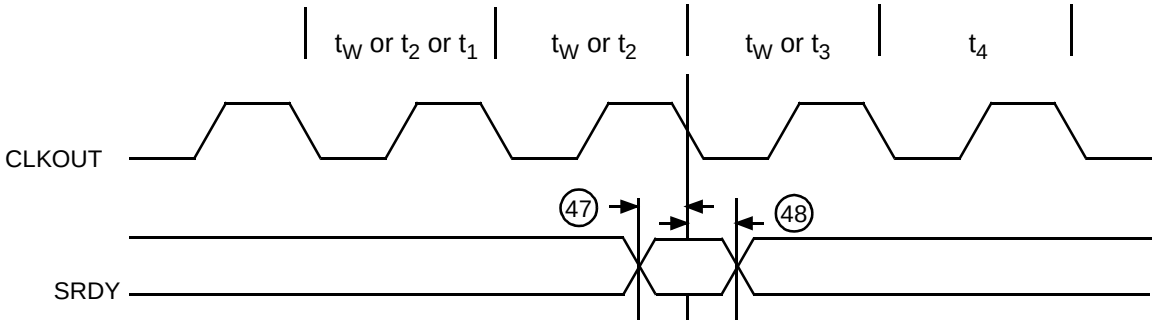
Notes:

1. All timings are measured at 1.5 V and 100-pF loading on CLKOUT unless otherwise noted. All output test conditions are with C_L = 50–100 pF (10–20 MHz). For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

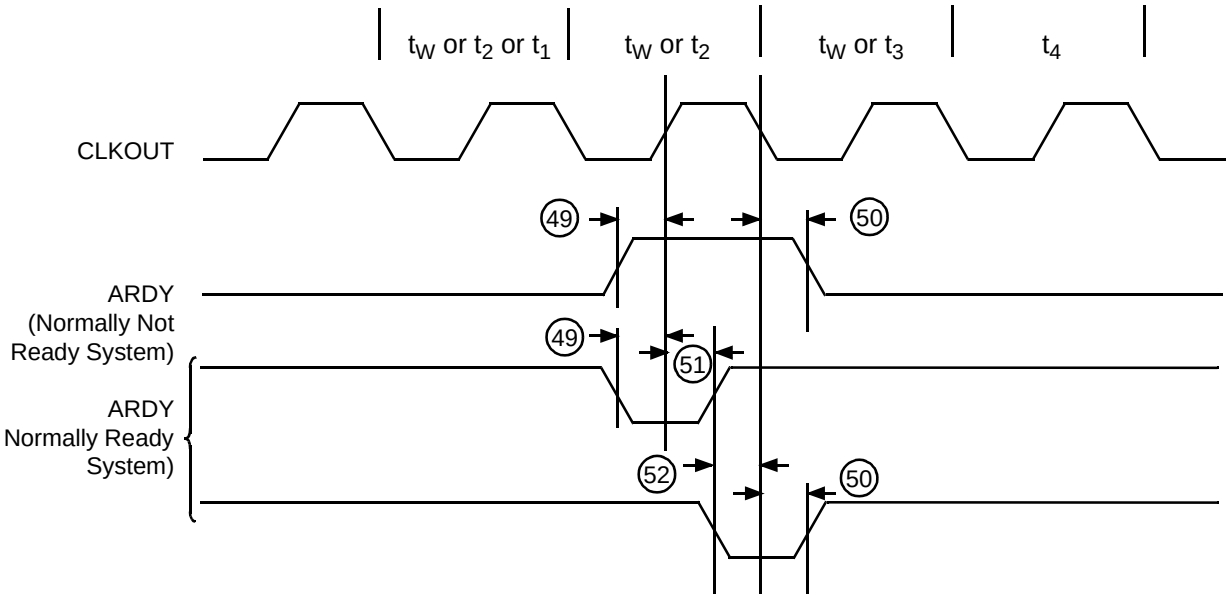
2. To guarantee proper operation.

3. To guarantee recognition at clock edge.

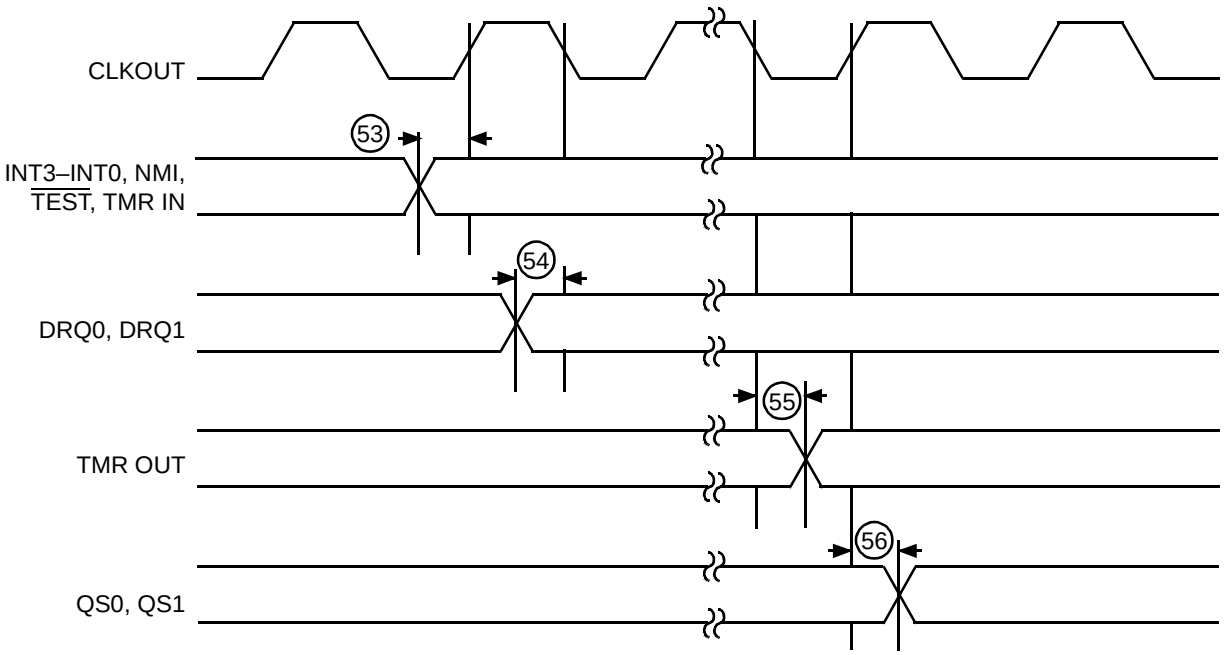
Synchronous Read (SRDY) Waveforms



Asynchronous Ready (ARDY) Waveforms



Peripheral and Queue Status Waveforms



RESET and HOLD/HLDA Timings[1]

$T_{A\text{-}IND}$ = –40°C to +85°C, V_{CC} = 5 V ± 10%

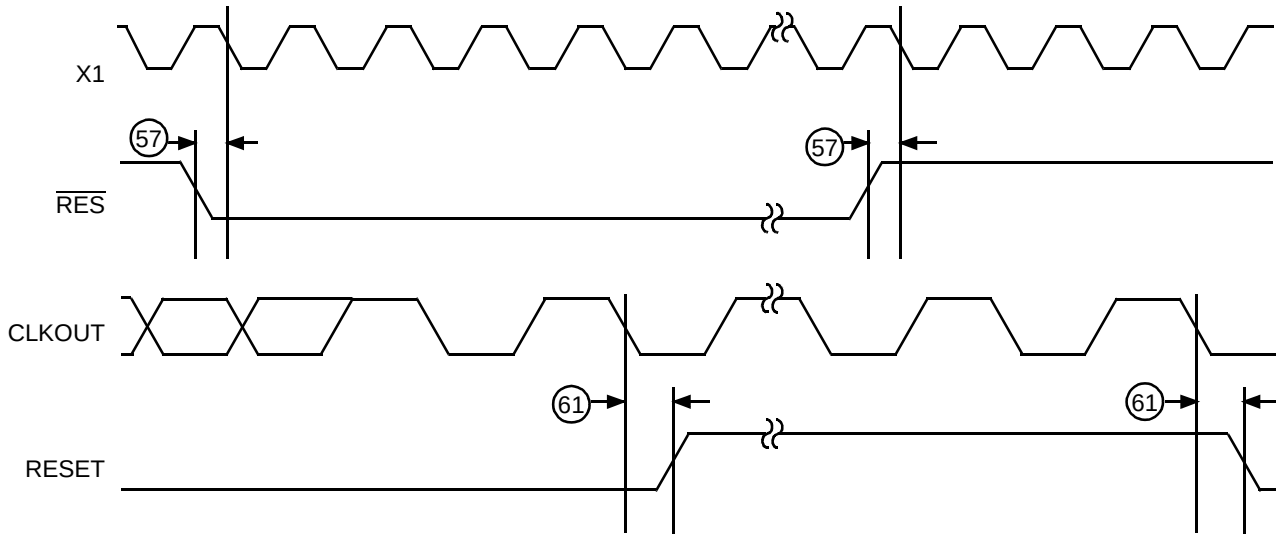
Parameter			Preliminary 20 MHz		Unit
#	Symbol	Description	Min	Max	
RESET and HOLD/HLDA Timing Requirements					
57	t_{RESIN}	RES Setup	10		ns
58	t_{HVCL}	HOLD Setup[2]	10		ns
15	t_{CLAZ}	Address Float Delay	0	17	ns
5	t_{CLAV}	Address Valid Delay	3	25	ns
RESET and HOLD/HLDA Timing Requirements					
61	t_{CLRO}	Reset Delay		22	ns
62	t_{CLHAV}	HLDA Valid Delay	3	22	ns
63	t_{CHCZ}	Command Lines Float Delay		25	ns
64	t_{CHCV}	Command Lines Valid Delay (after Float)		25	ns

Notes:

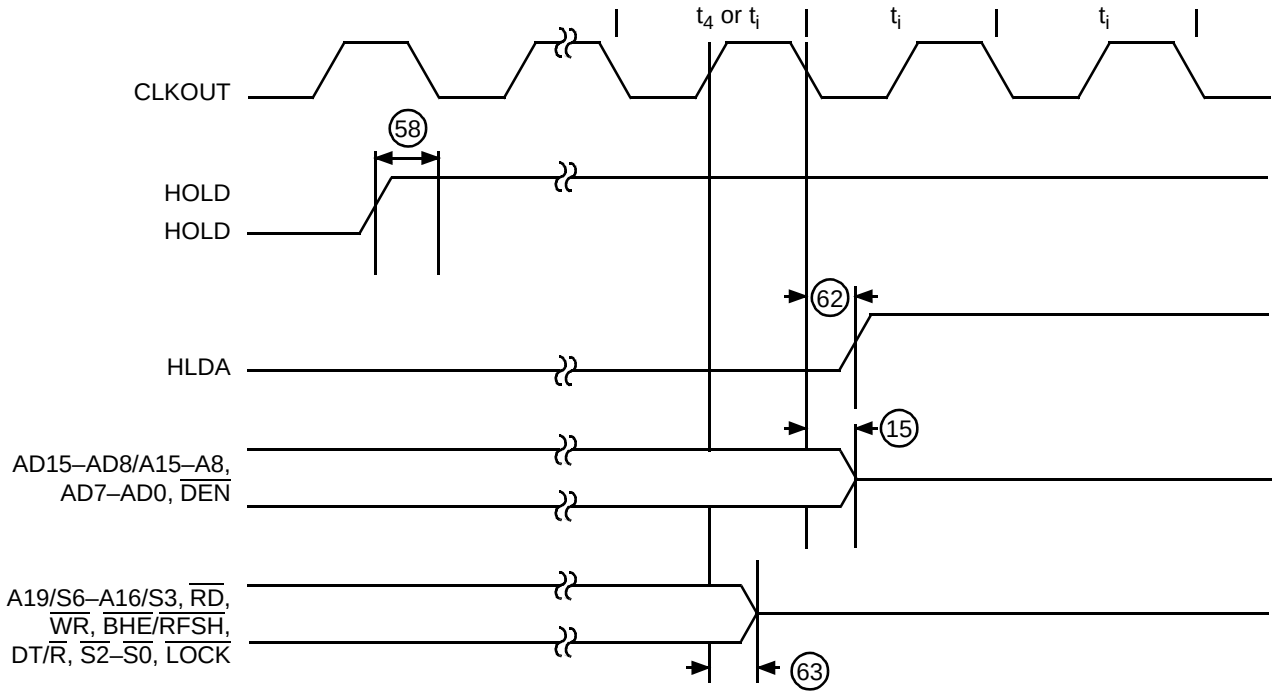
1. All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted. All output test conditions are with C_L = 50–100 pF (10–20 MHz). For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

2. To guarantee recognition at next clock.

RESET Waveforms



HOLD/HLDA Waveforms (Entering HOLD)



HOLD/HLDA Waveforms (Leaving HOLD)