Phase Lock Loop (PLL) Clock Control

Advanced Micro Devices

Application Note

Significant system power savings can be achieved by using the Phase Lock Loop (PLL) clock control circuit outlined in this application note with any Am486® or Am5$_X$86™ family microprocessor.

The Environmental Protection Agency's (EPA) Energy Star program, unveiled during the summer of 1992, provided the personal computer (PC) industry with a voluntary incentive to reduce desktop PC power consumption. The prime directive of the EPA's Energy Star program is that no more than 30 W will be consumed in low power mode for each of the following system components: the personal computer itself, the monitor, and the printer.

The Am486DX2-80 microprocessor serves as an example in this application note, illustrating how the Phase Lock Loop clock control circuit can enable your design to include an efficient and energy-saving clock control mechanism.

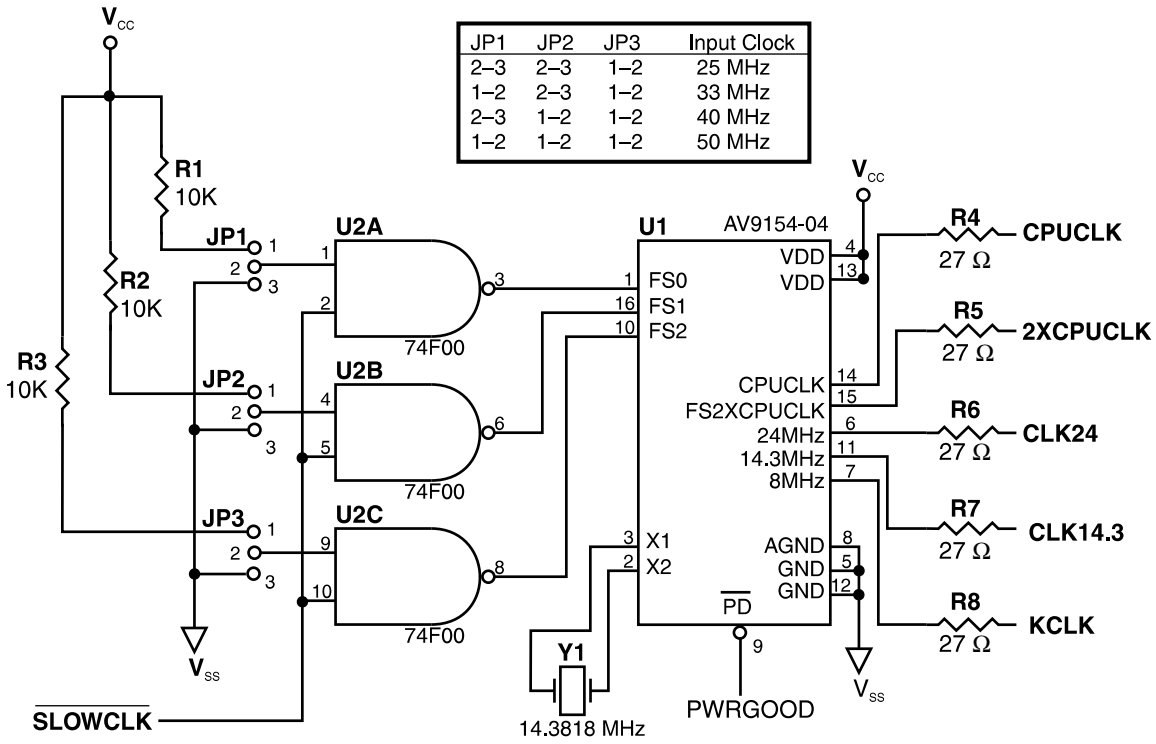
Power Consumption

The CPU accounts for a significant part of system power consumption. The data sheet typical I_{CC} for the 3.3-V Am486DX2-80 microprocessor is 640 mA, which translates to a typical power consumption of 2.1 W.

Using the simple Phase Lock Loop (PLL) clock control circuit with any member of the Am486 or Am5$_X$86 microprocessor family enables system power consumption to be significantly lowered. This feature assists designers in meeting the Energy Star requirements.

A typical motherboard, including an Am486DX2-80 CPU, consumes around 13 W, meaning that the CPU accounts for approximately 16 percent of the total motherboard power consumption. By controlling the clock, via the methods described in this application note, the CPU component of the motherboard power consumption can be reduced by approximately 90 percent (See Table 1). Overall motherboard power consumption is also lowered by the reduced clock speed.

Figure 1. Phase Lock Loop (PLL) Clock Control Circuit



Note: *This circuit may not be appropriate for all motherboard designs. To maintain proper system operation, ensure all other system clocks conform to required specifications when implementing this circuit in a design.*

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$\overline{\text{SLOWCLK}}$ For Power Savings

Because Phase Lock Loop clocks are not static, they may not be turned off or driven at a frequency less than 8 MHz. Furthermore, the frequency of the CPU clock cannot be changed more than 0.1 percent cycle-to-cycle per the data sheet specification. The designer must ensure this specification is met or the PLL will lose its lock and unstable operation will result.

The $\overline{\text{SLOWCLK}}$ signal is common to all three of the 74F00 NAND gates, and is normally High. Following a user-defined time-out, $\overline{\text{SLOWCLK}}$ is driven Low by any control line. With $\overline{\text{SLOWCLK}}$ Low, the outputs of all three of the 74F00 NAND gates are High, which selects an output frequency of 8 MHz from the frequency generator. Once activity is detected, $\overline{\text{SLOWCLK}}$ goes High, reselecting the full-on frequency. (See Figure 1).

Table 1. I_{CC} Values for Am486DX-80 CPU (V_{CC}=3.3 V)

Operating Frequency	Typical Power Supply Current (I_{CC})
8 MHz ($\overline{\text{SLOWCLK}}$)	64 mA
80 MHz	640 mA

$\overline{\text{SLOWCLK}}$ CONTROL

The AV9154-04 slowly ramps the CPU clock down to 8 MHz and may be driven by any general purpose output, or any other control line.

One solution is to use this clock control solution with Phoenix Technologies' Multikey/42G energy-efficient keyboard controller. Implement the Multikey/42G solution by replacing the system's standard 8042 keyboard controller with the Mulitkey/42G. Available in either a 40-pin Dual In-line package (DIP) or 44-pin Plastic Leaded Chip Carrier (PLCC) package, the Multikey/42G solution uses one of the unused 8042 port signals, (P1.1 to P1.7, or P2.0 to P2.3), to control the $\overline{\text{SLOWCLK}}$ signal.

Once the Multikey/42G keyboard controller is configured, Phoenix Technologies' FOCUS utility, provided as part of this solution, runs as a standard or TSR utility. The FOCUS utility permits refinements to the initial configuration, such as timer settings, which turn off the hard disk(s) after a period of inactivity.

POWER SAVINGS

Clock control solutions, evaluated in the Advanced Micro Devices laboratory, have shown significant power savings of over 4 W. Placing a power-managed hard disk drive in standby mode can account for an additional system power savings of 2.2 W, resulting in a total possible system savings of 6.2 W.

***Note**: Care should be taken when slowing the CPU clock in systems where other clocks are derivatives of the CPU clock. The designer must ensure that all system timing requirements are maintained when changing the frequency of the clock to the microprocessor.*

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