Technical Bulletin

Arbiter Solution for Shared-Bus Systems Using the Am29030™ or Am29035™ Microprocessor

EPD Systems Engineering

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Purpose

The Revision D Am29030 and Am29035 microprocessors inappropriately assert the $\overline{\text{REQ}}$ signal after $\overline{\text{BGRT}}$ is deasserted. In doing so, they create the potential for a bus collision in *shared-bus systems*. This bulletin includes the PAL equations for a state machine used in an EB29030™ board to prevent bus collisions. These equations may be revised to suit a particular arbiter design.

Affected Parts

The information in this bulletin affects the following parts:

Device	Revision
Am29030 microprocessor	B, D
Am29035 microprocessor	B, D

If You Need Assistance

Product support for the 29K Family processors is available from our Embedded Processor Division (EPD) Technical Support Hotlines located in the U.S. and in the U.K.

Assistance is available in the U.S. from 9:00 A.M. to 6:00 P.M. central time, Monday through Friday (except major holidays). In Europe assistance is available during U.K. business hours. Contact us at one of the following numbers:

To reach the U.S.

From	Call
U.S.	1-800-2929-AMD
U.K.	0-800-89-1455
Japan	0031-11-1163
Any other location	+1-512-462-4118†

†Toll applies.

To reach the U.K.

From	Call
U.K.	(0)256-811101
France	0590-8621
Germany	0130-813875
Italy	1678-77224
Any other location	+44-(0)256-811101†

†Toll applies.

Example PAL Equations for the EB29030 Board Arbiter (in PLPL)

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"DEFINITIONS"
"030     = Am29030 or Am29035 microprocessor"
"AT      = PC AT"
"EB29030 = Am29030 Execution Board"

"NOTE"
"These PAL equations were designed for a state machine used in an EB29030"
"board.  These equations may be revised to suit a particular arbiter"
"design."

"U17 performs arbitration of 030 and AT access requests to EB29030 memory,"
"as well as freeing memory for refresh when posted by the AT."

"Rev 11 removes *BREQ from the arbitration, using *REQ and *BGRT only."

"Rev 12 implements pseudo-arbitration.  It relies on the 030 to relinquish"
"the bus by deasserting *REQ.  This is the only arbitration scheme for"
"Rev D in the EB29030 board."

DEVICE Arbitrat (p22v10)
PIN               "The PAL pin names and architectural features follow."

"Input pin definitions"

MEMCLK      = 1 (Clock)
/ATACCPLT   = 2 (Input Combinatorial)   "AT access complete"
/ATACRDY    = 3 (Input Combinatorial)   "AT access ready"
/BREQ       = 4 (Input Combinatorial)   "030 bus request"
/ATACREQ    = 5 (Input Combinatorial)   "AT access request"
/REFREQ     = 6 (Input Combinatorial)   "AT refresh request"
/REFECPLT   = 7 (Input Combinatorial)   "Even bank refresh complete"
/REFOCPLT   = 8 (Input Combinatorial)   "Odd bank refresh complete"
/RESET      = 9 (Input Combinatorial)   "Hardware reset"
/CASODD     = 10 (Input Combinatorial)  "Odd bank access complete"
/CASEVEN    = 11 (Input Combinatorial)  "Even bank access complete"
/REQ        = 13 (Input Combinatorial)  "030 request"
EXREFCPLT   = 14 (Input Combinatorial)  "EB29030 board refresh complete"
/ERLYA      = 23 (Input Combinatorial)  "030 early address mode"
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"Output pin definitions"

/state[4]   = 22 (Output Registered Active_low)  "SV4 and ATACGRNT"
/state[5]   = 21 (Output Registered Active_low)  "SV5 and ATACACK"
/state[0]   = 20 (Output Registered Active_low)  "SV0"
/state[1]   = 19 (Output Registered Active_low)  "SV1"
/state[2]   = 18 (Output Registered Active_low)  "SV2"
/state[3]   = 17 (Output Registered Active_low)  "SV3"
/state[7]   = 16 (Output Registered Active_low)  "SV7 and BGRT"
/state[6]   = 15 (Output Registered Active_low); "SV6 and REFACT"

Begin       "The logic definition and operation of the state machine is"
            "contained within this Begin-End construct."

Enable(/state[7]);
Enable(/state[6]);
Enable(/state[5]);
Enable(/state[4]);
Enable(/state[3]);
Enable(/state[2]);
Enable(/state[1]);
Enable(/state[0]);

If (RESET) then
   Begin
   "BGRT = 0"
   /state [7:0] = 126;
   End;
Else
   Case (/state [7:0])
      Begin

      126 ) Begin
                     "BGRT = 0"
                     "Let 030 have the bus upon reset or if no refresh"
                     "nor AT Access Request is outstanding."
            If (REFREQ * /ERLYA) then
               /state [7:0] = 127;    "Refresh request arrives."
            Else If (/REFREQ * ATACREQ * /ERLYA) then
               /state [7:0] = 124;    "AT host access request arrives."
            Else
               /state [7:0] = 126;    "Stay 126 if there is no request."
            End;
```

```
127 ) Begin
                "BGRT = 0"
                "Synchronize a refresh request from the AT with"
                "arbitration logic in this device."
      If (/REFREQ) then
         /state [7:0] = 126;    "REFREQ set-up time missed this cycle."
      Else If (/REQ) then
         /state [7:0] = 255;    "Move to 255 when *REQ deasserts."
      Else
         /state [7:0] = 127;    "Wait until 030 relinquishes bus."
      End;

255 ) Begin
      /state [7:0] = 243;       " *BGRT is deasserted in this cycle."
      End;

243 ) Begin
      If (/REQ) then
         /state [7:0] = 242;
      Else
         /state [7:0] = 243;
      End;

242 ) Begin
                "Work-around for 030 bug found 8-25-91 where 030"
                "asserts *REQ even after *REQ deassert from *BGRT"
                "deassertion."
      If (REQ) then
         /state [7:0] = 243;
      Else
         /state [7:0] = 191;
      End;

191 ) Begin
                "REFACT = 0"
                "Refresh Active is now asserted indicating that a"
                "refresh can begin by each bank ras/cas/refresh PAL."
                "This is the holding state which we remain in until"
                "both halves have completed their respective refresh"
                "cycle."
      If (/REFECPLT + /REFOCPLT + /EXREFCPLT) then
         /state [7:0] = 191;
      If (REFECPLT * REFOCPLT * EXREFCPLT) then
         /state [7:0] = 126;
      End;
```

```
124 ) Begin
                "BGRT = 0"
                "Synchronize an AT access request with the arbitration"
                "state machine."
      If (/ATACREQ) then
         /state [7:0] = 126;    "Set-up time was satisfied."
      Else If (/REQ) then
         /state [7:0] = 252;    "Move to 252 when *REQ deasserts."
      Else
         /state [7:0] = 124;    "Wait until 030 relinquishes bus."
      End;

252 ) Begin
      /state [7:0] = 246;       " *BGRT is deasserted here."
      End;

246 ) Begin
      If (/REQ) then
         /state [7:0] = 240;
      Else
         /state [7:0] = 246;
      End;

240 ) Begin
                "Work-around for 030 bug found 8-25-91 where 030"
                "asserts *REQ even after *BGRT is deasserted."
      If (REQ) then
         /state [7:0] = 246;
      Else
         /state [7:0] = 220;
      End;

220 ) Begin
                "ATACACK = 0"
                "AT Access Acknowledge is now asserted indicating that"
                "the AT can have the bus.  We wait here until the AT"
                "is ready to proceed with its access."
                "Synchronization of its ready status is also performed"
                "in this and the next adjacent state."
      If (/ATACRDY) then
         /state [7:0] = 220;
      Else
         /state [7:0] = 212;
      End;
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```
      212 ) Begin
                  "ATACACK = 0"
            If (/ATACRDY) then
               /state [7:0] = 220;
            Else
               /state [7:0] = 228;
            End;

      228 ) Begin
                  "ATACGRNT = 0"
                  "This arbitration logic now informs the"
                  "simple/page-mode PAL to perform a simple access to"
                  "the appropriate bank while waiting for the access to"
                  "be completed."
            If (/CASODD * /CASEVEN) then
               /state [7:0] = 228;
            If (CASODD + CASEVEN) then
               /state [7:0] = 245;
            End;

      245 ) Begin
                  "The AT arbitration logic will inform this logic that"
                  "its bus cycle is complete by asserting AT Access"
                  "Complete, but synchronization is required between it"
                  "and this PAL, i.e., different clocks."
            If (/ATACCPLT) then
               /state [7:0] = 245;
            Else
               /state [7:0] = 253;
            End;

      253 ) Begin
            If (/ATACCPLT) then
               /state [7:0] = 245;
            Else
               /state [7:0] = 126;
            End;

      End;

End.
```