Technical Bulletin

Byte and Half-Word Addressing in the Am29030 and Am29035 Microprocessors

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Purpose

This bulletin elaborates on byte and half word addressing for the Am29030 and Am29035 microprocessors. In addition, it provides a correction to a table in the *Am29030 and Am29035 Microprocessors User's Manual and Data Sheet*.

Affected Parts and Documentation

This bulletin affects the following parts:

Device	Revision
Am29030 microprocessor	All
Am29035 microprocessor	All

This bulletin affects the following documentation:

PID No.	Title
15723C	*Am29030 and Am29035 Microprocessors User's Manual and Data Sheet*

Byte and Half-Word Addressing

All 29K Family processors use big-endian byte ordering for *internal* registers. However, the Am29030 and Am29035 processors can access *external memory* using big- or little-endian format. The Byte Order (BO) bit of the configuration register sets the endian orientation. Big-endian orientation (BO=0) places the most significant bit (MSB) of data at the address "x..x00" and the least significant bit (LSB) of data at address "x..x11". Little-endian orientation (BO=1) places the MSB at "x..x11" and the LSB at "x..x00".

Byte Orientation	General Register	Memory Location ("x..x00")
Big endian (BO=0)	aa bb cc dd	aa bb cc dd
Little endian (BO=1)	aa bb cc dd	dd cc bb aa

For all external byte and half-word accesses, the selection of a byte within an external word is determined by the two LSBs of an address and the BO bit. The selection of a half-word within an external word is determined by the next-to-least significant bit of an address and the BO bit.

Additionally, the Option field in load and store instructions determine byte, half-word, or word accesses for the processor. However, for the EXBYTE, EXHW, EXHWS, INBYTE, and INHW instructions, the Byte Pointer (BP) field of the ALU Status Register determines the position of the half-word within the word. Restated, when these five instructions are executed, the appropriate value of the BP field preempts the LSBs of the address to determine the position of the byte or half-word.

Finally, for all word and half-word accesses, the Am29030 and Am29035 processors will either ignore or force alignment in most cases. Thus, half-word accesses are forced to be aligned to half-word boundaries. The processor will trap when an unaligned half-word access is attempted, which emulates the non-aligned access in trap code. The processor will perform unaligned byte accesses. (Note that this assumes the CPS:TU bit is set. If the CPS:TU bit is clear, data memory alignment is ignored. This is described in more detail in Section 3.3.7.3 of the user's manual.)

For big-endian orientation (BO=0), bytes are ordered within words such that a 00 in the BP field or in the least-significant address bits selects the high-order byte of a word; a 11, the low-order byte of a word. Again, the BP field is only referenced for the EXBYTE, EXHW, EXHWS, INBYTE, and INHW instructions.

For little-endian orientation (BO=1), a 00 in the BP field or in the two least-significant address bits selects the low-order byte of a word. A value of 11 selects the high-order byte.

For a half-word access, only the MSB of the BP field or the next-to-least-significant address bit selects the appropriate half-word. Since the LSB of the BP field or the address bits do not determine the half-word selection, the alignment of half-word data types are

positioned on half-word boundaries. Specifically, if BO=0 and the BP field or least-significant address bits are 0x (where x can be anything), the high order half-word will be selected and so on. The following table summarizes the use of the BO, BP and least-significant address bits for byte and half-word accesses.

BO	BP/Least Significant Address Bits	Selected Byte
0	00	High order byte
0	01	Second highest order byte
0	10	Second lowest order byte
0	11	Low order byte
1	00	Low order byte
1	01	Second lowest order byte
1	10	Second highest order byte
1	11	High order byte
		Selected Half-Word
0	00	High order half-word
0	10	Low order half-word
1	00	Low order half-word
1	10	High order half-word

There is a correction necessary to the *Am29030 and Am29035 Microprocessors User's Manual and Data Sheet, 1993/1994.* The table in Section 10.4.4 on page 10-11 in the manual is correctly shown below.

BO	OPT(2-0)	A(1-0)	$\overline{\text{BWE}}$(3-0)	On Write
0	001	00	0111	MSB, big endian
0	001	01	1011	
0	001	10	1101	
0	001	11	1110	LSB, big endian
0	010	0x	0011	MSHW, big endian
0	010	1x	1100	LSHW, big endian
1	001	00	1110	LSB, little endian
1	001	01	1101	
1	001	10	1011	
1	001	11	0111	MSB, little endian
1	010	0x	1100	LSHW, little endian
1	010	1x	0011	MSHW, little endian
x	000	xx	0000	Word access
x	110	xx	1111	Hardware development
-all	other	writes-	0000	

MSB = Most Significant Byte; LSB = Least Significant Byte; MSHW = Most Significant Half-Word; LSHW = Least Significant Half-Word

If You Need Assistance

Product support for the 29K Family processors is available from our Embedded Processor Division (EPD) Technical Support Hotlines located in the U.S. and in the U.K.

Assistance is available in the U.S. from 9:00 A.M. to 6:00 P.M. central time, Monday through Friday (except major holidays). In Europe assistance is available during U.K. business hours. Contact us at one of the following numbers:

To reach the U.S. hotline

From	Call
U.S.	1-800-2929-AMD
U.K.	0-800-89-1455
Japan	0031-11-1163
Any other location	+1-512-602-4118†

†Toll applies.

To reach the U.K. hotline

From	Call
U.K.	(0)256-811101
France	0590-8621
Germany	0130-813875
Italy	1678-77224
Any other location	+44-(0)256-811101†

†Toll applies.