FINAL

Am29000® and Am29005™

Streamlined Instruction Microprocessors

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Full 32-bit, three-bus architecture**
- **Efficient execution of high-level language programs**
- **CMOS technology/TTL compatible**
- **Concurrent instruction and data accesses**
- **Burst-mode access support**
- **192 general-purpose registers**
- **Demultiplexed, pipelined address, instruction, and data buses**
- **Three-address instruction architecture**
- **On-chip byte-alignment support allows optional byte/half-word accesses**
- **1.5 clock cycles per instruction average**
- **Double-precision, floating-point arithmetic unit (Am29027™ arithmetic accelerator)**
- **Fully pipelined**
- **On-chip timer facility**
- **On-chip clock generation**
- **On-chip debugging support**
- **Master/slave chip output checking**
- **23 million instructions per second (MIPS) sustained at 33-MHz operating frequency (Am29000 microprocessor only)**
- **9 MIPS sustained at 16-MHz operating frequency (Am29005 microprocessor only)**
- **33-, 25-, 20-, and 16-MHz operating frequencies (Am29000 microprocessor only)**
- **4-Gb virtual address space with demand paging (Am29000 microprocessor only)**
- **512-byte Branch Target Cache on-chip (Am29000 microprocessor only)**
- **64-entry Memory Management Unit on-chip (Am29000 microprocessor only)**

GENERAL DESCRIPTION

The Am29000® and the low-cost Am29005™ Streamlined Instruction microprocessors are high-performance, general-purpose, 32-bit microprocessors implemented in CMOS technology. They support a variety of applications by virtue of a flexible architecture and rapid execution of simple instructions that are common to a wide range of tasks.

Both processors efficiently perform operations common to all systems, while deferring most decisions on system policies to the system architect. They are well-suited for application in high-performance workstations, general-purpose super-minicomputers, high-performance real-time controllers, laser printer controllers, network protocol converters, and many other applications where high performance, flexibility, and the ability to program using standard software tools is important.

The Am29000 and Am29005 microprocessor instruction sets have been influenced by the results of high-level language, optimizing compiler research. They are appropriate for a variety of languages because they efficiently execute operations that are common to all languages. Consequently, the Am29000 and Am29005 microprocessors are an ideal target for high-level languages such as C, FORTRAN, Pascal, Ada, and COBOL.

The Am29000 and Am29005 microprocessors are available in a 168-lead Plastic Quad Flat Pack (PQFP) package. The package has 141 signal pins and 27 power and ground pins. The Am29000 microprocessor is also available in a 169-lead Pin Grid Array (PGA) package. The PGA has 141 signal pins, 27 power and ground pins, and 1 alignment pin.

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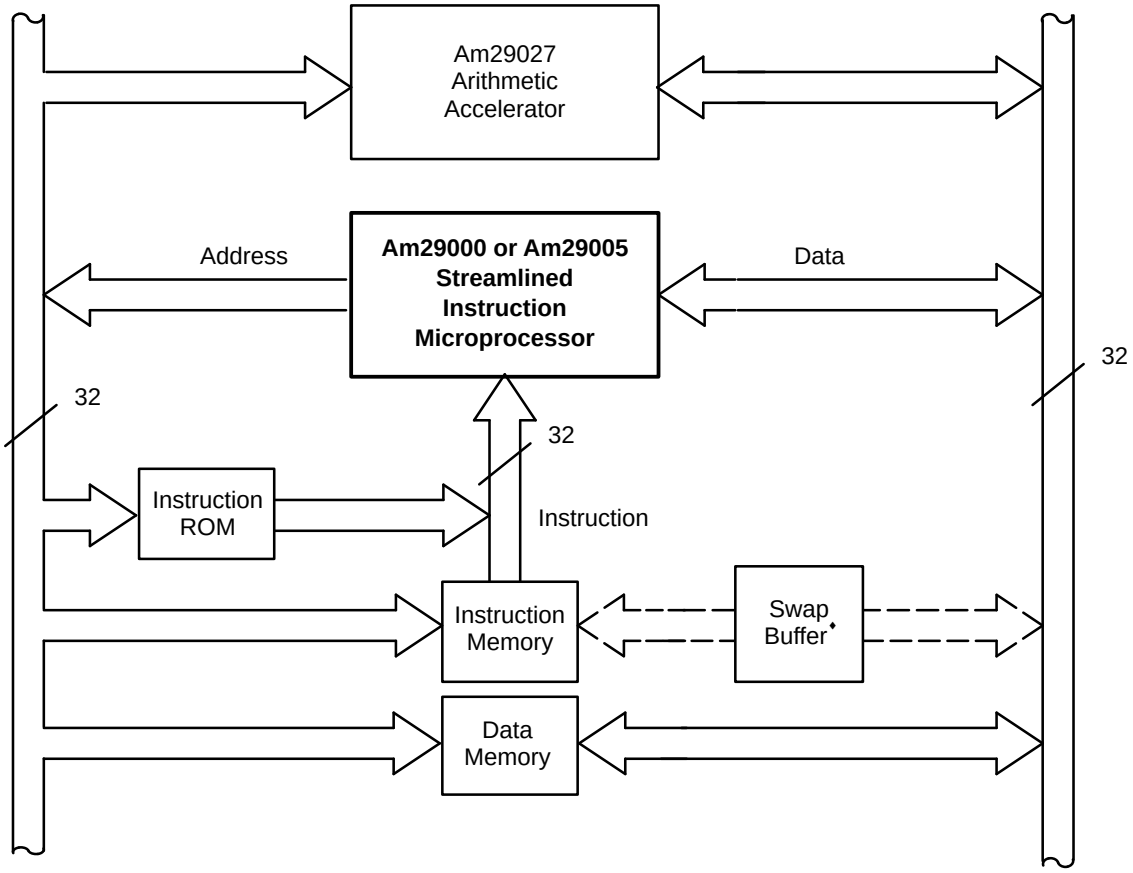
SIMPLIFIED BLOCK DIAGRAM



Note:

♦ *As a system option, a Swap Buffer may be used to join the instruction and data buses. This enables the system to read instructions as data.*

29K™ FAMILY DEVELOPMENT SUPPORT PRODUCTS

Contact your local AMD® representative for information on the complete set of development support tools. Software development products on several hosts:

- Optimizing compilers for common high-level languages
- Assembler and utility packages
- Source- and assembly-level software debuggers
- Target-resident development monitors
- Simulators

Hardware development products include:

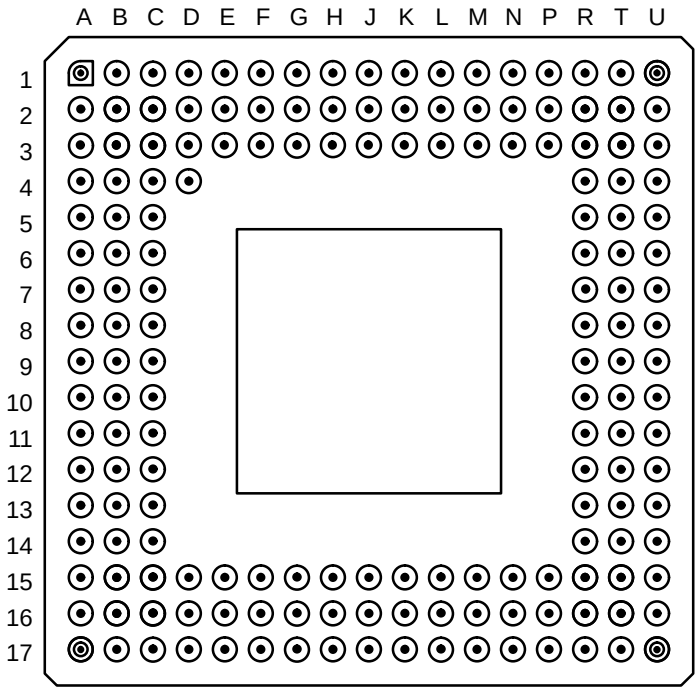
- In-circuit emulator and execution boards

RELATED AMD PRODUCTS

29K Family Devices

Part No.	Description
Am29027	Arithmetic Accelerator
Am29030™	RISC Microprocessor with 8-Kbyte Instruction Cache
Am29035™	RISC Microprocessor with 4-Kbyte Instruction Cache
Am29050™	Streamlined Instruction Microprocessor with On-Chip Floating Point
Am29200™	Single-Chip, 32-bit RISC Microcontroller
Am29205™	16-bit External Interface RISC Microcontroller

CONNECTION DIAGRAMS
169-Lead PGA—Am29000 Microprocessor Only
Bottom View



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Note:
Pinout observed from pin side of package.

PGA PIN DESIGNATIONS (Sorted by Pin Number)—Am29000 Microprocessor Only

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	GND	**C10**	GND	**J16**	A16	**R12**	STAT2
A2	I1	**C11**	GND	**J17**	A14	**R13**	GND
A3	I0	**C12**	D22	**K1**	I26	**R14**	OPT0
A4	D2	**C13**	D26	**K2**	I25	**R15**	A2
A5	D4	**C14**	V_{CC}	**K3**	GND	**R16**	A6
A6	D6	**C15**	D30	**K15**	V_{CC}	**R17**	A7
A7	D9	**C16**	D31	**K16**	A12	**T1**	INCLK
A8	D11	**C17**	A29	**K17**	A13	**T2**	$\overline{\text{BREQ}}$
A9	D12	**D1**	I11	**L1**	I27	**T3**	$\overline{\text{DERR}}$
A10	D14	**D2**	I10	**L2**	I28	**T4**	$\overline{\text{IRDY}}$
A11	D16	**D3**	I7	**L3**	V_{CC}	**T5**	$\overline{\text{WARN}}$
A12	D18	**D4**♦	PIN169	**L15**	V_{CC}	**T6**	$\overline{\text{INTR}}$2
A13	D20	**D15**	A31	**L16**	A10	**T7**	$\overline{\text{INTR}}$0
A14	D21	**D16**	A28	**L17**	A11	**T8**	$\overline{\text{BINV}}$
A15	D25	**D17**	A26	**M1**	I29	**T9**	$\overline{\text{BGRT}}$
A16	D27	**E1**	I13	**M2**	I30	**T10**	$\overline{\text{DREQ}}$
A17	GND	**E2**	I12	**M3**	GND	**T11**	$\overline{\text{LOCK}}$
B1	I6	**E3**	V_{CC}	**M15**	GND	**T12**	MSERR
B2	I5	**E15**	GND	**M16**	A0	**T13**	STAT0
B3	I3	**E16**	A27	**M17**	A1	**T14**	SUP/$\overline{\text{US}}$
B4	D0	**E17**	A23	**N1**	I31	**T15**	OPT1
B5	D1	**F1**	I16	**N2**	$\overline{\text{TEST}}$	**T16**	A3
B6	D5	**F2**	I15	**N3**	SYSCLK	**T17**	A4
B7	D8	**F3**	I14	**N15**	GND	**U1**	GND
B8	D10	**F15**	A25	**N16**	MPGM1	**U2**	$\overline{\text{PEN}}$
B9	D13	**F16**	A24	**N17**	MPGM0	**U3**	$\overline{\text{IERR}}$
B10	D15	**F17**	A21	**P1**	CNTL1	**U4**	$\overline{\text{IBACK}}$
B11	D17	**G1**	I19	**P2**	CNTL0	**U5**	$\overline{\text{INTR}}$3
B12	D19	**G2**	I18	**P3**	PWRCLK	**U6**	$\overline{\text{INTR}}$1
B13	D23	**G3**	I17	**P15**	A5	**U7**	$\overline{\text{TRAP}}$0
B14	D24	**G15**	A22	**P16**	A8	**U8**	$\overline{\text{IBREQ}}$
B15	D28	**G16**	A20	**P17**	A9	**U9**	$\overline{\text{IREQ}}$
B16	D29	**G17**	A19	**R1**	$\overline{\text{RESET}}$	**U10**	$\overline{\text{PIA}}$
B17	A30	**H1**	I20	**R2**	$\overline{\text{CDA}}$	**U11**	R/$\overline{\text{W}}$
C1	I9	**H2**	I22	**R3**	$\overline{\text{DRDY}}$	**U12**	DREQT1
C2	I8	**H3**	I21	**R4**	$\overline{\text{DBACK}}$	**U13**	DREQT0
C3	I4	**H15**	GND	**R5**	GND	**U14**	STAT1
C4	I2	**H16**	A18	**R6**	V_{CC}	**U15**	IREQT
C5	GND	**H17**	A17	**R7**	$\overline{\text{TRAP}}$1	**U16**	OPT2
C6	D3	**J1**	I23	**R8**	GND	**U17**	GND
C7	D7	**J2**	I24	**R9**	$\overline{\text{DBREQ}}$		
C8	V_{CC}	**J3**	GND	**R10**	$\overline{\text{PDA}}$		
C9	V_{CC}	**J15**	A15	**R11**	V_{CC}		

♦ ***Note:***

♦ *Pin Number D4 is the alignment pin and is electrically connected to the package lid.*

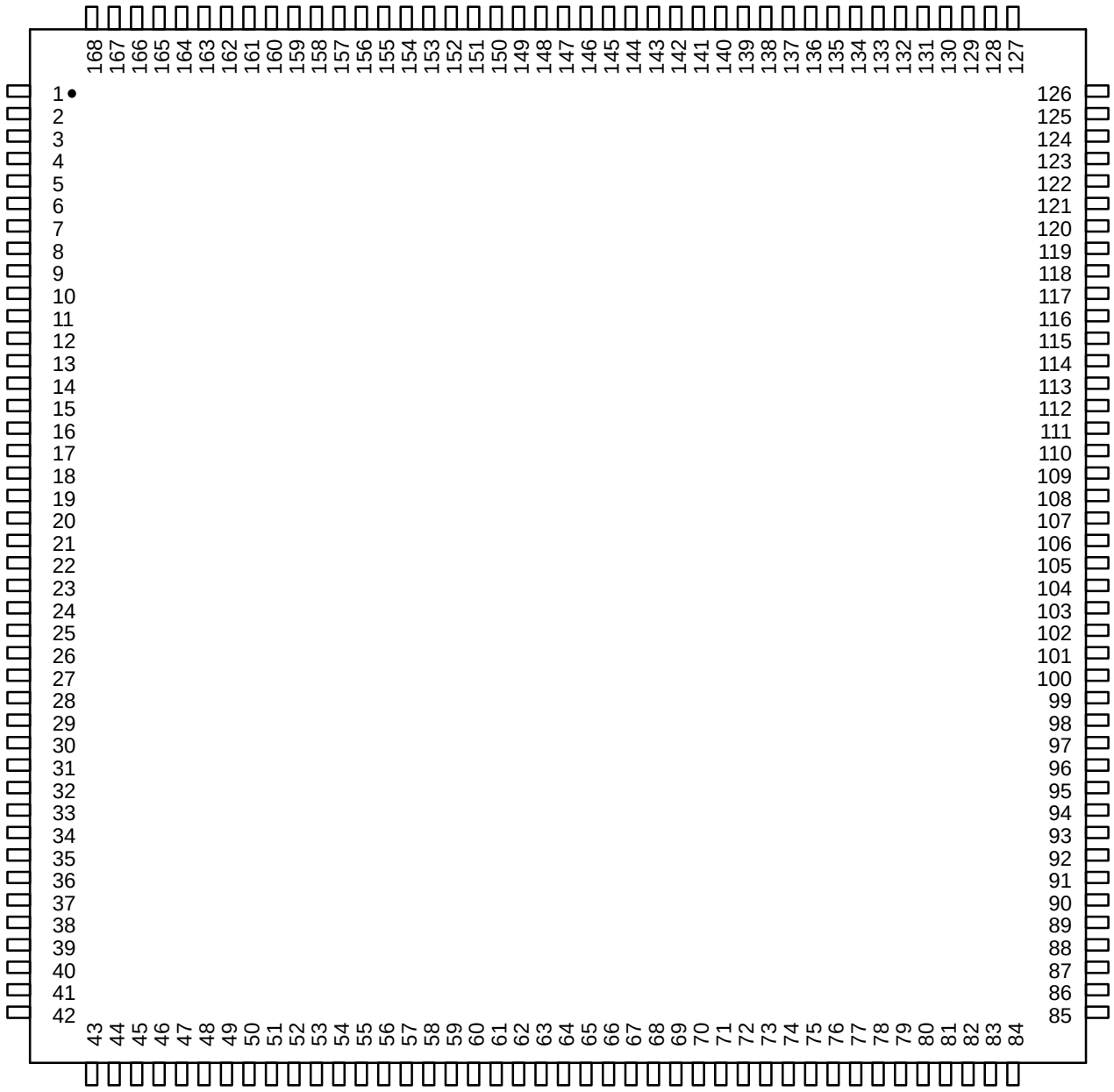
PGA PIN DESIGNATIONS (Sorted by Pin Name)—Am29000 Microprocessor Only

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A0	M16	**D5**	B6	**GND**	K3	**INCLK**	T1
A1	M17	**D6**	A6	**GND**	N15	**$\overline{\text{INTR0}}$**	T7
A2	R15	**D7**	C7	**GND**	R5	**$\overline{\text{INTR1}}$**	U6
A3	T16	**D8**	B7	**GND**	U1	**$\overline{\text{INTR2}}$**	T6
A4	T17	**D9**	A7	**GND**	R13	**$\overline{\text{INTR3}}$**	U5
A5	P15	**D10**	B8	**GND**	R8	**$\overline{\text{IRDY}}$**	T4
A6	R16	**D11**	A8	**GND**	M3	**$\overline{\text{IREQ}}$**	U9
A7	R17	**D12**	A9	**GND**	U17	**IREQT**	U15
A8	P16	**D13**	B9	**I0**	A3	**$\overline{\text{LOCK}}$**	T11
A9	P17	**D14**	A10	**I1**	A2	**MPGM0**	N17
A10	L16	**D15**	B10	**I2**	C4	**MPGM1**	N16
A11	L17	**D16**	A11	**I3**	B3	**MSERR**	T12
A12	K16	**D17**	B11	**I4**	C3	**OPT0**	R14
A13	K17	**D18**	A12	**I5**	B2	**OPT1**	T15
A14	J17	**D19**	B12	**I6**	B1	**OPT2**	U16
A15	J15	**D20**	A13	**I7**	D3	**$\overline{\text{PDA}}$**	R10
A16	J16	**D21**	A14	**I8**	C2	**$\overline{\text{PEN}}$**	U2
A17	H17	**D22**	C12	**I9**	C1	**$\overline{\text{PIA}}$**	U10
A18	H16	**D23**	B13	**I10**	D2	**PIN169**	D4♦
A19	G17	**D24**	B14	**I11**	D1	**PWRCLK**	P3
A20	G16	**D25**	A15	**I12**	E2	**R/$\overline{\text{W}}$**	U11
A21	F17	**D26**	C13	**I13**	E1	**$\overline{\text{RESET}}$**	R1
A22	G15	**D27**	A16	**I14**	F3	**STAT0**	T13
A23	E17	**D28**	B15	**I15**	F2	**STAT1**	U14
A24	F16	**D29**	B16	**I16**	F1	**STAT2**	R12
A25	F15	**D30**	C15	**I17**	G3	**SUP/$\overline{\text{US}}$**	T14
A26	D17	**D31**	C16	**I18**	G2	**SYSCLK**	N3
A27	E16	**$\overline{\text{DBACK}}$**	R4	**I19**	G1	**$\overline{\text{TEST}}$**	N2
A28	D16	**$\overline{\text{DBREQ}}$**	R9	**I20**	H1	**$\overline{\text{TRAP0}}$**	U7
A29	C17	**$\overline{\text{DERR}}$**	T3	**I21**	H3	**$\overline{\text{TRAP1}}$**	R7
A30	B17	**$\overline{\text{DRDY}}$**	R3	**I22**	H2	**V_{CC}**	C14
A31	D15	**$\overline{\text{DREQ}}$**	T10	**I23**	J1	**V_{CC}**	L15
$\overline{\text{BGRT}}$	T9	**DREQT0**	U13	**I24**	J2	**V_{CC}**	C8
$\overline{\text{BINV}}$	T8	**DREQT1**	U12	**I25**	K2	**V_{CC}**	C9
$\overline{\text{BREQ}}$	T2	**GND**	E15	**I26**	K1	**V_{CC}**	E3
$\overline{\text{CDA}}$	R2	**GND**	H15	**I27**	L1	**V_{CC}**	K15
CNTL0	P2	**GND**	M15	**I28**	L2	**V_{CC}**	L3
CNTL1	P1	**GND**	C10	**I29**	M1	**V_{CC}**	R6
D0	B4	**GND**	A1	**I30**	M2	**V_{CC}**	R11
D1	B5	**GND**	A17	**I31**	N1	**$\overline{\text{WARN}}$**	T5
D2	A4	**GND**	C5	**$\overline{\text{IBACK}}$**	U4		
D3	C6	**GND**	C11	**$\overline{\text{IBREQ}}$**	U8		
D4	A5	**GND**	J3	**$\overline{\text{IERR}}$**	U3		

Note:

♦ *Pin Number D4 is the alignment pin and is electrically connected to the package lid.*

CONNECTION DIAGRAMS (continued)
168-Pin PQFP — Am29000 and Am29005 Microprocessors
Top View



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PQFP PIN DESIGNATIONS (Sorted by Pin Number)—Am29000 and Am29005 Microprocessors

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	$\overline{\text{DRDY}}$	**43**	V_{CC}	**85**	GND	**127**	GND
2	CDA	**44**	I3	**86**	A31	**128**	OPT0
3	INCLK	**45**	I2	**87**	A30	**129**	OPT1
4	PWRCLK	**46**	I1	**88**	A29	**130**	OPT2
5	SYSCLK	**47**	GND	**89**	A28	**131**	SUP/$\overline{\text{US}}$
6	GND	**48**	I0	**90**	A27	**132**	IREQT
7	V_{CC}	**49**	D0	**91**	A26	**133**	STAT0
8	GND	**50**	D1	**92**	A25	**134**	STAT1
9	$\overline{\text{RESET}}$	**51**	D2	**93**	A24	**135**	STAT2
10	CNTL0	**52**	D3	**94**	A23	**136**	MSERR
11	CNTL1	**53**	D4	**95**	A22	**137**	DREQT0
12	$\overline{\text{TEST}}$	**54**	D5	**96**	A21	**138**	DREQT1
13	I31	**55**	D6	**97**	A20	**139**	$\overline{\text{LOCK}}$
14	I30	**56**	D7	**98**	A19	**140**	R/$\overline{\text{W}}$
15	I29	**57**	D8	**99**	A18	**141**	$\overline{\text{DREQ}}$
16	I28	**58**	D9	**100**	A17	**142**	$\overline{\text{PDA}}$
17	I27	**59**	D10	**101**	A16	**143**	$\overline{\text{PIA}}$
18	I26	**60**	D11	**102**	A15	**144**	$\overline{\text{IREQ}}$
19	I25	**61**	D12	**103**	GND	**145**	$\overline{\text{BGRT}}$
20	I24	**62**	D13	**104**	V_{CC}	**146**	$\overline{\text{DBREQ}}$
21	GND	**63**	D14	**105**	V_{CC}	**147**	$\overline{\text{IBREQ}}$
22	V_{CC}	**64**	V_{CC}	**106**	A14	**148**	$\overline{\text{BINV}}$
23	I23	**65**	GND	**107**	A13	**149**	V_{CC}
24	I22	**66**	D15	**108**	A12	**150**	V_{CC}
25	I21	**67**	D16	**109**	A11	**151**	GND
26	I20	**68**	D17	**110**	A10	**152**	V_{CC}
27	I19	**69**	D18	**111**	A1	**153**	GND
28	I18	**70**	D19	**112**	A0	**154**	$\overline{\text{TRAP}}$0
29	I17	**71**	D20	**113**	MPGM0♦	**155**	$\overline{\text{TRAP}}$1
30	I16	**72**	D21	**114**	MPGM1♦	**156**	$\overline{\text{INTR}}$0
31	I15	**73**	D22	**115**	V_{CC}	**157**	$\overline{\text{INTR}}$1
32	I14	**74**	D23	**116**	V_{CC}	**158**	$\overline{\text{INTR}}$2
33	I13	**75**	D24	**117**	A9	**159**	$\overline{\text{INTR}}$3
34	I12	**76**	D25	**118**	A8	**160**	$\overline{\text{WARN}}$
35	I11	**77**	D26	**119**	A7	**161**	$\overline{\text{IBACK}}$
36	I10	**78**	D27	**120**	A6	**1652**	$\overline{\text{IRDY}}$
37	I9	**79**	D28	**121**	A5	**163**	$\overline{\text{IERR}}$
38	I8	**80**	D29	**122**	A4	**164**	$\overline{\text{DERR}}$
39	I7	**81**	D30	**123**	A3	**165**	$\overline{\text{DBACK}}$
40	I6	**82**	D31	**124**	A2	**166**	$\overline{\text{PEN}}$
41	I5	**83**	GND	**125**	GND	**167**	$\overline{\text{BREQ}}$
42	I4	**84**	V_{CC}	**126**	GND	**168**	GND

Note:

♦ *MPGM0 and MPGM1 apply only to the Am29000 microprocessor.*

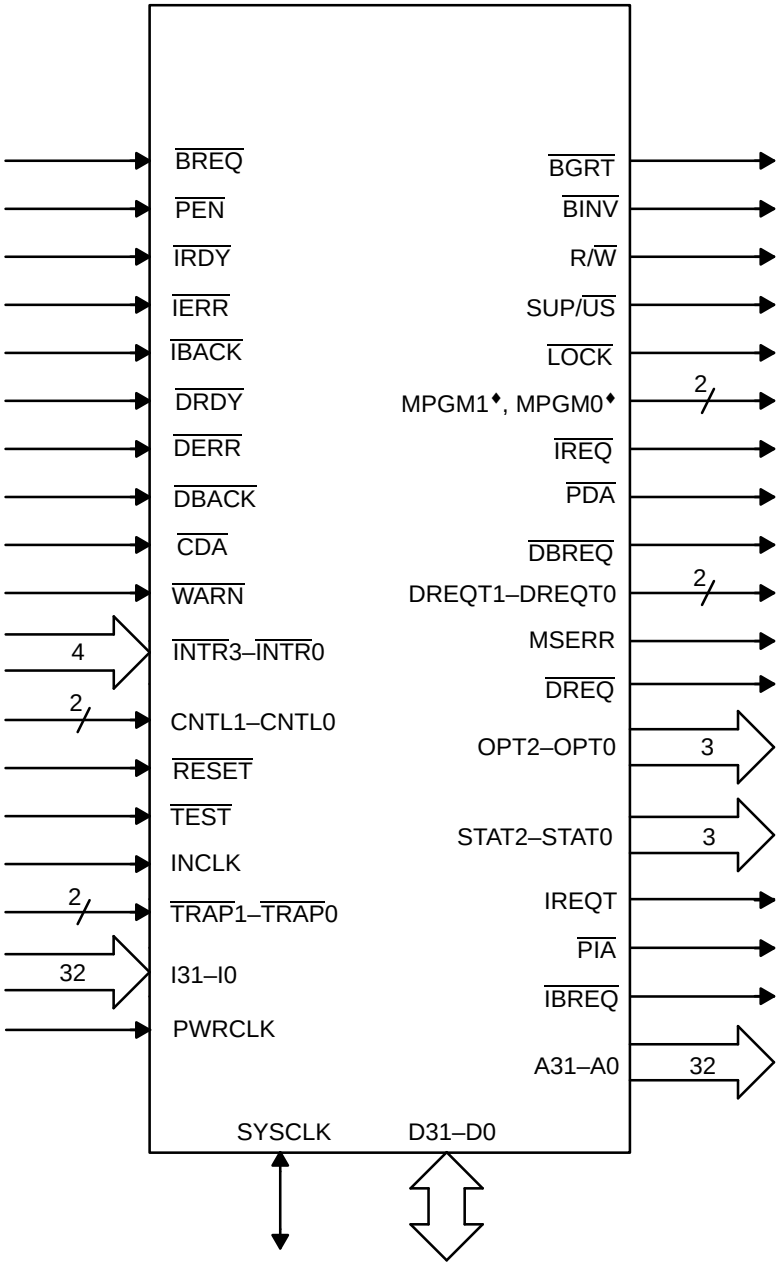
PQFP PIN DESIGNATIONS (Sorted by Pin Name)—Am29000 and Am29005 Microprocessors

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A0	112	**D4**	53	**GND**	103	**INCLK**	3
A1	111	**D5**	54	**GND**	125	**$\overline{\text{INTR0}}$**	156
A2	124	**D6**	55	**GND**	126	**$\overline{\text{INTR1}}$**	157
A3	123	**D7**	56	**GND**	127	**$\overline{\text{INTR2}}$**	158
A4	122	**D8**	57	**GND**	151	**$\overline{\text{INTR3}}$**	159
A5	121	**D9**	58	**GND**	153	**$\overline{\text{IRDY}}$**	162
A6	120	**D10**	59	**GND**	168	**$\overline{\text{IREQ}}$**	144
A7	119	**D11**	60	**I0**	48	**IREQT**	132
A8	118	**D12**	61	**I1**	46	**$\overline{\text{LOCK}}$**	139
A9	117	**D13**	62	**I2**	45	**MPGM0♦**	113
A10	110	**D14**	63	**I3**	44	**MPGM1♦**	114
A11	109	**D15**	66	**I4**	42	**MSERR**	136
A12	108	**D16**	67	**I5**	41	**OPT0**	128
A13	107	**D17**	68	**I6**	40	**OPT1**	129
A14	106	**D18**	69	**I7**	39	**OPT2**	130
A15	102	**D19**	70	**I8**	38	**$\overline{\text{PDA}}$**	142
A16	101	**D20**	71	**I9**	37	**$\overline{\text{PEN}}$**	166
A17	100	**D21**	72	**I10**	36	**$\overline{\text{PIA}}$**	143
A18	99	**D22**	73	**I11**	35	**PWRCLK**	4
A19	98	**D23**	74	**I12**	34	**R/$\overline{\text{W}}$**	140
A20	97	**D24**	75	**I13**	33	**$\overline{\text{RESET}}$**	9
A21	96	**D25**	76	**I14**	32	**STAT0**	133
A22	95	**D26**	77	**I15**	31	**STAT1**	134
A23	94	**D27**	78	**I16**	30	**STAT2**	135
A24	93	**D28**	79	**I17**	29	**SUP/$\overline{\text{US}}$**	131
A25	92	**D29**	80	**I18**	28	**SYSCLK**	5
A26	91	**D30**	81	**I19**	27	**$\overline{\text{TEST}}$**	12
A27	90	**D31**	82	**I20**	26	**$\overline{\text{TRAP0}}$**	154
A28	89	**$\overline{\text{DBACK}}$**	165	**I21**	25	**$\overline{\text{TRAP1}}$**	155
A29	88	**$\overline{\text{DBREQ}}$**	146	**I22**	24	**V_{CC}**	7
A30	87	**$\overline{\text{DERR}}$**	164	**I23**	23	**V_{CC}**	22
A31	86	**$\overline{\text{DRDY}}$**	1	**I24**	20	**V_{CC}**	43
$\overline{\text{BGRT}}$	145	**$\overline{\text{DREQ}}$**	141	**I25**	19	**V_{CC}**	64
$\overline{\text{BINV}}$	148	**DREQT0**	137	**I26**	18	**V_{CC}**	84
$\overline{\text{BREQ}}$	167	**DREQT1**	138	**I27**	17	**V_{CC}**	104
$\overline{\text{CDA}}$	2	**GND**	6	**I28**	16	**V_{CC}**	105
CNTL0	10	**GND**	8	**I29**	15	**V_{CC}**	115
CNTL1	11	**GND**	21	**I30**	14	**V_{CC}**	116
D0	49	**GND**	47	**I31**	13	**V_{CC}**	149
D1	50	**GND**	65	**$\overline{\text{IBACK}}$**	161	**V_{CC}**	150
D2	51	**GND**	83	**$\overline{\text{IBREQ}}$**	147	**V_{CC}**	152
D3	52	**GND**	85	**$\overline{\text{IERR}}$**	163	**$\overline{\text{WARN}}$**	160

Note:

♦ *MPGM0 and MPGM1 apply only to the Am29000 microprocessor.*

LOGIC SYMBOL



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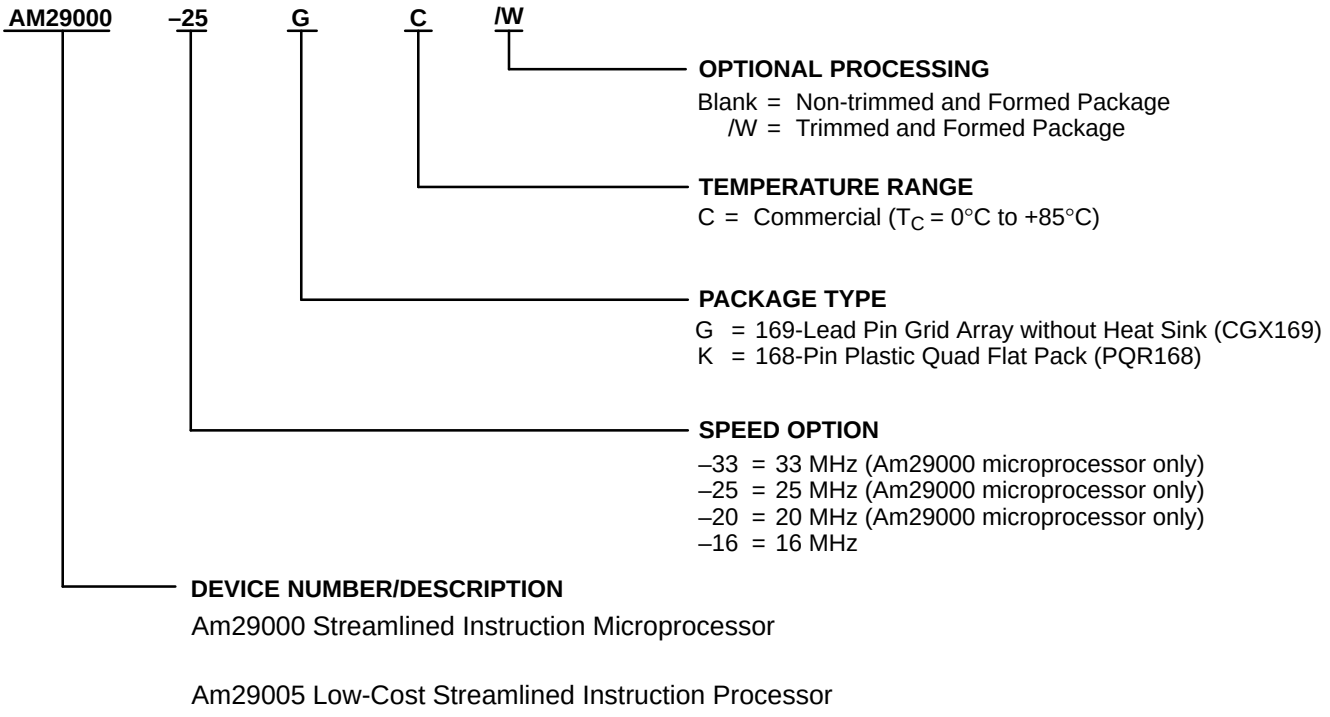
Note:

♦ *MPGM1 and MPGM0 apply only to the Am29000 microprocessor.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of the following elements.



Valid Combinations	
AM29000–16	KC/W, GC, KC
AM29000–20	
AM29000–25	GC
AM29000–33	GC
AM29005–16	KC, KC/W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: /W denotes a trimmed and formed package.

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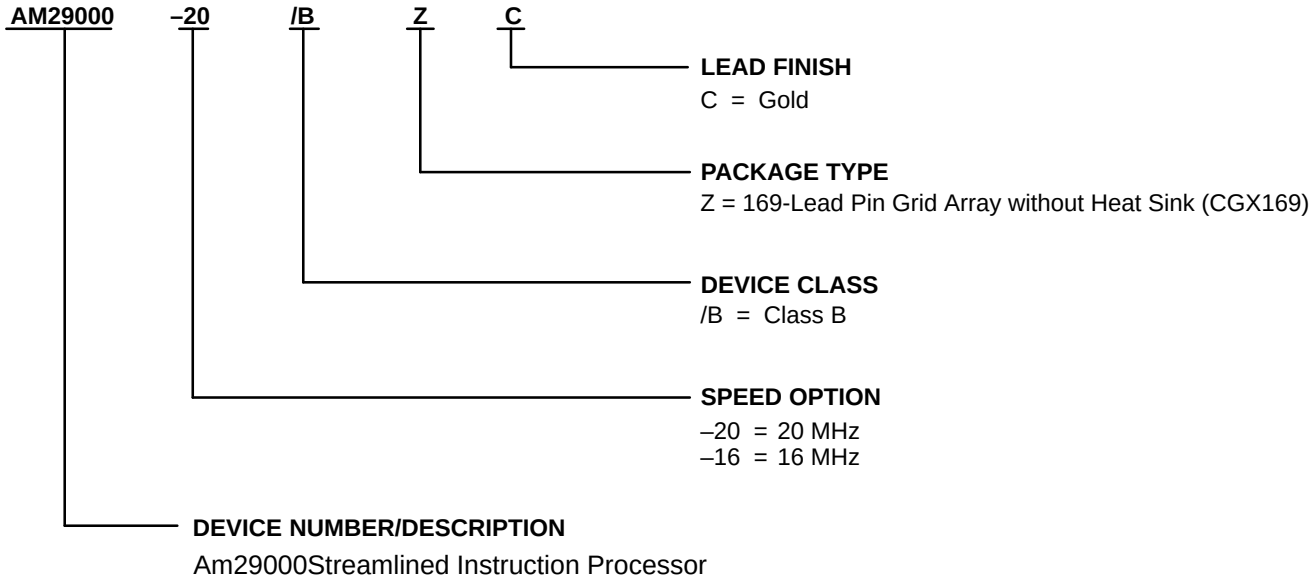
MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The ordering number (Valid Combination) is formed by a combination of the following elements.



Valid Combinations	
AM29000–20	/BZC
AM29000–16	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

PIN DESCRIPTIONS

Although certain outputs are described as being three-state or bidirectional outputs, all outputs (except MSERR) may be placed in a high-impedance state by the Test mode. The three-state and bidirectional terminology in this section is for those outputs (except SYSCLK) that are disabled when the processor grants the channel to another master.

A31–A0

Address Bus (Three-state Output; Synchronous)
The Address Bus transfers the byte address for all accesses except Burst-mode accesses. For Burst-mode accesses, it transfers the address for the first access in the sequence.

$\overline{\text{BGRT}}$

Bus Grant (Output; Synchronous)
This output signals to an external master that the processor is relinquishing control of the channel in response to $\overline{\text{BREQ}}$.

$\overline{\text{BINV}}$

Bus Invalid (Output; Synchronous)
This output indicates that the address bus and related controls are invalid. It defines an idle cycle for the channel.

$\overline{\text{BREQ}}$

Bus Request (Input; Synchronous)
This input allows other masters to arbitrate for control of the processor channel.

$\overline{\text{CDA}}$

Coprocessor Data Accept (Input; Synchronous)
This signal allows the coprocessor to indicate the acceptance of operands or operation codes. For transfers to the coprocessor, the processor does not expect a $\overline{\text{DRDY}}$ response; an active level on $\overline{\text{CDA}}$ performs the function normally performed by $\overline{\text{DRDY}}$. $\overline{\text{CDA}}$ may be active whenever the coprocessor is able to accept transfers.

CNTL1–CNTL0

CPU Control (Input; Asynchronous)
These inputs control the processor mode:

CNTL1	CNTL0	Mode
0	0	Load Test Instruction
0	1	Step
1	0	Halt
1	1	Normal

D31–D0

Data Bus (Bidirectional; Synchronous)
The Data Bus transfers data to and from the processor for load and store operations.

$\overline{\text{DBACK}}$

Data Burst Acknowledge (Input; Synchronous)
This input is active whenever a Burst-mode data access has been established. It may be active even though no data is currently being accessed.

$\overline{\text{DBREQ}}$

Data Burst Request (Three-state Output; Synchronous)
This signal is used to establish a Burst-mode data access and to request data transfers during a Burst-mode data access. $\overline{\text{DBREQ}}$ may be active even though the address bus is being used for an instruction access. This signal becomes valid late in the cycle, with respect to $\overline{\text{DREQ}}$.

$\overline{\text{DERR}}$

Data Error (Input; Synchronous)
This input indicates that an error occurred during the current data access. For a load, the processor ignores the content of the data bus. For a store, the access is terminated. In either case, a Data Access Exception trap occurs. The processor ignores this signal if there is no pending data access.

$\overline{\text{DRDY}}$

Data Ready (Input; Synchronous)
For loads, this input indicates that valid data is on the data bus. For stores, it indicates that the access is complete and that data no longer needs to be driven on the data bus. The processor ignores this signal if there is no pending data access.

$\overline{\text{DREQ}}$

Data Request (Three-state Output; Synchronous)
This signal requests a data access. When it is active, the address for the access appears on the address bus.

DREQT1–DREQT0

Data Request Type
(Three-state Output; Synchronous)
These signals specify the address space of a data access as follows (the value “x” is a “don’t care”):

DREQT1	DREQT0	Mode
0	0	Instruction/data memory access
0	1	Input/output access
1	x	Coprocessor transfer

An interrupt/trap vector request is indicated as a data-memory read. If required, the system can identify the vector fetch by the STAT2–STAT0 outputs. DREQT1–DREQT0 are valid only when $\overline{\text{DREQ}}$ is active.

I31–I0

Instruction Bus (Input; Synchronous)

The Instruction Bus transfers instructions to the processor.

$\overline{\text{IBACK}}$

Instruction Burst Acknowledge (Input; Synchronous)

This input is active whenever a Burst-mode instruction access has been established. $\overline{\text{IBACK}}$ may be active even though no instructions are currently being accessed.

$\overline{\text{IBREQ}}$

Instruction Burst Request (Three-state Output; Synchronous)

This signal is used to establish a Burst-mode instruction access and to request instruction transfers during a Burst-mode instruction access. $\overline{\text{IBREQ}}$ may be active even though the address bus is being used for a data access. This signal becomes valid late in the cycle with respect to $\overline{\text{IREQ}}$.

$\overline{\text{IERR}}$

Instruction Error (Input; Synchronous)

This input indicates that an error occurred during the current instruction access. The processor ignores the content of the instruction bus, and an Instruction Access Exception trap occurs if the processor attempts to execute the invalid instruction. The processor ignores this signal if there is no pending instruction access.

INCLK

Input Clock (Input)

When the processor generates the clock for the system, this is an oscillator input to the processor at twice the processor's operating frequency. In systems where the clock is not generated by the processor, this signal must be tied High or Low, except in certain master/slave configurations.

$\overline{\text{INTR3}}$–$\overline{\text{INTR0}}$

Interrupt Request (Input; Asynchronous)

These inputs generate prioritized interrupt requests. The interrupt caused by $\overline{\text{INTR0}}$ has the highest priority, and the interrupt caused by $\overline{\text{INTR3}}$ has the lowest priority. The interrupt requests are masked in prioritized order by the Interrupt Mask field in the Current Processor Status Register.

$\overline{\text{IRDY}}$

Instruction Ready (Input; Synchronous)

This input indicates that a valid instruction is on the instruction bus. The processor ignores this signal if there is no pending instruction access.

$\overline{\text{IREQ}}$

Instruction Request (Three-state Output; Synchronous)

This signal requests an instruction access. When it is active, the address for the access appears on the address bus.

IREQT

Instruction Request Type (Three-state Output; Synchronous)

This signal specifies the address space of an instruction request when $\overline{\text{IREQ}}$ is active:

IREQT	Mode
0	Instruction/data memory access
1	Instruction read-only memory access

$\overline{\text{LOCK}}$

Lock (Three-state Output; Synchronous)

This output allows the implementation of various channel and device interlocks. It may be active only for the duration of an access, or active for an extended period of time under control of the Lock bit in the Current Processor Status.

MPGM1–MPGM0

MMU Programmable (Three-state Output; Synchronous)

In the Am29000 microprocessor, these outputs reflect the value of two PGM bits in the Translation Look-Aside Buffer entry associated with the access. If no address translation is performed, these signals are both Low.

These outputs have no function in the Am29005 microprocessor and are always driven Low on an access. They are defined to ensure pin compatibility with the Am29000 microprocessor.

MSERR

Master/Slave Error (Output; Synchronous)

This output shows the result of the comparison of processor outputs with the signals provided internally to the off-chip drivers. If there is a difference for any enabled driver, this line is asserted.

OPT2–OPT0

Option Control
(Three-state Output; Synchronous)
These outputs reflect the value of bits 18–16 of the load or store instruction that begins an access. Bit 18 of the instruction is reflected on OPT2, bit 17 on OPT1, and bit 16 on OPT0.

The standard definitions of these signals (based on DREQT) are as follows (the value "x" is a "don't care"):

DREQT1	DREQT0	OPT2	OPT1	OPT0	Meaning
0	x	0	0	0	Word-length access
0	x	0	0	1	Byte access
0	x	0	1	0	Half-word access
0	0	1	0	0	Instruction ROM access (as data)
0	0	1	0	1	Cache control
0	0	1	1	0	In-circuit emulator accesses
—All Others—					Reserved

During an interrupt/trap vector fetch, the OPT2–OPT0 signals indicate a word-length access (000). Also, the system should return an entire aligned word for a read, regardless of the indicated data length.

The Am29000/005 microprocessor does not explicitly prevent a store to the instruction ROM. OPT2–OPT0 are valid only when $\overline{\text{DREQ}}$ is active.

$\overline{\text{PDA}}$

Pipelined Data Access
(Three-state Output; Synchronous)
If $\overline{\text{DREQ}}$ is not active, this output indicates that a data access is pipelined with another in-progress data access. The indicated access cannot be completed until the first access is complete. The completion of the first access is signaled by the assertion of $\overline{\text{DREQ}}$.

$\overline{\text{PEN}}$

Pipeline Enable (Input; Synchronous)
This signal allows devices that can support pipelined accesses (i.e., that have input latches for the address and required controls) to signal that a second access may begin while the first is being completed.

$\overline{\text{PIA}}$

Pipelined Instruction Access
(Three-state Output; Synchronous)
If $\overline{\text{IREQ}}$ is not active, this output indicates that an instruction access is pipelined with another in-progress instruction access. The indicated access cannot be completed until the first access is complete. The completion of the first access is signaled by the assertion of $\overline{\text{IREQ}}$.

R/$\overline{\text{W}}$

Read/Write (Three-state Output; Synchronous)
This signal indicates whether data is being transferred from the processor to the system, or from the system to the processor. R/$\overline{\text{W}}$ is valid only when the address bus is valid. R/$\overline{\text{W}}$ will be High when $\overline{\text{IREQ}}$ is active.

$\overline{\text{RESET}}$

Reset (Input; Asynchronous)
This input places the processor in the Reset mode.

STAT2–STAT0

CPU Status (Output; Synchronous)
These outputs indicate the state of the processor's execution stage on the previous cycle. They are encoded as follows:

STAT2	STAT1	STAT0	Condition
0	0	0	Halt or Step Modes
0	0	1	Pipeline Hold Mode
0	1	0	Load Test Instruction Mode, Halt/Freeze
0	1	1	Wait Mode
1	0	0	Interrupt Return
1	0	1	Taking Interrupt or Trap
1	1	0	Non-sequential Instruction
1	1	1	Fetch Executing Mode

SUP/$\overline{\text{US}}$

Supervisor/User Mode
(Three-state Output; Synchronous)
This output indicates the program mode for an access. The processor does not relinquish the channel (in response to $\overline{\text{BREQ}}$) when $\overline{\text{LOCK}}$ is active.

SYSCLK

System Clock (Bidirectional)
This is either a clock output with a frequency that is half that of INCLK, or an input from an external clock generator at the processor's operating frequency.

$\overline{\text{TEST}}$

Test Mode (Input; Asynchronous)

When this input is active, the processor is in Test mode. All outputs and bidirectional lines, except MSERR, are forced to the state.

$\overline{\text{TRAP}}$1–$\overline{\text{TRAP}}$0

Trap Request (Input; Asynchronous)

These inputs generate prioritized trap requests. The trap caused by $\overline{\text{TRAP}}$0 has the highest priority. These trap requests are disabled by the DA bit of the Current Processor Status Register.

$\overline{\text{WARN}}$

Warn (Input; Asynchronous; Edge-sensitive)

A High-to-Low transition on this input causes a non-maskable $\overline{\text{WARN}}$ trap to occur. This trap bypasses the normal trap vector fetch sequence, and is useful in situations where the vector fetch may not work (e.g., when data memory is faulty).

The following pins are not signal pins, but are named in Am29000 and Am29005 microprocessor documentation because of their special role in the processor and system.

PWRCLK

Power Supply for SYSCLK Driver

This pin is a power supply for the SYSCLK output driver. It isolates the SYSCLK driver and is used to determine whether or not the Am29000 or Am29005 microprocessor generates the clock for the system. If power (+5 V) is applied to this pin, the Am29000 or Am29005 microprocessor generates a clock on the SYSCLK output. If this pin is grounded, the Am29000 or Am29005 microprocessor accepts a clock generated by the system on the SYSCLK input.

PIN169 (PGA Package Only)

Alignment pin

In the PGA package, this pin is used to indicate proper pin-alignment of the Am29000 microprocessor and is used by the in-circuit emulator(s) to communicate its presence to the system. This pin does not exist on the Am29000 or Am29005 microprocessor in the PQFP package.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Voltage on any Pin with Respect to GND . . . . . –0.5 V to V_{CC} +0.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) . . . . . 0°C to +85°C

Supply Voltage (V_{CC}) . . . . . +4.75 V to +5.25 V

Military (MIL) Devices

Case Temperature (T_C) . . . . . –55°C to +125°C

Supply Voltage (V_{CC}) . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and MILITARY operating ranges

Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +0.5	V
$V_{ILINCLK}$	INCLK Input Low Voltage		–0.5	0.8	V
$V_{IHINCLK}$	INCLK Input High Voltage		2.0	V_{CC} +0.5	V
$V_{ILSYSCLK}$	SYSCLK Input Low Voltage		–0.5	0.8	V
$V_{IHSYSCLK}$	SYSCLK Input High Voltage		V_{CC} –0.8	V_{CC} +0.5	V
V_{OL}	Output Low Voltage for All Outputs except SYSCLK	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage for all Outputs except SYSCLK	I_{OH} = –400 µA	2.4		V
I_{LI}	Input Leakage Current	0.45 V ≤ V_{IN} ≤ V_{CC} –0.45 V		±10	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC} –0.45 V		±10	µA
I_{CCOP}	Operating Power Supply Current	V_{CC} = 5.25 V, Outputs Floating; Holding $\overline{\text{RESET}}$ active with externally supplied $\overline{\text{SYSCLK}}$		22 (C) 25 (MIL)	mA/MHz
V_{OLC}	SYSCLK Output Low Voltage	I_{OLC} = 20 mA		0.6	V
V_{OHC}	SYSCLK Output High Voltage	I_{OHC} = 20 mA	V_{CC} –0.6		V
I_{OSGND}	SYSCLK GND Short Circuit Current	V_{CC} = 5.0 V	100		mA
I_{OSVCC}	SYSCLK V_{CC} Short Circuit Current	V_{CC} = 5.0 V	100		mA

CAPACITANCE

Symbol	Parameter Description	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance			15	pF
C_{INCLK}	INCLK Input Capacitance			20	pF
C_{SYSCLK}	SYSCLK Capacitance	fC = 1 MHz (Note 1)		90	pF
C_{OUT}	Output Capacitance			20	pF
$C_{I/O}$	I/O Pin Capacitance			20	pF

Note:

1. Not 100% tested.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges
Am29000 Microprocessor Only

No.	Parameter Description	Notes	33 MHz		25 MHz		Unit
			Min	Max	Min	Max	
1	System Clock (SYSCLK); Period (T)	1	30	125	40	125	ns
1A	SYSCLK at 1.5 V to $\overline{\text{SYSCLK}}$ at 1.5 V when used as an output	13	0.5T – 1	0.5T + 1	0.5T – 1	0.5T + 1	ns
2	SYSCLK High Time when used as input	13	14		19		ns
3	SYSCLK Low Time when used as input	13	13		17		ns
4	SYSCLK Rise Time	2		4		5	ns
5	SYSCLK Fall Time	2		4		5	ns
6	Synchronous SYSCLK Output Valid Delay	3, 12	2	12	2	14	ns
6A	Synchronous SYSCLK Output Valid Delay for D31–D0	12	2	14	2	18	ns
7	Three-State Synchronous SYSCLK Output Invalid Delay	4, 14, 15	2	20	2	30	ns
8	Synchronous SYSCLK Output Valid Delay	5, 12	2	10	2	14	ns
8A	Three-State SYSCLK Synchronous Output Invalid Delay	5, 14, 15	2	20	2	30	ns
9	Synchronous Input Setup Time	7	10		12		ns
9A	Synchronous Input Setup Time for D31–D0, I31–I0		4		6		ns
9B	Synchronous Input Setup Time for $\overline{\text{DRDY}}$		11		13		ns
10	Synchronous Input Hold Time	6	2		2		ns
11	Asynchronous Input Minimum Pulse Width	8	T + 10		T + 10		ns
12	INCLK Period		15	62.5	20	62.5	ns
12A	INCLK to SYSCLK Delay		2	8	2	10	ns
12B	INCLK to $\overline{\text{SYSCLK}}$ Delay		2	8	2	10	ns
13	INCLK Low Time		3.5		8		ns
14	INCLK High Time		3.5		8		ns
15	INCLK Rise Time			3		5	ns
16	INCLK Fall Time			3		5	ns
17	INCLK to Deassertion of $\overline{\text{RESET}}$ (for phase synchronization of SYSCLK)	9	0	4	0	5	ns
18	$\overline{\text{WARN}}$ Asynchronous Deassertion Hold Minimum Pulse Width	10	4T		4T		ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	12	0	6	0	7	ns
20	Three-State Synchronous SYSCLK Output Invalid Delay for D31–D0	11, 14, 15	2	15	2	20	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Am29000 and Am29005 Microprocessors

No.	Parameter Description	Notes	20 MHz♦		16 MHz♦♦		Unit
			Min	Max	Min	Max	
1	System Clock (SYSCLK); Period (T)	1	50	125	60	125	ns
1A	SYSCLK at 1.5 V to $\overline{\text{SYSCLK}}$ at 1.5 V when used as an output	13	0.5T – 1	0.5T + 1	0.5T – 2	0.5T + 2	ns
2	SYSCLK High Time when used as input	13	22		27		ns
3	SYSCLK Low Time when used as input	13	19		22		ns
4	SYSCLK Rise Time	2		5		5	ns
5	SYSCLK Fall Time	2		5		5	ns
6	Synchronous SYSCLK Output Valid Delay	3, 12	2	16	2	16	ns
6A	Synchronous SYSCLK Output Valid Delay for D31–D0	12	2	20	2	20	ns
7	Three-State Synchronous SYSCLK Output Invalid Delay	4, 14, 15	2	30	2	30	ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	5, 12	2	16	2	16	ns
8A	Three-State $\overline{\text{SYSCLK}}$ Synchronous Output Invalid Delay	5, 14, 15	2	30	2	30	ns
9	Synchronous Input Setup Time	7	15		15		ns
9A	Synchronous Input Setup Time for D31–D0, I31–I0		8		8		ns
9B	Synchronous Input Setup Time for $\overline{\text{DRDY}}$		16		16		ns
10	Synchronous Input Hold Time	6	2		2		ns
11	Asynchronous Input Minimum Pulse Width	8	T + 10		T + 10		ns
12	INCLK Period		25	62.5	30	62.5	ns
12A	INCLK to SYSCLK Delay		2	12	2	15	ns
12B	INCLK to $\overline{\text{SYSCLK}}$ Delay		2	12	2	15	ns
13	INCLK Low Time		10		12		ns
14	INCLK High Time		10		12		ns
15	INCLK Rise Time			5		5	ns
16	INCLK Fall Time			5		5	ns
17	INCLK to Deassertion of $\overline{\text{RESET}}$ (for phase synchronization of SYSCLK)	9	0	5	0	5	ns
18	$\overline{\text{WARN}}$ Asynchronous Deassertion Hold Minimum Pulse Width	10	4T		4T		ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	12	0	8	0	9	ns
20	Three-State Synchronous SYSCLK output invalid delay for D31–D0	11, 14, 15	2	25	2	25	ns

Notes:

♦ *20 MHz applies to the Am29000 microprocessor only.*

♦♦ *16 MHz applies to both the Am29000 and Am29005 microprocessors.*

SWITCHING CHARACTERISTICS over MILITARY operating ranges

Am29000 Microprocessor Only

No.	Parameter Description	Notes	20 MHz		16 MHz		Unit
			Min	Max	Min	Max	
1	System Clock (SYSCLK); Period (T)	1	50	125	60	125	ns
1A	SYSCLK at 1.5 V to $\overline{\text{SYSCLK}}$ at 1.5 V when used as an output	13	0.5T – 1	0.5T + 1	0.5T – 2	0.5T + 2	ns
2	SYSCLK High Time when used as input	13	22		27		ns
3	SYSCLK Low Time when used as input	13	19		22		ns
4	SYSCLK Rise Time	2		5		5	ns
5	SYSCLK Fall Time	2		5		5	ns
6	Synchronous SYSCLK Output Valid Delay	3, 12	0	16	0	16	ns
6A	Synchronous SYSCLK Output Valid Delay for D31–D0	12	0	20	0	20	ns
7	Three-State Synchronous SYSCLK Output Invalid Delay	4, 14, 15	0	30	0	30	ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	5, 12	0	16	0	16	ns
8A	Three-State $\overline{\text{SYSCLK}}$ Synchronous Output Invalid Delay	5, 14, 15	0	30	0	30	ns
9	Synchronous Input Setup Time	7	15		15		ns
9A	Synchronous Input Setup Time for D31–D0, I31–I0		8		8		ns
9B	Synchronous Input Setup Time for $\overline{\text{DRDY}}$		16		16		ns
10	Synchronous Input Hold Time	6	2		2		ns
11	Asynchronous Input Minimum Pulse Width	8	T + 10		T + 10		ns
12	INCLK Period		25	62.5	30	62.5	ns
12A	INCLK to SYSCLK Delay		2	12	2	15	ns
12B	INCLK to $\overline{\text{SYSCLK}}$ Delay		2	12	2	15	ns
13	INCLK Low Time		10		12		ns
14	INCLK High Time		10		12		ns
15	INCLK Rise Time			5		5	ns
16	INCLK Fall Time			5		5	ns
17	INCLK to Deassertion of $\overline{\text{RESET}}$ (for phase synchronization of SYSCLK)	9	0	5	0	5	ns
18	$\overline{\text{WARN}}$ Asynchronous Deassertion Hold Minimum Pulse Width	10	4T		4T		ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	12	0	8	0	9	ns
20	Three-State Synchronous SYSCLK output invalid delay for D31–D0	11, 14, 15	0	25	0	25	ns

Notes:

1. *AC measurements made relative to 1.5 V, except where noted.*
2. *SYSCLK rise and fall times measured between 0.8 V and (V_{CC} – 1.0 V).*
3. *Synchronous Outputs relative to SYSCLK rising edge include: A31–A0,* $\overline{\text{BGRT}}$*, R/*$\overline{\text{W}}$*, SUP/*$\overline{\text{US}}$*,* $\overline{\text{LOCK}}$*, MPGM1–MPGM0,* $\overline{\text{IREQ}}$*, IREQT,* $\overline{\text{PIA}}$*,* $\overline{\text{DREQ}}$*, DREQT1–DREQT0,* $\overline{\text{PDA}}$*, OPT2–OPT0, STAT2–STAT0, and MSERR.*
4. *Three-state Synchronous Outputs relative to SYSCLK rising edge include: A31–A0, R/*$\overline{\text{W}}$*, SUP/*$\overline{\text{US}}$*,* $\overline{\text{LOCK}}$*, MPGM1–MPGM0,* $\overline{\text{IREQ}}$*, IREQT,* $\overline{\text{PIA}}$*,* $\overline{\text{DREQ}}$*, DREQT1–DREQT0,* $\overline{\text{PDA}}$*, and OPT2–OPT0.*
5. *Synchronous Outputs relative to SYSCLK falling edge (*$\overline{\text{SYSCLK}}$*):* $\overline{\text{IBREQ}}$*,* $\overline{\text{DBREQ}}$*.*
6. *Synchronous Inputs include:* $\overline{\text{BREQ}}$*,* $\overline{\text{PEN}}$*,* $\overline{\text{IRDY}}$*,* $\overline{\text{IERR}}$*,* $\overline{\text{IBACK}}$*,* $\overline{\text{DERR}}$*,* $\overline{\text{DBACK}}$*,* $\overline{\text{CDA}}$*, I31–I0,* $\overline{\text{DRDY}}$*, and D31–D0.*
7. *Synchronous Inputs include:* $\overline{\text{BREQ}}$*,* $\overline{\text{PEN}}$*,* $\overline{\text{IRDY}}$*,* $\overline{\text{IERR}}$*,* $\overline{\text{IBACK}}$*,* $\overline{\text{DERR}}$*,* $\overline{\text{DBACK}}$*, and* $\overline{\text{CDA}}$*.*
8. *Asynchronous Inputs include:* $\overline{\text{WARN}}$*,* $\overline{\text{INTR}}$*3–*$\overline{\text{INTR}}$*0,* $\overline{\text{TRAP}}$*3–*$\overline{\text{TRAP}}$*0, and CNTL1–CNTL0.*
9. $\overline{\text{RESET}}$ *is an asynchronous input on assertion/deassertion. As an option to the user,* $\overline{\text{RESET}}$ *deassertion can be used to force the state of the internal divide-by-two flip-flop to synchronize the phase of SYSCLK (if internally generated) relative to* $\overline{\text{RESET}}$*/INCLK.*
10. $\overline{\text{WARN}}$ *has a minimum pulse width requirement upon deassertion.*
11. *To guarantee Store/Load with one-cycle memories, D31–D0 must be asserted relative to SYSCLK falling edge from an external drive source.*
12. *Refer to Capacitive Output Delay table when capacitive loads exceed 80 pF.*
13. *When used as an input, SYSCLK presents a 90-pF maximum load to the external driver. When SYSCLK is used as an output, timing is specified with an external load capacitance of* $\leq$ *200 pF.*
14. *Three-State Output Inactive Test Load. Three-State Synchronous Output Invalid Delay is measured as the time to a* $\pm$*500 mV change from prior output level.*
15. *When a three-state output makes a synchronous transition from a valid logic level to a high-impedance state, data is guaranteed to be held valid for an amount of time equal to the lesser of the minimum Three-state Synchronous Output Invalid Delay and the minimum Synchronous Output Valid Delay.*

Conditions:

a. *All inputs/outputs are TTL compatible for V_{IH}, V_{IL}, V_{OH}, and V_{OL} unless otherwise noted.*

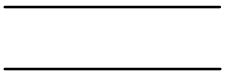
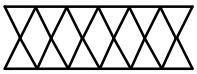
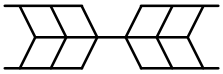
b. *All output timing specifications are for 80 pF of loading.*

c. *All setup, hold, and delay times are measured relative to SYSCLK or INCLK unless otherwise noted.*

d. *All input Low levels must be driven to 0.45 V and all input High levels must be driven to 2.4 V except SYSCLK.*

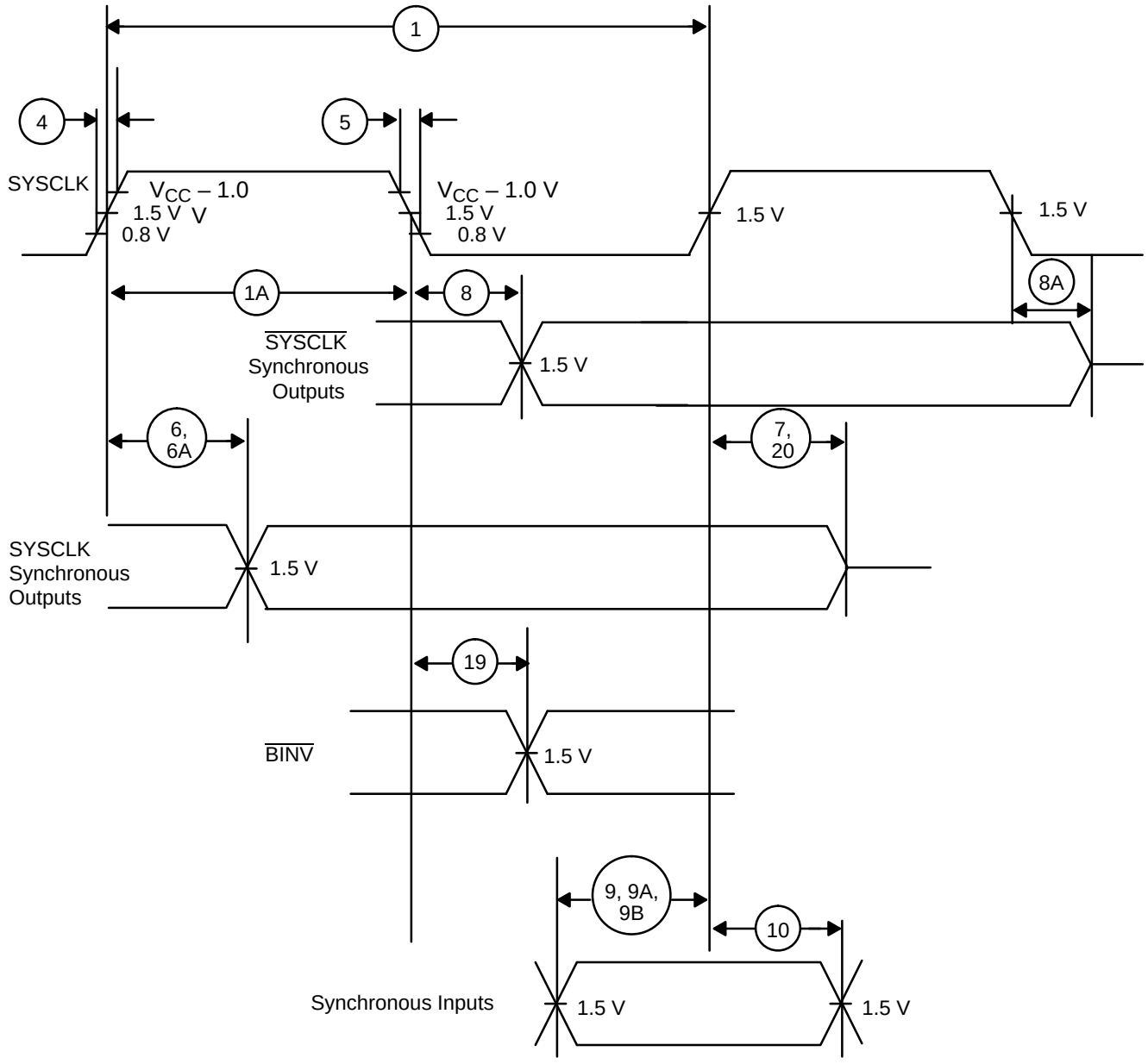
SWITCHING WAVEFORMS

Key To Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance “Off” State

SWITCHING WAVEFORMS (continued)

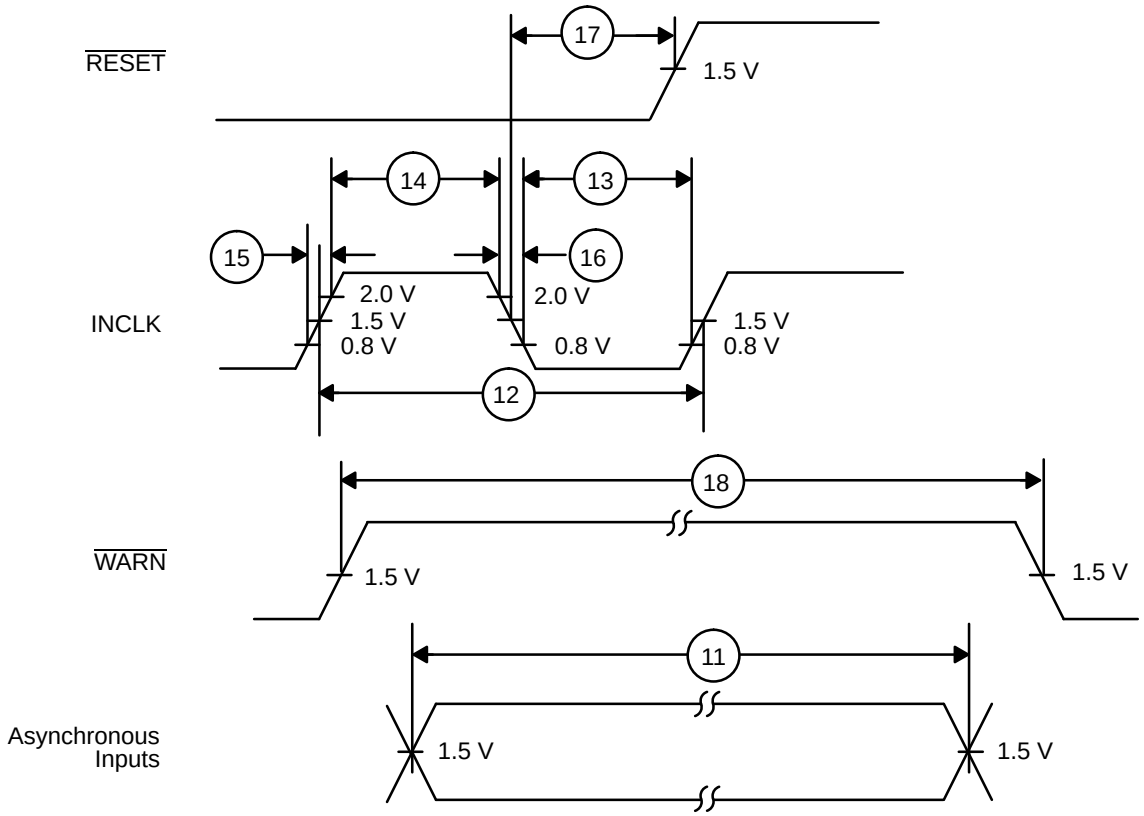
Relative to SYSCLK



09075–006A

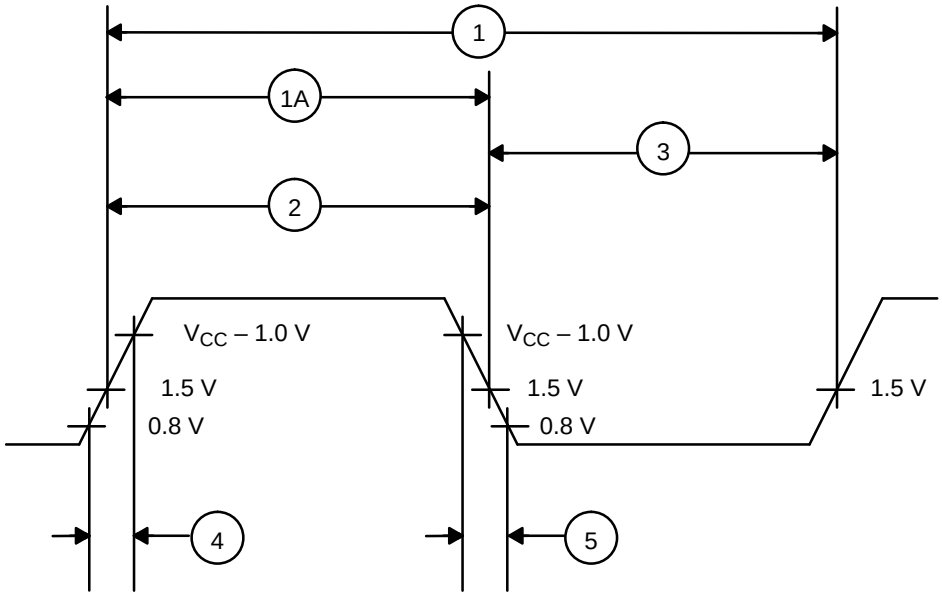
SWITCHING WAVEFORMS (continued)

INCLK and Asynchronous Inputs



09075–007A

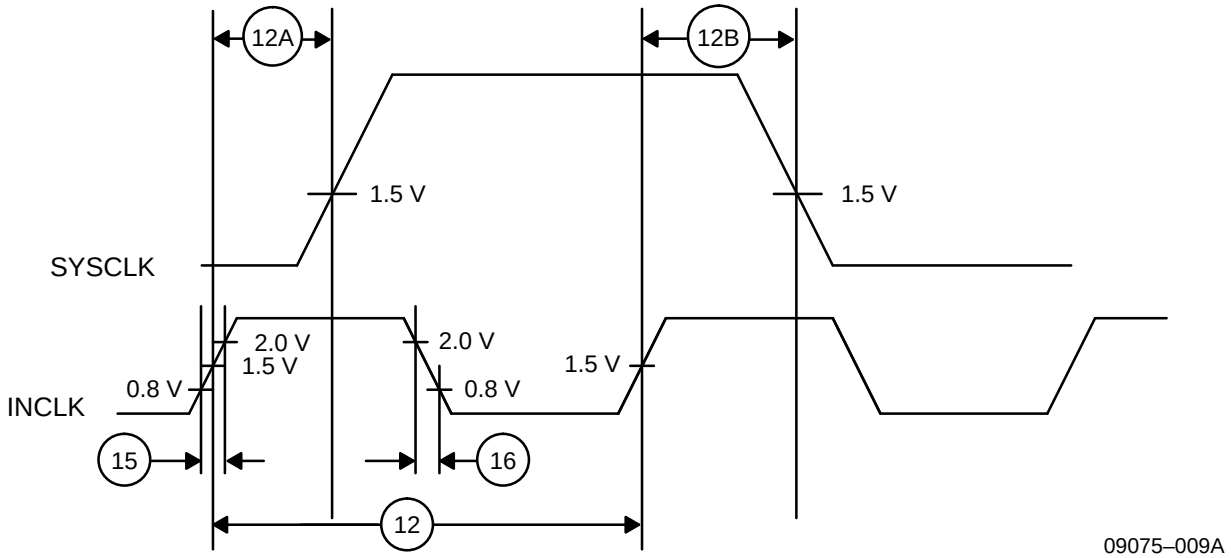
SYSCLK Definition



09075–008A

SWITCHING WAVEFORMS (continued)

INCLK to SYSCLK Delay



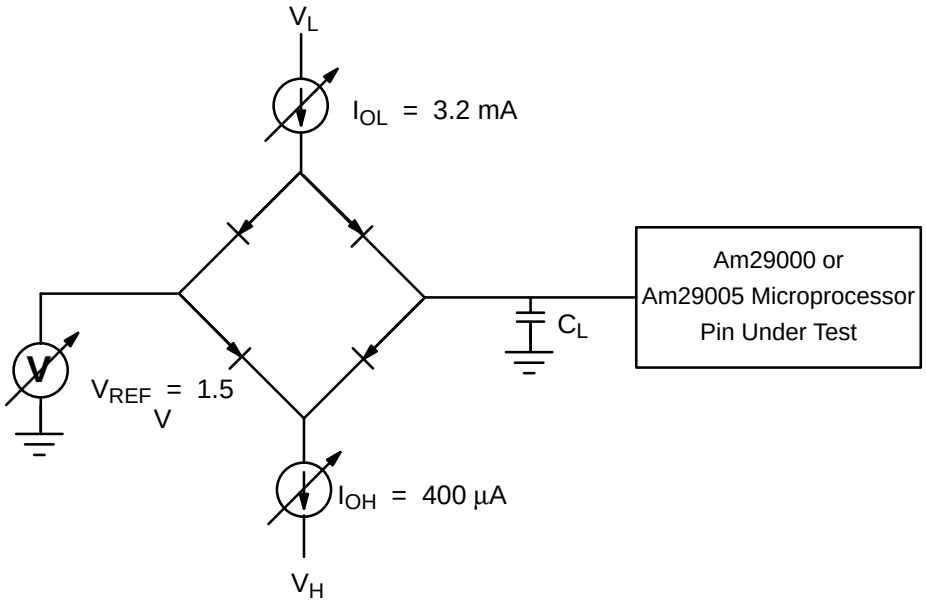
CAPACITIVE OUTPUT DELAYS

For loads greater than 80 pF

This table describes the additional output delays for capacitive loads greater than 80 pF. Values in the Maximum Additional Delay column should be added to the value listed in the Switching Characteristics table. For loads less than or equal to 80 pF, refer to the delays listed in the Switching Characteristics table.

No.	Parameter Description	Total External Capacitance	Maximum Additional Delay
6	Synchronous SYSCLK Output Valid Delay	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +2 ns +4 ns +6 ns +8 ns
6A	Synchronous SYSCLK Output Valid Delay for D31–D0	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +6 ns +10 ns +15 ns +19 ns
8	Synchronous $\overline{\text{SYSCLK}}$ Output Valid Delay	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +2 ns +4 ns +6 ns +8 ns
19	$\overline{\text{BINV}}$ Synchronous Output Valid Delay from $\overline{\text{SYSCLK}}$	100 pF 150 pF 200 pF 250 pF 300 pF	+1 ns +3 ns +4 ns +6 ns +7 ns

SWITCHING TEST CIRCUIT

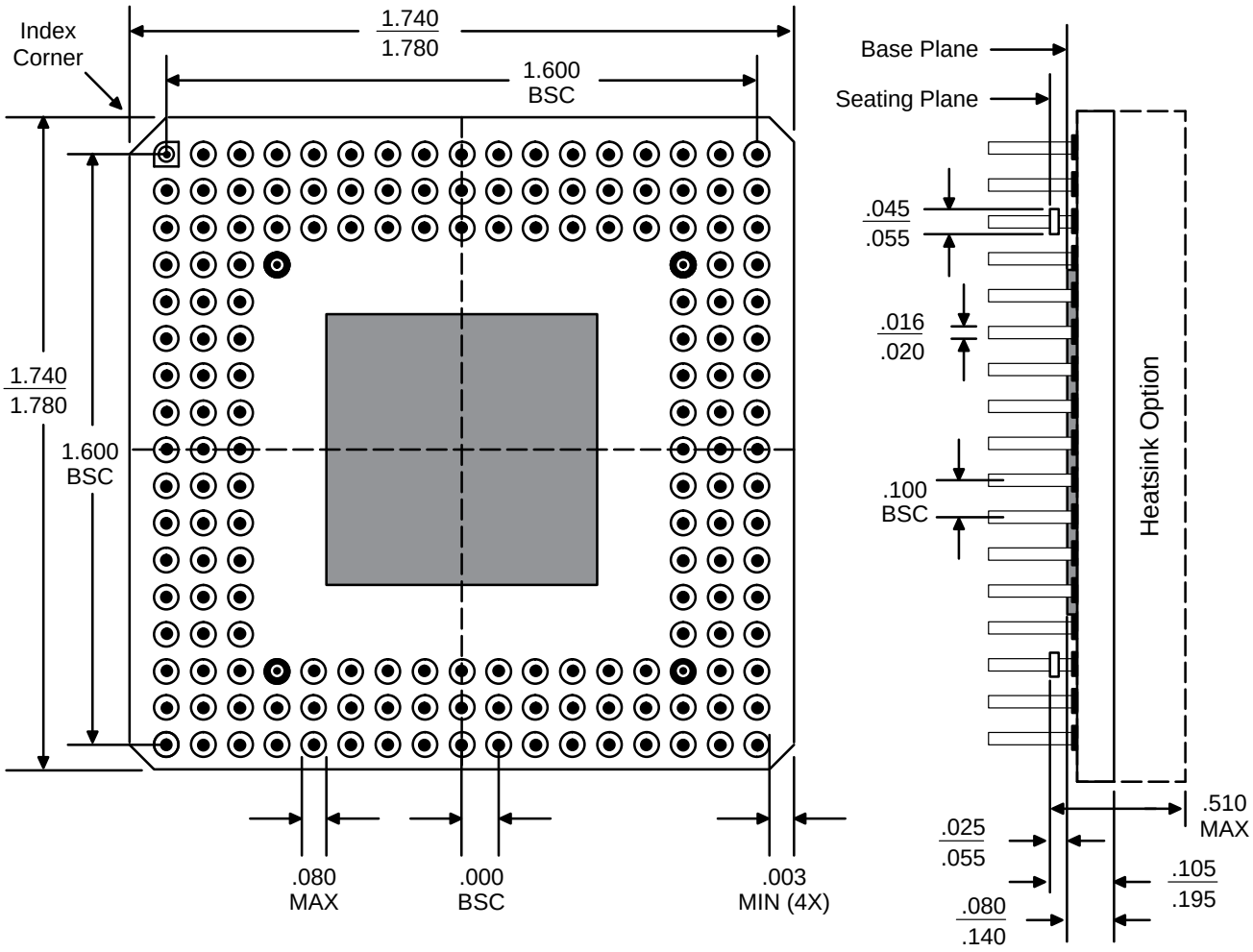


C_L is guaranteed to 80 pF. For capacitive loading greater than 80 pF, refer to the Capacitive Output Delay table.

09075–010A

PHYSICAL DIMENSIONS

CGX 169 Pin Grid Array (measured in inches)



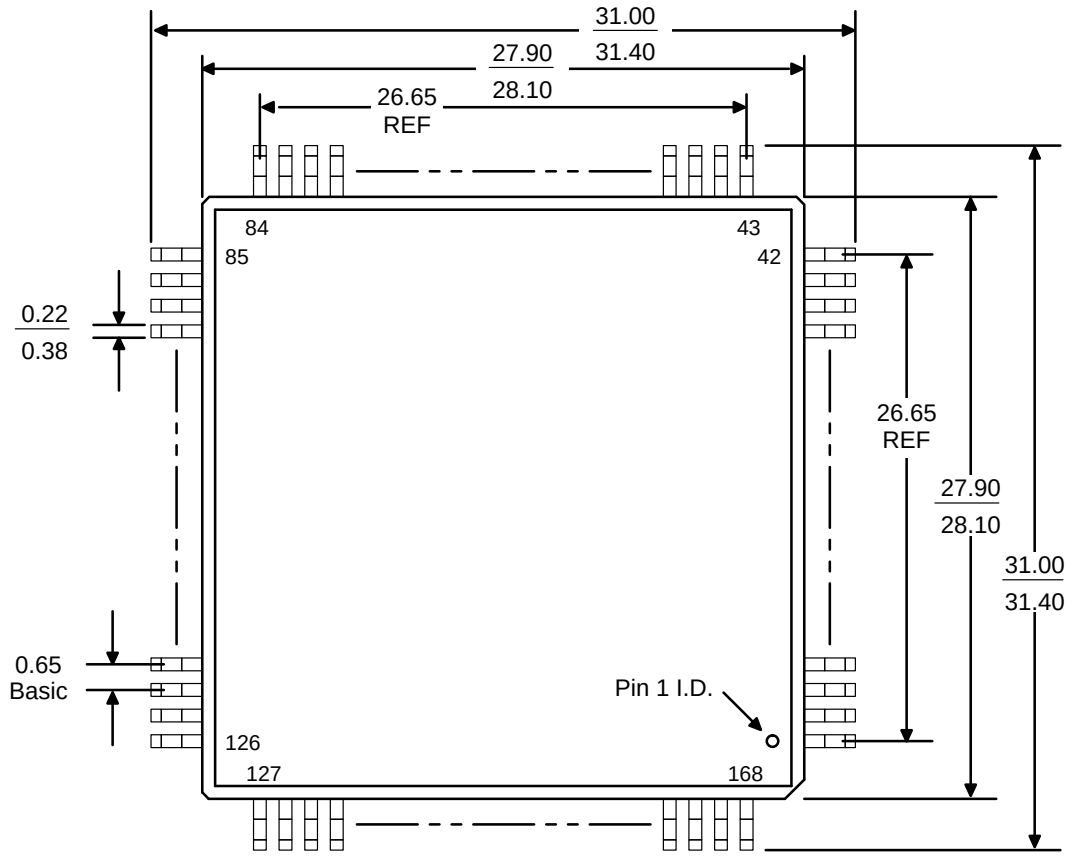
Bottom View **Side View**

07322E
BP 37 CGX169
7/8/92 c dc
09075–011A

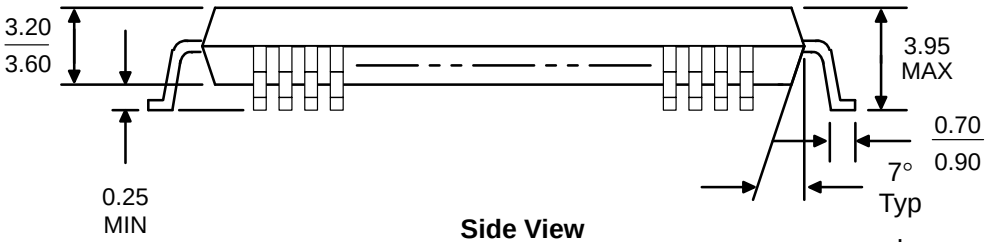
Note:

BSC is an ANSI standard for Basic Space Centering.

PQR 168 Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)



Top View



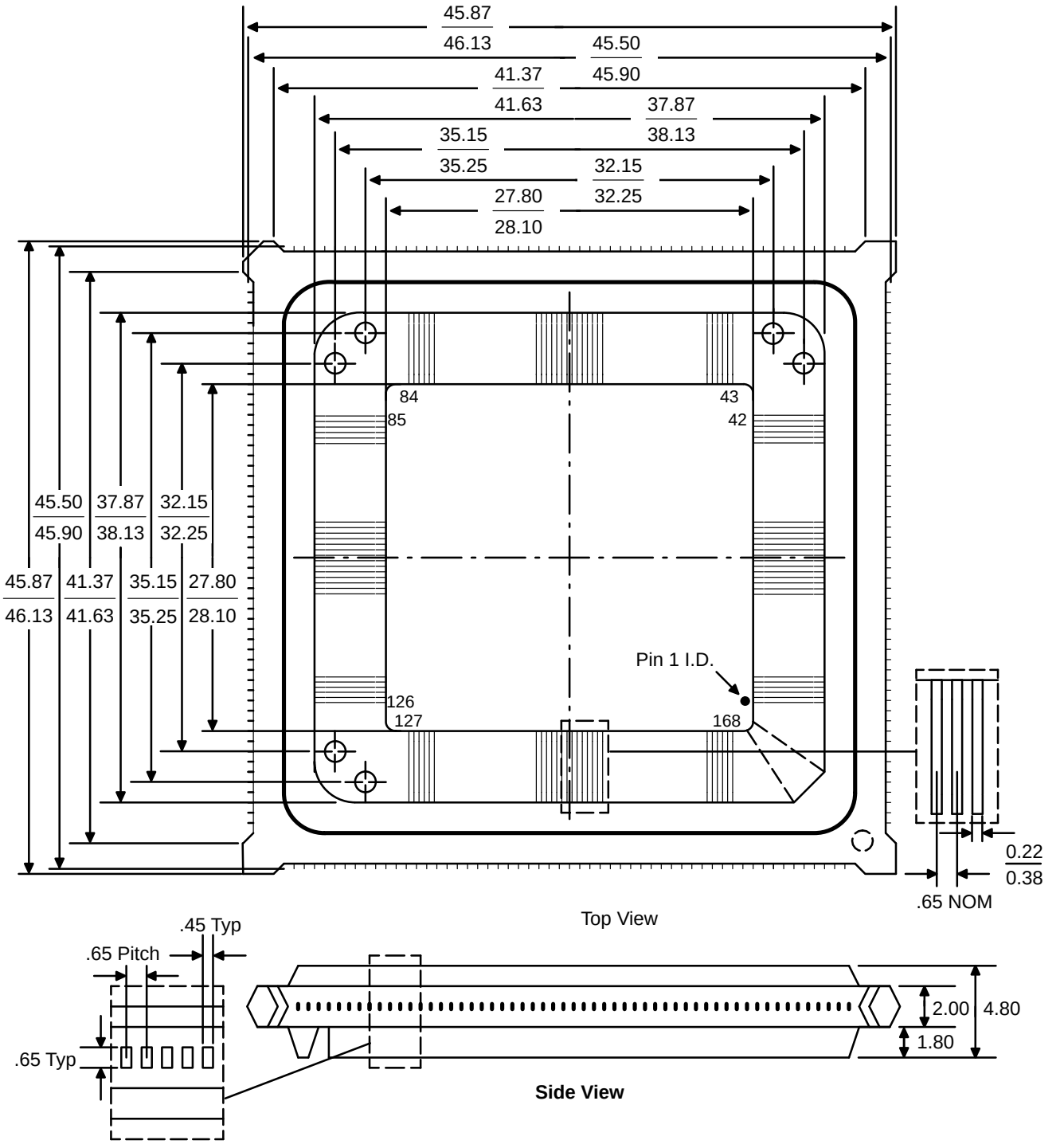
Side View

14995C
CG 47
5/4/92 SG
09075–012A

Note:

All dimensions are measured in millimeters unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.

PQR 168 Plastic Quad Flat Pack with Molded Carrier Ring (measured in millimeters)



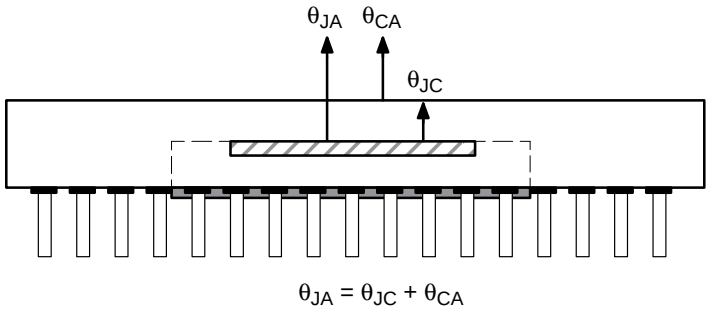
15000C
CG 50
5/4/92 SG
09075–013A

Note:

All dimensions are measured in millimeters unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.

THERMAL CHARACTERISTICS

Pin Grid Array (PGA) Package



Average Thermal Resistance — °C/Watt

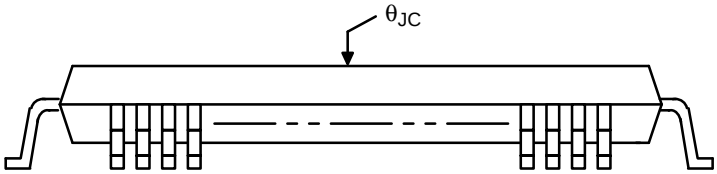
Parameter	Airflow—ft./min. (m/sec) 0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.05)
θ_{JC} Junction-to-Case	2	2	2	2	2
θ_{CA} Case-to-Ambient (no Heatsink)	20	16	15	14	12
θ_{CA} Case-to-Ambient (with omnidirectional 4-Fin Heatsink, Thermalloy 0417261)	9	7	4	3	2

Notes:

09075–014A

1. *θ_{JC} measured in controlled fluorinert fluid bath as infinite heatsink medium.*
2. *$\theta_{JA} = \theta_{JC} + \theta_{CA}$.*

Plastic Quad Flat Pack (PQFP) Package



PQFP Thermal Resistance — °C/Watt

Parameter	Airflow—ft./min. (m/sec) 0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.05)
θ_{JC} Junction-to-Case	10	10	10	10	10
θ_{CA} Case-to-Ambient (no Heatsink)	27	23	21	18	17

Notes:

09075–015A

1. *θ_{JC} measured in controlled fluorinert fluid bath as infinite heatsink medium.*
2. *$\theta_{JA} = \theta_{JC} + \theta_{CA}$.*