Digital DNA™
from Motorola

MOTOROLA
Semiconductor Products Sector

Why ColdFire ?

Complementing Embedded 32-bit Architectures

PowerPC™

Value in Performance

- Highest performance 32-bit RISC architecture
- Desktop software compatibility
- Full computer architecture
- Optimized for high-performance embedded applications

68K ColdFire® Microprocessors

Value in Legacy

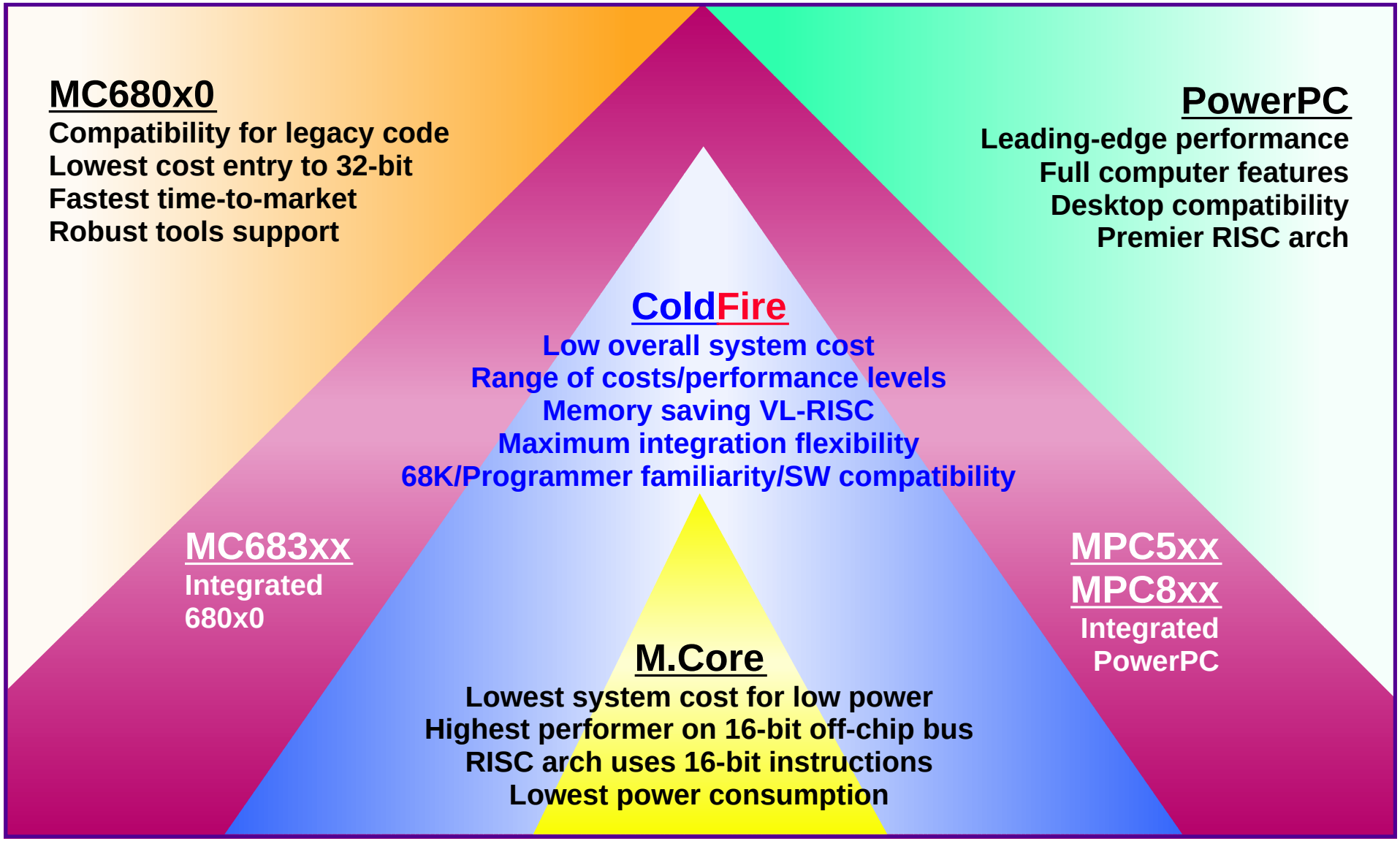
- 32-bit RISC architecture using variable length instructions
- 68K Programmer familiarity/software compatibility
- Low overall systems cost -- compact code density
- A range of costs /performance levels

m•core™

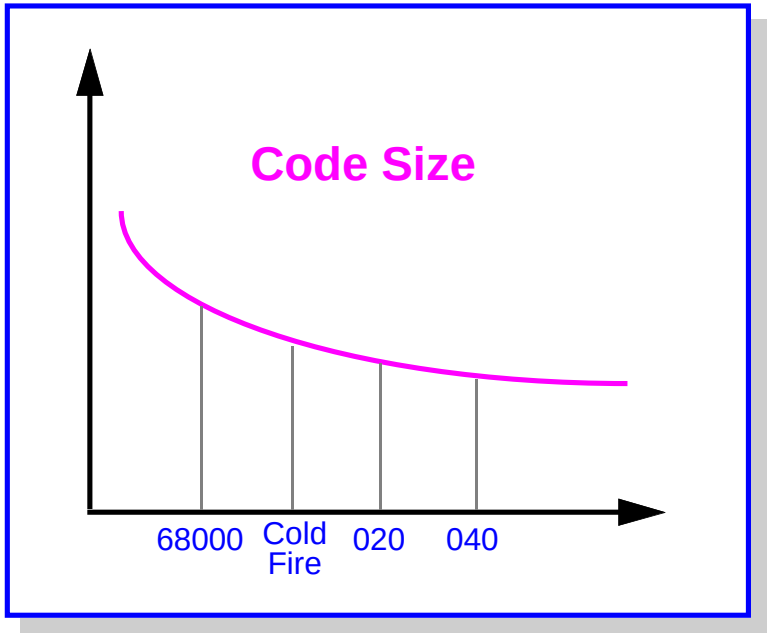
Value in Low Power

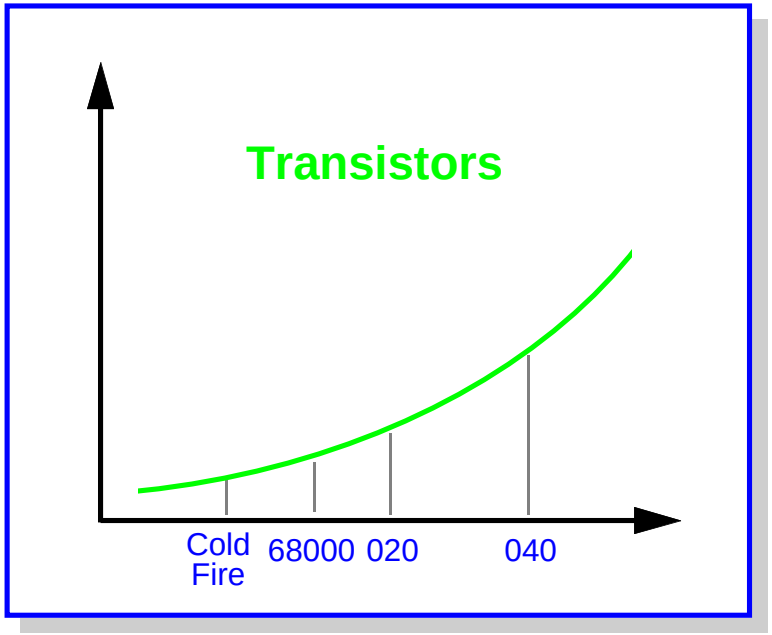
- 32-bit RISC architecture using 16-bit instructions
- Lowest power consumption
- Lowest system cost for low power
- Highest performer on 16-bit off-chip bus

Where ColdFire Fits in Motorola's 32-Bit Processing Solutions



Instruction Set Complexity

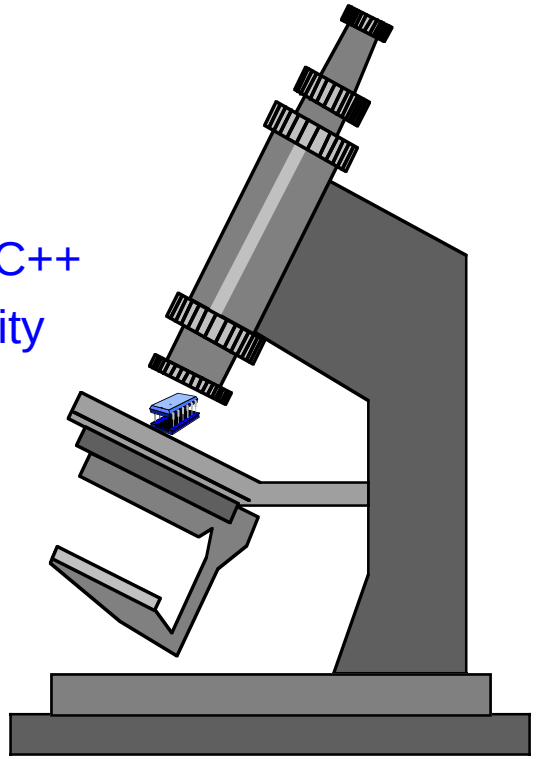




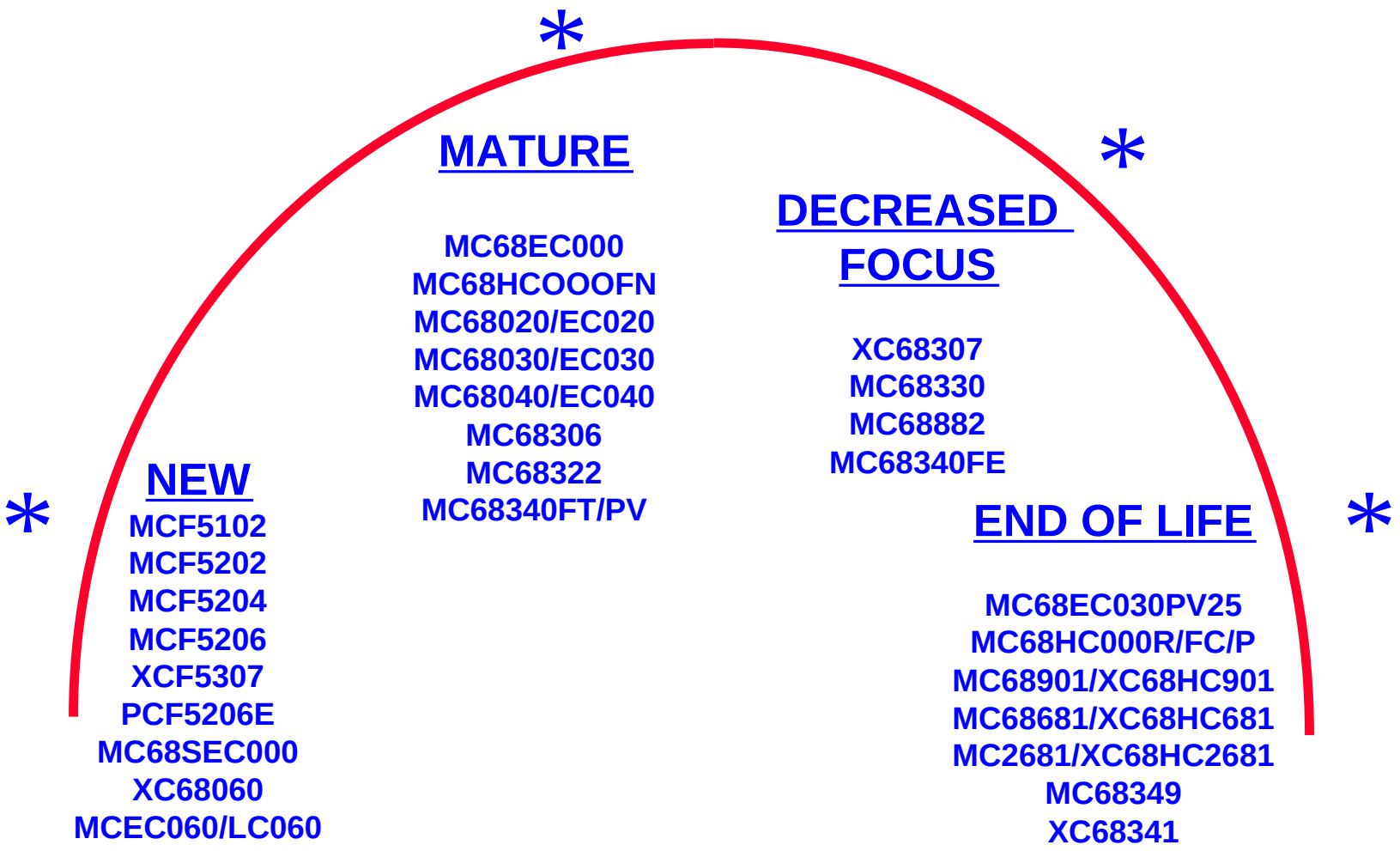
- Optimize core size by balancing instruction set with code size
  - Eliminate instructions rarely or never emitted by compilers
  - Minimize dynamic code expansion
  - Optimize transistor count -> minimal power and core size

A New RISC Architecture based on 68K

- **Started with a clean slate**
  - Existing 68K product offerings did not address all of the embedded design issues
- **Defined needs for embedded applications**
  - Identified instructions required for CPU support of C/C++
  - Variable-length instruction set is critical to code density
    - » Reduces memory size and bandwidth requirements
- **Maintained close ties to MC680x0 architecture**
  - Maps instructions onto M68000 op-codes
  - Easy transition in tools support
  - Capitalizes on programmer familiarity
    - » Very similar to 68K architecture
  - Decreases time-to-market

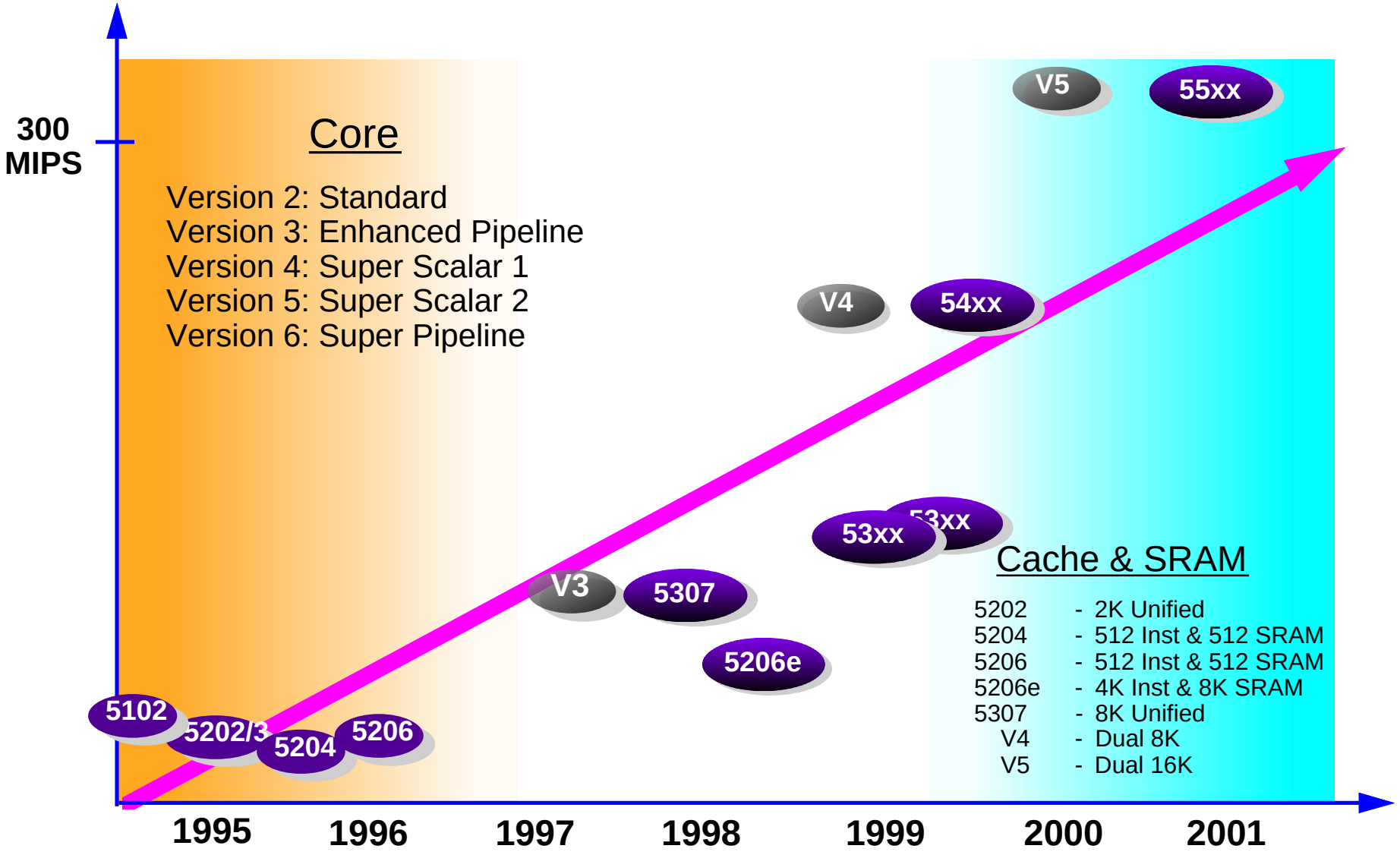


68K / ColdFire® PRODUCT LIFE CYCLE



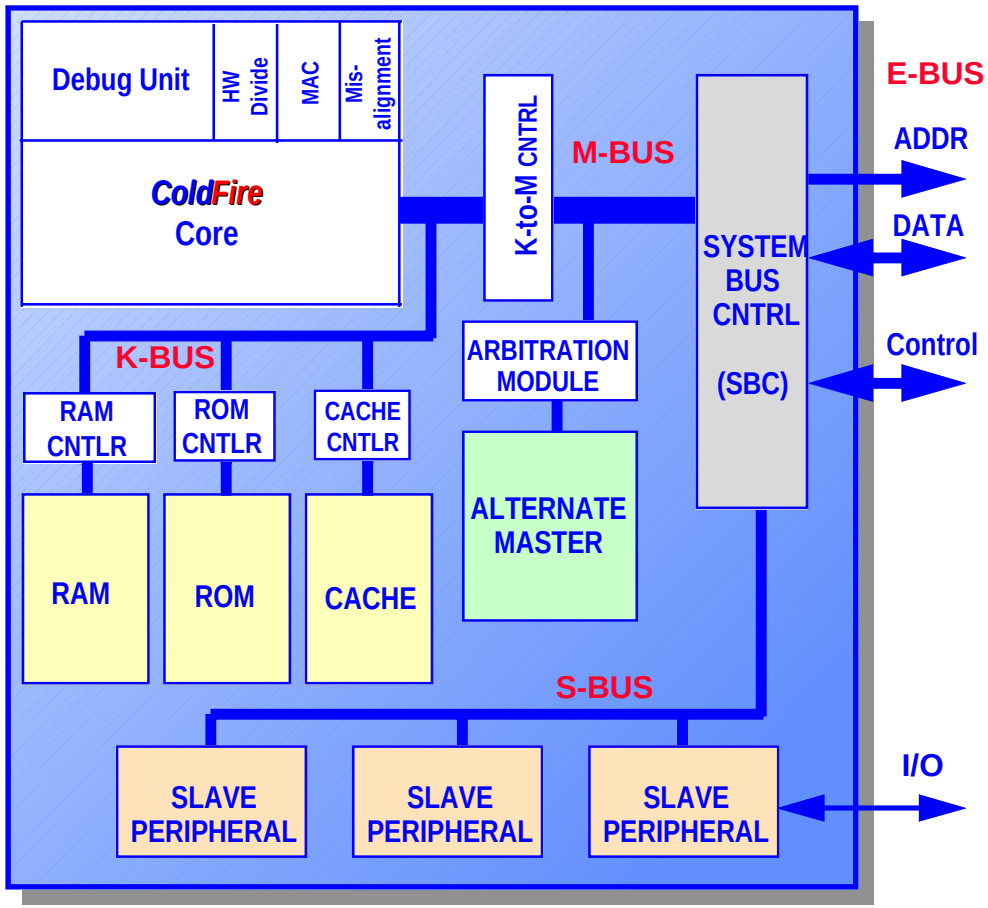
ColdFire Roadmap and Device Overview

ColdFire® Core Performance Roadmap



ColdFire® Architecture

- ColdFire's internal hierarchical bus structure {K, M, S} provides layers of bandwidth and an efficient partitioning of the optional on-chip modules.
- *K-Bus* is a single-cycle bus that provides maximum bandwidth for the ColdFire Core and its dedicated memories.
- *M-Bus* is a multi-cycle bus connecting the processor complex and the SBC, plus any other bus masters.
- *S-Bus* is a simple multi-cycle "slave" bus controlled by the SBC that interfaces to integrated peripheral modules.
- The external bus (*E-Bus*) connects the MPU to the outside resources.

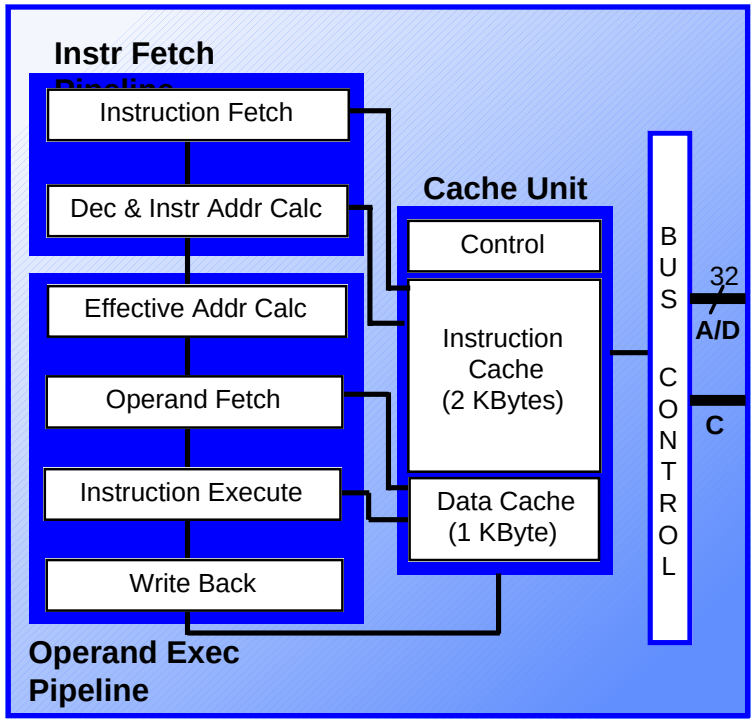


ColdFire Standard Products

MCF5102: The Bridge to ColdFire®

- **Features**
  - Fully ColdFire compatible
  - Includes ISA extensions to support 68EC0x0 binaries
    - » Bridges EC040 legacy to ColdFire
    - » S/W reuse
    - » Established tools
    - » Time-to-market
  - 2 Kbyte instruction cache
  - 1 Kbyte data cache
  - Muxed address/data bus
    - » Low cost 144 pin TQFP package
  - Low power–typically < 1W
- **Power Management**
  - 3.3v static design
    - » I/O to 3V or 5V logic
  - Variable frequency of operation
  - Software powerdown
- **Performance**
  - 44 Dhrystone 2.1 MIPs @ 40 MHz
- **Technology**
  - 0.5µm TLM CMOS

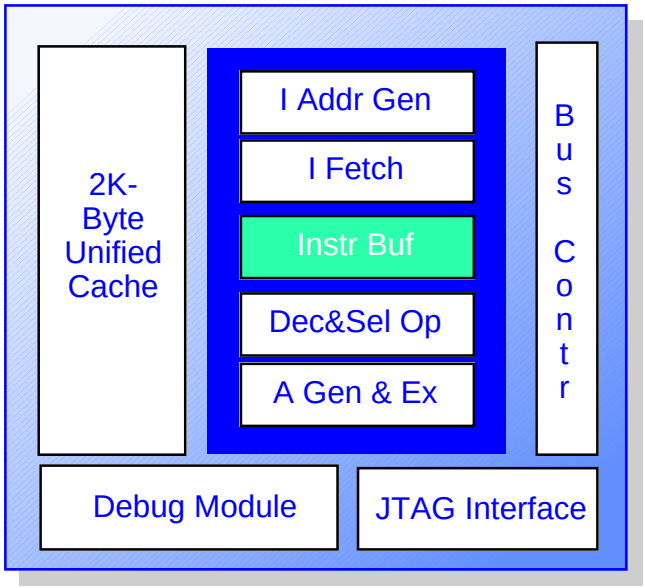
MCF5102



Second Generation ColdFire: The MCF5202/03

- **Features**
  - Fully ColdFire compatible
  - 2K Unified cache
    - » Non-blocking, 4-way set associative
  - Synchronous multiplexed bursting bus w/ dynamic bus sizing
    - » 32-bit data bus 5202
    - » 16-bit data bus 5203
  - Debug Module
  - JTAG Interface
  - 16, 25 & 33 MHz versions
- **Power Management**
  - Variable frequency of operation
  - Software powerdown
- **Performance***
  - MCF5202: 25 MIPS @ 33MHz
  - MCF5203: 24 MIPS @ 33MHz
- **Technology**
  - 0.8µm TLM CMOS
  - 100 pin TQFP package
  - 5202/03 extended temperature offering at 16 and 25 MHz available now
  - 5202/03: XC Production NOW (16, 25, 33 MHz)
  - 5202/03: MC Production 4Q98 (16, 25, 33 MHz)
  - 5202 Evaluation board: 68040IDP + 5202 Daughter card avail. NOW

MCF5202/03



* Dhrystone 2.1 MIPS using Diab 3.6f compiler

MCF5204

Features

- Fully ColdFire compatible
- Integrated Processor
  - » Two 16-Bit Timers
  - » UART
  - » General Purpose I/O
  - » System Integration Module incl. chip selects & interrupt controller
  - » Debug Module
- Asynchronous psuedo-burst bus w/ static bus sizing
  - » 16-bit non-multiplexed data bus
- 512 byte I-Cache + 512 byte I/D SRAM

Power Management

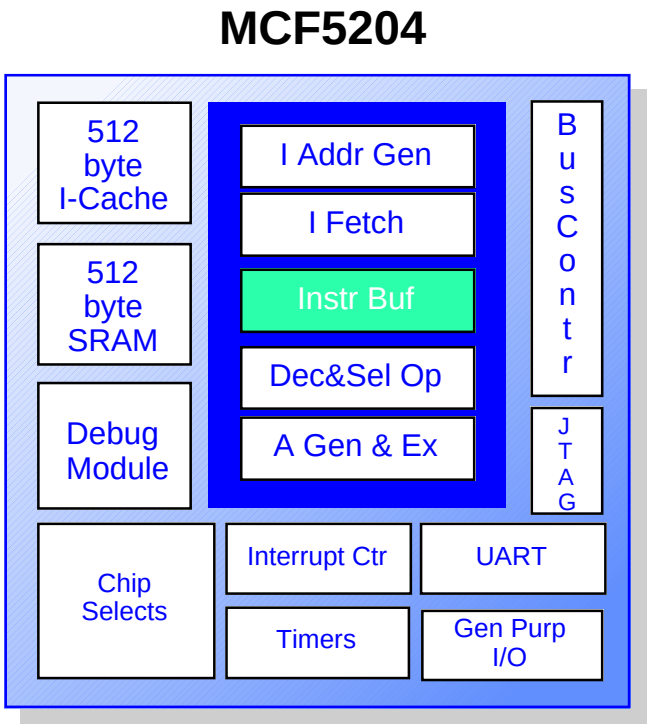
- Variable frequency of operation
- Software powerdown

Performance*

- 13.5 MIPs @ 33MHz

Technology

- 0.8µm TLM CMOS
- 100 pin QFP package
- 5204 extended temperature offering available now
- MC Production NOW (16, 25, 33 MHz)
- Low Cost Evaluation Board: Available NOW



* Dhrystone 2.1 MIPS using Diab 3.6f compiler

MCF5206

Features

- Fully ColdFire compatible
- Integrated Processor
  - » DRAM Controller (glueless interface):
    - »Supports Page mode & EDO RAM
  - » 2 UARTS
  - » Chip Selects
  - » 8-bit General-Purpose I/O
  - » M-bus interface (I^2C compatible*)
  - » Two 16-Bit Timers
  - » System Integration Module
- 32-bit non-multiplexed data bus w/ bus sizing
- 512 byte I-Cache + 512 byte I/D SRAM

Power Management

- Variable frequency of operation
- Software powerdown

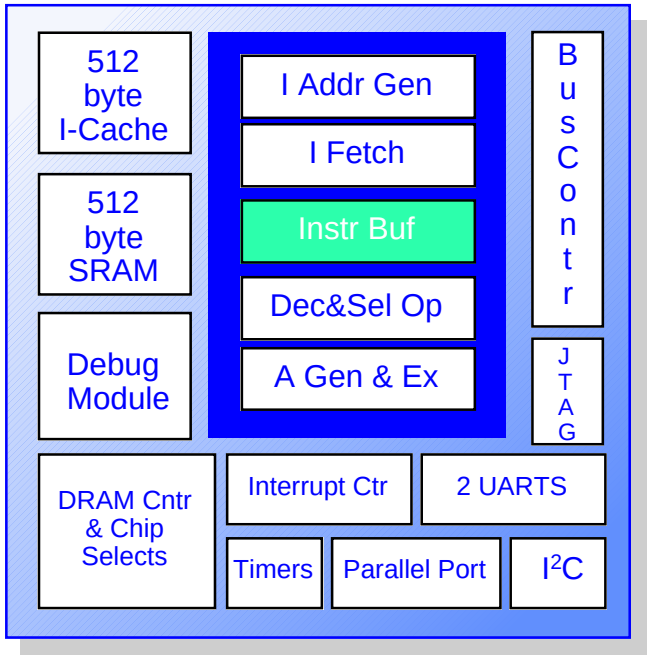
Performance**

- 17 MIPs @ 33MHz

Technology

- 0.8µm TLM CMOS
- 160 pin QFP package
- 5206 extended temperature offering available now
- MC Production: NOW (16, 25, 33 MHz)
- Low Cost Evaluation Board: NOW

MCF5206



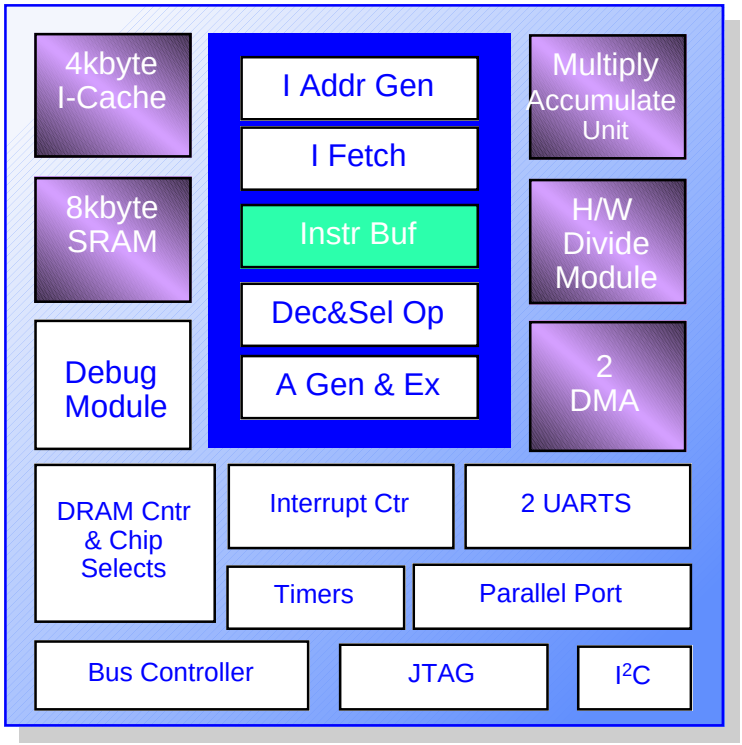
* I^2C is a Philips Proprietary Interface

** Dhrystone 2.1 MIPS using Diab 3.6f compiler

MCF5206e

- **Features**
  - Fully ColdFire ISA compatible
  - Integrated Processor
    - » DRAM Controller (glueless interface):
      - »Supports Page mode & EDO RAM
    - » 2 UARTS
    - » Chip Selects
    - » General-Purpose I/O
    - » M-bus interface (I^2C compatible)
    - » Two 16-Bit Timers
    - » System Integration Module
    - » DMA Controller - two channels
    - » Multiply Accumulate Unit
    - » Hardware divide module
  - 32-bit non-multiplexed data bus w/ bus sizing
  - 4 Kbyte I-Cache, 8 Kbyte SRAM
- **Power Management**
  - Variable frequency of operation
  - Software powerdown
- **Performance** *
  - 50 MIPS @ 54 MHz
- **Technology**
  - 0.35 µm TLM CMOS
  - Operating Voltage : 3.3 V, 5 V I/O Tolerant
  - 160 pin QFP package (pin compatible with 5206)
- **Availability**
  - Sampling available now
  - XC Production 7/98

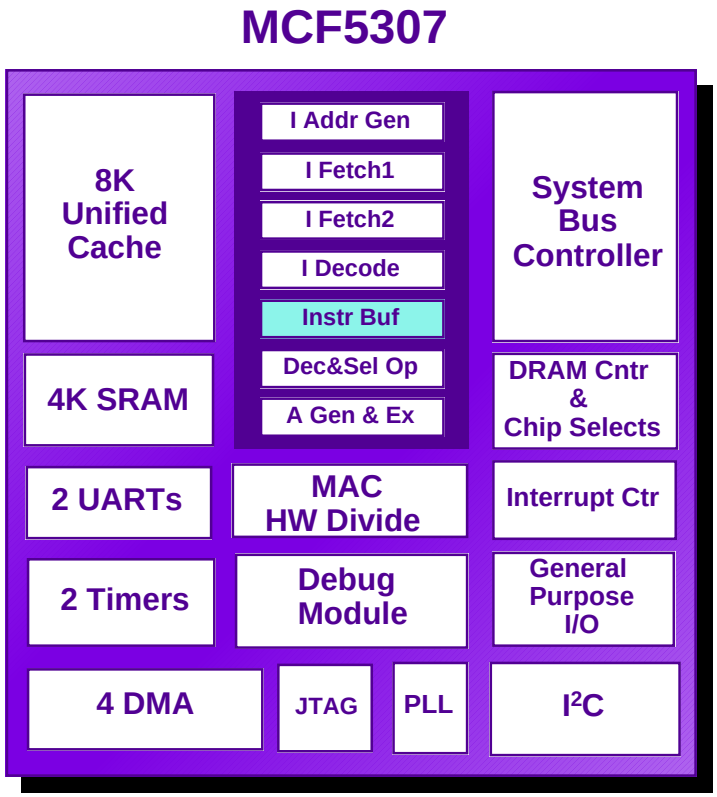
MCF5206e



* Dhrystone 2.1 MIPS

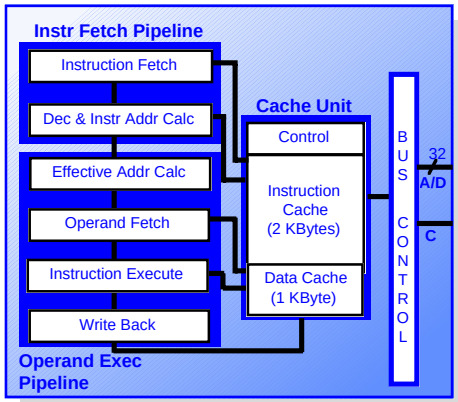
MCF5307

- **Features**
  - Fully ColdFire® compatible w/ Version3 Core
  - Integrated Processor
    - » DRAM Controller (glueless interface: EDO &SDRAM)
    - » 2 UARTS
    - » 4 channel DMA
    - » Chip Selects
    - » 16-bit General-Purpose I/O
    - » Two 16-Bit Timers
    - » M-bus interface (I^2C compatible)
    - » System Integration Module (PLL, SW Watchdog)
  - 32-bit non-multiplexed data bus w/ bus sizing
  - 8 KByte Unified Cache (4-way set associative; write through, copyback capability, non-blocking)
  - 4 KByte SRAM
  - MAC Module
  - HW Divide
- **Power Management**
  - Doze Mode & Variable frequency of operation
- **Performance**
  - 70 MIPS @ 90MHz
- **Technology**
  - 0.35µm TLM CMOS
  - 208 QFP
  - 3.3V pads / 5V tolerant
  - Offered at 90 MHz w/ bus programmability of 22.5, 30, and 45 MHz@ 0 to 70C
  - Offered at 66 MHz w/ bus programmability of 16.5, 22, and 33 MHz@ 0 to 70C, -40 to 85
  - 5307 extended temperature offering available 8/98
  - XC Production NOW
  - Evaluation board available NOW

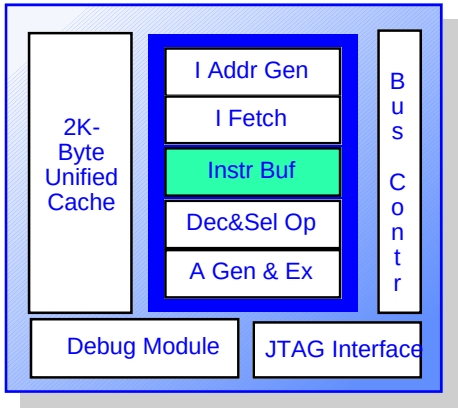


Standard Products in ColdFire Family

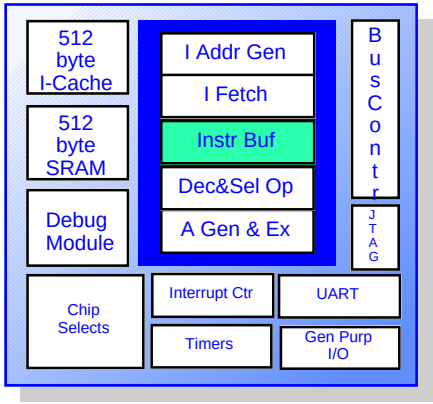
MCF5102



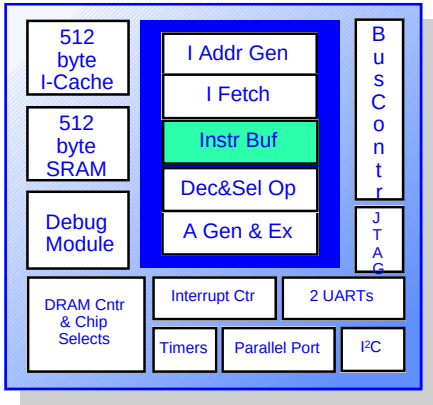
MCF5202/03



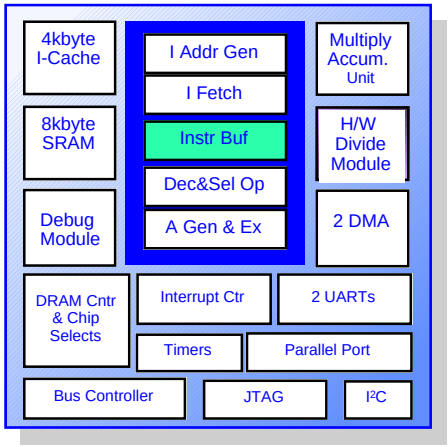
MCF5204



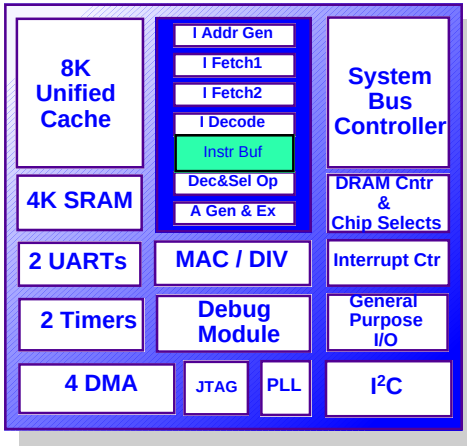
MCF5206



MCF5206e



MCF5307

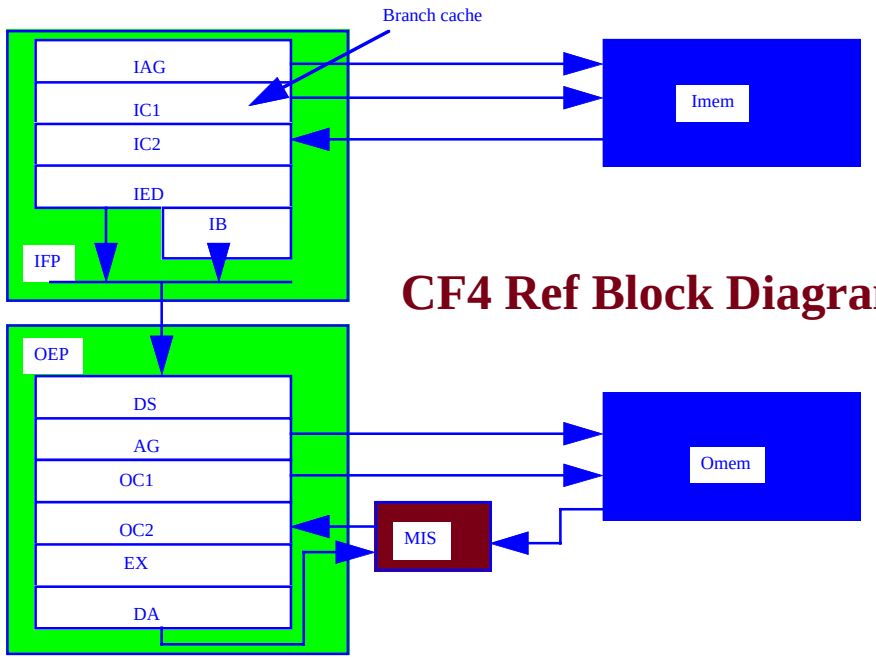


Device	Max Freq.	Perf. (Dhrystone 2.1 MIPS)
5102	40 MHz	44 MIPS
5202	33 MHz	25 MIPS
5203	33 MHz	24 MIPS
5204	33 MHz	13.5 MIPS
5206	33 MHz	17 MIPS
5206e	54 MHz	50 MIPS
5307	90 MHz	70 MIPS

ColdFire Device Summary

ColdFire Processor	MCF5102	MCF5202	MCF5203	MCF5204	MCF5206	MCF5206e	MCF5307
Frequency (MHz)	16,20,25,33,40	16,25,33	16,25,33	16,25,33	16,25,33	40,54	66,90
Voltage	3.3V	5V	5V	5V	5V	3.3V	3.3V
Power Dissipation (typical)	0.64W	0.59W	0.59W	0.63W	0.72W	TBD	0.95W
MIPS @ maximum MHz	44	25	24	13.5	17	50	70
Data Bus Size	32-bit, dynamic	32-bit, dynamic	16-bit, dynamic	16 bit, dynamic	32-bit, dynamic	32-bit, dynamic	32-bit, dynamic
Processor Cache (bytes)	2K I, 1K D	2K Unified	2K Unified	512 I-Cache	512 I-Cache	4K I-Cache	8K Unified
Processor RAM (bytes)				512	512	8K SRAM	4K SRAM
Serial Interface, UART				1	2	2	2
Timers				2	2	2	2
Chip Selects				6	8	8	8
General Purpose I/O Signals				8	8	8	16
Debug Module		Debug module	Debug module	Debug Module	Debug module	Debug module	Debug module
DMA						2-channel	4-channel
MAC						Yes	Yes
H/W Divide						Yes	Yes
DRAM Ctrl					Yes	Yes	Yes
M-Bus (I^2C)					Yes	Yes	Yes
SIM				Yes	Yes	Yes	Yes
Process/Package Type	0.5µ TLM 144 TQFP	0.8µ TLM 100 TQFP	0.8µ TLM 100 TQFP	0.8µ TLM 100 TQFP	0.8µ TLM 160 QFP	0.35µ TLM 160 QFP	0.35µ TLM 208 QFP

ColdFire Version 4



CF4 Ref Block Diagram

Version 4 is the next generation on the ColdFire core roadmap

- Adds microarchitectural enhancements to a Version 3 core base
- Significantly raises performance by lowering cycles-per-instruction (CPI)
- Also achieves higher frequencies

ColdFire V4 Microarchitecture

- Provides limited superscalar execution - approaching full dual-instruction issue performance, but at a much lower silicon cost
- Provides Harvard memory architecture for expanded core/ memory bandwidth
- V4 Operand Execution Pipeline [OEP] redesigned to execute most ColdFire instructions in 1 clock cycle
- Adds sophisticated two-level branch acceleration mechanisms
- V4 is a fully static design including gated clock implementation to minimize power dissipation

ColdFire V4 Specification Targets

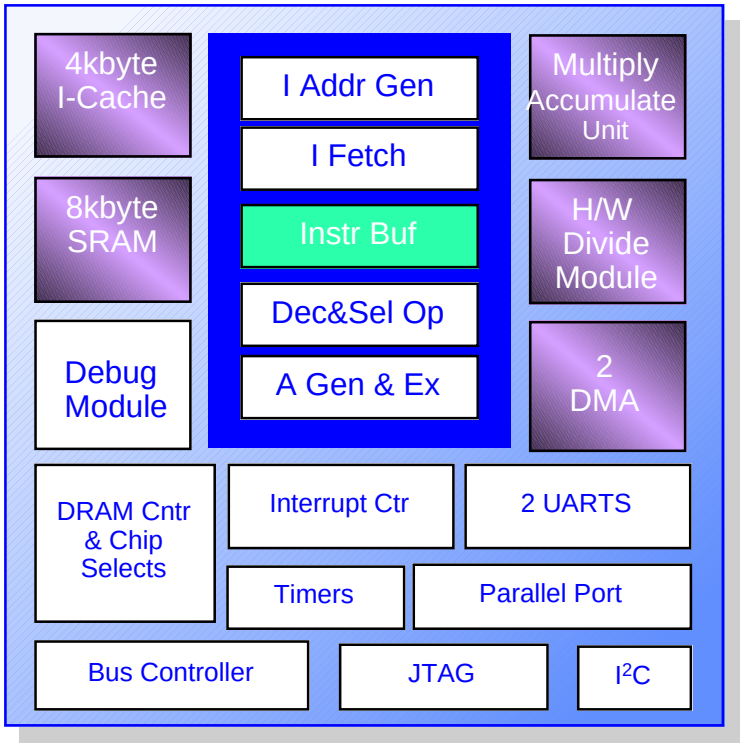
- **V4 Target Performance**
  - **~1.4 Dhrystone 2.1 MIPS/MHz [225 MIPS @ 166 MHz]**
  - **Base CPI of 1.4 (across broad range of embedded applications)**
  - **For imaging application suite:**
    - » 150/75 MHz V4 with 8K I-Cache & 8K D-Cache = 2.1 x 90/45 MHz ColdFire V3 with 8K Unified Cache (6-1-1-1 V4 and 4-1-1-1 V3 interfaces to external SDRAM)
- **V4 Target Frequency**
  - **150-166 MHz in HiP4 (.25μ) process technology**
- **V4 Target Size**
  - **Core plus processor-local Memories (8K I-, 8K O-Caches + 4K SRAM) in HiP4 process technology = ~12.2 mm^2**
- **V4 Target Deployment & Device Schedule Targets**
  - **V4 core deployed to internal & external partners - 3Q98**
  - **V4 FlexFire CPU and evaluation board - 1Q99**
    - » Core complex with M-bus pinout
    - » Configurable cache and SRAM sizes
  - **MCF5407 (1st V4 standard product) - 1H99**

Newest ColdFire Devices
5206e and 5307

MCF5206e

- **Features**
  - Fully ColdFire ISA compatible
  - Integrated Processor
    - » DRAM Controller (glueless interface):
      - »Supports Page mode & EDO RAM
    - » 2 UARTS
    - » Chip Selects
    - » General-Purpose I/O
    - » M-bus interface (I^2C compatible)
    - » Two 16-Bit Timers
    - » System Integration Module
    - » DMA Controller - two channels
    - » Multiply Accumulate Unit
    - » Hardware divide module
  - 32-bit non-multiplexed data bus w/ bus sizing
  - 4 Kbyte I-Cache, 8 Kbyte SRAM
- **Power Management**
  - Variable frequency of operation
  - Software powerdown
- **Performance** *
  - 50 MIPS @ 54 MHz
- **Technology**
  - 0.35 µm TLM CMOS
  - Operating Voltage : 3.3 V, 5 V I/O Tolerant
  - 160 pin QFP package (pin compatible with 5206)
- **Availability**
  - Sampling available now
  - XC Production 7/98

MCF5206e



* Dhrystone 2.1 MIPS

MCF5206e: for current ColdFire® customers

- **Pin compatibility, feature set and bus interface similarity makes the 5206e a natural performance upgrade for 5206 users.**
  - 5206 is our most popular device today
  - Many of the peripherals have been re-used from the 5206 to 5206e to ease user transition (timer, UART, M-bus)
- **The 5206e will give 5206 users *2 channels of DMA, increased internal memory, MAC unit, hardware divide and pin compatibility***

FEATURE SET	5206	5206e	Upgrade Advantages
CORE	17 MIPS V2 Core	50 MIPS V2 Core	Software/Programming Model Compatibility
MEMORY	512B I-Cache/512B RAM	4K I-cache, 8K SRAM	Larger On-chip Memories
MAC UNIT	None	Yes	Enhanced functionality of DSP algorithm
H/W DIVIDE	None	Yes	
BUS INTERFACE	28-bit Addr./32-bit Data	28-bit Addr/32-bit Data	
M-BUS (I^2C)	Yes	Yes	
UART	2 UARTs	2 UARTs	
TIMER	2 16-bit timers	2 16-bit timers	
DMA	None	2 channel	High Performance DMA with auto-alignment, features & UART dedicated DMA option)
DRAM Ctrl	Yes	Yes	
SBC	Yes	Yes	
DEBUG MODULE	Yes	Yes	Offers powerful real-time trace and real-time debug capability
VOLTAGE	5V	3.3V	5V I/O Tolerant

MCF5206e: A solution for 68K customers

- The 5206e gives 68340 customers a performance (up to 5x) and enhanced integration upgrade path with a lower price
  - **Almost 3 million 68340 units shipped in 1997; much of this market share will be migrated to 5206e**
  - **The 5206e feature set along with the MicroAPL assembly tool creates an easy upgrade for 68340 customers**

FEATURE SET	68340	5206e	Upgrade Advantages
CORE	8 MIPS CPU32	50 MIPS V2 Core	Software/Programming Model Compatibility
MEMORY	None	4K cache, 8K SRAM	On-chip memory
MAC UNIT	None	Yes	Enhanced functionality of DSP algorithms
H/W DIVIDE	None	Yes	
BUS INTERFACE	32-bit Addr./16-bit Data	28-bit Addr/32-bit Data	More bus bandwidth
M-BUS (I^2C)	None	Yes	Offers fast bi-directional serial data transfer
UART	2 UARTs	2 UARTs	
TIMER	2 16-bit timers	2 16-bit timers	
DMA	2 channel	2 channel	5206e DMA encompasses more functionality (auto-alignment, UART dedicated DMA option)
DRAM Ctrl	None	Yes	Offers Asynchronous & EDO DRAM support
SBC	Yes	Yes	Offers more chip selects
DEBUG MODULE	BDM	BDM+RTD+RTT	Offers powerful real-time trace and real-time debug capability

5206e Key Messages

5206e offers:

- A pin compatible upgrade (although requires a 3.3 V supply)
- Higher performance - 50 Dhrystone 2.1 MIPS at 54 MHz
- Higher integration - 2 channel DMA, MAC, H/W Divide, larger internal memories
- Lower cost

✔ **5206e is extremely attractive due to lower cost and higher performance**

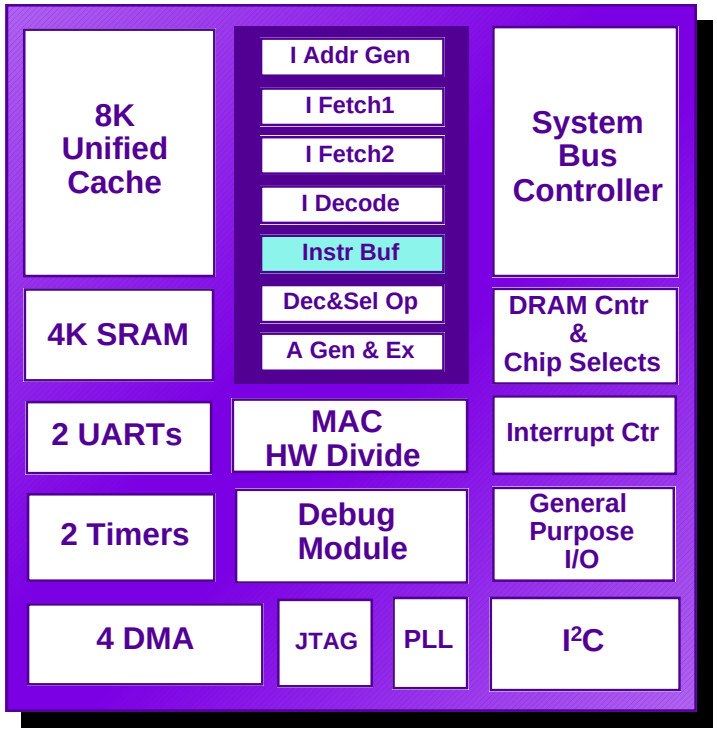
✔ **5206e achieves new price/performance level with V2 core, at lower cost**

✔ **Ease of moving the ColdFire® architecture to new technologies**

MCF5307

- **Features**
  - Fully ColdFire® compatible w/ Version3 Core
  - Integrated Processor
    - » DRAM Controller (glueless interface: EDO &SDRAM)
    - » 2 UARTS
    - » 4 channel DMA
    - » Chip Selects
    - » 16-bit General-Purpose I/O
    - » Two 16-Bit Timers
    - » M-bus interface (I^2C compatible)
    - » System Integration Module (PLL, SW Watchdog)
  - 32-bit non-multiplexed data bus w/ bus sizing
  - 8 KByte Unified Cache (4-way set associative; write through, copyback capability, non-blocking)
  - 4 KByte SRAM
  - MAC Module
  - HW Divide
- **Power Management**
  - Doze Mode & Variable frequency of operation
- **Performance**
  - 70 MIPS @ 90MHz
- **Technology**
  - 0.35µm TLM CMOS
  - 208 QFP
  - 3.3V pads / 5V tolerant
  - Offered at 90 MHz w/ bus programmability of 22.5, 30, and 45 MHz@ 0 to 70C
  - Offered at 66 MHz w/ bus programmability of 16.5, 22, and 33 MHz@ 0 to 70C, -40 to 85
  - 5307 extended temperature offering available 8/98
  - XC Production NOW
  - Evaluation board available NOW

MCF5307



MCF5307 DMA CONTROLLER FEATURES

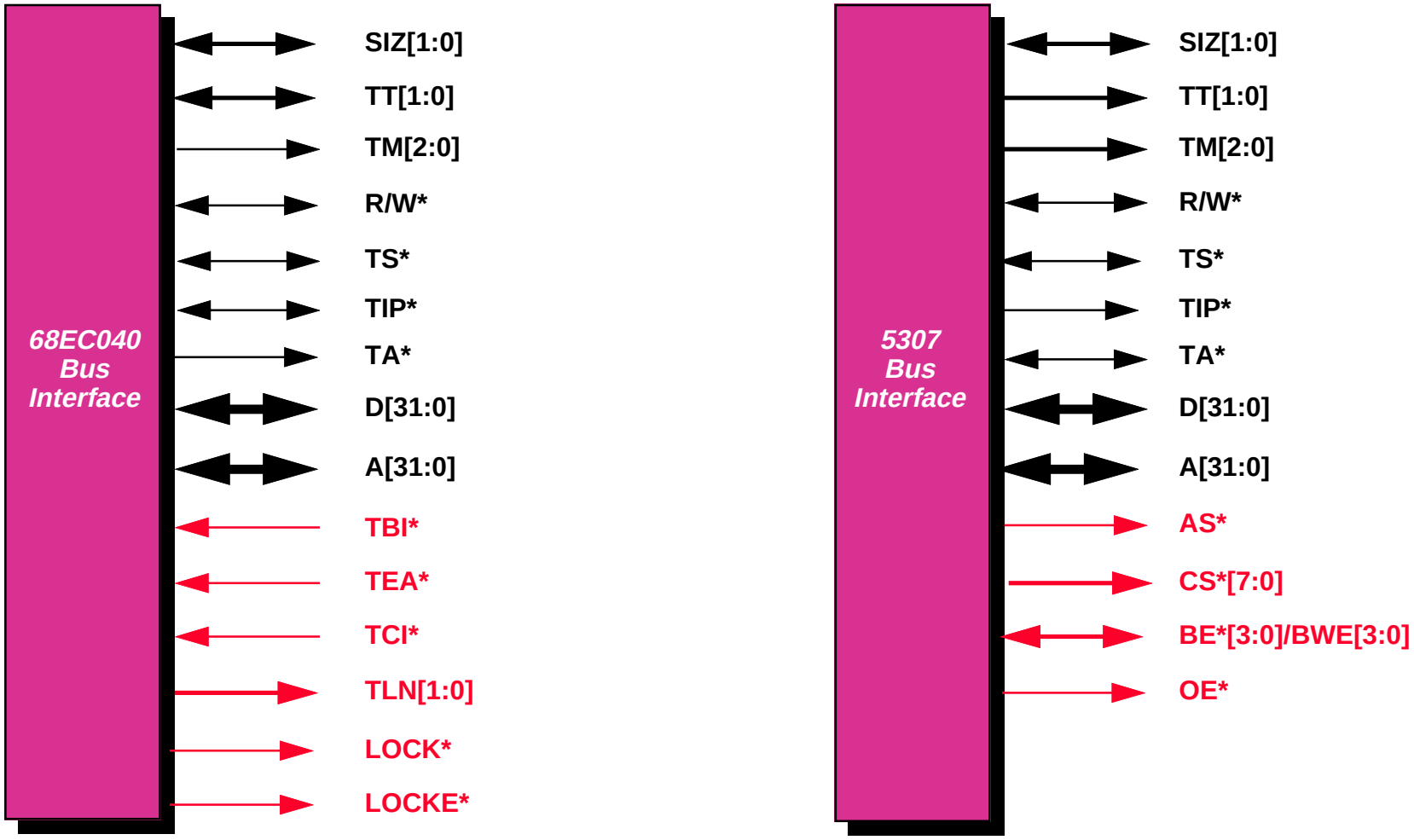
- ✔ Four Fully Independent DMA Channels (Two w/ external request pins)
- ✔ Single And Dual Address Transfer Operation
- ✔ 16-Byte Holding Buffer Size
- ✔ Data Transfer of 8, 16, 32 or 128-bit block w/ bursting capability
- ✔ Auto-Alignment capable on source or destination transfers
- ✔ DMA transfer operation can be initiated internally or externally
- ✔ Channel arbitration on transfer boundaries
- ✔ Two Address Pointers, source and destination
- ✔ 16-bit Byte Count Register allowing block transfers up to 64KBytes
- ✔ Support data transfers from and to:
  - memory to memory
  - peripheral to memory
  - memory to peripheral
- ✔ Independent transfer widths for source and destination
- ✔ Source and destination pointer may be programmed to increment after transfer or not
- ✔ DMA channel can be programmed for dedicated UART buffer transfers

MCF5307 DRAM FEATURES

- **THE FLEXIBLE DRAM CONTROLLER SUPPORTS 3 TYPES OF DRAMS GLUELESSLY:**
  - **1) ASYNCHRONOUS.** Has basic modes of operation:
    - Non-page mode
    - Burst page mode
    - Continuous page mode
  - **2) SYNCHRONOUS.** Supports common SDRAM implementations.
    - Burst page mode
    - Continuous Page mode
  - **3) EDO.**
    - Full Page Mode
    - Burst Page Mode

- **Synchronous & Asynchronous DRAM function differently.**
  - The DRAM registers are used differently
  - The DRAM pins are used differently
  - Both banks of DRAM will be in the same mode of operation based on programming the DRAM Configuration Register's (DCR) Synchronous Operation bit (SO bit)

68EC040, 5307 Bus Similarities



Burst-inhibit is enabled through chip-select registers on 5307; Note that another main difference between the 68EC040 & 5307 is that the 68EC040 has cache snoop controls

5307 Key Messages

- ✔ **5307 is optimal for three types of customers:**
  - **New customers** looking for a highly integrated, low cost 70 MIPS device
  - **Current 68K customers** (especially those using 68340 & 68040)
  - **Current ColdFire® customers** (especially 5206 customers needing higher performance)
- ✔ **5307 customers have comprehensive development tools support enhanced by our patented debug module**
  - **Real-time debug and real-time trace** capability from our debug module aid customers in gaining more insight into what their system is doing
  - Due to 68K opcode compatibility & programming model similarity, third party tool vendors can offer customers a **mature tool suite**
- ✔ **Non-ColdFire ISA execution capability**

MCF5307: A solution for 68K customers

- The 5307 gives 68340 customers a performance (up to 9x !) and enhanced integration upgrade path at 68340 prices!
  - **Over 3 million 68340 units shipped in 1997; much of this market share will be migrated to 5307**
  - **The 5307 feature set along with the MicroAPL assembly create an easy upgrade for 68340 customers**

FEATURE SET	68340	5206e	5307	Upgrade Advantages
CORE	8 MIPS CPU	50 MIPS V2 Core	70 MIPS V3 Core	Software/Programming Model Compatibility
MEMORY	None	4K cache, 8K SRAM	8K unified, 4K SRAM	On-chip memory
MAC UNIT	None	Yes	Yes	Enhanced functionality of DSP algorithms
H/W DIVIDE	None	Yes	Yes	
BUS INTERFACE	32-bit Addr./16-bit Data	32-bit Addr/32-bit Data	32-bit Addr/32-bit Data	More bus bandwidth
M-BUS (I^2C)	None	Yes	Yes	Offers fast bi-directional serial data transfer
UART	2 UARTs	2 UARTs	2 UARTs	
TIMER	2 16-bit timers	2 16-bit timers	2 16-bit timers	
DMA	2 channel	2 channel	4 channel	5307 DMA encompasses more functionality (auto-alignment, UART dedicated DMA option)
DRAM Ctrl	None	Yes	Yes	Offers Asynchronous, EDO, Synch DRAM support
SBC	Yes	Yes	Yes	Offers more chip selects
DEBUG MODULE	BDM	BDM+RTD+RTT	BDM+RTD+RTT	Offers powerful real-time trace and real-time debug capability

MCF5307: A solution for 68K customers

- The 5307 gives 68EC040 customers a performance (almost 2x !) and integration upgrade path at substantially lower prices
  - Almost a million 68EC040 units shipped in 1997
  - The 5307 bus interface similarities along with the MicroAPL assembly code translator creates an easy upgrade for 68EC040 customers

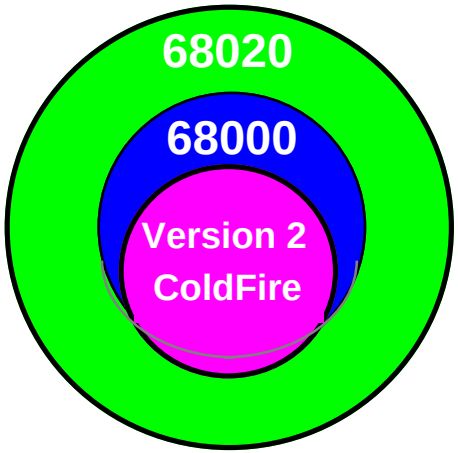
FEATURE SET	68EC040	5307	Upgrade Advantages
CORE	44 MIPS 040 Core	70 MIPS V3 Core	Software/Programming Model Compatibility
MEMORY	4K I-cache, 4K D-cache	8K unified, 4K SRAM	Larger On-chip Memories
MAC UNIT	None	Yes	Enhanced functionality of DSP algorithms
H/W DIVIDE	None	Yes	
BUS INTERFACE	32-bit Addr./32-bit Data	32-bit Addr/32-bit Data	
M-BUS (I^2C)	None	Yes	Offers fast bi-directional serial data transfer
UART	None	2 UARTs	Offers RS-232, Modem support
TIMER	None	2 16-bit timers	Offers pulse generation, timing features
DMA	None	4 channel	High Performance DMA with auto-alignment, features & UART dedicated DMA option)
DRAM Ctrl	None	Yes	Offers Asynchronous, EDO, Synch DRAM support
SBC	None	Yes	Offers chip selects w/ port sizing & wait state ctrl/ glueless interface to ROM, RAM
DEBUG MODULE	None	Yes	Offers powerful real-time trace and real-time debug capability

Possible ColdFire Customers

Current 68K Product	ColdFire Processor Upgrade
68010/020/030	• 5102/5202: Customer could use 5102/5202 if high performance is needed with minimal integration. Note that 5102/5202 have muxed buses. • 5204/5206e: If a smaller jump in performance and integration is needed, customer could use 5204/5206e.
68EC040	• 5102: For customers interested in 68EC040, the 5102 is a lower price alternative. • 5307: Offers high performance and lots of integration.
68306	• 5206 & 5206e: has same set of modules integrated on-chip and the added bonus of I-cache, SRAM, and M-bus (I^2C).
68307	• 5204/5206/5206e: All three could be solutions depending on the integration mix that is desired.
68330	• For those requiring limited peripheral integration, the 5102/5202/5203 is the answer. If integration is needed, select the 5204,5206,5206e.
68340/341/349	• 5206e: Offers closest match in existing peripherals with DMA (50 MIPS). • 5307: Offers lots of integration + DMA, extremely high performance jump (70 MIPS).

What are the differences between 68K and ColdFire?

ColdFire Instruction Set Architecture



Deletions from M68000:

- BCD instructions
- Divide instructions (optional)
- Rotate instructions
- Simplified fault model
  - » Single stack pointer
- Reduced support for .b & .w instrs
- Eliminated support for r-m-w instrs

Additions beyond M68000:

- x2 and x4 scale factors for index registers
- Longword Multiplies
- Extend Byte to Long Instruction
- trapf, trapf.w and trapf.l
- Vector Base Register (modulo-1M addr)
- BDM Instructions
- H/W Divide (5206e and V3 cores)

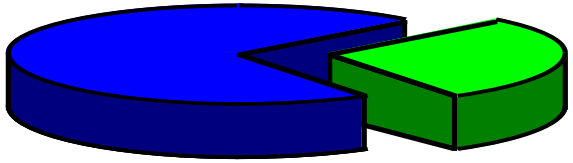
Includes:

- Full support for basic effective addressing modes
- Full support for move byte, word, and long operands
- Supervisor/user privilege modes

ColdFire: Variable Length RISC

- Reduced instruction set architecture

Total 68030 Instructions



Version 2 ColdFire Instructions (28%)

	MC68030	MCF5200
Instruction Mnemonics	175	93
Total Instructions[1]	3,145[2]	893
Longest Instr. Length (words)	11[2]	3
Exception Stack Frames	8	1

[1]Implemented Mnemonics x Addressing modes x Operand sizes

[2]Does not count co-processor instructions

68K/ColdFire Addressing Modes

Addressing Modes	Syntax
Register Direct Data Address	 Dn An
Register Indirect Address Address with Postincrement Address with Predecrement Address with Displacement	 (An) (An)+ –(An) (d16, An)
Address Register Indirect with Index 8-Bit Displacement	 (d_8, An, Xn)
Program Counter Indirect with Displacement	 (d_{16}, PC)
Program Counter Indirect with Index 8-Bit Displacement	 (d_8, PC, Xn)
Absolute Data Addressing Short Long	 (xxx).W (xxx).L
Immediate	#<xxx>

ColdFire Addressing Modes

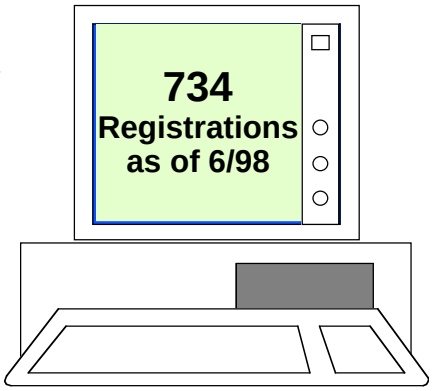
68K Only Extended Addressing Modes

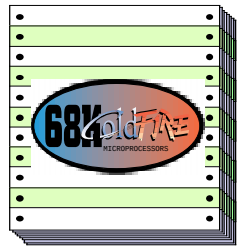
Addressing Modes	Syntax
Program Counter Indirect with Index Base Displacement	 (bd, PC, Xn)
Address Register Indirect with Index Base Displacement	 (bd, An, Xn)
Memory Indirect Postindexed Preindexed	 ([bd, An], Xn, od) ([bd, An, Xn], od)
Program Counter Memory Indiect Postindexed Preindexed	 ([bd, PC], Xn, od) ([bd, PC, Xn], od)

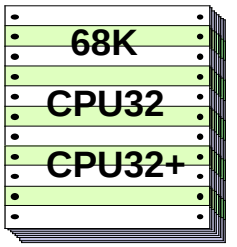
Converting from 68K to ColdFire

68K to ColdFire® Assembler Translator

- **MicroAPL PortASM/68K Software Promotion- Available for FREE since November 1997**
  - **Automated tool will translate M680x0 Family, CPU32, and CPU32+ assembly source code to ColdFire® Family source code**
  - **Software will run on DOS/Windows 3.1, Windows95/WindowsNT, Solaris (SPARC) and SunOS(SPARC)**
  - **Features of tool:**
    - » Tool has capability to
      - – choose between optimization of code size or performance when doing translation
      - – choose between ColdFire® core versions with or without the MAC and/or divide unit.
    - » Input formats of tool that customer can choose from are
      - – Diab Data 68K 'DAS' Assembler
      - – Microtec 'ASM68K' Assembler
      - – Motorola 'MASM68K' Assembler
      - – GNU 68K 'GAS' Assembler
    - » Output Formats that user can choose from are:
      - – Diab Data ColdFire Assembler
      - – Motorola Embedded Syntax
      - – GNU ColdFire Assembler
    - » 68K code that PortASM/68K can not readily convert will be flagged by the program and will recommend corrections
    - » Tool allows debug instructions to be inserted into code giving users the flexibility to use tools that take advantage of the ColdFire® debug module
  - **Tool Availability**
    - » Downloadable from WWW (http://www.mot.com/coldfire) for *FREE*
    - » Available on CD-ROM for *FREE*
  - **Support Availability**
    - » *FREE* installation support
    - » Full support available from MicroAPL for less than $500/year



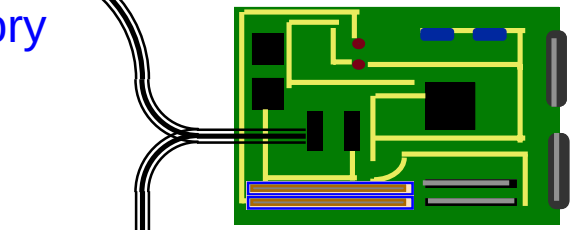




ColdFire Development Tools

ColdFire Debug Port

- Inexpensive Debug: Non-Real-Time-Debug
  - Provides serial control and visibility of CPU & memory
  - Enhanced version of 683xx Background Debug Mode (BDM)
  - Read / write CPU registers and memory
  - Pipeline control operations

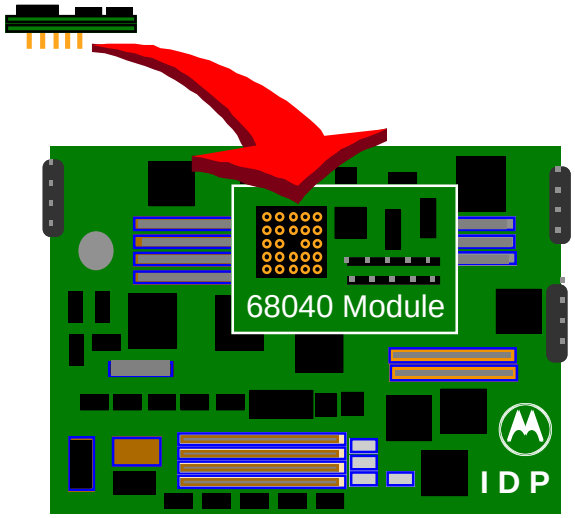


- Low Cost Emulation Capability: Real-Time-Debug
  - Least obtrusive to CPU performing time critical code
  - Hardware breakpoints: PC w/ mask, Address range & Data w/ mask
  - Trigger based on 1-2 levels of breakpoints
  - Can force infinite priority interrupt, make data visible, or force CPU halt
- Full Emulation Support: Real-time trace
  - Allows 100% code tracking with in-circuit emulator
  - PULSE instruction in ISA for easy signaling to emulator under S/W control

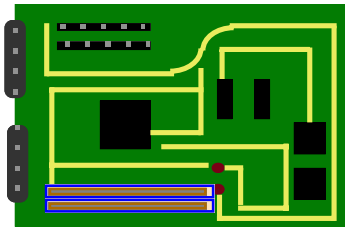
ColdFire Tool Summary

	Provider	Availability
COMPILERS	Diab Data	NOW
AND	Green Hills Software	NOW
	Lauterbach	NOW
SOURCE	Microtec	NOW (Beta)
DEBUGGERS	Software Development Systems	NOW
OTHER	Huntsville MIcrosystems	NOW
DEBUG TOOLS	P&E Microcomputer	NOW
RTOS	Accelerated Technology	NOW
	Embedded System Products	NOW
	Integrated Systems, Inc	NOW
	Precise Software	NOW
	Wind River Systems	NOW
EMULATORS	Embedded Support Tools (BDM and full ICE features)	NOW
	Microtek International	NOW (BDM)
	Noral Micrologics	NOW
	Yokogawa/Orion Instruments	NOW (Full 5202 ICE)
OTHER TOOLS	Applied Microsystems (NetROM and CodeTEST)	NOW
	MENTOR GRAPHICS (HW/SW CO-VERIFICATION)	NOW
LOGIC ANALYZER	Tektronix (disassembler)	NOW
EVALUATION BOARDS	M5102EVM and M5202EVM	NOW
	M5204AN and M5206AN, Arnewsh Inc.	NOW
	M5206EAN, Arnewsh Inc.	3Q98
	M5307AN, Arnewsh Inc.	NOW

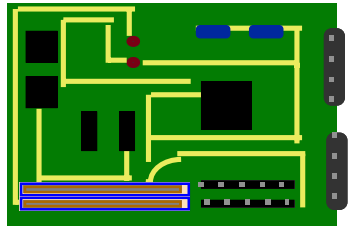
ColdFire 520x Evaluation Solutions



- **5202** -> 040 Adapter
  - Works in 040 IDP platform
  - Optional SRAM for 3-1-1-1 operation
  - ColdFire ROM monitor
  - BDM connector
  - Available NOW

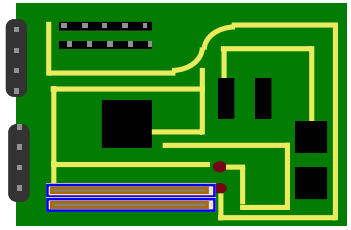


- **5204** Eval Board
- Order M5204AN
  - 10 baseT Ethernet
  - 256 KB SRAM (Expandable to 512 KB)
  - 256 KB FLASH (Expandable to 512 KB)
  - 8-, 16-bit bus
  - RS-232 port
  - BDM connector
  - ColdFire ROM mon
  - Avail NOW

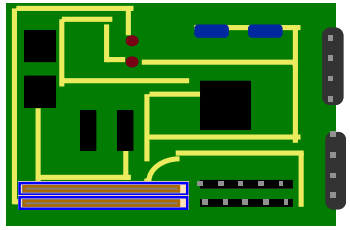


- **5206** Eval Board
- Order M5206AN
  - 10 baseT Ethernet
  - 1 MB DRAM (Expandable to 32 MB)
  - 256 KB FLASH (Expandable to 512 KB)
  - 8-, 16-, or 32-bit bus
  - RS-232 port
  - BDM connector
  - ColdFire ROM mon
  - Avail NOW

ColdFire 5206e & 5307 Evaluation Solutions



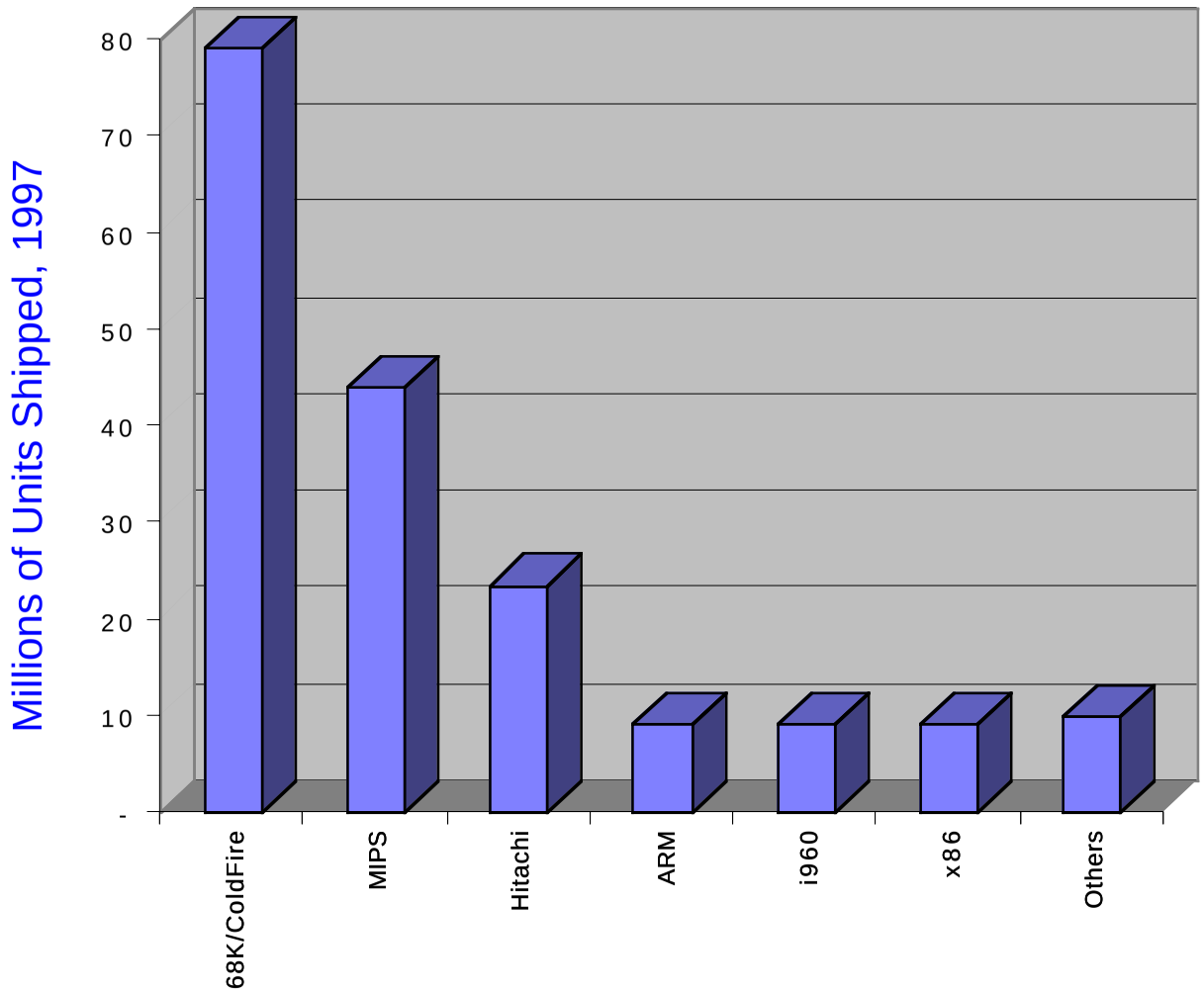
- **5206e** Eval Board
- Order M5206EAN
  - 10 baseT Ethernet
  - 4 MB DRAM (Expandable to 32 MB)
  - 512 KB FLASH
  - 8-, 16-, or 32-bit bus
  - RS-232 port
  - BDM connector
  - ColdFire ROM mon
  - Avail 3Q98



- **5307** Eval Board
- Order M5307PROMO (limited time)
- Order M5307AN (3Q98)
  - 10 baseT Ethernet
  - 8 MB SDRAM
  - 512 KB FLASH
  - 8-, 16-, or 32-bit bus
  - RS-232 port
  - BDM connector
  - ColdFire ROM mon
  - Avail NOW

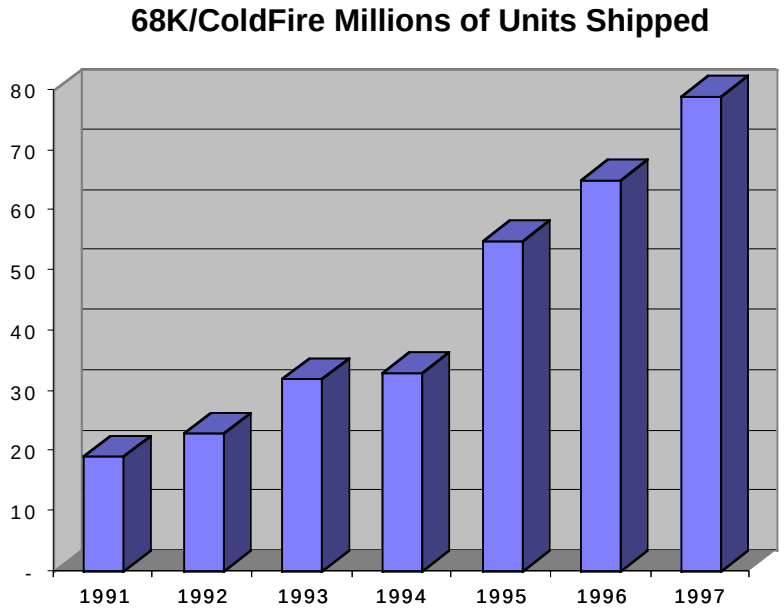
ColdFire Market Share and Benchmark Analysis

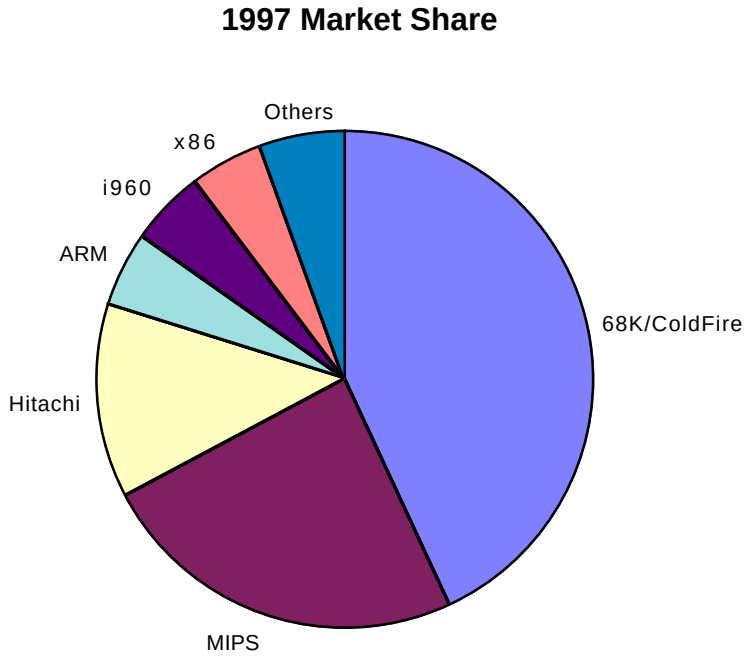
32-Bit Embedded Microprocessor Market



Source: MicroDesign Resources, 1998

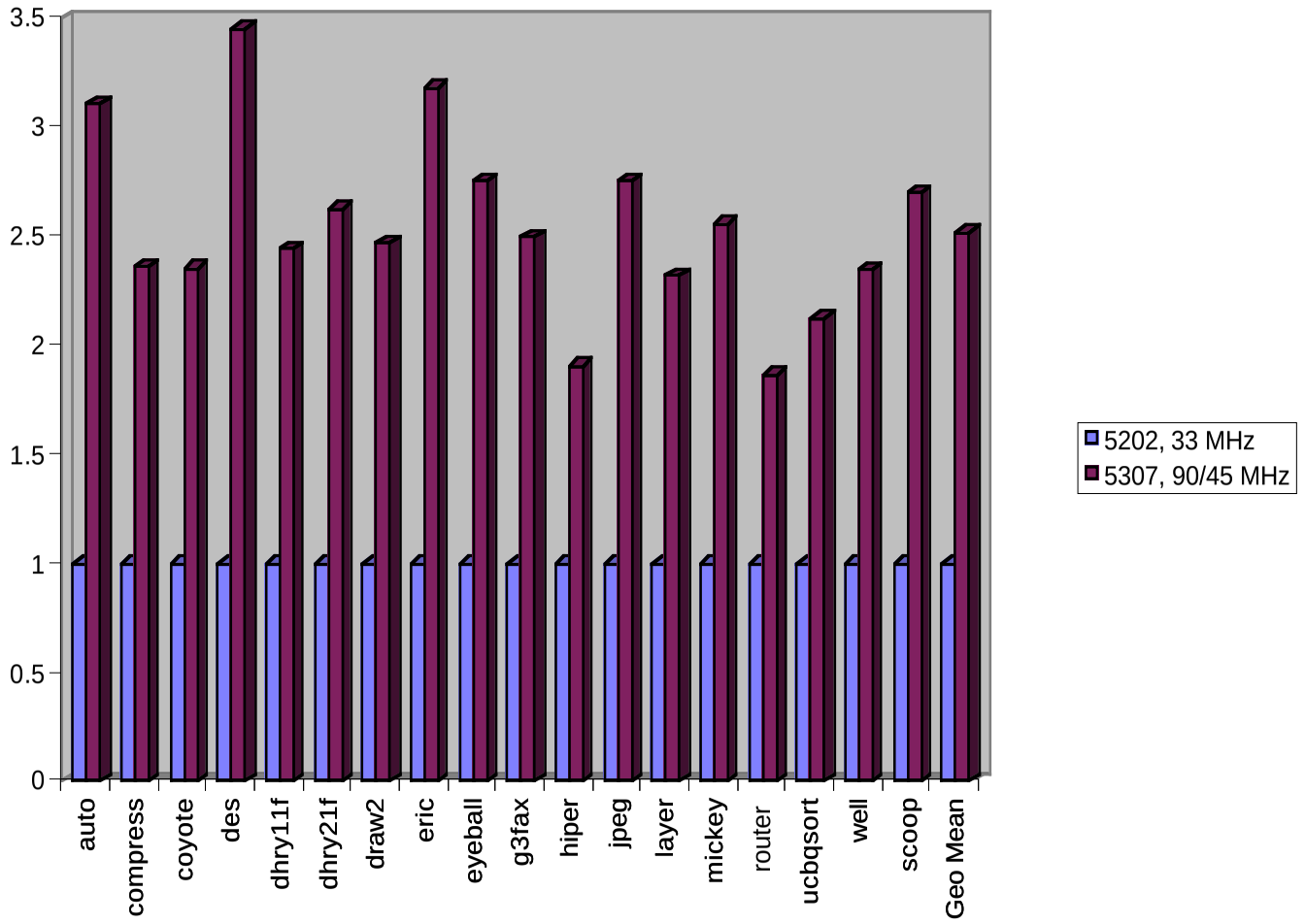
68K/ColdFire: 32 Bit Embedded Leader





Source: Motorola, MicroDesign Resources

Benchmark Comparison



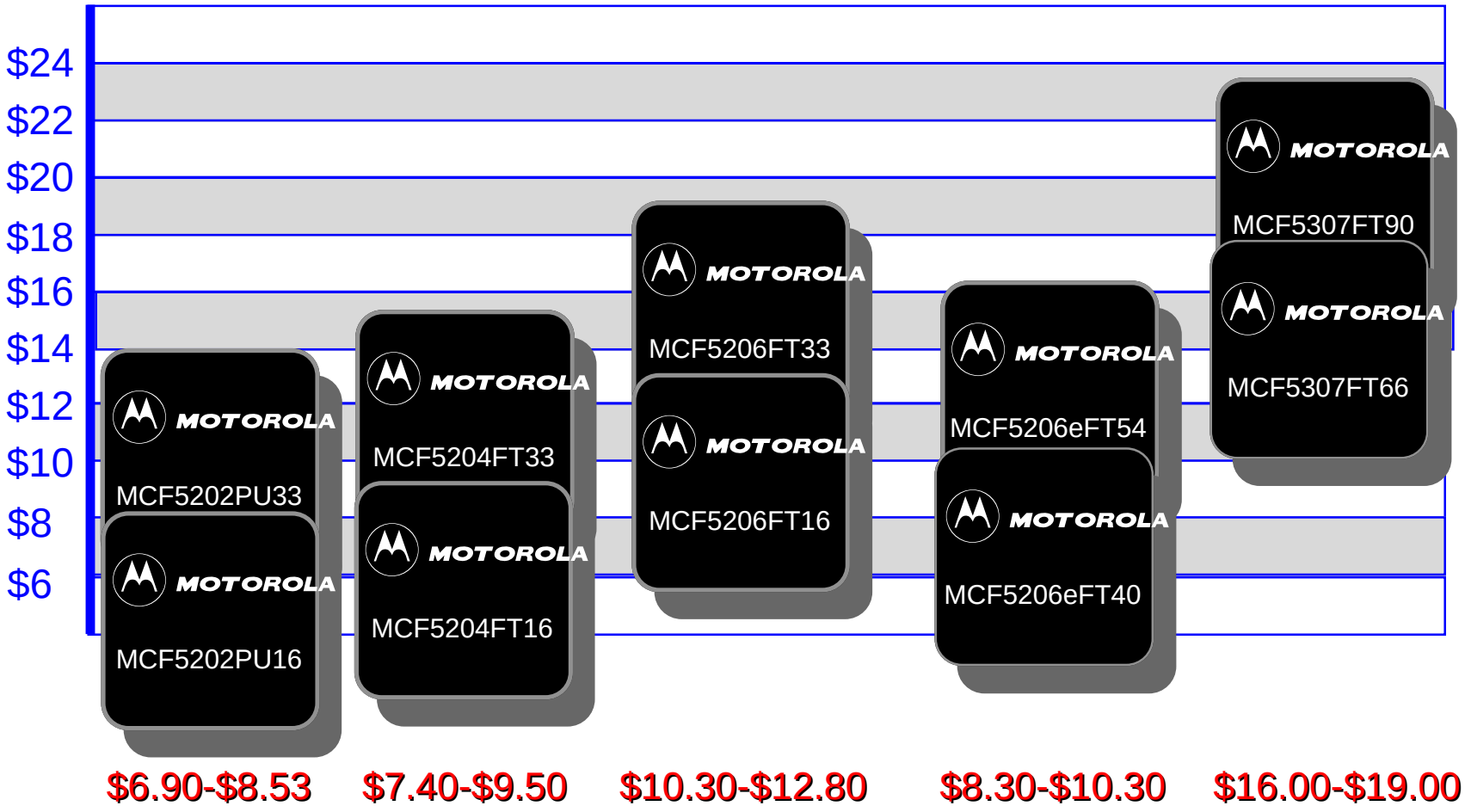
Dhrystone 2.1 MIPS:	**5202, 33 MHz**	**25**
Using the same external memory subsystem	**5307, 90/45 MHz**	**70**

ColdFire Target Applications & Design Wins

Examples of ColdFire Product Design Wins

- Robotics
- LAN Board
- Digital Loop Communication
- Fiber Channel
- Graphics Accelerator Card
- Traffic Control System
- Transportable Receiver
- Resource Processing Board
- Power Meter
- Handheld Scope
- DVD Player
- Tape Drive
- Testing Equipment
- PABX/Line Cards
- Automatic Bowling Scoring
- Cellular Base Station
- Digital PPC (multiple)
- Printer (multiple)
- FRAD
- Sports Simulator
- Office Computer
- Impact printer
- Advanced Motion Control
- Servo Board
- Music Synthesizer
- LAN System
- SCSI Interface
- Digital Copier
- DVD-RAM
- CEM Board
- Computer Projector
- Phone Systems
- Fabric Defect Detection
- Telecom E-1
- Motor Controller
- Medical Instrumentation
- ATM Machine
- Print Server
- VME Bus Application
- Router
- GPS System
- Intelligent I/O Processor
- Sound Board
- CCD Camera
- Video Server
- I/O Card
- IV Pump
- VF ISDN
- IDE Drive Controller
- Set-top Boxes (multiple)
- Telephone Repeaters
- Video Security System
- Telecommunications
- 10 Channel GPS Receiver
- Weight Scale
- User Interface System
- Ethernet Controller
- Hard Disk Drive
- Laser Beam Positioning Equip.
- Automotive Wheel Balancing Machine

1998, 10K Resale Prices



(approximated values)

68K/ColdFire Summary

ColdFire Family Features

- **Minimizes Product Memory Costs**
  - Variable-Length-RISC instruction set optimized for code density
  - Code requires substantially less memory than fixed length RISCs
  - Lower memory bandwidth required to support given level of performance
- **Low CPU Cost**
  - Small die for low cost: Ideal for advanced consumer products
  - Cost effective integration of memories, system modules, and peripherals
- **High Performance RISC-based Microarchitecture**
  - Simple instruction set
  - Single cycle execution of most instructions
  - Hardwired control
- **Full-Featured Debug Module**
  - Enhances time to market
  - Supports BDM, real-time trace and real-time debug capabilities
  - Configurations from standard MPUs to completely embedded designs
- **Easy migration from 68k products**
- **Complete Tools Solution**

68K/ColdFire Advantages over Competition

- ColdFire offers existing 68K customers an ease of transition to high performing VL RISC that no other competitor can provide!
- Upgrading C and Assembly code
  - » Customers who have C code merely need to recompile in order to transition to ColdFire; no extra work needed
  - » Most common 68K assembler commands port directly to ColdFire. Customers who want to use existing assembly code only need to emulate some instructions and addressing modes. Simply rewrite or use the MicroAPL code converter
- Other 32-bit offerings may tout better price & performance but
  - » provide poor integration (need external devices = more cost & power)
  - » have poor development tools and limited 3rd Party support
  - » Processor core may run slower to access external devices not integrated
- ColdFire offers:
  - » Performance: Ranging from 11 MIPS to 70 MIPS today, up to 300 MIPS in by year 2000
  - » Price: 32-bit embedded solutions from $7 to $19 (6/1/98)
  - » Integration on-chip peripherals such as UARTs, TIMERs, Parallel Ports, DRAM controllers, Chip Select controller, MAC, H/W Divide, DMA, & SRAM
  - » Development tools: On-chip debug module for low-cost emulation; software tools from a broad base of well-known third-party tool vendors

Questions and Answers

- I want more performance without rewriting code. How can I get that?
  - C/C++ users simply recompile with ColdFire® Compilers
  - Assembly users can convert their code with MicroAPL code converter
  - Most 68K Assembly directives port directly to ColdFire®
    - » Tool allows debug instructions to be inserted into code giving users the flexibility to use tools that take advantage of the ColdFire® debug module
- I am used to programming with 68K. Is ColdFire® difficult to learn?
  - No. Same programming model (D7-D0, A7-A0, CCR)
  - The designer sees little or no difference programming ColdFire®
- Does increased performance mean increased price?
  - No. Generally, ColdFire® devices cost much less than the competition and 68K devices while providing more integration with higher performance
- Where do I find the latest information on ColdFire® devices?
  - http://www.motorola.com/ColdFire/ for Motorola ColdFire information
  - http://www.motorola.com/ColdFire/ cf_cool.html for interesting ColdFire links
  - Additional information is found under “Product Info” for each device. This includes code examples, manual addenda, errata, etc
- I need technical support on ColdFire® devices. Who do I contact?
  - CFCSUPT1@email.sps.mot.com
  - 1-800-521-6274