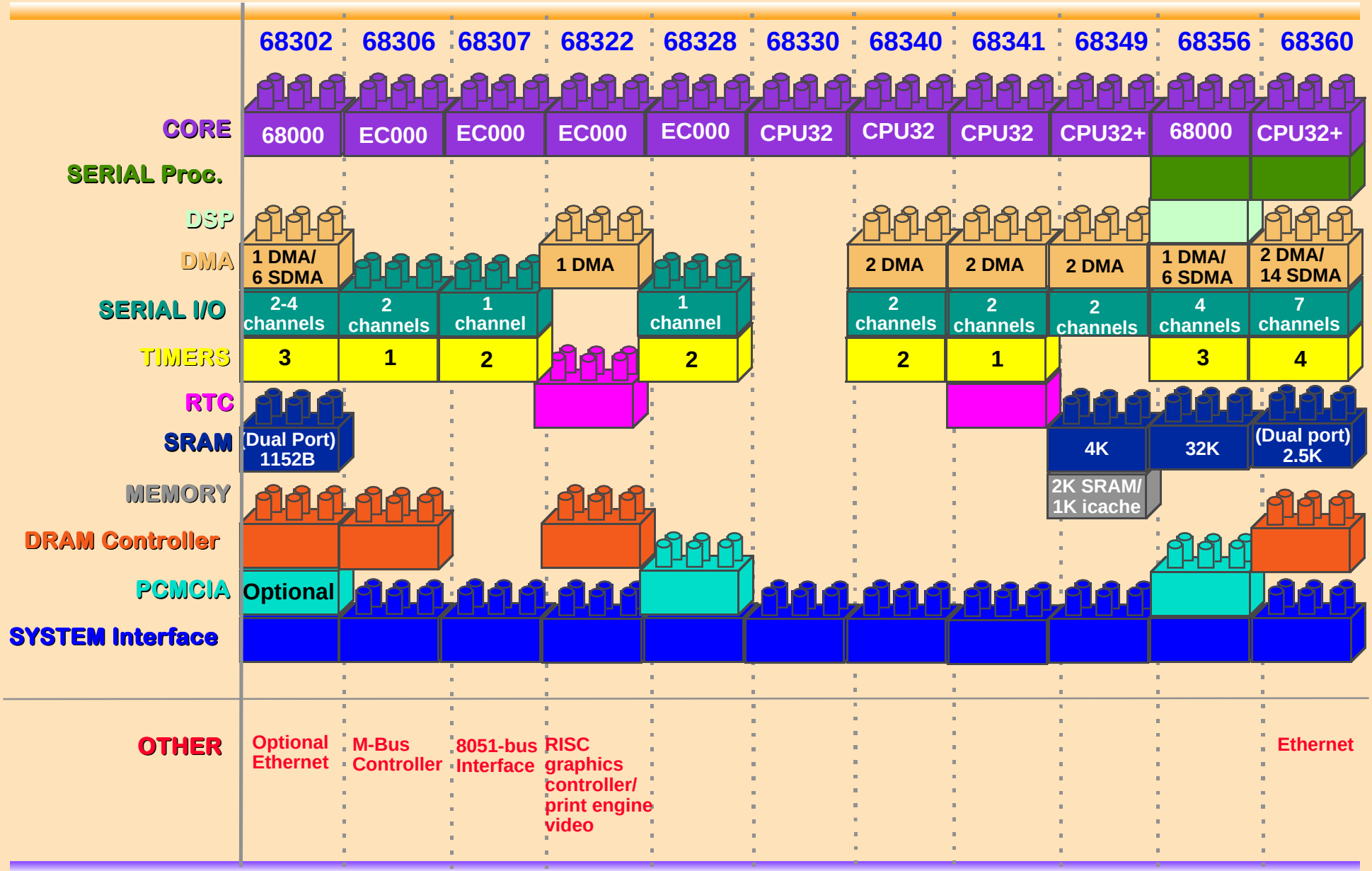
68300 Family Presentation

ISD Embedded Systems Products

1997

68300 Family: At a Glance



MOTOROLA
Semiconductor Products Sector

68300 Family Core Processors

The 68300 Family Devices contain a variety of cores especially designed to interface with Motorola's integrated modules:

- **EC000 Core Processor**
- **CPU32 Core Processor**
- **CPU32+ Core Processor**

EC000 Core: Features

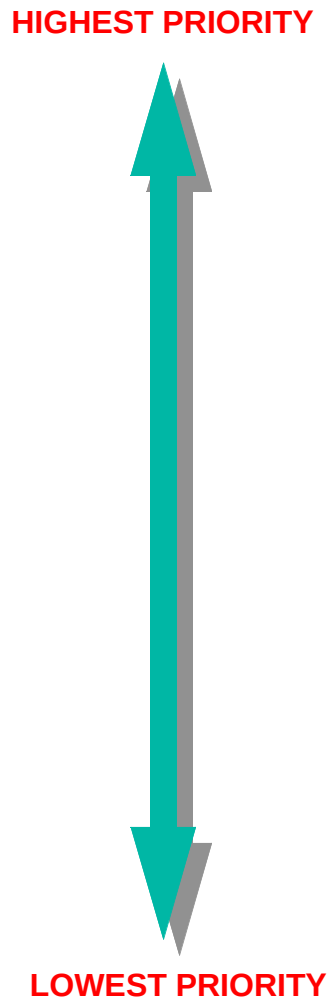
- EC000 internal architecture allows for 32-bit performance
  - 32-bit address bus & 16-bit data bus
  - Eight 32-bit address registers
  - Eight 32-bit data registers
- Features create flexibility of use
  - Supports 56 Instructions & 14 addressing modes!
  - User/Supervisor privileges
  - Support of several data types
    - **Bit**
    - **BCD**
    - **Byte, word, longword integer**
  - Three processing modes: Normal, Exception, & Halt
  - Capability of handling numerous exception types
- 2.4 MIPS @ 16.67 MHz
- 16, 20 Mhz

EC000: Features

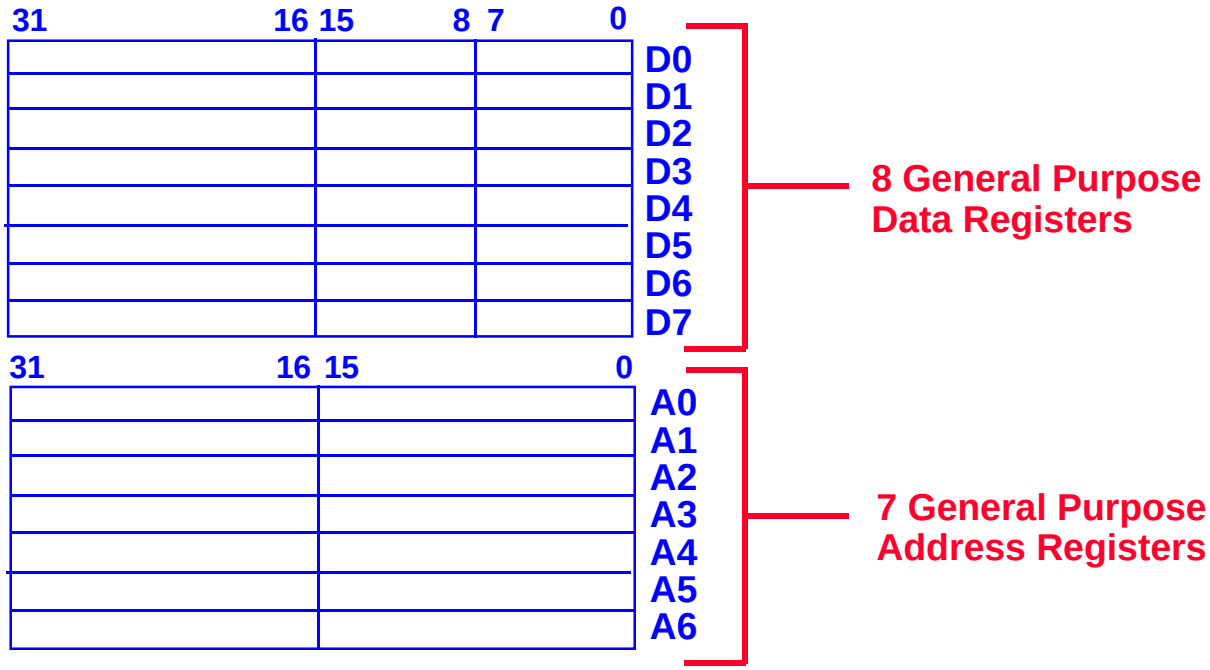
- 68000 Development Support:
  - Trace on Instruction Execution
    - » Supports change of flow trace
  - Breakpoint Instruction
  - Unimplemented Instruction Execution
    - » F-line & A-line instructions

EC000 Core: Exception Processing

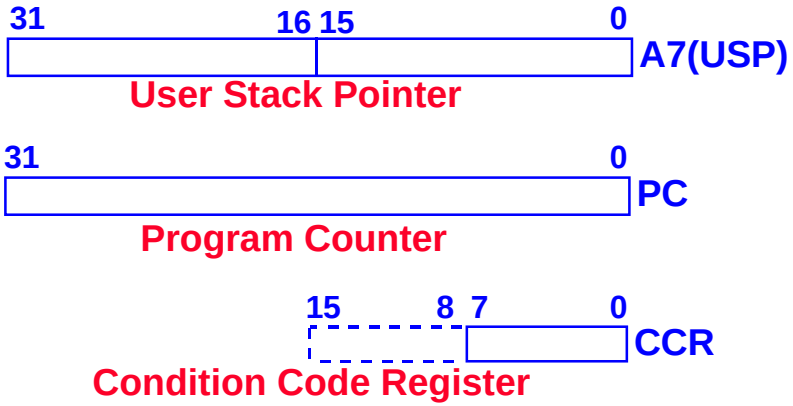
- Exceptions taken by EC000:
  - Group 0:
    - Reset
    - Address Error
    - Bus Error
  - Group 1:
    - Trace
    - Uninitialized or Spurious Interrupt
    - Illegal or Unimplemented Instruction
    - Privilege Violation
  - Group 2:
    - TRAP
    - TRAPV-- Overflow
    - CHK-- Out of bounds
    - DIV--Divide by zero



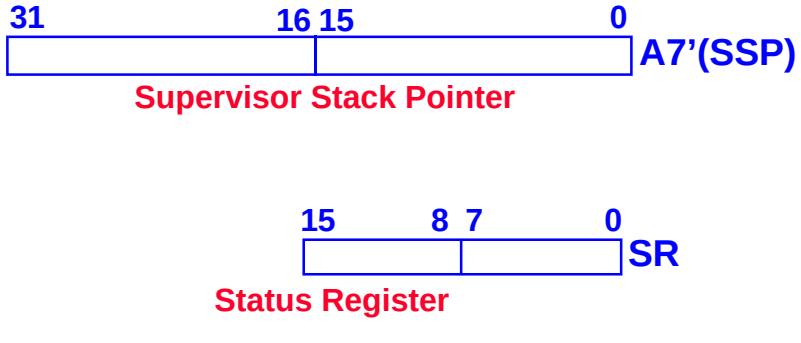
EC000 Core: Programming Model



User Programming Model Supplement



Supervisor Programming Model Supplement



EC000 Core: Addressing Modes

DATA REGISTER DIRECT

ADDRESS REGISTER DIRECT

PC RELATIVE WITH
- Displacement
- Index (8 bit displacement)
- Index (base displacement)

ADDRESS REGISTER INDIRECT WITH (optional)
- Postincrement
- Predecrement
- Displacement
- Index (8 bit displacement)
- Index (base displacement)

ABSOLUTE LONG

ABSOLUTE SHORT

IMMEDIATE

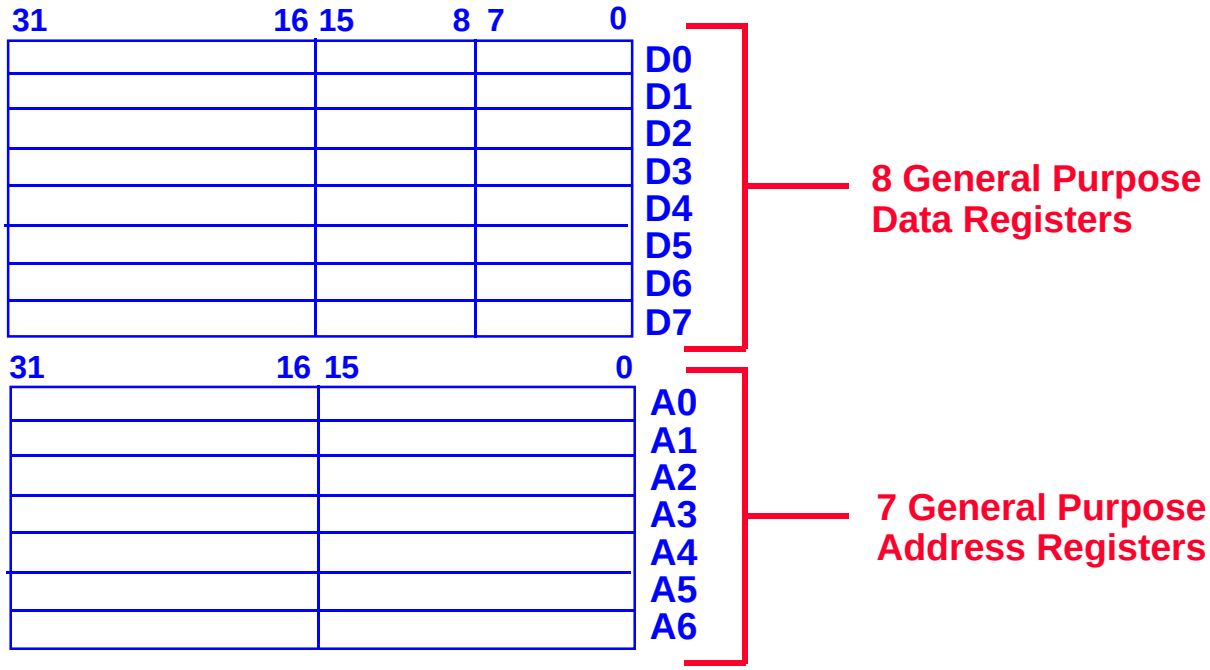
CPU32: Features

- Based on 68000 core
  - Source code & binary code compatible w/ 68000
- Contains features of 68010 & 68020
  - Supports many 68010/020 instructions
- Designed to interface with Intermodule Bus (IMB)
- Internal 32-bit address bus, 16-bit data bus
- Virtual Memory Implemented for use w/ disk drives
  - Page Fault Exception processing implemented
- Loop Mode Supported
  - DBcc instruction
- Fast multiply, divide, & shift instructions
- Relocatable Vector Table
  - 64 processor-defined vectors; 192 user-defined

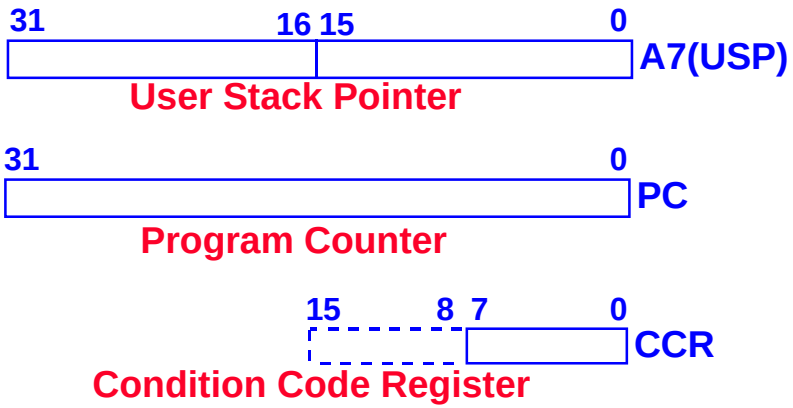
CPU32: Features

- Additional addressing modes compared to 68000
- Special embedded application instructions
  - **TBL: Table Lookup & Interpolate**
  - **LPSTOP: Low Power Stop**
  - **BGND: Background Debug Mode**
- Processing States:
  - **Normal**
  - **Exception**
  - **Halted**
  - **Background**
- Development Support
  - **Trace capability**
  - **Unimplemented Instruction Emulation**
  - **Debug Module**
  - **Deterministic Opcode Tracking**
  - **Breakpoint capability**

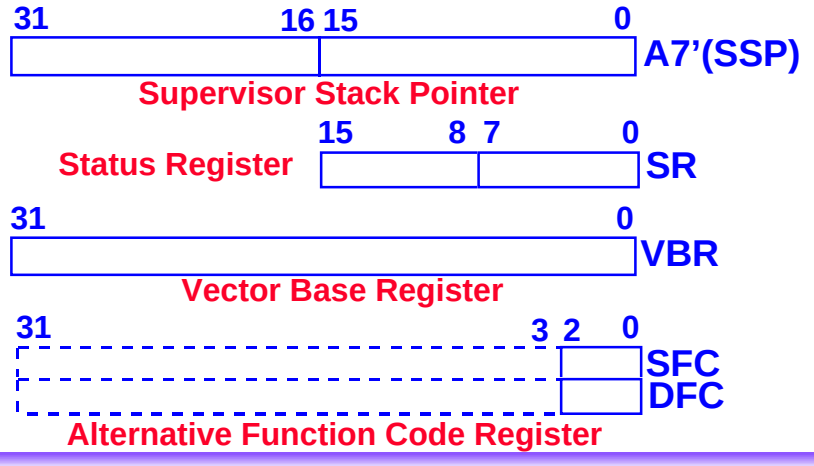
CPU32: Programming Model



User Programming Model Supplement



Supervisor Programming Model Supplement



CPU32: Addressing Modes

DATA REGISTER DIRECT

ADDRESS REGISTER DIRECT

PC RELATIVE **WITH**

- Displacement
- Index (8 bit displacement)
- Index (base displacement)

ADDRESS REGISTER INDIRECT **WITH** (optional)

- Postincrement
- Predecrement
- Displacement
- Index (8 bit displacement)
- Index (base displacement)

ABSOLUTE LONG

ABSOLUTE SHORT

IMMEDIATE

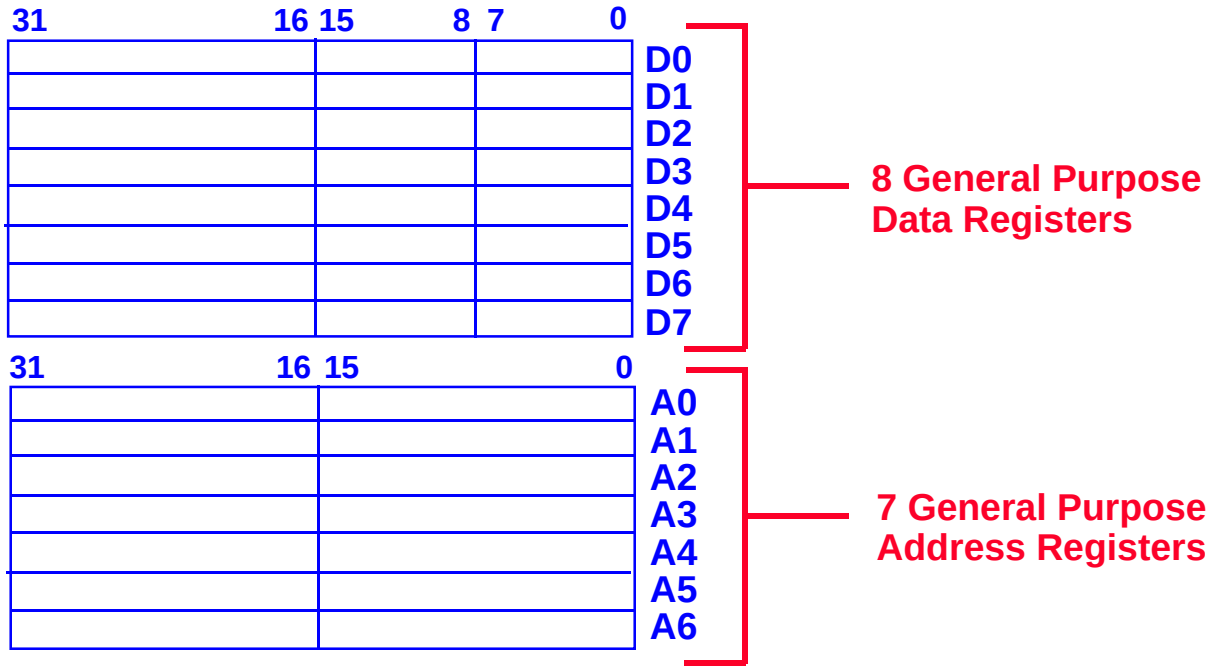
CPU32+: Features

- Based on 68000 core
  - **Source code & binary code compatible w/ 68000**
- Contains features of 68010 & 68020
  - **Supports many 68010/020 instructions**
- Internal 32-bit address bus, 32-bit data bus
- Designed to interface with the 68300 Intermodule Bus (IMB)
- Connected directly to Configurable Instruction Cache for fast, dedicated memory access
- Longword access in one bus cycle
- Support of byte-misaligned operands

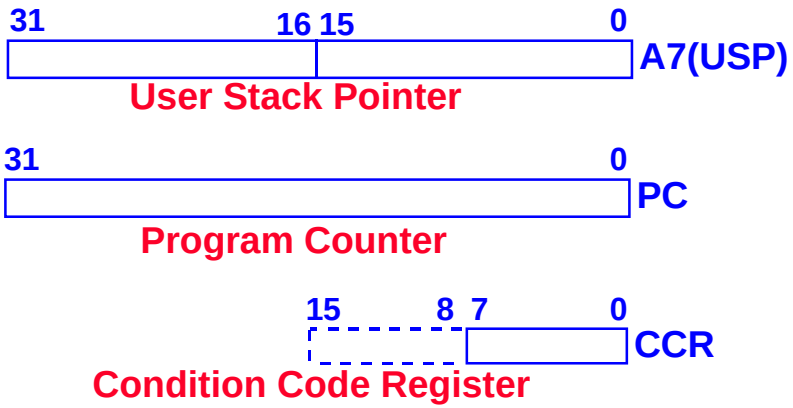
CPU32+: Features

- Supports low power modes:
  - HCMOS technology provides low power during normal operation
  - LPSTOP mode
- Virtual Memory Implemented for use w/ disk drives
  - **Page Fault Exception processing implemented**
- Loop Mode Supported
  - **DBcc instruction**
- Fast multiply, divide, & shift instructions
- Relocatable Vector Table
  - **64 processor-defined vectors; 192 user-defined**

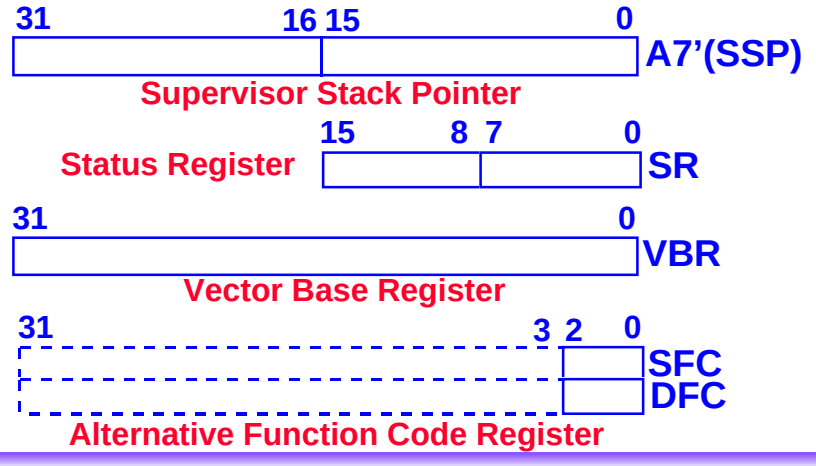
CPU32+: Programming Model



User Programming Model Supplement



Supervisor Programming Model Supplement



CPU32+: Addressing Modes

DATA REGISTER DIRECT

ADDRESS REGISTER DIRECT

PC RELATIVE **WITH**

- Displacement
- Index (8 bit displacement)
- Index (base displacement)

ADDRESS REGISTER INDIRECT **WITH** (optional)

- Postincrement
- Predecrement
- Displacement
- Index (8 bit displacement)
- Index (base displacement)

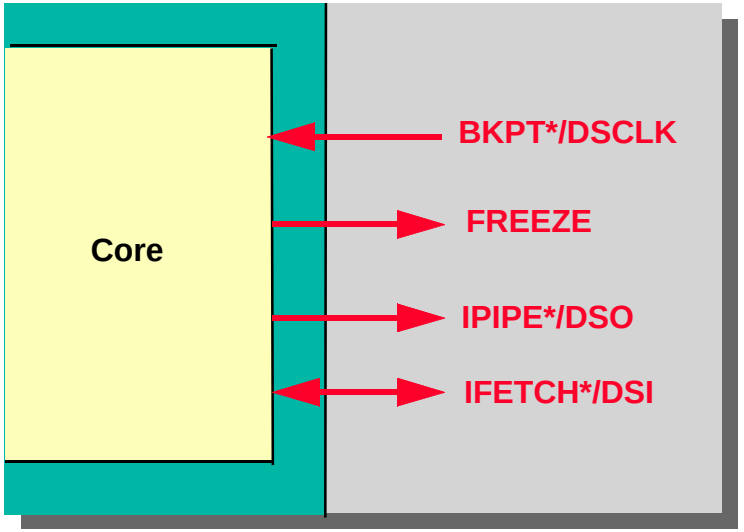
ABSOLUTE LONG

ABSOLUTE SHORT

IMMEDIATE

CPU32, CPU32+: Development Support

- Includes 68000 Development Support:
  - Trace on Instruction Execution
    - » Supports change of flow trace
  - Breakpoint Instruction
  - Unimplemented Instruction Execution
    - » F-line & A-line instructions
- Additional Debug Support:
  - Background Debug Mode (BDM)
    - » Eliminates need for in-circuit emulator
    - » Allows viewing & alteration of registers
    - » Test features can be initiated here
  - Deterministic Opcode Tracking
    - » IFETCH* identifies instruction fetches & pipeline flushes
    - » IPIPE* flags instruction pipeline advancement
  - Hardware breakpoint
    - » Initiates breakpoint exception processing or BDM



CPU32, CPU32+: Background Debug Mode

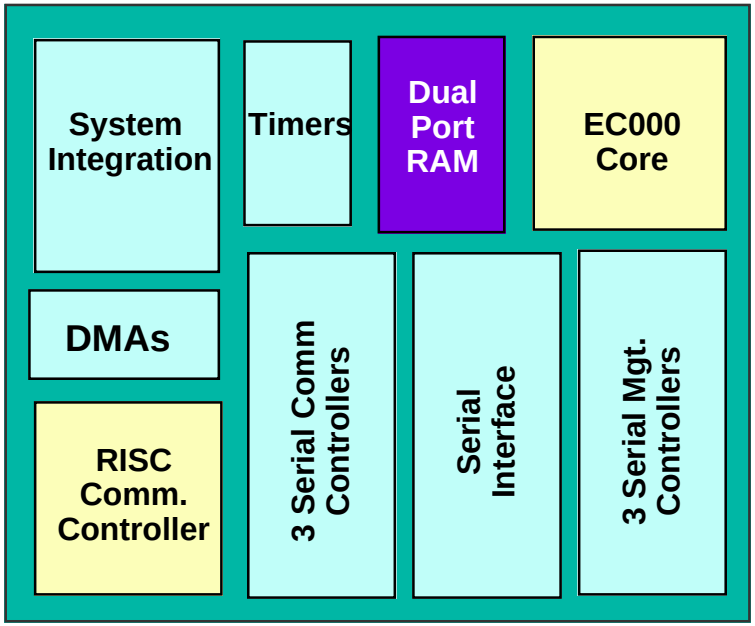
- BDM allows development system to send debug commands through SPI-type interface
  - BDM can be entered through:
    - » Generated Breakpoints
    - » Internal Peripheral Breakpoints
    - » Special Background Instruction (BGND)
    - » Error Exception Conditions (ie. Double Bus Fault)
  - BDM commands allow thorough debug capability:

BDM COMMANDS

• RAREG/RDREG-	Read selected data or address register	• DUMP-	Dump memory block. Used with READ command
• WAREG/WDREG-	Write to selected data or address register	• FILL-	Fill memory block. Used with WRITE command
• RSREG-	Read a control register	• GO-	Resume execution at return PC
• WSREG-	Write to a control register	• CALL-	Executes user patch code
• READ-	Read a memory location	• RST-	Asserts RESET
• WRITE-	Write to a memory location	• NOP-	No operation/ null command

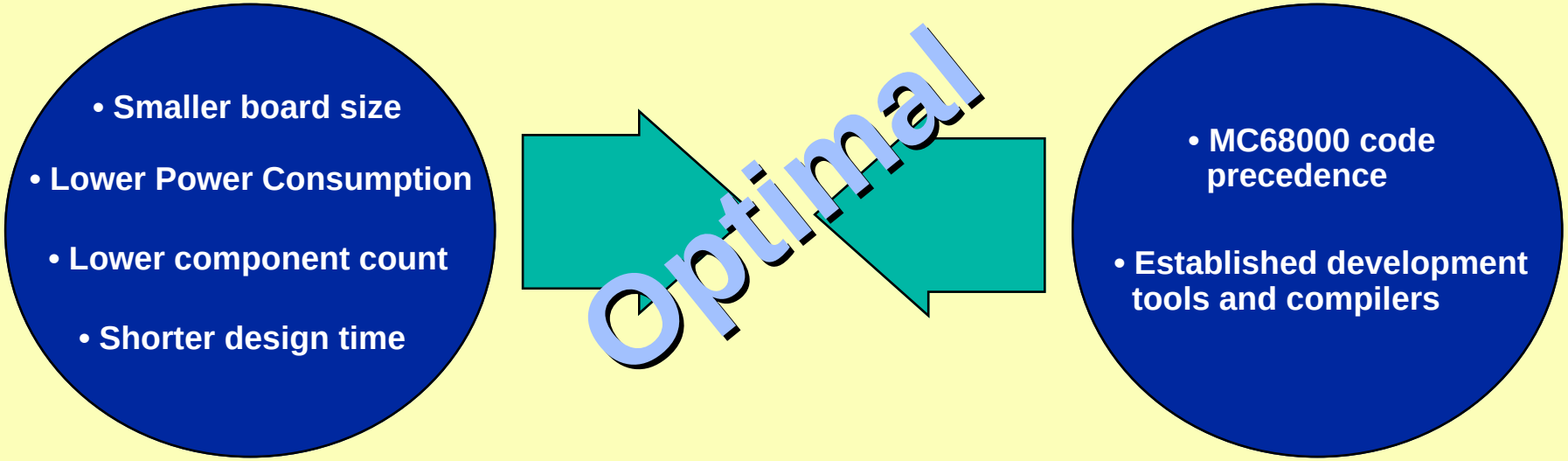
68302: Features

- HCMOS MC68000 Core Processor
- System Integration
  - DMA
  - Interrupt Controller
  - Parallel I/O
  - 1152 Byte Dual-Port RAM
  - Three Timers
  - Four Programmable Chip Selects
  - On-Chip Clock Generator
- RISC Communications Processor
- Communications Integration
  - 3 Full-Duplex Serial Communication Controllers
  - Six DMA channels
  - 2 Serial Management Controllers



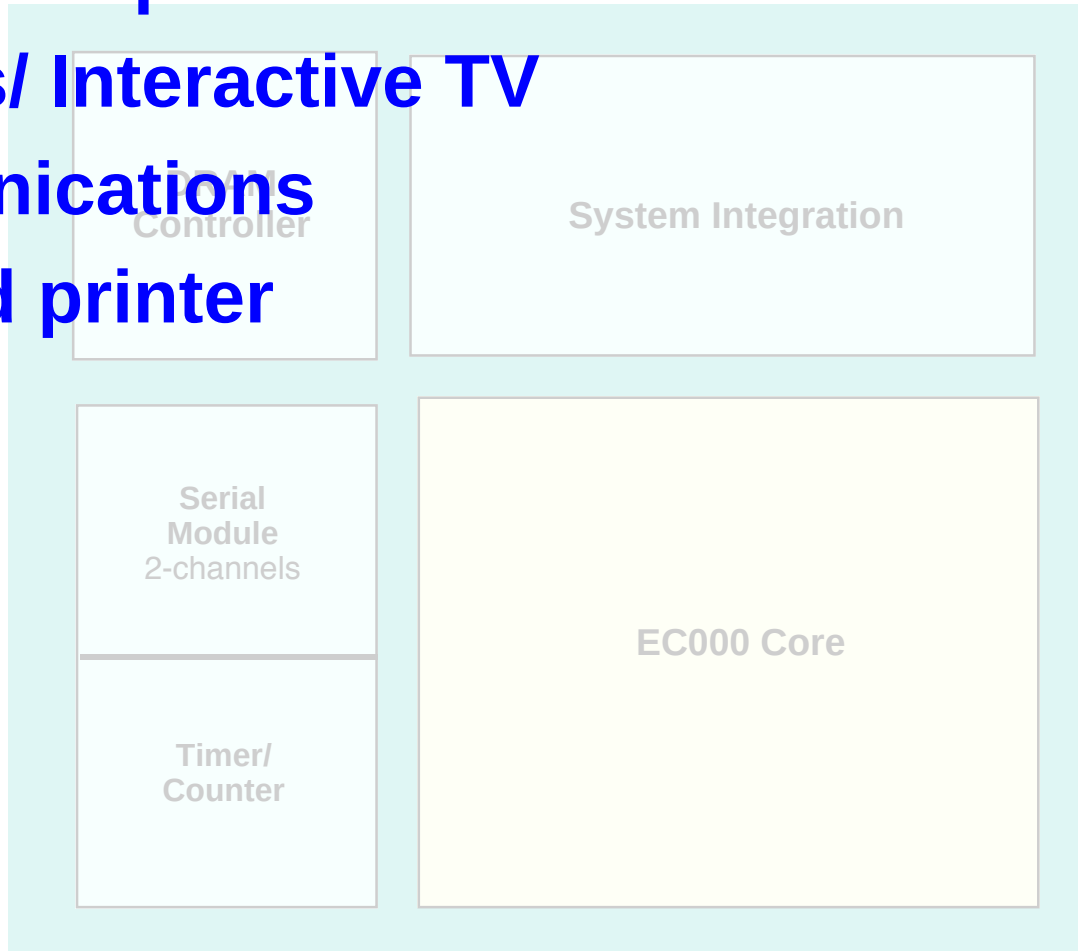
68306 ADVANTAGE

THE 68306 MERGES THE ADVANTAGES OF INTEGRATION AND LEGACY TO CREATE AN OPTIMAL SOLUTION



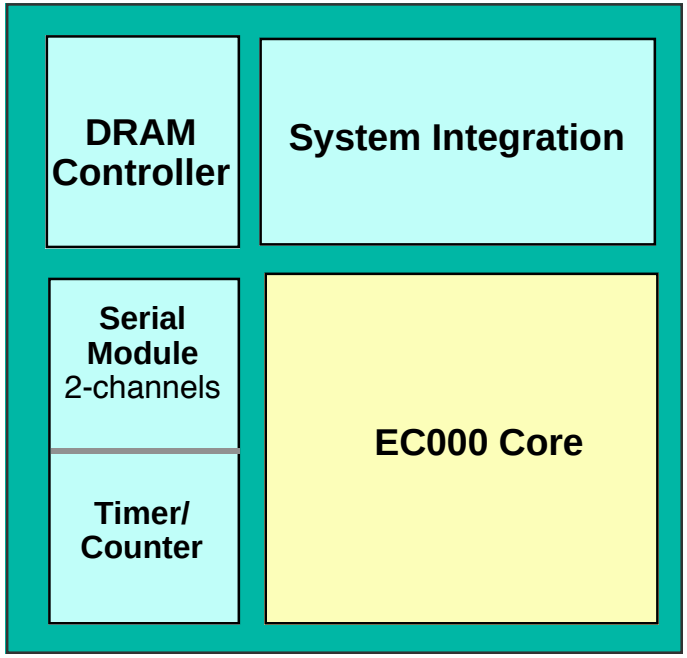
68306: Applications

- General Purpose Embedded Control
- Set-tops/ Interactive TV
- Communications
- Low-end printer
- GPS



68306: Features

- EC000 Core
- 2 Serial Channels
- DRAM Controller
- System Integration
  - 8 Chip Selects
  - 16 Parallel I/O Lines
  - Programmable Interrupt Controller
  - Clock
  - Watchdog Timer
  - JTAG Port
- 24 Address lines, 16 Data lines
- 16 MHz @ 5V
- Packages
  - 132 QFP and 144 TQFP
- Status:
  - MC Status

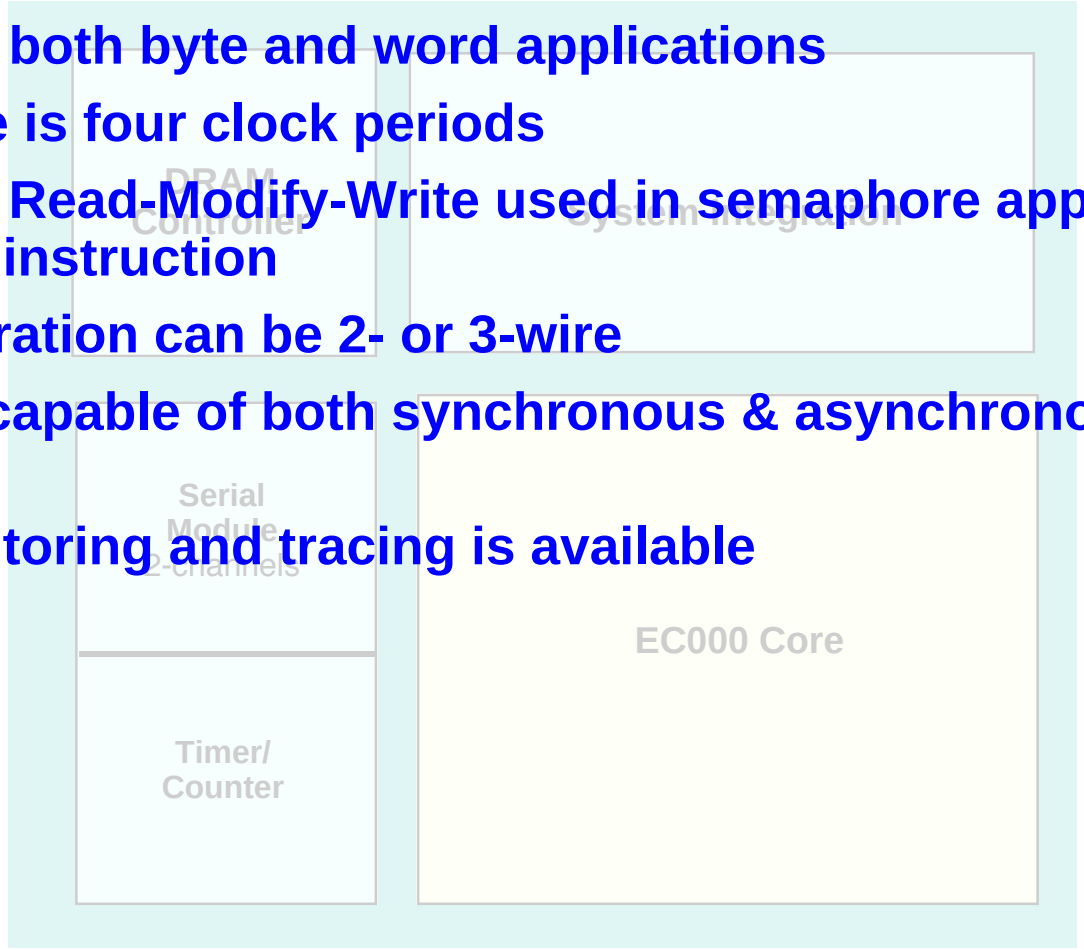


68306: Performance

- 2.7 MIPS @ 16.67 Mhz
- 0.525W power dissipation @ 16.67 Mhz @ 5.25 V

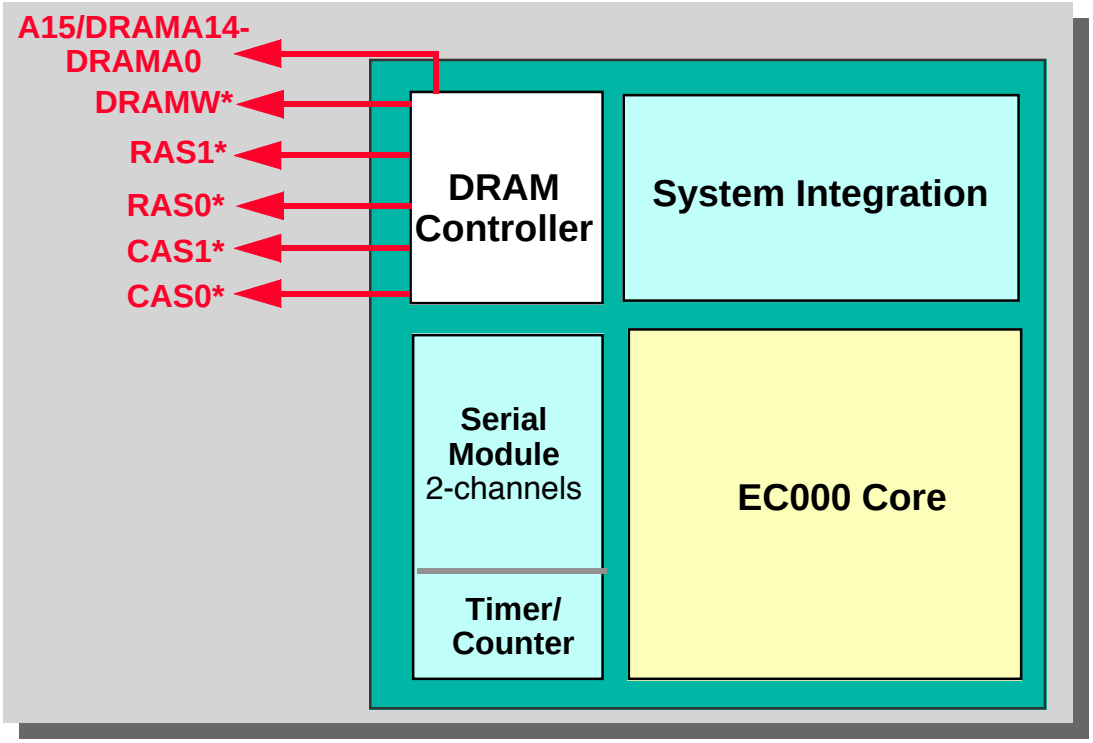
68306: Bus Operation

- 24 Address lines & 16 Data lines
- Supports both byte and word applications
- Bus cycle is four clock periods
- Supports Read-Modify-Write used in semaphore applications with TAS instruction
- Bus arbitration can be 2- or 3-wire
- 68306 is capable of both synchronous & asynchronous bus operation
- Bus monitoring and tracing is available



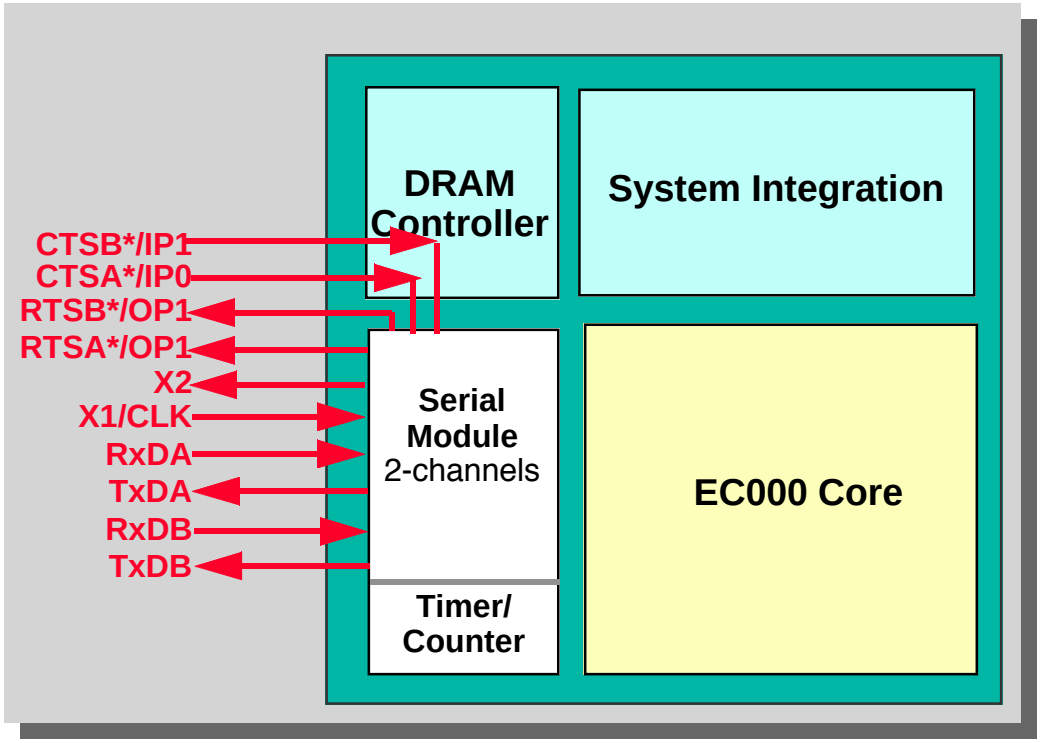
68306: DRAM Controller Module

- Supports up to 64 Mbyte of DRAM
- Programmable refresh timer with CAS* before RAS* refresh
- Zero wait state using 80-ns DRAM; one-wait state using up to 120-ns DRAM
- Refresh request programmable from every 16 to every 4096 EXTAL periods. Programmable in 16 EXTAL periods.
- Supports refresh during reset, except when there is an alternate bus master
- 4 clock accesses to memory
- 15 DRAM addresses lines are multiplexed with system address lines



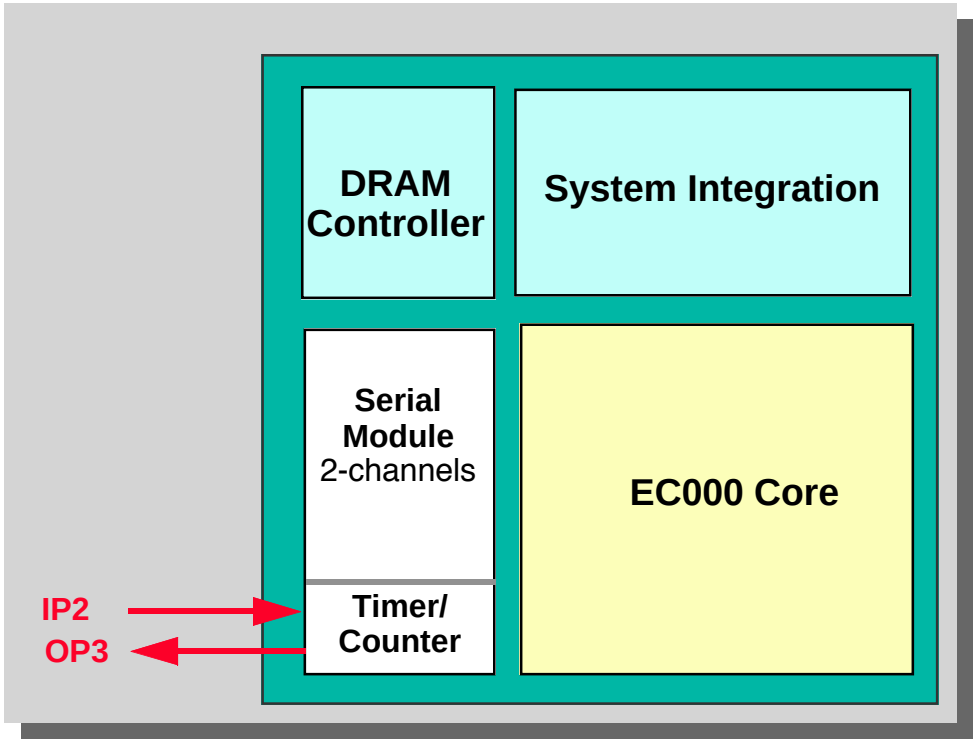
68306: Serial Module

- Full Duplex Asynchronous/Synchronous Receiver/Transmitter
- Quadruple-buffered receiver, double buffered transmitter
- Compatible with MC68681
- Flexible baud rate generator
  - Logic for each receiver & transmitter
  - 18 possible fixed rates-- from 50 to 38.4 Kbaud
- Programmable data format
- Automatic wake up mode for multi-drop applications
- Full modem support
- Autovectoring capability
- Error/Break Detection
- Various looping modes supported
  - Automatic echo
  - Local loopback
  - Remote loopback



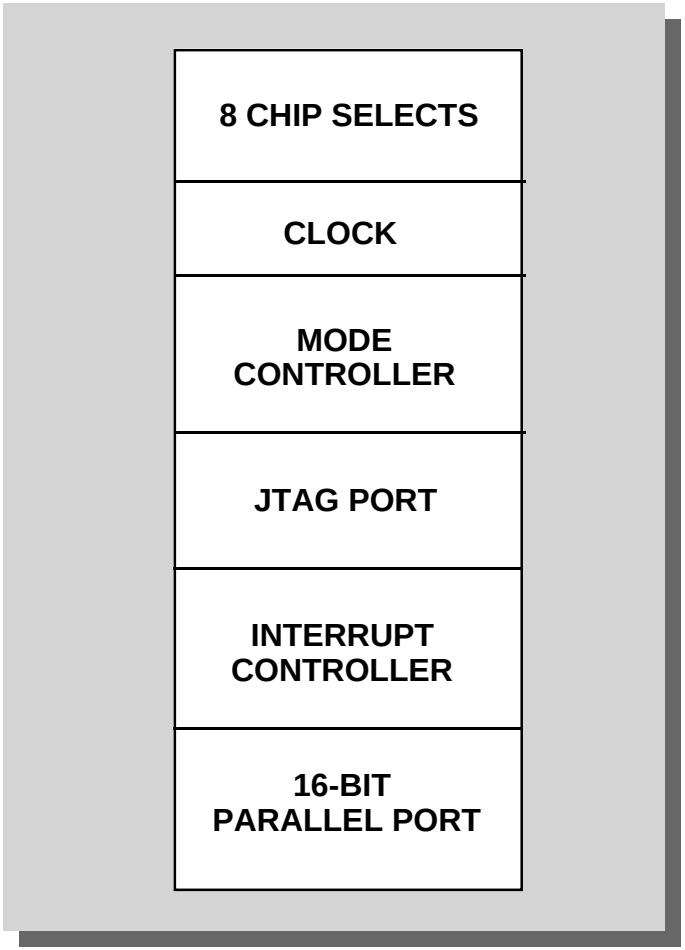
68306: Counter/Timer Module

- 16-bit Programmable Counter/Timer
- Multiple clock source inputs
- Timer/Counter Features
  - Uses Clock Source For Serial Module
  - Periodic Interrupt Generator
  - Square Wave Generator
  - System Stopwatch
  - Real-Time Single Interrupt Generator
  - Device Watchdog
- Counter May Generate Interrupt Request
- Timer Can Generate Interrupt Request



68306: System Integration

- Seven programmable interrupts
- Eight programmable chip selects
  - Handshaking & timing signals support up to 950 ns access times
  - Programmable wait state insertion supported
- 16 Parallel Input/Output Signals
  - Programmable on a bit-by-bit basis
- Clock
- Bus Watchdog Timer
- JTAG
  - IEEE 1149.1 compliant



68306: FAQs

- In the least significant word of the chip-select configuration register in the SIM, what function do the the CSFCx bits (bits 14, 13, 10, & 9) have?
  - The CSFCx bits designate how the function code pins will be encoded for a given chip select. For example, CSFC6 will drive 110 on the FCx pins; CSFC2 will drive 010 on the FCx pins.
- When writing a byte to 16-bit memory, how can I prevent the byte being replicated on both the high & low bytes of the data bus?
  - By connecting the LDS* & UDS* signals to the appropriate memory bytes, users doing a byte write will ensure that only the proper half of the data bus is selected
- Since the data book indicates that DRAM control registers are indeterminate after power-up, will there be a conflict with DRAM & boot ROM at this point?
  - No, since CS0* acts as a global chip select at reset. It is asserted for any memory access after reset to prevent this conflict until the other chip selects are initialized.

68307 ADVANTAGE

MULTIPLE BUS FUNCTIONALITY & LOW POWER MANAGEMENT GIVE 68307 THE ADVANTAGE IN BATTERY-POWERED APPLICATIONS

- 68000 BUS
- 8051-COMPATIBLE BUS
- I²C COMPATIBLE BUS[1]

+

- STATIC CORE DESIGN
- LOW POWER SLEEP LOGIC
- VARIABLE CLOCK SPEED

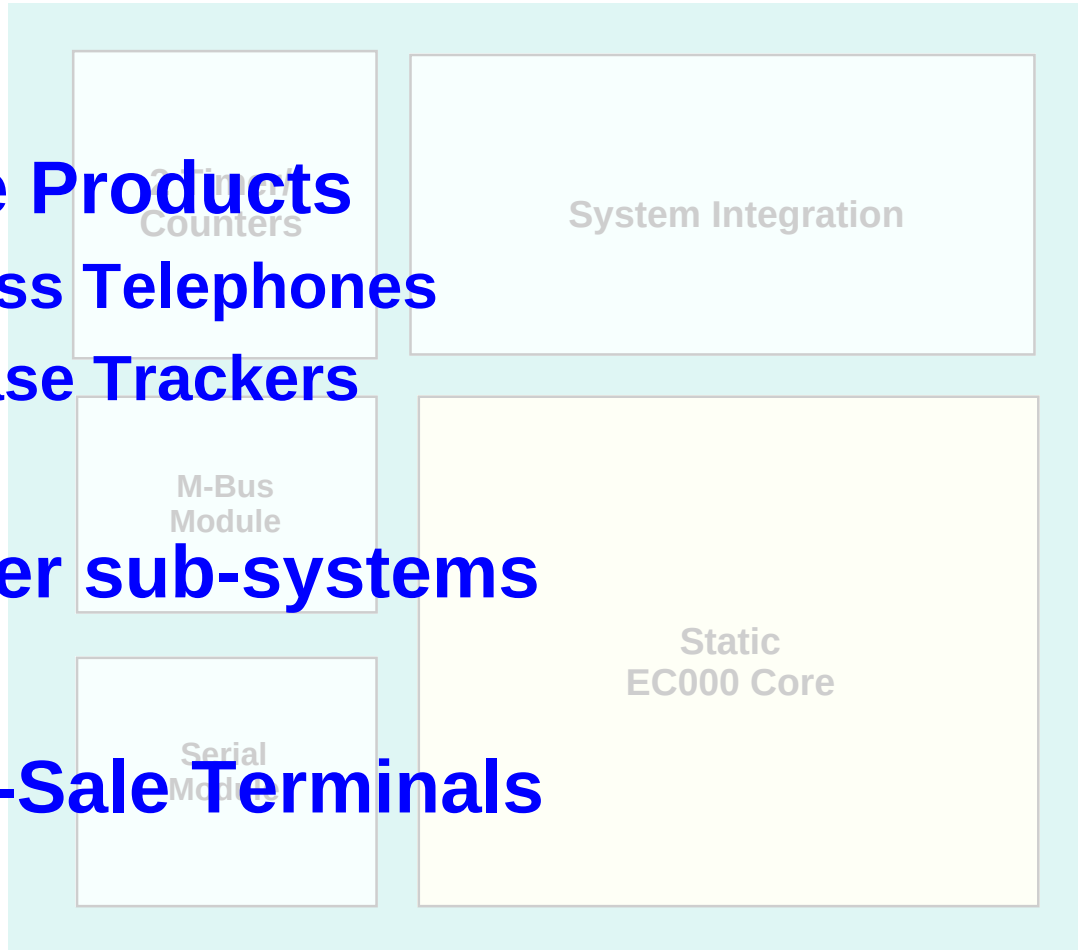
=

LOW POWER INTEGRATED SOLUTION

[1] I²C Bus is a proprietary Philips interface bus

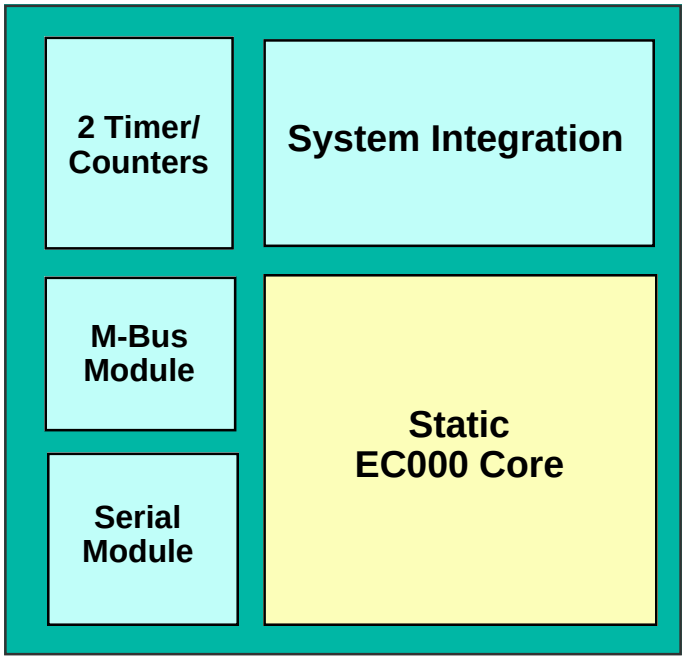
68307: Applications

- Embedded Control
- Portable Products
  - Cordless Telephones
  - Database Trackers
- Computer sub-systems
- Point-of-Sale Terminals



68307: Features

- Static EC000 Core
- External M68000 Bus Interface with dynamic sizing capability
- External 8051-Compatible Bus Interface
- Variety of Power Saving Operations
- M-Bus Module for fast bi-directional transfers
- UART compatible with MC68681
- Two 16-bit General Purpose Timer/Counters
- System Integration Module (SIM) which eliminates usual interface logic
- Processed in .8 µ HCMOS technology
- Offered in 3.3V and 5V
- Extended temperature devices are available
- Speeds: 8, 16 MHz
- Packages: 100-lead PQFP, 100-lead thin QFP
- Status: XC

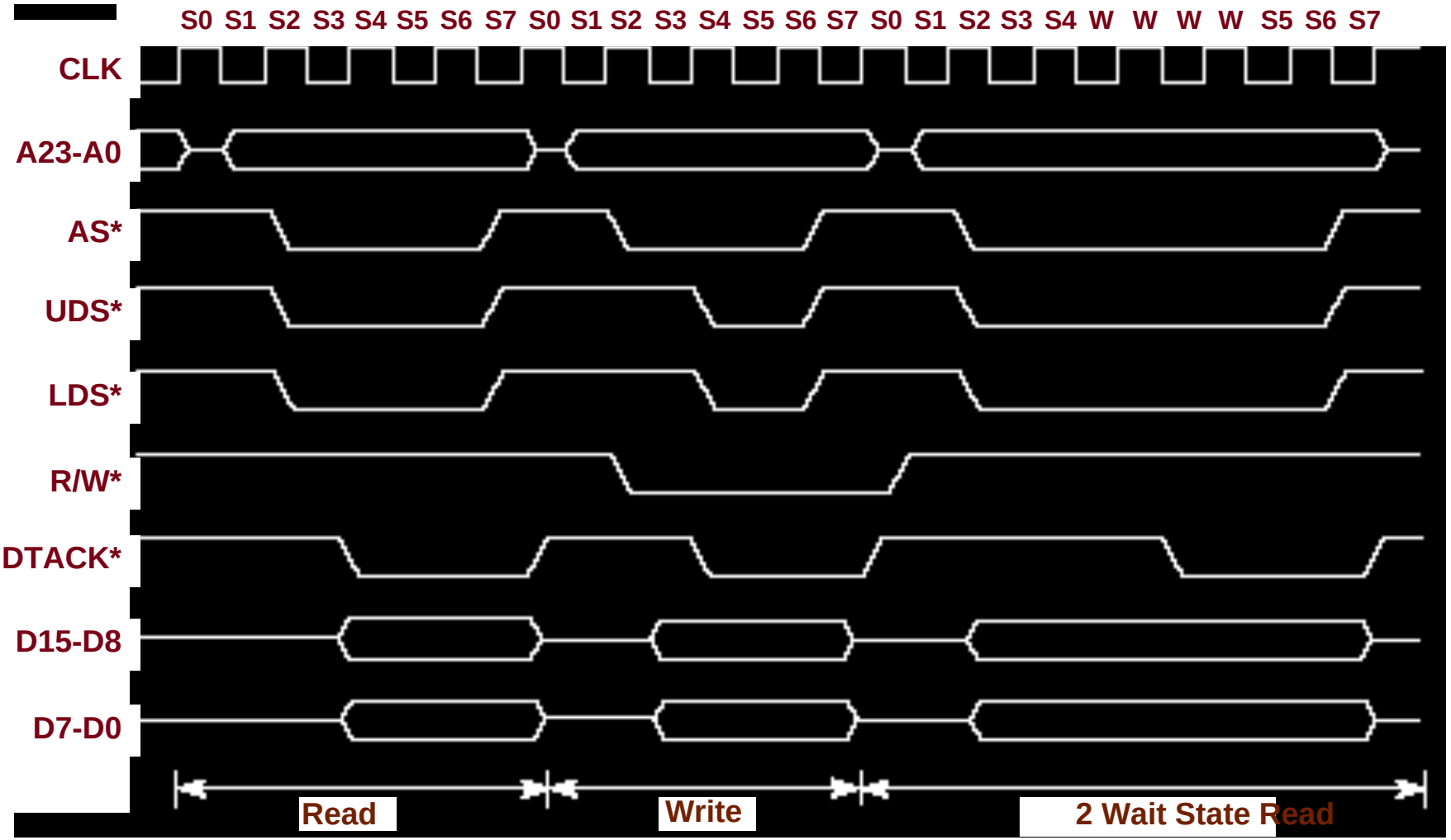


68307: Bus Operations

- External Bus contains 24 address lines, 16 data lines
- Bus Interface features:
  - Option of using M68000 Bus or the 8051-Compatible Bus
  - Dynamic sizing-- ease of accessing both 8- and 16- bit wide memory contiguously
  - Support for multi-processing environments w/ Read-Modify-Write
  - Elimination of external logic:
    - » 8051-Compatible bus interface to ASICs
    - » Internal bus arbitration logic
  - Option of synchronous or asynchronous operation depending on timing requirements needed
- 4 clock cycle bus transfers
- Bus logic is designed to handle exception operations such as bus error, retry, halt, double bus fault, and reset

68307: Bus Operations

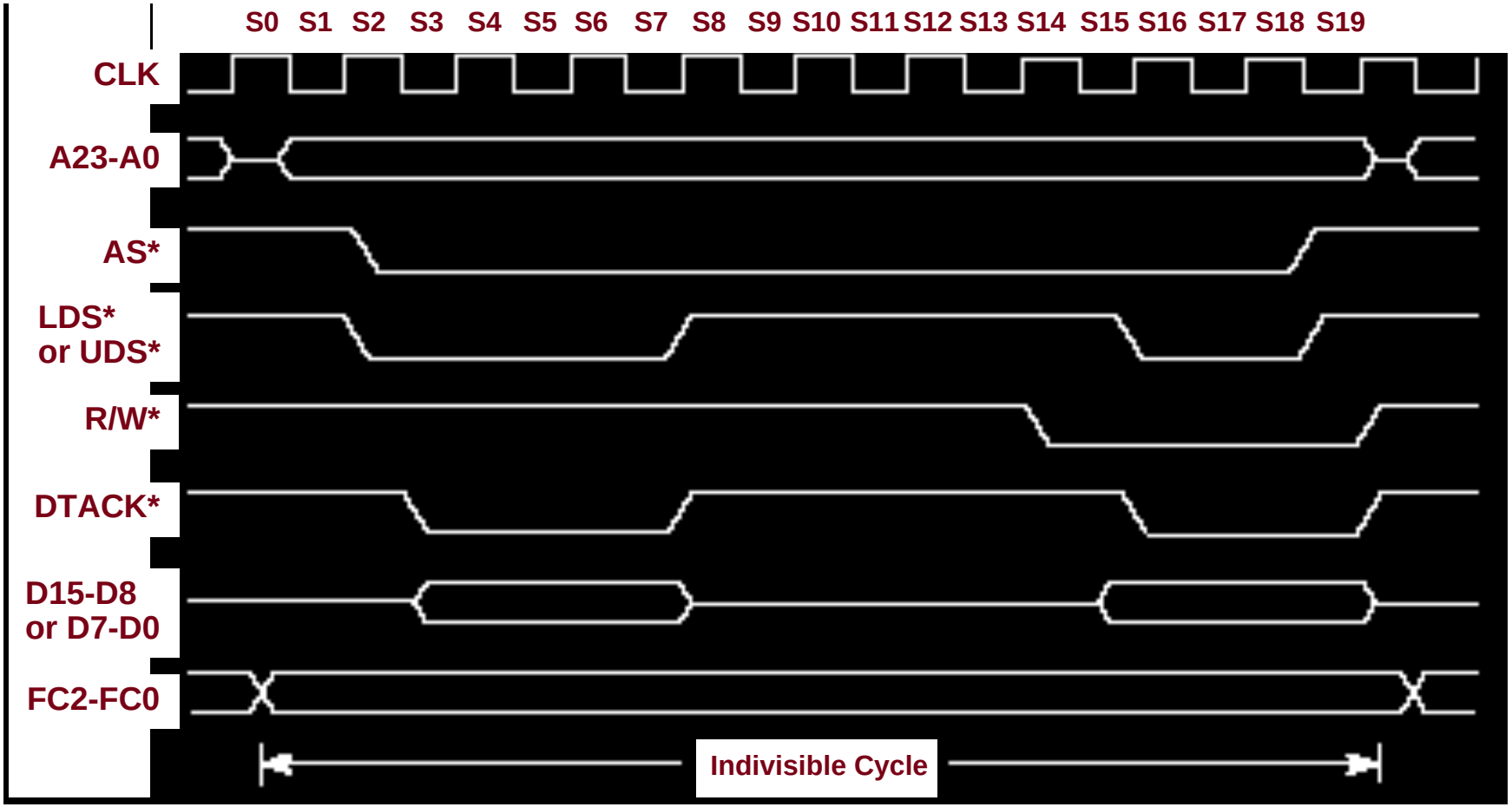
Typical Bus transfers take 4 clock cycles. If chip selects are used, the user can program DTACK* to be internally generated with up to six wait states



Read & Write Cycle Timing Diagram (16-Bit Bus)

68307: Bus Operations

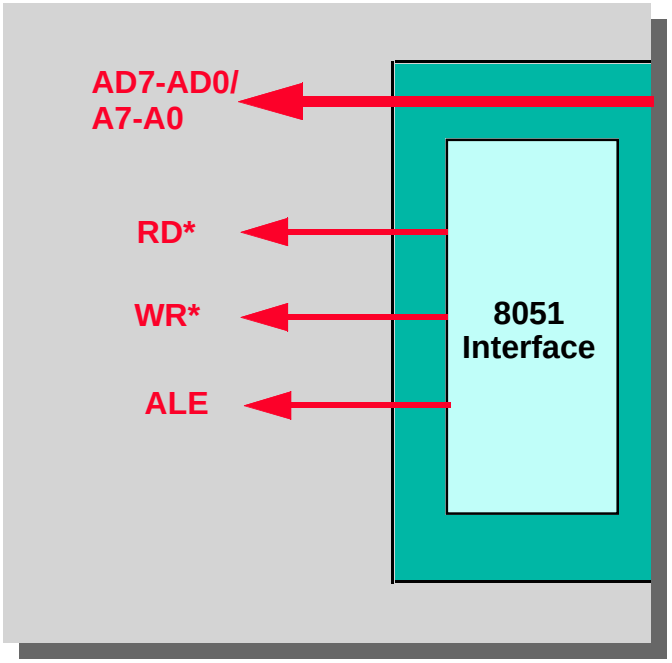
A Read-Modify-Write cycle is initiated through the TAS instruction. During this cycle, AS* remains asserted through the read and the write cycle.



Read-Modify-Write Cycle Timing

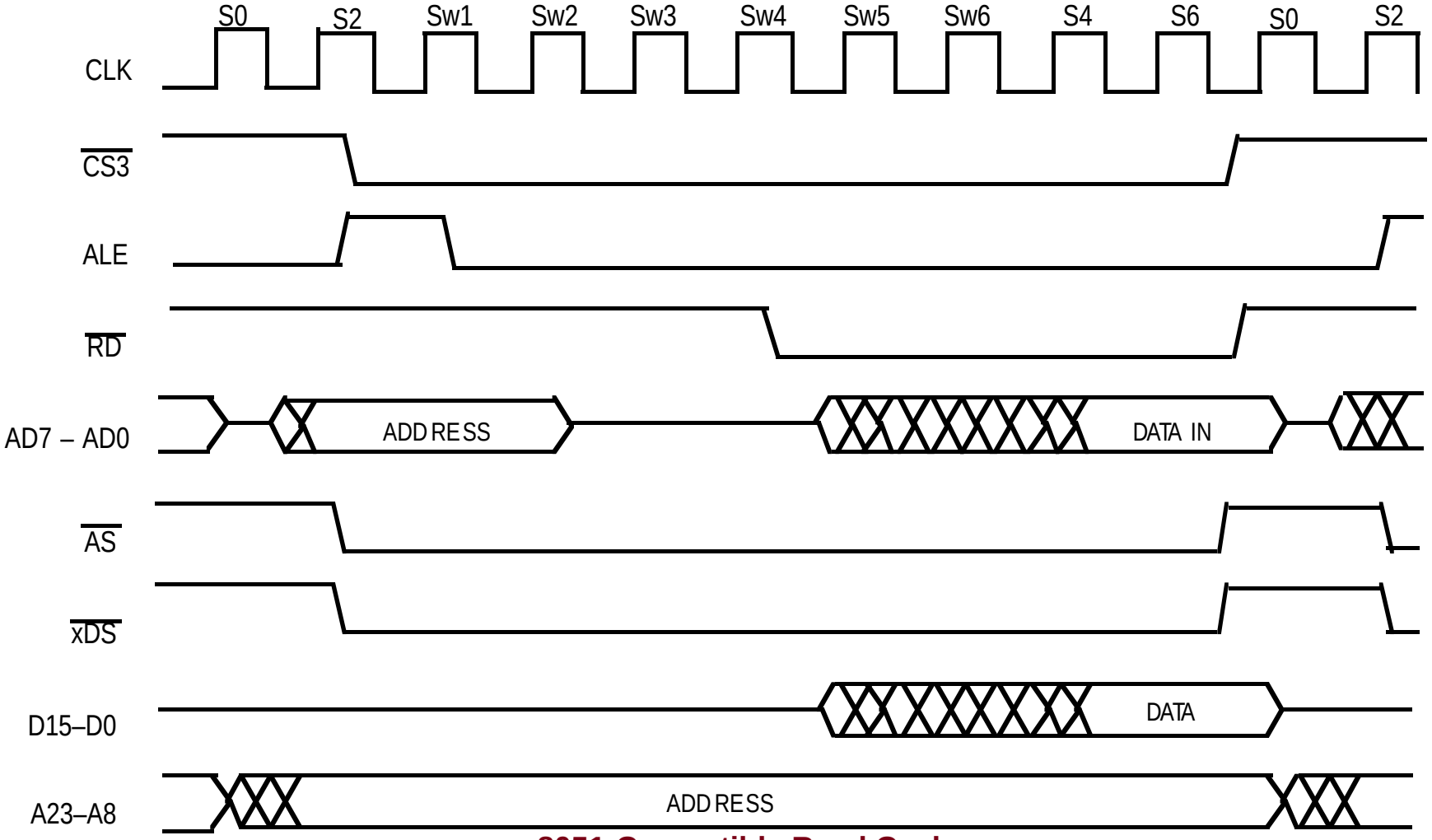
68307: 8051-Compatible Bus

- The 8051-Compatible Bus is useful for ASIC interfacing where pin-count minimization is important
  - Eight multiplexed AD lines serve as a bi-directional bus for the ASIC
  - The 8051-bus control signals include RD*, WR*, and ALE
  - CS3* can be programmed by the user to select 8051 memory range



68307: Bus Operations

During an 8051-compatible bus cycle, only the multiplexed address & data lines, the higher order address bus, and control signals CS3*, ALE, RD*, WR* are used. The M68000 control signals remain asserted indicating the underlying M68000 cycle.



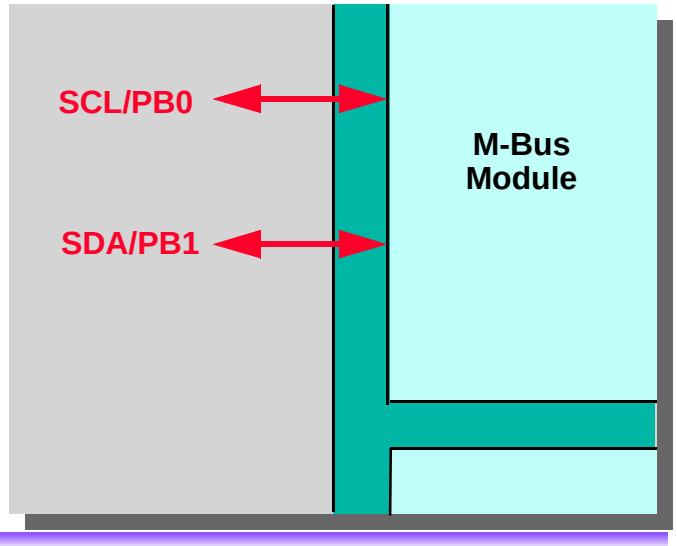
8051-Compatible Read Cycle

68307: Power Saving Options

- User can enable Low-Power Standby Mode
  - This mode turns off the external bus and stops the clock to the EC000 core processor
  - Current can be as low as 140 µA
  - Any interrupt can wake the part out of Low-Power Sleep Mode
- Low-Power Stop Mode uses least amount of power
  - This mode goes one step further than Low-Power Standby Mode by turning off the external clock to the device
  - Current can be as low as 52 µA
- External clock speed can be reduced by programming the System Configuration Register (SCR)
  - Clock speed can be divided down from 16 MHz to 64 kHz
- 68307's power savings modes create reductions in power consumption up to 94% from fully operational mode!!

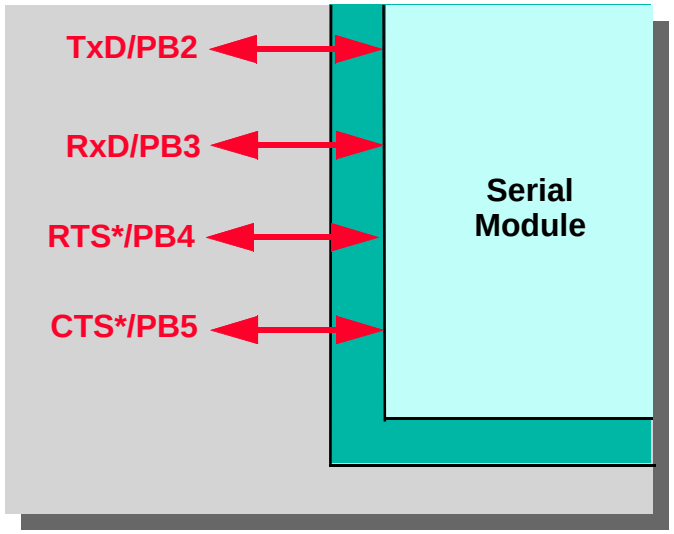
68307: M-Bus Module

- M-Bus is an ideal interface for EEPROMs, LCD controllers, A/D converters and other components that could benefit from fast serial transfers
  - This two-wire bi-directional serial bus allows a master and a slave to rapidly exchange data
  - It allows for fast communication with no address translation
  - Multiple slaves and masters are possible
  - Arbitration and collision detection features are available
  - Clock speeds can be programmed by user. Maximum transfer rate is 100 kb/s



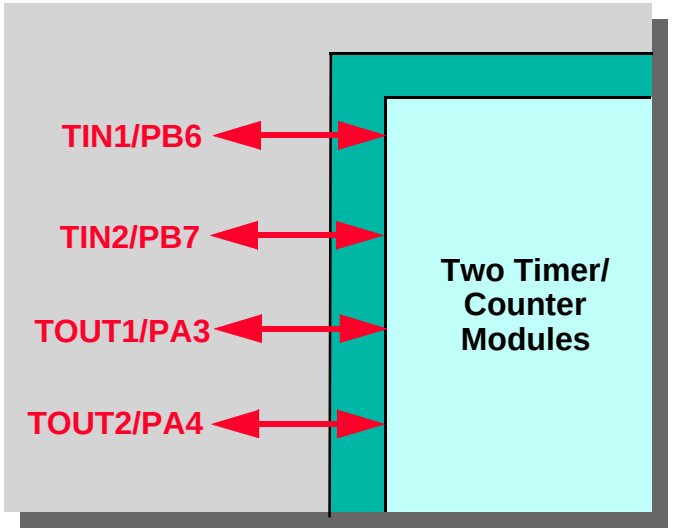
68307: Serial Module

- Full-Duplex Asynchronous/Synchronous Receiver/Transmitter
  - Quadruple-Buffered Receiver
  - Double-Buffered Transmitter
- Compatible with MC68681
- Flexibility of separate baud rates for the receiver and transmitter (up to 260kbaud)
- Full support of multidrop mode (up to 256 slaves)
- 5 Maskable Interrupt Conditions
- Modes available for connection diagnostics:
  - Automatic Echo
  - Remote Loopback
  - Local Loopback
- Error detection
  - Parity
  - Overrun
  - Framing
- Break generation and detection



68307: Timer Module

- Two 16-bit Programmable Timer/Counters
- Multiple Clock Sources
  - External oscillator
  - System clock
- 8-bit prescaler that acts as clock divider
- Operational Modes
  - Free run/restart
  - Toggle or pulse at reference value
    - » Used for square wave generation
    - » Used for periodic interrupt generation
  - Capture counter value on TIN transition
- System Watchdog Timer Logic to protect against non-terminating bus cycles
  - Watchdog timer must be cleared periodically to ensure time-out value is not reached
- 60-ns resolution @ 16.67 Mhz



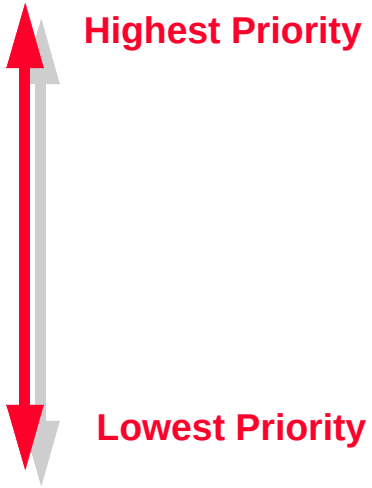
68307: System Integration Module

- System Integration takes the place of much of the external logic usually required in a system
  - System Configuration Module
    - » Module Base Address Register (MBAR) for relocatable peripheral register addressing
    - » System Configuration Register to set operation modes
  - System Protection Module

    - » Hardware Watchdog (count length range from 128 to 16384 clock cycles)
    - » Software Watchdog
  - Chip Select Logic
    - » 4 programmable chip selects that can access up to 16 Mbyte of memory
    - » Capable of being read only, write only, or both read/write
    - » Up to six wait states
    - » Minimum block size is 8192 bytes
  - External Bus Interface
    - » M68000 or 8051-Compatible bus and control signals

68307: System Integration Module

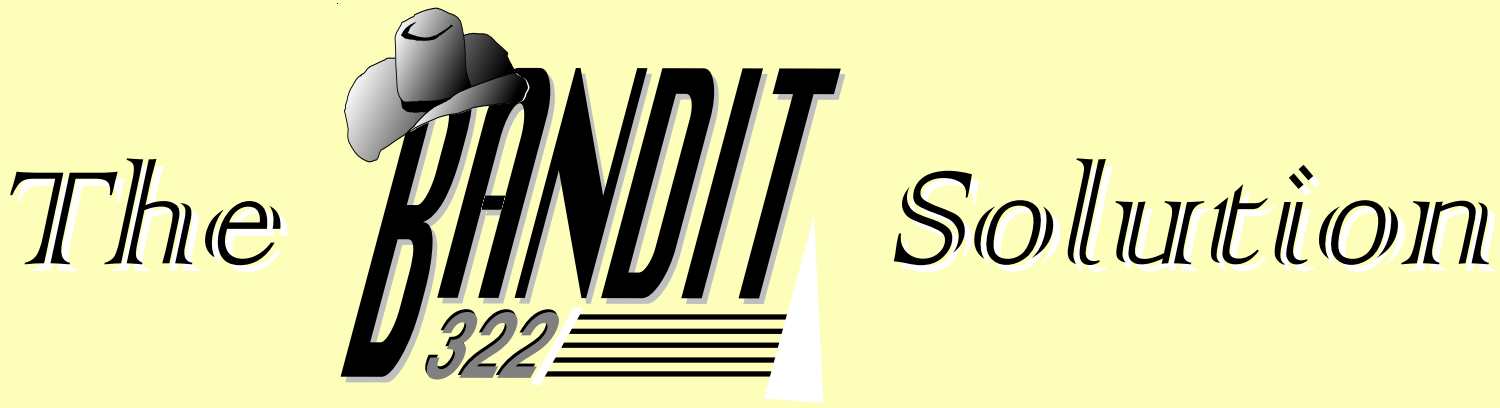
- Parallel I/O Port
  - 24 programmable pins as inputs or outputs on a bit-by-bit basis
- Interrupt Controller
  - IRQ7*
  - INT1*(highest) - INT8*(lowest)
  - Timer1
  - Timer2
  - UART
  - M-Bus



- Low Power Sleep Logic
  - Logic to support various power saving modes
- JTAG Module
  - IEEE 1149.1 compliant
  - Used for board level interface testing

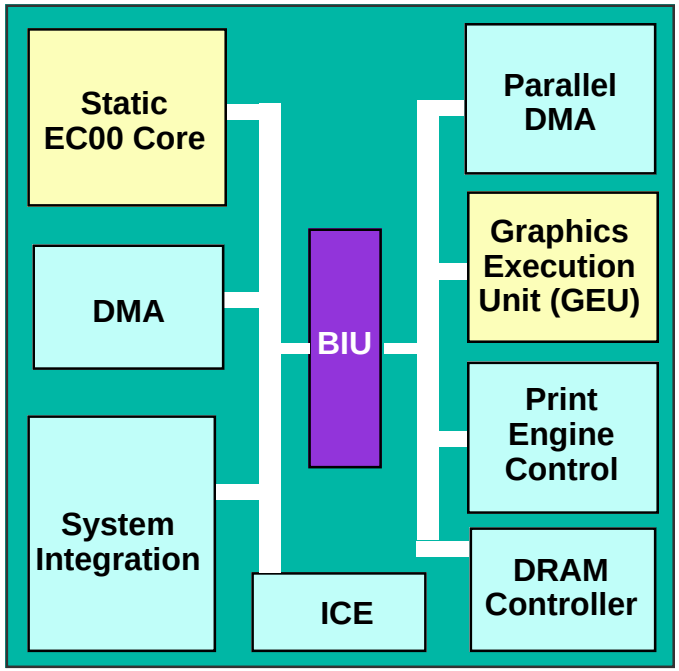
68322: Advantage

The 68322 offers a single-chip printer solution by integrating a 68EC000 core with a RISC graphics engine



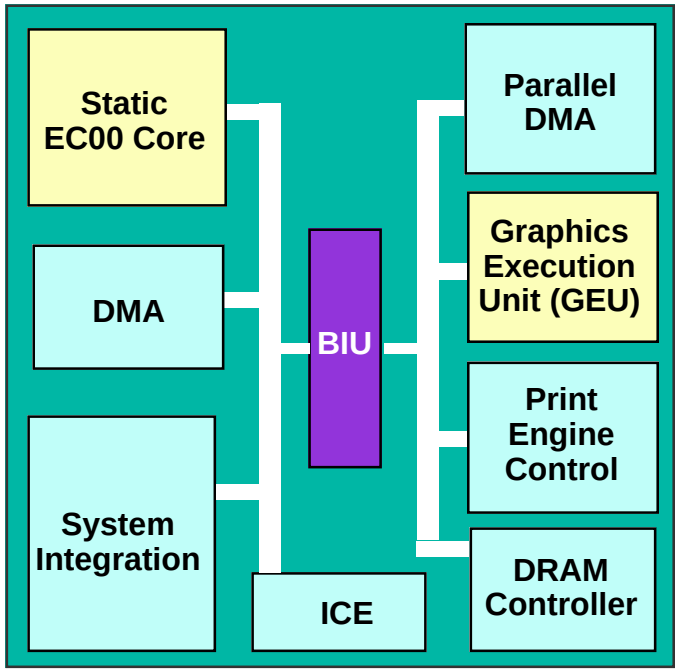
68322: Features

- Completely integrated, single-chip printer solution
  - Static EC000 core processor
    - » EPA Energy Star
  - RISC graphics engine
    - » Enables H/W Banding
    - » Reduced System Memory Cost
- Dual Bus Architecture
  - High Bus Bandwidth
  - True Parallel Processing
  - Distributed Workload
- Print Engine Video Controller
  - Programmable Printer Interface
  - Toner Conservation
  - 4-8 PPM Performance
- Memory Reduction Techniques
  - Hardware assisted 300-600 DPI Resolution
  - 3x Memory Reduction

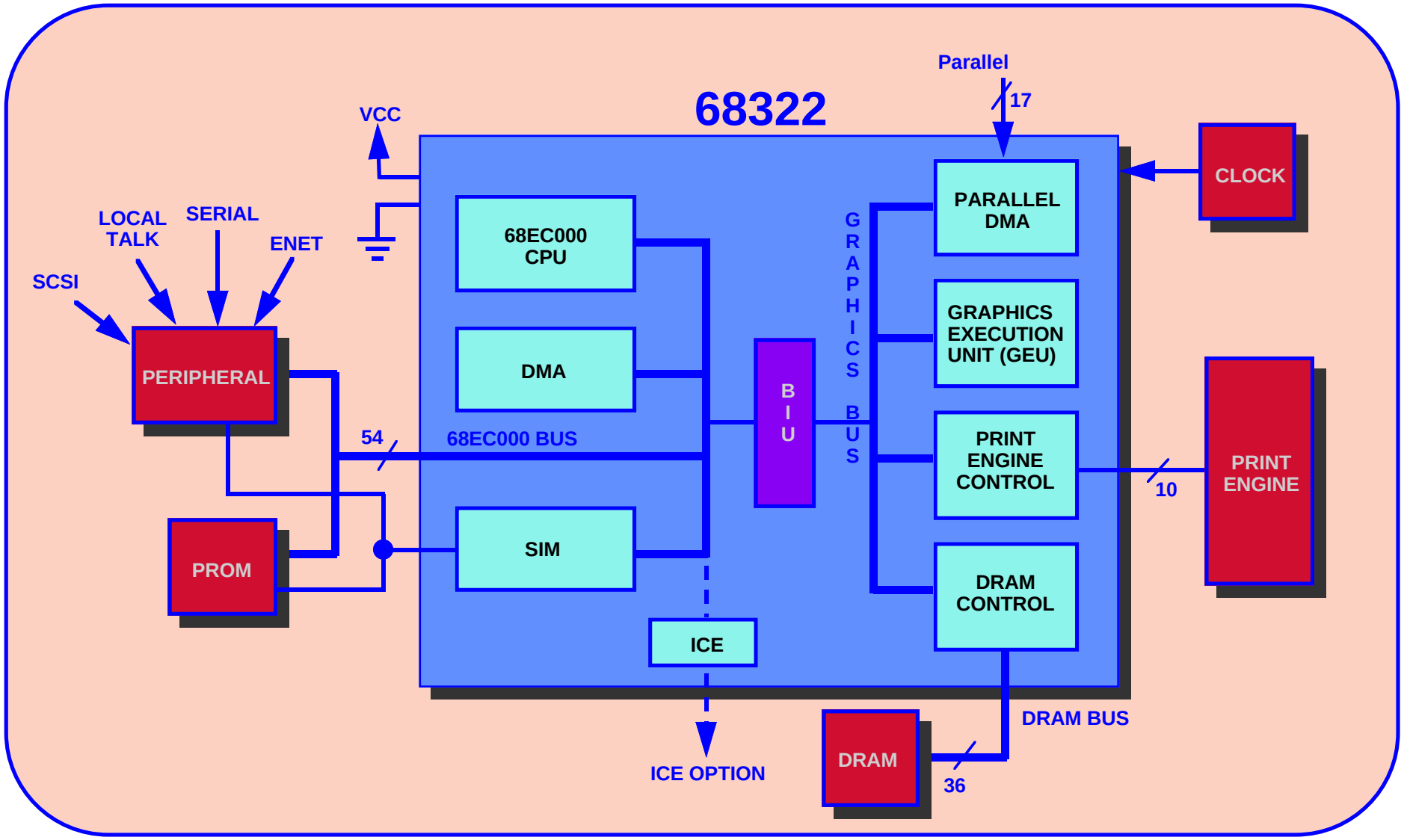


68322: Features

- Bursting DRAM controller
  - Controls 6 banks of variable size DRAM
  - Transparent Refresh
- IEEE 1284 Parallel Port
  - High speed bi-directional DMA transfers
- General Purpose DMA Controller
  - Low Impact, High Speed Peripheral Downloading
- System Integration
  - Glueless Interface to peripherals
  - Font Cartridge Support
  - Programmable Chip Selects
- Available in 16, 20 Mhz
- 160-lead FT package



68322: Block Diagram



Banding: A Memory/System Cost Saver

- Banding techniques render page image in strips or “bands”
  - Banding consumes as little as 1/20th of the memory required to render the entire page
  - Reduces printer systems dependency on expensive memory
- Direct hardware executed banding outperforms software banding
  - Enables more complex pages to be printed
  - Utilizes fewer band buffers than software banding
- Hardware banding is driven by compressed display list
  - Display list represents compressed page image defined by RGP graphics orders
  - RGP automatically updates display list on band fault
- Display List generation is key
  - Display lists are simple data structures

The Power of the RISC Graphics Processor

- One blt2bb_sd RGP graphic order (60x100) equivalent to execution of over 3400 MC68000 instructions
  - Software bitBLT was hand-coded, fine-tuned MC68000 assembly routine
  - MC68000 is CISC, RISC would require even more instructions
- "Setup" graphic orders lower the number of parameters required by subsequent drawing graphic orders (bitBLTs and scanline transfers)
  - Memory requirements reduced
  - Emulation code simplified
- Graphic orders provide basic low-level operations
  - Easily map into various PDL emulations

68322: User Benefits

- Overall system cost savings
  - Reduced component count
  - Reduced manufacturing costs
  - Reduced memory requirements
- System performance
  - High speed IEEE 1284 parallel port
  - Dual bus architecture enables parallel processing
  - Hardware Banding
  - Power of RGP Graphics Orders
  - 68322 provides up to 8 ppm/600 dpi level of performance
- Time-to-market
  - Motorola Support Environment
  - Third party ISV's provide source code, reference designs & turnkey systems
  - Upwardly compatible solutions provide migration path to higher performance

68322: Support Environment

- 68K Source
  - Language Development Tools
  - Debuggers, Simulators, Analyzers & Testers
  - Real-Time Operating Systems
  - Emulators and Logic Analyzers
- Independent Software Developers
  - Peerless Systems
  - Destiny
  - Xionics (formerly Phoenix Technologies)
  - PCPI
- Motorola's AESOP Bulletin Board -> World Wide Web
  - Documentation
  - FreeWare
- Motorola Applications Engineering
  - Development Boards

68322: Support Environment

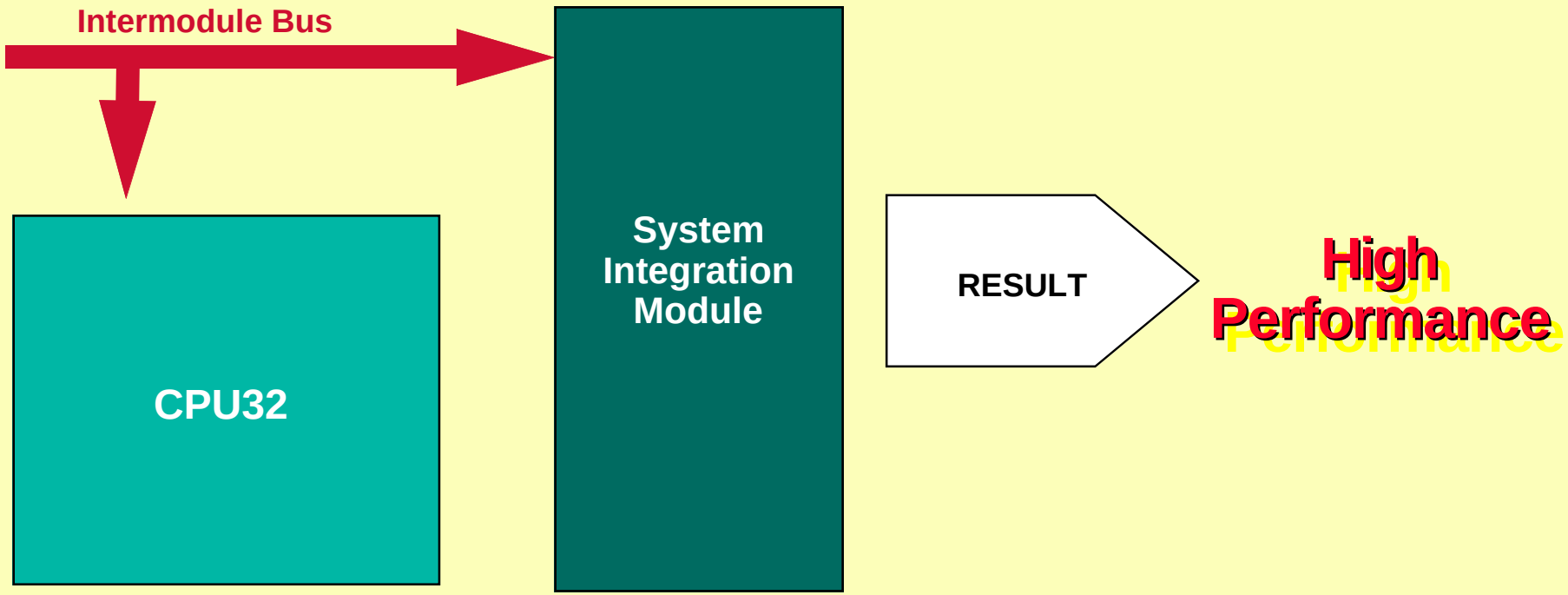
- Parallel Port Software Package (PPSP)
  - Supports IEEE1284 protocol
    - Compatibility mode
    - Byte mode
    - Nibble mode
    - Extended Capabilities Port (ECP) mode
  - Incorporates 68322 hardware support for enhanced performance
    - Compatibility mode
    - ECP forward data transfers
    - Run-length encoding in ECP mode
  - User requirements
    - Integrate buffering scheme for reverse data transfers
    - Add timing functions to support host timeout
  - Qualified PPSP product using Genoa Test Suite

68322: Support Environment

- Display List Viewer (DLV) Tool
  - Enables software development to take place in parallel with hardware development
  - Emulates 322 Graphics Execution Unit to enable debugging of 322 display lists
  - Produces pixel for pixel representation of rendered image on screen
  - Runs under PC (Windows) or Sun (Unix) environments
  - 322 Display List Disassembler

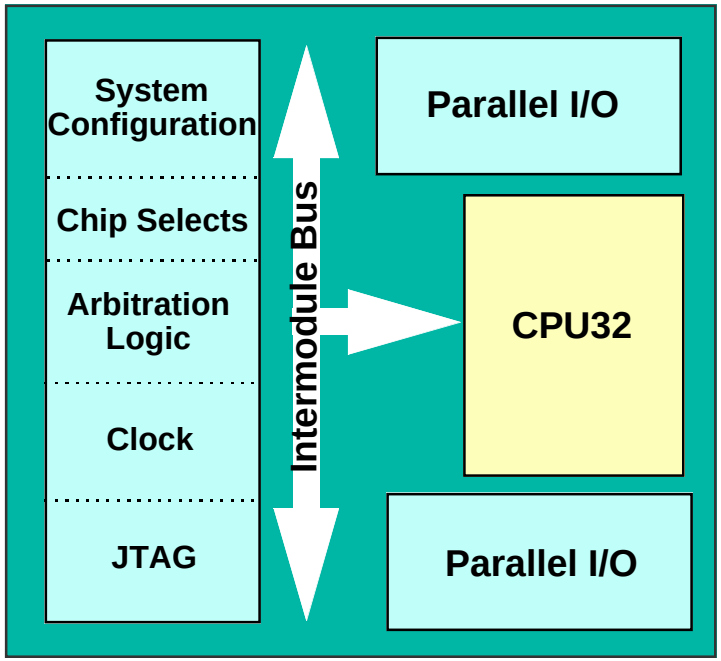
68330 Advantage

The 68330 is a general purpose processor that combines the powerful CPU32 with system integration over an Intermodule Bus (IMB) that is specially designed to interface with the CPU32 and on-chip modules



68330: Features

- CPU32 core based on 68020
- Four Programmable Chip Selects
- System Integration Module
  - **Configuration & Protection Logic**
    - » Software Watchdog Timer
    - » Periodic Interrupt Timer
    - » Various bus monitors
    - » Programmable bus termination
  - **External Bus Interface**
    - » 24 address lines, 16 data lines
  - **Power-Saving Features**
    - » HCMOS technology
    - » LPSTOP instruction and much more!
- 16 Programmable I/O Pins
- Available in 5V or 3.3V
- Frequency: 16 or 25Mhz
- Extended Temperature range at 5V
- Packages: 144-lead PV



68330: Bus Operations

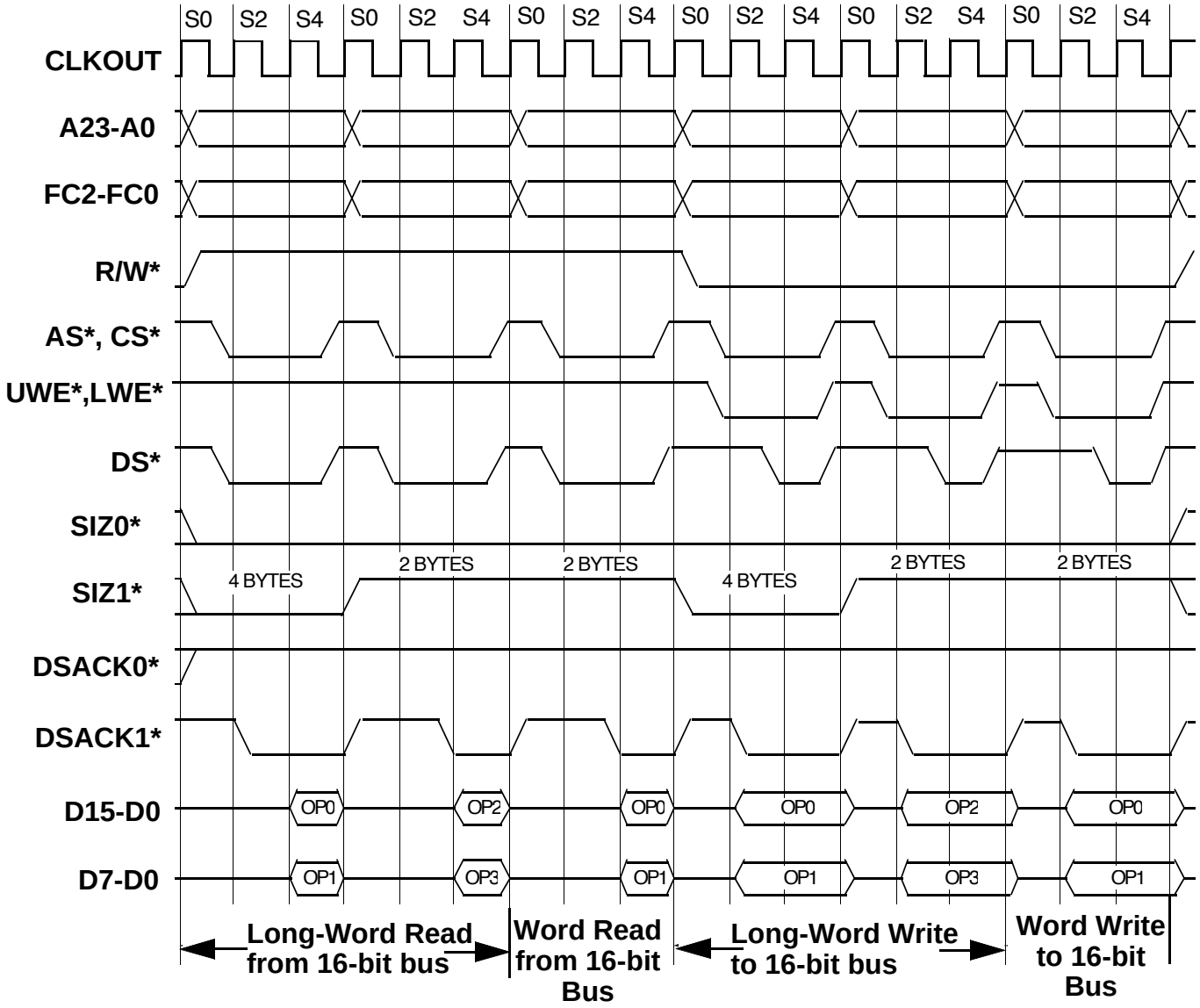
- 24 external address lines can address up to 4 Gigabytes of memory; 16 data lines available
- Bus Controller allows flexible data transfers
  - Byte, word, or longword transfers are possible
  - Dynamic bus sizing
  - Synchronous & Asynchronous transfers
    - » Synchronous transfers are 3 clock cycles
  - Fast Termination mode generates 2 clock accesses
- External function code pins indicate space type

Function Code Bits				Address Spaces
3	2	1	0	
0	0	0	0	Reserved (Motorola)
0	0	0	1	User Data Space
0	0	1	0	User Program Space
0	0	1	1	Reserved (User)
0	1	0	0	Reserved (Motorola)
0	1	0	1	Supervisor Data Space
0	1	1	0	Supervisor Program Space
0	1	1	1	Supervisor CPU Space
1	x	x	x	Reserved (Motorola)

68330: Bus Operations

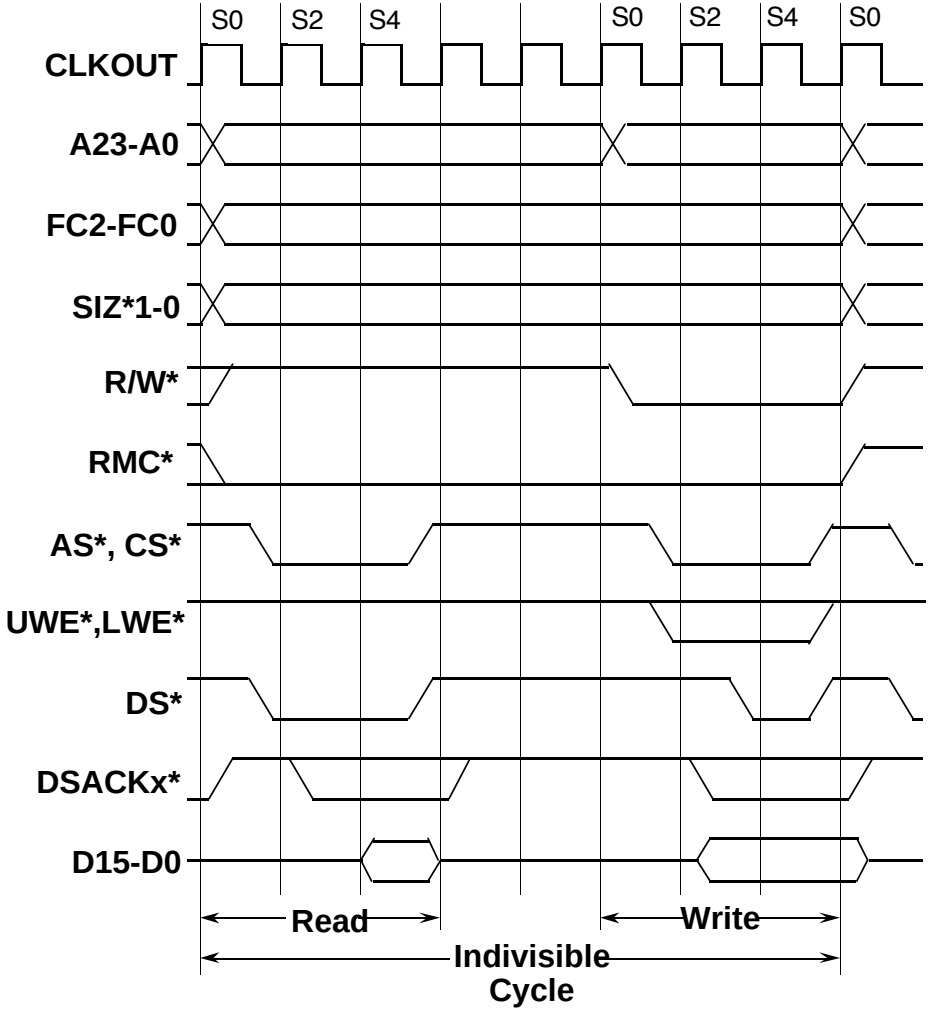
- 68330 efficiently handles exception operations:
  - BERR
  - Retry
  - Halt
  - Double Bus Fault
- Bus arbitration logic allows external masters to control the bus
- Read-Modify-Write Logic is present for multi-processing environments
- Internal cycles can be shown on the external bus through programming Module Configuration Register (MCR)

68330: Bus Operations (Read & Write)



68330: Bus Operations

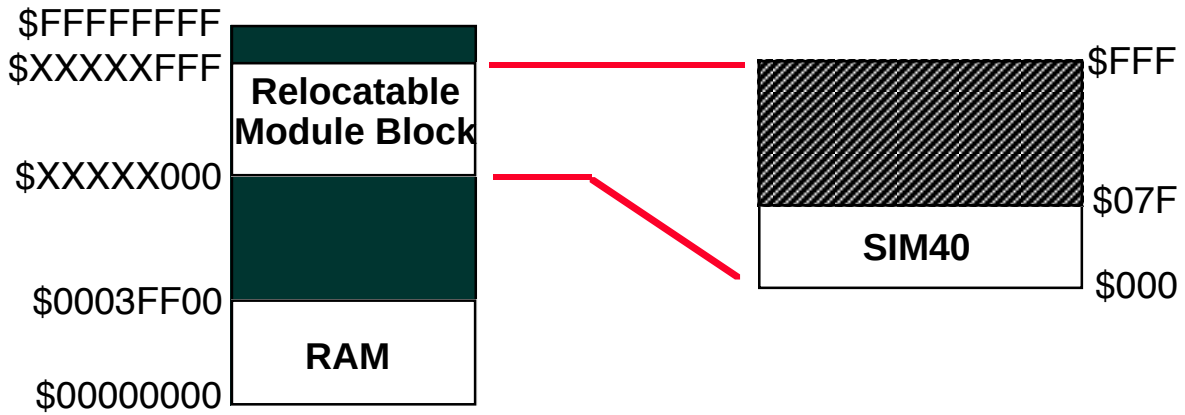
Read-Modify-Write cycles do not acknowledge bus requests or interrupts until both the read and the write cycle are finished



Read-Modify-Write Cycle

68330: System Integration

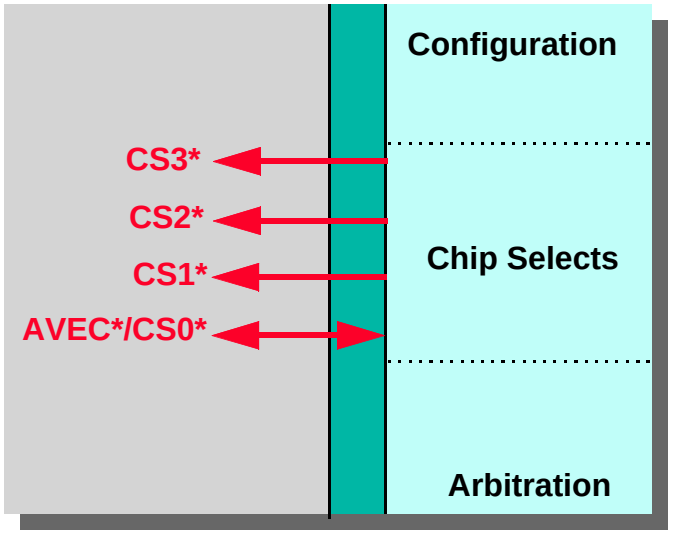
- System Configuration & Protection
  - 4K relocatable module register block
    - » Defined by Module Base Address Register (MBAR at $0003FF00)



  - Module Configuration Register
    - » Controls functional operations of processor
  - Bus Monitor Logic for error checking
    - » Internal Bus Monitor
    - » Double Bus Fault Monitor
    - » Spurious Interrupt Monitor
  - Software Watchdog Timer
    - » Prevents infinite looping of software

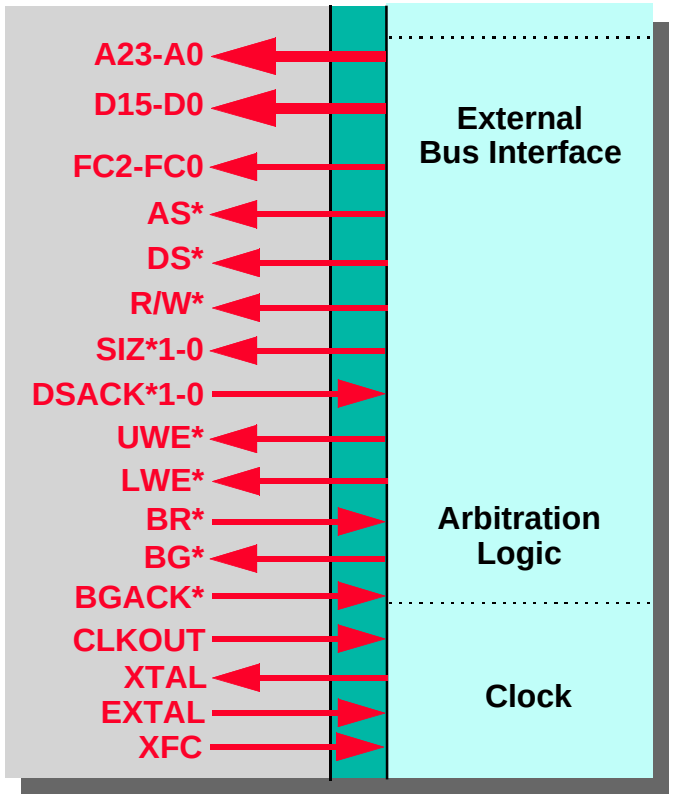
68330: System Integration

- Periodic Interrupt Timer
  - Used in multi-tasking or as real time clock (RTC)
- Four Programmable Chip Selects
  - Can access 256 bytes to 4 Gigabytes in increments of 2^n
  - Capable of selecting 8- & 16- bit ports
  - Control of write protection
  - Option of fast termination
  - Option of pre-programmed wait states (up to 3)
  - Choice of address space type selection (ex. CPU, user data)



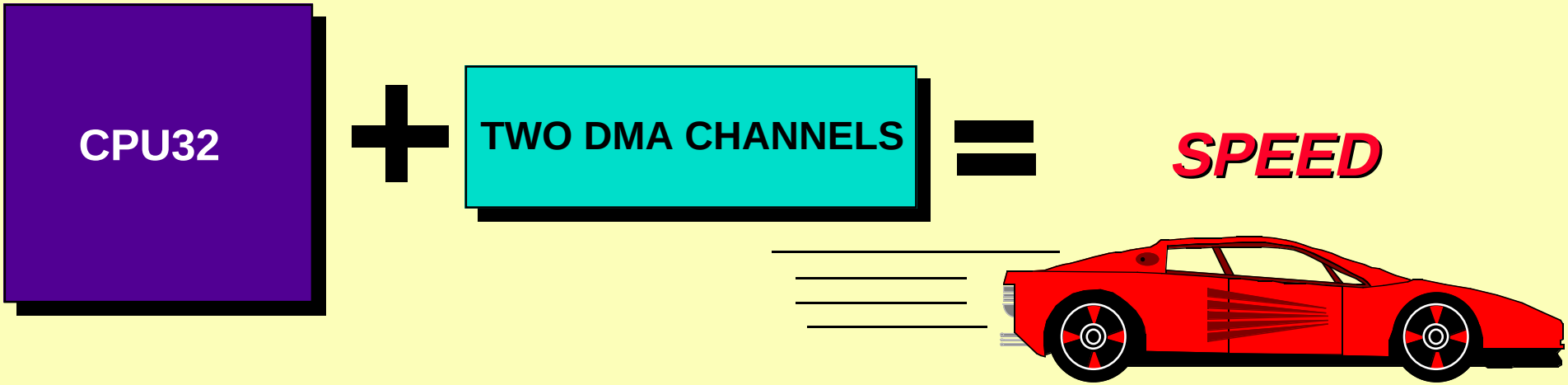
68330: System Integration

- External Bus Interface & Bus Arbitration Logic
  - 24 address lines, 16 data lines, control signals
  - External device can gain bus mastership through three-wire or two-wire arbitration
    - » SIM is always has a level seven bus priority
- Parallel I/O Port & Interrupt Controller
  - 16 programmable I/O pins
  - Seven multiplexed external interrupt request lines for peripheral devices
- Clock Synthesizer Logic allows 68330 to operate with different clock sources
  - Crystal oscillator
  - External clock
  - External clock w/ PLL activated
  - Limp mode
- 1149.1 IEEE JTAG



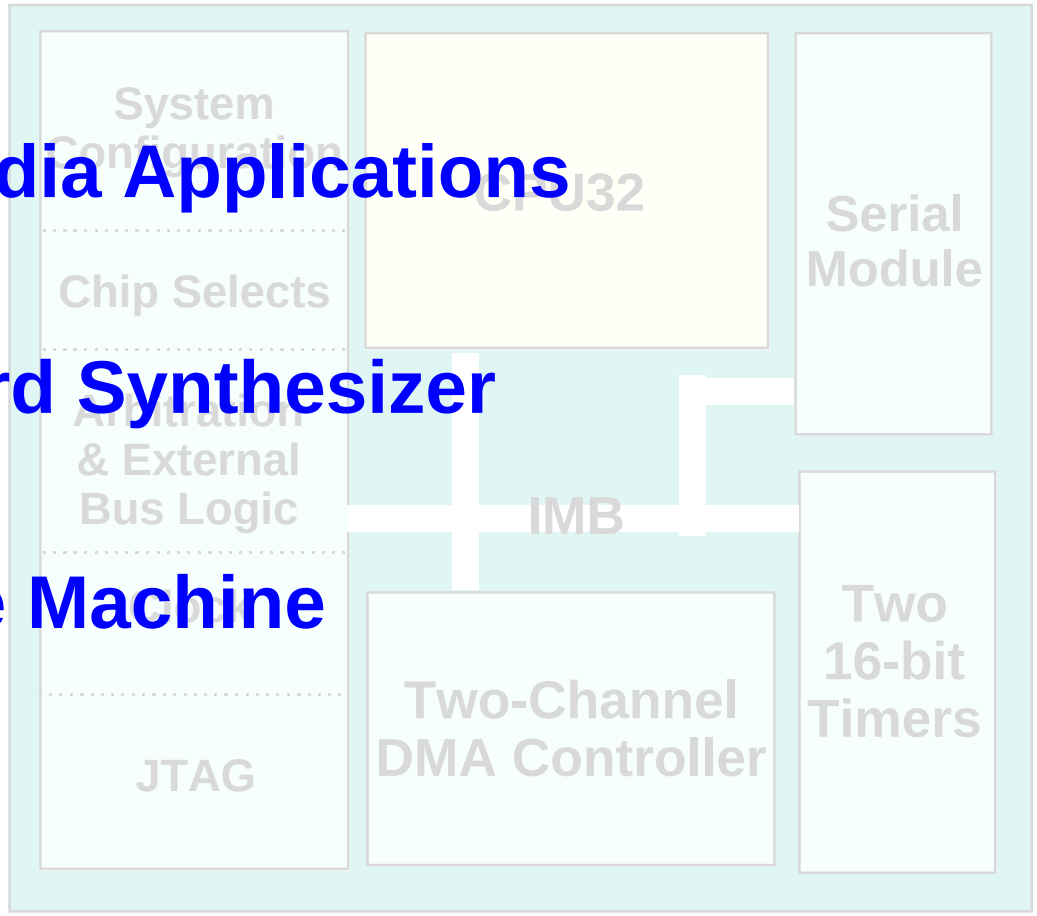
68340 Advantage

By integrating DMA & the CPU32 on-chip, applications with fast data movement are optimized!



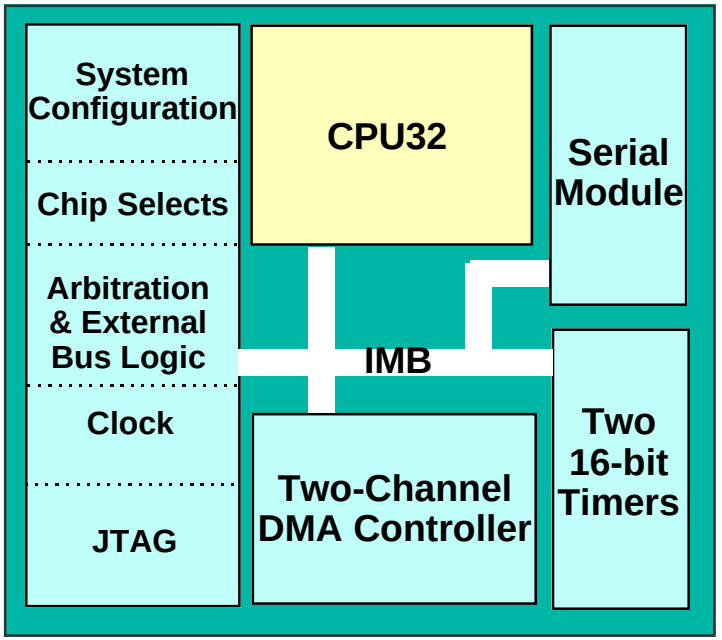
68340: Applications

- LAN Interconnects
- Multimedia Applications
- Keyboard Synthesizer
- Karaoke Machine



68340: Features

- CPU32 core based on MC68020
- Two-channel DMA module
- DUART compatible with MC68681/MC2681
- Two 16-bit Timer/Counters
- System Integration
  - System Protection & Configuration
  - Four Programmable Chip Selects
  - External Bus Interface & Arbitration Logic
  - Clock Synthesizer
  - JTAG
  - 16 Programmable I/O Pins
- 0.65µ & 0.8µ HCMOS process
- Offered in 16 & 25 MHz, 3.3V & 5V
- Extended Temperature Available
- Packages: 144- lead FE, PV, & FT



68340: Bus Operations

- 24 external address lines can address up to 4 Gigabytes of memory; 16 data lines available
- Bus Controller allows flexible data transfers
  - Byte, word, or longword transfers are possible
  - Dynamic bus sizing
  - Synchronous & Asynchronous transfers
    - » Synchronous transfers are 3 clock cycles
  - Fast Termination mode generates 2 clock accesses
- External function code pins indicate space type

Function Code Bits				Address Spaces
3	2	1	0	
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0	0	0	1	User Data Space
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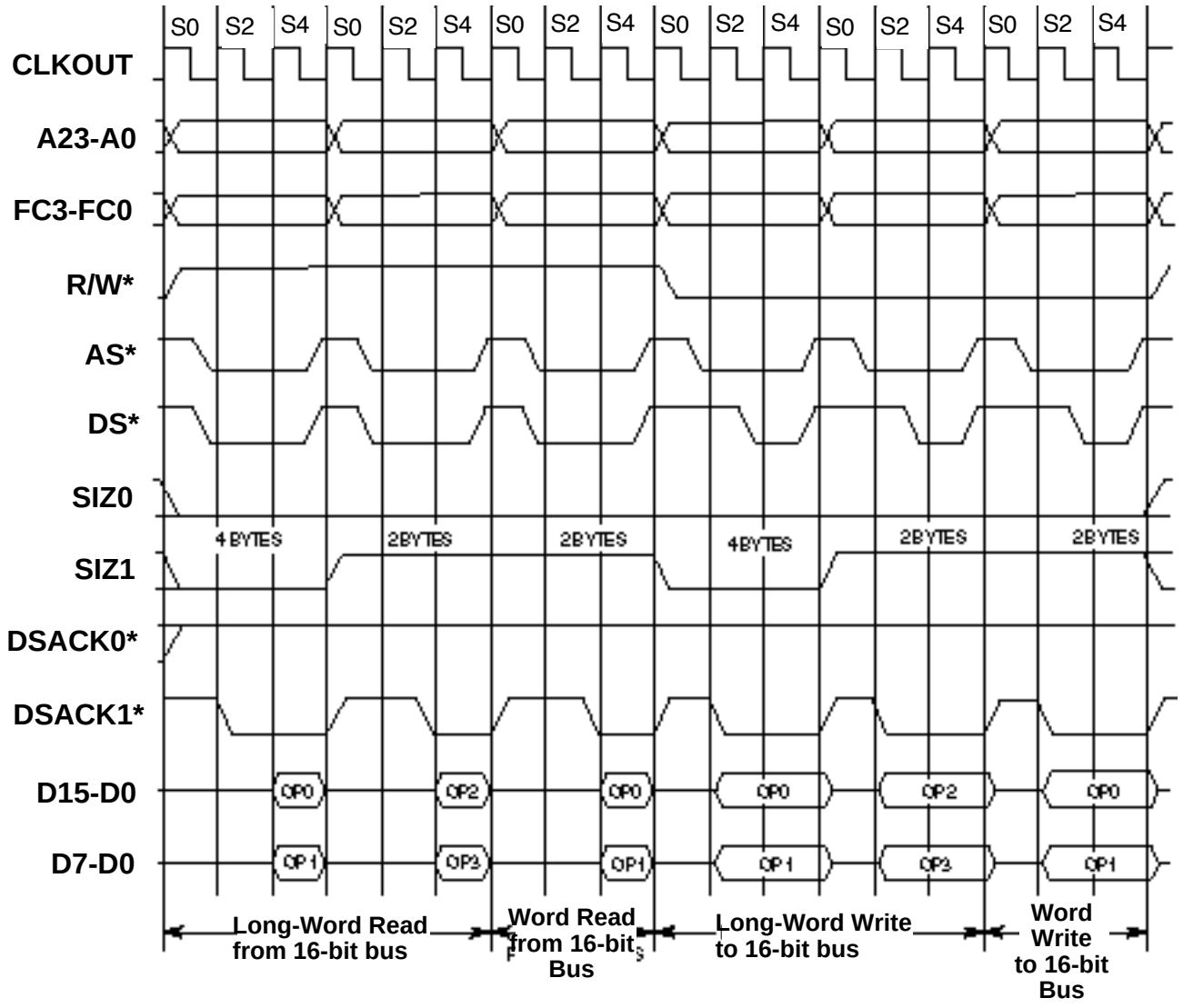
0	0	1	1	Reserved (User)
0	1	0	0	Reserved (Motorola)
0	1	0	1	Supervisor Data Space
0	1	1	0	Supervisor Program Space
0	1	1	1	Supervisor CPU Space
1	x	x	x	DMA Space

68340: Bus Operations

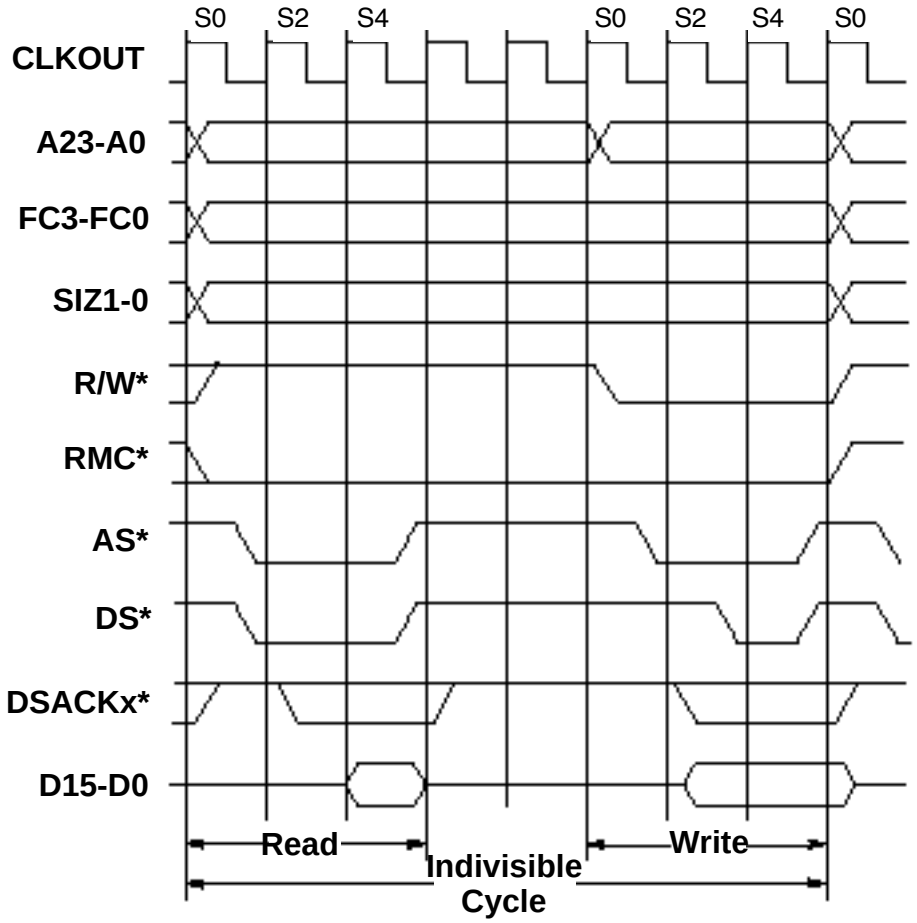
- 68340 efficiently handles exception operations:
  - BERR
  - Retry
  - Halt
  - Double Bus Fault
- Bus arbitration logic allows external masters to control the bus
- Read-Modify-Write Logic is present for multi-processing environments
- Internal cycles can be shown on the external bus through programming Module Configuration Register (MCR)

68340: Bus Operations (Read & Write)



68340: Bus Operations

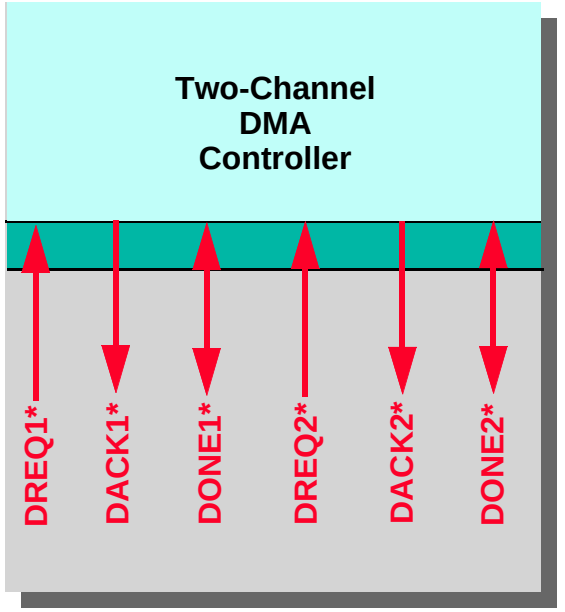
Read-Modify-Write cycles do not acknowledge bus requests or interrupts until both the read and the write cycle are finished



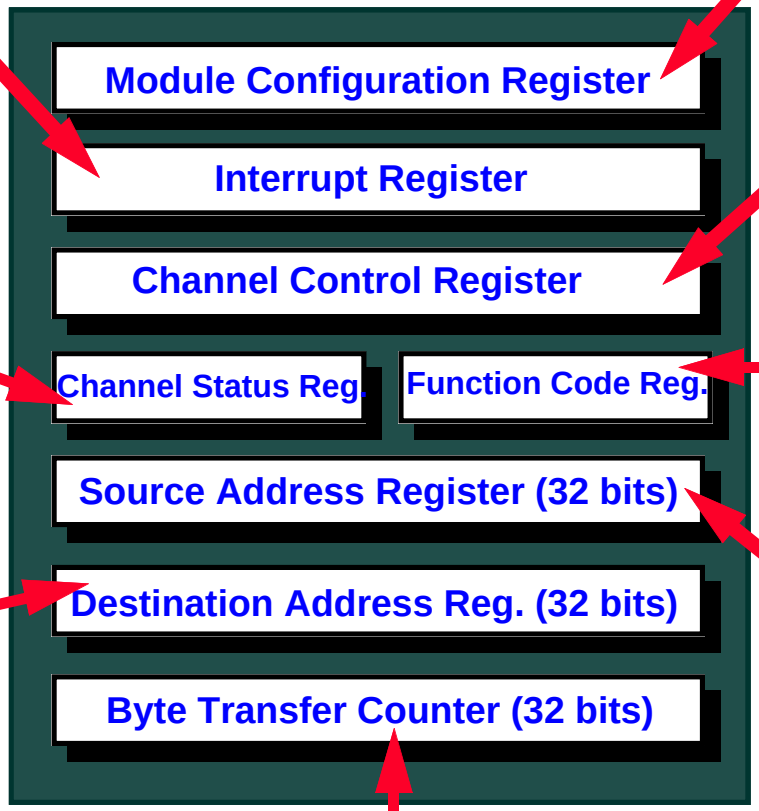
Read-Modify-Write Cycle

68340: DMA Module

- Two-independent fully programmable DMA channels for high speed data transfer
- Single address & Dual Address transfer supported
  - **Single address is only implemented externally**
  - **Dual address transfer supports packing & unpacking**
- Internal cycles allow 25, 50, 75, or 100% bus bandwidth
- External cycles support burst & cycle steal mode
- Transfer rate
  - **25 Mhz: 12.5 Mbytes/s in dual address transfer mode**
    50.0 Mbytes/s in single address mode
  - **16 Mhz: 8.4 Mbytes/s in dual address transfer mode**
    33.3 Mbytes/s in single address transfer mode
- Interrupt generation on normal termination, errors, or breakpoints



68340: DMA Module



Controls DMA configuration such as arbitration ID and Interrupt arbitration ID

Contains priority level and interrupt vector number for channel interrupt request

Controls functions of DMA such as when interrupts occur, what mode the part is in, etc.

Contains status of DMA channel

Source & destination codes for channel

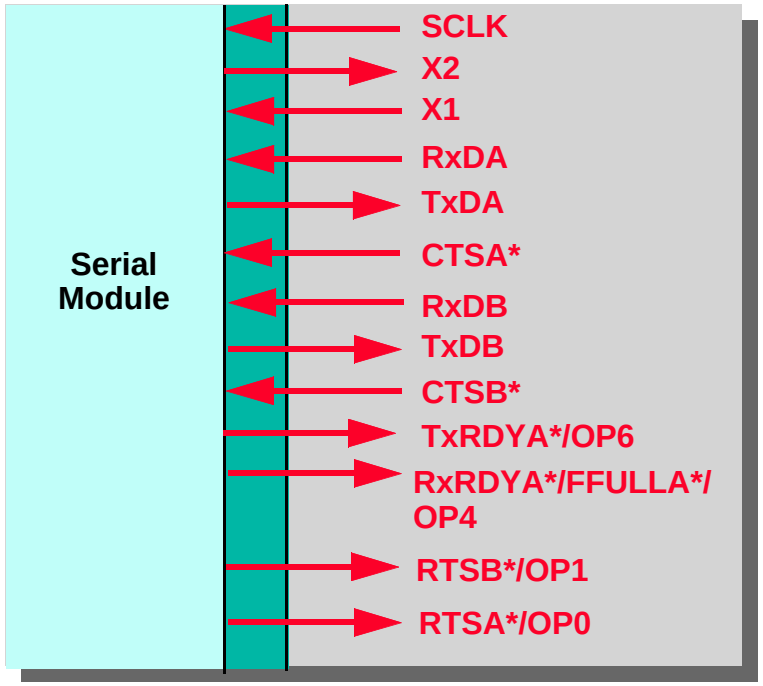
Contains address of source operand used by DMA to access memory or peripheral. Can be incremented or remain constant.

Contains address of destination operand used by DMA to write to memory or peripheral. Can be incremented or remain constant.

Contains the number of bytes left to transfer in a given block.

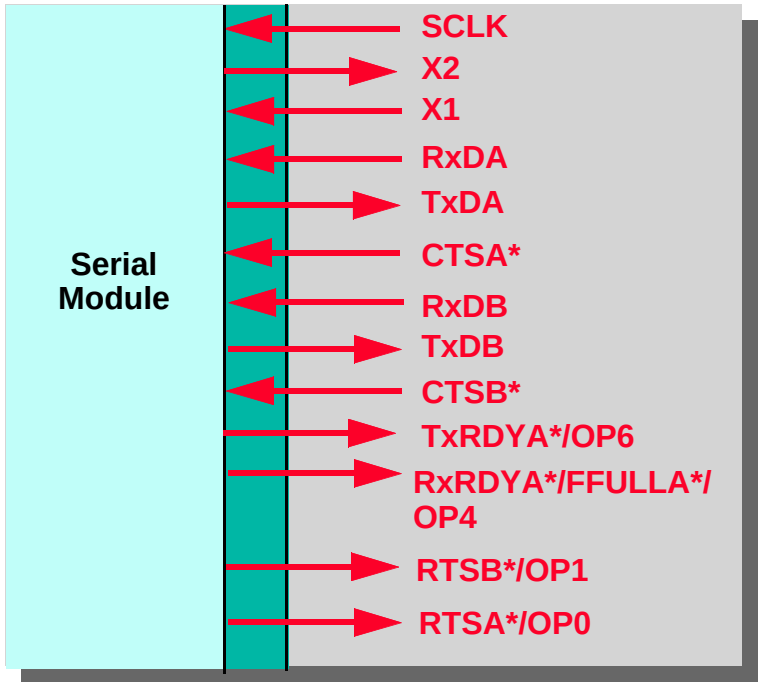
68340: Serial Module

- Two independent, full Duplex Asynchronous/Synchronous Receiver/ Transmitter (DUART) Channels
- Compatible with MC68681/MC2681
- Quadruple-Buffered Receiver
- Double-Buffered Transmitter
- On-chip Crystal Oscillator
- Maximum transfer rate:
  - **1x Mode: 9.8 Mbps@ 25 MHz CLKOUT**
  - **16x Mode: 612 kbps@ 25 MHz CLKOUT**
- Each receiver & transmitter is independently programmable
  - **19 fixed rates from 50 to 76.8 Kbaud**
  - **1x or 16x clock frequency**

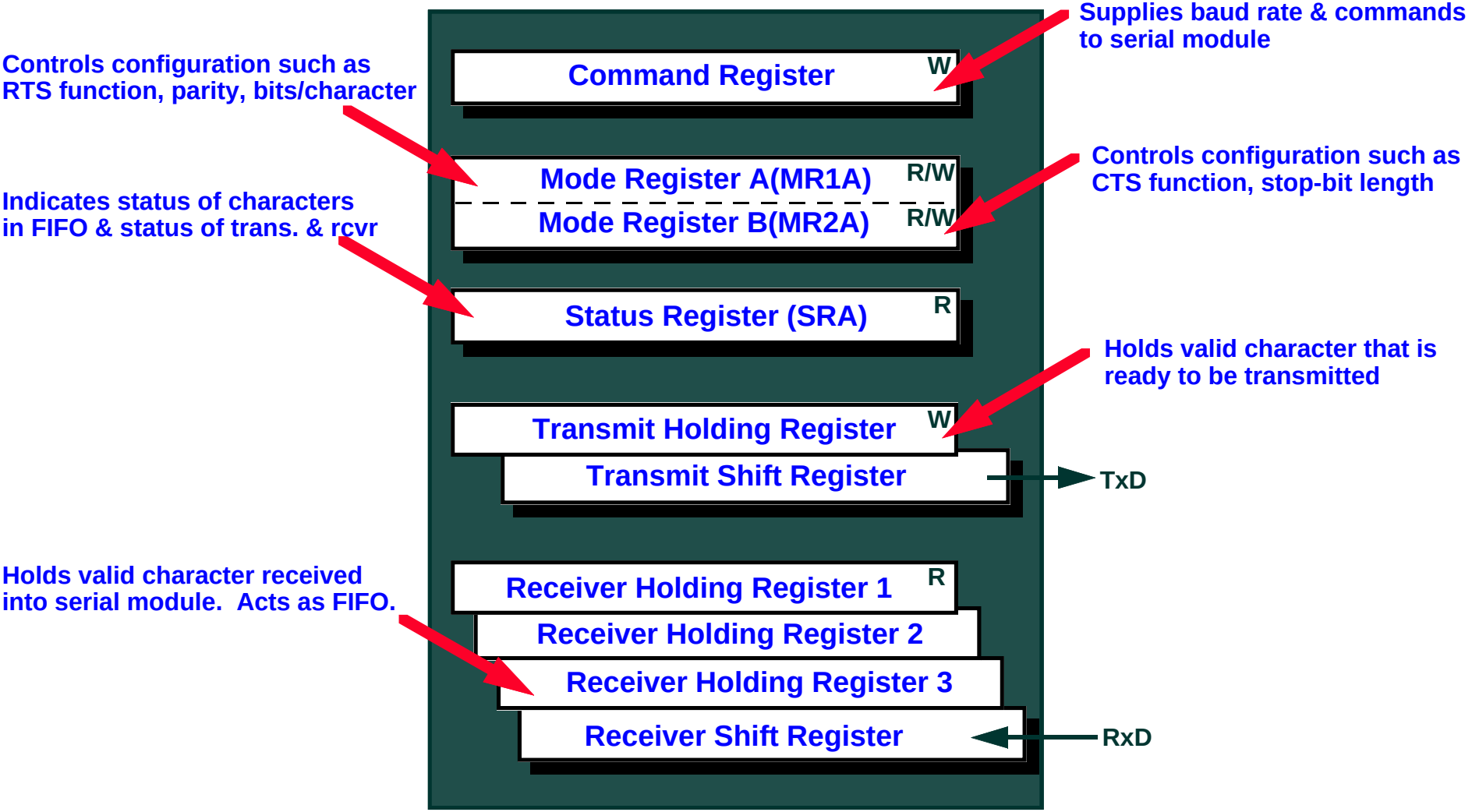


68340: Serial Module

- Seven maskable interrupt conditions
  - Change-of-State on CTSx*
  - Break Condition (either channel)
  - Ready Receive/FIFO Full (either channel)
  - Transmitter Ready (either channel)
- Channel modes for connectivity testing:
  - Automatic Echo
  - Local Loopback
  - Remote Loopback
- Multidrop Mode Supported
- Convenient Break Detection & Generation
- Error Detection:
  - Parity
  - Framing
  - Overrun
- Modem Support

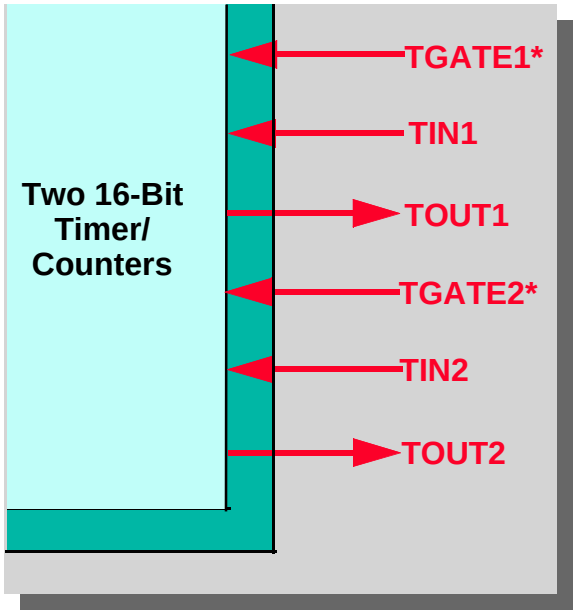


68340: Serial Module

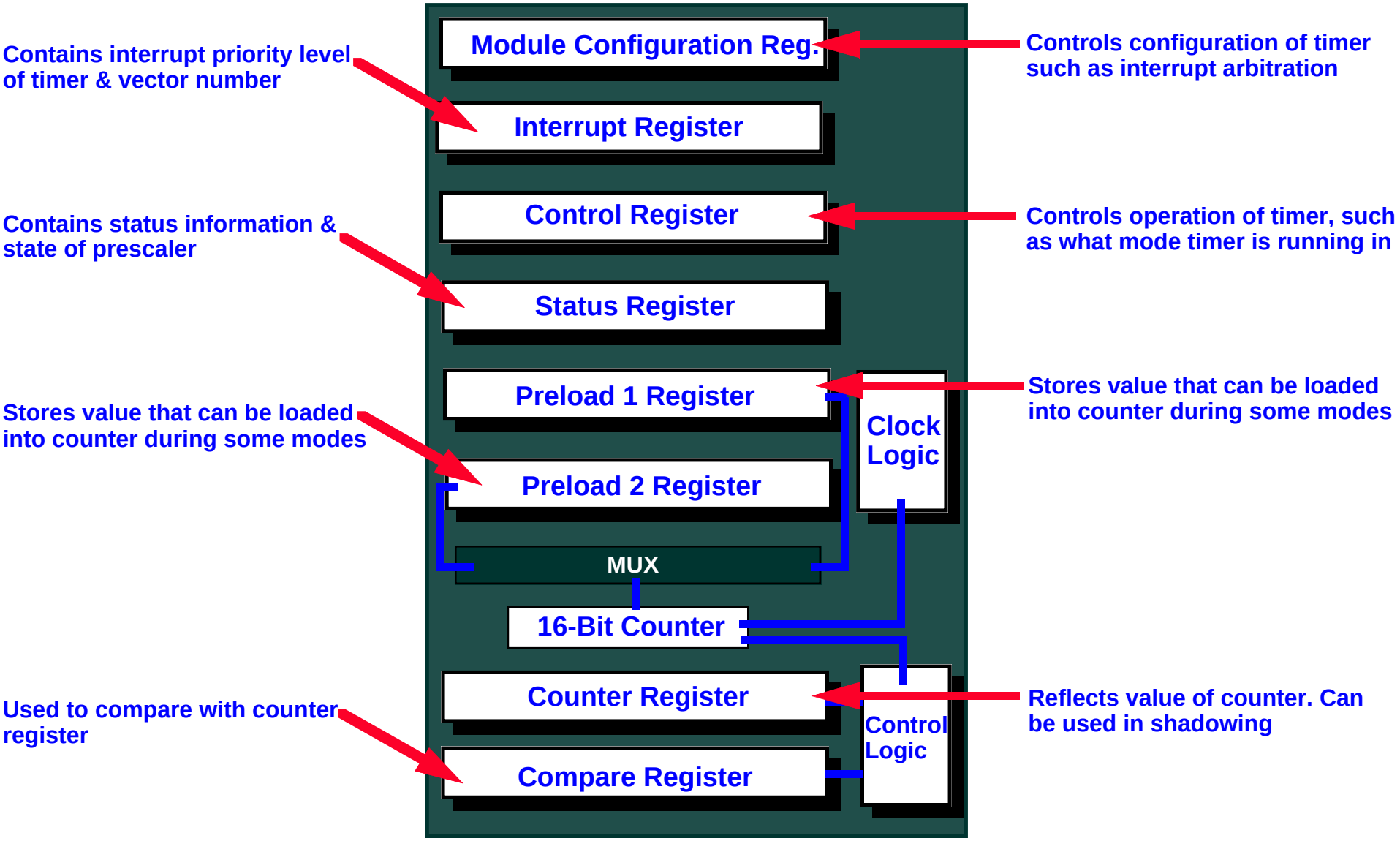


68340: Timer Module

- Two General Purpose Timer/Counters
  - 16-bit countdown counter
  - 8-bit prescaler
  - Multiple Clock Inputs
  - Seven Maskable interrupt conditions based on timer events
- Unique control logic offers numerous operation modes
  - Input Capture/Output Compare
  - Square Wave Generator
  - Variable Duty Cycle Square Wave Generator
  - Variable Width Single Shot Pulse Generator
  - Pulse Width Measurement
  - Period Measurement
  - Timer Bypass
    - » Signals can be programmed as simple I/O ports

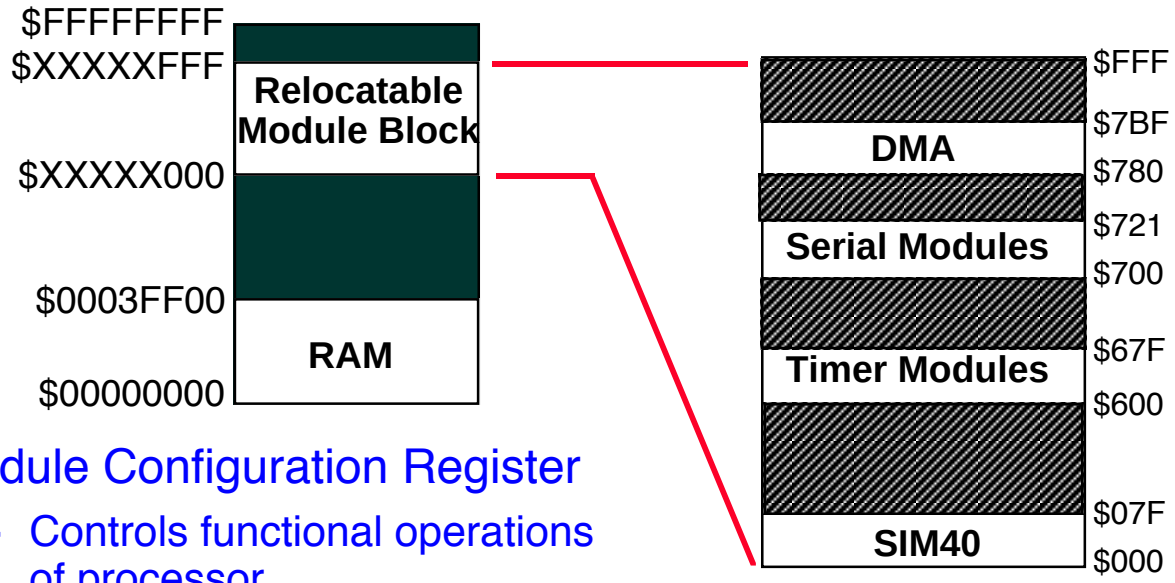


68340: Timer Module



68340: System Integration

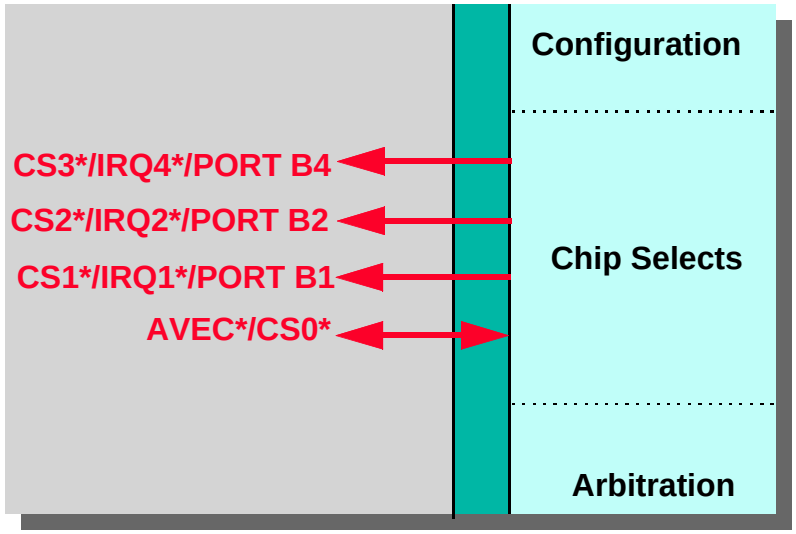
- System Configuration & Protection
  - 4K relocatable module register block
    - » Defined by Module Base Address Register (MBAR at $0003FF00)



  - Module Configuration Register
    - » Controls functional operations of processor
  - Bus Monitor Logic for error checking
    - » Internal Bus Monitor
    - » Double Bus Fault Monitor
    - » Spurious Interrupt Monitor
  - Software Watchdog Timer
    - » Prevents infinite looping of software

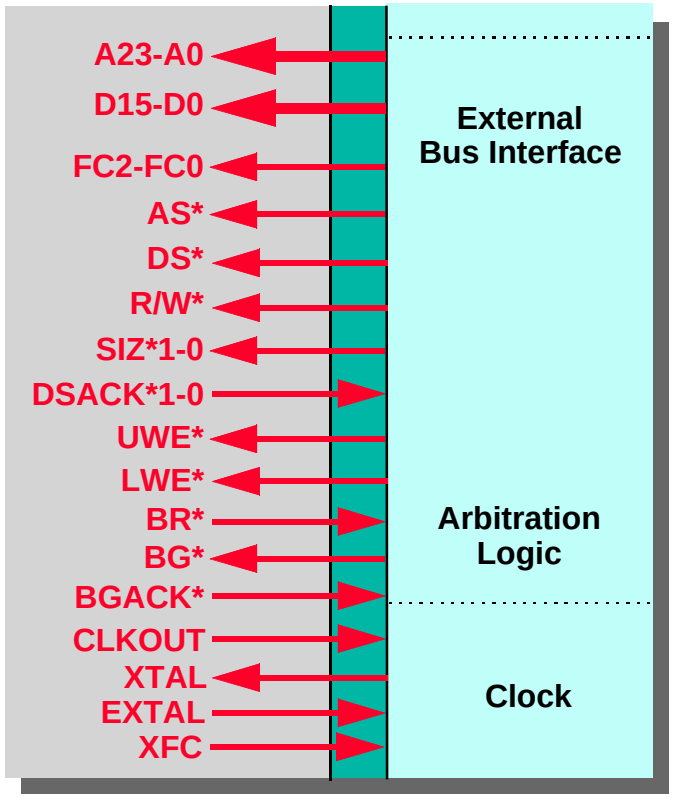
68340: System Integration

- Periodic Interrupt Timer
  - Used in multi-tasking or as Real Time Clock
- Four Programmable Chip Selects
  - Can access 256 bytes to 4 Gigabytes in increments of 2^n
  - Capable of selecting 8- & 16- bit ports
  - Control of write protection
  - Option of fast termination
  - Option of pre-programmed wait states (up to 3)
  - Choice of address space type selection (ex. CPU, user data)



68340: System Integration

- External Bus Interface & Bus Arbitration Logic
  - 24 address lines, 16 data lines, control signals
  - External device can gain mastership through three-wire or two-wire arbitration
    - » SIM always has a level seven bus priority
- Parallel I/O Port & Interrupt Controller
  - 16 programmable I/O pins
  - Seven multiplexed external interrupt request lines for peripheral devices
- Clock Synthesizer Logic allows 68340 to operate with different clock sources
  - Crystal oscillator
  - External clock
  - External clock w/ PLL activated
  - Limp mode
- 1149.1 IEEE JTAG



68340 FAQs

- Can a longword transfer be interrupted by bus arbitration?
  - Yes. The CPU will relinquish control of the bus at the end of the bus cycle following recognition of BR* going active. The only exception to this is that a RMC cycle will not be interrupted, but will complete before the bus is relinquished.
- When bus is driven by an external master, will CS* assert for the same address ranges?
  - CS will NOT assert for addresses driven by an external master. When an external master controls the bus, the 68340 will place its bus in high-impedence state and does not read nor decode the information placed on the bus by the external master.
- Can a user input a clock to BOTH X1 & SCLK, allowing selection of the timing source to be done with the clock-select register?
  - It is permitted to drive both the X1 & the SCLK inputs at the same time, selecting the desired one through the clock-select register.

68340 FAQs

- Why does the 68340 place invalid data on the lower half of the data bus if a user is trying to read from an 8-bit port attached to it?
  - An 8-bit port MUST reside on the data bus bits 15-8. For a write operation the 68340 drives a single-byte operand on both bytes of the data bus because it does not know the port size until the DSACKx* signals are read. For a read, operation, the slave must place data on bits 15-8 of the data bus & assert DSACK0* & negate DSACK1* to indicate an 8-bit port. The MC68340 ignores data bits 7-0.
- Can the bus be arbitrated during RESET?
  - The arbiter is operational even when RESET* is active. The bus can be arbitrated away from the processor during RESET, and the CPU will not begin running bus cycles until the bus is returned to it.

68341: Advantage

With its high-level of integration (DMA, DUART, QSPI) and detailed timing and low-power logic, the 68341 is ideal for multimedia and network applications.

Handheld Computers

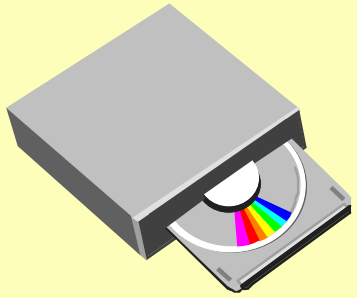
Modems

Set-top Boxes

Compact Disc Interactive

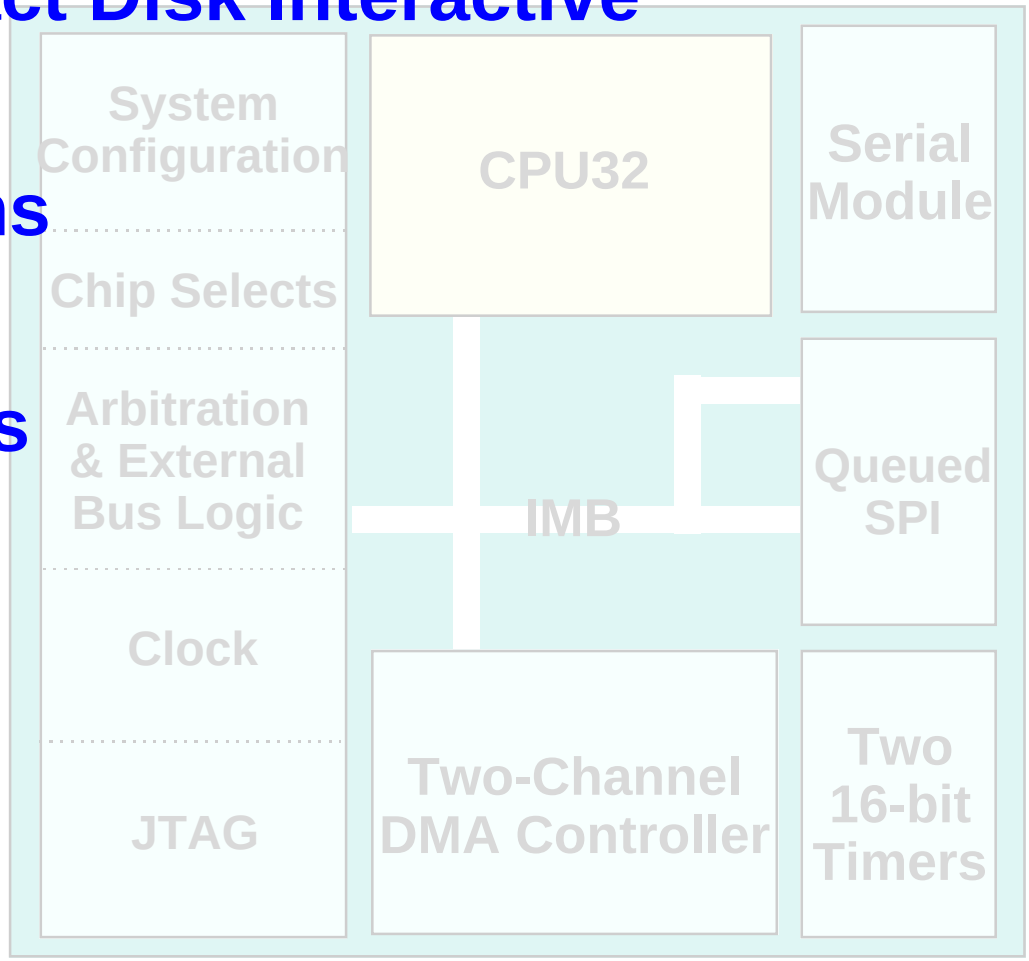
LAN servers

PRINTERS



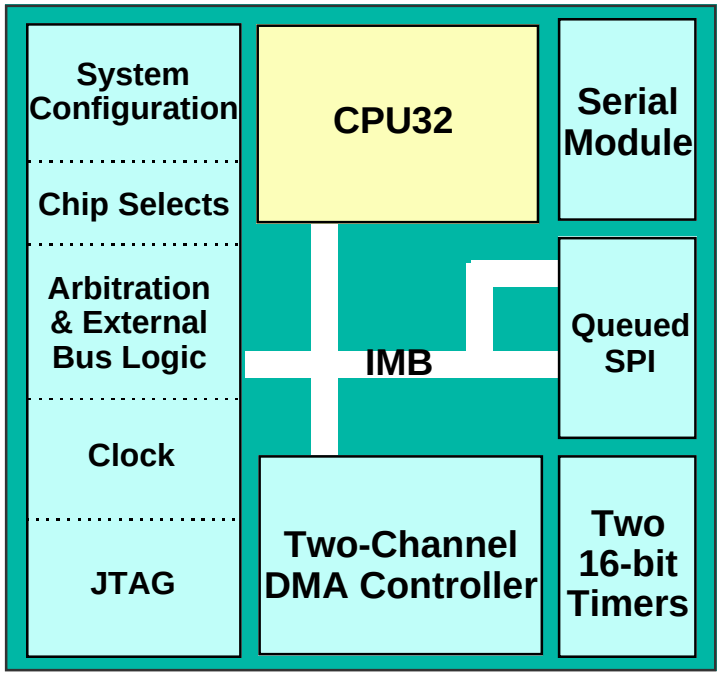
68341: Applications

- Compact Disk Interactive
- Modems
- Printers



68341: Features

- CPU32 core based on MC68020
- Two-channel DMA module
- DUART compatible with MC68681/MC2681
- Two 16-bit Timer/Counters
- Queued Serial Peripheral Module
- System Integration
  - **System Protection & Configuration**
  - **Eight Programmable Chip Selects**
  - **68300/MC68000 bus interface &Arbitration Logic**
  - **Clock Synthesizer**
  - **16 Programmable I/O Pins**
  - **JTAG**
- 0.8µ HCMOS process
- Offered in 16 & 25 MHz, 3.3V & 5V
- Extended Temperature Available
- Packages: 160- lead FT



68341: Bus Operations

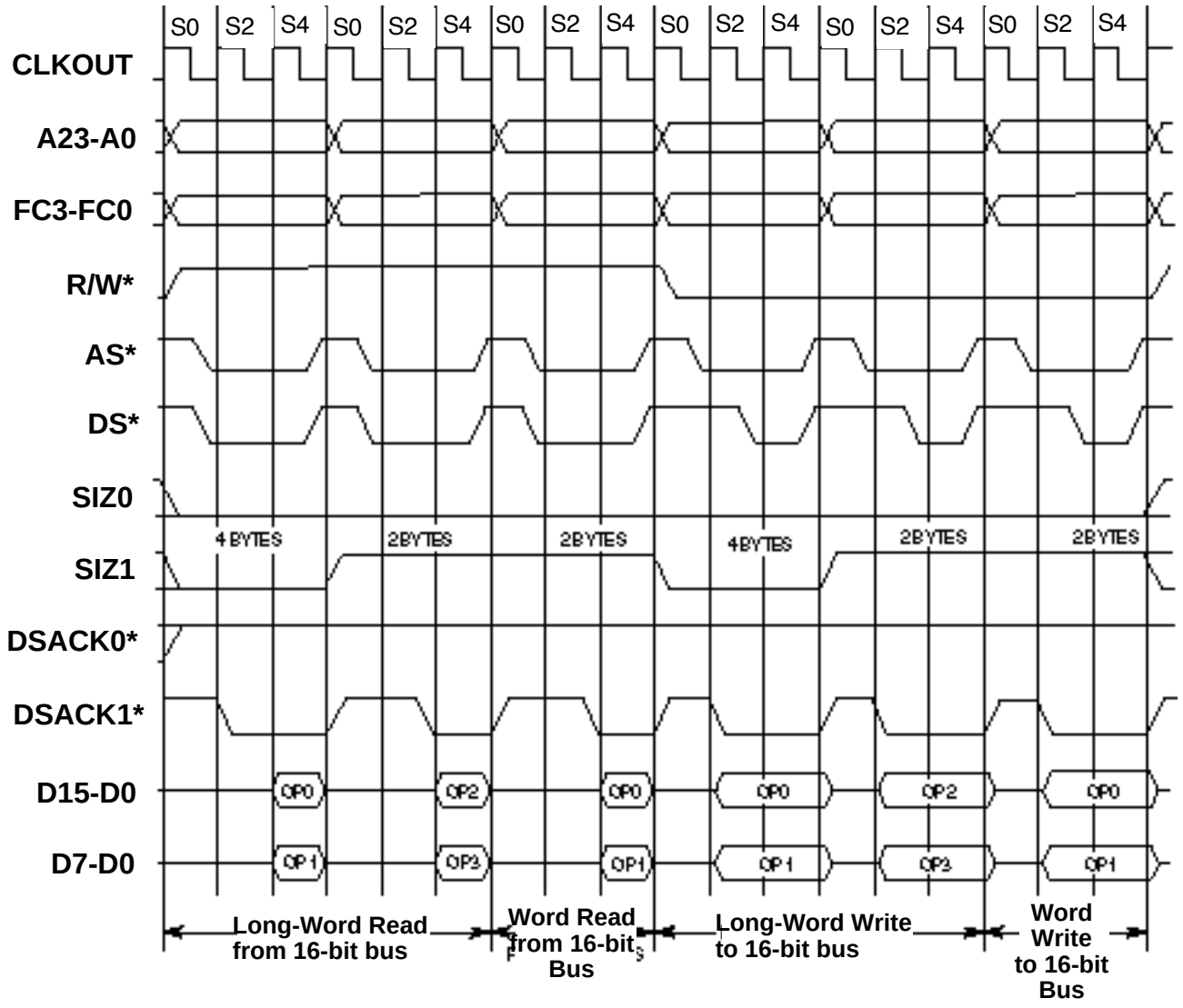
- 24 external address lines can address up to 4 Gigabytes of memory; 16 data lines available
- Option of using both 68300 & MC68000 bus interface
- Bus Controller allows flexible data transfers
  - Byte, word, or longword transfers are possible
  - Dynamic bus sizing
  - Synchronous & Asynchronous transfers
    - » Synchronous transfers are 3 clock cycles
  - Fast Termination mode generates 2 clock accesses
- External function code pins indicate space type

Function Code Bits				Address Spaces
3	2	1	0	
0	0	0	0	Reserved (Motorola)
0	0	0	1	User Data Space
0	0	1	0	User Program Space
0	0	1	1	Reserved (User)
0	1	0	0	Reserved (Motorola)
0	1	0	1	Supervisor Data Space
0	1	1	0	Supervisor Program Space
0	1	1	1	Supervisor CPU Space
1	x	x	x	DMA Space

68341: Bus Operations

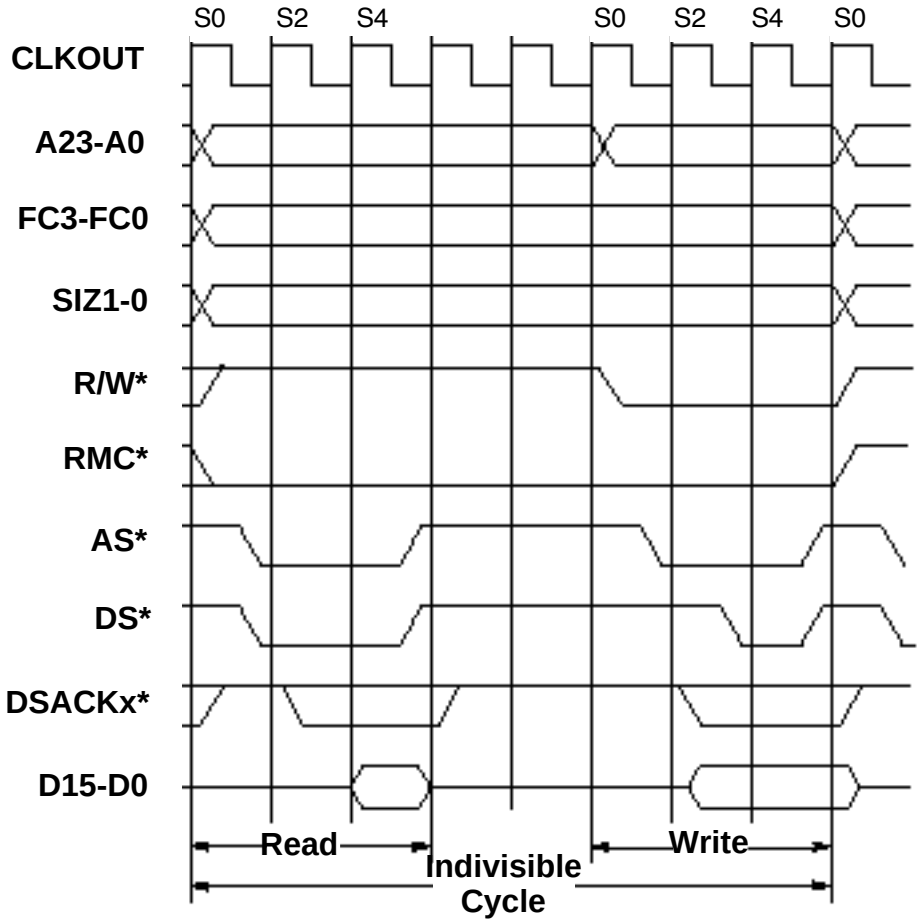
- 68341 efficiently handles exception operations:
  - BERR
  - Retry
  - Halt
  - Double Bus Fault
- Bus arbitration logic allows external masters to control the bus
- Read-Modify-Write Logic is present for multi-processing environments
- Internal cycles can be shown on the external bus through programming Module Configuration Register (MCR)

68341: Bus Operations (Read & Write)



68341: Bus Operations

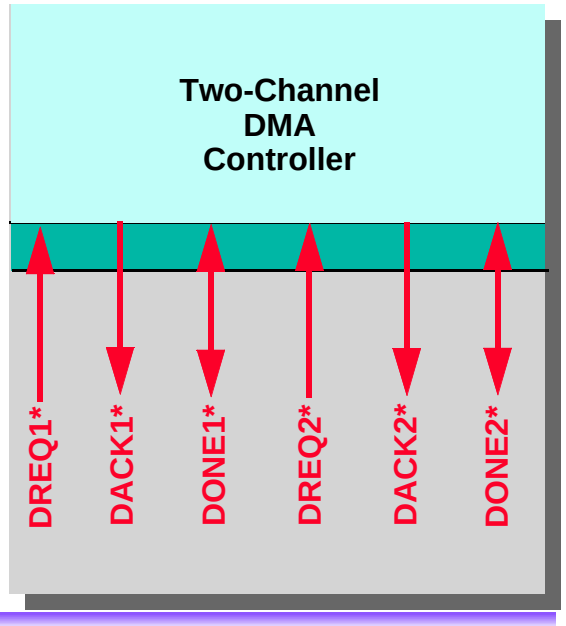
Read-Modify-Write cycles do not acknowledge bus requests or interrupts until both the read and the write cycle are finished



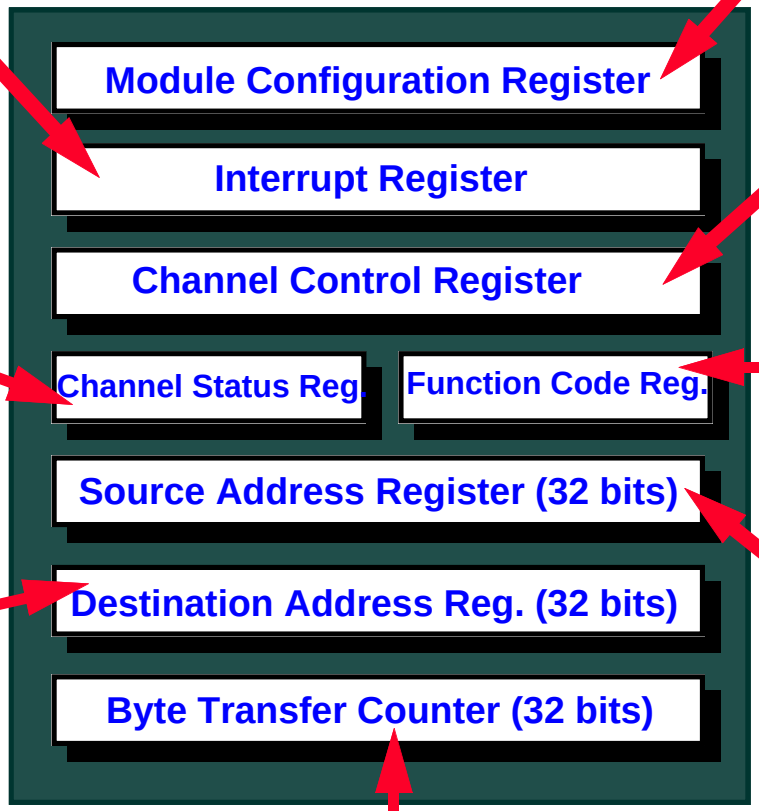
Read-Modify-Write Cycle

68341: DMA Module

- Two-independent fully programmable DMA channels for high speed data transfer
- Single address & Dual Address transfer supported
  - **Single address is only implemented externally**
  - **Dual address transfer supports packing & unpacking**
- Internal cycles allow 25, 50, 75, or 100% bus bandwidth
- External cycles support burst & cycle steal mode
- Transfer rate
  - **25 Mhz: 12.5 Mbytes/s in dual address transfer mode**
    50.0 Mbytes/s in single address mode
  - **16 Mhz: 8.4 Mbytes/s in dual address transfer mode**
    33.3 Mbytes/s in single address transfer mode
- Interrupt generation on normal termination, errors, or breakpoints



68341: DMA Module



Controls DMA configuration such as arbitration ID and Interrupt arbitration ID

Contains priority level and interrupt vector number for channel interrupt request

Controls functions of DMA such as when interrupts occur, what mode the part is in, etc.

Contains status of DMA channel

Source & destination codes for channel

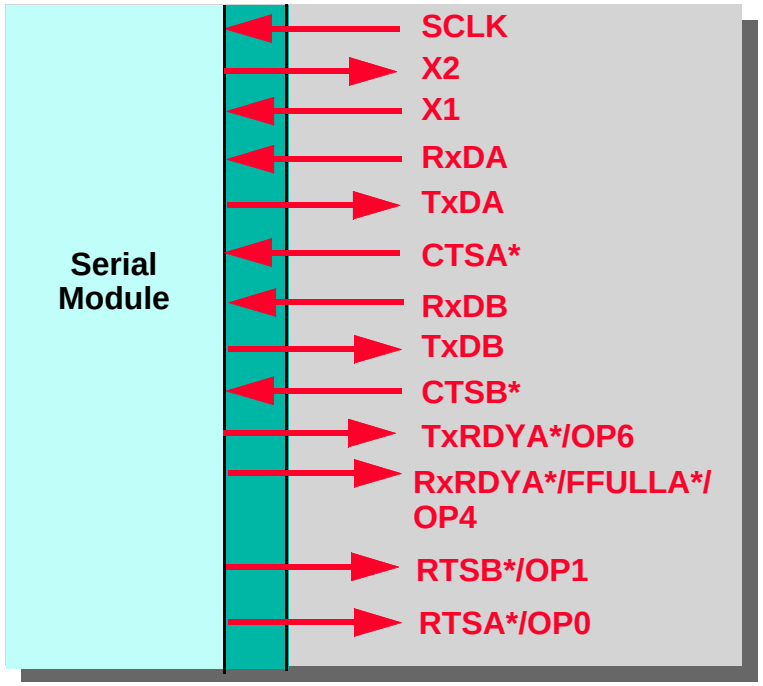
Contains address of source operand used by DMA to access memory or peripheral. Can be incremented or remain constant.

Contains address of destination operand used by DMA to write to memory or peripheral. Can be incremented or remain constant.

Contains the number of bytes left to transfer in a given block.

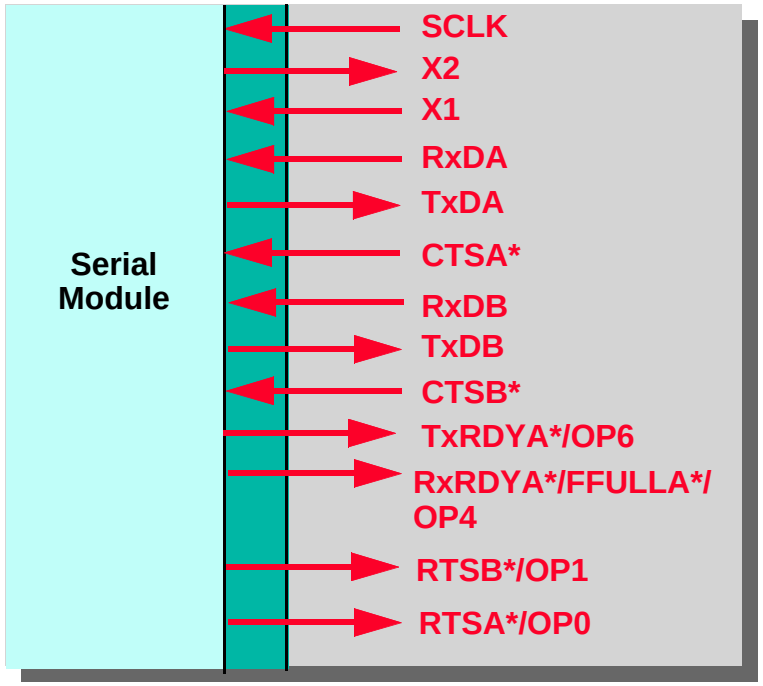
68341: Serial Module

- Two independent, full Duplex Asynchronous/Synchronous Receiver/ Transmitter (DUART) Channels
- Compatible with MC68681/MC2681
- Quadruple-Buffered Receiver
- Double-Buffered Transmitter
- On-chip Crystal Oscillator
- Maximum transfer rate:
  - **1x Mode: 9.8 Mbps@ 25 MHz CLKOUT**
  - **16x Mode: 612 kbps@ 25 MHz CLKOUT**
- Each receiver & transmitter is independently programmable
  - **19 fixed rates from 50 to 76.8 Kbaud**
  - **1x or 16x clock frequency**

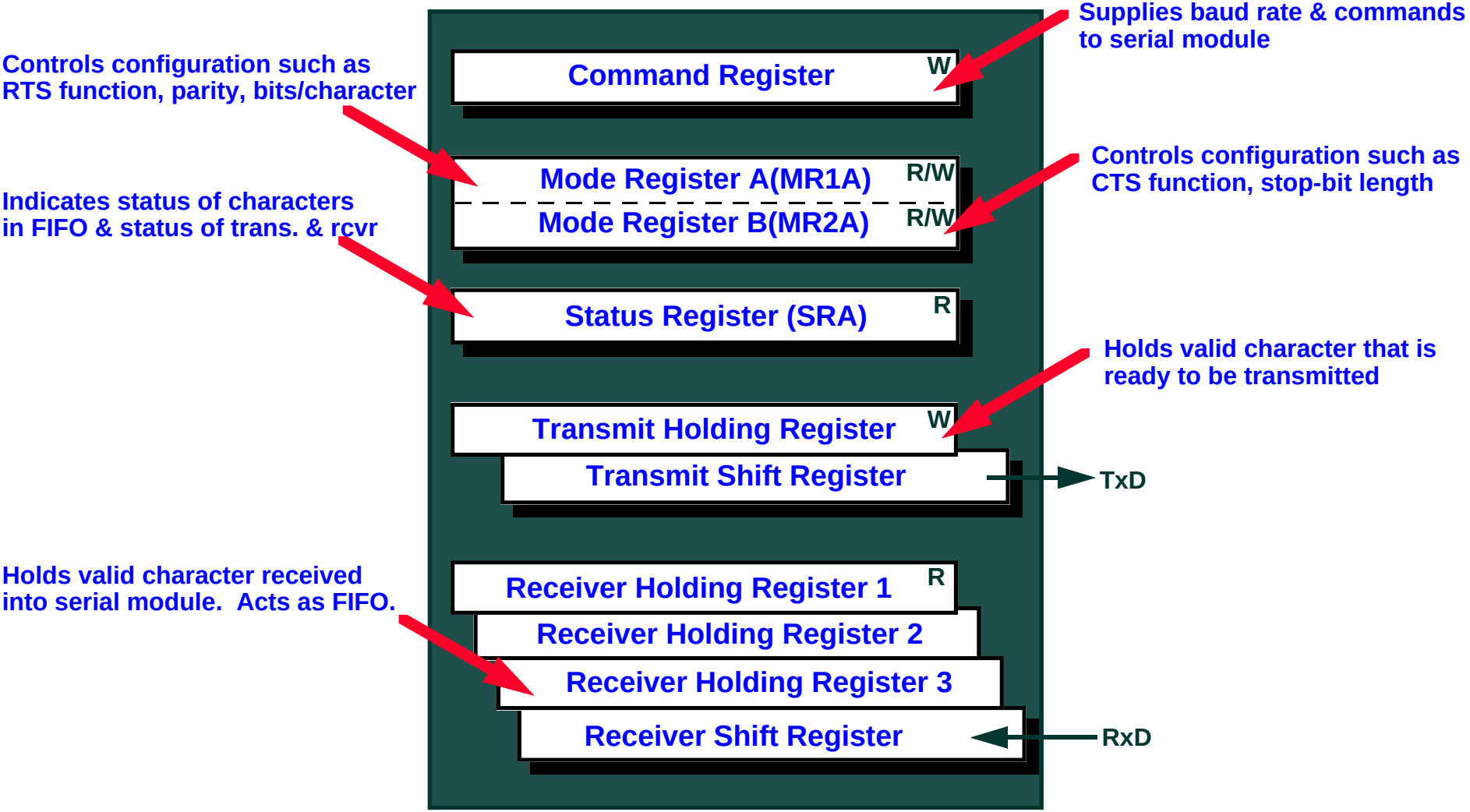


68341: Serial Module

- Seven maskable interrupt conditions
  - Change-of-State on CTSx*
  - Break Condition (either channel)
  - Ready Receive/FIFO Full (either channel)
  - Transmitter Ready (either channel)
- Channel modes for connectivity testing:
  - Automatic Echo
  - Local Loopback
  - Remote Loopback
- Multidrop Mode Supported
- Convenient Break Detection & Generation
- Error Detection:
  - Parity
  - Framing
  - Overrun
- Modem Support

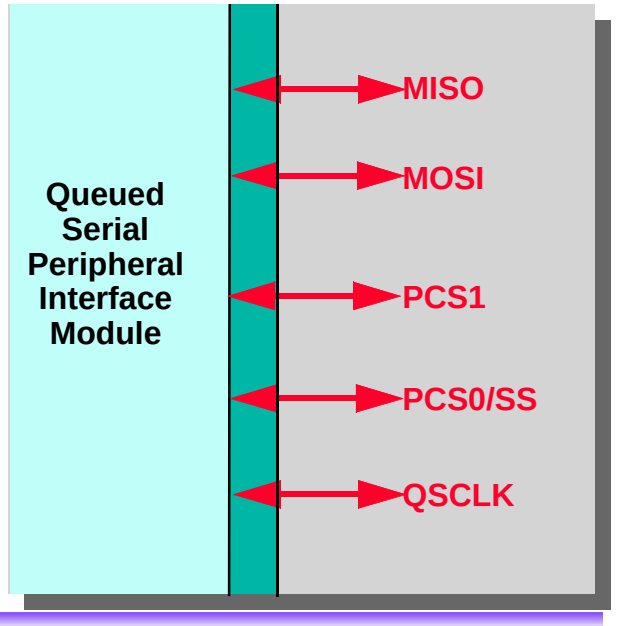


68341: Serial Module

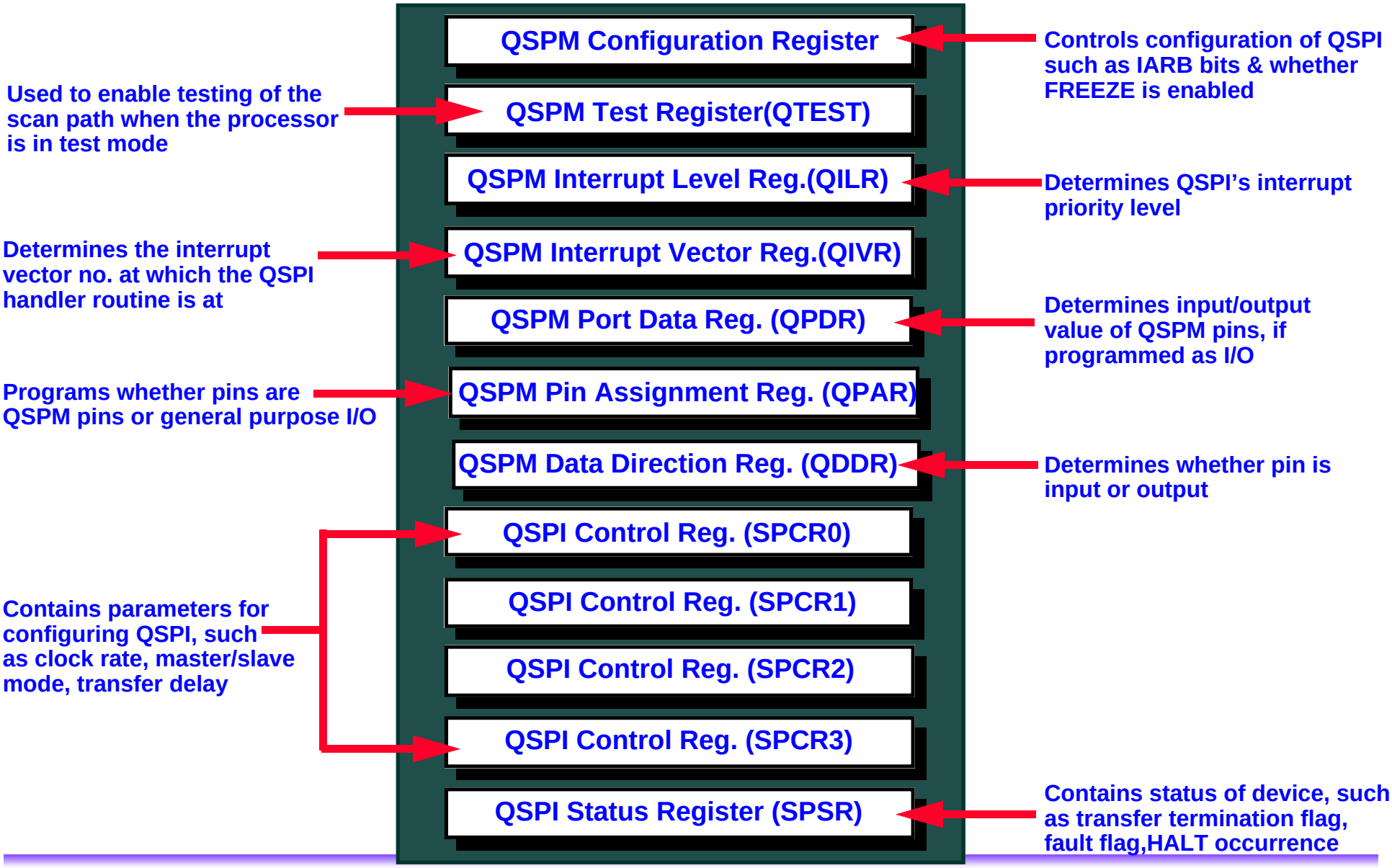


68341: Queued Serial Peripheral Interface Module

- Full duplex, synchronous serial interface to communicate w/ peripherals & microprocessors
  - Queue allows QSPI Module to function without CPU intervention
    - » Queue for receive & transmit data & command control
    - » 80 bytes RAM
    - » Wraparound mode allows continuous execution
  - Can operate in slave or master mode
  - Compatible to 68332 QSM
  - Provides chip selects for peripherals
  - Supports programmable transfer control options:
    - » Transfer length (from 8 to 16 bits) & bit rate
    - » Transfer delay (1 to 500 µs)
    - » Clock polarity & phase
  - Contains status information of QSPI
    - » End-of transmission interrupt
    - » Master-Master fault flag

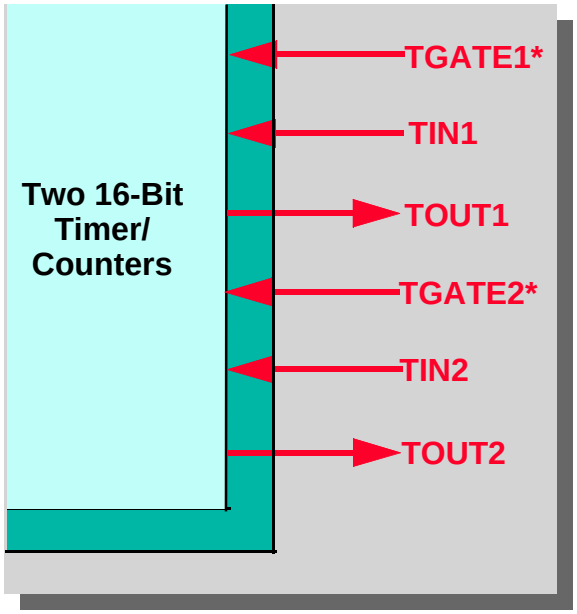


68341: Queued Serial Peripheral Interface Module

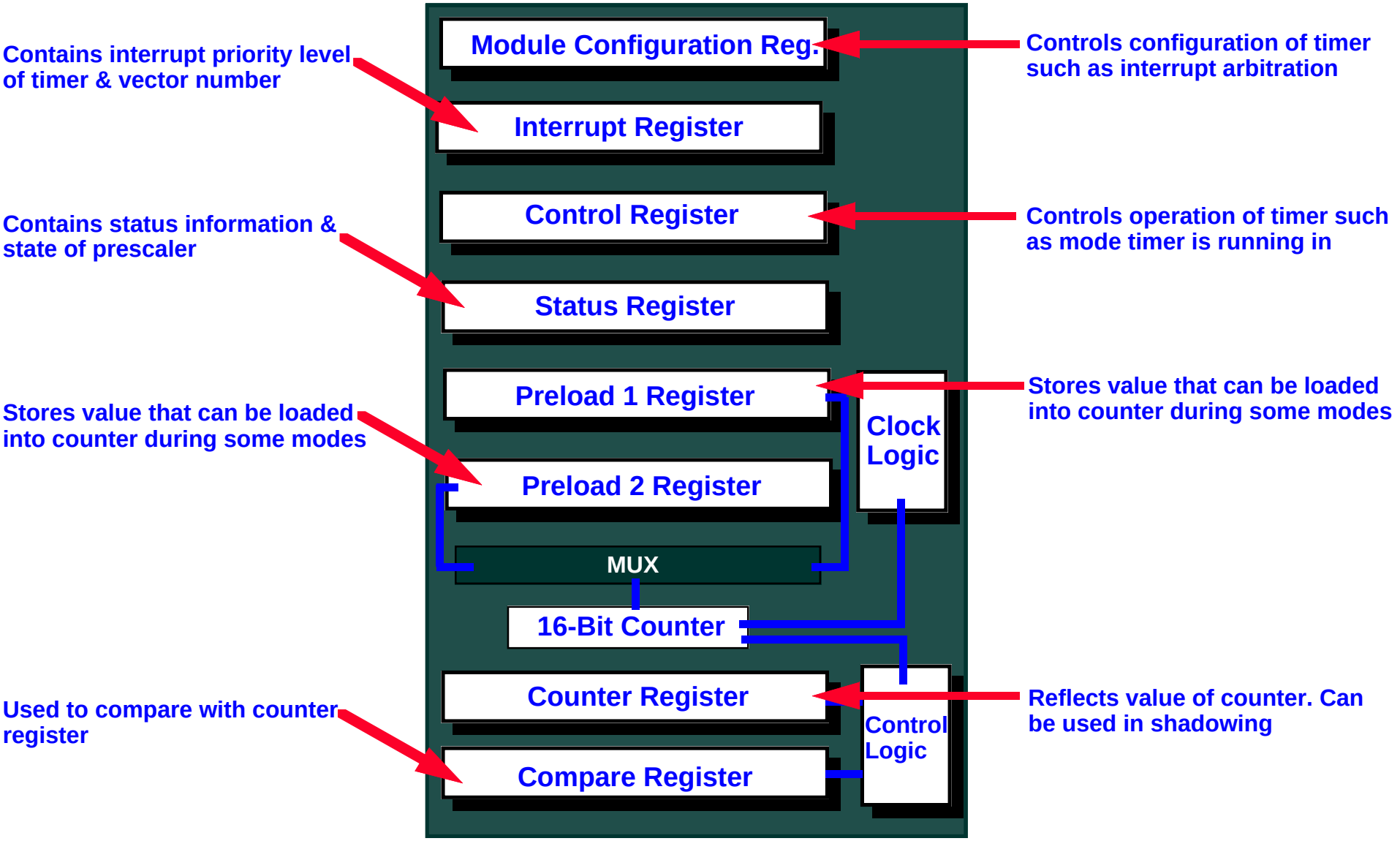


68341: Timer Module

- Two General Purpose Timer/Counters
  - 16-bit countdown counter
  - 8-bit prescaler
  - Multiple Clock Inputs
  - Seven Maskable interrupt conditions based on timer events
  - 80 ns Resolution
- Unique control logic offers numerous operation modes
  - Input Capture/Output Compare
  - Square Wave Generator
  - Variable Duty Cycle Square Wave Generator
  - Variable Width Single Shot Pulse Generator
  - Pulse Width Measurement
  - Period Measurement
  - Timer Bypass
    - » Signals can be programmed as simple I/O ports

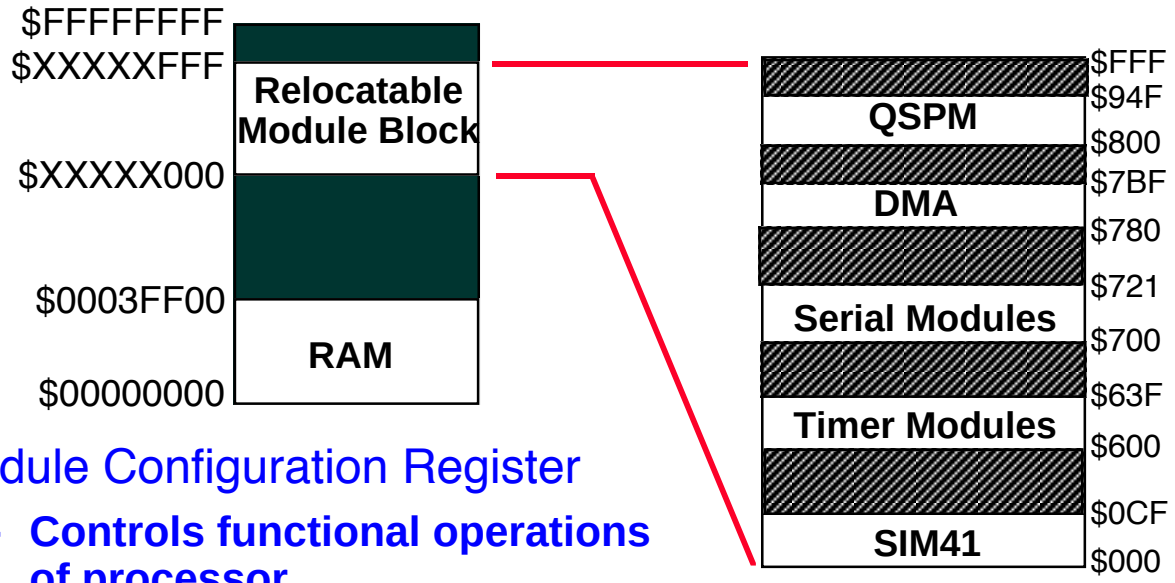


68341: Timer Module



68341: System Integration

- System Configuration & Protection
  - 4K relocatable module register block
    - » **Defined by Module Base Address Register (MBAR at $0003FF00)**

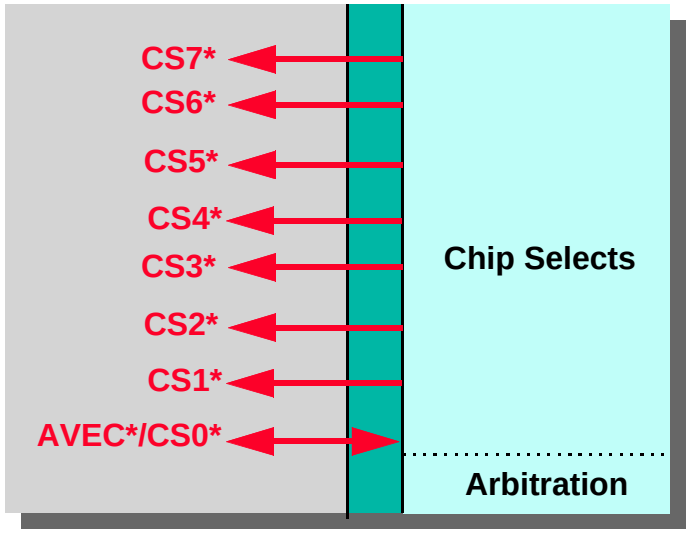


  - Module Configuration Register
    - » **Controls functional operations of processor**
  - Bus Monitor Logic for error checking
    - » **Internal Bus Monitor**
    - » **Double Bus Fault Monitor**
    - » **Spurious Interrupt Monitor**
  - Software Watchdog Timer
    - » **Prevents infinite looping of software**

68341: System Integration

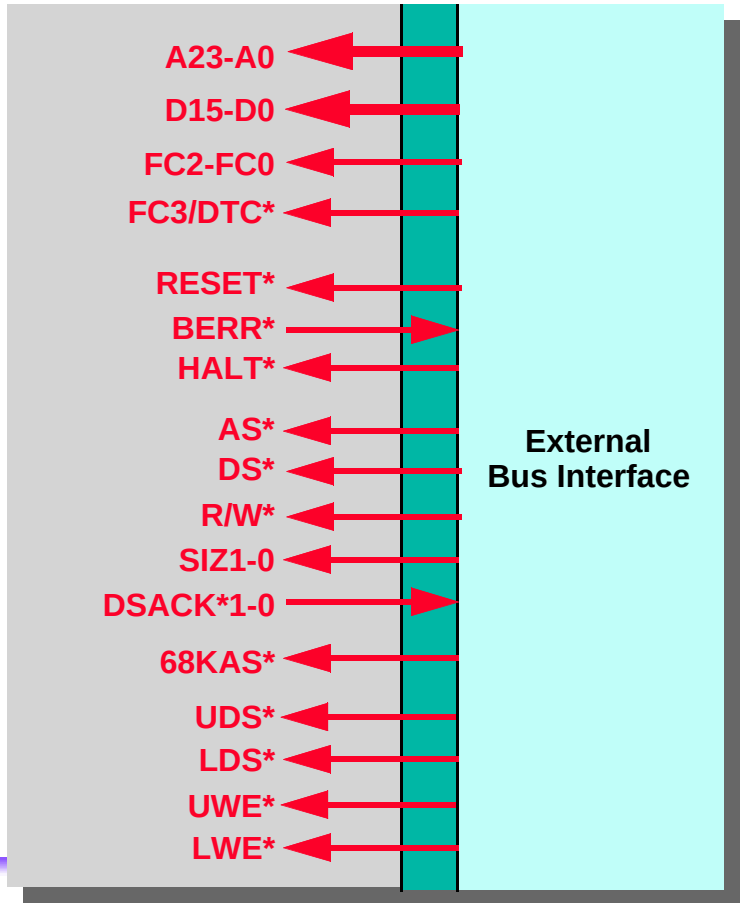
- Periodic Interrupt Timer
  - Can be used in multi-tasking
  - Time can vary from 122µs to 15.94s

- Eight Programmable Chip Selects
  - Can access 256 bytes to 4 Gigabytes in increments of 2^n
  - Capable of selecting 8- & 16- bit ports
  - Control of write protection
  - Option of fast termination in 68300 bus mode
  - Option of pre-programmed wait states (up to 6)
  - Choice of address space type selection (ex. CPU, user data)



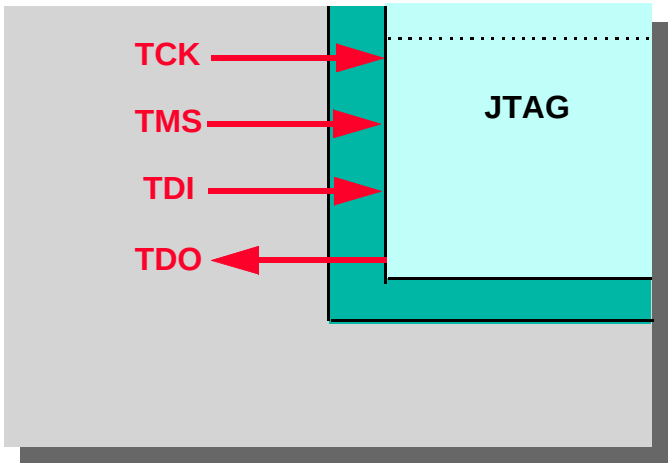
68341: System Integration

- External Bus Interface & Bus Arbitration Logic
  - 31 address lines, 16 data lines, control signals
  - 68300 & M68000 bus support logic
  - External device can gain mastership through three-wire or two-wire arbitration
    - » SIM always has a level seven bus priority
- Real Time Clock (RTC)
  - Ability to keep time and calendar dates
  - Interrupt capability & alarm output
  - Operational from battery supply
- Clock Synthesizer Logic allows 68341 to operate with different clock sources
  - Crystal oscillator
  - External clock
  - External clock w/ PLL activated
  - Limp mode



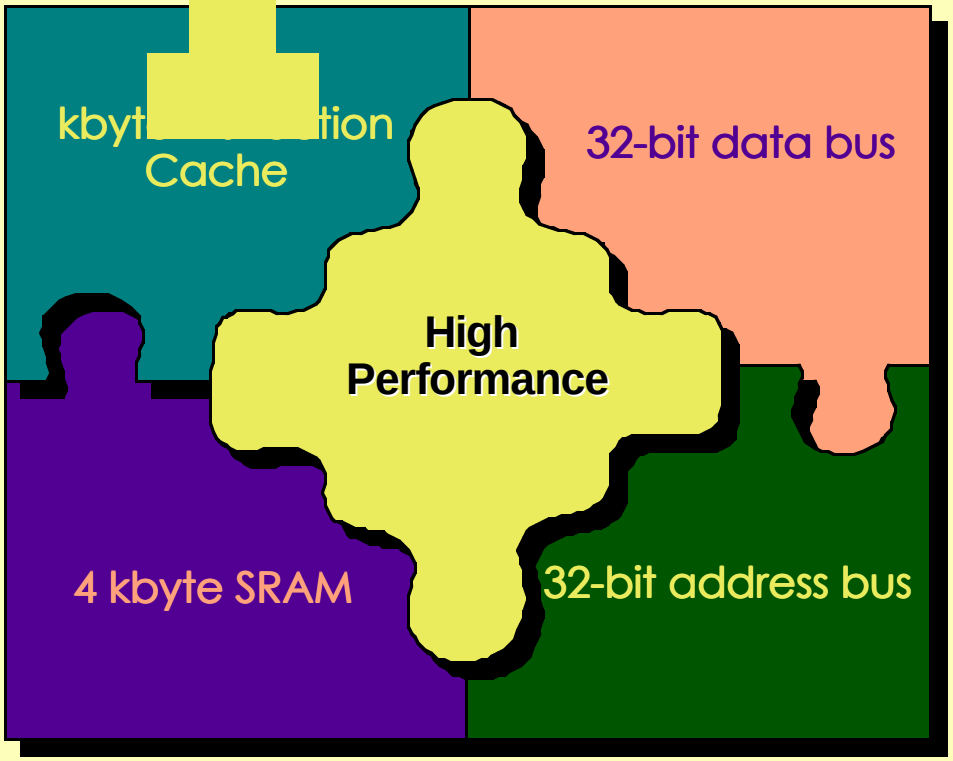
68341: System Integration

- Parallel I/O Port & Interrupt Controller
  - 16 programmable I/O pins
  - Seven multiplexed external interrupt request lines for peripheral devices
  - Option of programming interrupt lines to be edge-sensitive or level-sensitive
- 1149.1 IEEE JTAG



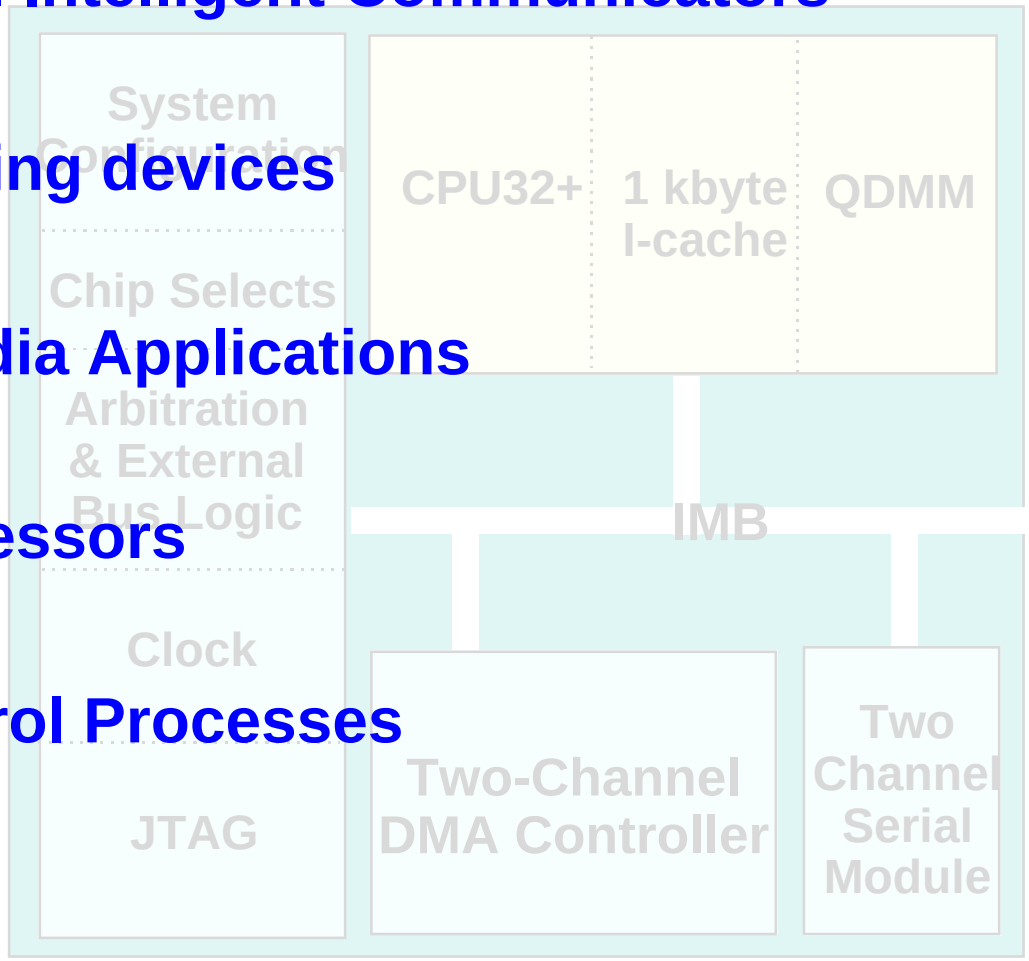
C1349: Advantage

On-chip memory & a l 32-bit architecture combine with integration to create rocessor with high performance.



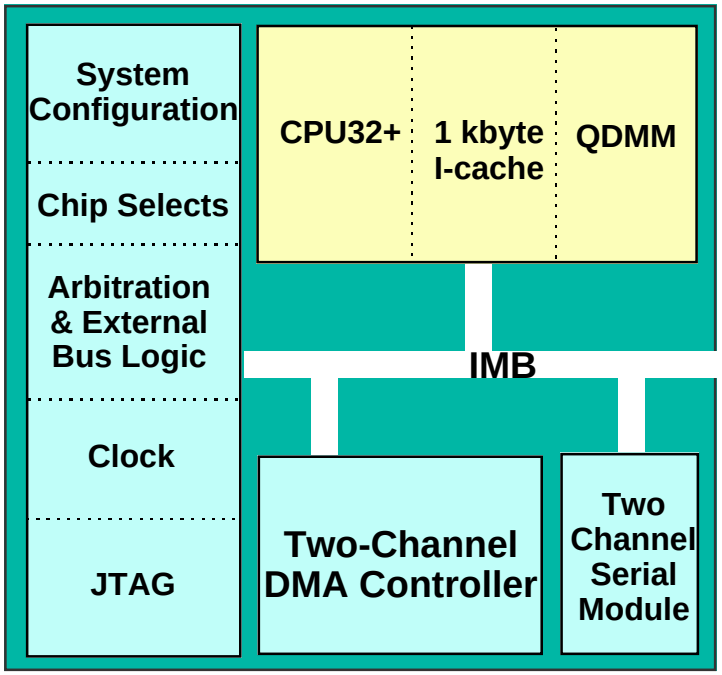
68349: Applications

- Personal Intelligent Communicators
- Networking devices
- Multimedia Applications
- I/O Processors
- RT Control Processes



68349: Features

- CPU32+ core
  - **Full 32-bit extension of CPU32**
- 1 kbyte instruction cache/ 2 kbyte SRAM
- Quad Data Memory Module (QDMM- 4 kbyte SRAM)
- Two-channel DMA module
- DUART compatible with MC68681/MC2681
- System Integration
  - **System Protection & Configuration**
  - **Eight Programmable Chip Selects**
  - **External Bus Interface & Arbitration Logic**
  - **Clock Synthesizer**
  - **16 Programmable I/O Pins**
  - **JTAG**
- 0.8µ HCMOS process
- Offered in 16 & 25 MHz, 3.3V & 5V
- Extended Temperature Available
- Packages: 160- lead FT



68349: Bus Operations

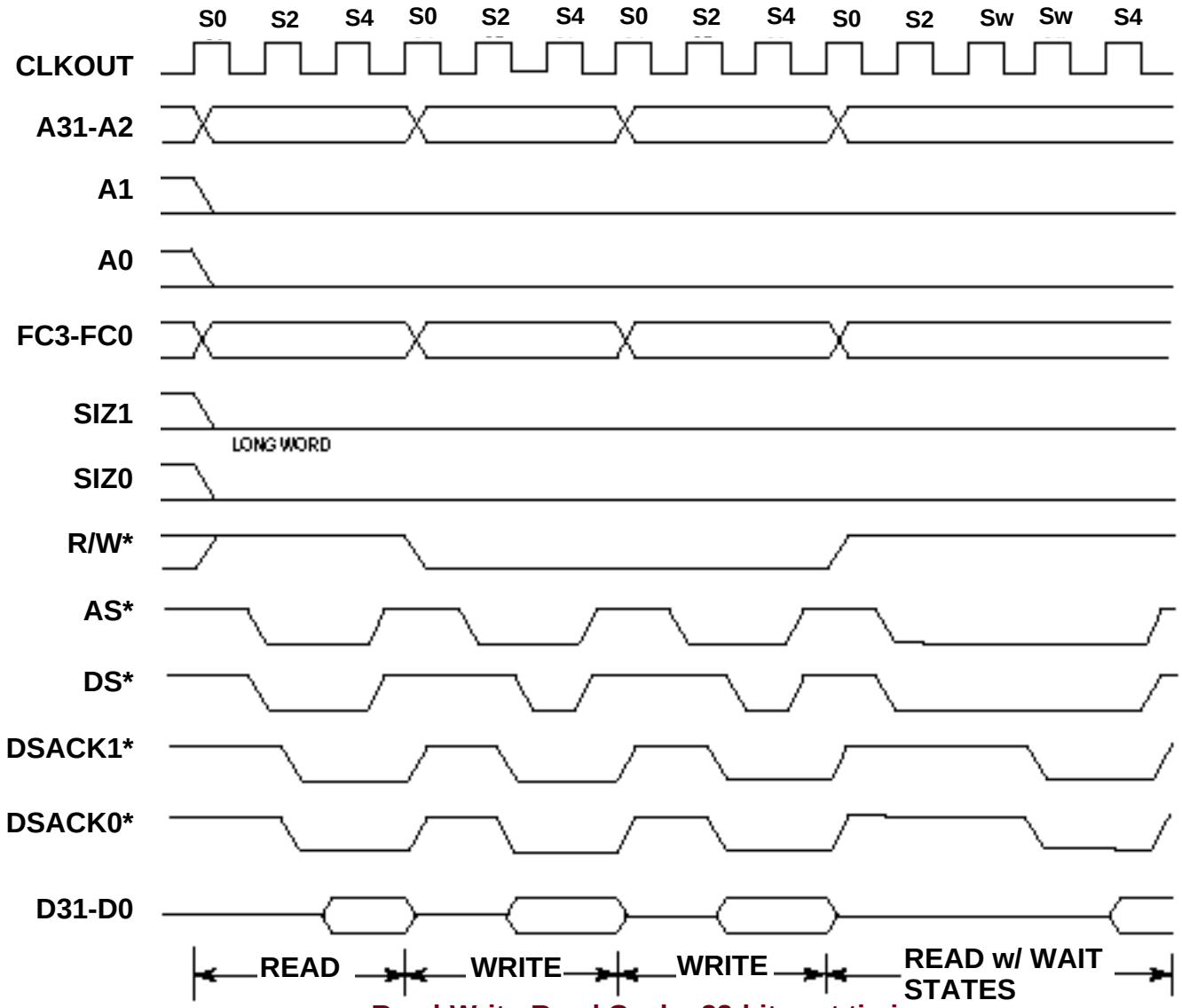
- 32 external address lines can address up to 4 Gigabytes of memory; 32 data lines available
- Bus Controller allows flexible data transfers
  - Byte, word, or longword transfers are possible
  - Dynamic bus sizing
  - Synchronous & Asynchronous transfers
    - » Synchronous transfers are 3 clock cycles
  - Fast Termination mode generates 2 clock accesses
- External function code pins indicate space type

Function Code Bits				Address Spaces
3	2	1	0	
0	0	0	0	Reserved (Motorola)
0	0	0	1	User Data Space
0	0	1	0	User Program Space
0	0	1	1	Reserved (User)
0	1	0	0	Reserved (Motorola)
0	1	0	1	Supervisor Data Space
0	1	1	0	Supervisor Program Space
0	1	1	1	Supervisor CPU Space
1	x	x	x	DMA Space

68349: Bus Operations

- Support of data misalignment
- 68349 efficiently handles exception operations:
  - BERR
  - Retry
  - Halt
  - Double Bus Fault
- Bus arbitration logic allows external masters to control the bus
- Read-Modify-Write Logic is present for multi-processing environments
- Internal cycles can be shown on the external bus through programming Module Configuration Register (MCR)

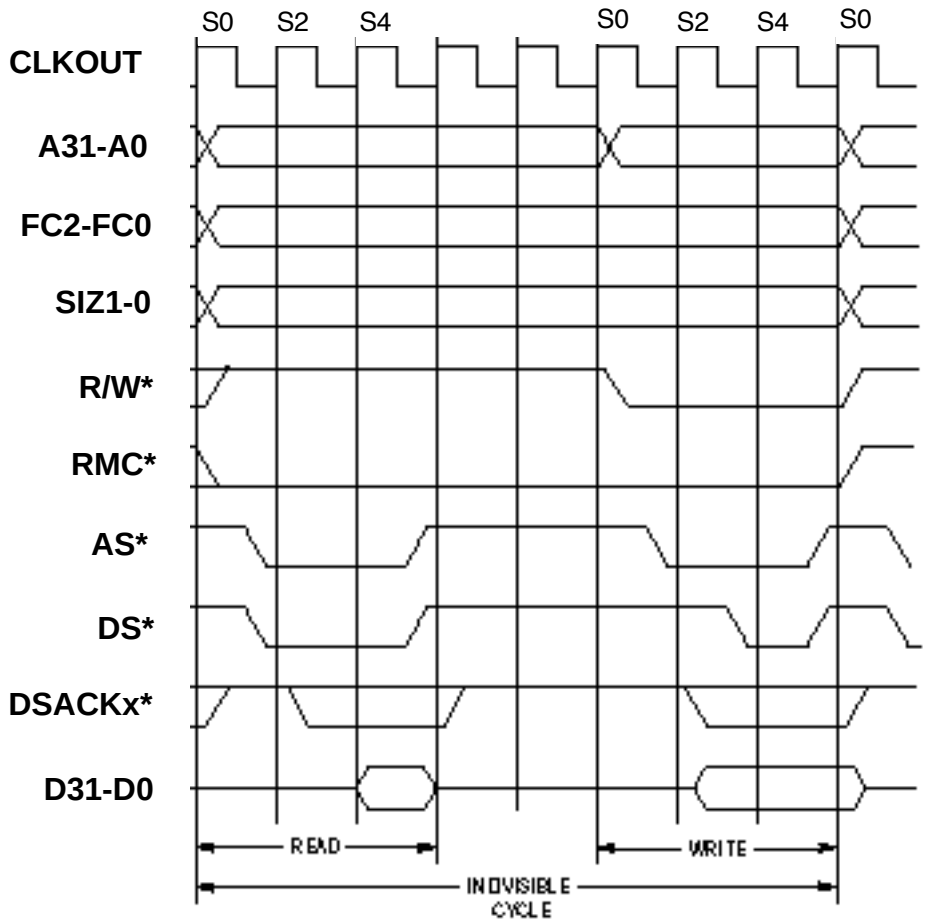
68349: Bus Operations



Read-Write-Read Cycle- 32-bit port timing

68349: Bus Operations

Read-Modify-Write cycles do not acknowledge bus requests or interrupts until both the read and the write cycle are finished



Read-Modify-Write Cycle

68349: Configurable Instruction Cache

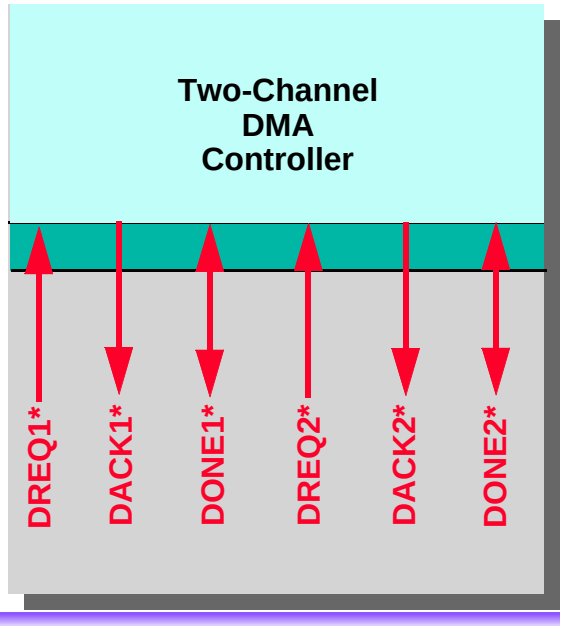
- 1 Kbyte Instruction Cache
  - 4 blocks of 256 byte instruction cache
    - » Acts as direct-mapped cache
    - » Up to 4-way set associative
    - » Ability to freeze contents in each block
  - 4 blocks of 512 byte SRAM
    - » Can store instructions of operands
    - » Relocatable in system address space
- Optimizes supply of instructions to CPU32+
  - Module isolated from IMB allowing other masters to occupy bus
- Reduces power by decreasing no. of off-chip accesses
- Option to program memory on task-by-task basis

68349: Quad Data Memory Module (QDMM)

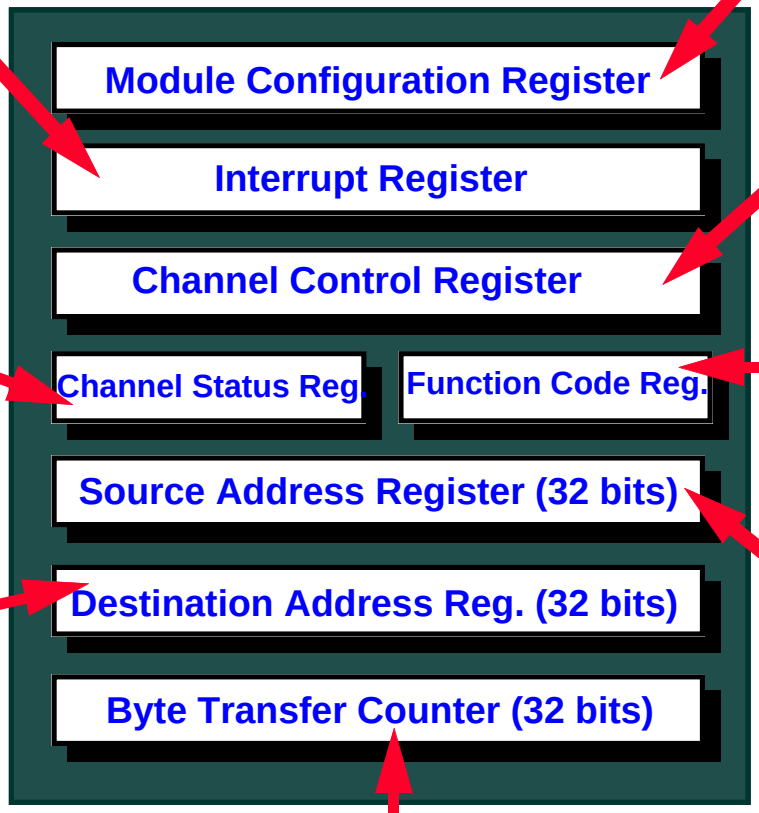
- Dedicated data storage area
  - Four 1 kbyte SRAM blocks
  - Relocatable in system memory space
- Programmable Supervisor or User space
- Optional write-protect
- Variety of uses to programmer:
  - Scratchpad memory
  - Stack caches
  - Buffers for I/O operations
  - Parameter storage

68349: DMA Module

- Two-independent fully programmable DMA channels for high speed data transfer
- Single address & Dual Address transfer supported
  - **Single address is only implemented externally**
  - **Dual address transfer supports packing & unpacking**
- Internal cycles allow 25, 50, 75, or 100% bus bandwidth
- External cycles support burst & cycle steal mode
- Transfer rate
  - **25 Mhz: 12.5 Mbytes/s in dual address transfer mode**
    50.0 Mbytes/s in single address mode
  - **16 Mhz: 8.4 Mbytes/s in dual address transfer mode**
    33.3 Mbytes/s in single address transfer mode
- Interrupt generation on normal termination, errors, or breakpoints



68349: DMA Module



Controls DMA configuration such as arbitration ID and Interrupt arbitration ID

Contains priority level and interrupt vector number for channel interrupt request

Controls functions of DMA such as when interrupts occur, what mode the part is in, etc.

Contains status of DMA channel

Source & destination codes for channel

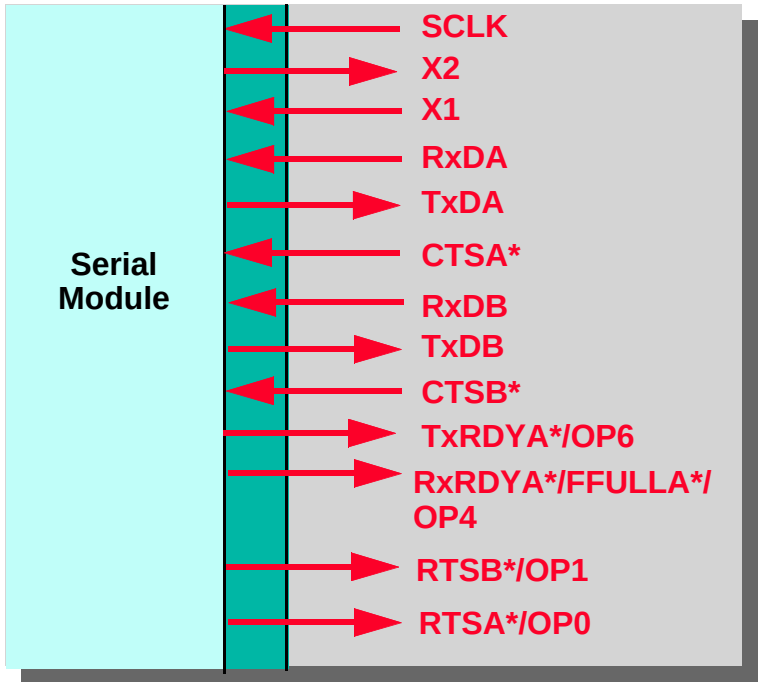
Contains address of source operand used by DMA to access memory or peripheral. Can be incremented or remain constant.

Contains address of destination operand used by DMA to write to memory or peripheral. Can be incremented or remain constant.

Contains the number of bytes left to transfer in a given block.

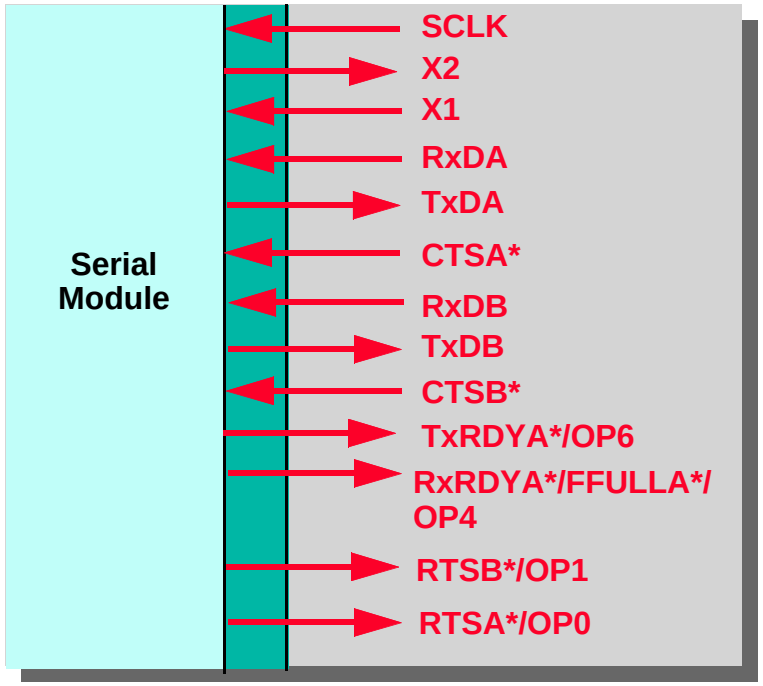
68349: Serial Module

- Two independent, full Duplex Asynchronous/Synchronous Receiver/ Transmitter (DUART) Channels
- Compatible with MC68681/MC2681
- Quadruple-Buffered Receiver
- Double-Buffered Transmitter
- On-chip Crystal Oscillator
- Maximum transfer rate:
  - **1x Mode: 9.8 Mbps@ 25 MHz CLKOUT**
  - **16x Mode: 612 kbps@ 25 MHz CLKOUT**
- Each receiver & transmitter is independently programmable
  - **19 fixed rates from 50 to 76.8 Kbaud**
  - **1x or 16x clock frequency**



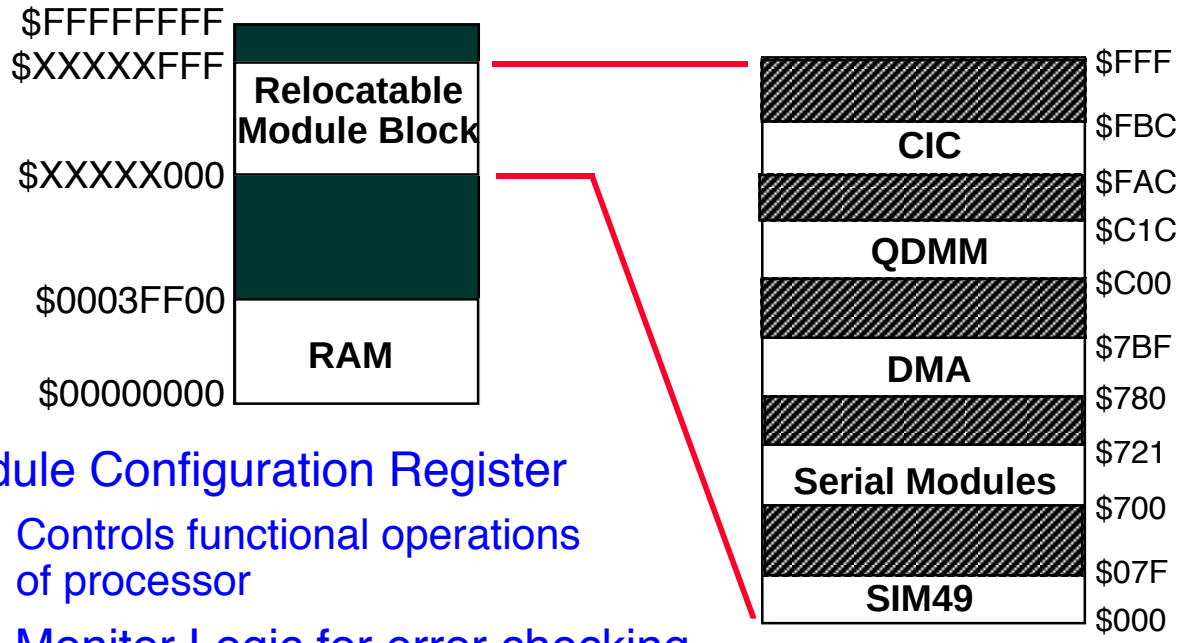
68349: Serial Module

- Seven maskable interrupt conditions
  - Change-of-State on CTSx*
  - Break Condition (either channel)
  - Ready Receive/FIFO Full (either channel)
  - Transmitter Ready (either channel)
- Channel modes for connectivity testing:
  - Automatic Echo
  - Local Loopback
  - Remote Loopback
- Multidrop Mode Supported
- Convenient Break Detection & Generation
- Error Detection:
  - Parity
  - Framing
  - Overrun
- Modem Support



68349: System Integration

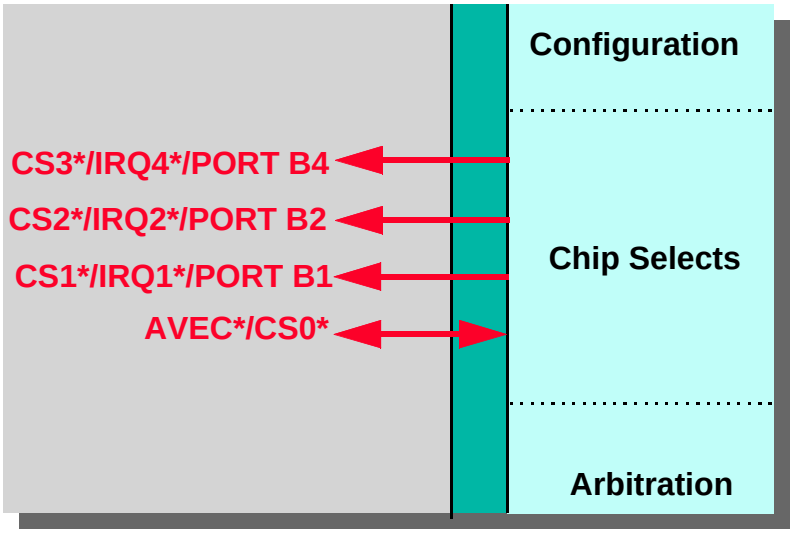
- System Configuration & Protection
  - 4K relocatable module register block
    - » Defined by Module Base Address Register (MBAR at $0003FF00)



  - Module Configuration Register
    - » Controls functional operations of processor
  - Bus Monitor Logic for error checking
    - » Internal Bus Monitor
    - » Double Bus Fault Monitor
    - » Spurious Interrupt Monitor
  - Software Watchdog Timer
    - » Prevents infinite looping of software

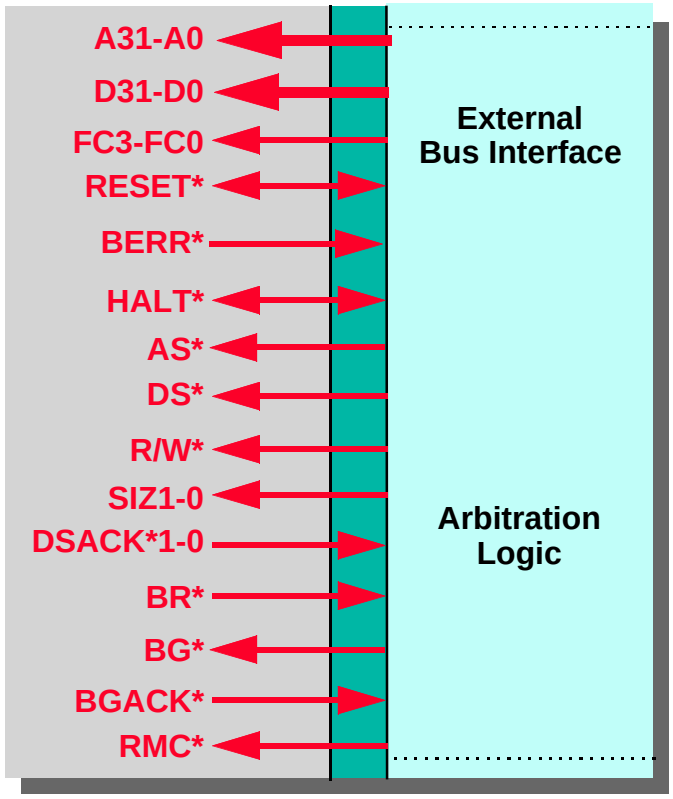
68349: System Integration

- Periodic Interrupt Timer
  - Used in multi-tasking or as Real Time Clock
- Four Programmable Chip Selects
  - Can access 256 bytes to 4 Gigabytes in increments of 2^n
  - Capable of selecting 8-,16-, 32- bit ports
  - Control of write protection
  - Option of fast termination
  - Option of pre-programmed wait states (up to 6)
  - Choice of address space type selection (ex. CPU, user data)



68349: System Integration

- External Bus Interface & Bus Arbitration Logic
  - 32 address lines, 32 data lines, control signals
  - External device can gain mastership through three-wire or two-wire arbitration
    - » SIM always has a level seven bus priority
- Parallel I/O Port & Interrupt Controller
  - 16 programmable I/O pins
  - Seven multiplexed external interrupt request lines for peripheral devices
- Clock Synthesizer Logic allows 68349 to operate with different clock sources
  - Crystal oscillator
  - External clock
  - External clock w/ PLL activated
  - Limp mode
- 1149.1 IEEE JTAG



68349 FAQs

- When are the configuration pins (MODCLK, D29, D30, D31) read during RESET, & what are the setup/hold requirements?
  - These pins are read during the 512 clock period (TCLKOUT periods) at the end of the RESET cycle. The configuration pins should be held active during this time, but they should be released when RESET goes high. There is no requirement that they be held beyond the release of reset.