Marvell® 88E6361

8-Port Switch with 5 Integrated GbE PHYs and 3 2.5 Gbps SERDES

Addendum to 88E6393X/88E6193X/88E6191X Datasheet

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Preface

About this Document

The 88E6361 Datasheet is an addendum to the 88E6393X/88E6193X/88E6191X device information and provides additional or supplementary information for the 88E6361 device.

For complete information about this device, refer to the following documents:

- 88E6393X/88E6193X/88E6191X Switch Functional Specification - Doc. No. MV-S111519-00
- 88E6393X/88E6193X/88E6191X PHY and SERDES Functional Specification - Doc. No. MV-S111464-00
- 88E6393X/88E6193X/88E6191X Rev A0 Release Notes - Doc. No. MV-S302885-00

OVERVIEW

The Marvell® 88E6361 device is a single-chip integration of a 8-port Ethernet switch with five integrated Gigabit Ethernet (GbE) transceivers and three 2.5 Gigabit interfaces. This device supports the latest IEEE 802.1 Audio Video Bridging (AVB) and Time Sensitive Networking (TSN) standards. The devices use these AVB/TSN technologies to identify and reserve network resources for AVB traffic streams and supports precise isochronous streaming capability.

The device contains five 10/100/1000 triple speed Ethernet transceivers (PHYs), three 2.5 Gigabit SERDES interfaces in a 264-pin BGA package.

The three 2.5 Gigabit SERDES support 2500BASE-X, 1000BASE-X, and SGMII.

The device contains one digital interface that supports a combination of RGMII, MII, and RMII interfaces, which shares the same MAC with one SERDES.

The device has a high-speed, non-blocking eight traffic class QoS switch fabric that uses the unique Marvell Dynamic Queue Limit architecture. The QoS architecture switches packets into one of eight traffic class queues based upon Port, IEEE 802.1p, IPv4 Type of Service (TOS) or Differentiated Services (Diff-Serv), IPv6 Traffic Class, 802.1Q VLAN ID, DA MAC address or SA MAC address. The device also contains a high-performance address lookup engine with support for up to 16K active nodes, and a 2 Mbit frame buffer memory. Back-pressure and pause frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion. The MAC units in the devices comply fully with the applicable sections of IEEE 802.3 and support frame sizes up to 10 KB.

The 88E6361 device includes a TCAM-based Policy Control List (PCL) engine that supports 256 rules. The PCL engine can inspect the first 48B of a frame with a full 48B match. Rules can be combined to inspect the first 96B of a frame with a full 96B match. Actions supported include rule based filtering, VLAN assignment, QoS remarking, policy based switching and routing.

The device's RGMII (or MII/RMII) interface supports a direct connection to Management or Router CPUs with integrated MACs. This interface, along with BPDU handling for IEEE 802.1D Spanning Tree Protocol, 802.1w Rapid Spanning Tree, 802.1s Multiple VLAN Spanning Tree, programmable per-port VLAN configurations, 802.1Q and Port States, supports fully managed switches and truly isolated WAN vs. LAN firewall applications. The device supports 4,096 802.1Q VLAN IDs which can be enabled on a per port basis. Three levels of 802.1Q security is supported with error frame trapping and logging.

The PHY units in the device support the latest 802.3az Energy Efficient Ethernet (EEE) standard. They are designed with Marvell cutting-edge mixed-signal processing technology for digital implementation of adaptive equalization and clock data recovery. The device also integrates MDI interface termination resistors into the PHYs. This resistor integration facilitates board layout and reduces board cost by reducing the number of external components. Both the PHY and MAC units in the devices comply fully with the applicable sections of IEEE 802.3, IEEE 802.3u, and IEEE 802.3x standards.

The PHYs also include an integrated Advanced Virtual Cable Tester® (VCT™) enabling fault detection and advanced cable performance monitoring.

The 88E6361 also includes an integrated 200 MHz microprocessor with 256 KB of integrated RAM. The microprocessor's has direct access to all switch registers and its integrated Ethernet controller enables support for Ethernet protocols as well as lightly managed or smart switches.

The device's many operating modes can be configured using SMI (serial management interface - MDC/MDIO) or through the Remote Management Interface. The device also supports a standalone QoS mode or configuration via a low cost serial EEPROM.

Highlighted Features

- Integrated 200 MHz Z80 compatible microprocessor
  - Integrated 256 KB zero wait state RAM
  - Boots via EEPROM, SMI interface, or Remote Management Unit
  - Integrated Ethernet NIC connects directly to switch fabric
- Supports TCAM based L3 Routing
  - 256/128 IPv4/IPv6 LPM
- Supports 802.1 AVB/TSN Standards
  - 802.1AS - Precise Timing Protocol
  - 802.1Qat - Stream Reservation Protocol
  - 802.1Qav - Egress Pacing and Shaping
  - 802.1Qbv - Time Aware Shaping
- Supports 1588v2 over Layer 2 and Layer 4
- Timing Application Interface for AVB/TSN end nodes

- Supports Synchronous Ethernet
- Supports Cut-through switch fabric for low latency applications
- TCAM-based Policy Control List (PCL) Engine
  - Line rate, ingress packet classification and filtering based on packet's first 48 or 96 bytes
  - 256 rules of 48 bytes or 128 rules of 96 bytes with independent bit-by-bit masking capability per rule
  - Allows co-existence of short (48B) and long (96B) rules
  - Flexible actions including filtering, VLAN assignment, QoS remarking, policy based switching and routing
  - Rules can be assigned to any combination of ingress or egress ports
- Supports 802.3az Energy Efficient Ethernet
- Wire speed performance with Maximum Frame size up to 10 kB
- 'Best-in-Class' per port TCP/IP Ingress Rate Limiting along with independent Storm Prevention
  - 5 Ingress Rate Limiting buckets per port, supporting Rate-based and Priority-based rate limiting
- Supports 802.1Qbb Priority Based Flow Control

Features

- Quality of Service support with 8 traffic classes
- QoS determined by Port, IEEE 802.1p tagged frames, IPv4's Type of Service (TOS) & Differentiated Services (DS), IPv6's Traffic Class 802.1Q VID, Destination MAC address, or Source MAC address
- Frame and Queue priority overrides based on DA, SA, VID, Ethertype, BC, IP, PPPoE, ARP, or Snoop
- Strict, Weighted, or mixed mode QoS selectable per port
- Programmable QoS weighting via a 128-entry table
- Wake-on-LAN and Wake of Frame Event Detection
- Remote Management capabilities allow device configuration and readback via Ethernet frames
- Supports 16K MAC addresses and 4K VLAN IDs
- Enhanced 802.1s Per VLAN Spanning Tree supporting up to 64 spanning tree instances
- Per port, programmable MAC hardware address learn limiting
- 3 integrated 2.5 Gigabit interfaces
- 2500BASE-X, 1000BASE-X, SGMII modes
- 5 integrated Gigabit Ethernet PHYs fully compliant with the applicable sections of IEEE802.3 and IEEE802.3u
  - Integrated MDI interface termination resistors
  - Integrated Advanced Virtual Cable Tester® (VCT™) cable diagnostic feature
- RGMII/MII/RMII interface supporting 1.8V, 2.5V or 3.3V I/O, which shares the same MAC with one SERDES interface
- 25 MHz XTAL or LVDS clock source
- Supports 2-Wire EEPROMs for configuration
  - 32 Kbit to 512 Kbit densities supported
  - Able to program attached EEPROMs to save configurations
- 15 x 15 mm 264-pin TFBGA package

Applications

- Gigabit Ethernet switch with five 1000BASE-T LAN ports and one or more 2.5 Gigabit uplink

Table 1 shows the 88E6361 device features.

Table 1: 88E6361 Device Features

		88E6361
Features	# GE PHYs	5
	# RGMII/MII/RMII	1 (Shared)
	1000BASE-X/SGMII/2.5G SERDES	3
	Packet Buffer Memory	2 Mbit
	Jumbo Frame Support	10K Bytes
	# MAC Addresses	16K
	Link Aggregation (LAG/Port Trunking	Yes
QoS	Queues per Port	8
	802.1p, Port, TOS/DS, IPv6 TC, MAC	Yes
	Programmable Weighting	Yes
VLAN	Port-based VLANs	Yes
	802.1Q VLANs	4096
	Double Tagging (Q in Q)	Yes
L3	LPM Entries	256
Mgmt	Wake On LAN / Wake On Frame	Yes
	Remote Mgmt/Ethertype DSA	Yes
	Layer 2 PCLs	Yes
	TCAM	Yes
	802.1D/s/w Spanning Tree	Yes
	802.1X Port & MAC Authentication	Yes
	Port Mirroring	Yes
	IGMP/MLD Snooping	Yes
TSN	802.1AS / Qat / Qav / 1588v2	Yes
	802.1Qbv	Yes
	Timing App I/F (TAI)	Yes
Other	Integrated Management Processor	Yes
	Synchronous Ethernet	Yes
	Cut Through Switch Fabric	Yes
	Ingress Rate Limiting Resources	8/port
	Package	264-Pin TFBGA

Device Identification

The 88E6361 device can be identified in software by reading a value of 0x261 from the Switch Identification Register at Port Register 0x03, bits 15:4 as noted in Table 2.

Table 2: Switch Identifier Register
Offset: 0x03 or decimal 3 – Port

Bits	Field	Type	Description
15:4	Product Num	RO	Product Number or identifier. The product number is: 0x261 for the 88E6361 device
3:0	Rev	RO	Revision Identifier. The initial version of the devices has a Rev of 0x0 (Rev 0x0 of the device). This Rev field may change at any time. Please contact Marvell® FAE's for current information on the device revision identifier.

Figure 1: 88E6361 Block Diagram

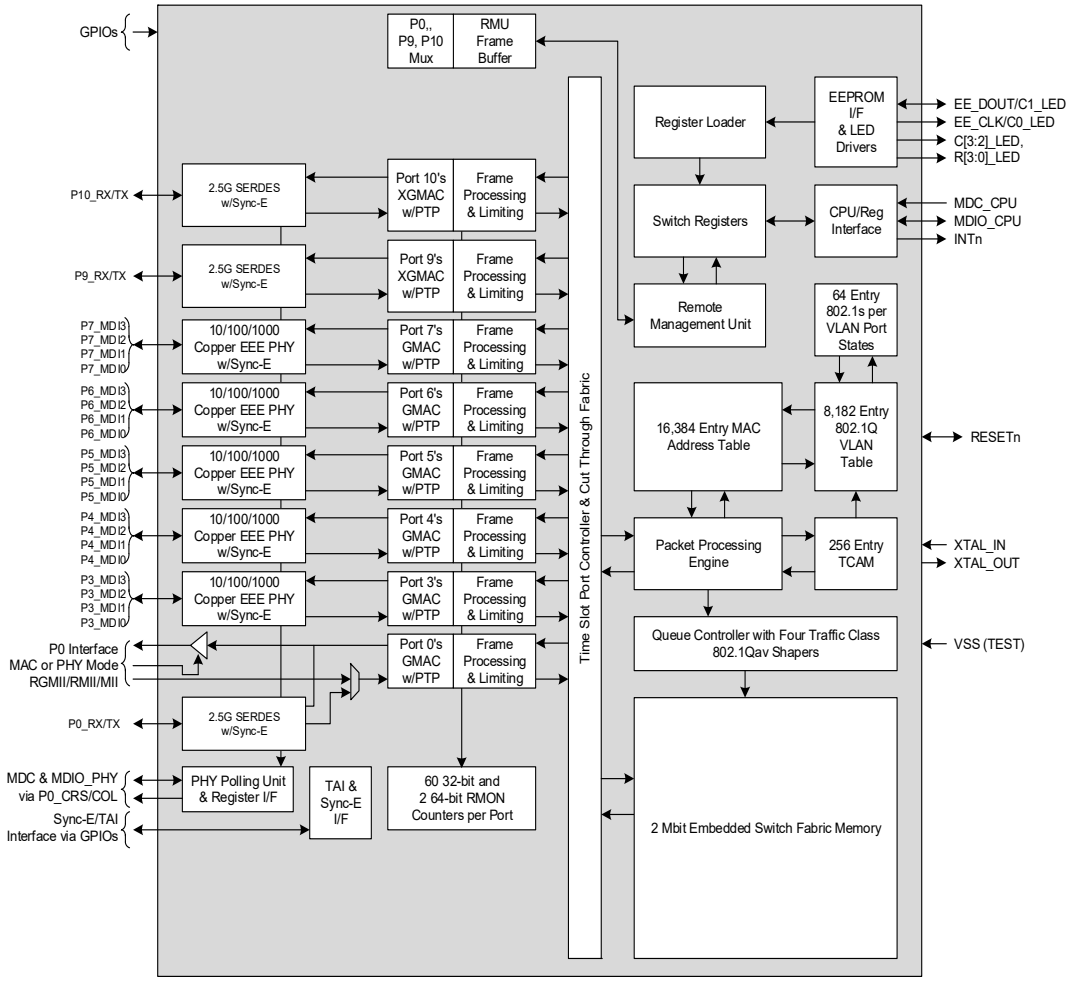


Table of Contents

List of Tables

List of Figures

1 Signal Description

1.1 Pin Description

1.1.1 Pin Map

Due to the large number of pins, the TFBGA package is depicted graphically over two facing pages.

	1	2	3	4	5	6	7	8	9	
A	VSS	P4_MDIN[1]	P4_MDIP[0]	P3_MDIN[3]	P3_MDIP[2]	P3_MDIN[1]	P3_MDIP[0]	DNC	DNC	A
B	VSS	P4_MDIP[1]	P4_MDIN[0]	P3_MDIP[3]	P3_MDIN[2]	P3_MDIP[1]	P3_MDIN[0]	DNC	DNC	B
C	P4_MDIP[2]	P4_MDIN[2]	VSS	P3_P4_ AVDD33	P3_P4_ AVDD33	P3_P4_ AVDD15	VSS	VSS	P3_P4_ AVDD33	C
D	P4_MDIN[3]	P4_MDIP[3]	VSS	P3_P4_ AVDD15						D
E	VSS	VSS	VSS	VSS						E
F	C3_LED	C2_LED	EE_DOUT	EE_VDDO		VDD	VSS	VSS	VSS	F
G	EE_CLK	R4_LED	R3_LED	EE_VDDO		VDD	VSS	VSS	VSS	G
H	R2_LED	R1_LED	R0_LED	DNC		VDD	VSS	VSS	VSS	H
J	RESETn	GPIO[12]	GPIO[11]	REFCLK_ SRC		VDD	VSS	VSS	VSS	J
K	P0_OUTD[1]	P0_OUTD[2]	P0_OUTD[3]	P0_VDDO		VDD	VSS	VSS	VSS	K
L	P0_OUTD[0]	P0_OUTEN	P0_ OUTCLK	P0_VDDO		VDD	VSS	VSS	VSS	L
M	P0_INCLK	P0_INDV	P0_IND[0]	VSS		VDD	VSS	VSS	VSS	M
N	P0_IND[1]	P0_IND[2]	P0_IND[3]	VSS		VDD	VSS	VSS	VSS	N
P	P0_CRS	P0_COL	TEST2	VSS						P
R	VSS	VSS	VSS	P5_P7_ AVDD15						R
T	P5_MDIN[0]	P5_MDIP[0]	VSS	P5_P7 AVDD33	P5_P7 AVDD33	P5_P7 AVDD15	VSS	VSS	VSS	T
U	P5_MDIP[1]	P5_MDIN[1]	P5_MDIP[2]	P5_MDIN[3]	P6_MDIP[0]	P6_MDIN[1]	P6_MDIP[2]	P6_MDIN[3]	P7_MDIN[0]	U
V	VSS	VSS	P5_MDIN[2]	P5_MDIP[3]	P6_MDIN[0]	P6_MDIP[1]	P6_MDIN[2]	P6_MDIP[3]	P7_MDIP[0]	V
	1	2	3	4	5	6	7	8	9	

(Top View)

	10	11	12	13	14	15	16	17	18	
A	DNC	DNC	DNC	DNC	DNC	DNC	VSS	SE_SCLK	VSS	**A**
B	DNC	DNC	DNC	DNC	DNC	DNC	VSS	AVDD_XTAL	XTAL_OUT/ REFCLK_N	**B**
C	P3_P4_ AVDD15	VSS	VSS	P3_P4_ AVDD33	P3_P4_ AVDD15	VSS		AVSS_XTAL	XTAL_IN/ REFCLK_P	**C**
D						VSS	VSS	VSS	VSS	**D**
E						VSS	P0_TXN	P0_TXP		**E**
F	VSS	VSS	VSS	VDD		P0_AVDD15	VSS	P0_RXN	P0_RXP	**F**
G	VSS	VSS	VSS	VDD		P0_AVDD15	VSS	VSS	VSS	**G**
H	VSS	VSS	VSS	VDD		VSS	P10_TXN	P10_TXP		**H**
J	VSS	VSS	VSS	VDD		P10_ AVDD15	VSS	P10_RXN	P10_RXP	**J**
K	VSS	VSS	VSS	VDD		P10_ AVDD15	MDIO_ CPU	TEST	VSS	**K**
L	VSS	VSS	VSS	VDD		VDDO_ GPIO	MDC_CPU	GPIO9	GPIO10	**L**
M	VSS	VSS	VSS	VDD		VSS	VSS	VSS	INTn	**M**
N	VSS	VSS	VSS	VDD		VSS	P9_TXN	P9_TXP		**N**
P						P9_AVDD15	VSS	P9_RXN	P9_RXP	**P**
R						P9_AVDD15	VSS	VSS	VSS	**R**
T	P5_P7 AVDD33	P5_P7 AVDD15	VSS	P5_P7 AVDD33	P5_P7 AVDD15	VSS	AVDD_ COM	TSTPT	RSET	**T**
U	P7_MDIP[1]	P7_MDIN[2]	P7_MDIP[3]	DNC	DNC	DNC	DNC	HSDACN	HSDACP	**U**
V	P7_MDIN[1]	P7_MDIP[2]	P7_MDIN[3]	DNC	DNC	DNC	DNC	VSS	VSS	**V**
	10	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	

(Top View)

1.1.2 Pin Description

Table 3: Network 1G/2.5G SERDES Interface (Ports 0, 9, 10)

Pin #	Pin Name	Type	Description
J18 P18 F18	P10_RXP P9_RXP P0_RXP	Input	Receiver input – Positive. Px_RXP[x] connects directly to the fiber-optic receiver's positive output or to another device's TXP (Transmitter output – Positive) pins. When directly connecting to another device instead of an SFP, cage capacitor isolation should be used. **NOTE:** Px_RXP[x] must be left floating if not used.
J17 P17 F17	P10_RXN P9_RXN P0_RXN	Input	Receiver input – Negative. Px_RXN[x] connects directly to the fiber-optic receiver's negative output or to another device's TXN (Transmitter output – Negative) pins. When directly connecting to another device instead of an SFP, cage capacitor isolation should be used. **NOTE:** Px_RXN[x] must be left floating if not used.
H17 N17 E17	P10_TXP P9_TXP P0_TXP	Output	Transmitter output – Positive. Px_TXP[x] connects directly to the fiber-optic transmitter's positive input or to another device's RXP (Receiver input – Positive) pins. When directly connecting to another device instead of an SFP, cage capacitor isolation should be used. **NOTE:** Px_TXP[x] must be left floating if not used.
H16 N16 E16	P10_TXN P9_TXN P0_TXN	Output	Transmitter output – Negative. Px_TXN[x] connects directly to the fiber-optic transmitter's negative input or to another device's RXN (Receiver input – Negative) pins. When directly connecting to another device instead of an SFP, cage capacitor isolation should be used. **NOTE:** Px_TXN[x] must be left floating if not used.

Note Connection to non-SFP devices must be AC coupled.

Note This device supports internal terminated media pins. They must be left floating if they are unused.

Table 4: Network 10/100/1000 PHY Interface (Ports 3 to 7)

Pin #	Pin Name	Type	Description
V9 U5 T2 A3 A7 U9 V5 T1 B3 B7	P7_MDIP[0] P6_MDIP[0] P5_MDIP[0] P4_MDIP[0] P3_MDIP[0] P7_MDIN[0] P6_MDIN[0] P5_MDIN[0] P4_MDIN[0] P3_MDIN[0]	Input/Output	Media Dependent Interface [0]. In 1000BASE-T mode in MDI configuration, Px_MDIP/N[0] corresponds to BI_DA±. In MDIX configuration, Px_MDIP/N[0] corresponds to BI_DB±. In 100BASE-TX and 10BASE-T mode in MDI configuration, Px_MDIP/N[0] are used for the transmit pair. In MDIX configuration, Px_MDIP/N[0] are used for the receive pair. Px_MDIP/N[0] must be left floating if not used.
U10 V6 U1 B2 B6 V10 U6 U2 A2 A6	P7_MDIP[1] P6_MDIP[1] P5_MDIP[1] P4_MDIP[1] P3_MDIP[1] P7_MDIN[1] P6_MDIN[1] P5_MDIN[1] P4_MDIN[1] P3_MDIN[1]	Input/Output	Media Dependent Interface [1]. In 1000BASE-T mode in MDI configuration, Px_MDIP/N[1] corresponds to BI_DB±. In MDIX configuration, Px_MDIP/N[1] corresponds to BI_DA±. In 100BASE-TX and 10BASE-T mode in MDI configuration, Px_MDIP/N[1] are used for the receive pair. In MDIX configuration, Px_MDIP/N[1] are used for the transmit pair. Px_MDIP/N[1] must be left floating if not used.
V11 U7 U3 C1 A5 U11 V7 V3 C2 B5	P7_MDIP[2] P6_MDIP[2] P5_MDIP[2] P4_MDIP[2] P3_MDIP[2] P7_MDIN[2] P6_MDIN[2] P5_MDIN[2] P4_MDIN[2] P3_MDIN[2]	Input/Output	Media Dependent Interface [2]. In 1000BASE-T mode in MDI configuration, Px_MDIP/N[2] corresponds to BI_DC±. In MDIX configuration, Px_MDIP/N[2] corresponds to BI_DD±. In 100BASE-TX and 10BASE-T modes, Px_MDIP/N[2] are not used. Px_MDIP/N[2] must be left floating if not used.

Table 4: Network 10/100/1000 PHY Interface (Ports 3 to 7) (Continued)

Pin #	Pin Name	Type	Description
U12 V8 V4 D2 B4 V12 U8 U4 D1 A4	P7_MDIP[3] P6_MDIP[3] P5_MDIP[3] P4_MDIP[3] P3_MDIP[3] P7_MDIN[3] P6_MDIN[3] P5_MDIN[3] P4_MDIN[3] P3_MDIN[3]	Input/Output	Media Dependent Interface [3]. In 1000BASE-T mode in MDI configuration, Px_MDIP/N[3] corresponds to BI_DD±. In MDIX configuration, Px_MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, Px_MDIP/N[3] are not used. Px_MDIP/N[3] must be left floating if not used.

Table 5: Reference, Clock and Reset

Pin #	Pin Name	Type	Description
T18	RSET	Analog	Resistor Current reference. A 4.99 kΩ 1% resistor is placed between the RSET and VSS. This resistor is used to set an internal bias reference current.
C18	XTAL_IN/ REFCLK_P	Input	When REFCLK_SRC is pulled high, this signal is XTAL_IN and is connected to a 25 MHz crystal or oscillator. When REFCLK_SRC is pulled low, this pin becomes REFCLK_P and can be connected to 25 MHz LVDS clock source connected via AC isolation.
B18	XTAL_OUT /REFCLK_N	Output	When REFCLK_SRC is pulled high, this signal is XTAL_OUT and is connected to a 25 MHz crystal. If external oscillator is used, XTAL_OUT must connected with 0.1uF capacitor to ground. When REFCLK_SRC is pulled low, this pin becomes REFCLK_N and can be connected to 25 MHz LVDS clock source connected via AC isolation.
A17	SE_SCLK	Input	Synchronous Ethernet Source Clock. This is a 25 MHz reference clock which can be used as a synchronous clock input from the board or system. This signal must come from a high quality clock conditioning circuit or Synchronous Ethernet PLL. Each PHY, via a PHY register, can select this clock input as its reference clock input instead of using the default XTAL_IN input. SE_SCLK is internally pulled low via a resistor so the pin can be left floating when unused.
J1	RESETn	Input, PU	Hardware reset. Active low. The device is configured during reset. When RESETn is low some configuration pins become inputs and the value seen on these pins is latched on the rising edge of RESETn or sometime after. Other configuration pins are active during RESETn low and become inputs after RESETn rises. These pins latch their configuration data sometime after RESETn rises and then these pins become their defined function. Refer to Section 3.6.1 of the AC Electrical Specifications for Reset and Configuration Timing details.

Table 5: Reference, Clock and Reset (Continued)

Pin #	Pin Name	Type	Description
J4	REFCLK_SRC	Input, PU	Reference Clock Source Selection. 0x0 = Differential mode. Use XTAL_IN (REFCLK_P) and XTAL_OUT (REFCLK_N) as LVDS differential input. 0x1 = XTAL/OSC mode. Use XTAL_IN for 25 MHz XTAL single-ended input. In differential mode, REFCLK_P and REFCLK_N are used as LVDS differential input, the inputs with a 100 Ω differential internal termination resistor and internal ac-coupling. In XTAL/OSC mode, XTAL_IN and XTAL_OUT can connect to external crystal or connect to external oscillator with XTAL_IN. If external oscillator is used, XTAL_OUT must connected with 0.1uF capacitor to ground. REFCLK_SRC should be pulled high for XTAL and single ended clocks, or pulled low for and external LVDS clock.

Table 6: Port Status LEDs

Pin #	Pin Name	Type	Description
G2	R4_LED /P5_LED0 /ADDR[4]n	Typically Output, PU	Parallel multiplexed LED outputs. These active low LED pins directly drive the port's LEDs supporting a range from 1 to 20 LEDs in a multiplexed fashion. In this mode the cathode of each LED connects to these pins through a series current limiting resistor. The anode of each LED connects to one of the Cx_LED pins below. These same pins can be used to directly drive from 1 to 5 LEDs in a non-multiplexed fashion (5 from this set of pins – P[5:1]_LED0). In this mode the cathode of each LED connects to these pins through a series current limiting resistor. The anode of each LED connects to a power source. The LEDs can be configured to display many options (see Section 2.3.1, LED Options, on page 55). Rx_LED are multifunction pins which are used to configure the device after a hardware reset. After reset is asserted, the Rx_LED pins become inputs and the configuration information below is latched 1 ms after the rising edge of RESETn as follows: R4_LED = ADDR[4]n R3_LED = ADDR[3]n R2_LED = ADDR[2]n R1_LED = ADDR[1]n R0_LED = LED_SEL ADDR[4:1]n sets the device's SMI address. Note: The inverted values 'seen' on these CONFIG pins are used as the SMI address[4:1]. ADDR[0] is always 0. If ADDR[4:1]n are all 1's the device is configured to address 0, which places the device in single-chip addressing mode. LED_SEL 1 = Link/Activity w/Separate Speed LED 0 = Link/Activity w/Speed by 3 Color Rx_LED pins are internally pulled high via a resistor so the pins can be left floating when unused. Use a 4.7 kΩ resistor to VSS for a configuration low. **NOTE:** Direct drive LEDs require register settings from the CPU or from an EEPROM.
G3	R3_LED /P4_LED0 /ADDR[3]n		
H1	R2_LED /P3_LED0 /ADDR[2]n		
H2	R1_LED /P2_LED1/ADDR[1]n		
H3	R0_LED /P1_LED0/LED_SEL		

Table 6: Port Status LEDs (Continued)

Pin #	Pin Name	Type	Description
G1	EE_CLK /C0_LED /P6_LED0 /FLOW	Typically Output, PD	Serial EEPROM clock and column 0 for the matrix LEDs. EE_CLK is the serial EEPROM clock reference output by the devices. It is used to shift the external serial EEPROM (if installed) to the next data bit so the default values of the internal registers can be overridden. EE_CLK is a multi-function pin which is also used to connect to the anode of LED column 0 for each row, if used in the multiplexed LED mode (see R[4:0]_LED above). If an EEPROM is not connected, then this pin can be used to directly drive a LED in a non-multiplexed fashion (P6_LED0). If an EEPROM is connected, this pin cannot be used when the LEDs are in a non-multiplexed mode. It is also used to configure the device after a hardware reset. After reset is asserted, EE_CLK becomes an input and the FLOW configuration information below is latched 1 mSec after the rising edge of RESETn as follows: 0x0 = Disable advertisement of full-duplex flow control on all PHYs and enable “forced collision” flow control on all half-duplex ports 0x1 = Enable advertisement of full-duplex flow control on all PHYs and enable “forced collision” flow control on all half-duplex ports Full-duplex flow control requires support from the end station. It is supported on any full-duplex port that has Auto-Negotiation enabled, advertises that it supports Pause (that is, FLOW = 1 at reset), and sees that the end station also supports Pause (from data returned during Auto-Negotiation). Half-duplex flow control is active on all half-duplex ports when enabled. EE_CLK is internally pulled low via a resistor so the pin can be left floating when unused. Use a 4.7 kΩ resistor to EE_VDDO for a configuration high.
F3	EE_DOUT /C1_LED	Input/Output, PU	Serial EEPROM data I/O to/from a 2-wire EEPROM device and Column 1 for the LEDs. EE_DOUT is serial EEPROM data referenced to EE_CLK used to receive and send the EEPROM address/data to/from the external serial EEPROM (if present). 2-wire EEPROMs require that this pin is connected to EE_VDDO through a 2.0 kΩ pull-up resistor. EE_DOUT is internally pulled high via a resistor so the pin can be left floating when unused.

Table 6: Port Status LEDs (Continued)

Pin #	Pin Name	Type	Description
F2	C2_LED /P7_LED0 /S_MODE[0]	Typically Output, PD	C2_LED is a multi-function pin which is used to connect to the anode of LED column 2 for each row, if used in the multiplexed LED mode (see R[4:0]_LED above). This same pin can be used to directly drive an LED in a non-multiplexed fashion (P7_LED0). In this mode the cathode of the LED connects to this pin through a series current limiting resistor. The anode of each LED connects to a power source. It is also used to configure the device after a hardware reset. After reset is asserted, C2_LED becomes an input and the S_MODE[0] configuration information below is latched 1 mSec after the rising edge of RESETn. S_MODE[0] together with S_MODE[1] below are pins to configure the device for sets both Port 9 and Port 10's mode of operation as follows S_MODE[1:0] 00 = 1000BASE-X/SGMII Mode (based on PHYDETECT) 01 = 2500BASE-X Mode 10 = Reserved 11 = Reserved C2_LED is internally pulled low via a resistor so the pin can be left floating when unused.
F1	C3_LED /P8_LED0 /S_MODE[1]	Typically Output, PD	C3_LED is a multi-function pin which is used to connect to the anode of LED column 3 for each row, if used in the multiplexed LED mode (see R[4:0]_LED above). This same pin can be used to directly drive an LED in a non-multiplexed fashion (P8_LED0). In this mode the cathode of the LED connects to this pin through a series current limiting resistor. The anode of each LED connects to a power source. It is also used to configure the device after a hardware reset. After reset is asserted, C3_LED becomes an input and the S_MODE[1] configuration information below is latched 1 mSec after the rising edge of RESETn. S_MODE[1] together with S_MODE[0] above are pins to configure the device for sets both Port 9 and Port 10's mode of operation. S_MODE[1:0] 00 = 1000BASE-X/SGMII Mode (based on PHYDETECT) 01 = 2500BASE-X Mode 10 = Reserved 11 = Reserved C3_LED is internally pulled low via a resistor so the pin can be left floating when unused.

Table 7: Port 0 xMII Receive Interface

Pin #	Pin Name	Type	Description
M1	P0_INCLK /GPIO[1]	Input/Output, PU	Input Clock. P0_INCLK is a reference for INDV and IND. The speed of P0_INCLK is expected to be 125 MHz, 50 MHz, 25 MHz or 2.5 MHz depending upon the speed of the port. In RGMII mode INCLK is used as RXC. P0_INCLK is an output when the xMII is configured in a PHY mode (when the port's Px_MODE = 0x0, or 0x1) or when it is a GPIO pin which is configured to be an output. When the port is in RMII mode or disabled (by its Px_MODE = 0x4, 0x5 or 0x6) this pin becomes GPIO[1]. P0_INCLK is tri-stated during RESETn and it is internally pulled high so the pin can be left floating when unused.
M2	P0_INDV /GPIO[2]	Input, PD	Input Data Valid. Input Data Valid is used to indicate when IND[3:0] (or IND[1:0] where appropriate) contains frame information. P0_INDV must be synchronous to P0_INCLK for all modes except for RMII modes where INDV must be synchronous to OUTCLK. In RGMII mode P0_INDV is used as RX_CTL. When this port is disabled (by its P0_MODE = 0x6) this pin becomes GPIO[2]. P0_INDV is internally pulled low via resistor so the pin can be left floating when unused.
N3 N2 N1 M3	P0_IND[3] /GPIO[6] P0_IND[2] /GPIO[5] P0_IND[1] /GPIO[4] P0_IND[0] /GPIO[3]	Input, PU	Input Data. P0_IND[3:0] (or P0_IND[1:0] in RMII modes) receives the data to be sent into the switch. P0_IND must be synchronous to P0_INCLK for all modes except for RMII modes. In MII, 200BASE, 100BASE and 10BASE modes P0_IND[3:0] are used. In RMII modes only P0_IND[1:0] are used and they must be synchronous to P0_OUTCLK. In RGMII mode P0_IND[3:0] are used as RXD[3:0]. When this port is disabled (by its P0_MODE = 0x6) these pins becomes GPIO[6:3]. When the port is in RMII mode (by its P0_MODE = 0x4 or 0x5) P0_IND[3:2] become GPIO[6:5]. The P0_IND pins are internally pulled high via resistor so the pins can be left floating when unused.

Table 7: Port 0 xMII Receive Interface (Continued)

Pin #	Pin Name	Type	Description
P2	P0_COL /GPIO[7] /I2C_SDA	Input/Output PU	Collision, GPIO[7] or I2C_SDA Collision is used to indicate both transmit and receive are occurring at the same time in half duplex mode. P0_COL is not synchronous to INCLK. P0_COL is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is COL when the port's P0_MODE = 0x1 or 0x2. P0_COL is an output for P0_MODE = 0x1 and it's an input for P0_MODE = 0x2. Alternatively, this pin becomes GPIO[7]. When GPIO[7] is used as I^2C interface, GPIO[7] will function as the I2C_SDA, and GPIO[8] will function as I2C_SCL. P0_COL is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the port's P0_MODE pins at the rising edge of RESETn (during RESETn this pin is an input).
P1	P0_CRS /GPIO[8] /I2C_SCL	Input/Output PU	Carrier Sense, GPIO[8] or I2C_SCL Carrier sense is used to indicate carrier has been detected on the line. P0_CRS is not synchronous to INCLK. P0_CRS is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is CRS when the port's P0_MODE = 0x1 or 0x2. P0_CRS is an output for P0_MODE = 0x1 and it's an input for P0_MODE = 0x2. Alternatively, this pin becomes GPIO[8]. When GPIO[8] is used as I^2C interface, GPIO[8] will function as I2C_SCL while GPIO[7] functions as I2C_SDA. P0_CRS is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the port's P0_MODE pins at the rising edge of RESETn (during RESETn this pin is an input).

Table 8: Port 0 xMII Transmit Interface

Pin #	Pin Name	Type	Description
L2	P0_OUTEN /CPU_MGD	Typically Output, PD	Output Enable. Output enable is used to indicate when P0_OUTD[3:0] or OUTD[1:0] contains frame information. OUTEN is synchronous to OUTCLK in all modes. In RGMII mode OUTEN is used as TX_CTL. P0_OUTEN is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin become an input and the configuration information below is latched at the rising edge of RESETn: CPU_MGD 0 = No CPU Attached 1 = CPU Managed or CPU is Attached When 'CPU is managed' mode is selected, all the ports will be initialized in the Disabled Port State (Switch Port, Offset 0x4 bits 1:0) and the PHYs will be powered down (PHY Register 0_0.11 = 1). This allows software time to boot and fully configure the switch before it allows packets to flow through it. Whenever the switch is used with a CPU, the 'CPU is managed' mode should be used. P0_OUTEN is tri-stated during RESETn. OUTEN is internally pulled low via resistor so the pin can be left floating when unused. Use a 4.7 kΩ resistor to P0_VDDO for a configuration high.
L3	P0_OUTCLK /P0_TXC /GPIO[0]	Input/Output, PU	Output Clock. OUTCLK is a clock reference for OUTEN and OUTD[3:0]. The speed of OUTCLK is 125 MHz, 50 MHz, 25 MHz or 2.5 MHz depending on the speed of the Port. The direction of OUTCLK is a function of the port's Px_MODE (Port offset 0x00). See the C_Mode register bits in Port offset 0x00. In RGMII mode OUTCLK is used as TXC. In RMII mode OUTCLK is used as REFCLK and is always 50 MHz regardless of the speed of the port. When this port is disabled (by its Px_MODE = 0x6) this pin becomes GPIO[0]. OUTCLK is internally pulled high via resistor so the pin can be left floating when unused.

Table 8: Port 0 xMII Transmit Interface (Continued)

Pin #	Pin Name	Type	Description
K3 K2 K1 L1	P0_OUTD[3] /P0_VDDOS P0_OUTD[2] /P0_MODE[2] P0_OUTD[1] /P0_MODE[1] P0_OUTD[0] /P0_MODE[0]	Typically Output, PU	Output Data. P0_OUTD[3:0] (or P0_OUTD[1:0] in RMII Modes) outputs the data to be transmitted from the switch. P0_OUTD is synchronous to OUTCLK in all modes. In RGMII mode P0_OUTD[3:0] are used as TXD[3:0]. In RMII mode P0_OUTD[1:0] are used and P0_OUTD[3:2] are tri-stated. P0_OUTD are multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn as follows: P0_OUTD[3] = P0_VDDOS P0_OUTD[2:0] = P0_MODE[2:0] P0_VDDOS 0 = The P0_VDDO pins are powered by 2.5V 1 = The P0_VDDO pins are powered by 3.3V The device automatically detects 1.8V. When P0_MODE[3:0] is equal to port disable mode (0x6), P0_OUTD pins are tri-stated, and P0 SERDES is power down. P0_MODE[2:0] combine with P0_MODE[3] below for the options as defined in pin P0_MODE[3] definition. P0_OUTD pins are tri-stated during RESETn. P0_OUTD pins are internally pulled high via resistor so the pins can be left floating when unused. Use a 4.7 kΩ resistor to VSS for a configuration low.

Table 9: GPIO

Pin #	Pin Name	Type	Description
L17	GPIO[9] /I2C_SDA /MDIO_PHY /EEE	Input/Output, PU	General Purpose I/O pins, Management Data I/O, Master, or I^2C SDA General Purpose I/O pins. GPIO[9] is general purpose input/output pin whose function, direction, and data is controllable via switch registers When GPIO[9] is used as I^2C interface, GPIO[9] will function as the I2C_SDA, and GPIO[10] will function as I2C_SCL. This device only has one I^2C master. It can be configured to two sets of pins. Software should not enable both sets of GPIO as I^2C at the same time. As a Management Data I/O, in Master mode, this pin is used to transfer management data in and out of the device synchronously to MDC_PHY. This pin requires an external pull-up resistor in the range of 4.7 kΩ to 10 kΩ. This pin is MDIO_PHY while GPIO[10] is MDC_PHY when CPU_MGD is configured to 0x0 at the rising edge of RESETn[1]. When CPU_MGD is pulled low this signal is automatically configured as MDIO_PHY. When CPU_MGD is pulled high, this signal is automatically configured as GPIO[9]. After reset SMI PHY Config can be used to select between GPIO and SMI_PHY operation. GPIO[9] is the multi-function pin used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn: EEE 0 = Disable Energy Efficient Ethernet (EEE) in the PHYs. 1 = Enable Energy Efficient Ethernet (EEE) in the PHYs. When GPIO[9] is used as MDIO_PHY or I2C_SDA, due to the required external pull up resistor, EEE can't configure to zero, but it can be modified by changing internal register. See GPIO_VDDO for the list of pins that are powered by this rail. GPIO[9] pins are internally pulled high via resistor so the pins can be left floating when unused. Use a 4.7 kΩ resistor to VSS for a configuration GPIO[9] low. When GPIO[9] is configured as MDIO_PHY an external pull up resistor is required even if no PHY is connected to prevent false PHY detection.

Table 9: GPIO (Continued)

Pin #	Pin Name	Type	Description
L18	GPIO[10] /I2C_SCL /MDC_PHY /GPIO_VDDOS	Input/Output PU	General Purpose I/O pins, Management Data Clock, Master, or I2C_SCL General Purpose I/O pins. GPIO[10] is general purpose input/output pin whose direction and data is controllable via switch registers When GPIO[10] is used as I^2C interface, GPIO[10] will function as I2C_SCL while GPIO[9] function as I2C_SDA. Multiple pairs of I^2C interfaces can be selected for the I^2C interface. This device has one I^2C master which can be used by two sets of pins. Software should only enable one set of pins at a time. As a Management Data Clock, in Master mode, this pin is the reference clock output for the serial management interface (SMI) that connects to an external SMI slave device, typically external PHYs. By default the frequency of MDC_PHY is 7.8 MHz. The speed can be changed to .98 MHz, 3.91 MHz, or 15.625 MHz via the SMI_SETUP function of the SMI_PHY_COMMAND and SMI_PHY_DATA registers. When CPU_MGD is pulled low at reset, this signal is automatically configured to MDC_PHY. When CPU_MGD is pulled high at reset this signal is automatically configured as GPIO[10]. GPIO[10] is the multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn: GPIO_VDDOS 0 = The GPIO_VDDO pins are powered by 2.5V 1 = The GPIO_VDDO pins are powered by 3.3V The device automatically detects 1.8V. See GPIO_VDDO for the list of pins that are powered by this rail. GPIO[10] pins are internally pulled high via resistor so the pins can be left floating when unused. Use a 4.7 kΩ resistor to VSS for a configuration GPIO[10] low.

Table 9: GPIO (Continued)

Pin #	Pin Name	Type	Description
J3	GPIO[11]/SW_24P	Input/Output PD	General Purpose I/O General Purpose I/O pins. GPIO[11] is general purpose input/output pin whose direction and data is controllable via switch registers GPIO[11] is the multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn: SW_24P 0x0 = Normal operation 0x1 = Configures the device for 3-chip ring topology • Cross-chip 2.5GBASE-R on Port 9, and 10 interfaces. • Force link up for Port 9 and Port 10 • Port Based VLAN between Port 9 and Port 10 • Enable configuration of Learn2All • Message port • Set FrameMode to DSA mode for Port 9 and Port 10 • If FLOW is set to one: • Force flow control “on” for Port 9 & 10. • Set FlowControlMessage to one • Set TagFlowControl to one GPIO[11] pin is internally pulled down via resistor so the pins can be left floating when unused. Use a 4.7 kΩ resistor to P0_VDDO for a configuration GPIO[11] high.

Table 9: GPIO (Continued)

Pin #	Pin Name	Type	Description
J2	GPIO[12]/ P0_MODE[3]	Input/Output PD	General Purpose I/O pins. GPIO[12] is general purpose input/output pin whose direction and data is controllable via switch registers GPIO[12] is the multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn: Port 0 Mode Configuration Bit 3 When: P0_MODE[3:0] sets Port 0's Mode of operation as follows: 0x0 = Full-duplex Only MII MAC Mode 0x1 = MII PHY mode w/output MII CLKs at 2.5, 25 or 50 MHz 0x2 = MII MAC mode w/input MII CLKs 0x3 = Reserved for future use 0x4 = RMII PHY mode w/output P0_OUTCLK at 50 MHz 0x5 = RMII MAC mode w/input P0_OUTCLKs at 50 MHz 0x6 = Port disabled (with its pins tri-stated) 0x7 = RGMII mode 0x8 = Reserved for future use 0x9 = 1000X 0xA = SGMII 0xB - 0xF = Reserved for future use When P0_MODE[3:0] is equal to port disable mode (0x6), P0_OUTD pins above are tri-stated, and P0 SERDES is power down. When P0_MODE[3] is configured to zero, P0_SERDES is also powered down. GPIO[12] pin is internally pulled down via resistor so the pins can be left floating when unused. Use a 4.7 kΩ resistor to P0_VDDO for a setting GPIO[12] high.

1. The CPU_MGD configuration pin is used to determine the initial function of this pin after reset. The pin's function can be modified by changing a register (see Misc Configuration, Index: Index 0x2 of Scratch/Misc. - G2 Offset 0x1A, bit 7).

Table 10: GPIO vs. P0_MODE

P0_MODE	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8 ~0xF
GPIO[0]				√			√		√
GPIO[1]				√	√	√	√		√
GPIO[2]				√			√		√
GPIO[3]				√			√		√
GPIO[4]				√			√		√
GPIO[5]				√	√	√	√		√
GPIO[6]				√	√	√	√		√
GPIO[7]	√			√	√	√	√	√	√
GPIO[8]	√			√	√	√	√	√	√
GPIO[9]	CPU_MGD Configuration								
GPIO[10]	CPU_MGD Configuration								
GPIO[11]	Available in all modes								
GPIO[12]	Available in all modes								

Table 11: System & Register Access

Pin #	Pin Name	Type	Description
L16	MDC_CPU	Input, PU	Management Data Clock, Slave. MDC_CPU is the reference clock input for the serial management interface (SMI) that connects to an external SMI master, typically a CPU. A continuous clock stream is not expected. The maximum frequency supported is 20.0 MHz The CPU's SMI interface is used to access the device's registers but it cannot be used until the device's INTn pin becomes active low. MDC_CPU is internally pulled high via a resistor so it can be left floating when unused. **NOTE:** MDC_CPU is powered by the GPIO_VDDO pins and this pin is 3.3V tolerant if GPIO_VDDO is powered at 2.5V.
K16	MDIO_CPU	Input/Output, PU	Management Data I/O, Slave. MDIO_CPU is used to transfer management data in and out of the device synchronously to MDC_CPU. This pin requires an external pull-up resistor in the range of 4.7 kΩ to 10 kΩ. In Single-chip addressing mode the devices own all addresses on the SMI bus. In Multi-chip addressing mode the device owns only one SMI address and all registers and data structures are accessed indirectly from one device address. The device is in Multi-chip addressing mode when the SMI address 0. The address(es) that are used are selectable using the Rx_LED/ADDRn configuration pins. MDIO_CPU is internally pulled high via a resistor so it can be left floating when unused.
M18	INTn	Input/Open Drain Output	INTn is an active low, open drain pin that is asserted to indicate an unmasked interrupt event occurred. A single external pull-up resistor is required somewhere on this interrupt net for it to go high when it is inactive. The INTn pin can be configured as an interrupt input pin to the integrated microprocessor – see the Link Street Integrated Micro Processor (IMP) Functional Specification document.

Table 12: Test

Pin #	Pin Name	Type	Description
K17	TEST	Input, PD	Test Input. TEST is used to place the chip into its manufacturing test modes. Do not connect this pin to anything other than VSS or improper device operation may result. TEST is internally pulled low via resistor so the pin can be left floating when unused.
P3	TEST2	--	Test. TEST2 is used for manufacturing test and must be pulled high for normal operation.
T17	TSTPT	O	DC Test Point. The TSTPT pin should be left floating.
U18 U17	HSDACP HSDACN	Output	AC Test Points (Positive and Negative) The HSDACP/N outputs are used for AC Test Points. These pins are used to bring out a differential TX_TCLK for IEEE testing and AC Test Points for debug purposes. These pins must be connected to a 50 Ω termination resistor to VSS. These pins can be left floating if not used for IEEE testing, and debug test points are not of importance.

Table 13: Power & Ground

Pin #	Pin Name	Type	Description
K4 L4	P0_VDDO	Power	Power to Port 0's interface. P0_VDDO must be connected to 3.3V for 3.3V I/O, 2.5V for 2.5V I/O or 1.8V for 1.8V I/O (and P0_VDDOS must be configured accordingly – see P0_TXD[3]). 1.8V configuration will be automatically detected by internal voltage sensing logic.
F4 G4	EE_VDDO	Power	Power to LED, EEPROM interface and the RESETn pin. EE_VDDO must be connected to 3.3V for 3.3V I/O.
L15	GPIO_VDDO	Power	Power to GPIO[10:9] interface pins. GPIO_VDDO must be connected to 3.3V for 3.3V I/O, 2.5V for 2.5V I/O or 1.8V for 1.8V I/O (and GPIO_VDDOS must be configured accordingly – see GPIO[10]). 1.8V configuration will be automatically detected by internal voltage sensing logic.
C4 C5 C9 C13	P3_P4_AVDD33	Power	3.3V power to analog core used to power each Gig PHY interfaces.
T4 T5 T10 T13	P5_P7_AVDD33	Power	
C6 C10 C14 D4	P3_P4_AVDD15	Power	1.5V power to analog core used to power each Gig PHY interfaces, the Reference clock and the analog common block.
R4 T6 T11 T14	P5_P7_AVDD15	Power	
T16	AVDD_COM	Power	
B17	AVDD_XTAL	Power	
F15 G15	P0_AVDD15	Power	1.5V power to analog core used to power the SERDES interface.
P15 R15	P9_AVDD15	Power	
J15 K15	P10_AVDD15	Power	

Table 13: Power & Ground (Continued)

Pin #	Pin Name	Type	Description
F6 F13 G6 G13 H6 H13 J6 J13 K6 K13 L6 L13 M6 M13 N6 N13	VDD	Power	1.05V power to digital core.
C17	AVSS_XTAL	Ground	
A1 A16 A18 B1 B16 C3 C7 C8 C11 C12 C15 D3 D15 D16 D17 D18 E1 E2 E3 E4 E15 F7 F8 F9 F10 F11 F12 F16 G7 G8 G9 G10 G11 G12 G16	VSS	Ground	Ground to the device.

Table 13: Power & Ground (Continued)

Pin #	Pin Name	Type	Description
G17 G18 H7 H8 H9 H10 H11 H12 H15 J7 J8 J9 J10 J11 J12 J16 K7 K8 K9 K10 K11 K12 K18 L7 L8 L9 L10 L11 L12 M4 M7 M8 M9 M10 M11 M12 M15 M16 M17 N4 N7 N8 N9 N10 N11 N12 N15 P4 P16 R1 R2 R3	VSS (cont.)	Ground	Ground to the device.

Table 13: Power & Ground (Continued)

Pin #	Pin Name	Type	Description
R16 R17 R18 T3 T7 T8 T9 T12 T15 V1 V2 V17 V18	VSS (cont.)	Ground	Ground to the device.

Table 14: No Connect

Pin #	Pin Name	Type	Description
A8 A9 A10 A11 A12 A13 A14 A15 B8 B9 B10 B11 B12 B13 B14 B15 H4 U13 U14 U15 U16 V13 V14 V15 V16	DNC	NC	Do not connect. Do not connect these pins to anything.

1.2 Pin Assignment Lists

1.2.1 264-pin TFBGA Pin Assignment List

Table 15: 264-pin TFBGA Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
T16	AVDD_COM
B17	AVDD_XTAL
C17	AVSS_XTAL
F2	C2_LED
F1	C3_LED
A8	DNC
A9	DNC
A10	DNC
A11	DNC
A12	DNC
A13	DNC
A14	DNC
A15	DNC
B8	DNC
B9	DNC
B10	DNC
B11	DNC
B12	DNC
B13	DNC
B14	DNC
B15	DNC
H4	DNC
U13	DNC
U14	DNC
U15	DNC
U16	DNC
V13	DNC

Pin Number	Pin Name
V14	DNC
V15	DNC
V16	DNC
G1	EE_CLK
F3	EE_DOUT
F4	EE_VDDO
G4	EE_VDDO
L15	GPIO_VDDO
L17	GPIO[9]
L18	GPIO[10]
J3	GPIO[11]
J2	GPIO[12]
U17	HSDACN
U18	HSDACP
M18	INTn
L16	MDC_CPU
K16	MDIO_CPU
F15	P0_AVDD15
G15	P0_AVDD15
P2	P0_COL
P1	P0_CRS
M1	P0_INCLK
M3	P0_IND[0]
N1	P0_IND[1]
N2	P0_IND[2]
N3	P0_IND[3]
M2	P0_INDV

Pin Number	Pin Name
L3	P0_OUTCLK
L1	P0_OUTD[0]
K1	P0_OUTD[1]
K2	P0_OUTD[2]
K3	P0_OUTD[3]
L2	P0_OUTEN
F17	P0_RXN
F18	P0_RXP
E16	P0_TXN
E17	P0_TXP
K4	P0_VDDO
L4	P0_VDDO
C6	P3_P4_AVDD15
C10	P3_P4_AVDD15
C14	P3_P4_AVDD15
D4	P3_P4_AVDD15
C4	P3_P4_AVDD33
C5	P3_P4_AVDD33
C9	P3_P4_AVDD33
C13	P3_P4_AVDD33
B7	P3_MDIN[0]
A6	P3_MDIN[1]
B5	P3_MDIN[2]
A4	P3_MDIN[3]
A7	P3_MDIP[0]
B6	P3_MDIP[1]
A5	P3_MDIP[2]
B4	P3_MDIP[3]
B3	P4_MDIN[0]
A2	P4_MDIN[1]

Pin Number	Pin Name
C2	P4_MDIN[2]
D1	P4_MDIN[3]
A3	P4_MDIP[0]
B2	P4_MDIP[1]
C1	P4_MDIP[2]
D2	P4_MDIP[3]
T1	P5_MDIN[0]
U2	P5_MDIN[1]
V3	P5_MDIN[2]
U4	P5_MDIN[3]
T2	P5_MDIP[0]
U1	P5_MDIP[1]
U3	P5_MDIP[2]
V4	P5_MDIP[3]
R4	P5_P7_AVDD15
T6	P5_P7_AVDD15
T11	P5_P7_AVDD15
T14	P5_P7_AVDD15
T4	P5_P7_AVDD33
T5	P5_P7_AVDD33
T10	P5_P7_AVDD33
T13	P5_P7_AVDD33
V5	P6_MDIN[0]
U6	P6_MDIN[1]
V7	P6_MDIN[2]
U8	P6_MDIN[3]
U5	P6_MDIP[0]
V6	P6_MDIP[1]
U7	P6_MDIP[2]
V8	P6_MDIP[3]

Pin Number	Pin Name
U9	P7_MDIN[0]
V10	P7_MDIN[1]
U11	P7_MDIN[2]
V12	P7_MDIN[3]
V9	P7_MDIP[0]
U10	P7_MDIP[1]
V11	P7_MDIP[2]
U12	P7_MDIP[3]
P15	P9_AVDD15
R15	P9_AVDD15
P17	P9_RXN
P18	P9_RXP
N16	P9_TXN
N17	P9_TXP
J15	P10_AVDD15
K15	P10_AVDD15
J17	P10_RXN
J18	P10_RXP
H16	P10_TXN
H17	P10_TXP
H3	R0_LED
H2	R1_LED
H1	R2_LED
G3	R3_LED
G2	R4_LED
J4	REFCLK_SRC
J1	RESETn
T18	RSET
A17	SE_SCLK
K17	TEST

Pin Number	Pin Name
P3	TEST2
T17	TSTPT
F6	VDD
F13	VDD
G6	VDD
G13	VDD
H6	VDD
H13	VDD
J6	VDD
J13	VDD
K6	VDD
K13	VDD
L6	VDD
L13	VDD
M6	VDD
M13	VDD
N6	VDD
N13	VDD
A1	VSS
A16	VSS
A18	VSS
B1	VSS
B16	VSS
C3	VSS
C7	VSS
C8	VSS
C11	VSS
C12	VSS
C15	VSS
D3	VSS

Pin Number	Pin Name
D15	VSS
D16	VSS
D17	VSS
D18	VSS
E1	VSS
E2	VSS
E3	VSS
E4	VSS
E15	VSS
F7	VSS
F8	VSS
F9	VSS
F10	VSS
F11	VSS
F12	VSS
F16	VSS
G7	VSS
G8	VSS
G9	VSS
G10	VSS
G11	VSS
G12	VSS
G16	VSS
G17	VSS
G18	VSS
H7	VSS
H8	VSS
H9	VSS
H10	VSS
H11	VSS

Pin Number	Pin Name
H12	VSS
H15	VSS
J7	VSS
J8	VSS
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J16	VSS
K7	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K18	VSS
L7	VSS
L8	VSS
L9	VSS
L10	VSS
L11	VSS
L12	VSS
M4	VSS
M7	VSS
M8	VSS
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M15	VSS

Pin Number	Pin Name
M16	VSS
M17	VSS
N4	VSS
N7	VSS
N8	VSS
N9	VSS
N10	VSS
N11	VSS
N12	VSS
N15	VSS
P4	VSS
P16	VSS
R1	VSS
R2	VSS
R3	VSS
R16	VSS
R17	VSS
R18	VSS
T3	VSS
T7	VSS
T8	VSS
T9	VSS
T12	VSS
T15	VSS
V1	VSS
V2	VSS
V17	VSS
V18	VSS
C18	XTAL_IN/REFCLK_P
B18	XTAL_OUT/REFCLK_N

2 Application Examples

The 88E6361 device is an 8-port Ethernet switch with 5 integrated 1000BASE-T integrated PHYs and an xMII digital interface. In addition, the device has three single lane 2.5G SERDES. Refer to Table 16 for a list of interfaces supported by the 88E6361 device.

Table 16: 88E6361 Device Supported Interfaces

Port	1000BASE-T (Triple Speed)	RGMII	RMII	MII/ 200 Mbps MII	1000BASE-X/ SGMII	2.5GBASE-X
0		x	x	x	x	x
3-7	x					
9					x	x
10					x	x

Note The Remote Management Unit (RMU) can not be used on the Network 10/100/1000 PHY Interface Ports 3-7.

2.1 Port 0 Configuration Options

Port 0 be configured SERDES mode or xMII mode using P0_MODE signals Table 17 indicates all supported Port 0 modes. Some unused Port 0 pins can be used as GPIO signals.

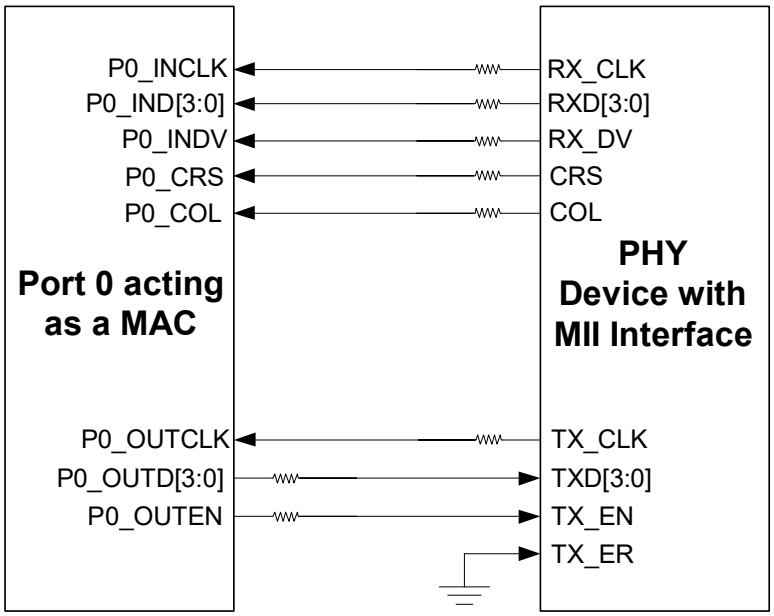
Table 17: Port 0 Configuration Summary

P0_MODE[3:0]	Mode	Notes
0000	Full-duplex MII MAC	COL and CRS are not used
0001	MII PHY	Supports connection to MAC
0010	MII MAC	Supports connection to external PHY type device
0100	RMII PHY	OUTCLK = 50 MHz
0101	RMII MAC	OUTCLK is a 50 MHz input.
0110	Disabled	P0 is not used and pins are tri-stated until configured for other functions via register access.
0111	RGMII	Supports connection to external CPU and PHY
1001	1000BASE-X	Supports connection to an SFP
1010	SGMII	Supports connection to CPU or PHY
1011	2500BASE-X	Supports connection to CPU or PHY
1100	Reserved	Reserved
1101	Reserved	Reserved
1110	Reserved	Reserved

2.1.1 MII MAC Mode

In MII MAC Mode, sometimes called 'Forward MII mode, P0_INCLK and P0_OUTCLK are inputs. The clock provided by the attached device can be from DC-50 MHz. This mode is typically used to support connections to external PHYs. Figure 2 is an example of MII MAC mode when connected to a device emulating a PHY.

Figure 2: MII MAC Mode



.

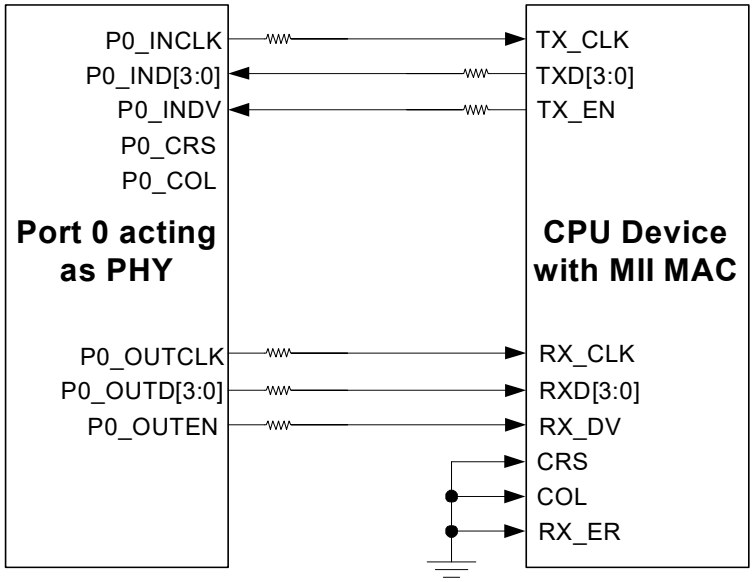
Note If P0_COL and P0_CRS are not used, use a 4.7k pull-down resistor.

Note When configured in MII MAC mode and no clock is provided, the link should be forced down via Switch Port Register 1.

2.1.2 MII PHY Mode

MII PHY Mode is sometimes called ‘Reverse MII’ mode, This mode is typically used to connect the switch port to a CPU. In this mode, P0_INCLK and P0_OUTCLK are both outputs. Figure 3 is an example of using port 0 MII PHY mode. INCLK and OUTCLK output frequency is 2.5 MHz for 10 Mbps, 25 MHz for 100 Mbps and 50 MHz in 200 Mbps mode. P0_COL and P0_CRS are only used when operating in half-duplex mode. RX_ER should be tied to ground because the switch does not generate this signal.

Figure 3: MII PHY Interface Pins



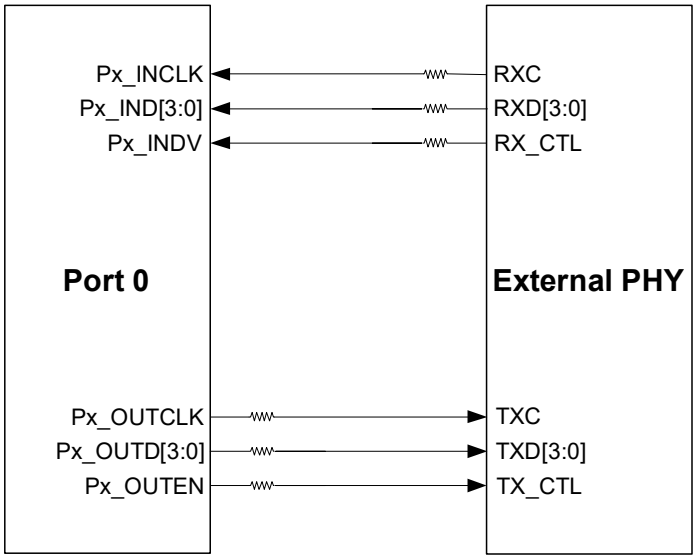
2.1.3 MII 200 Mbps Mode

When Port 0 is configured in MII MAC or MII PHY mode, it can configured to run at 200 Mbps mode. This is done via register access. In 200 Mbps mode, the Tx/Rx clocks run at 50 MHZ.

2.1.4 RGMII Mode

In RGMII Mode, Port 0 emulates a Reduced Gigabit Media Independent Interface (RGMII) so that it can be directly connected to an external RGMII-based Gigabit PHY or CPU. When the RGMII mode is selected, transmit control (P0_OUTEN) is presented on both clock edges of Px_OUTCLK. Receive control (Px_INDV) is presented on both clock edges of Px_INCLK or Px_INCLK. A triple speed interface is supported in RGMII mode (that is, 10, 100 and 1000). When the PHY completes auto-negotiation and brings the link up, the auto-negotiated speed, duplex and flow control information must be moved from the PHY to the MAC so the MAC matches the PHY's link state. This is done automatically by the PPU if the port's PHYDetect bit is set to a one (Port offset 0x00). The default speed and duplex is 1000 Mbps/full-duplex. The speed can be changed at any time with port register 1. RGMII supports an internal transmit and receive delay mechanism which allows for all traces to be routed at the same length without adding additional timing skew in the board layout. RGMII is a symmetrical interface therefore there is no need for separate MAC/PHY emulation. Refer to Figure 4 for RGMII connections.

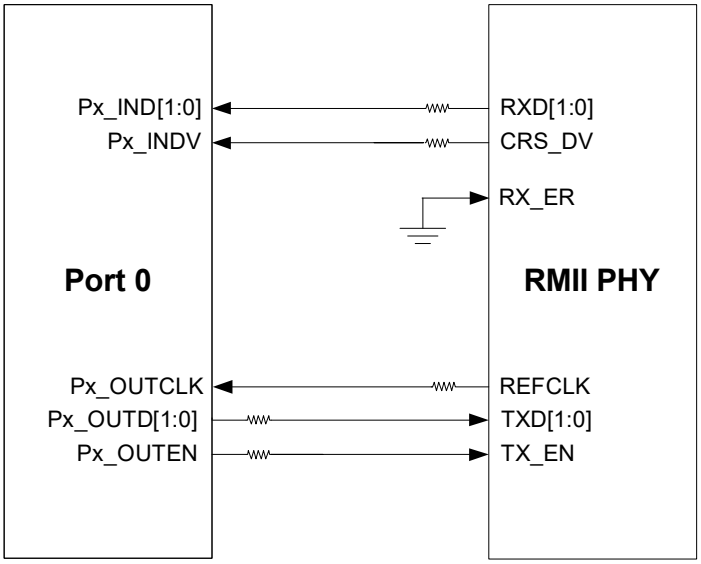
Figure 4: RGMII Interface Pins



2.1.5 RMII MAC Mode

RMII MAC mode supports 10 or 100 Mbps full or half-duplex. RMII mac mode is typically used to connect an external PHY but can be used for other applications. In RMII MAC mode, REFCLK is an input and is expected to be 50 MHz for all data rates. Refer to Figure 5 for RMII MAC connection to an external PHY.

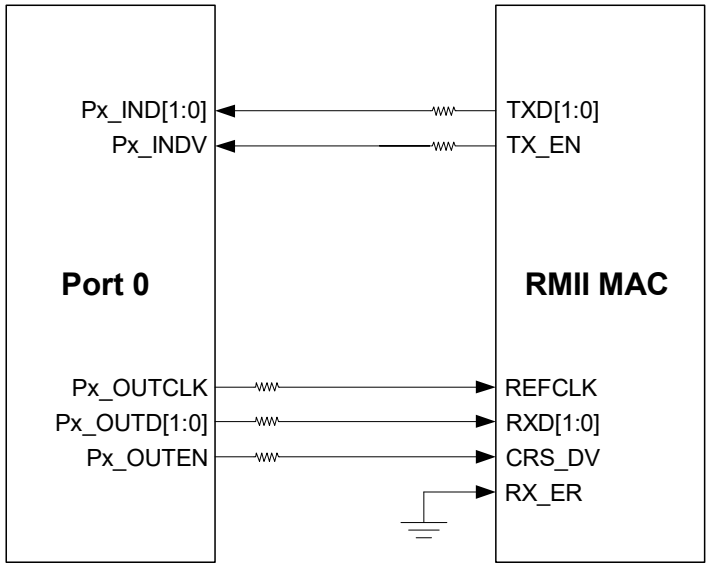
Figure 5: RMII MAC Interface Pins



2.1.6 RMII PHY Mode

In RMII PHY mode, REFCLK (P0_OUTCLK) is an output. OUTCLK is always 50 MHZ regardless of configured data interface speed. Figure 6 is an example of RMII PHY mode connections.

Figure 6: RMII PHY Interface



Note If P0_COL and P0_CRS are not used, they should be pulled- down with a 4.7 kΩ resistor.

2.1.7 1000BASE-T PHY Interface

Ports 3-7 are 10/100/1000 PHY interface. In the device, this interface supports 10BASE-T, 100BASE-TX, and 1000BASE-T copper IEEE 802.3az standards. The MAC inside the switch works the same way regardless of the external interface being used. Each PHY's Link, Speed, Duplex and Flow Control information is automatically communicated to the MAC. This information can be read on the Port status register. The PHY core registers are not directly accessible via the SMI interface. All access to PHY registers must be performed indirectly via SMI_PHY_COMMAND and SMI_PHY_DATA registers. Other than customer specific PHY configuration there should be no reason for a CPU to continuously access internal PHY's registers.

2.1.8 SGMII MAC or PHY Mode

SGMII MAC mode is used to connect a SERDES port to an external PHY. When the link state on the external PHY's media changes the new link state is communicated to switch MAC with in-band auto negotiation to the MAC.

SGMII PHY mode is typically used when the switch port is connected to a CPU or another switch.

SGMII mode supports 10/1000/1000 Mbps full or half-duplex. It uses the same 8B/10 encoding that 1000BASE-X uses. Lower speeds are supported by repeating the same symbol 10 times for 100 Mbps and 100 times to support 10 Mbps.

2.1.9 1000BASE-X

1000BASE-X is typically used to connect a switch port to an SFP fiber optics module. It can also be used to connect to another switch or CPU. 1000BASE-X supports auto negotiation bypass mode. This means the link can be established by receiving valid symbols. If the connected device only supports SGMII mode a link can be established by disabling auto negotiation on the connected device.

2.1.10 Port Status Registers

Each switch port has a status register that reports information about that port's PHY, SERDES or (x)MII interface. These registers can be used to check the current port configuration and link state. The C_MODE bits indicate the current configuration of the port. This is especially useful for auto media application to see which interface is currently internally connected to a given switch port. The port status register also indicates the speed duplex and if flow control is used.

2.1.11 PHY Polling Unit (PPU)

This device has an internal PHY polling unit. Clause 22 PHYs can be connected to MDC_PHY and MDIO_PHY pins. The PPU will automatically poll external PHYs using standard clause 22 defined PHY registers and update speed duplex and flow control in the MAC. By default the PPU is expecting the PHY connected to port 0 to be at external device address 0x0, Port 9 to be at external SMI address 0x9 and port 10 to be at external SMI address 0x0A. After reset the PPU will attempt to read the registers on external PHYs. If PHY responds to SMI address 0x0 0x9 or 0xA, it will automatically set the PHY detect bit in port register 0 of the corresponding port. The PPU will then continuously monitor the link status of the PHY. If software does not want the PPU to perform this function it can clear the PHY detect bit which will cause the PPU stop polling that PHY at the end of the next poling cycle. The PPU polls PHY register 0,1,4,5,9,10 to determine the speed link duplex and flow control state of the PHY.

The SmiSetup function in the SMI_PHY_COMMAND register can be used to change the relationship between switch port and an external PHY's SMI address. See functional spec for details.

Internal PHYs and External PHYs registers are accessed via the SMI_PHY_COMMAND register. This part has an internal SMI bus for accessing internal PHYs and an external SMI bus for accessing PHYs via the MDC_PHY and MDIO_PHY signals. This allows an external PHY to share the same SMI address with an internal PHY without address conflicts.

Proprietary and Clause 45 managed PHYs can be connected to MDC_PHY and MDIO_PHYs - however the PPU cannot automatically manage them. In these usage cases the IMP or an external CPU must be used to communicate the state of the external PHY to the switch port using switch port register 1 and port register 2.

If CPU_MGD is pulled high, the device is in CPU attached mode. In CPU attached mode MDC_PHY and MDIO_PHY are defined as GPIO inputs. During system initialization the CPU reconfigure these pins by changing scratch and misc register index 0x02 bit 7(SMI_PHY_Config)=1.

2.1.12 GPIO Assignments

This device supports up to 13 GPIO pins. GPIO[8:0] is shared with P0 xMII signals.Table 18 for GPIO availability for each P0_MODE.

Table 18: Port 0 GPIO Assignments

P0_MODE	xMII Setting	GPIO Available on Port 0	
000	Full-duplex MII PHY	GPIO [8:7]	When CPU_MGD signal is pulled high at reset, These signals are defined as GPIO[8:7] When CPU_MGD signal is pulled low at reset these signals are defied as MDC_PHY,MDIO_PHY. By clearing the NormalSMI bit (Global 2 Register 0x1A Index 0x2) the affect of the NO_CPU signal is inverted.
001	MII PHY	None Available	
010	MII MAC	None Available	
100	RMII PHY	GPIO [8:5], GPIO [1]	
101	RMII MAC	GPIO [8:5], GPIO [1]	
110	Disabled	GPIO[8:0]	
111	RGMII	GPIO [8;7]	When CPU_MGD signal is pulled high at reset, These signals are defined as GPIO[8:7] When CPU_MGD signal is pulled low at reset these signals are defied as MDC_PHY,MDIO_PHY. By clearing the NormalSMI bit (Global 2 Register 0x1A Index 0x2) the affect of the NO_CPU signal is inverted.
1xxx	SERDES modes	GPIO[8:0]	

Once configured as a GPIO, the pin can be programmed to the following functions:

- P0_ENABLE
- General Purpose Input
- General Purpose Output
- Timing Application Interface (TAI)
  - PTP Trigger Output (PTP_TRIG)
  - PTP Event Request Input (PTP_EVREQ)
  - PTP External Clock Input (PTP_EXTCLK)
- Synchronous Ethernet Recovered Clock 0 Output (SE_RCLK0)
- Synchronous Ethernet Recovered Clock 1 Output (SE_RCLK1)
- 125 MHz Clock output
- Port Stall – can be used to stall the transmission of a specific port (or ports) as needed

These functions can be programmed through the Scratch and Misc Register at Switch Global 2, Offset 0x1A (see Functional Specification).

2.2 Configuring GPIO as a Port Enable Pin

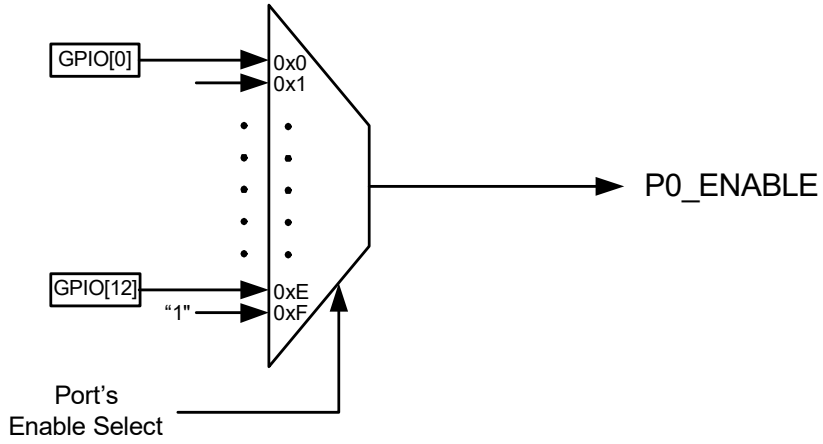
Each of the GPIO pins has the capability to be used as the P0_Enable pin for the xMII interfaces (Port 0) which can drive the link state of the port. When GPIO is used as P0_Enable the xMII output is tristated.

To use a GPIO as a Port Enable pin, the GPIO must first be configured as an input.

To select the specific GPIO to be used as an enable pin, program the xMII port's Enable Select register (Port Offset 0x1F, bits 15:12) to the number of the GPIO pin that will be used as the enable pin.

For example, setting the Enable Select to 0x0 selects GPIO 0, 0x1 selects GPIO 1, etc. Setting the bits to 0xF connects the enable function to a logic high, enabling the interface. Refer to Figure 7 for a configuration diagram. When the port does not have any GPIO selected the input state to Px_Enable is 1 so the link will be up if the PHY Detect bit in port register 0=0. When the PHY detect bit is 1 the link state will be driven by the PPU results.

Figure 7: GPIO Enable Example



2.3 LED Interface

The device uses a matrix LED interface allowing each PHY port to have up to two LEDs. The cathode of each LED is connected to a single row signal (Rx_LED). The anode of each LED is connected to a single column signal (Cx_LED). The physical LEDs on the device pins are organized as 5 rows with 4 columns. Table 19 shows the port to physical mapping.

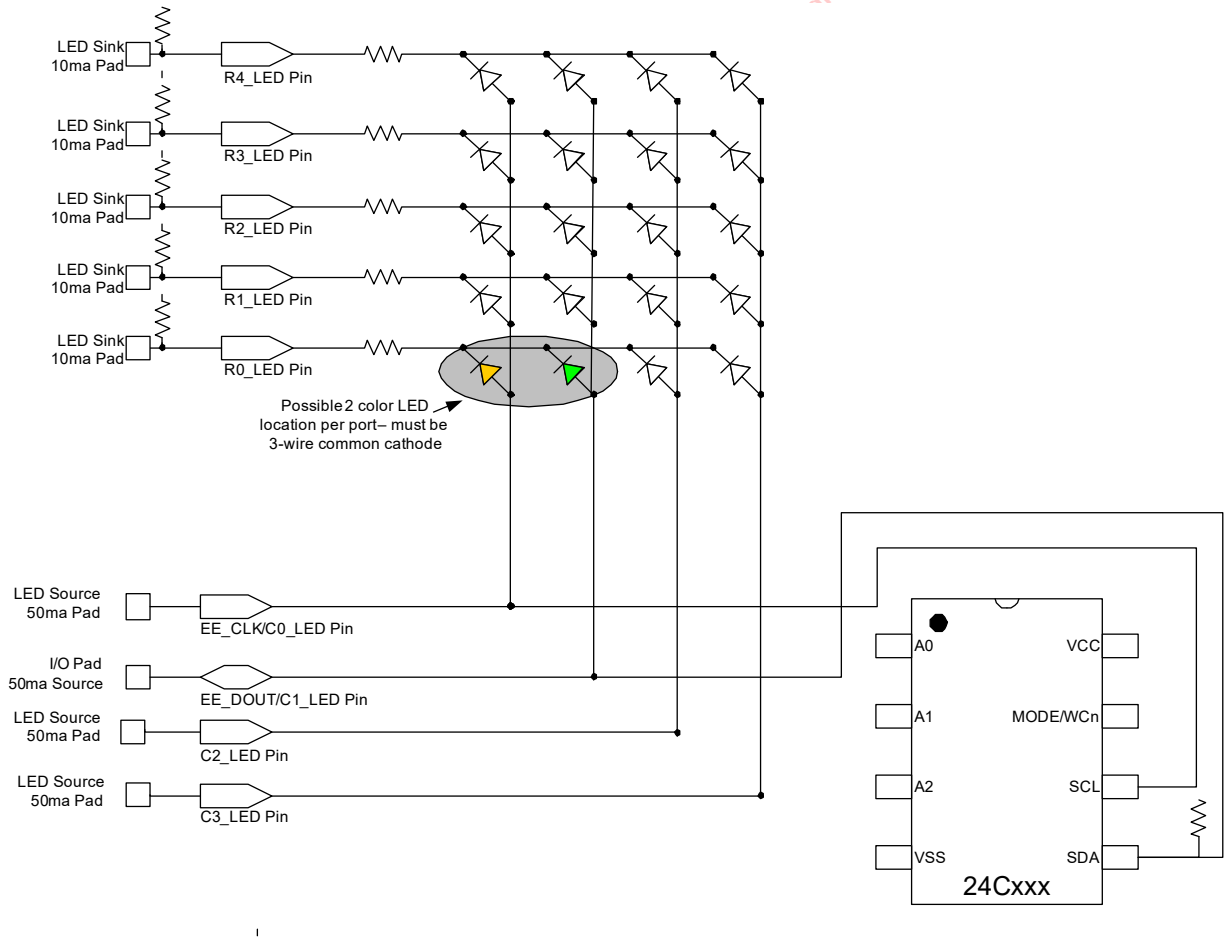
Table 19: LED Mapping

	C0_LED	C1_LED	C2_LED	C3_LED
R0_LED	Port 1, LED 0	Port 1, LED 1	Port 2, LED 0	Port 2, LED 1
R1_LED	Port 3, LED 0	Port 3, LED 1	Port 4, LED 0	Port 4, LED 1
R2_LED	Port 5, LED 0	Port 5, LED 1	Port 6, LED 0	Port 6, LED 1
R3_LED	Port 7, LED 0	Port 7, LED 1	Port 8, LED 0	Port 8, LED 1
R4_LED	Port 9, LED 0	Port 9, LED 1	Port 10, LED 0	Port 10, LED 1

The column signals (Cx_LED) are also shared with the EEPROM interface, and the architecture allows for the LEDs and EEPROM to operate at the same by time multiplexing the bus into 6 time cycles (C0_LED, C1_LED, C2_LED, C3_LED, and EEPROM). This prevents EEPROM access from interfering with LED operation and vice versa.

Refer to Figure 8 for EEPROM LED design.

Figure 8: LEDs plus 2-wire EEPROM



The EEPROM type can be 24C32-24C512.

2.3.1 LED Options

Each port supports up to two LEDs that can be configured individually to support many different options. Please note some functions are not supported on all LEDs.

Port 3-7 LED0 can be configured in one of the following modes:

- Link/Act/Speed by Blink Rate3 (off = no link, on = link, blink = activity, blink speed = link speed)
- 100/Gb Link/Act (off = no link, on = 100 or Gb link, blink = activity)
- Gb Link/Act (off = no link, on = Gb link, blink = activity)
- Link/Act (off = no link, on = link, blink = activity)
- Duplex/Collision (off = half-duplex, on = full-duplex, blink = col)
- 10/Gb Link/Act (off = no link, on = 10 or Gb link, blink = activity)
- Link (off = no link, on = link)
- 10 Link (off = no link, on = 10 link)
- 10 Link/Act (off = no link, on = 10 link, blink = activity)
- 100/Gb Link (off = no link, on = 100 or Gb link)
- PTP Act (blink on = PTP activity)
- Force Blink
- Force Off
- Force On

Port 3-7 LED1 can be configured in one of the following modes:

- 10/100 Link/Act (off = no link, on = 10 or 100 link, blink = activity)
- 10/100 Link/Act (off = no link, on = 10 or 100 link, blink = activity)
- Gb Link (off = no link, on = Gb link)
- Link/Act (off = no link, on = link, blink = activity)
- 10/Gb Link/Act (off = no link, on = 10 or Gb link, blink = activity)
- 10/Gb Link (off = no link, on = 10 or Gb link)
- Gb Link/100 Blink (off = no link or 10 Link, blink = 100 Link, on = Gb
- Link)
- 100 Link (off = no link, on = 100 link)
- 100 Link/Act (off = no link, on = 100 link, blink = activity)
- 10/100 Link (off = no link, on = 10 or 100 link)
- PTP Act (blink on = PTP activity)
- Force Blink
- Force Off
- Force On

The LED select configuration signal determines the value of port register 0x16 Index 0x0 Table 20,Table 21 and Table 22 indicates the default behavior of the LEDs for each supported hardware configuration. The LED configuration can be changed at any time with register access.

Table 20: Port 3-7 Hardware Reset LED Configuration

LED_SEL	LED Mode (Port 3-7 register 0x16 Index 0x0)	LED 0	LED 1
1	0x2	Gb Link/Activity Off = No link On = Gb link Blink = Activity	10/100 Link/Activity Off = No link On = 10/100 link, Blink = Activity)
0	0x3	Link/Act: Off = No link On = Link Blink = Activity	0x3 = Gb Link (Off = No link, On = Gb link)

Table 21: Port 9 Hardware Reset LED Configuration

LED_SEL	LED Mode (Port 9 Register 0x16 Index 0x0)	LED 0	LED 1
1	0x2	Port 0 Link/Activity	Port 10 Link Activity
0	0x3	Port 9 Link/Activity	Combined Link/Activity for ports 1-8

Table 22: Port 10 Hardware Reset LED Configuration

LED_SEL	LED Mode (Port register 0x16)	LED 0	LED 1
1	0x2	PTP Activity	Port 9 Link/Activity
0	0x3	Port 10 Link Activity	Port Link/Activity

2.3.2 Special LEDs

Special LEDs are used to display the Link/Activity status on a group of ports.This device supports 4 Special LED groups. A special LED group can be assigned to LED 0 or LED 1 on any port. A typical applicator where Special LEDs are used is all the LAN ports are combined into a single LED. A special LED group can be assigned to more than one LED. See LED control registers in the Functional specification.

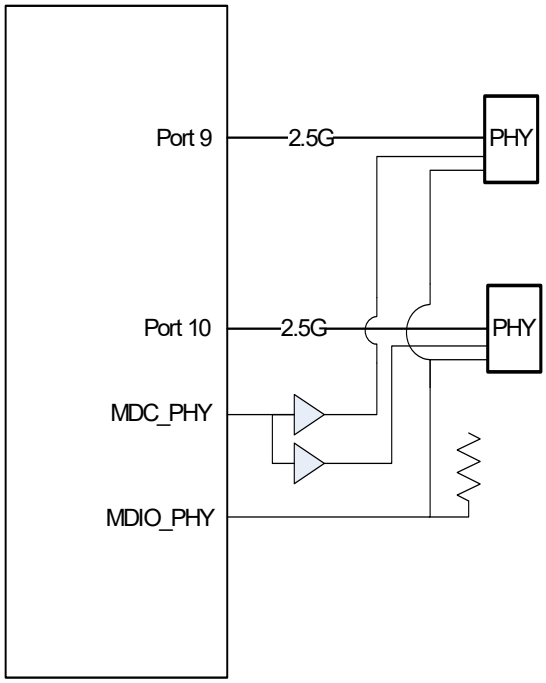
2.4 Connection of External PHYs

Port 0, Port 9, and Port 10 can be connected to external PHYs. The PHY polling unit can be used to poll any standard 802.3 Clause 22 compliant PHY. The PHY polling unit communicates the link, speed, duplex, and flow control state of the PHY. After reset the PPU will poll SMI address 0x00 for Port 0, 0x09 for Port 9, and 0x0A for Port 10. With register access, the association between external SMI address and switch port can be changed by using the SmiSetup operation in Global 2. An external PHY's SMI addresses can be any PHY address between 0 and 0x1F.

2.4.1 Connection to 1000BASE- T PHY

Figure 9 represents a typical connection to an external N-BASE-T PHY on Ports 9 and 10. Depending on trace length, if multiple PHYs are connected, a buffer on MDC_PHY is advisable.

Figure 9: Typical SGMII Connection to External PHY Connections



3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 23: Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD(3.3)}$	Power Supply Voltage on any 3.3V signal with respect to VSS	-0.5	3.3	+3.6	V
$V_{DD(2.5)}$	Power Supply Voltage on any 2.5V signal with respect to VSS	-0.5	2.5	+3.6 or $V_{DD(3.3)}$ +0.5[1] whichever is less	V
$V_{DD(1.8)}$	Power Supply Voltage on any 1.8V supply with respect to VSS	-0.5	1.8	+3.6 or $V_{DD(2.5)}$ +0.5[2] whichever is less	V
$V_{DD(1.5)}$	Power Supply Voltage on any 1.5V supply with respect to VSS	-0.5	1.5	+3.6 or $V_{DD(1.8)}$ +0.5[3] whichever is less	V
$V_{DD(1.05)}$	Power Supply Voltage on any 1.15V supply with respect to VSS	-0.5	1.05	+3.6 or $V_{DD(1.5)}$ +0.5[4] whichever is less	V
V_{PIN}	Voltage applied to any input pin with respect to VSS	-0.5	–	+3.6 or V_{DDO_PIN}[5] +0.5[6] whichever is less	V

1. VDD(2.5) must never be more than 0.5V greater than VDD(3.3) or damage will result. Power must be applied to VDD(3.3) before or at the same time as VDD(2.5).
2. VDD(1.8) must never be more than 0.5V greater than VDD(2.5) or damage will result. Power must be applied to VDD(2.5) before or at the same time as VDD(1.8).
3. VDD(1.5) must never be more than 0.5V greater than VDD(1.8) or damage will result. Power must be applied to VDD(1.8) before or at the same time as VDD(1.5).
4. VDD(1.15) must never be more than 0.5V greater than VDD(1.5) or damage will result. Power must be applied to VDD(1.5) before or at the same time as VDD(1.15).
5. The VDDO pad ring has separate I/O power supply options. Therefore, the voltage applied to a group of I/O pins must follow what is defined in Section 1.
6. VPIN must never be more than 0.5V greater than VDDO or damage will result.

3.1.1 Power Supply Sequencing

Power supply voltage on any pin must never be more than 0.5V greater than the next highest voltage pin, or damage will result. Power must be applied to the higher voltage pin before or at the same time as power is applied to the pins with the next lower voltage.

3.2 Recommended Operating Conditions

Table 24: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(3.3)}$	3.3V power supply	For any 3.3V supply pin[1]	3.135	3.3	3.465	V
$V_{DD(2.5)}$	2.5V power supply	For any 2.5V supply pin[2]	2.375	2.5	2.625	V
$V_{DD(1.8)}$	1.8V power supply	For any 1.8V supply pin	1.710	1.8	1.890	V
$V_{DD(1.5)}$	1.5V power supply	For any 1.5V supply pin	1.425	1.5	1.575	V
$V_{DD(1.05)}$	1.05V power supply	For any 1.05V supply pin	0.998	1.05	1.155	V
T_A	Ambient operating temperature[3]	Commercial parts	0	–	70	°C
		Industrial parts[4]	-40	–	85	°C
T_J	Maximum junction temperature		–	–	125[3]	°C
RSET	Internal bias reference	External resistor value required to be placed between RSET and VSS pins	4950	5000	5050	Ω

1. Some VDDO pins can be set to either 1.8V or 2.5V or 3.3V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.375V, and between 2.625V and 3.135V are not supported.
2. Some VDDO pins can be set to either 1.8V or 2.5V or 3.3V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.375V, and between 2.625V and 3.135V are not supported.
3. The important parameter is maximum junction temperature. As long as the maximum junction temperature is not exceeded, the device can be operated at any ambient temperature. Refer to White Paper on “TJ Thermal Calculations” for more information.
4. Industrial part numbers have an “I” following the commercial part numbers. For details see Section 5, Part Order Numbering/Package Marking, on page 94.

3.3 Thermal Conditions

3.3.1 Thermal Conditions for the 264-pin TFBGA Package

Table 25: Thermal Conditions for the 264-pin TFBGA Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient of the 264-Pin TFBGA package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	22.28	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	20.13	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	19.38	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	18.92	–	°C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 264-Pin TFBGA package $\psi_{JT} = (T_J - T_{TOP})/P$. T_{TOP} = Temperature on the top center of the package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	0.13	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	0.21	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	0.26	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow	–	0.29	–	°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 264-Pin TFBGA package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow	–	5.08	–	°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 264-Pin TFBGA package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow	–	12.68	–	°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

3.4 Current Consumption

Note

Typical current consumption values represent a device from a typical process corner operating at room temperature with typical voltage applied. Max Current consumption represents a device from the worst case process corner operating at 120°C case temp with +5% voltage applied to all rails.

Table 26: 88E6361 Device Current Consumption

Pins	Parameter	Condition	Typ	Max	Units
Px_AVDD33	3.3V power to analog core for Gigabit PHY interfaces	5 GPHY 1G, full traffic	257	440	mA
		5 GPHY 100M, full traffic	73	140	mA
		5 GPHY 10M, full traffic	113	230	mA
		5 GPHY, IEEE Power Down (0.11 = b'1)	12	20	mA
		5 GPHY 1G, EEE mode Idle link	12	20	mA
		5 GPHY 100M, EEE mode Idle link	12	20	mA
		5 GPHY, no link	37	40	mA
		Reset	11	12	mA
Px_AVDD15	1.5V power to analog core for Gigabit PHY interfaces, AVDD_REFCLK and AVDD_COM	5 GPHY 1G, full traffic	194	280	mA
		5 GPHY 100M, full traffic	114	145	mA
		5 GPHY 10M, full traffic	108	135	mA
		5 GPHY, IEEE Power Down (0.11 = b'1)	5	10	mA
		5 GPHY 1G, EEE mode Idle link	128	145	mA
		5 GPHY 100M, EEE mode Idle link	91	115	mA
		5 GPHY, no link	94	115	mA
		Reset	91	100	mA
EE_VDDO	3.3V to EEPROM and LED pins	Average Operating Conditions	15	30	mA
P0_VDDO	3.3V for Port 0's RGMII/MII/RMII I/O pins Current scales with voltage	All ports active at 1000 Mbps	44	–	mA
		All ports active at 100 Mbps	23	–	mA
		All ports active at 10 Mbps	20	–	mA
GPIO_VDDO	3.3V for GPIO Current scales with voltage	Typical GPIO connections and configuration pins	32	50	mA

Table 26: 88E6361 Device Current Consumption (Continued)

Pins	Parameter	Condition	Typ	Max	Units
P0_AVDD15 P9_AVDD15 P10_AVDD15	1.5V Power to SERDES cores	3 SERDES running at 2.5G	274	303	mA
		3 SERDES running at 1G	221	429	mA
		All SERDES powered down via register	5	20	mA
		Reset	5	20	mA
VDD_CORE	1.05V power to digital core	3 SERDES 2.5G, 5 GPHY 1G, full traffic	1073	1600	mA
		3 SERDES 2.5G, 5 GPHY 100M, full traffic	627	941	mA
		3 SERDES 2.5G, 5 GPHY 10M, full traffic	590	885	mA
		3 SERDES 2.5G, 5 GPHY, IEEE Power Down (0.11 = b'1)	435	603	mA
		3 SERDES 2.5G, 5 GPHY 1G, EEE mode Idle link	615	933	mA
		3 SERDES 2.5G, 5 GPHY 100M, EEE mode Idle link	580	869	mA
		3 SERDES 2.5G, 5 GPHY, no link	427	557	mA
		Reset	55	83	mA

3.5 DC Electrical Characteristics

3.5.1 Digital Operating Conditions

Table 27: Digital Operating Conditions
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VDDO	3.3V/2.5V/1.8V power.	See EE_VDDO, P0_VDDO and GPIO_VDDO pin definitions in Table 13 for details.		3.135	3.3	3.465	V
				2.375	2.5	2.625	V
				1.71	1.8	1.89	V
V_{IH}	High level input voltage	XTAL_IN, SE_SCLK	AVDD15	1.4	–	1.99	V
		EE_VDDO	VDDO = 3.135V	VDDO*70%	–	VDDO+0.4	V
		P0_VDDO GPIO_VDDO	VDDO = 2.375V				V
			VDDO = 1.710V				V
V_{IL}	Low level input voltage	XTAL_IN, SE_SCLK	AVDD15	-0.3	–	0.54	V
		All VDDO	VDDO = 3.135V	-0.4	–	VDDO*30%	V
		P0_VDDO GPIO_VDDO	VDDO = 2.375V				V
			VDDO = 1.710V				V
V_{OH}	High level output voltage	LED pins	I_{OH} = -7 mA	VDDO - 0.4	–	–	V
		All others (except INTn [1])	I_{OH} = -4 mA	VDDO - 0.4	–	–	V
		Others @ 1.8V	I_{OH} = -2 mA	VDDO - 0.2			V
V_{OL}	Low level output voltage	INTn and LED pins	I_{OL}= 7 mA	–	–	0.4	V
		All others	I_{OL}= 4 mA	–	–	0.4	V
		Others 1.8V	I_{OL}= 2 mA	–	–	0.2	V
I_{ILK}	Input leakage current	With pull-up resistor	$0<V_{IN}<V_{DDO}$	–	–	+ 10 - 60	µA
		With pull-down resistor	$0<V_{IN}<V_{DDO}$	–	–	+ 60 - 10	µA
		Others	$0<V_{IN}<V_{DDO}$	–	–	+ 10 - 10	µA
C_{IN}	Input capacitance	XTAL_IN, SE_SCLK		–	5	–	pF
		All others		–	–	5	pF

1. The INTn is an active low, open drain pin. See INTn description in the Signal Description.

3.6 AC Electrical Specifications

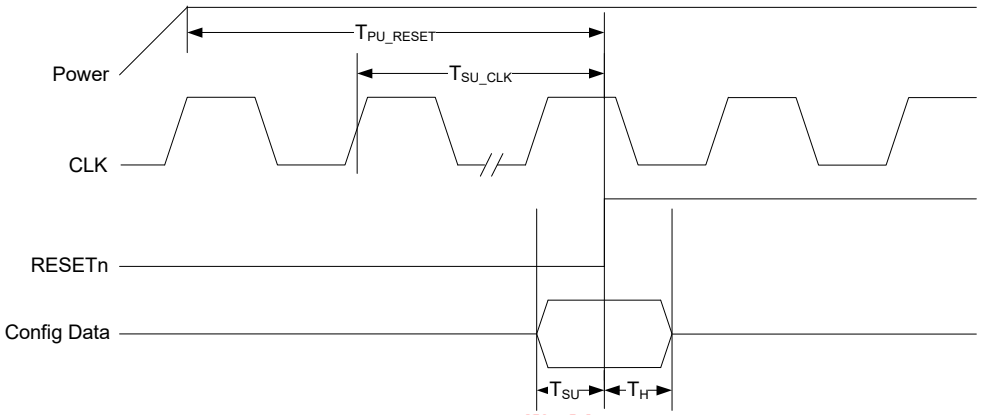
3.6.1 Reset and Configuration Timing

Table 28: Reset and Configuration
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted or RESETn assertion time	At power up or subsequent resets after power up	10	–	–	ms
T_{SU_CLK}	Number of valid REFCLK cycles prior to RESETn de-asserted		10	–	–	Clks
T_{SU}	Configuration data valid prior to RESETn de-asserted[1]		200	–	–	ns
T_{HD}	Config data valid after RESETn de-asserted		0	–	–	ns

1. When RESETn is low all configuration pins become inputs, and the value seen on these pins is latched on the rising edge of RESETn. All configuration pins that become outputs during normal operation will remain tri-stated for 40 ns after the rising edge of RESETn.

Figure 10: Reset and Configuration Timing



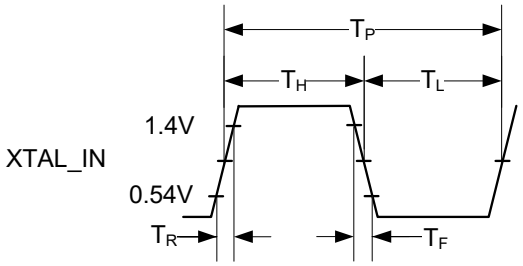
3.6.2 Clock Timing

Table 29: XTAL_IN Timing Specifications
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	XTAL_IN period		40 -50 ppm	40	40 +50 ppm	ns
T_H	XTAL_IN high time		13	20	27	ns
T_L	XTAL_IN low time		13	20	27	ns
T_R	XTAL_IN rise		–	–	3	ns
T_F	XTAL_IN fall		–	–	3	ns
$T_{J\_XTAL\_IN}$	XTAL_IN total jitter[1]		–	–	200	ps

1. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason. Broadband peak-peak = 200 ps, Broadband rms = 3 ps, 12 kHz to 20 MHz rms = 1 ps.

Figure 11: Oscillator Clock Timing



3.7 MII Timing

3.7.1 MII PHY Mode Receive Timing - 100 Mbps

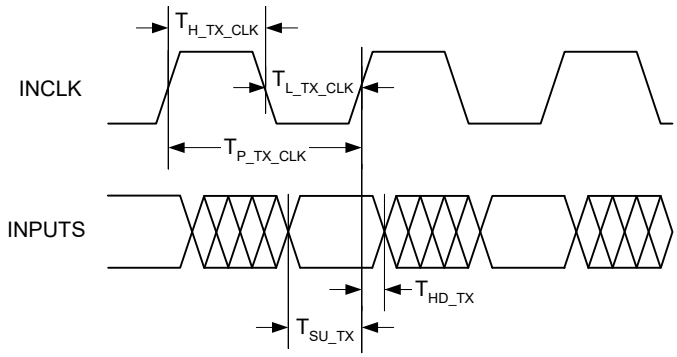
In PHY mode, the P[x]_INCLK pins are outputs.

Table 30: MII PHY Mode Receive Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$[1]	P[x]_INCLK period	10BASE mode	–	400	–	ns
		100BASE mode	–	40	–	ns
$T_{H\_TX\_CLK}$	P[x]_INCLK high	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
$T_{L\_TX\_CLK}$	P[x]_INCLK low	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
T_{SU_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high.		15	–	–	ns
T_{HD_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_IN-CLK going high.		0	–	–	ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 12: MII PHY Mode Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an output in this mode.

3.7.2 MII PHY Mode Transmit Timing - 100 Mbps

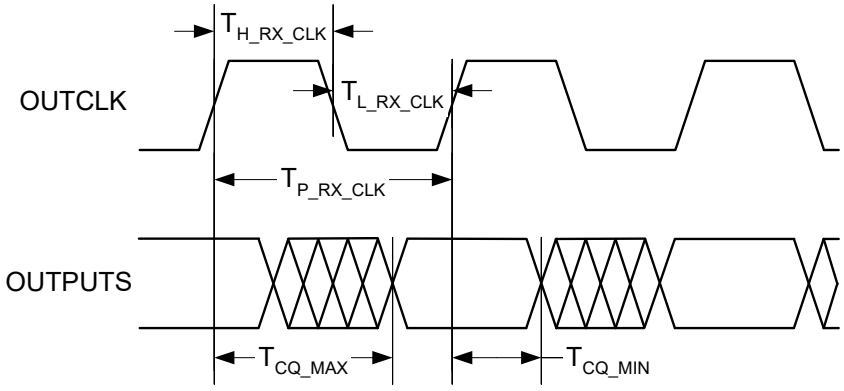
In PHY mode, the P[x]_OUTCLK pins are outputs.

Table 31: MII PHY Mode Transmit Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	10BASE mode	–	400	–	ns
		100BASE mode	–	40	–	ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	10BASE mode	160	200	240	ns
		100BASE mode	16	20	24	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid		–	–	25	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[3:0], P[x]_OUTEN) invalid		10	–	–	ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 13: MII PHY Mode Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

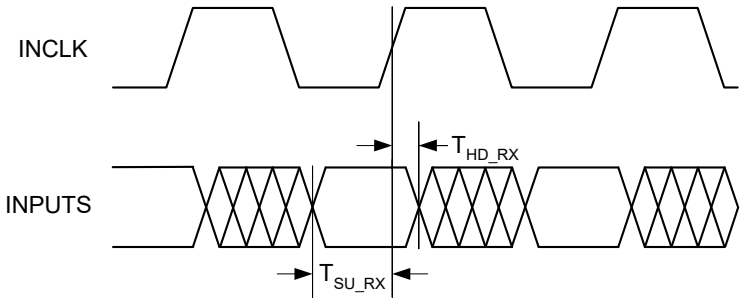
3.7.3 MII MAC Mode Receive Timing

In MAC mode, the P[x]_INCLK pins are inputs.

Table 32: MII Receive Timing - MAC Mode
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high	With 10 pF load	10	–	–	ns
T_{HD_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high	With 10 pF load	10	–	–	ns

Figure 14: MII MAC Mode Receive Timing



NOTE: INCLK is the clock used to clock the input data.
It is an input in this mode.

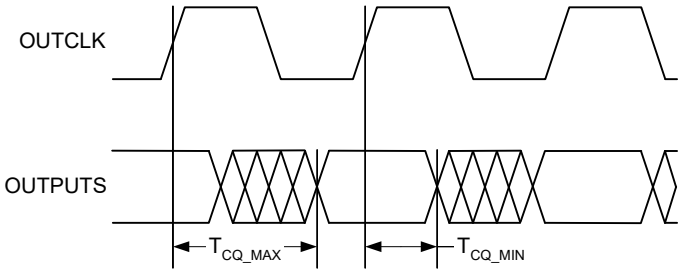
3.7.4 MII MAC Mode Transmit Timing

In MAC mode, the P[x]_OUTCLK pins are inputs.

Table 33: MII MAC Mode Transmit Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid	With 10 pF load	–	–	25	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) invalid	With 10 pF load	0	–	–	ns

Figure 15: MII MAC Mode Transmit Timing



NOTE: OUTCLK is the clock used to clock the output data.
It is an input in this mode.

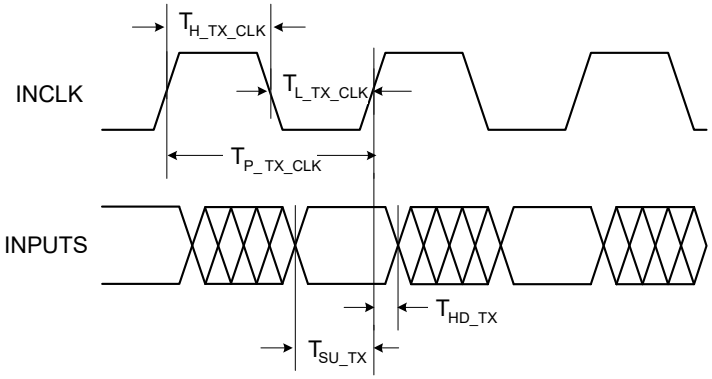
3.7.5 TMII PHY Mode Receive Timing - 200 Mbps

In PHY mode, the P[x]_INCLK pins are outputs.

Table 34: TMII PHY Mode Receive Timing - 200 Mbps
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$	P[x]_INCLK period	200BASE mode	–	20	–	ns
$T_{H\_TX\_CLK}$	P[x]_INCLK high	200BASE mode	8	10	12	ns
$T_{L\_TX\_CLK}$	P[x]_INCLK low	200BASE mode	8	10	12	ns
T_{SU_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high.		5	–	–	ns
T_{HD_TX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high.		3	–	–	ns

Figure 16: TMII PHY Mode Receive Timing - 200 Mbps



NOTE: INCLK is the clock used to clock the input data. It is an output in this mode.

3.7.6 TMII PHY Mode Transmit Timing - 200 Mbps

In PHY mode, the P[x]_OUTCLK pins are outputs.

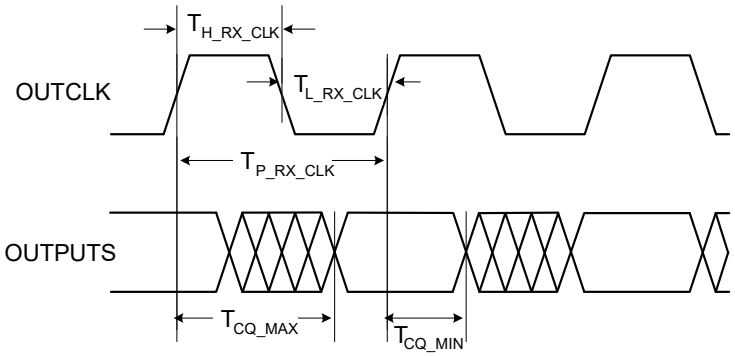
Table 35: TMII PHY Mode Transmit Timing - 200 Mbps

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	200BASE mode	–	20	–	ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	200BASE mode	8	10	12	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	200BASE mode	8	10	12	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTEN) valid		–	–	15	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[3:0], P[x]_OUTEN) invalid		2	–	–	ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

Figure 17: TMII PHY Mode Transmit Timing - 200 Mbps



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

3.7.7 TMII MAC Mode Clock Timing - 200 Mbps

In MAC mode, INCLK and OUTCLK are inputs.

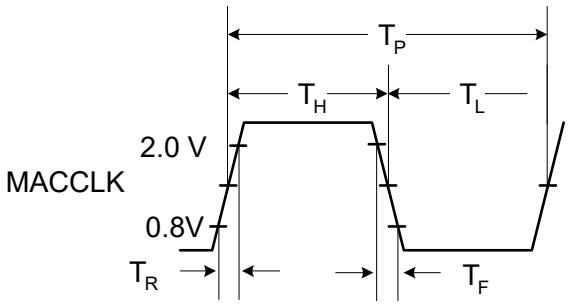
Table 36: TMII MAC Mode Clock Timing - 200 Mbps

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P[1]	MACCLK_IN period		0	20	20 +50 ppm	ns
T_H	MACCLK_IN high time		8	–	–	ns
T_L	MACCLK_IN low time		8	–	–	ns
T_R	MACCLK_IN rise		–	–	3	ns
T_F	MACCLK_IN fall		–	–	3	ns

1. DC to 25 MHz

Figure 18: TMII MAC Clock Timing - 200 Mbps



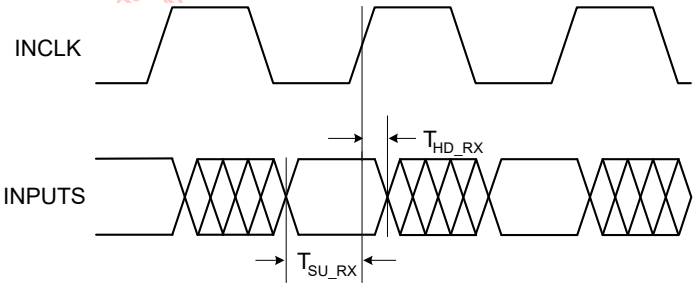
3.7.8 TMII MAC Mode Receive Timing - 200 Mbps

In MAC mode, the P[x]_INCLK pins are inputs.

Table 37: TMII MAC Mode Receive Timing - 200 Mbps
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid prior to P[x]_INCLK going high	With 10 pF load	5	–	–	ns
T_{HD_RX}	MII inputs (P[x]_IND[3:0], P[x]_INDV) valid after P[x]_INCLK going high	With 10 pF load	2	–	–	ns

Figure 19: TMII MAC Mode Receive Timing - 200 Mbps



NOTE: INCLK is the clock used to clock the input data. It is an input in this mode.

3.7.9 TMII MAC Mode Transmit Timing - 200 Mbps

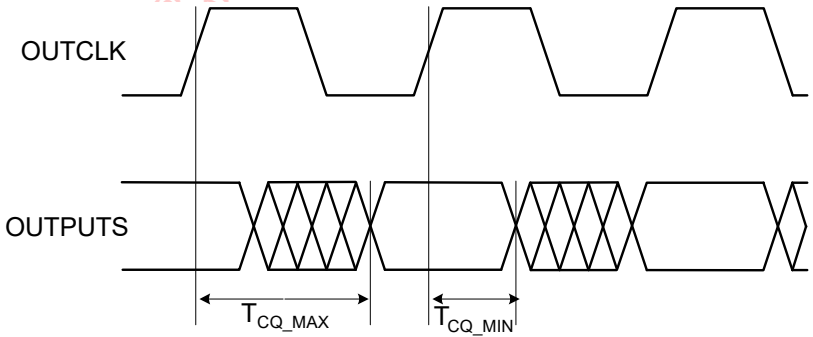
In MAC mode, the P[x]_OUTCLK pins are inputs.

Table 38: TMII MAC Transmit Timing - 200 Mbps

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTDV valid	With 10 pF load	–	–	15	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs (P[x]_OUTD[3:0], P[x]_OUTDV invalid	With 10pF load	0	–	–	ns

Figure 20: TMII MAC Mode Transmit Timing - 200 Mbps



NOTE: OUTCLK is the clock used to clock the output data. It is an input in this mode.

3.8 RGMII Timing

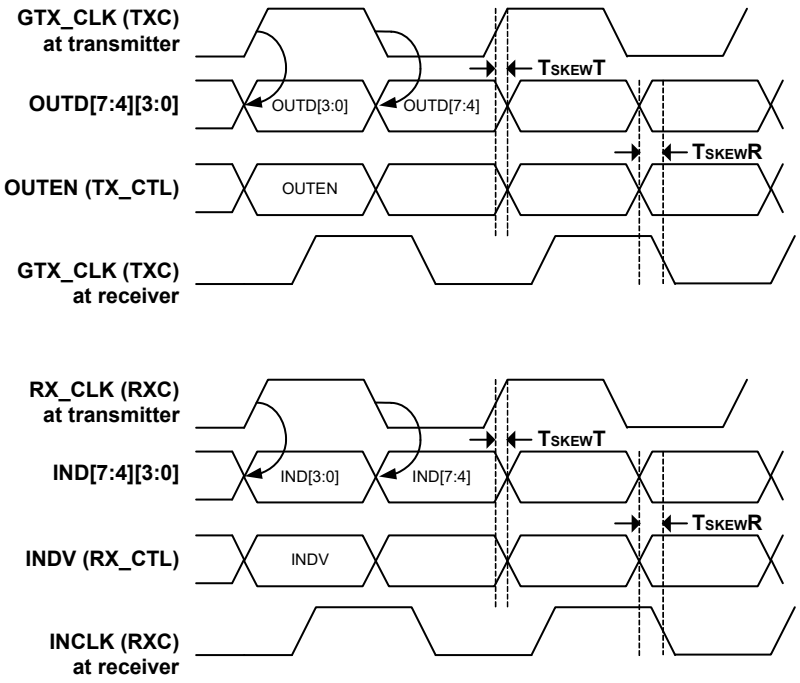
Table 39: RGMII Interface Timing

For other timing modes see Section 3.8.1, RGMII Timing for Different RGMII Modes, on page 76.

Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	-	2.6	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH1000}$	High Time for 1000BASE-T [1]	3.6	4.0	4.4	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20-80%)	–	–	0.75	ns

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three TCYCLE of the lowest speed transitioned between.

Figure 21: RGMII Multiplexing and Timing



3.8.1 RGMII Timing for Different RGMII Modes

3.8.1.1 RGMII Transmit Timing

Table 40: Transmit - TXC Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{sskew}	RGMII Transmit Delay Control (bit 3) = 0	-0.5	–	0.5	ns

Figure 22: Transmit - TXC Timing when RGMII Transmit Delay Control (bit 3) = 0

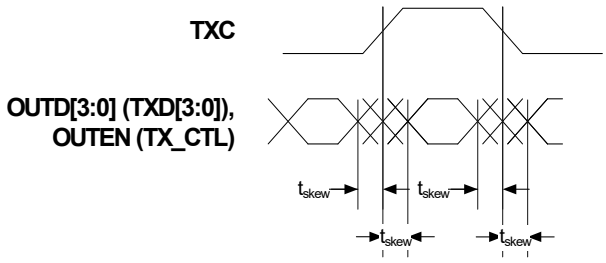
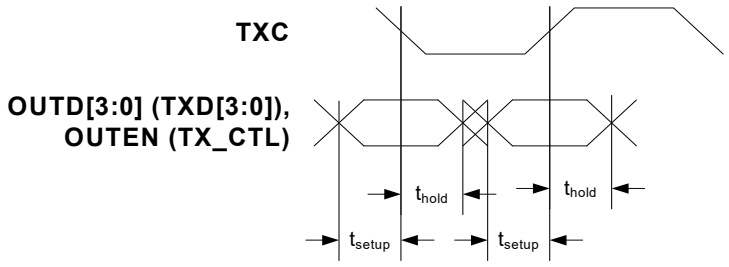


Table 41: Transmit - TXC Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Transmit Delay Control (bit 3) = 1	1.2	–	–	ns
t_{hold}		1.2	–	–	ns

Figure 23: Transmit - TXC Timing when RGMII Transmit Delay Control (bit 3) = 1



3.8.1.2 RGMII Receive Timing

Table 42: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 0	1.0	–	–	ns
t_{hold}		0.8	–	–	ns

Figure 24: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (bit 4) = 0

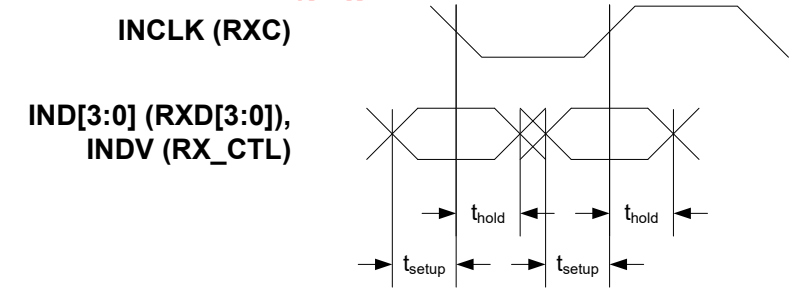
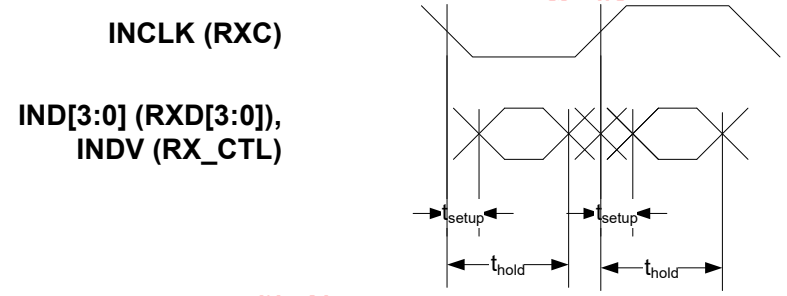


Table 43: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 1	-0.9	–	–	ns
t_{hold}		2.7	–	–	ns

Figure 25: Receive - RXC Timing when RGMII Receive Delay Control (bit 4) = 1



3.9 RMII Timing

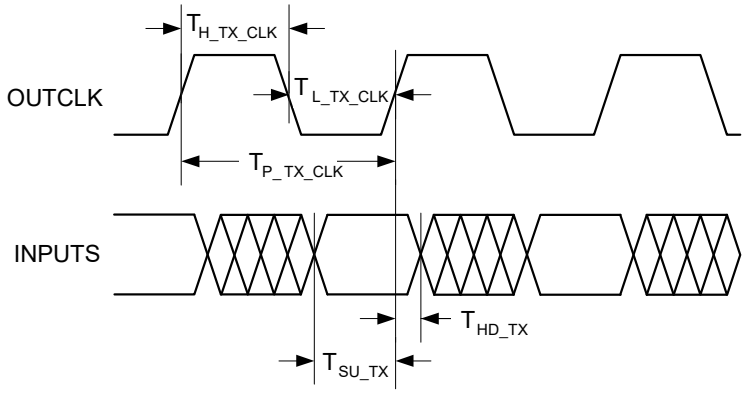
3.9.1 RMII Receive Timing

Table 44: RMII Receive Timing using INCLK
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_TX\_CLK}$	P[x]_OUTCLK period[1]	100BASE mode	–	20	–	ns
$T_{H\_TX\_CLK}$	P[x]_OUTCLK high	100BASE mode	8	10	12	ns
$T_{L\_TX\_CLK}$	P[x]_OUTCLK low	100BASE mode	8	10	12	ns
T_{SU_TX}	RMII inputs (P[x]_IND[1:0], P[x]_INDV) valid prior to P[x]_OUTCLK going high.		4	–	–	ns
T_{HD_TX}	RMII inputs (P[x]_IND[1:0], P[x]_INDV) valid after P[x]_OUTCLK going high.		2	–	–	ns

1. 50 MHz for 100 Mbps.

Figure 26: RMII Receive Timing using OUTCLK



NOTE: OUTCLK is the clock used to clock the input data. It is an output in this mode.

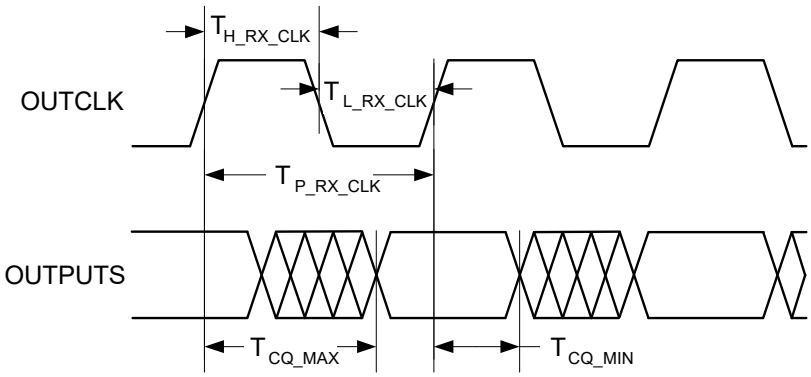
3.9.2 RMII Transmit Timing

Table 45: RMII Transmit Timing using INCLK
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_RX\_CLK}$[1]	P[x]_OUTCLK period	100BASE mode	–	20	–	ns
$T_{H\_RX\_CLK}$	P[x]_OUTCLK high	100BASE mode	8	10	12	ns
$T_{L\_RX\_CLK}$	P[x]_OUTCLK low	100BASE mode	8	10	12	ns
T_{CQ_MAX}	P[x]_OUTCLK to outputs (P[x]_OUTD[1:0], P[x]_OUTEN) valid		–	–	16	ns
T_{CQ_MIN}	P[x]_OUTCLK to outputs P[x]_OUTD[1:0], P[x]_OUTEN) invalid		2	–	–	ns

1. 50 MHz for 100 Mbps.

Figure 27: RMII Transmit Timing using OUTCLK



NOTE: OUTCLK is the clock used to clock the output data. It is an output in this mode.

3.10 SERDES

3.10.1 2500BASE-X

Table 46: 2500BASE-X Electrical Summary

Test Parameters	Specification			Units
Transmitter Tests				
	Min	**Typ**	**Max**	
Signaling Rate	-100 ppm	3.125	+ 100 ppm	GBd
Nominal Unit Interval	–	320	–	ps
Differential Output	800	1000	1200	mVpp
Deterministic Jitter	–	–	0.17	UI
Random Jitter	–	–	0.27	UI
Total Jitter Output	–	–	0.35	UI
Receiver Tests				
Signaling Rate	-100 ppm	3.125	+100 ppm	GBd
Nominal Unit Interval	–	320	–	ps
Receiver Coupling	–	AC	–	N/A
Differential Input peak-to-peak Amplitude	–	–	1600	mVpp
Applied Sinusoidal Jitter (min. peak-to-peak)	0.17	–	–	UI
Applied Random Jitter (min. peak-to-peak)	0.18	–	–	UI

3.10.2 SGMII

Table 47: SGMII Electrical Summary

Test Parameters	Specification			Units
Transmitter Tests				
	Min	**Typ**	**Max**	
Output Voltage High	–	–	1525	mV
Output Voltage Low	875	–		mV
Output Ringing	–	–	10%	
Output Differential Voltage	150	–	400	mV
Output Offset Voltage	1.075	–	1.325	V
Single Ended Output Impedance	40	–	140	Ω
Output Current On Short to Ground	–	–	40	mA
Output Current When P and N are shorted	–	–	12	mA
Power Off Leakage Current	–	–	10	mA
Output Differential DC Resistance	N/A			UI
Skew between P and N	–	–	20	ps
Total Output Jitter	–	–	300	ps
Receiver Tests				
Sensitivity	–	–	100	mVpp
Single ended termination	–	50	–	Ω
Jitter Tolerance	500	–	–	ps

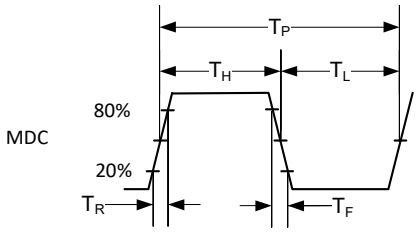
3.11 Serial Management Interface (SMI) Timing

3.11.1 SMI Clock Timing (CPU Set)

Table 48: SMI Clock Timing (CPU Set)
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		50	–	–	ns	20 MHz Max
T_H	MDC high time		25	–	–	ns	–
T_L	MDC low time		25	–	–	ns	–
T_R	MDC rise		–	–	3	ns	–
T_F	MDC fall		–	–	3	ns	–

Figure 28: SMI Clock Timing (CPU Set)

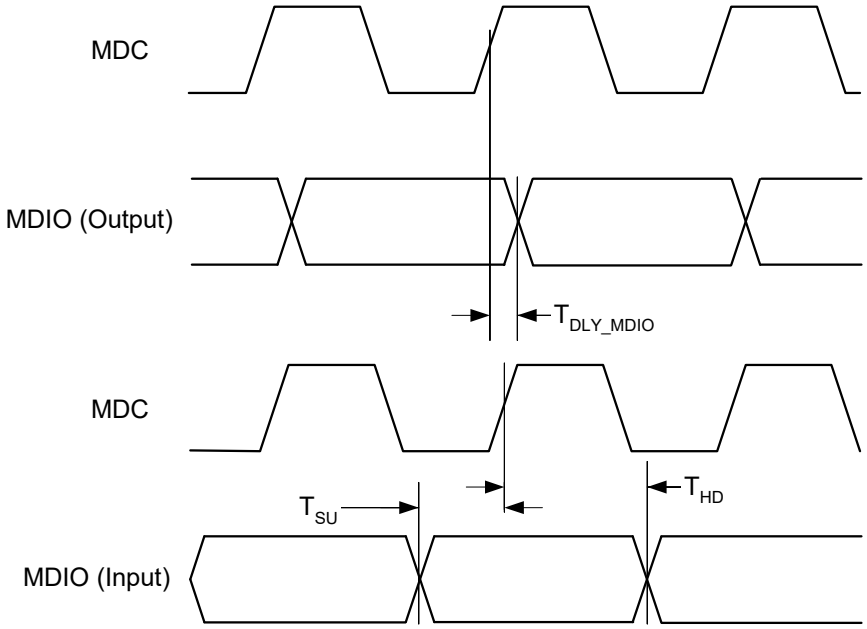


3.11.2 SMI Data Timing (CPU Set)

Table 49: SMI Clock Timing (CPU Set)
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0	–	30	ns	–
T_{SU}	MDIO (Input) to MDC setup time		10	–	–	ns	–
T_{HD}	MDIO (Input) to MDC hold time		10	–	–	ns	–

Figure 29: SMI Data Timing



3.11.3 SMI Timing (PHY Set)

Table 50: SMI Clock Timing (PHY Set)
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		1.02	.128	.064	µs	Default = 7.8 MHz
T_H	MDC high time		.51	.064	.032	µs	–
T_L	MDC low time		.51	.064	.032	µs	–
T_R	MDC rise		–	–	6	ns	–
T_F	MDC fall		–	–	6	ns	–
T_{TX_SU}	MDIO output setup time		10	–	–	ns	1
T_{TX_HD}	MDIO output hold time		10	–	–	ns	2
T_{RX_SU}	MDIO input setup time		–	–	–	–	–
T_{RX_HD}	MDIO input hold time		–	–	–	–	–
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0	–	5	ns	2

1. MDIO input setup and hold time is intentionally sampled with respect to the MDC falling edge.
2. MDIO data is intentionally clocked out on the falling edge of MDC.

Figure 30: SMI Timing Output (PHY Mode)

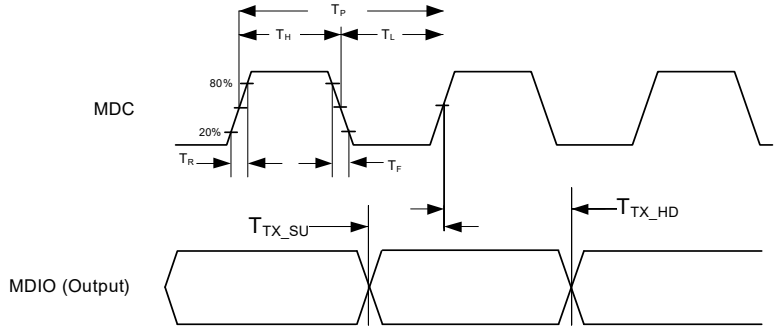
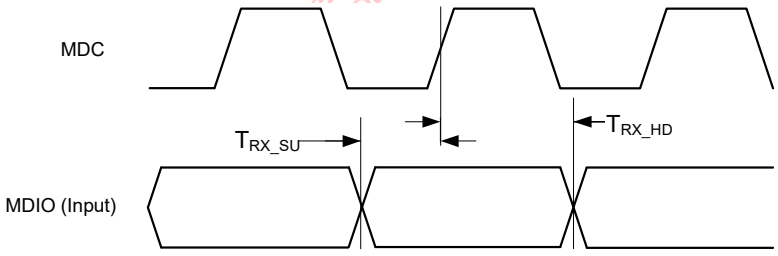


Figure 31: SMI Timing Input (PHY Mode)



3.12 EEPROM Timing

3.12.1 2-Wire EEPROM Timing

Table 51: 2-Wire EEPROM Input Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Freq	EE_CLK frequency	3.3V	–	–	1000	kHz
T_H	EE_CLK high time	3.3V	500	–	–	ns
T_L	EE_CLK low time	3.3V	500	–	–	ns
T_{IN}	Data input time	3.3V	50	–	250	ns

Figure 32: 2-Wire Input Timing

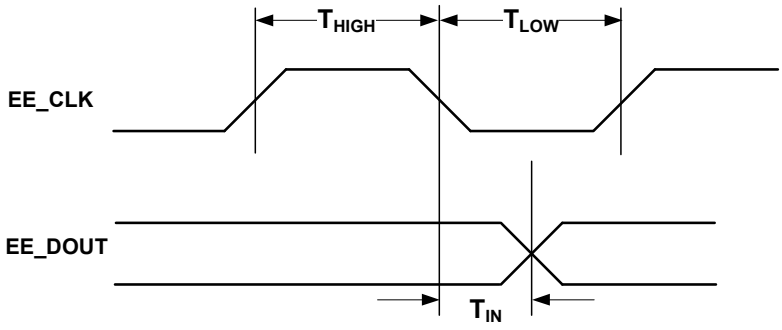
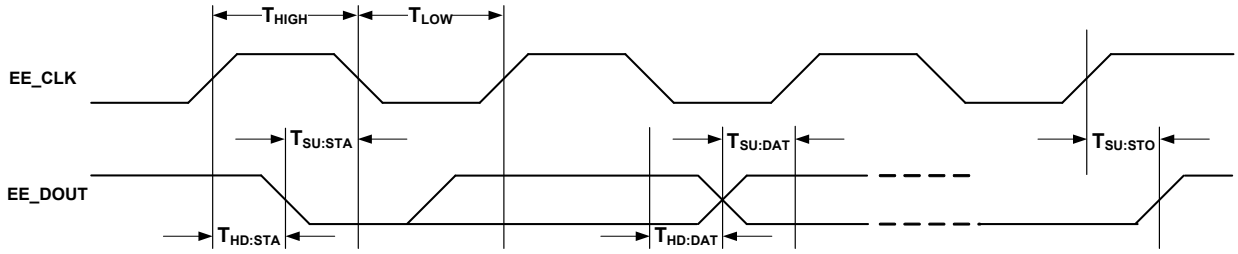


Table 52: 2-Wire EEPROM Output Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
Freq	EE_CLK frequency	3.3V	–	–	1000	kHz
T_H	EE_CLK high time	3.3V	500	–	–	ns
T_L	EE_CLK low time	3.3V	500	–	–	ns
$T_{HD:STA}$	Start condition hold time	3.3V	250	–	–	ns
$T_{SU:STA}$	Start condition setup time	3.3V	250	–	–	ns
$T_{HD:DAT}$	EE_DOUT data output hold time	3.3V	250	–	–	ns
$T_{SU:DAT}$	EE_DOUT data output setup time	3.3V	250	–	–	ns
$T_{SU:STO}$	Start condition setup time	3.3V	250	–	–	ns

Figure 33: 2-Wire EEPROM Output Timing



3.13 IEEE AC Characteristics

3.13.1 IEEE AC Transceiver Parameters

Table 53: IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:
-10BASE-T IEEE 802.3 Clause 14-2000
-100BASE-TX ANSI X3.263-1995
-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall Time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
$T_{RISE/TFALL}$ Symmetry		MDIP/N[1:0]	100BASE-TX	0	–	0.5	ns
DCD	Duty Cycle Distortion	MDIP/N[1:0]	100BASE-TX	0	–	0.5[1]	ns, peak-peak
Transmit Jitter		MDIP/N[1:0]	100BASE-TX	0	–	1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3

3.13.2 IEEE DC Transceiver Parameters

Table 54: IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.
-10BASE-T IEEE 802.3 Clause 14
-100BASE-TX ANSI X3.263-1995
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	MDIP/N[1:0]	10BASE-T no cable	2.2	2.5	2.8	V
		MDIP/N[1:0]	10BASE-T cable model	585[1]	–	–	mV
		MDIP/N[1:0]	100BASE-TX mode	0.950	1.0	1.050	V
		MDIP/N[3:0]	1000BASE-T[2]	0.67	0.75	0.82	V
	Overshoot[2]	MDIP/N[1:0]	100BASE-TX mode	0	–	5%	V
	Amplitude Symmetry (positive/ negative)	MDIP/N[1:0]	100BASE-TX mode	0.98x	–	1.02x	V+/V-
V_{IDIFF}	Peak Differential Input Voltage	MDIP/N[1:0]	10BASE-T mode	585[3]	–	–	mV

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. IEEE 802.3ab Figure 40 -19 points A&B.
3. The input test is actually a template test ; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.

3.14 XTAL_IN/XTAL_OUT Receiver DC Specifications

Table 55: XTAL_IN/XTAL_OUT Receiver DC Specifications

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)
All voltages are given with respect to receiver circuit ground voltage

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_i	Input voltage range		0	–	AVDD_XTAL	V
V_{icm}	Input common mode voltage range		300	–	1300	mV
V_{icm_delta}	Variation of Input common mode			–	50	mV
$V_{id\ p\text{-}p}$	Input differential voltage peak-to-peak		200	–	1200	mV
R_{in}	Receiver differential input impedance		80	100	120	Ω

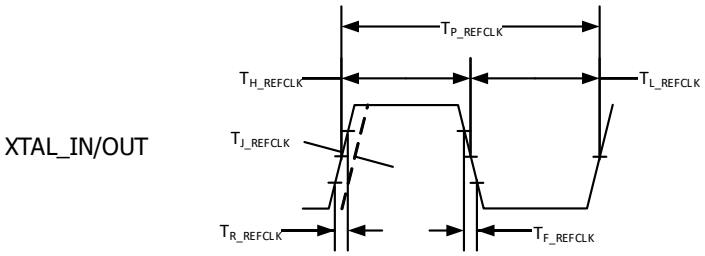
3.15 XTAL_IN/XTAL_OUT Receiver AC Specifications

Table 56: XTAL_IN/XTAL_OUT Receiver AC Specifications

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)
All voltages are given with respect to receiver circuit ground voltage

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_25\_REFCLK}$	25 MHz REFCLK Period		40 -50 ppm	40	40 +50 ppm	ns
$T_{H\_25\_REFCLK}$	25 MHz REFCLK High Time		18	20	22	ns
$T_{L\_25\_REFCLK}$	25 MHz REFCLK Low Time		18	20	22	ns
T_r/T_f	Rise and Fall Time (10% - 90%)		–	–	1000	ps
t_{skew}	Skew tolerable at receiver input to meet setup and hold time requirements		–	–	325	ps
T_{J_REFCLK}	REFCLK Jitter (RMS)	12 kHz - 20 MHz				ps

Figure 34: REFCLK Timing



4 Mechanical Drawings and Package Information

4.1 Mechanical Drawings

Figure 35: 264-pin TFBGA (15 x 15 mm) Package Mechanical Drawings - Top and Side View

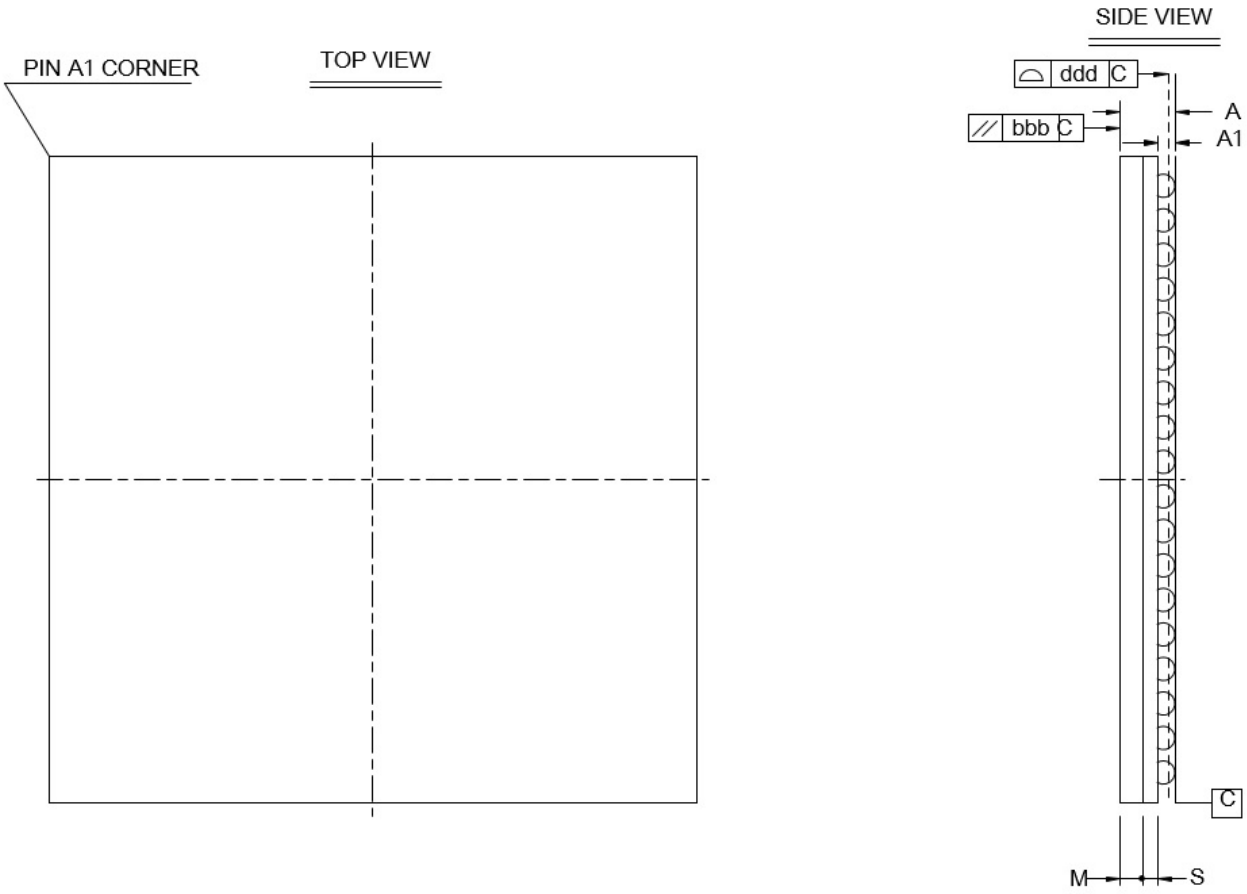


Figure 36: 264-pin TFBGA (15 x 15 mm) Package Mechanical Drawing - Bottom View

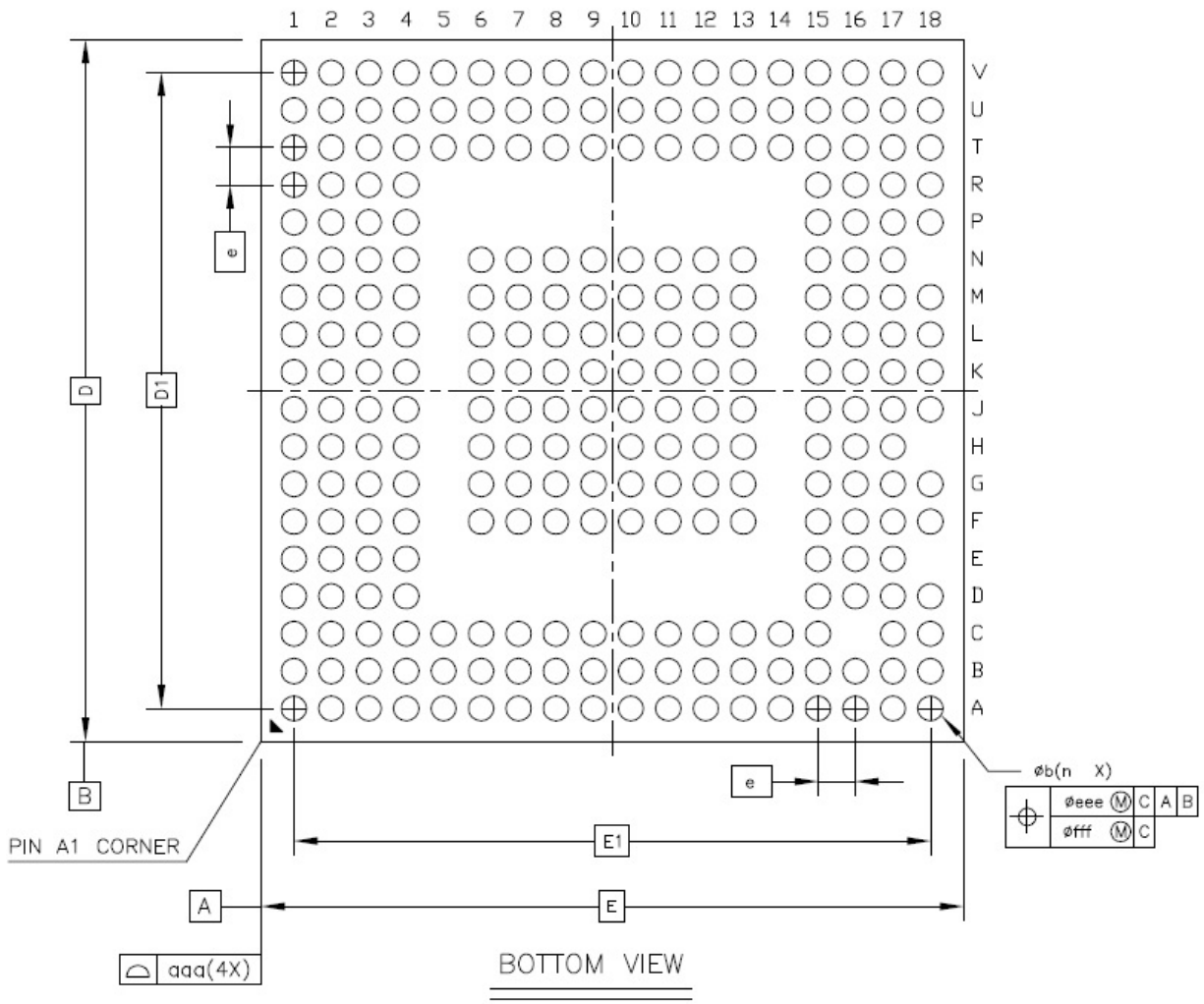


Table 57: 264-pin TFBGA (15 x 15 mm) Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
E	14.90	15.00	15.10
D	14.90	15.00	15.10
e		0.800	
A	1.230	1.300	1.370
M		0.530 Ref.	
S		0.360 Ref.	
Ball Diameter		0.500	
A1	0.360	0.410	0.460
b	0.440	0.540	0.640
aaa		0.100	
bbb		0.200	
ddd		0.150	
eee		0.150	
fff		0.080	
Ball Count		264	
E1		13.600	
D1		13.600	

4.2 264-pin TFBGA (15 x 15 mm) Package Information

Table 58: 264-pin TFBGA (15 x 15 mm) Package Information

Symbol	Parameter	Min	Typ	Max	Units
$P_{PRESSURE}$	Maximum pressure on the 264-pin TFBGA (15 x 15 mm) package	–	–	31	N
$T_{STORAGE}$	Storage temperature	-55		+125[1]	°C

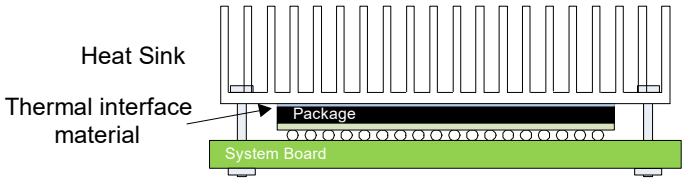
1. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.

4.2.1 Mechanical Stress Guidelines

- The maximum static load should not exceed 31 Newton.
- The load must be applied uniformly and distributed perpendicularly to the package top surface.
- The applied load should meet the thermal solution and thermal interface material specifications.

Figure 37 shows the heat sink attachment for the 88E6361 devices.

Figure 37: Heat Sink Attachment



5 Part Order Numbering/Package Marking

5.1 Part Order Numbering

Figure 38 shows the part order numbering scheme for the 88E6361 device. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 38: Sample Part Number

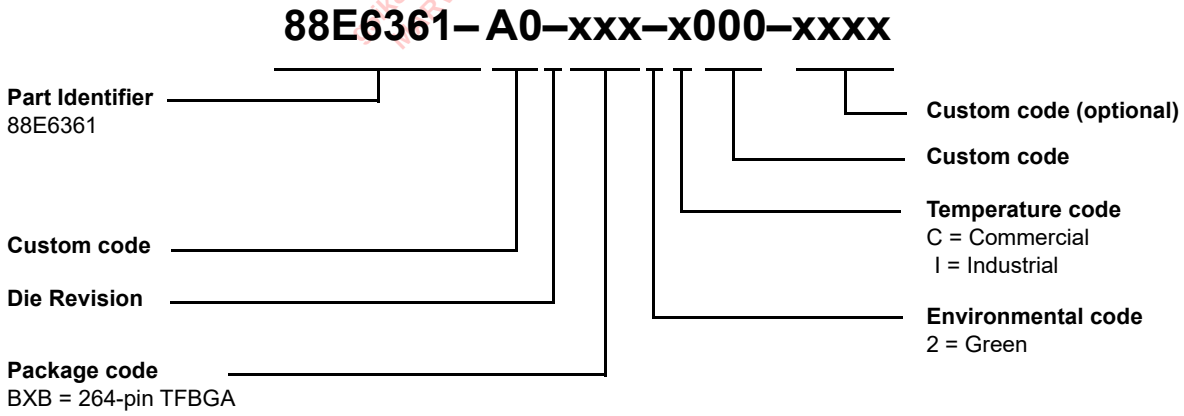


Table 59: Part Order Options

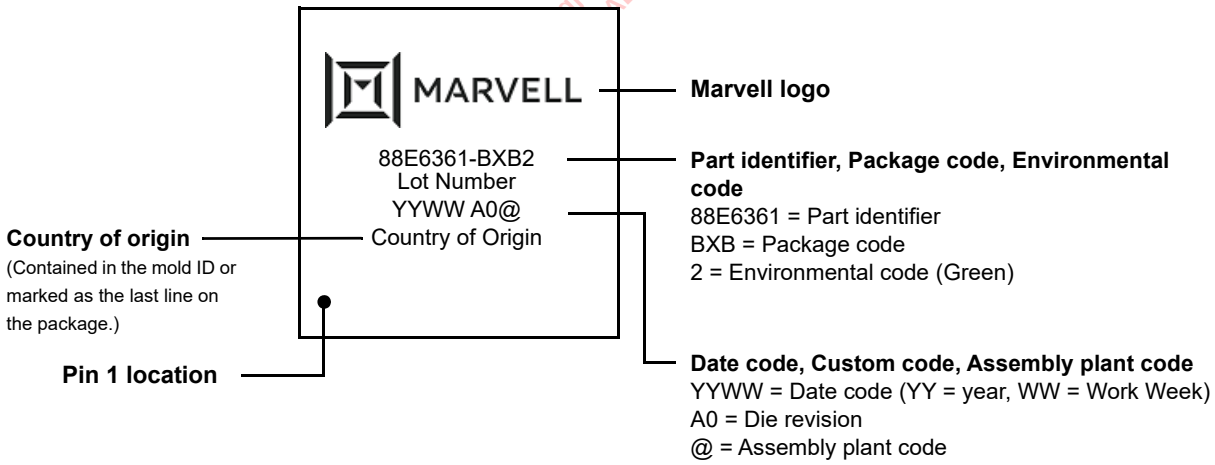
Package Type	Part Order Number
264-pin TFBGA (15 x 15 mm)	88E6361-A0-BXB2C000 (Commercial, Green-compliant package)
	88E6361-A0-BXB2I000 (Industrial, Green-compliant package)

5.2 Package Marking

5.2.1 Commercial Package Marking

Figure 39 shows a sample Commercial package marking and pin A1 location for the 88E6361 device.

Figure 39: Commercial Package Marking and Ball 1 Location

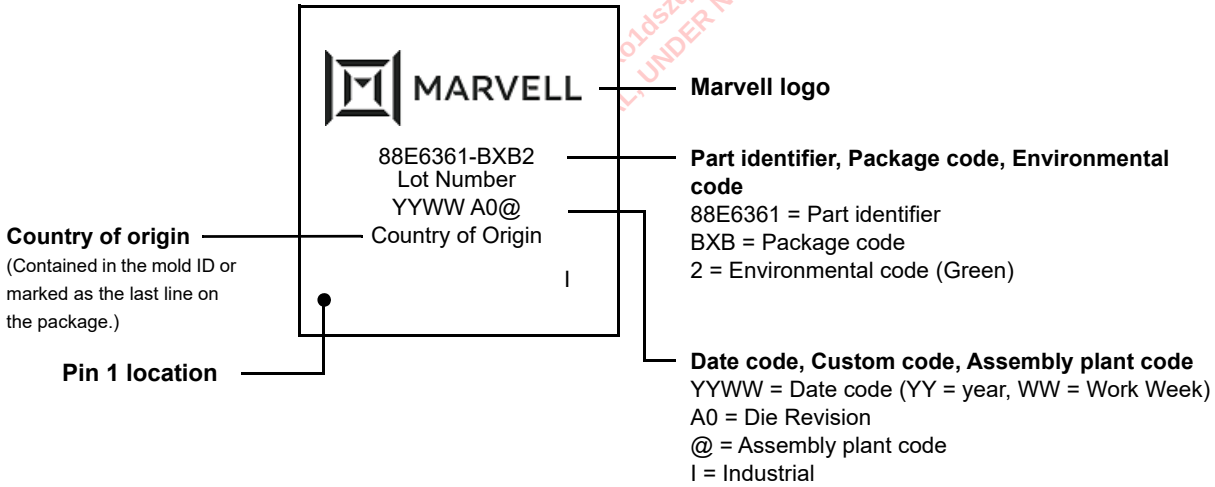


Note: The above drawing is not drawn to scale. Location of markings is approximate.

5.2.2 Industrial Package Marking

Figure 40 shows a sample Industrial package marking and pin A1 location for the 88E6361 device.

Figure 40: Industrial Package Marking and Ball 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

A Revision History

Table 60: Revision History

Revision	Date	Description
Rev. 2	December 9, 2021	Transition Addendum from Preliminary to Final status.
Rev. 1	October 8, 2021	Initial release, formal. Added word “Preliminary” to titles, updated Revision History.
	September 30, 2021	Initial release. Not approved by Document Control version for customer initial release.

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Doc. No. TD-001867 Rev. 2 Revised: December 9, 2021