SFF specifications are available at http://www.snia.org/sff/specifications
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This specification was developed by the SFF Committee prior to it becoming the SFF TA (Technology Affiliate) TWG (Technical Working Group) of SNIA (Storage Networking Industry Association).

The information below should be used instead of the equivalent herein.

POINTS OF CONTACT:

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If you are interested in participating in the activities of the SFF TWG, the membership application can be found at:
http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on can be found at:
http://www.snia.org/sff/specifications/SFF-8000.TXT

The operations which complement the SNIA's TWG Policies & Procedures to guide the SFF TWG can be found at:
http://www.snia.org/sff/specifications/SFF-8032.PDF

Suggestions for improvement of this specification will be welcome, they should be submitted to:
http://www.snia.org/feedback

SFF Committee documentation may be purchased in hard copy or electronic form.
SFF specifications are available at ftp://ftp.seagate.com/sff

SFF Committee

INF-8077i

10 Gigabit Small Form Factor Pluggable Module

Revision 4.5 August 31, 2005

Secretariat: SFF Committee

Abstract: This specification defines the electrical, management, and mechanical interfaces of the XFP module. The module is a hot pluggable small footprint serial-to-serial data-agnostic multirate optical transceiver, intended to support Telecom (SONET OC-192 and G.709 “OTU-2”) and Datacom applications (10 Gb/s Ethernet and 10 Gb/s Fibre Channel). Nominal data rates range from 9.95 Gb/s, 10.31 Gb/s, 10.52 Gb/s, 10.70 Gb/s, and the emerging 11.09 Gb/s. The modules support all data encodings for these technologies. The modules may be used to implement single mode or multi-mode serial optical interfaces at 850 nm, 1310 nm, or 1550 nm. The XFP module design may use one of several different optical connectors. An adaptable heatsink option allows a single module design to be compatible with a variety of hosts.

Support: This document was adopted by the XFP MSA and is provided to the SFF for distribution and as a source document for related SFF projects.

Documentation: This document has been prepared according to the guidelines and agreements of the XFP MSA. The XFP MSA has the stated intention of encouraging broad and rapid industry adoption of the specification. The XFP specification and the technologies it uses may be offered to formal standards bodies to further support the adoption of the specification.

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If you are not a member of the SFF Committee, but you are interested in participating, the following principles have been reprinted here for your information.

PRINCIPLES OF THE SFF COMMITTEE

The SFF Committee is an ad hoc group formed to address storage industry needs in a prompt manner. When formed in 1990, the original goals were limited to defining de facto mechanical envelopes within which disk drives can be developed to fit compact computer and other small products.

In November 1992, the SFF Committee objectives were broadened to encompass other areas which needed similar attention, such as pinouts for interface applications, and form factor issues on larger disk drives. SFF is a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Documents created by the SFF Committee are expected to be submitted to bodies such as EIA (Electronic Industries Association) or an ANSI Accredited Standards Committee. They may be accepted for separate standards, or incorporated into other standards activities.

The principles of operation for the SFF Committee are not unlike those of an accredited standards committee. There are 3 levels of participation:

- Attending the meetings is open to all, but taking part in discussions is limited to member companies, or those invited by member companies
- The minutes and copies of material which are discussed during meetings are distributed only to those who sign up to receive documentation.
- The individuals who represent member companies of the SFF Committee receive documentation and vote on issues that arise. Votes are not taken during meetings, only guidance on directions. All voting is by letter ballot, which ensures all members an equal opportunity to be heard.

Material presented at SFF Committee meetings becomes public domain. There are no restrictions on the open mailing of material presented at committee meetings. In order to reduce disagreements and misunderstandings, copies must be provided for all agenda items that are discussed. Copies of the material presented, or revisions if completed in time, are included in the documentation mailings.

The sites for SFF Committee meetings rotate based on which member companies volunteer to host the meetings. Meetings have typically been held during the INCITS T10 weeks. The meetings of the SFF Special Subject Working Group on Transceivers have typically been held during INCITS T11 weeks.

The funds received from the annual membership fees are placed in escrow, and are used to reimburse ENDL for the services to manage the SFF Committee.

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- The current revision of all the SFF Specifications, as well as any previous revisions distributed during the current year.

Meeting documentation contains:
- Minutes for the current meeting cycle.
- Copies of Specifications revised during the current meeting cycle.

Each electronic document mailing obsoletes the previous mailing of that year e.g. July replaces May. To build a complete set of archives of all SFF documentation, retain the last SFF CD_Access mailing of each year.

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Foreword for SFF documents

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers in which space was at a premium and time to market with the latest machine was an important factor. System integrators worked individually with vendors to develop the packaging. The result was wide diversity, and with space being such a major consideration in packaging, it was not possible to replace one vendor's drive with a competitive product.

The desire to reduce disk drive sizes to even smaller dimensions such as 1.8" and 1.3" made it likely that devices would become even more constrained in dimensions because of a possibility that such small devices could be inserted into a socket, not unlike the method of retaining semiconductor devices.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology in disk drives. After two informal gatherings on the subject in the summer of 1990, the SFF Committee held its first meeting in August.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced problems other than the physical form factors of disk drives. In November 1992, the members approved an expansion in charter to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

At the same time, the principle was adopted of restricting the scope of an SFF project to a narrow area, so that the majority of documents would be small and the projects could be completed in a rapid timeframe. If proposals are made by a number of contributors, the participating members select the best concepts and uses them to develop specifications which address specific issues in emerging storage markets.

Those companies which have agreed to support a documented specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

Suggestions for improvement of this document will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070. The suggestions should additionally be sent to the XFP Chair and Technical Editor.

The development work on this specification was done by the XFP Group, an industry MSA.

SFF Specifications

There are several projects active within the SFF Committee. At the date of printing, document numbers had been assigned to the following projects. The status of Specifications is dependent on committee activities.

F = Forwarded	The document has been approved by the members for forwarding to a formal standards body.
P = Published	The document has been balloted by members and is available as a published SFF Specification.
A = Approved	The document has been approved by ballot of the members and is in preparation as an SFF Specification.
C = Canceled	The project was canceled, and no Specification was Published.
D = Development	The document is under development at SFF.
E = Expired	The document has been published as an SFF Specification, and the members voted against re-publishing it when it came up for annual review.
e = electronic	Used as a suffix to indicate an SFF Specification which has Expired but is still available in electronic form from SFF e.g. a specification has been incorporated into a draft or published standard which is only available in hard copy.
i = Information	The document has no SFF project activity in progress, but it defines features in developing industry standards. The document was provided by a company, editor of an accredited standard in development, or an individual. It is provided for broad review (comments to the author are encouraged).

s = submitted The document is a proposal to the members for consideration to become an SFF Specification.

Spec #	Rev	List of Specifications as of March 3, 2003
SFF-8000		SFF Committee Information
INF-8001i	E	44-pin ATA (AT Attachment) Pinouts for SFF Drives
INF-8002i	E	68-pin ATA (AT Attachment) for SFF Drives
SFF-8003	E	SCSI Pinouts for SFF Drives
SFF-8004	E	Small Form Factor 2.5" Drives
SFF-8005	E	Small Form Factor 1.8" Drives
SFF-8006	E	Small Form Factor 1.3" Drives
SFF-8007	E	2mm Connector Alternatives
SFF-8008	E	68-pin Embedded Interface for SFF Drives
SFF-8009	4.1	Unitized Connector for Cabled Drives
SFF-8010	E	Small Form Factor 15mm 1.8" Drives
INF-8011i	E	ATA Timing Extensions for Local Bus
SFF-8012	3.0	4-Pin Power Connector Dimensions
SFF-8013	E	ATA Download Microcode Command
SFF-8014	C	Unitized Connector for Rack Mounted Drives
SFF-8015	E	SCA Connector for Rack Mounted SFF SCSI Drives

Spec #	Rev	List of Specifications as of March 3, 2003
SFF-8016	C	Small Form Factor 10mm 2.5" Drives
SFF-8017	E	SCSI Wiring Rules for Mixed Cable Plants
SFF-8018	E	ATA Low Power Modes
SFF-8019	E	Identify Drive Data for ATA Disks up to 8 GB
INF-8020i	E	ATA Packet Interface for CD-ROMs
INF-8028i	E	- Errata to SFF-8020 Rev 2.5
SFF-8029	E	- Errata to SFF-8020 Rev 1.2
SFF-8030	1.8	SFF Committee Charter
SFF-8031		Named Representatives of SFF Committee Members
SFF-8032	1.5	SFF Committee Principles of Operation
INF-8033i	E	Improved ATA Timing Extensions to 16.6 MBs
INF-8034i	E	High Speed Local Bus ATA Line Termination Issues
INF-8035i	E	Self-Monitoring, Analysis & Reporting Technology
INF-8036i	E	ATA Signal Integrity Issues
INF-8037i	E	Intel Small PCI SIG
INF-8038i	E	Intel Bus Master IDE ATA Specification
INF-8039i	E	Phoenix EDD (Enhanced Disk Drive) Specification
SFF-8040	1.2	25-pin Asynchronous SCSI Pinout
SFF-8041	C	SCA-2 Connector Backend Configurations
SFF-8042	C	VHDCI Connector Backend Configurations
SFF-8043	E	40-pin MicroSCSI Pinout
SFF-8045	4.5	40-pin SCA-2 Connector w/Parallel Selection
SFF-8046	E	80-pin SCA-2 Connector for SCSI Disk Drives
SFF-8047	C	40-pin SCA-2 Connector w/Serial Selection
SFF-8048	C	80-pin SCA-2 Connector w/Parallel ESI
SFF-8049	E	80-conductor ATA Cable Assembly
INF-8050i	1.0	Bootable CD-ROM
INF-8051i	E	Small Form Factor 3" Drives
INF-8052i	E	ATA Interface for 3" Removable Devices
SFF-8053	5.5	GBIC (Gigabit Interface Converter)
SFF-8054		Automation Drive Interface Connector
INF-8055i	E	SMART Application Guide for ATA Interface
SFF-8056	C	50-pin 2mm Connector
SFF-8057	E	Unitized ATA 2-plus Connector
SFF-8058	E	Unitized ATA 3-in-1 Connector
SFF-8059	E	40-pin ATA Connector
SFF-8060	1.1	SFF Committee Patent Policy
SFF-8061	1.1	Emailing drawings over the SFF Reflector
SFF-8062		Rolling Calendar of SSWGs and Plenaries
SFF-8065	C	40-pin SCA-2 Connector w/High Voltage

Spec #	Rev	List of Specifications as of March 3, 2003
SFF-8066	C	80-pin SCA-2 Connector w/High Voltage
SFF-8067	3.0	40-pin SCA-2 Connector w/Bidirectional ESI
INF-8068i	1.0	Guidelines to Import Drawings into SFF Specs
SFF-8069	E	Fax-Access Instructions
INF-8070i	1.3	ATAPI for Rewritable Removable Media
SFF-8072	1.2	80-pin SCA-2 for Fibre Channel Tape Applications
SFF-8073	C	20-pin SCA-2 for GBIC Applications
INF-8074i	1.0	SFP (Small Formfactor Pluggable) Transceiver
SFF-8075	1.0	PCI Card Version of SFP Cage
SFF-8076	-	SFP Additional IDs
INF-8077i	3.0	XFP
SFF-8078		XFP-E
SFF-8080	E	ATAPI for CD-Recordable Media
SFF-8082		Labeling of Ports and Cable Assemblies
INF-8090i	5.4	ATAPI for DVD (Digital Video Data)
SFF-8101	C	3 Gbs and 4 Gbs Signal Characteristics
SFF-8110	C	5V Parallel 1.8" drive form factor
SFF-8111	1.3	1.8" drive form factor (60x70mm)
SFF-8120	2.6	1.8" drive form factor (78x54mm)
SFF-8200e	1.1	2 1/2" drive form factors (all of 82xx family)
SFF-8201e	1.3	2 1/2" drive form factor dimensions
SFF-8212e	1.2	2 1/2" drive w/SFF-8001 44-pin ATA Connector
SFF-8221	2.0	Pre-Aligned 2.5" Drive >10mm Form Factor
SFF-8222	1.1	2.5" Drive w/SCA-2 Connector
SFF-8223	0.4	2.5" Drive w/Serial Attachment Connector
SFF-8225	C	2.5" Single Voltage Drive
SFF-8300	1.2	3 1/2" drive form factors (all of 83xx family)
SFF-8301	1.4	3 1/2" drive form factor dimensions
SFF-8302e	1.1	3 1/2" Cabled Connector locations
SFF-8323	0.4	3 1/2" drive w/Serial Attachment Connector
SFF-8332e	1.2	3 1/2" drive w/80-pin SFF-8015 SCA Connector
SFF-8337e	1.2	3 1/2" drive w/SCA-2 Connector
SFF-8342e	1.3	3 1/2" drive w/Serial Unitized Connector
INF-8350i	6.1	3 1/2" Packaged Drives
SFF-8400	C	VHDCI (Very High Density Cable Interconnect)
SFF-8410	16.1	High Speed Serial Testing for Copper Links
SFF-8411		High Speed Serial Testing for Backplanes
SFF-8412	12.1	HSOI (High Speed Optical Interconnect) Testing
SFF-8415	4.1	HPEI (High Performance Electrical Interconnect)
SFF-8416	0.1	HPEI Measurement of Bulk Cable

Spec #	Rev	List of Specifications as of March 3, 2003
SFF-8420	11.1	HSSDC-1 Shielded Connections
SFF-8421	2.4	HSSDC-2 Shielded Connections
SFF-8422	C	FCI Shielded Connections
SFF-8423	C	Molex Shielded Connections
SFF-8424		Dual Row HSSDC-2 Shielded Connections
SFF-8425		Single Voltage Drives
SFF-8430	4.1	MT-RJ Duplex Optical Connections
SFF-8441	14.1	VHDCI Shielded Configurations
SFF-8451	10.1	SCA-2 Unshielded Connections
SFF-8452	3.1	Glitch Free Mating Connections for Multidrop Aps
SFF-8453		Shielded High Speed Serial connectors
SFF-8460	1.2	HSS Backplane Design Guidelines
SFF-8470	2.5	Multi Lane Copper Connector
SFF-8471	C	ZFP Multi Lane Copper Connector
SFF-8472	9.3	Diagnostic Monitoring Interface for Optical Xcvrs
INF-8475i	2.2	XPAK Small Formfactor Pluggable Receiver
SFF-8480	2.1	HSS (High Speed Serial) DB9 Connections
SFF-8482	0.0	Internal Serial Attachment Connector
SFF-8483	C	External Serial Attachment Connector
SFF-8500e	1.1	5 1/4" drive form factors (all of 85xx family)
SFF-8501e	1.1	5 1/4" drive form factor dimensions
SFF-8508e	1.1	5 1/4" ATAPI CD-ROM w/audio connectors
SFF-8523	0.4	5 1/4" drive w/Serial Attachment Connector
SFF-8551	3.2	5 1/4" CD Drives form factor
SFF-8572	C	5 1/4" Tape form factor
SFF-8610	C	SDX (Storage Device Architecture)

Document Sources

Copies of ANSI standards or proposed ANSI standards may be purchased from Global Engineering.

15 Inverness Way East	800-854-7179 or 303-792-2181
Englewood	303-792-2192Fx
CO 80112-5704	

Copies of SFF Specifications are available by joining the SFF Committee as an Observer or Member or by download at ftp://ftp.seagate.com/sff

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(10 Gigabit Small Form Factor Pluggable Module)

XFP Revision 4.5

Review Revision

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XFP Legal Disclaimer

This specification has been formally adopted by the XFP Promoters. Changes to the document may be made to correct any errata in the specification, including clarifications and other changes. Verify that you are using the latest revision of the specification by visiting the XFP web-site at www.xfpmsa.org.

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XFP Identification of defects

If errors are identified in this specification, please notify the chair and editor identified on the first page. Please provide a clear identification of the error, the text of any proposed correction, and a justification or explanation of the correction.

XFP Publication History

Revision Number	Description	Date
0.1	Initial Publication of Document, Preliminary	3/27/02
0.5	First full draft	4/11/02
0.7	Second full draft	5/23/02
0.8	Third full draft	6/21/02
0.9	Pre-Public Release 0	7/15/02
0.91	Pre-Public Release 1	7/16/02
0.92	1st-Public Release	7/19/02
0.93	Pre-Meeting Editing Draft	8/21/02
0.95	Internal draft	09/21/02
0.99	2nd pre-Public Release	10/31/02
1.0	Pre-Ratification Draft	12/2/02
2.0	Adoption Draft	12/16/02
3.0	Adopted Specification	3/3/03
3.1	Modified Copyright Statement	4/02/03
4.0	Adopted Specification. Updated CRC R/W, Updated Designations, and Updated Registers Nomenclature	4/13/04
4.1	I2C Errata, S-parameters adjustment, Annex E3, Correcting mixed mode equation of Annex C4, Annex for BER 1E-15, address role over	4/20/05
4.5	Non-EQJ Jitter definition, Annex E3, and Bail Color.	8/31/05

XFP Foreword

The XFP Promoters, Broadcom Corporation, Brocade Communications Systems, Inc., Ciena Corporation, Emulex Corporation, Finisar Corporation, Innovation Core SEI, Inc. (a Sumitomo Electric Company), JDS Uniphase Corporation, Maxim Integrated Products, Tyco Electronics Corporation, Velio Communication, and many contributors gathered together to develop a specification for a 10 Gigabit small foot print pluggable module. The Promoters stated a wish to encourage broad and rapid industry adoption of the specification. The XFP specification may be offered to formal standards bodies to further support the adoption of the specification. The XFP Promoters and Contributors solicited technical review and contributions to the XFP specification among many component, module, and system designers and manufacturers to assure that it meets a broad variety of requirements.

Signed agreements exist among the promoters and between the promoters and contributors that allowed them to carry forward these activities in a manner that encouraged rapid development, open sharing of technology, and the timely resolution of disagreements. The agreements further explained and protected the rights of both promoters and contributors. Similar agreements protect the rights of adopters of the specification.

Organizations may become adopters of the XFP specification by contacting any XFP Promoter and requesting the necessary forms and following the required procedures.

XFP Contributors

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Xilinx, Inc.

XFP Acknowledgments

The XFP members would like to acknowledge and thank Dr. Ali Ghiasi for his tremendous effort and diligence in editing this specification.

The members would like to thank Dr. Lew Aronson and Mr. Ed Bright for writing the Management and Mechanical chapters. In addition, they would like to thank Mr. Tom Lindsay for the jitter Appendix, Dr. Piero Bradley for jitter section, Mr. Lawrence Williams for the XFI Channel Simulation and Modeling and the Optimum Via Appendix, Mr. Henrik Johansen for the compliance test boards Appendix, Mr. Steve Silverman for the power supply section, Mr. Gary Heitkamp for the Thermal Appendix, Mr. Randy Clark for the 2-Wire Protocol, Mr. Ron Miller for the TDR Appendix, and Dr. Stefanos Sidiropoulos for the VPS section.

The members would also like to thank Mr. Robert Snively for skillfully steering the MSA, as without him we could not have achieved our goal.

Special thanks are due to all those who attended the meetings and made contributions, as this document is a collection of their work.

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XFP List of Tables

XFP List Figures

CHAPTER 1: SCOPE OF XFP SPECIFICATION

1.1 INTRODUCTION

This specification defines the electrical, management, and mechanical interfaces of the XFP module. The module is a hot pluggable small footprint serial-to-serial data-agnostic multirate optical transceiver, intended to support Telecom (SONET OC-192 and G.709 “OTU-2”) and Datacom applications (10 Gb/s Ethernet and 10 Gb/s Fibre Channel). Nominal data rates range from 9.95 Gb/s, 10.31 Gb/s, 10.52 Gb/s, 10.70 Gb/s, and the emerging 11.09 Gb/s. The modules support all data encodings for these technologies. The modules may be used to implement single mode or multi-mode serial optical interfaces at 850 nm, 1310 nm, or 1550 nm. The XFP module design may use one of several different optical connectors 5.17. An adaptable heatsink option allows a single module design to be compatible with a variety of hosts.

The XFP specification includes the following information:

- XFP reference model and description 3.2
- Chapter 2: XFP Electrical Interface , Low Speed Electrical Interface
- Chapter 3: High Speed Electrical Specification XFI , High speed 10 Gb/s serial electrical specification (XFI)
- Chapter 4: XFP 2-Wire Interface Protocol , XFP 2-Wire Interface Protocol
- Chapter 5: Management interface , Management and diagnostic interface
- Chapter 6: Mechanical and Board definition , Mechanical interface, including guides, EMI shields, module retention, cooling, and electrical connector.
- Appendixes providing implementation and measurement suggestions.
  - Appendix A: Application Reference Model
  - Appendix B: XFI Channel Measurements and Modeling
  - Appendix C: Differential S-Parameters and TDR
  - Appendix D: Optimum Via Design
  - Appendix E: Jitter Methodology and Measurement
  - Appendix G: Module Thermal Testing

1.2 REQUIREMENTS ON PRESS ANNOUNCEMENTS

All press announcements specifying XFP compliant modules and components shall include the following text to identify the origin of the XFP specification.

The XFP is a development activity promoted by Broadcom Corporation, Brocade Communications Systems, Inc., Emulex Corporation, Finisar Corporation, JDS Uniphase Corporation, Innovation Core SEI, Inc., Maxim Integrated Products, Ciena Corporation, Tyco Electronics Corporation, Velio Communication, and many contributors.

CHAPTER 2: XFP ELECTRICAL INTERFACE

2.1 INTRODUCTION

The XFI "Ziffy" is the high speed serial electrical interface for XFP modules with a nominal baudrate of 9.95-11.1 Gb/s. XFI connects a serial 9.95-11.1 Gb/s SerDes to a module over 300mm of improved FR4[1] material or up to 200mm of standard FR4 with one connector. The electrical interface is based on high speed low voltage AC coupled logic with a nominal differential impedance of 100 Ω. The XFP module could be an Electrical-to-Optical or an Electrical-to-Electrical device.

The XFP modules and the host system are hot-pluggable. The module or the host system shall not be damaged by unexpected insertion or removal of the module.

2.2 GENERAL REQUIREMENTS

All electrical specifications shall be met over the entire specified range of power supplies given in section 2.7.

All XFP electrical specifications apply over the Environmental and Thermal range described in section 6.13. If an extended operating range is specified by the module vendor (see 5.35), then the electrical specifications apply over this extended operating range.

2.3 XFP HOST CONNECTOR DEFINITION

The XFP host connector is based on a 0.8 mm pitch 30 position right angle connector 6.9. Host PCB pin assignment is given by Figure 1 and pin definition are listed in Table 1. All XFP compliance points are defined using this connector. An improved version of this connector will be available from Tyco and possibly from other sources. It is recommended that host systems use the new improved connector for better signal integrity and EMI.

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[1] Standard FR4 has a typical loss tangent of 0.022, where improved FR4 such as Nelco 4000-13 has a typical loss tangent of 0.016.

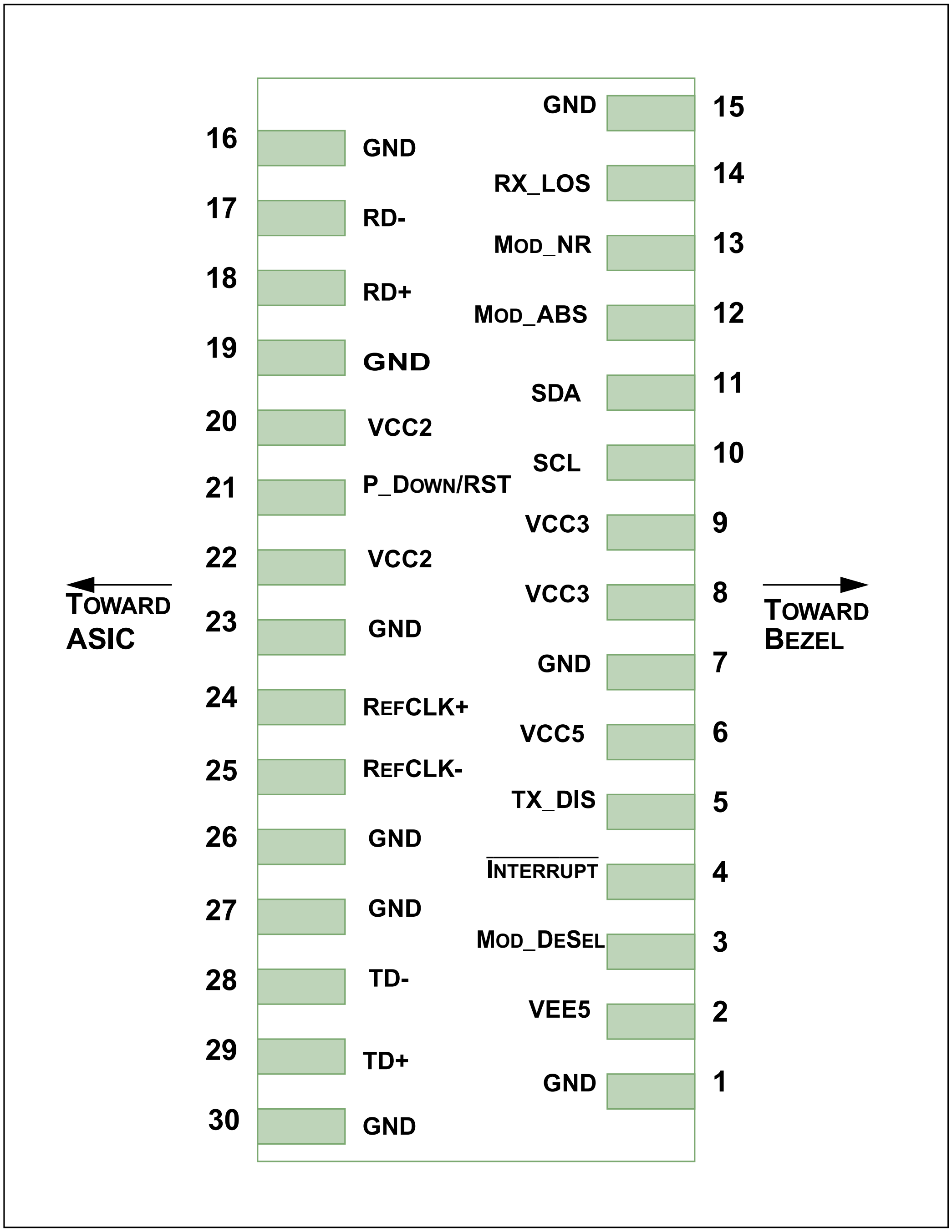

Figure 1 Host PCB XFP Pinout Top View

Table 1 Module Electrical Pin Definition

Pin	*Logic*	*Symbol*	*Name/Description*	*Note*
1		GND	Module Ground	1
2		VEE5	Optional -5.2V Power Supply	
3	LVTTL-I	Mod_DeSel	Module De-select; When held low allows module to respond to 2-wire serial interface	
4	LVTTL-O	$\overline{\text{Interrupt}}$	$\overline{\text{Interrupt}}$; Indicates presence of an important condition which can be read over the 2-wire serial interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		VCC5	+5V Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I/O	SCL	2-Wire Serial Interface Clock	2
11	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply	3
21	LVTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode.	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply	3
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board	
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board	
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	1

1. Module ground pins Gnd are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.
3. The 1.8 V power supply can be optionally programmed to voltages lower than 1.8 V in modules supporting the variable power supply.

2.4 LOW SPEED ELECTRICAL HARDWARE PINS

In addition to the 2-wire serial interface the XFP module has the following low speed pins for control and status:

- Mod_NR
- Mod_DeSel
- $\overline{\text{Interrupt}}$
- TX_DIS
- Mod_ABS
- RX_Los
- P_Down/RST.

2.4.1 MOD_NR

The Mod_NR is an output pin that when High, indicates that the module has detected a condition that renders transmitter and or receiver data invalid, shall consist of logical OR of the following signals:

- Transmit Signal Conditioner Loss of Lock
- Transmitter Laser Fault
- Receiver Signal Conditioner Loss of Lock

Other conditions deemed valuable to the detection of fault may be added to the Mod_NR.

The Mod_NR output pin is an open collector and must be pulled to Host_Vcc on the host board.

2.4.2 MOD_DESEL

The Mod_DeSel is an input pin. When held Low by the host, the module responds to 2-wire serial communication commands. The Mod_DeSel allows the use of multiple XFP modules on a single 2-wire interface bus. When the Mod_DeSel pin is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host. Mod_DeSel pin must be pulled to VCC3 in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the Mod_DeSel assert time after any XFP modules are deselected. Similarly, the host must wait at least for the period of the Mod_DeSel deassert time before communicating with the newly selected module. The assertion and de-assertion periods of different modules may overlap as long as the above timing requirements are met.

2.4.3 INTERRUPT

Interrupt is an output pin. When “Low”, indicates possible module operational fault or a status critical to the host system. The Interrupt pin is an open collector output and must be pulled up to Host_Vcc the host board.

2.4.4 TX_DIS

TX_DIS is an input pin. When TX_DIS is asserted High, the XFP module transmitter output must be turned off. The TX_DIS pin must be pulled up to VCC3 in the XFP module.

2.4.5 MOD_ABS

Mod_ABS is pulled up to Host_Vcc on the host board and grounded in the XFP module. Mod_ABS is then asserted “High” when the XFP module is physically absent from a host slot.

2.4.6 RX_LOS

The RX_LOS when High indicates insufficient optical power for reliable signal reception. The RX_LOS pin is an open collector output and must be pulled up to Host_Vcc on the host board.

2.4.7 P_DOWN/RST

This is a multifunction pin for module Power Down and Reset. The P_Down/RST pin must be pulled up to VCC3 in the XFP module.

2.4.7.1 POWER DOWN FUNCTION

The P_Down pin, when held High by the host, places the module in the standby (Low Power) mode with a maximum power dissipation of 1.5W. This protects hosts which are not capable of cooling higher power modules which may be accidentally inserted.

The module’s 2-wire serial interface and all laser safety functions must be fully functional in this low power mode. During P_Down, the module shall still support the completion of reset Interrupt, as well as maintain functionality of the variable power supply as described in section 5.7.

2.4.7.2 RESET FUNCTION

The negative edge of P_Down/RST signal initiates a complete module reset.

2.4.7.3 MODULE BEHAVIOR DURING POWER DOWN AND RESET

During execution of a reset (t_init) or while held in Power Down mode, a module may be unable to determine the correct value for Mod_NR and RX_LOS. These outputs as well as all interrupt related flags, except completion of Reset flag, shall be disregarded by the host. When the module completes a Reset and is not in Power Down mode, the module must represent the correct value of both signals on its outputs before posting a completion of reset interrupt to the host (see Table 39, bit 0 register address 84).

At no time shall a module cause spurious assertion of the Interrupt pin.

When a host initially applies power to a module with the P_Down/RST signal asserted, a module comes up in power down mode. The module shall only assert the Interrupt signal pin to inform the host it has completed a reset. The completion of reset flag (see Table 39, bit 0 register address 84) shall be the only interrupt source flag set during power down mode. The host is expected to clear this interrupt before releasing the module from the power down mode. The transition from power down mode to normal mode will trigger a reset of the module and result in a 2nd module reset and a 2nd reset completion interrupt to the host

2.5 LOW SPEED ELECTRICAL SPECIFICATIONS

Low speed signaling is based on Low Voltage TTL (LVTTL) operating at Vcc3 at a nominal supply of (3.3V ± 5%). Hosts shall use a pull-up resistor connected to a host_Vcc of +3.3 volts (3.15 to 3.45 volts) on the 2-wire interface SCL (clock), SDA (Data), and all low speed status outputs.

The XFP low speed electrical specifications are given in Table 2. This specification ensures compatibility between host bus masters and XFP SCL/SDA lines and compatibility with I^2C.

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Table 2 Low speed control and sense signals, electronic characteristics

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
XFP Interrupt, Mod_NR, RX_LOS	V_{OL}	0.0	0.40	V	Rpullup pulled to host_Vcc, measured at host side of connector. $I_{OL}(max) = 3$ mA
	V_{OH}	host_Vcc - 0.5	host_Vcc + 0.3	V	Rpullup pulled to host_Vcc, measured at host side of connector.
XFP TX_Dis, P_Down/RST	V_{IL}	-0.3	0.8	V	Rpullup pulled to VCC3,measured at XFP side of connector. $I_{IL}(max) = -10$ uA
	V_{IH}	2.0	VCC3 + 0.3	V	Rpullup pulled to VCC3, measured at XFP side of connector. $I_{IH}(max) = 10$ uA
XFP SCL and SDA	V_{OL}	0.0	0.40	V	Rpullup[1] pulled to host_Vcc, measured at host side of connector. $I_{OL}(max) = 3$ mA
	V_{OH}	host_Vcc - 0.5	host_Vcc + 0.3	V	Rpullup[1] pulled to host_Vcc, measured at host side of connector.
XFP SCL and SDA	V_{IL}	-0.3	Vcc3*0.3	V	Rpullup[1] pulled to Host_VCC, measured at XFP side of connector. $I_{IL}(max) = -10$ uA
	V_{IH}	Vcc3*0.7	VCC3 + 0.5	V	Rpullup[1] pulled to Host_VCC, measured at XFP side of connector. $I_{IH}(max) = 10$ uA
Leakage Current	I_l	-10	10	µA	
Capacitance for XFP SCL and SDA I/O Pin	C_i		14	pF	10pF for XFP IC I/O pin, 4 pF for XFP PCB trace
Total bus capacitive load for SCL and for SDA	C_b		100	pF	At 400 KHz, 3.0 Kohms Rp, max At 100 KHz, 8.0 Kohms Rp, max
			400	pF	At 400 KHz, 0.80 Kohms Rp, max At 100 KHz, 2.0 Kohms Rp, max

1. For combinations of Rpullup (Rp), bus capacitance and speed, see Philips I^2C specification revision 2.1, figures 39 and 44. Rise and fall time measurement levels are defined in the XFP management interface ac electrical specifications. Active bus termination may be used by the host in place of a pullup resistor, as described in the Philips I2C specification

2.6 TIMING REQUIREMENT OF CONTROL AND STATUS I/O

The timing requirements of control and status I/O are defined inTable 3.

Table 3 Timing Parameters for XFP Management

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
TX_DIS assert time	t_off		10	µsec	rising edge of TX_DIS to fall of output signal below 10% of nominal
TX_DIS negate time	t_on		2	msec	Falling edge of TX_DIS to rise of output signal above 90% of nominal
Time to initialize	t_init		300	msec	From power on or hot plug after supply meeting Table 4 or from falling edge of P_Down/RST.
$\overline{\text{Interrupt}}$ assert delay	$\overline{\text{Interrupt}}$_on		200	msec	From occurrence of the condition triggering $\overline{\text{Interrupt}}$
$\overline{\text{Interrupt}}$ negate delay	$\overline{\text{Interrupt}}$_off		500	µsec	From clear on read $\overline{\text{Interrupt}}$ flags
P_Down/RST assert delay	P_Down/RST_on		100	µsec	From Power down initiation
Mod_NR assert delay	Mod_nr_on		1	msec	From Occurrence of fault to assertion of MOD_NR
Mod_NR negate delay	Mod_nr_off		1	msec	From clearance of signal to negation of MOD_NR
P-Down reset time		10		µsec	Min length of P-Down assert to initiate reset
RX_LOS assert delay	t_loss_on		100	µsec	From Occurrence of loss of signal to assertion of RX_LOS
RX_LOS negate delay	t_loss_off		100	µsec	From Occurrence of presence of signal to negation of RX_LOS

The 2-wire serial bus timing is described in Chapter 4: XFP 2-Wire Interface Protocol .

2.7 XFP POWER REQUIREMENT

The XFP host has 3 power supplies +1.8 V, +3.3 V, +5.0 V and an optional -5.2 V supply. The +1.8 V and +3.3 V supplies have two designated power pins in the connector for each power supply rail. The +5 V and -5.2 supplies have one designated power pin each. The maximum continuous or peak current carrying capacity for each connector pin is 500 mA.

The host system may alter the VCC2 supply to a voltage level lower that the nominal +1.8 V value. This mode of operation is *optional* and can be supported by modules and hosts that strive to meet lower power/current requirements. Modules supporting this optional lower power mode must be backwards compatible with modules and hosts supporting only 1.8 V on VCC2, i.e. modules implementing these optional modes must be able to operate normally with a voltage of +1.8 V applied on their VCC2 pins (albeit with higher power dissipation). For more details see section 5.7.

XFP module maximum power dissipation must meet one of the following classes:

- Power Level 1 modules – Up to 1.5 W
- Power Level 2 modules – Up to 2.5 W
- Power Level 3 modules – Up to 3.5 W
- Power Level 4 modules – Greater than 3.5 W

To avoid exceeding system power supply limits and cooling capacity, the module may be placed in the power down mode by pulling pin 21 High. This guarantees module operating in Low Power mode with maximum power dissipation of ≤ 1.5W.

A host board together with XFP module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host and limits inrush charge/current during hot plug insertion.

All specifications shall be met at the maximum power supply current. No power sequencing of the power supplies is required of the host system.

2.7.1 POWER NOISE OUTPUT

To limit wide band noise power, the host system and module shall each meet a maximum of 2% peak-peak noise when measured with a 1MHz low pass filter. In addition, the host system and the module shall each meet a maximum of 3% peak-peak noise when measured with a high pass filter from 1MHz-10 MHz.

The XFP port on a host board is tested with a resistive load in place of the XFP module, each voltage rail at maximum current supported by the host. Voltage is measured at the module side of the XFP connector. The test is performed with all other portions of the host board/system active. Hosts with multiple XFP modules shall test ports one at a time, with active XFPs in all the remaining ports.

The XFP module is tested with a high quality power supply connected through the sample filter Figure 3. Voltage is measured at the host side of the XFP connector, between the sample host filter network and the XFP. The module must pass this test in all operating modes. This test ensures the module will not couple excessive noise from inside the module back onto the host board.

2.7.2 POWER NOISE SUSCEPTIBILITY

A module will meet all electrical requirements and remain fully operational in the presence of noise on all voltage inputs. The recommended susceptibility test is to sweep a sinuosidal waveform on each voltage input, with peak amplitude as described in Figure 2. This test applies at minimum and maximum DC setpoint levels. It is also desirable for a module and host to each tolerate a degree of random or semi-random noise on all voltage pins simultaneously, but the characteristics of this noise are beyond the scope of this document.

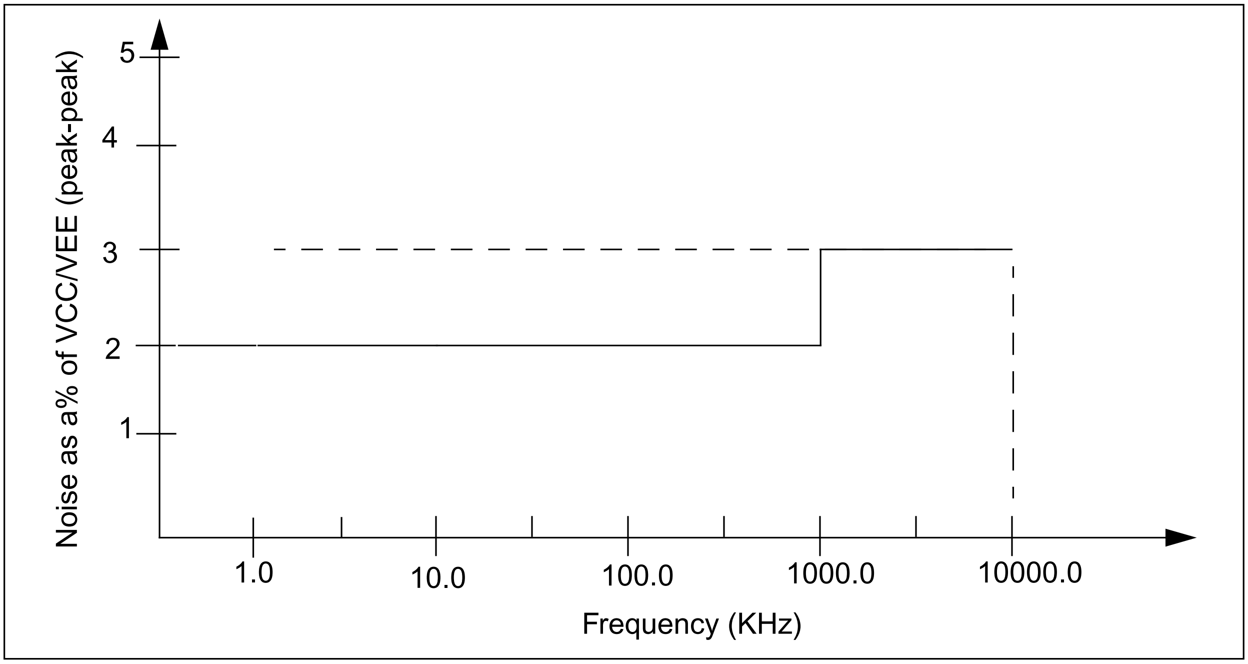

Figure 2 Power Noise Requirement

For power supply noise susceptibility testing and methodology see E.7.

2.7.3 HOST FILTERING

The example host board power supply filtering shown in Figure 3 will meet the noise filtering requirements in most systems. Other filtering implementations or local regulation may be used to meet the power noise output requirements described in section 2.7.1.

Any voltage drop across a filter network on the host is counted against the Host DC setpoint accuracy specification in Table 4. For this reason, the example filter illustrated in Figure 3 may not be appropriate for a host powering multiple XFPs and/or other host components from a shared voltage supply.

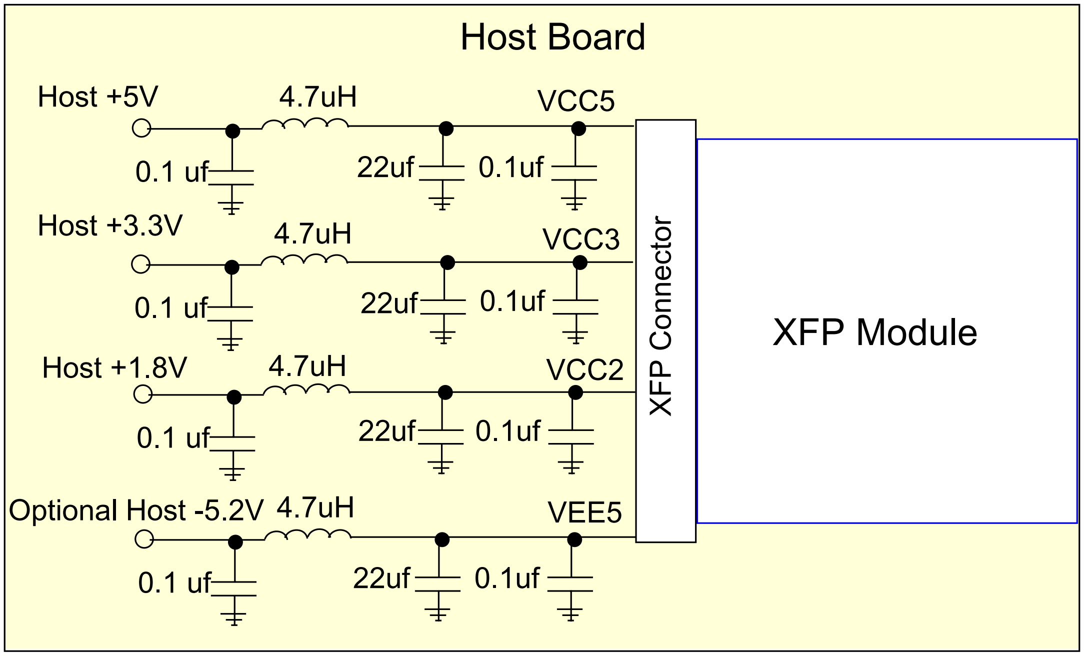

Figure 3 Example of Host Board Supply Filtering Network

Table 4 XFP Power Supply

Parameters	*Symbol*	*Conditions*	*Min*	*Max*	*Units*
VCC5 (5V)/VEE5 (-5.2V) Pin					
Power Supply Noise including Ripple [peak-to-peak]	VCC5/VEE5	see 2.7.1			%
Host DC set point accuracy			-5	+5	%
Module Maximum Current Inrush		Note 1		0.5	A
Module current ramp rate		Note 1		100	mA/µs
Maximum Power for the +5 and -5.2V Rail				2.5	W
Maximum Power for the +5 and -5.2V Rail During Power Down		Note 2		0.25	W
Host Bulk bypass capacitance for the module		Note 3	22		uF
VCC3 (3.3V) Rail					
Power Supply Noise including Ripple [peak-to-peak]	VCC3	see 2.7.1			%
Host DC set point accuracy			-5	+5	%
Module Maximum Current Inrush		Note 1		0.75	A
Module current ramp rate		Note 1		100	mA/µs
Maximum Power for the +3.3V Rail				2.5	W
Maximum Power for the +3.3V Rail During Power Down		Note 2		1	W
Host Bulk bypass capacitance for the module		Note 3	22		uF
VCC2 (1.8V) Rail					
Power Supply Noise including Ripple [peak-to-peak]	VCC2	see 4, 2.7.1			%
Host DC set point accuracy			-5	+5	%
Module Maximum Current Inrush		Note 1		1	A
Module current ramp rate		Note 1		100	mA/µs
Maximum Power for the 1.8V Rail				1.8	W
Maximum Power for the 1.8V Rail During Power Down		Note 2		1	W
Host Bulk bypass capacitance for the module		Note 3	22		uF

1. Modules which present a small capacitive load to the host during hotplug ($C \le 300nF$) are exempt from the inrush current requirements since they limit the total in rush charge.
2. Maximum module power dissipation shall not exceed 1.5 W.
3. Host provides bulk capacitance to suppress low frequency noise inside the XFP module. Host and module must each implement appropriate high frequency bypass to independently meet the noise requirement defined in section 2.7.1.
4. VCC2 can be optionally programmed to voltages less than 1.8V in modules supporting the Variable Power Supply 5.7.

2.8 ESD

The XFP module and host XFI pins (High Speed Pins) shall withstand 500 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The XFP module and all host pins with exception of the XFI pins (High Speed Pins) shall withstand 2KV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The XFP module shall meet ESD requirement given in EN61000-4-2, criterion B test specification such that units are subjected to 15KV air discharges during operation and 8KV direct contact discharges to the case.

CHAPTER 3: HIGH SPEED ELECTRICAL SPECIFICATION XFI

3.1 INTRODUCTION

XFI signaling is based on high speed low voltage logic, with nominal 100 Ohms differential impedance and AC coupled in the module. XFI was developed with the primary goal of low power and low Electro-Magnetic-Interference (EMI). To satisfy this requirement the nominal differential signal levels are 500 mV p-p with edge speed control to reduce EMI.

3.2 XFI APPLICATIONS DEFINITION

The application reference model for XFI, which connects a high speed ASIC/SERDES to the XFP module is shown in Figure 4. The XFI interface is designed to support SONET OC-192, IEEE.Std-802.3ae, 10GFC and G.709(OTU-2) applications. The SERDES is required to meet the application requirements for jitter generation and transfer when interfaced with a compliant XFP module through an XFP compliant channel. Modules or hosts designed only for 10 Gigabit Ethernet or 10GFC are not required to meet more stringent Telecom jitter requirements. XFI supported data rates are listed in Table 5. XFP compliant module are not required to support all the rates listed in Table 5 in simultaneously.

Table 5 XFI Supported Data Rates

Standard	*Description*	*Nominal Bit Rate*	*Units*
OC-192/SDH-64	SONET	9.95	Gigabaud
IEEE std-802.3ae	10 Gb/s Ethernet LAN PHY	10.31	Gigabaud
INCITS/T11 Project 1413-D	10GFC	10.52	Gigabaud
ITU G.709(OTU-2)	OC-192 Over FEC	10.70	Gigabaud
Emerging	10Gb/s Ethernet Over G.709	11.09	Gigabaud

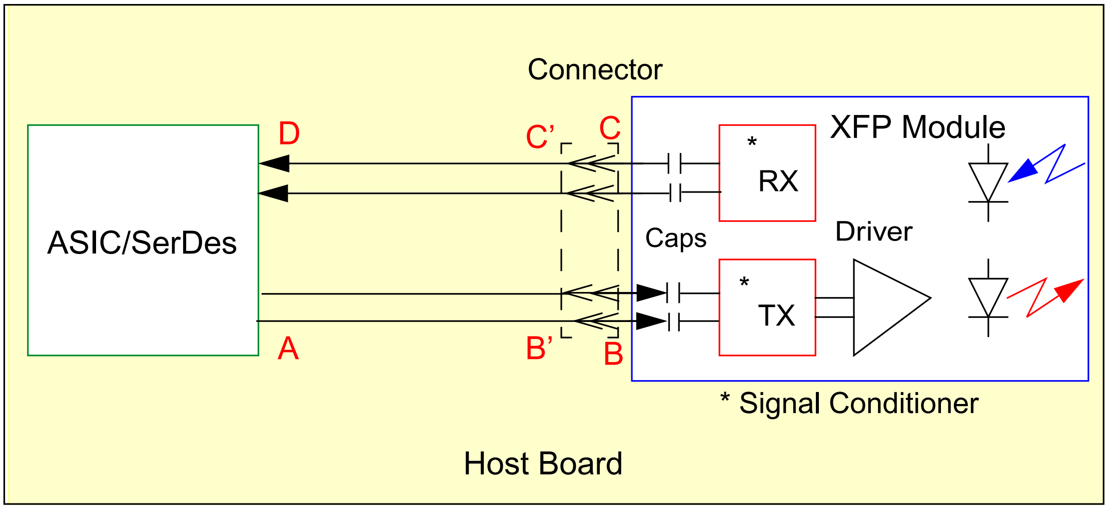

Figure 4 Application Reference Model

XFI Compliance points are defined as the following:

- A: SerDes transmitter output at ASIC/SerDes package pin on a DUT board 3.6 and A.1
- B: Host system SerDes output across the host board and connector at the Host Compliance Test Card 3.7.1 and A.2
- B': XFP transmitter input across the Module Compliance Test Board 3.8.1 and A.3.
- C: Host system input at the Host Compliance Test Card input 3.7.2 and A.2
- C': XFP module output across the Module Compliance Test Board 3.8.2 and A.3.
- D: ASIC/SerDes input package pin on the DUT board 3.6.2 and A.1.

ASIC/SerDes compliance points are informative.

3.3 XFI TERMINATION AND DC BLOCKING

The XFI link requires nominal 100 Ω differential source and load terminations on both the host board and the module. The XFI terminations shall provide both differential and common mode termination to effectively absorb differential and common mode noise and reflections as described:

- ASIC/SerDes – Table 8 and Table 10
- Host – Table 12 and Table 14
- Module – Table 17 and Table 18.

All XFI transmitters and receivers are AC coupled. XFP modules shall incorporate blocking capacitors on all XFI lines as shown in Figure 5. Resistor R_p and R_n each have a nominal 50 Ω value, together forming 100 Ω differential input. Some implementation may also use a resistor R_t from the common point to the termination voltage.

XFI differential reference impedance for driver, transmission line, and receivers are defined as 100 Ohms. XFI common mode reference impedance for driver, transmission lines, and receivers are specified as 25 Ohms.

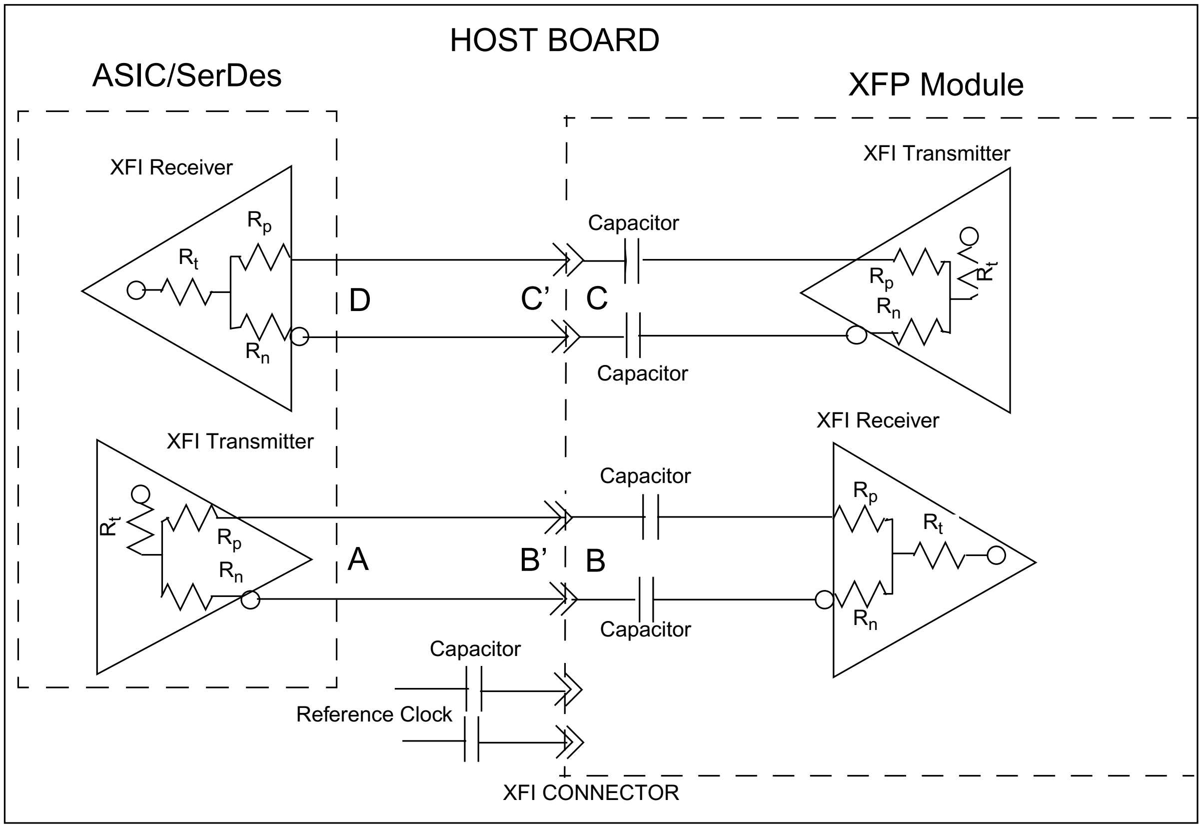

Figure 5 XFI Termination and AC Coupling

3.4 XFI JITTER DEFINITIONS

The XFI total jitter (TJ) consists of Random Jitter (RJ), Duty Cycle Distortion (DCD), Periodic Jitter (PJ), and Inter symbol Interference (ISI). For general jitter definitions and properties please see MJSQ[1].

XFI defines the term non-EQJ jitter which helps in the definition of links with receive equalization. non-EQJ jitter is related to jitter components defined in MJSQ by the following relationship:

$$non - EQJ = TJ - ISI = (RJ + DCD + PJ)$$

3.5 XFI COMPLIANCE CHANNEL

The XFI compliance channel consists of PCB traces, Vias, and the XFP connector 6.9. The PCB traces differential impedance is recommended to meet 100 ±10Ω.

The XFI channel has a loss budget of 9.6 dB allocated as shown in Table 6. Due to rounding, actual budgets may be slightly different than 9.6 dB.

Table 6 XFI Loss Budget

Parameter	*Symbol*	*Conditions*	*Max*	*Units*
Channel Loss Including Connector [1]		at 5.5 GHz	6.0	dB
Channel Crosstalk and Reflection Margin			3.6	dB
Total Channel Loss			9.6	dB
1. Loss allocated to the connector is 0.5 dB at 5.5 GHz.				

Based on measurement and simulation of compliance channel, the worst case channel transfer SDD21 shall meet:

$$SDD21(dB) = (-0.1 - 0.78 \times \sqrt{f} - 0.74 \times f)$$

where the variable *f* (frequency) unit is in GHz. The above equation is specified in terms of two ports S-parameters assuming the channel meets

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[1] Information Technology - Fibre Channel - Methodologies for Jitter and Signal Quality Specification - MJSQ, Project 1316-DT/Rev 14, June 9, 2004.

XFI return loss, therefore differential coupling effects may be neglected for insertion loss S21. Please see Appendix C: for differential measurements and conversions.

The above equation is valid from 250MHz to 7 GHz. An approximate diagram is shown in Figure 6.

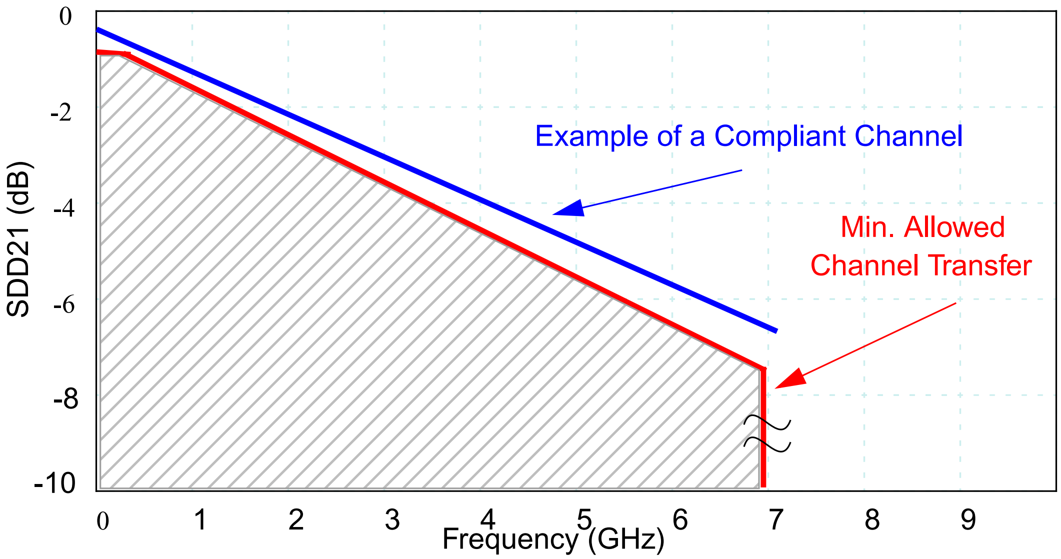

Figure 6 Channel Transfer Model

The channel transfer model is given by two port S-parameters SDD21 in Figure 6. Detailed descriptions of two port and 4 port measurements and conversions are provided in Appendix C:.

Architectural Note

For loosely coupled symmetrical structures, differential SDD21 may be approximated by direct measurement of S21.

The XFI compliance channel must meet a differential return loss of 10 dB from 1MHz-7500MHz. For frequencies in the range of 7.5 to 15 GHz channel return loss is given by:

$$SDD11(dB) = 10 - 25Log_{10}\left(\frac{f}{7.5}\right)$$

where variable *f* (frequency) is in GHz.

A host board meeting the Channel Transfer Model given by Figure 6 may be implemented with Microstrip or Stripline. A list of common host board configurations with maximum recommended host PCB trace lengths are listed in Table 7.

Table 7 Host Board Configuration

Type	*Material*	*Trace Width (mm)*	*Loss Tan*	*Copper (oz)*	*Trace Length (mm)*
Microstrip	4000-6	0.3	0.025	1	200
	4000-13	0.3	0.016	1	300
Stripline	4000-6	0.125	0.025	1/2	150
	4000-13	0.125	0.016	1/2	200

Architectural Note

Use of lossy materials or finer traces may be beneficial for short channels since they introduce additional attenuation, which in turn, improves Return Loss.

3.6 XFI ASIC/SERDES SPECIFICATION

XFI ASIC/SerDes specifications are informative. XFI ASIC/SerDes Transmitter specifications at compliance point A are given in 3.6.1. XFI ASIC/SerDes Receiver specifications at compliance point D are given in 3.6.2.

3.6.1 XFI ASIC/SERDES TRANSMITTER OUTPUT SPECIFICATIONS AT A (INFORMATIVE)

The XFI driver is based on low voltage high speed driver logic with a nominal differential impedance of 100 Ω. The XFI transmitter electrical specifications at compliance point A are given in Table 8. The source must provide both differential and common mode termination for quality signal termination and low EMI.

Return loss at A is measured with the SerDes on a DUT board as shown in A.1.

Table 8 XFI ASIC/SerDes Transmitter Output Electrical Specifications at A

Parameter - A	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Reference Differential Impedance	Z_d	See Figure 5		100		Ω
Termination Mismatch	ΔR_M	See E.6, Figure 5			5	%
DC Common Mode Voltage	Vcm		0		3.6	V
Output Rise and Fall time (20% to 80%)	t_{RH}, t_{FH}		24			ps
Output AC Common Mode Voltage		See E.5			15	mV (RMS)
Differential Output Return Loss [1]	SDD22	0.05-0.1 GHz	20			dB
		0.1-7.5 GHz	10			dB
		7.5-15 GHz	see 2			
Common Mode Output Return Loss [2]	SCC22	0.1-15 GHz	6			dB

1. Return Loss given by equation SDD22(dB)= 10 - 16.6 Log10(f/7.5), with f in GHz.
2. Common mode reference impedance is 25 Ω. Common Mode Return Loss helps absorb reflections and noise for EMI.

Transmitter jitter specifications are listed in Table 9. Figure 7 gives the compliance eye mask.

Table 9 XFI ASIC/SerDes Transmitter Output Jitter Specifications at A

Transmitter - A	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Determinstic Jitter	DJ	See E.1, 1			0.15	UI (p-p)
Total Jitter	TJ	See E.1, 1			0.30	UI (p-p)
Eye Mask	X1				0.15	UI
Eye Mask	X2				0.4	UI
Eye Mask	Y1		180			mV
Eye Mask	Y2				385	mV
Jitter Generation for Telecom Applications		50KHz to 8 MHz see 2			6.5	mUI (RMS)

1. In loop timing mode, includes jitter that transfers through the ASIC from the receiver during any valid operational input conditions.
2. Measured with a filter with 50 KHz high-pass cutoff desinged frequency and 8 MHz low pass cut off frequency. The filter rolls off at least for one decade on each side of the passband with -20 dB/Dec. Does not apply to a host designed with Optional Synchronous CMU clock, when used in conjunction with a Synchronous CMU module 3.10.1.

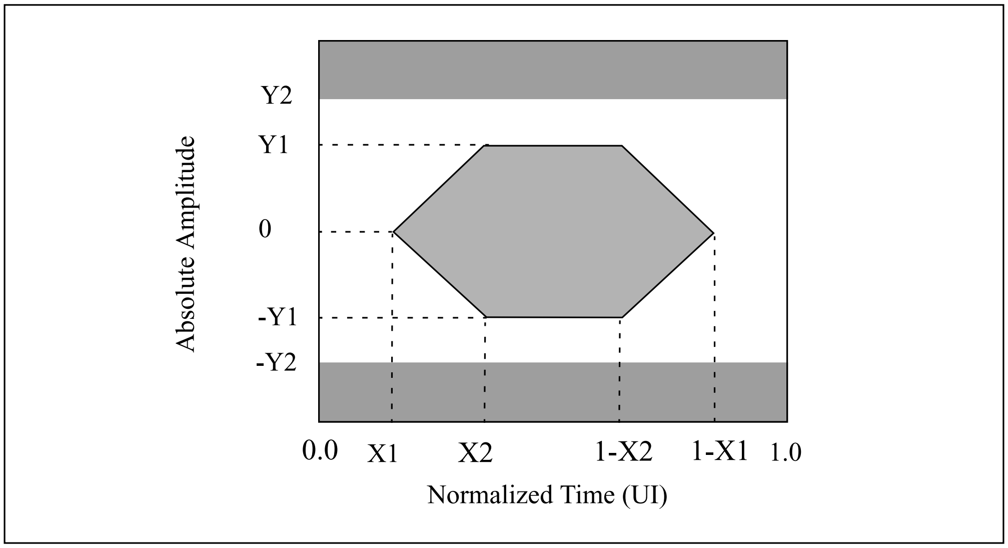

Figure 7 XFI ASIC/SerDes Transmitter Differential Output Compliance Mask at A

3.6.2 XFI ASIC/SERDES RECEIVER INPUT SPECIFICATIONS AT D (INFORMATIVE)

XFI receiver electrical specifications are given in Table 10 and measured at compliance point D. The return loss at D is measured with the SerDes on a DUT board A.1. Receiver input impedance is 100 Ohms differential. The load must provide differential termination and minimize differential to common mode conversion for high quality signal termination and low EMI, as given by Table 10.

Table 10 XFI ASIC/SerDes Receiver Electrical Input Specifications at D

Parameter - D	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Reference Differential Impedance	Z_d	See Figure 5		100		Ω
Termination Mismatch	ΔZ_M	See E.6, Figure 5			5	%
AC Common Mode Voltage		See E.5			25	mV (RMS)
Differential Input Return Loss	SDD11	0.05-0.1 GHz	20			dB
		0.1-7.5 GHz	10			dB
		7.5-15 GHz	see 1			
Common Mode Input Return Loss[2]	SCC11	0.1-15 GHz	6			dB
Differential to Common Mode Input Conversion[2]	SCD11	0.1-15 GHz	12			dB

1. Return Loss given by equation SDD11(dB)= 10 - 16.6 Log10(f/7.5), with f in GHz C.4.
2. Common mode reference impedance is 25 Ω. SCD11 relates to conversion of differential to common mode and the associated generation of EMI C.4

The XFI jitter specifications at reference D are listed in Table 11 and the compliance mask is shown in Figure 8. Only a compliant transmitter passing through the XFI channel is guaranteed for interoperablity.

Table 11 XFI ASIC/SerDes Receiver Input Jitter Specifications at D

Receiver- D	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Total Jitter	TJ	See E.1, E.2			0.65	UI (p-p)
Total non-EQJ Jitter		See E.1, E.2			0.45	UI (p-p)
Sinusoidal Jitter Tolerance	SJ	E.3			see 1	
Eye Mask	X1	Note [2]			0.325	UI
Eye Mask	Y1		55			mV
Eye Mask	Y2	Note [3]			525	mV

1. Sinuosidal jitter tolerance for Telecom and Datacom respectively given by Figure 9 and Figure 10.
2. Mask coordinate X1=0.225 if total non-EQJ jitter is measured.
3. Out of 525 mV, 100 mV is allocated for multiple reflection.

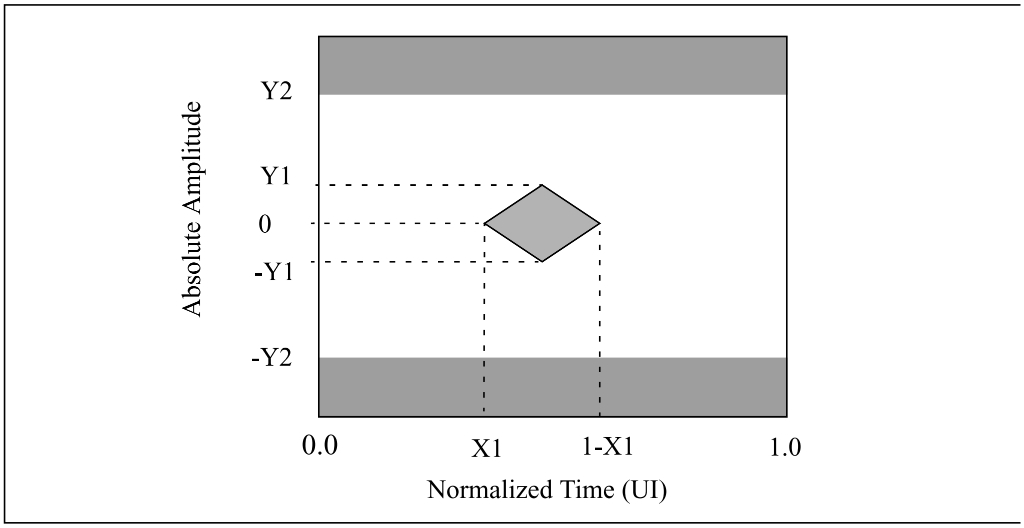

Figure 8 XFI ASIC/SerDes Receiver Differential Input Compliance Mask

An XFI receiver for Telecom (SONET OC-192 and G. 709 “OTU-2”) applications must meet jitter tolerance given by Figure 9 with the addition of input jitter given by Table 11. An XFI receiver for Datacom (Ethernet 802.3ae or Fibre Channel 10GFC) must meet the jitter tolerance given by Figure 10 with the addition of random and deterministic jitter given by Table 11.

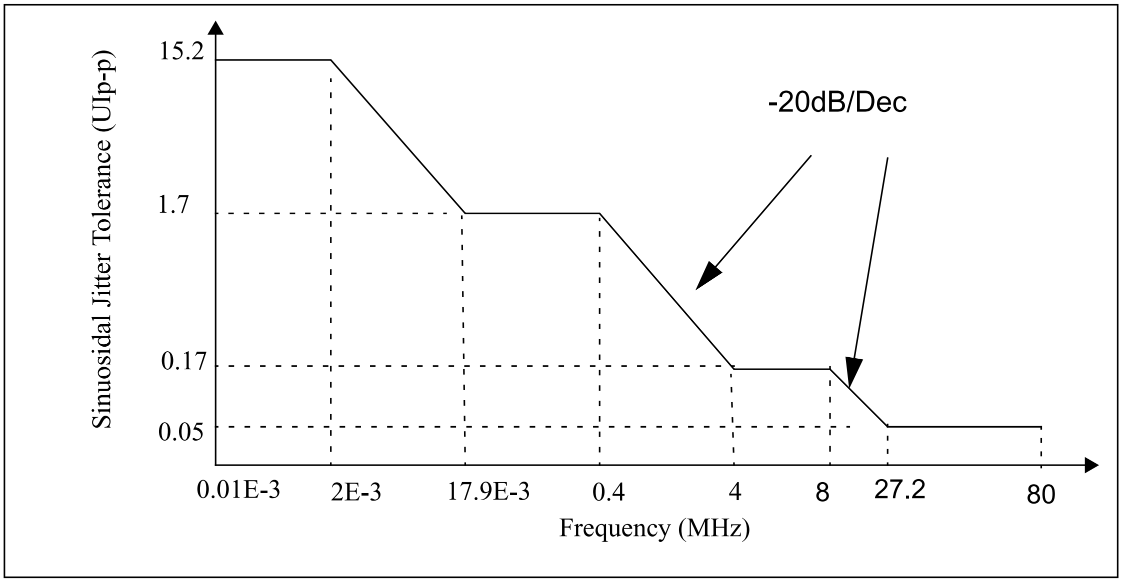

Figure 9 XFI ASIC/SerDes Receiver Input Telecom Sinuosidal Jitter

Tolerance

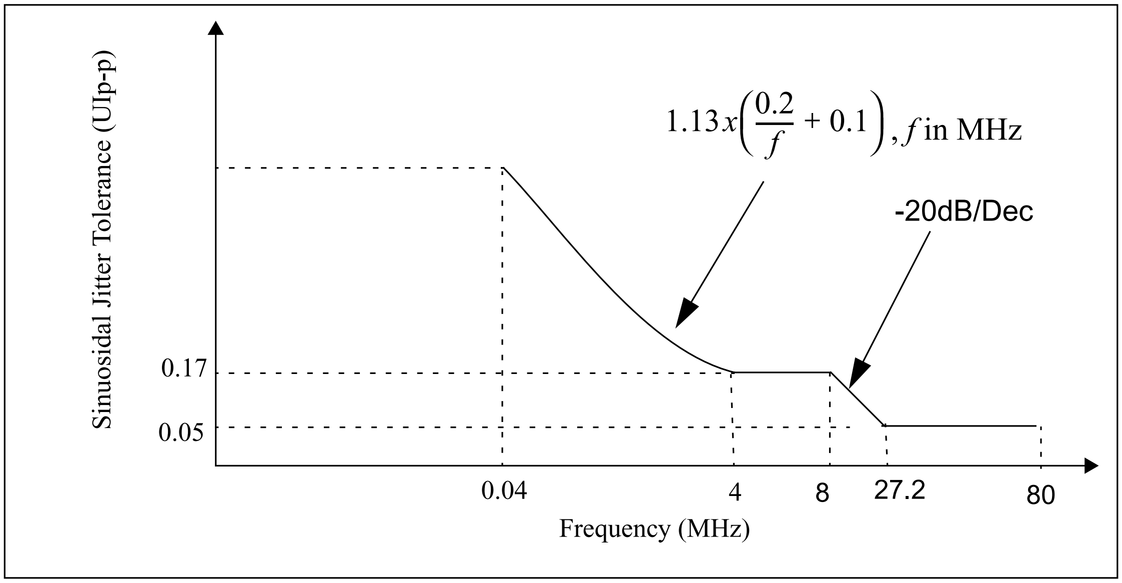

Figure 10 XFI ASIC/SerDes Receiver Input Datacom Sinuosidal Jitter Tolerance

3.7 XFI HOST SYSTEM SPECIFICATION

XFI Host system transmitter specifications at compliance point B are given in 3.7.1. XFI Host system receiver specifications at compliance point C are given in 3.7.2.

3.7.1 XFI HOST TRANSMITTER OUTPUT SPECIFICATIONS AT B

XFI Host transmitter electrical specifications are given in Table 12 and measured at compliance point B.

Table 12 XFI Host Transmitter Output Electrical Specifications at B

Parameter - B	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Reference Differential Impedance	Z_d			100		Ω
Termination Mismatch	ΔZ_M	See E.6, Figure 5			5	%
DC Common Mode Voltage	Vcm		0		3.6	V
Output AC Common Mode Voltage		See E.5			25	mV (RMS)
Differential Output Return Loss	SDD22	0.05-0.1 GHz	20			dB
		0.1-5.5 GHz	8			dB
		5.5-12 GHz	see 1			
Common Mode Output Return Loss[2]	SCC22	0.1-12 GHz	3			dB

1. Return Loss given be equation SDD22(dB)= 8 - 20.66 Log10(f/5.5), with f in GHz.
2. Common mode reference impedance is 25 Ω. Common Mode Input return loss helps absorb reflections and noise reducing EMI.

The XFI jitter specifications at reference point B are listed in Table 13 and the compliance mask is shown in Figure 11. Only a compliant transmitter passing through the XFI channel is guaranteed for interoperablity.

Table 13 XFI Host Transmitter Output Jitter Specifications at B

Receiver- B	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Total Jitter [1,]	TJ	See E.1			0.61	UI
Total non-EQJ Jitter [1]		See E.1, E.2			0.41	UI
Eye Mask	X1	see 2			0.305	UI
Eye Mask	Y1		60			mV
Eye Mask	Y2	see 3			410	mV
Jitter Generation at B Telecom Applications		50KHz-8MHz, see 4			7	mUI (RMS)

1. In loop timing mode, includes jitter that transfers through ASIC from the receiver during any valid operational input conditions.
2. . Mask cordinate X1=0.205 if total non-EQJ jitter is measured.
3. Out of 410 mV, 25 mV is allocated for multiple reflection.
4. Measured with a filter with 50 KHz high-pass cutoff desinged frequency and 8 MHz low pass cut off frequency. The filter rolls off at least for one decade on each side of the passband with -20 dB/Dec. Does not apply to a host designed with Optional Synchronous CMU clock, when used in conjunction with a Synchronous CMU Signal Conditioner module see 3.10.1.

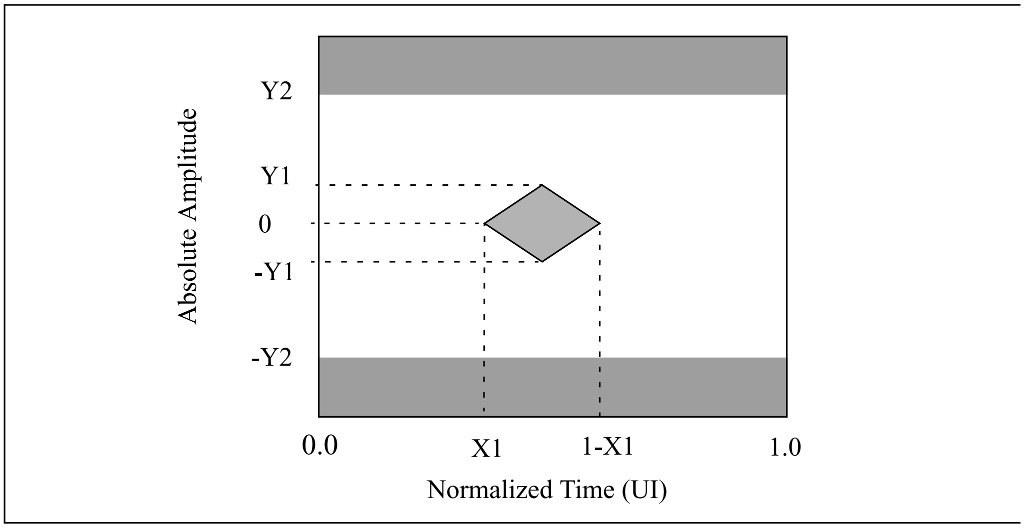

Figure 11 XFI Host Transmitter Differential Output Compliance Mask at B

3.7.2 XFI HOST RECEIVER INPUT SPECIFICATIONS AT C

The XFI Host receiver electrical specifications at compliance point C are given in Table 14. The load must provide differential termination and minimize differential to common mode conversion for quality signal termination and low EMI, as given in Table 14.

Return loss at compliance point C is measured with the Host Test Board plugged into the host as shown in A.2.

Table 14 XFI Host Receiver Input Electrical Specifications at C

Parameter - C	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Reference Differential Impedance	Z_d	See Figure 5		100		Ω
Termination Mismatch	ΔZ_M	See E.6, Figure 5			5	%
Source to Sink DC Potential Difference	Vcm		0		3.6	V
Input AC Common Mode Voltage		See E.5			15	mV (RMS)
Input Rise and Fall time (20% to 80%)	t_{RH}, t_{FH}		24			ps
Differential Input Return Loss	SDD11	0.05-0.1 GHz	20			dB
		0.1-5.5 GHz	8			dB
		5.5-12 GHz	see 1			
Common Mode Return Loss [2]	SCC11	0.1-12 GHz	3			dB
Differential to Common Mode Conversion [2]	SCD11	0.1-12 GHz	10			dB

1. Return Loss given be equation SDD11(dB)= 8 - 20.66 Log10(f/5.5), with f in GHz C.4.
2. Common mode reference impedance is 25 Ω. SCD11 and SCC11 help minimize generated EMI C.4.

Transmitter jitter specifications are listed in Table 15. Figure 12 gives the host compliance eye mask.

Table 15 XFI Host Receiver Input Jitter Specifications at C

Transmitter - C	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Determinstic Jitter	DJ	See E.1			0.18	UI (p-p)
Total Jitter	TJ	See E.1			0.34	UI (p-p)
Sinusoidal Jitter Tolerance	SJ	E.3			see 1	
Eye Mask	X1				0.17	UI
Eye Mask	X2				0.42	UI
Eye Mask	Y1		170			mV
Eye Mask	Y2	see 2			425	mV

1. Sinuosidal jitter tolerance for Telecom and Datacom respectively given by Figure 13 and Figure 14.
2. Out of 425 mV, 25 mV is allocated for multiple reflections.

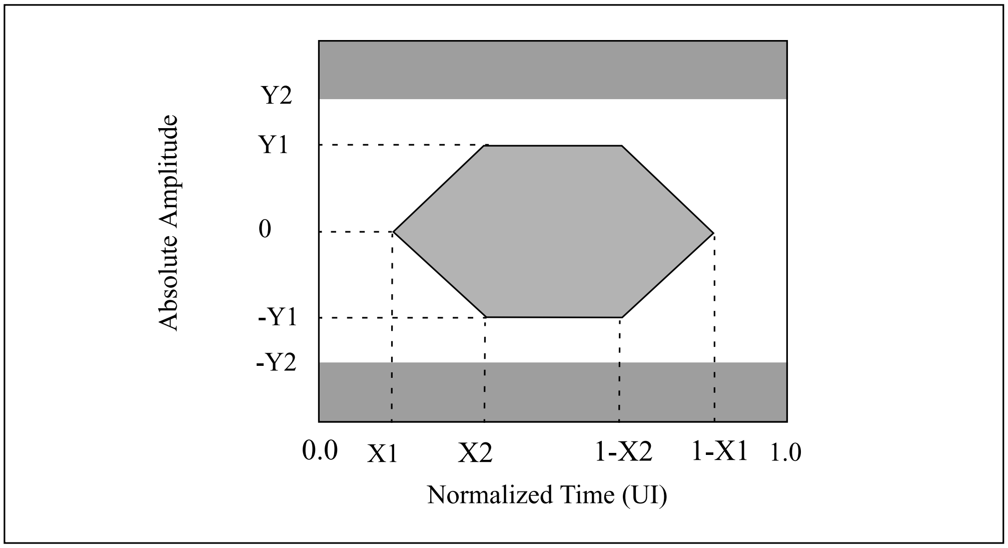

Figure 12 XFI Host Receiver Differential Input Compliance Mask at C

The XFI receiver for Telecom (SONET OC-192 and G. 709 “OTU-2”) applications must meet the jitter tolerance with the addition of deterministic and random jitter given by Table 15. The XFI receiver for Datacom (Ethernet 802.3ae or Fibre Channel 10GFC) Host must meet jitter tolerance given by Figure 14 with the addition of deterministic and random jitter given by Table 15.

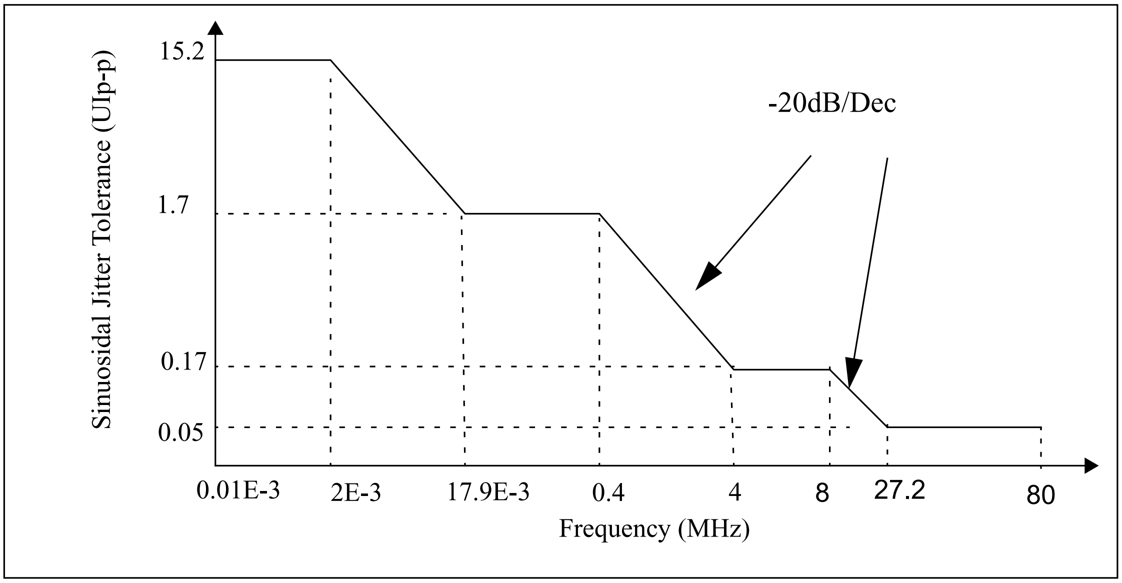

Figure 13 XFI Host Receiver Telecom Input Sinuosidal Jitter Tolerance

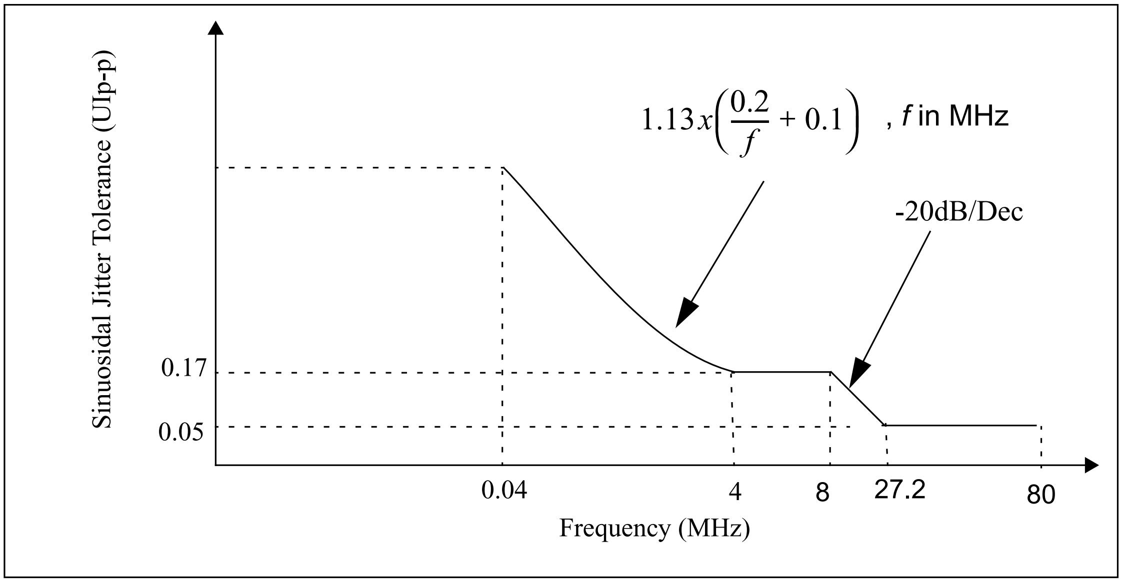

Figure 14 XFI Host Receiver Input Datacom Sinuosidal Jitter Tolerance

3.8 XFI MODULE SPECIFICATIONS

XFI Module Transmitter specifications at compliance point B' are given in 3.8.1. XFI Module Receiver specifications at compliance point C' are given in 3.8.2.

3.8.1 XFI MODULE TRANSMITTER INPUT SPECIFICATIONS AT B'

The XFI module transmitter electrical specifications are given in Table 16, measured at compliance point B' as shown in A.3. The receiver input impedance is 100 Ohms differential. The load must provide differential termination and minimize differential to common mode conversion for quality signal termination and low EMI, as given in Table 16.

The XFI jitter specifications at reference point B' are listed in Table 17 and the compliance mask is shown in Figure 15. Only a compliant transmitter passing through the XFI channel is guaranteed for interoperability.

Return loss at compliance point B' is measured with the Module Test Board plugged into the host as shown in A.3.

Table 16 XFI Module Transmitter Input Electrical Specifications at B’

Parameter - B’	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Reference Differential Input Impedance	Z_d	See Figure 5		100		Ω
Termination Mismatch	ΔZ_M	See E.6, Figure 5			5	%
Source to Sink DC Potential Difference	Vcm		0		3.6	V
Input AC Common Mode Voltage		See E.5			25	mV (RMS)
Differential Input Return Loss	SDD11	0.05-0.1 GHz	20			dB
		0.1-5.5 GHz	8			dB
		5.5-12 GHz	see 1			
Common Mode Input Return Loss[2]	SCC11	0.1-12 GHz	3			dB
Differential to Common Mode Conversion[2]	SCD11	0.1-12 GHz	10			dB

1. Return Loss given be equation SDD11(dB)= 8 - 20.66 Log10(f/5.5), with f in GHz C.4.
2. Common mode reference impedance is 25 Ω. Differential to common mode conversion relates to generation of EMI C.4.

Table 17 XFI Module Transmitter Input Jitter Specifications at B’

Receiver- B’	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Total Non-EQJ Jitter	0.41	See E.1, E.2			0.41	UI (p-p)
Total Jitter	TJ	See E.1, E.2			0.61	UI (p-p)
Sinusoidal Jitter Tolerance	SJ	E.3			see 1	
Eye Mask	X1	see 2			0.305	UI
Eye Mask	Y1		60			mV
Eye Mask	Y2	see 3			410	mV

1. Sinuosidal jitter tolerance for Telecom and Datacom respectively given by Figure 16 and Figure 17.
2. Mask cordinate X1=0.205 if total non-EQJ jitter is measured.
3. Out of 410 mV, 50 mV is allocated for multiple reflection.

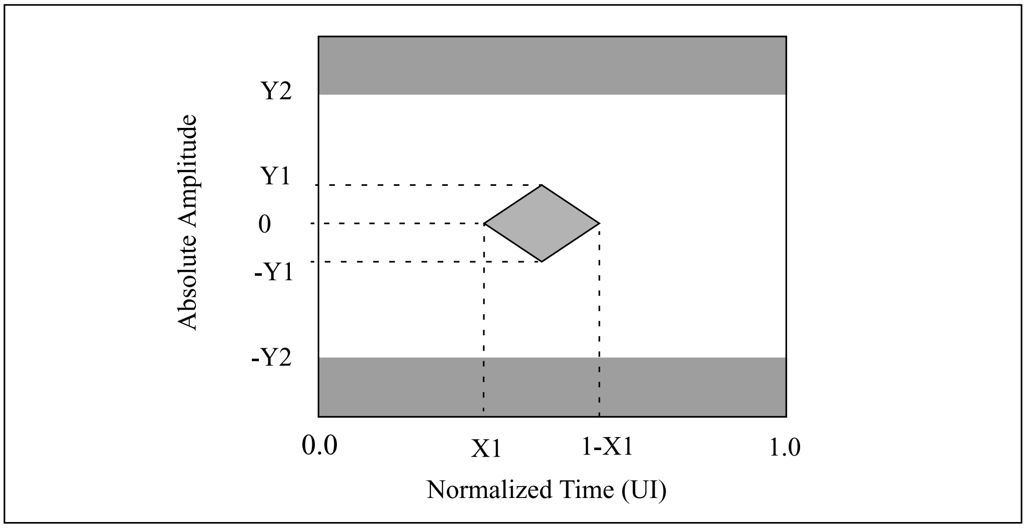

Figure 15 XFI Module Transmitter Differential Input Compliance Mask at B'

XFI Module for Telecom (SONET OC-192 and G. 709 "OTU-2") applications must meet the jitter tolerance given by Figure 16 with addition of input jitter given by Table 17. The XFI Module for Datacom (Ethernet 802.3ae and Fibre Channel 10GFC) must meet the jitter tolerance given by Figure 17 with the addition of random and deterministic jitter given in Table 17.

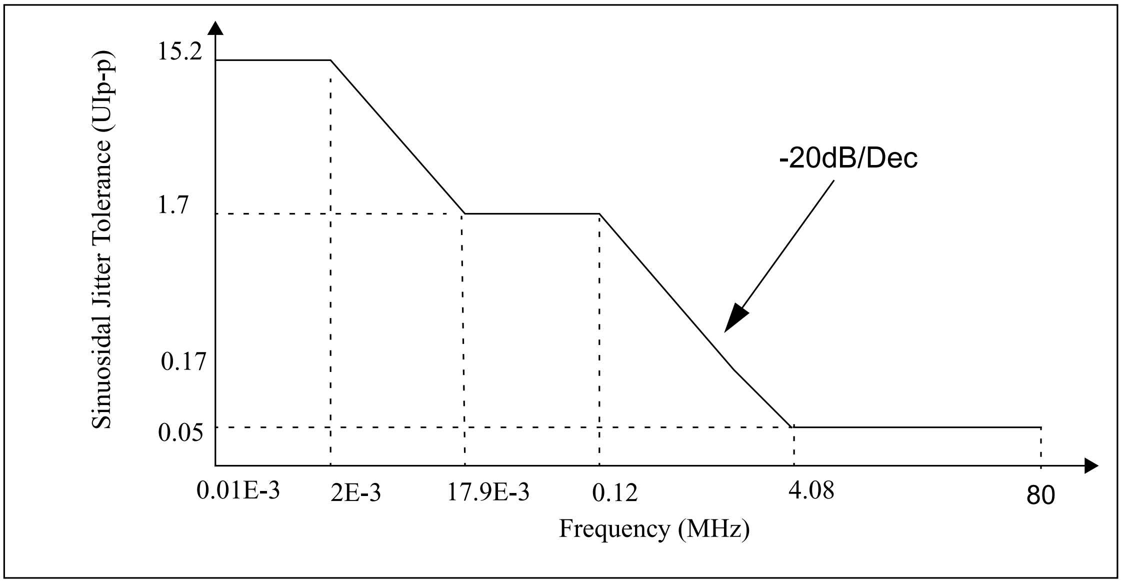

Figure 16 XFI Module Transmitter Input Telecom Sinuosidal Jitter Tolerance

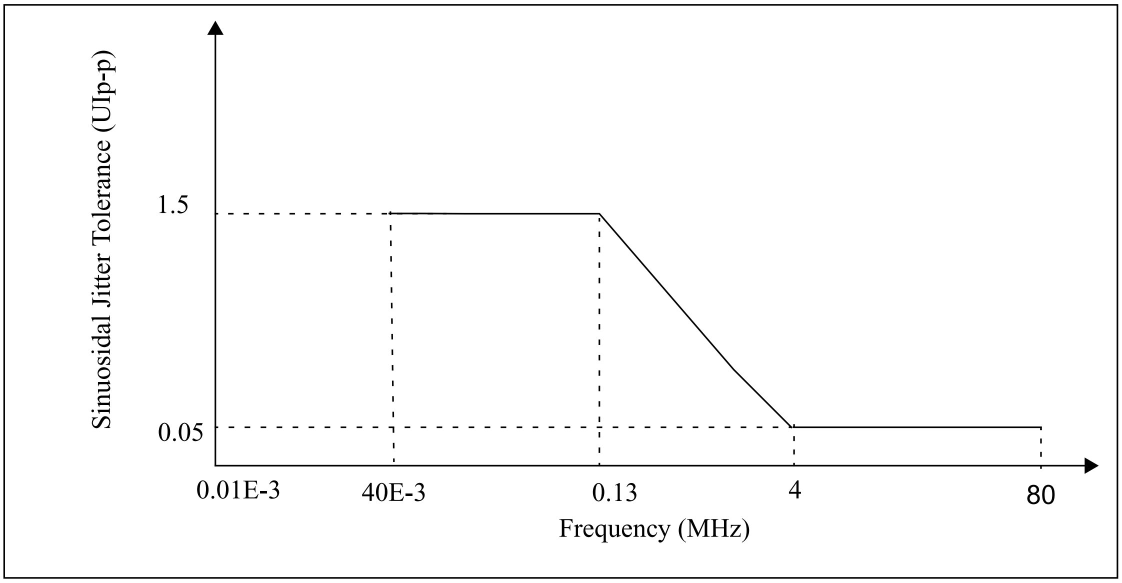

Figure 17 XFI Module Transmitter Input Datacom Margin Mask

3.8.2 XFI MODULE RECEIVER OUTPUT SPECIFICATIONS AT C’

The XFI transmitter electrical specifications at compliance point C’ are given in Table 18. The source must provide differential termination and common mode termination for quality signal termination and low EMI, as given in Table 18.

Return loss at C’ is measured with the module on a Module Compliance Test Board A.3.

Table 18 XFI Module Receiver Output Electrical Specifications at C'

Parameter - C	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Reference Differential Output Impedance	Z_d	See Figure 5		100		Ω
Termination Mismatch	ΔZ_M	See E.6, Figure 5			5	%
DC Common Mode Potential	Vcm		0		3.6	V
Output AC Common Mode Voltage		See E.5			15	mV (RMS)
Output Rise and Fall time (20% to 80%)	t_{RH}, t_{FH}		24			ps
Differential Output Return Loss	SDD22	0.05-0.1 GHz	20			dB
		0.1-5.5 GHz	8			dB
		5.5-12 GHz	see 1			dB
Common Mode Output Return Loss [2]	SCC22	0.1-12 GHz	3			dB

1. Differential Return Loss given be equation SDD22(dB)= 8 - 20.66 Log10(f/5.5), with f in GHz C.4.
2. Common mode reference impedance is 25 Ω. Common Mode Output Return Loss helps absorb reflection and noise improving EMI C.4.

Transmitter jitter specifications are listed in Table 19. Figure 18 gives the compliance eye mask.

Table 19 XFI Module Receiver Output Jitter Specifications at C'

Transmitter - C	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Determinstic Jitter	DJ	See E.1, 1			0.18	UI (p-p)
Total Jitter	TJ	See E.1, 1			0.34	UI (p-p)
Eye Mask	X1				0.17	UI
Eye Mask	X2				0.42	UI
Eye Mask	Y1		170			mV
Eye Mask	Y2				425	mV

1. Includes jitter transfered from the optical receiver during any valid operational input condition.

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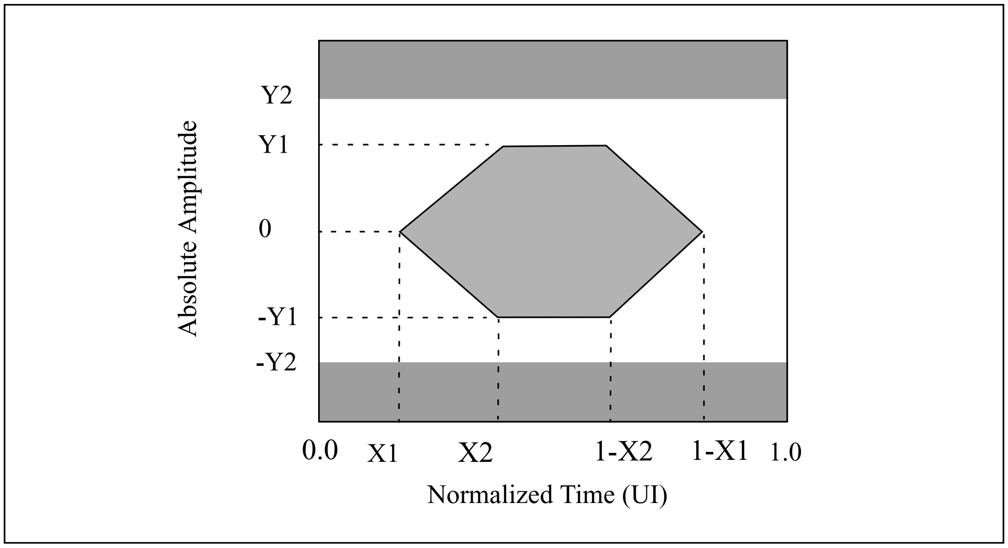

Figure 18 XFI Module Receiver Differential Output Compliance Mask at C'

3.9 SIGNAL CONDITIONER

The XFI Signal Conditioner is an active device that overcomes host board and connector signal degradations by reshaping, regenerating, and attenuating jitter. The XFP module shall include a Signal Conditioner based on CDR (Clock Data Recovery) technology for complete regeneration. An optional CMU (Clock Multiplier Unit) based regenerator, which requires a clean frequency locked clock provided by the host XFI interface, is defined as well.

The telecom XFI signal conditioner must meet SONET OC-192 and G.709 (OTU-2) specifications, while the datacom signal conditioner must meet IEEE 802.3ae and 10 GFC specifications. The following sections define the signal conditioner for each application. A common signal conditioner meeting telecom and datacom specifications is desirable, but not mandatory.

3.9.1 TELECOM MODULE

The XFP Telecom module must meet SONET OC-192 per GR-253 and G.709 (OTU-2) requirements.

The XFP Telecom module transmitter shall meet the requirements of both SONET GR-253 and Table 20.

Table 20 XFP Telecom Module Transmitter Requirement

Module Transmitter B'	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Jitter Transfer Bandwidth	BW	PRBS 2^{31}-1 Data, see 1			8	MHz
Jitter Peaking		Frequency <120 KHz see 2			0.03	dB
		Frequency >120 KHz see 3			1	dB
Module Jitter Generation at Optical Output		Measured 50KHz-80MHz see 4			10 100	mUI (RMS) mUI (p-p)

1. OC-192/SDH-64 Sinusoidal Jitter Tolerance Mask

2. Only required for loop timing, see E.4.
3. Does not apply to the optional CMU mode, see E.4.
4. In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter from 50KHz-8 MHz Table 13. In CMU mode it is assumed that worst case phase noise given by Table 25. Jitter generation of an optical transmitter must include jitter that transfers from the host during any valid operational conditions.

The XFP Telecom modules receiver shall meet the requirements of both SONET GR-253 and Table 21.

Table 21 XFP Telecom Module Receiver Requirement

Module Transmitter C'	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Jitter Transfer Bandwidth	BW	PRBS $2^{\wedge 31}$-1 Data, see 1			8	MHz
Jitter Peaking		Frequency <120 KHz see 2			0.03	dB
		Frequency >120 KHz			1	dB
1. OC-192/SDH-64 Sinusoidal Jitter Tolerance Mask 2. Only required for loop timing, see E.4.						

3.9.2 DATACOM MODULE

XFP Datacom module shall meet IEEE 802.3ae and 10 GFC requirement, in addition to the requirements given in Table 20 and Table 21.

Table 22 XFP Datacom Module Transmitter Requirement

Module Transmitter B'	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Jitter Transfer Bandwidth	BW	PRBS $2^{\wedge 31}$-1 Data or Scrambled 64B/66B, see 1			8	MHz
Jitter Peaking		Frequency >50 KHz			1	dB
1. Based on IEEE 802.3ae Clause 52 Sinuosidal Jitter Tolerance Mask Figure 52-4.						

Table 23 XFP Datacom Module Receiver Requirement

Module Transmitter C'	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Jitter Transfer Bandwidth	BW	PRBS $2^{\wedge 31}$-1 Data or Scrambled 64B/66B, see 1			8	MHz
Jitter Peaking		Frequency >50 KHz			1	dB
1. Based on IEEE 802.3ae Clause 52 Sinuosidal Jitter Tolerance Mask Figure 52-4.						

3.10 REFERENCE CLOCK SPECIFICATIONS

The host system shall supply a reference clock to the XFP module with a frequency of +/-100 PPM of Baudrate/64 with specifications listed in Table 24. The Signal Conditioners in the XFP module may use the reference clock for VCO centering. The reference clock is intended for VCO centering so jitter requirements are intentionally relaxed to allow implementation flexibility on the host board.

Table 24 Reference Clock Specifications

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Clock Differential Input impedance	Z_d		80	100	120	Ω
Differential Input Clock Amplitude (p-p)		AC Coupled PECL	640		1600	mV
Reference Clock Duty Cycle			40		60	%
Reference Clock Rise/Fall Time	Tr/Tf	20%-80%	200		1250	ps
Reference Clock Frequency	f_0			Baud[1]/64		MHz
RMS Jitter Random Jitter	σ	Up to 100 MHz			10	ps
Reference Clock Frequency Tolerance	Δf		-100		100	PPM

[1] Reference clock frequency is not locked to the data frequency and may deviate by Δf.

3.10.1 OPTIONAL SYNCHRONOUS CMU CLOCK

The host system may optionally supply a synchronous reference clock to the XFP module, with frequency exactly equal to the Baudrate/64 according to the specifications listed in Table 25. The transmitter Signal Conditioners in the XFP module may use the synchronous clock to retime the data.

In order to select Optional Synchronous CMU clock, bit 0 of Byte 1, in the two wire interface Table 34 must be set high. A CDR based module may be used in conjunction with a synchronous clock from the host see 5.3.

Architectural Note

In applications where the Host System uses the XFP module in the optional CMU mode, the Host must provide a synchronous low phase noise clock.

Table 25 Optional Reference Clock Specifications

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Clock Differential Input impedance	Z_d		80	100	120	Ω
Differential Input Clock Amplitude (p-p)		AC Coupled PECL	640		1600	mV
Reference Clock Duty Cycle			40		60	%
Reference Clock Rise/Fall Time	Tr/Tf	20%-80%	200		1250	ps
Reference Clock Frequency	f_0	see 1		Baud[1]/64		MHz
CMU Reference Clock Skew	TD	Baud[2]	-10		+10	UI
Single Side Band Phase Noise		@1KHz			-85	dBc/Hz
		@10KHz			-108	
		@100KHz			-128	
		@1MHz			-138	
		@10MHz			-138	

1. Reference clock frequency is exactly 1/64 of the Baudrate.
2. A UI defined by the serial Baudrate.

CHAPTER 4: XFP 2-WIRE INTERFACE PROTOCOL

4.1 INTRODUCTION

Low speed signaling is based on Low Voltage TTL (LVTTL) operating at Vcc3 at a nominal supply of (3.3V ± 5%). Hosts shall use a pull-up resistor connected to a host_Vcc of +3.3 volts (3.15 to 3.45 volts) on the 2-wire interface SCL (clock) and SDA (Data) signals. Detailed electrical specification are given in section 2.5.

Nomenclature for all registers more than 1 bit long are MSB-LSB.

4.2 XFP 2-WIRE TIMING DIAGRAM

XFP is positioned to leverage 2-wire timing (Fast Mode devices) to align the use of related cores on host ASICs. XFP 2-wire bus timing is shown in Figure 19. XFP AC specifications are given in Table 26.

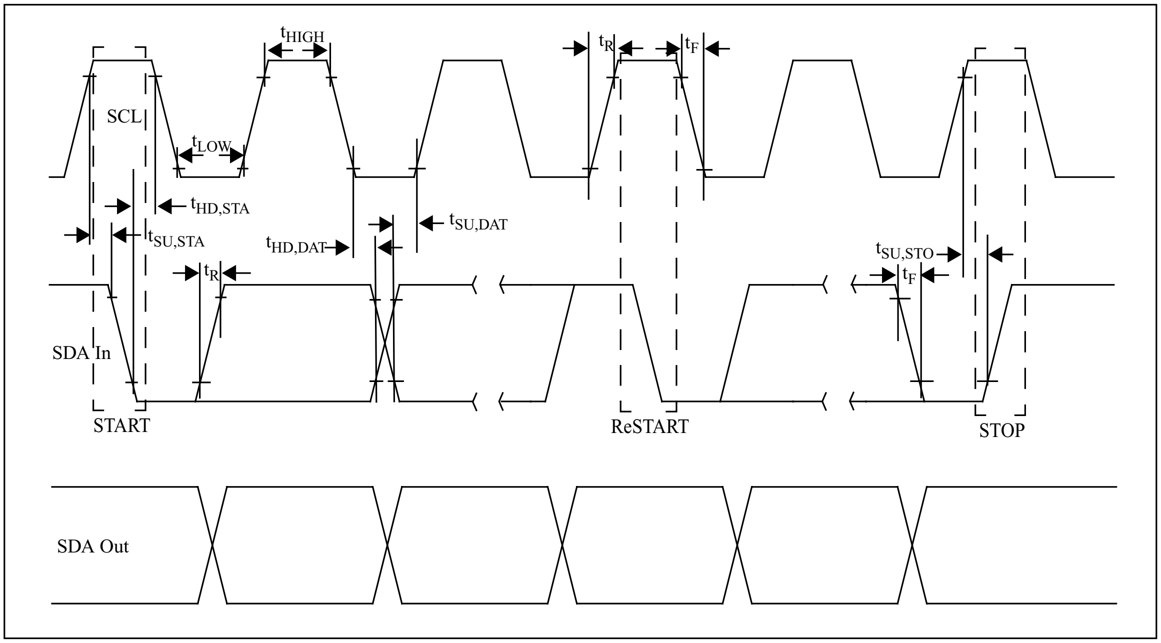

Figure 19 XFP Timing Diagram

Before initiating a 2-wire serial bus communication, the host shall provide setup time (Host select_setup - table 26) on the Mod_DeSel line of all modules on the 2-wire bus. The host shall not change the Mod_DeSel line of any module until the 2-wire serial bus communication is complete and the hold time requirement (Host_select_hold - Table 26) is satisfied.

The 2-wire serial interface address of the XFP module is 1010000X (A0h). In order to allow access to multiple XFP modules on the same 2-wire serial bus, the XFP pinout includes a Mod_DeSel or module deselect pin. This pin (which is pulled high or deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

Table 26 XFP 2-Wire Timing Specifications

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	t_{LOW}	1.3		µs	
Clock Pulse Width High	t_{HIGH}	0.6		µs	
Time bus free before new transmission can start	t_{BUF}	20		µs	Between STOP and START
START Hold Time	$t_{HD,STA}$	0.6		µs	
START Set-up Time	$t_{SU,STA}$	0.6		µs	
Data In Hold Time	$t_{HD,DAT}$	0		µs	
Data In Set-up Time	$t_{SU,DAT}$	0.1		µs	
Input Rise Time (100kHz)	$t_{R,100}$		1000	ns	From ($V_{IL,MAX}$ - 0.15) to ($V_{IH,MIN}$ + 0.15)
Input Rise Time (400kHz)	$t_{R,400}$		300	ns	From ($V_{IL,MAX}$ - 0.15) to ($V_{IH,MIN}$ + 0.15)
Input Fall Time (100kHz)	$t_{F,100}$		300	ns	From ($V_{IH,MIN}$ + 0.15) to ($V_{IL,MAX}$ - 0.15)
Input Fall Time (400kHz)	$t_{F,400}$		300	ns	From ($V_{IH,MIN}$ + 0.15) to ($V_{IL,MAX}$ - 0.15)
STOP Set-up Time	$t_{SU,STO}$	0.6		µs	
Host Supplied Module DeSelect Setup Time	Host_select_setup	2		ms	Setup time on the select lines before start of a host initiated serial bus sequence
Host Supplied Module DeSelect Hold Time	Host_select_hold	10		µs	Delay from completion of a serial bus sequence to changes of transceiver select status
Aborted sequence - bus release	Deselect_Abort		2	ms	Delay from a host asserting Mod_DeSel (at any point in a bus sequence), to the XFP module releasing SCL and SDA

4.3 MEMORY TRANSACTION TIMING

XFP memory transaction timings are given in Table 27. Single Byte writable memory blocks are given in Table 28. Multiple Byte writable memory blocks are given in Table 29.

Table 27 XFP Memory Specifications

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Conditions*
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	µs	Maximum time the XFP module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	t_{WR}		40	ms	Complete (up to) 4 Byte Write
Endurance (Write Cycles)		50 k		cycles	70 °C

Table 28 Single Byte Writable Memory Blocks

Byte Address	*Volatile or NV*	*Description*
1	V	Signal Conditioner Control Register
110	V	General Control Bits
118	V	Packet Error Checking Control
127	V	Table Select Byte

Table 29 Multiple Byte Writable Memory Blocks

Byte Address	*# Bytes*	*Volatile or NV*	*Description*
72-73	2	V	Wavelength Control Registers
76-77	2	V	FEC Control Registers
88-93	6	V	Interrupt Masking Bits
119-122	4	V	Password Change Entry
123-126	4	V	Password Entry
128-255	128	NV	Table 02h – Customer Writable

4.4 DEVICE ADDRESSING AND OPERATION

Serial Clock (SCL): The host supplied SCL input to XFP transceivers is used to positively edge clock data into each XFP device and negative clock data out of each device. The SCL line may be pulled low by an XFP module during clock stretching.

Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven and may be wire-ORed with any number of open-drain or open collector devices.

Master/Slave: XFP transceivers operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Device Address: Each XFP is hard wired at the device address A0h. See XFP MSA Chapter 5: Management interface for memory structure within each transceiver.

Multiple Devices per SCL/SDA: While XFP transceivers are compatible with point-to-point SCL/SDA, they can also be paralleled on a single SCL/SDA bus by using the XFP Mod_DeSel line. See section 2.4.2 and Table 26 for more information.

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the XFP in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host shall be acknowledged by XFP transceivers. Read data bytes transmitted by XFP transceivers shall be acknowledged by the host for all but the final byte read, for which the host shall respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the XFP management interface can be reset. Memory reset is intended only to reset the XFP transceiver management interface (to correct a hung bus). No other transceiver functionality is implied.

1) Clock up to 9 cycles.
2) Look for SDA high in each cycle while SCL is high.
3) Create a START condition as SDA is high

Device Addressing: XFP devices require an 8 bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory one zero sequence for the first seven most significant bits Table 30. This is common to all XFP devices.

Table 30 XFP Device Address

1	0	1	0	0	0	0	R/W
MSB							LSB

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address (with Mod_DeSel in the low state) the XFP transceiver shall output a zero (ACK) on the SDA line to acknowledge the address.

4.5 READ/WRITE FUNCTIONALITY

4.5.1 PACKET ERROR CHECKING

In addition to the basic I2C read/write functionality, all XFP modules shall support packet error checking defined in the sections below. The packet error checking system may be enabled or disabled by the host system, and will default to being disabled on power-up or reset. Packet error checking allows the host system to confirm the validity of any read data including the address from which the read originated. Packet error checking also allows the XFP module to determine the validity of write data and to reject write commands with errors. Finally, the host may use the system to determine if a write communication was successful. All packet error checking operations involve the calculation of a CRC-8 value by the module and host. The CRC-8 value is the cyclical redundancy check as defined in the SMBUS 2.0 standard.

4.5.2 XFP MEMORY ADDRESS COUNTER (READ AND WRITE OPERATIONS)

XFP devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the transceiver. This address stays valid between operations as long as XFP power is maintained. The address “roll over” during read and write operations is from the last byte of the 128 byte memory page to the first byte of the same page.

In order to read both the lower page and currently selected upper page, at least two read operations must be performed, one with start address of ZERO and another with start address of 128. A single 256-byte read operation with start address of ZERO would contain the 128 bytes of the lower page twice, instead of the lower page followed by the currently selected upper page.

4.5.3 READ OPERATIONS (CURRENT ADDRESS READ)

A current address read operation requires only the device address read word (10100001) be sent, Figure 20. Once acknowledged by the XFP, the current address data word is serially clocked out. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

		< ---- XFP ADDRESS --->																	
HOST	START	MSB						LSB	READ									NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
XFP										ACK	MSB							LSB		
											<------ DATA WORD ------>									

Figure 20 XFP Current Address Read Operation

4.5.4 READ OPERATIONS (RANDOM READ)

A random read operation requires a “dummy” write operation to load in the target byte address Figure 21. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the XFP. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The XFP acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

		< ---- XFP ADDRESS --->									<--- MEMORY ADDRESS -->										< ---- XFP ADDRESS --->																		
HOST	START	MSB						LSB	WRITE		MSB							LSB		START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
XFP										ACK									ACK										ACK	MSB							LSB		
																														<------ DATA WORD ------>									

Figure 21 XFP Random Read

4.5.5 READ OPERATIONS (SEQUENTIAL READ)

Sequential reads are initiated by either a current address read Figure 22 or a random address read Figure 23. To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the XFP receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

		< ---- XFP ADDRESS --->																																			
HOST	START	MSB						LSB	READ										ACK									ACK									NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
XFP										ACK	MSB							LSB		MSB							LSB		MSB							LSB		
											<---- DATA WORD n ---->									<---- DATA WORD n+1 ---->									<---- DATA WORD n+x ---->									

Figure 22 Sequential Address Read Starting at XFP Current Address

		< ---- XFP ADDRESS --->									<--- MEMORY ADDRESS -->										< ---- XFP ADDRESS --->																																				
HOST	START	MSB						LSB	WRITE		MSB							LSB		START	MSB						LSB	READ										ACK									ACK									NACK	STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
XFP										ACK									ACK										ACK	MSB							LSB		MSB							LSB		MSB							LSB		
																														<---- DATA WORD n ---->									<---- DATA WORD n+1 ---->									<---- DATA WORD n+x ---->									

Figure 23 Sequential Address Read Starting with Random XFP Read

4.5.6 READ OPERATION PACKET ERROR CHECKING

For packet error checking, the host shall begin with the XFP device Address and Starting Memory Address, followed by the number of bytes to be read. The XFP CRC-8 calculation requires an explicit starting memory address be incorporated as the first byte processed by the algorithm, followed by the number of bytes to be read, and finally all data bytes. After the host reads the required number of bytes, the CRC-8 value will be sent by the XFP module. The host will follow with NACK and STOP to complete the READ operation. XFP read operation with packet error checking is illustrated in Figure 24. The CRC-8 value is calculated on the starting memory address (MSB first) followed by the number of bytes and the Read Bytes in the order they are sent. The host may then verify the CRC-8 value and reject the read if the CRC-8 value does not correspond to the received data and desired Read address. Note the XFP address itself is not included in the CRC-8 calculation.

Only reads of 1-128 bytes are supported. Any transaction that does not follow the protocol described in this section will result in an unpredictable response from the module when PEC is enabled.

		< ---- XFP ADDRESS --->									<----- MEMORY ADDRESS ---->									< ---- Number of BYTES ---->										< ---- XFP ADDRESS --->																
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		START	MSB						LSB	READ									
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x
XFP										ACK									ACK									ACK										ACK	MSB							LSB
																																							<---- DATA WORD 1 --->							

HOST									ACK									ACK									NACK	STOP
	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
XFP	MSB							LSB		MSB							LSB		MSB							LSB		
	<---- DATA WORD n-1 ---->									<----- DATA WORD n --->									<----- CRC-8 ---->									

Figure 24 XFP READ OPERATION PACKET ERROR CHECKING

4.5.7 WRITE OPERATIONS (BYTE WRITE)

A write operation requires an 8-bit data word address following the device address write word (10100000) and acknowledgement Figure 25. Upon receipt of this address, the XFP shall again respond with a zero (ACK) to acknowledge and then clock in the first 8 bit data word. Following the receipt of the 8 bit data word, the XFP shall output a zero (ACK) and the host master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the I^{2}C specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the XFP enters an internally timed write cycle, t_{WR}, to internal memory. The XFP disables it's management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the write is complete. Note that I^{2}C "Combined Format" using repeated START conditions is not supported on XFP write commands.

		< ---- XFP ADDRESS -->									<--- MEMORY ADDRESS -->									<-------- DATA WORD ------>									
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
XFP										ACK									ACK									ACK	

Figure 25 XFP Write Byte Operation

4.5.8 WRITE OPERATIONS (SEQUENTIAL WRITE)

XFP's shall support up to a 4 sequential byte write without repeatedly sending XFP address and memory address information. A "sequential" write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the XFP acknowledges receipt of the first data word, the host can transmit up to three more data words. The XFP shall send an acknowledge after each data word received. The host must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that I2C "combined format" using repeated START conditions is not supported on XFP write commands."

.

		< ---- XFP ADDRESS --->									<--- MEMORY ADDRESS -->									<------ DATA WORD 1 ------>									<------ DATA WORD 2 ------>									<------ DATA WORD 3 ------>									<------ DATA WORD 4 ------>									
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		MSB							LSB		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
XFP										ACK									ACK									ACK									ACK									ACK									ACK	

Figure 26 XFP Sequential Write Operation

4.5.9 WRITE OPERATION PACKET ERROR CHECKING

All types of Write operations will use the same packet error checking technique (when enabled) as follows.

The form of the write transfer for packet error checking will include the number of bytes to be transferred as shown in Figure 27. After the host transmits the 1 to 4 Bytes of data Write operation and receives an ACK from the module, as in normal Write operation the host will further transmitted a CRC-8 value. The CRC-8 value is calculated based on the starting memory address followed by the number of bytes and then the 1 to 4 Bytes in the order they are transmitted. Following the CRC-8 value, the host will transmit a dummy byte: CAB (CRC Add-on Byte).

		< ---- XFP ADDRESS --->									<--- MEMORY ADDRESS -->									<--- NUMBER OF BYTES--->									<------ DATA WORD 1 ------>									<------ DATA WORD 2 ------>								
HOST	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		MSB							LSB		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	Cont.
XFP										ACK									ACK									ACK									ACK									

		<------ DATA WORD 3 ------>									<------ DATA WORD 4 ------>									<------ CRC-8 VALUE ------>									<------ CAB ------>										
HOST		MSB							LSB		MSB							LSB		MSB							LSB		MSB							LSB		STOP	
	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	*		* XFP Responds with an ACK (0) if CRC-8 is CORRECT and a NACK (1) if the CRC-8 is INCORRECT.
XFP	ACK									ACK									ACK									ACK											

Figure 27 XFP Write Operation Packet Error Checking

The XFP module will calculate the validity of the received Write data and Address based on the CRC-8. If the CRC-8 data is correct, the write will be accepted and the module will respond to the CAB with an ACK after which the host will issue a STOP. If the CRC-8 data is incorrect, the module shall reject the write and respond with a NACK after which the host will issue a STOP.

A CRC-8 should not be appended to a Dummy Write used in a Random Read since the subsequent Read will confirm the address in its CRC-8.Only writes of 1-4 bytes are supported. Any transaction that does not follow the protocol described in this section will result in an unpredictable response from the module when PEC is enabled

4.5.10 WRITE OPERATIONS (ACKNOWLEDGE POLLING)

Once the XFP internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the XFP respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

CHAPTER 5: MANAGEMENT INTERFACE

This chapter defines the operation of the XFP 2-wire serial interface which is used for serial ID, digital diagnostics, and certain control functions. The 2-wire serial interface is mandatory for all XFP modules. It is modeled largely after the digital diagnostics monitoring interface proposed for the SFP and GBIC optical transceivers and defined in SFF draft document SFF-8472 Rev 9.3, which in turn is an extension of the original serial ID systems defined for the GBIC and SFP transceivers. One major difference, however, is that the memory structure is changed to use a single 2-wire interface address.

The structure of the memory map is shown in Figure 28. The normal 256 Byte I2C address space is divided into lower and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control functions described in this document that must be accessed repeatedly. One exception to this is that the standard module identifier Byte defined in the GBIC and SFP is located in Byte 0 of the memory map (in the diagnostics space) to allow software developed for multiple module types to have a common branching decision point. This Byte is repeated in the Serial ID section so that it also appears in the expected relationship to other serial ID bits.

Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of 128 * 256 = 32Kbytes in this upper memory space.

The upper address space tables are used for less frequently accessed functions such as serial ID, user writable EEPROM, reserved EEPROM and diagnostics and control spaces for future standards definition, as well as ample space for vendor specific functions. These are allocated as follows:

- Table 00h: Reserved for future diagnostic and control functions
- Table 01h: Serial ID EEPROM
- Table 02h: User writable EEPROM
- Table 03h – 7Fh:Vendor specific functions
- Table 80h – FFh:Reserved

The details of each memory space are described in the sections that follow. All 2-Wire registers are read with bit 7 the MSB first. Nomenclature for all registers more than 1 bit long are MSB-LSB.

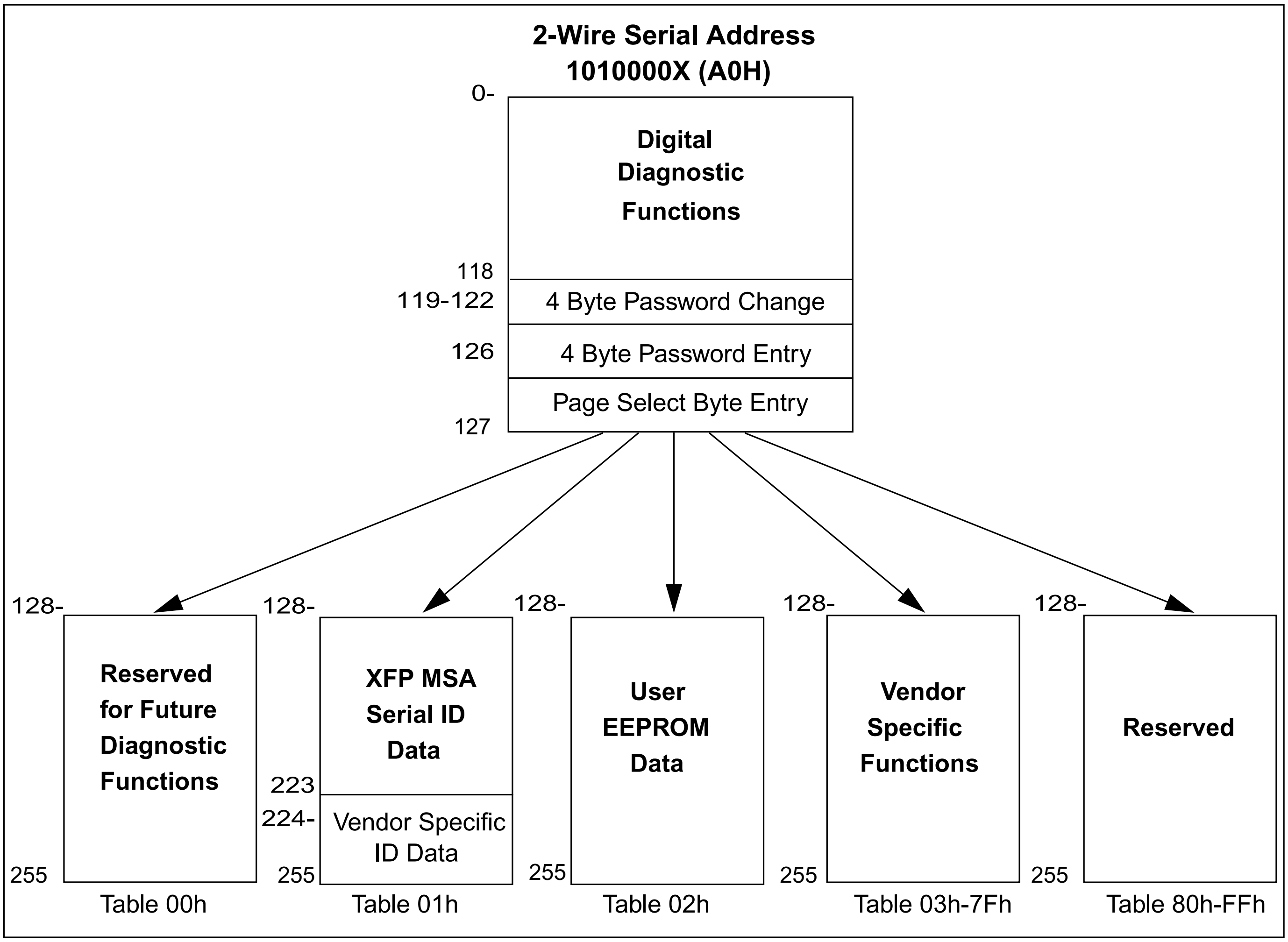

Figure 28 2-wire Serial Digital Diagnostic Memory Map

The memory structure also provides for an optional password entry location in the lower memory space that may be used to protect vendor internal functions or user writable memory. Passwords shall not be required to read any serial ID or diagnostics information in the lower memory address space or in Tables 00h – 02h. Nor shall passwords be required to write any controls defined in the digital diagnostic functions described in this document. Passwords may be used by vendors to control write access to MSA defined read only data for factory setup, or to OEMs to limit write access in the User EEPROM Table (02h). Finally, passwords may be used to control read or write access to the vendor specific tables 03h – 7Fh.

Separate Passwords value ranges will be defined for host vendor passwords and module vendor passwords to prevent accidental writing into critical module control areas by the host vendor. Details are defined in 5.5.

Note: Unless specifically noted, all informative ID fields must be filled out. Using a value of 0 to indicate a field is unspecified (as is common in the SFP definition) is not permitted.

5.0.1 APPLICABLE DOCUMENTS

Digital Diagnostic Monitoring Interface for Optical Transceivers SFF document number: SFF-8472, rev. 9.3 August 4, 2002.

5.1 DESCRIPTION OF LOWER MEMORY MAP: CONTROL FUNCTIONS, DIAGNOSTICS, TABLE ACCESS

The lower 128 Bytes of the 2-wire serial bus address space is used to access a variety of measurements and diagnostic functions, to implement a set of control functions, and finally to select which of the various upper memory map tables are accessed on subsequent reads. This portion of the address space is always directly addressable and thus is chosen for diagnostics and control functions that may need to be repeatedly accessed.

Table 31 shows the general memory map of the lower 128 Byte address space.

Table 31 Lower Memory Map

Byte Address	*Description*
0	Identifier (1 Byte)
1	Signal Conditioner Control
2-57	Threshold Values used for Alarm and Warning Flags (56 Bytes)
58-59	Optional VPS Control Registers(2 Byte)
60-69	Reserved (10 Bytes)
70-71	BER Reporting
72-75	Wavelength Control Registers (4 Bytes)
76-79	FEC control Registers (4 Bytes)
80-95	Flags and $\overline{\text{Interrupt}}$ Control (16 Bytes)
96-109	A/D readout (14 Bytes)
110-111	General Control/Status bits (2 Bytes)
112-117	Reserved (6 Bytes)
118	Serial Interface Read/Write Error Checking (1 Bytes)
119-122	Password Change Entry Area (Optional) (4 Bytes)
123-126	Password Entry Area (optional) (4 Bytes)
127	Page Select Byte

5.2 IDENTIFIER

Byte 0 of the lower memory map contains the module identifier value. The identifier value specifies the physical device described by the serial ID information. This value is also included in the serial ID data table (01h). The defined identifier values are shown in Table 32. The XFP transceiver should use identifier 06h.

Table 32 Identifier values Byte 128

Value	*Description of Physical Device*
00h	Unknown or unspecified
01h	GBIC
02h	Module/connector soldered to motherboard
03h	SFP
04h	300 pin XBI
05h	XENPAK
06h	**XFP**
07h	**XFF**
08h	**XFP-E**
09h	XPAK
0Ah	X2
0Ah-7Fh	Reserved
80h-FFh	Vendor specific

5.3 SIGNAL CONDITIONER CONTROL

The XFP MSA defines two modes of transmitter signal conditioner operation. The default mode, which must be included in all XFP implementations, uses a REFCLK which need not be synchronous with the data and with relatively loose jitter requirements. This mode is generally intended for Clock and Data Recovery techniques for retiming the transmitter data. An optional mode is defined whereby the host system provides a synchronous REFCLK with relatively tight frequency and jitter requirements. This mode is intended to allow the use of a Clock Multiplication (CMU) based retiming scheme. The electrical requirements for these modes are defined in Section 3.10.

In order to select between these modes in modules which implement both, a control bit is defined in Byte 1, bit 0, as shown in Table 34. This bit shall power up with a value of 0 corresponding to the default asynchronous clock mode. The host system may switch the XFP module to the synchronous clock mode by writing a value of 1 into this bit.

An identifier bit indicating the availability of this capability is defined in the Serial ID Page in Byte 221, Bit 0 Page 01h. XFP modules not implementing the optional REFCLK mode shall not have a writable bit in this location and should report a value of 0 when read.

In order to accommodate signal conditioner devices with limited tuning range, host system shall inform the XFP module of the data rate. The data rate is written into the upper 4 bits of Byte 01h. The value to be entered are given by:

$$\text{Byte 01h[bits 7-4]} = \text{INT}((\text{Data Rate(Gb/s)} - 9.5)/0.2))$$

This covers a range of 9.5-12.5 Gb/s. Thus for example, for 10.3 Gb/s, Bits 7-4 are 0100b.

The signal conditioner may optionally support two different loopback modes which may be useful for various diagnostics needs.

The first of these modes is known as XFI Loopback. In this mode, which is set by writing a 1 into Bit 1 of Byte 1 of the lower memory map, data input on the TX pins of the XFP module are retimed and output on the RX pins of the module. Optical data is not transmitted or received when in the XFI Loopback mode. This control bit will power up and reset to 0 resulting in normal operation.

The second loopback mode is known as Lineside Loopback. In this mode, which is set by writing a 1 into Bit 2 of Byte 1 of the lower memory map, data received on the XFP module receiver is retimed and output on optical transmitter. This optical data is not present on the electrical interface in this mode. This control bit will power up and reset to 0 resulting in normal operation.

Support for these loopback modes is indicated in the serial ID memory map in Byte 164 (CDR Support). Simultaneous operation of both loopback modes are not supported.

5.4 2-WIRE SERIAL INTERFACE CHECKSUM

XFP modules shall support selectable packet error checking. Packet error checking is defined in Section 4.5.6 and 4.5.9. Packet error checking is enabled by setting Bit 0 of Byte 118 to 1 (see Table 43), and disabled by setting it to 0. Bit 0 will default to 0 on power-up or reset.

5.5 TABLE SELECTION AND PASSWORD ENTRY (TABLE 44)

Access to information in the various upper memory address tables is provided by the use of a Table Select Byte in Byte 127 of the lower memory map. The Table Select Byte is both readable and writable and shall default on power-up or reset to 01h [Serial ID memory space]. The user may write other table numbers into Byte 127 before subsequent read/writes into those spaces. The current Table Select Byte value will be retained until power down, reset, or rewritten by host.

If the host attempts to write a table select value which is not supported in a particular module, the table select byte will revert to 01h.

Bytes 123-126 are reserved for an optional password entry function. The Password entry bytes are write only and will be retained until power down, reset, or rewritten by host.

This function may be used to control read/write access to vendor specific tables 03h – 7Fh. Additionally, module vendors may use this function to implement write protection of Serial ID and other MSA read only information. Passwords may be supplied to and used by Host manufacturers to limit write access in the User EEPROM Table (02h).

Password access shall not be required to access MSA defined data in the lower memory space or in Tables 00h – 02h. Note that multiple module manufacturer passwords may be defined to allow selective access to read or write to various sections of memory as allowed above.

Host manufacturer and module manufacturer passwords shall be distinguished by the high order bit (bit 7, Byte 123). All host manufacturer passwords shall fall in the range of 00000000h to 7FFFFFFFh, and all module manufacturer passwords in the range of 80000000h to FFFFFFFFh. Host manufacturer passwords shall be initially set to 00001011h in new modules. Host manufacturer passwords may be changed by writing a new password in Bytes 119-122 when the correct current Host manufacture password has been entered in 123-126, with the high order bit being ignored and forced to a value of 0 in the new password.

The password entry field shall be set to 00000000h on power up and reset.

5.6 BASIC MONITORING FUNCTIONS

The basic measured quantities are transceiver temperature, TX bias current, TX output power, received optical power, and two additional quantities which are defined in Byte 222 of the Serial ID table (Table 01h).

Measured parameters are reported in 16 bit data fields, i.e., two concatenated bytes. These are shown in Table 41. The 16 bit data fields allow for wide dynamic range. This is not intended to imply that a 16 bit A/D system is recommended or required in order to achieve the accuracy goals stated below. The width of the data field should not be taken to imply a given level of precision. It is conceivable that the accuracy goals herein can be achieved by a system having less than 16 bits of resolution. It is recommended that any low-order data bits beyond the system's specified accuracy be fixed at zero. Overall system accuracy and precision will be vendor dependent.

To guarantee coherency of the diagnostic monitoring data, the host is required to retrieve any multi-byte fields from the diagnostic monitoring data structure (IE: Rx Power MSB – byte 104, Rx Power LSB – byte 105) by the use of a single two-byte read sequence across the 2-wire serial interface.

The transceiver is required to insure that any multi-byte fields that are updated with diagnostic monitoring data (IE: Rx Power MSB – byte 104, Rx Power LSB – byte 105) must have this update done in a fashion that guarantees coherency and consistency of the data. In other words, the update of a multi-byte field by the transceiver must not occur such that a partially updated multi-byte field can be transferred to the host. Also, the transceiver shall not update a multi-byte field within the structure during the transfer of that multi-byte field to the host, such that partially updated data would be transferred to the host.

Accuracy requirements specified below shall apply to the operating signal range specified in the relevant standard. The manufacturer's specification should be consulted for more detail on the conditions under which the accuracy requirements are met.

Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real time 16 bit data.

- Internally measured transceiver temperature. Represented as a 16 bit signed twos complement value in increments of 1/256 degrees Celsius valid between –40 and +125C. Temperature accuracy is vendor specific but must be better than +/-3 degees Celsius over specified operating temperature and voltage. Please see vendor specification for details on location of temperature sensor. Temperature in degrees Celsius is given by the signed two's complement value with LSB equal to 1/256 C.

- Measured TX bias current in µA. Represented as a 16 bit unsigned integer with the current defined as the full 16 bit value (0 – 65535) with LSB equal to 2 µA, yielding a total measurement range of 0 to 131 mA. Accuracy is vendor specific but must be better than +/-10% of the manufacturer's nominal value over specified operating temperature and voltage.
- Measured TX output power in mW. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 – 65535) with LSB equal to 0.1 µW, yielding a total measurement range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Data is assumed to be based on measurement of laser monitor photodiode current. It is factory calibrated to absolute units using the most representative fiber output type. Accuracy is vendor specific but must be better than +/- 2dBover specified temperature and voltage. Reported measurement values must maintain +/-1dB relative accuracy over the specified temperature and voltage range over the life of the product into a fixed measurement system.Data is not valid when the transmitter is disabled.
- Measured RX received optical power in mW. Value can represent either average received power or OMA depending upon how bit 3 of byte 220 (Table 01h) is set. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 – 65535) with LSB equal to 0.1 µW, yielding a total measurement range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than +/-2 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific. Reported measurement values must maintain +/-1dB relative accuracy over the above received power range and specified temperature and voltage ranges over the life of the product using a fixed test source fiber.
- Up to two Auxiliary Measurements may be implemented by the vendor. The auxiliary monitoring channels, if any, are defined in Byte 222 of Table 01h. That table also details the units which should be used in reporting the corresponding values.
- Internally measured transceiver supply voltage. Represented as a 16 bit unsigned integer with the voltage defined as the full 16 bit value (0 – 65535) with LSB equal to 100 µVolt, yielding a total measurement range of 0 to +6.55 Volts. Practical considerations to be defined by

transceiver manufacturer will tend to limit the actual bounds of the supply voltage measurement. Accuracy is vendor specific but must be better than ±3% of the manufacturer's nominal value over specified operating temperature and voltage.

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory-preset values allow the user to determine when a particular value is outside of "normal" limits as determined by the transceiver manufacturer. It is assumed that these values will vary with different technologies and different implementations. These values are stored in read-only memory in Bytes 2 – 57 as shown in Table 35.

The values reported in the Alarm and Warning Thresholds area may be typical values at some chosen nominal operating conditions and may be temperature compensated or otherwise adjusted when setting warning and/or alarm flags. Any compensation or adjustment is vendor specific and completely optional. If temperature compensation or other adjustment takes place, the corresponding alarm and warning flags may not match the result of a comparison performed by the host using the reported Auxiliary Measurement diagnostic data and thresholds.

A set of alarm and warning flags are implemented. The flags are latched and detailed in the Interrupt Control Descriptions. These flags indicate when the various monitored quantities are above or below the thresholds. For users who do not wish to set their own threshold values or read the values in locations 2 - 57, the flags alone can be monitored. Two flag types are defined:

1) Alarm flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power as well as reserved locations for future flags. Alarm flags indicate conditions likely to be associated with a faulty link and cause for immediate action.

2) Warning flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power as well as reserved locations for future flags. Warning flags indicate conditions outside the normally guaranteed bounds but not necessarily causes of immediate link failures. Certain warning flags may also be defined by the manufacturer as end-of-life indicators (such as for higher than expected bias currents in a constant power control loop).

5.7 OPTIONAL VARIABLE POWER SUPPLY (VPS) CONTROL

To facilitate the power/current savings of deep-submicron CMOS processes, the XFP specification defines modules that optionally support a VCC2 supply lower than 1.8-V. These modules are intended for use in systems employing a variable power supply (VPS). In the default mode, which must be included in every XFP compliant implementation, the module is supplied and can operate normally with a 1.8-V voltage on its VCC2 pins.

An XFP module might include a discrete or integrated regulator, which supplies the CMOS ICs with a voltage lower than 1.8-V by stepping down the VCC2 supply. The module powers up in the default mode of operation capable of operating normally with 1.8-V on the VCC2 pins.

In the first optional mode (“operational LV regulator mode”) the regulator is still operational but the host system supplies the module with a VCC2 voltage lower than +1.8-V. In the second optional mode (“bypassed regulator mode”) the regulator is bypassed and the CMOS ICs are connected directly to the VCC2 pins of the module. Serial ID Byte 221 (Table 01h), bit 7 indicates if optional VPS is implemented. VPS control registers are located in Bytes 58-59 as defined in the *Table 33*.

Table 33 VPS Fields

Byte	*Bit*	*Name*	*Description*
58	7-4	Lowest Voltage Supported with an Operational LV Regulator	Read Only See Note 1, 2
58	3-0	Voltage Supplied on the VCC2 Pins.	Read Write. Powers up to 0000b. See Note 1.
59	7-4	Voltage Supported with a Bypassed Regulator.	Read Only. See Note 1.
59	3-1	Reserved	
59	0	Regulator bypass mode	0b = Mode disabled. Powers up to 0b. 1b = Mode enabled

1. The values in these fields are unsigned 4-bit binary integers (INT[3:0]. To translate to absolute voltage use: V[absolute] = (1.8 V)-(INT[3:0])*(0.1-V).

2. Any XFP compliant module supporting the optional LV regulator mode should be operational with any power supply voltage between 1.8 V and the value signified on Byte58, Bits 7-4.

Modules which implement an optional voltage mode must monitor the VCC2 rail as part of the Auxiliary Monitoring described in sections 5.42.

When a host selects one of the optional voltage modes, the module will automatically adjust the appropriate threshold and alarm register values described in Table 35. The module will issue an Interrupt if the Vcc2 voltage is ever outside the acceptable range.

When a host selects one of the optional voltage modes, power and current requirements of the module should scale *at least linearly* with voltage *(this assumption is made to simplify the specification - in most cases power savings will be larger than linear).* Implementing these optional modes enables a module to fall into two classes of power dissipation according to the mode of operation. However, when a module is switched to one of the optional modes it will not change the values in Table 54. The host can use the default values in Table 54 to calculate the minimum power savings of the optional modes.

All voltage setting changes should take place when the module is in the low power, stand-by mode (i.e. P_Down pin is held high). The 2-wire serial bus and XFP interface signals must remain fully functional during voltage setting changes, and the falling edge of P_Down should not reset these changes. To achieve the lowest power operation under any condition a host supporting an optional voltage mode should hold the P_Down pin high on empty module sockets.

To enable the “operational LV regulator mode” the following sequence must occur:

1. Host sets the module into the stand-by mode by holding the P_Down/RST pin asserted. During stand-by mode the module transmitter should be disabled.
2. Host reads the content of Byte 58 and 59 to determine the most desirable setting for VPS and changes the voltage on VCC2 pins of the XFP connector.
3. Host then writes Bits 3-0 of Byte58 to indicate the new voltage and module updates settings in Table 35.
4. When P_Down is de-asserted module verifies the voltage on VCC2 is within range. If voltage is within range, module enables all circuitry within the module and resumes with normal operation. If voltage is not within range, module sets the appropriate voltage monitoring Interrupt bit to inform the host and asserts Mod_NR.

To enable the “bypassed regulator mode” the host should follow the sequence described above, with the only difference that bit 0 of Byte 59 is written to 1b in step 3.

To return the module to the default mode (VCC2=1.8-V) the host must assert P_Down and return the R/W fields of Bytes 58 and 59 to their default values.

In modules that implement both optional modes the value written in Byte 58 takes precedence over the value written in Byte 59, i.e. if both of Byte 58, bits 3-0 and Byte 59, bit 0 are non-zero the module will be in “operational LV regulator mode”.

Two identifier bits indicating the availability of these optional modes are defined in the Serial ID Page in Byte 221, Bits 3-4 Page 01h. Bit 4 corresponds to the availability of the “operational LV regulator mode”. Bit 3 corresponds to the availability of the “bypassed regulator mode”. XFP modules not implementing these optional modes will return 0 from these locations as well as from all fields of bytes 58-59.

5.8 SYSTEM BER REPORTING

A host system implementing a forward error correction device can report receive BER. The 2-Wire host management interface can transfer FEC reported BER data to the XFP module. The module may use this information to improve system BER. Implementation of BER Reporting functions is indicated in Serial ID Byte 220 (Table 01h), bit 4. Control registers are located in Bytes 70 and 71 (see Table 36).

Byte 70 requests the desired level of BER from the XFP module. Byte 71 reports the FEC actual BER to the XFP module. The data format for Byte 70 it is given by:

$$BER = \left[\frac{Byte(70(MSB-4bits))}{16}\right]\times 10^{-[Byte(70(LSB-4bits))]}$$

Similarly for byte 71 is given by:

$$BER = \left[\frac{Byte(71(MSB-4bits))}{16}\right]\times 10^{-[Byte(71(LSB-4bits))]}$$

MSB-Octet is the decimal value of the 4 MSB bits. LSB-Octet is the decimal value of the 4 LSB bits. If byte 71 reports Hexadecimal value of 4C then the BER would be 0.25x10E-12.

5.9 WAVELENGTH CONTROL

This section of memory includes registers (Table 37) that allow the implementation of a wavelength tunable XFP module.   Implementation of wavelength tunability is indicated in Serial ID Byte 221 (Table 01h), bit 1. Bytes 72-73 are used to input the desired wavelength setpoint in the same format described for XFP center wavelength in the Serial ID Byte 186-187 (units of 0.05 nm). For a wavelength tunable module, the serial ID Bytes for wavelength and tolerance will define the allowed tuning range. Inputs to tuning control bytes 72-73 which are outside this range will be clipped to the allowed tuning range as defined in the serial ID tuning range.

Bytes 74 and 75 are optional monitor values that can be used to report the measured error between the actual wavelength and the entered setpoint. It is a 16 bit signed 2’s complement value in units of 0.005. Thus:

Reported Error [Bytes 74,75] =(Meas. Wavelength – Setpoint [Bytes 72,73])*(0.005nm)

Finally, the latched flag in Byte 85 bit 5 may be used to report a wavelength error exceeding the manufacturer’s tolerance, and this condition may be configured by the user as an interrupt trigger as described in the Interrupt control section below.

5.10 FEC CONTROL

In some forward error correction schemes, the host system may optimize the sensitivity of an optical link or minimize the error rate by adjusting the phase and amplitude threshold for data quantization in the limiting amplifier section of the module receive path. Implementation of FEC control functions is indicated in Serial ID Byte 221 (Table 01h), bit 2. Control registers are located in Bytes 76 and 77 (see Table 38).

Byte 76 is used to set the amplitude threshold of receive path quantization. It is a 2's complement 7 bit value (-128 - +127), where the threshold is given by:

Amplitude Threshold = 50% + [Byte(76)/256] *100%

Similarly, Byte 77 is used to set the phase point in the eye diagram for quantization, and is set in terms of unit interval relative to the eye center:

Phase setpoint = 0.5 UI + [Byte(77)/256] UI

5.11 INTERRUPT SYSTEM LOGIC

The XFP implements a real time hardware Interrupt pin (see 2.4) to alert the host system to any condition outside normal operating conditions. Interrupt system logic may be triggered and latched by a set of flags. These include:

- Alarm and Warning flags as described in the section on Basic Monitoring Functions. These correspond to monitored quantities going outside factory programmed threshold values.
- Flags corresponding to basic module status conditions including:

TX_NR:	Any condition leading to invalid data on the TX path
TX_Fault	Laser fault condition (same as TX_Fault in SFP and GBIC)
TX CDR Unlocked:	Unlocked:Loss of Lock of TX side CDR
RX_NR:	Any condition leading to invalid data on the RX path
RX_LOS:	RX Loss of Signal (mirroring hardware output pin)
RX_CDR Unlocked:	Unlocked:Loss of Lock of RX side CDR
MOD_NR:	Module Not Ready (mirroring hardware output pin)

- Flag indicating completion of the XFP Module Reset (as initiated by power up or P_Down/RST pin)
- Flags corresponding to optional extended capabilities including:
    - APD Supply Fault
    - TEC Fault
    - Wavelength Unlocked Condition

Existence of any of these conditions shall lead to a latched flag. These flags are located in Bytes 80 – 87 and are detailed in Table 39.

The presence of any 1 values in Bytes 80 – 87 will assert the hardware Interrupt output pin (active low). When the Interrupt pin alerts the host system to a latched flag condition, the host may query the latched flag bits in Bytes 80 – 87. The latched flags are cleared on the read of the corresponding Byte. Thus a read of all Bytes from 80 – 87 can be used to reset all latched flags and deassert the hardware Interrupt output pin.

Because of the bytewise nature of the 2-wire serial bus reads, it is not possible to clear individual flag bits. It is recommended that all latched flag bits be read and cleared in the same operation.

The host system may control which flags result in an Interrupt by setting high individual bits from a set of masking bits in Bytes 88-95, and described in Table 40. A 1 value in a masking bit prevents the assertion of the hardware Interrupt pin by the corresponding latched flag bit.

Masking bits should be volatile and startup with all unmasked (masking bits 0).

Hardware Interrupt Pin = Logical NOR of all (Latched Flag Bit AND NOT Masking Bit)

The mask bits may be used to prevent continued interruption from ongoing conditions, which would otherwise continually reassert the hardware Interrupt pin.

5.11.1 GENERAL CONTROL AND STATUS BITS

In order to allow virtually complete operation of the XFP module via the 2-wire serial interface, a set of control and status bits are provided to mirror the operation of key status and control pins. These are provided in Bytes 110-111 and are detailed in Table 42. All status bits except soft bits in this set are dynamic (not latched)

The bits fall into three categories:

- Bits mirroring hardware status lines: TX-DIS, MOD_NR, P_Down/RST, Interrupt, RX_LOS
- Bits providing more specific information: TX_NR, RX_NR, TX and RX CDR Loss of Lock, and TX Fault.
- A set of read/write bits which can be used to implement the optional “soft” control of TX-Disable and the Power-Down functions. (Described fully in Table 42). Availability of this option is defined in Byte 221 (Table 01h).

5.12 TIMING FOR SOFT CONTROL AND STATUS FUNCTIONS

Detail timing for soft control and status functions are described in Table 45 accessible with the 2-wire Serial interface Chapter 4:.

Table 34 Signal Conditioner Control Field

Byte	*Bit*	*Name*	*Description*
1	7-4	Data Rate Control	Data Rate=9.5Gb/s + 0.2 * Value
	3	Reserved	
	2	Lineside Loopback	0b=Normal Operation 1b=Loopback Module Optical Input to Output
	1	XFI Loopback	0b=Normal Operation 1b=Loopback Module XFI Input to Output
	0	Signal Conditioner Control	0b = Normal Asynchronous REFCLK mode 1b = Optional Synchronous REFCLK mode

.

Table 35 Alarm and Warning Thresholds

Address	*# Bytes*	*Name*	*Description*
02-03	2	Temp High Alarm	MSB at low address
04-05	2	Temp Low Alarm	MSB at low address
06-07	2	Temp High Warning	MSB at low address
08-09	2	Temp Low Warning	MSB at low address
10-17	8	Reserved A/D Flag Thresholds	Reserved A/D Flag Thresholds
18-19	2	Bias High Alarm	MSB at low address
20-21	2	Bias Low Alarm	MSB at low address
22-23	2	Bias High Warning	MSB at low address
24-25	2	Bias Low Warning	MSB at low address
26-27	2	TX Power High Alarm	MSB at low address
28-29	2	TX Power Low Alarm	MSB at low address
30-31	2	TX Power High Warning	MSB at low address
32-33	2	TX Power Low Warning	MSB at low address
34-35	2	RX Power High Alarm	MSB at low address
36-37	2	RX Power Low Alarm	MSB at low address
38-39	2	RX Power High Warning	MSB at low address
40-41	2	RX Power Low Warning	MSB at low address
42-43	2	AUX 1 High Alarm	MSB at low address
44-45	2	AUX 1 Low Alarm	MSB at low address
46-47	2	AUX 1 High Warning	MSB at low address
48-49	2	AUX 1 Low Warning	MSB at low address
50-51	2	AUX 2 High Alarm	MSB at low address
52-53	2	AUX 2 Low Alarm	MSB at low address
54-55	2	AUX 2 High Warning	MSB at low address
56-57	2	AUX 2 Low Warning	MSB at low address

Table 36 BER Control Fields

Byte	*Bit*	*Name*	*Description*
70	All	Acceptable BER	Acceptable BER Reported by the FEC to the Module
71	All	Actual BER	Actual BER Reported by the FEC to the Module

Table 37 Wavelength Control Fields

Byte	*Bit*	*Name*	*Description*
72 - 73	All	Wavelength Set MSB	User input of Wavelength setpoint. (Units of 0.05 nm)
74 - 75	All	Wavelength Error LSB	Monitor of Current Wavelength Error (Units of 0.005nm) [Signed 2’s complement value]

Table 38 FEC Control Fields

Byte	*Bit*	*Name*	*Description*
76	All	Amplitude Adjustment	Relative amplitude of receive quantization threshold
77	All	Phase Adjustment	Phase of receive quantization relative to 0.5 UI.
78-79	All	Reserved	

Table 39 Latched Interrupt Flag Fields

Address	*# Bit*	*Name*	*Description*
80	7	L- Temp High Alarm	Latched high Temperature alarm.
80	6	L- Temp Low Alarm	Latched low Temperature alarm.
80	5	Reserved	
80	4	Reserved	
80	3	L- TX Bias High Alarm	Latched high TX Bias alarm.
80	2	L- TX Bias Low Alarm	Latched low TX Bias alarm.
80	1	L- TX Power High Alarm	Latched high TX Power alarm.
80	0	L- TX Power Low Alarm	Latched low TX Power alarm.
81	7	L- RX Power High Alarm	Latched high RX Power alarm.
81	6	L- RX Power Low Alarm	Latched low RX Power alarm.
81	5	L- AUX 1 High Alarm	Latched high AUX1 monitor alarm.
81	4	L- AUX 1 Low Alarm	Latched low AUX1 monitor alarm.
81	3	L- AUX 2 High Alarm	Latched high AUX2 monitor alarm.
81	2	L- AUX 2 Low Alarm	Latched low AUX2 monitor alarm.
81	1	Reserved	
81	0	Reserved	
82	7	L- Temp High Warning	Latched high Temperature warning.
82	6	L- Temp Low Warning	Latched low Temperature warning.
82	5	Reserved	
82	4	Reserved	
82	3	L- TX Bias High Warning	Latched high TX Bias warning.
82	2	L- TX Bias Low Warning	Latched low TX Bias warning.
82	1	L- TX Pow. High Warning	Latched high TX Power warning.
82	0	L- TX Pow. Low Warning	Latched low TX Power warning.
83	7	L- RX Pow. High Warning	Latched high RX Power warning.
83	6	L- RX Pow. Low Warning	Latched low RX Power warning.
83	5	L- AUX 1 High Warning	Latched high AUX1 monitor warning.
83	4	L- AUX 1 Low Warning	Latched low AUX1 monitor warning.
83	3	L- AUX 2 High Warning	Latched high AUX2 monitor warning.
83	2	L- AUX 2 Low Warning	Latched low AUX2 monitor warning.
83	1	Reserved	

Table 39 Latched $\overline{\text{Interrupt}}$ Flag Fields

Address	*# Bit*	*Name*	*Description*
83	0	Reserved	
84	7	L- TX_NR	Latched TX_NR Status
84	6	L- TX_Fault	Latched Laser Fault condition. Generated by laser safety system.
84	5	L- TX CDR not Locked	Latched TX CDR Loss of Lock
84	4	L- RX_NR	Latched RX_NR Status
84	3	L- RX_LOS	Latched mirror of RX_LOS pin (Receiver loss of optical signal)
84	2	L- RX CDR not Locked	Latched RX CDR Loss of Lock
84	1	L- MOD_NR	Latched Mirror of MOD_NR pin
84	0	L- Reset Complete	Latched Reset Complete Flag
85	7	L- APD Supply Fault	Latched APD Supply Fault
85	6	L- TEC Fault	Latched TEC Fault
85	5	L- Wavelength Unlocked	Latched Wavelength Unlocked Condition
85	4-0	Reserved	
86	7	L-VCC5 High Alarm	VCC5 High Alarm Flag
86	6	L-VCC5 Low Alarm	VCC5 Low Alarm Flag
86	5	L-VCC3 High Alarm	VCC3 High Alarm Flag
86	4	L-VCC3 Low Alarm	VCC3 Low Alarm Flag
86	3	L-VCC2 High Alarm	VCC2 High Alarm Flag
86	2	L-VCC2 Low Alarm	VCC2 Low Alarm Flag
86	1	L-Vee5 High Alarm	Vee5 High Alarm Flag
86	0	L-Vee5 Low Alarm	Vee5 Low Alarm Flag
87	7	L-VCC5 High Warning	VCC5 High Warning Alarm Flag
87	6	L-VCC5 Low Warning	VCC5 Low Warning Flag
87	5	L-VCC3 High Warning	VCC3 High Warning Flag
87	4	L-VCC3 Low Warning	VCC3 Low Warning Flag
87	3	L-VCC2 High Warning	VCC2 High Warning Flag
87	2	L-VCC2 Low Warning	VCC2 Low Warning Flag
87	1	L-Vee5 High Warning	Vee5 High Warning Flag
87	0	L-Vee5 Low Warning	Vee5 Low Warning Flag

.

Table 40 Interrupt Masking Bits

Address	*# Bit*	*Name*	*Description*
88	7	M- Temp High Alarm	Masking bit for high Temperature alarm.
88	6	M- Temp Low Alarm	Masking bit for low Temperature alarm.
88	5	Reserved	
88	4	Reserved	
88	3	M- TX Bias High Alarm	Masking bit for high TX Bias alarm.
88	2	M- TX Bias Low Alarm	Masking bit for low TX Bias alarm.
88	1	M- TX Power High Alarm	Masking bit for high TX Power alarm.
88	0	M- TX Power Low Alarm	Masking bit for low TX Power alarm.
89	7	M- RX Power High Alarm	Masking bit for high RX Power alarm.
89	6	M- RX Power Low Alarm	Masking bit for low RX Power alarm.
89	5	M- AUX 1 High Alarm	Masking bit for high AUX1 monitor alarm.
89	4	M- AUX 1 Low Alarm	Masking bit for low AUX1 monitor alarm.
89	3	M- AUX 2 High Alarm	Masking bit for high AUX2 monitor alarm.
89	2	M- AUX 2 Low Alarm	Masking bit for low AUX2 monitor alarm.
89	1	Reserved	
89	0	Reserved	
90	7	M- Temp High Warning	Masking bit for high Temperature warning.
90	6	M- Temp Low Warning	Masking bit for low Temperature warning.
90	5	Reserved	
90	4	Reserved	
90	3	M- TX Bias High Warning	Masking bit for high TX Bias warning.
90	2	M- TX Bias Low Warning	Masking bit for low TX Bias warning.
90	1	M- TX Pow. Hi Warning	Masking bit for high TX Power warning.
90	0	M- TX Pow. Low Warning	Masking bit for low TX Power warning.
91	7	M- RX Pow. Hi Warning	Masking bit for high RX Power warning.
91	6	M- RX Pow. Low Warning	Masking bit for low RX Power warning.
91	5	M- AUX 1 High Warning	Masking bit for high AUX1 monitor warning.
91	4	M- AUX 1 Low Warning	Masking bit for low AUX1 monitor warning.
91	3	M- AUX 2 High Warning	Masking bit for high AUX2 monitor warning.
91	2	M- AUX 2 Low Warning	Masking bit for low AUX2 monitor warning.

Table 40 Interrupt Masking Bits

Address	*# Bit*	*Name*	*Description*
91	1	Reserved	
91	0	Reserved	
92	7	M- TX_NR	Masking bit for TX_NR Status
92	6	M- TX_Fault	Masking bit for Laser Fault condition.
92	5	M- TX CDR not Locked	Masking bit for TX CDR Loss of Lock
92	4	M- RX_NR	Masking bit for RX_NR Status
92	3	M- RX_LOS	Masking bit for mirror of RX_LOS pin (Receiver optical loss of signal)
92	2	M- RX CDR not Locked	Masking bit for RX CDR Loss of Lock
92	1	M- MOD_NR	Masking bit for Mirror of MOD_NR pin
92	0	M- Reset Complete	Masking bit for Reset Complete Flag
93	7	M- APD Supply Fault	Masking bit for APD Supply Fault
93	6	M- TEC Fault	Masking bit for TEC Fault
93	5	M- Wavelength Unlocked	Masking bit for Wavelength Unlocked Condition
93	4-0	Reserved	
94	7	M-VCC5 High Alarm	VCC5 High Alarm Flag
94	6	M-VCC5 Low Alarm	VCC5 Low Alarm Flag
94	5	M-VCC3 High Alarm	VCC3 High Alarm Flag
94	4	M-VCC3 Low Alarm	VCC3 Low Alarm Flag
94	3	M-VCC2 High Alarm	VCC2 High Alarm Flag
94	2	M-VCC2 Low Alarm	VCC2 Low Alarm Flag
94	1	M-Vee5 High Alarm	Vee5 High Alarm Flag
94	0	M-Vee5 Low Alarm	Vee5 Low Alarm Flag
95	7	M-VCC5 High Warning	VCC5 High Warning Alarm Flag
95	6	M-VCC5 Low Warning	VCC5 Low Warning Flag
95	5	M-VCC3 High Warning	VCC3 High Warning Flag
95	4	M-VCC3 Low Warning	VCC3 Low Warning Flag
95	3	M-VCC2 High Warning	VCC2 High Warning Flag
95	2	M-VCC2 Low Warning	VCC2 Low Warning Flag
95	1	M-Vee5 High Warning	Vee5 High Warning Flag
95	0	M-Vee5 Low Warning	Vee5 Low Warning Flag

Table 41 A/D Values

Byte	*Bit*	*Name*	*Description*
Converted analog values. Calibrated 16 bit data.			
96	All	Temperature MSB	Internally measured module temperature.
97	All	Temperature LSB	
98-99	All		Reserved
100	All	TX Bias MSB	Internally measured TX Bias Current.
101	All	TX Bias LSB	
102	All	TX Power MSB	Measured TX output power.
103	All	TX Power LSB	
104	All	RX Power MSB	Measured RX input power.
105	All	RX Power LSB	
106	All	AUX 1 MSB	Auxiliary measurement 1 defined in Byte 222 Page 01h
107	All	AUX 1 LSB	
108	All	AUX 2 MSB	Auxiliary measurement 2 defined in Byte 222 Page 01h
109	All	AUX 2 LSB	

Table 42 General Control/Status Bits

Byte	*Bit*	*Name*	*Description*
110	7	TX Disable State	Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin.
110	6	Soft TX Disable	Optional read/write bit that allows software disable of laser. Writing '1' disables laser. Turn on/off time is 100 msec max from acknowledgement of serial byte transmission. This bit is “OR”d with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0.
110	5	MOD_NR State	Digital state of the MOD_NR Pin. Updated within 100msec of change on pin.
110	4	P_Down State	Digital state of the P_Down Pin. Updated within 100msec of change on pin.
110	3	Soft P_Down	Optional read/write bit that allows the module to be placed in the power down mode. This is identical to the P_Down hardware pin function except that it does not initiate a system reset.
110	2	$\overline{\text{Interrupt}}$	Digital state of the $\overline{\text{Interrupt}}$ output pin.
110	1	RX_LOS	Indicates Optical Loss of Signal (per relevant optical link standard). Updated within 100msec of change on pin.
110	0	Data_Not_Ready	Indicates transceiver has achieved power up and A/D data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low.
111	7	TX_NR State	Identifies Not Ready condition as specific to the TX path
111	6	TX_Fault State	Identifies Laser fault condition (Generated by laser safety system)
111	5	TX_CDR not Locked	Identifies Loss of Lock in TX path CDR
111	4	RX_NR State	Identifies Not Ready condition as specific to the TX path
111	3	RX_CDR not Locked	Identifies Loss of Lock in RX path CDR
111	2-0	Reserved	

The Data_Not_Ready bit is high during module power up and prior to the first valid A/D reading. Once the first valid A/D reading occurs, the bit is set low until the device is powered down. The bit must be set low within 1 second of power up.

Table 43 Packet Error Checking

Byte	Bit	Name	Description
118	0	Error Checking	0 b = Disable Packet Error Checking 1b = Enable Packet Error Checking (see Section 4.5.6 and 4.5.9)
118	7-1	Reserved	

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Table 44 Password and Table Select Entry Bytes

Byte	Bit	Name	Description
119-122	All	New Password Entry	Location of Entry of New Optional Password
123-126	All	Password Entry	Location for Entry of Optional Password
127	All	Table Select	Entry Location for Table Select Byte

Table 45 I/O Timing for Soft Control & Status Functions

Parameter	Symbol	Min	Max	Unit	Conditions
TX_DISABLE assert time	t_off		100	ms	Time from TX_DIS bit set [1] until optical output falls below 10% of nominal
TX_DISABLE deassert time	t_on		100	ms	Time from TX_DISABLE bit cleared[1] until optical output rises above 90% of nominal
P_Down assert time	T_Pdown		100	ms	Time from P_Down bit set[1] until module dissipation falls below 1.5W
P_Down deassert time	T_Pup		300	ms	Time from P_Down bit cleared[1] until module returns to normal operation.
RX_LOS assert time	t_los_on		100	ms	Time from RX_LOS state to RX_LOS bit set
RX_LOS deassert time	t_los_off		100	ms	Time from non-LOS state to RX_LOS bit cleared
MOD_NR assert time	t_NR_on		100	ms	Time from TX_NR or RX_NR state to corresponding bit set
MOD_NR deassert time	t_NR_off		100	ms	Time from non-TX_NR or RX_NR state to corresponding bit set
Analog parameter data ready	t_data		1000	ms	From power on to data ready, bit 0 of byte 110 set

1. Measured from falling clock edge after stop bit of write transaction.

5.13 DESCRIPTION OF UPPER MEMORY MAP TABLE 00H – FUTURE DIAGNOSTICS FUNCTIONS

Table 00h is reserved for future diagnostics functions.

5.14 DESCRIPTION OF UPPER MEMORY MAP TABLE 01H – SERIAL ID MEMORY MAP

The serial ID memory map located in Table 01h in the upper address space is used for read only identification information.

Table 46 Serial ID: Data Fields - Page 01h

Address	***Size (Bytes)***	***Name***	***Description***
		Base ID Fields	
128	1	Identifier	Type of serial transceiver (see Table 32)
129	1	Ext. Identifier	Extended identifier of type of serial transceiver (see Table 47)
130	1	Connector	Code for connector type (see Table 48)
138-131	8	Transceiver	Code for electronic compatibility or optical compatibility (see Table 49)
139	1	Encoding	Code for serial encoding algorithm (see Table 50)
140	1	BR-Min	Minimum bit rate, units of 100 MBits/s.
141	1	BR-Max	Maximum bit rate, units of 100 MBits/s.
142	1	Length(SMF)-km	Link length supported for SMF fiber in km
143	1	Length (E-50µm)	Link length supported for EBW 50/125 µm fiber, units of 2 m
144	1	Length (50 µm)	Link length supported for 50/125 µm fiber, units of 1 m
145	1	Length (62.5 µm)	Link length supported for 62.5/125 µm fiber, units of 1 m
146	1	Length (Copper)	Link length supported for copper, units of 1m
147	1	Device Tech	Device technology (see Table 51, Table 52)
163-148	16	Vendor name	XFP vendor name (ASCII)
164	1	CDR Support	CDR Rate Support (see Table 53)
167-165	3	Vendor OUI	XFP vendor IEEE company ID
183-168	16	Vendor PN	Part number provided by XFP vendor (ASCII)
185-184	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
187-186	2	Wavelength	Nominal laser wavelength (Wavelength = value / 20 in nm)

Table 46 Serial ID: Data Fields - Page 01h

Address	*Size (Bytes)*	*Name*	*Description*
189-188	2	Wavelength Tolerance	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength. (Wavelength Tol. = value/200 in nm)
190	1	Max Case Temp	Maximum Case Temperature in Degrees C.
191	1	CC_BASE	Check code for Base ID Fields (addresses 120-190)
Extended ID Fields			
195-192	4	Power Supply	Power supply current requirements and max power dissipation (see Table 54)
211-196	16	Vendor SN	Serial number provided by vendor (ASCII)
219-212	8	Date code	Vendor's manufacturing date code (see Table 55)
220	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the transceiver (see Table 56) Bit 1, 0 Reserved
221	1	Enhanced Options	Indicates which optional enhanced features are implemented (if any) in the transceiver (see Table 57)
222	1	Aux Monitoring	Defines quantities reported by Aux. A/D channels (see Table 58 Table 59)
223	1	CC_EXT	Check code for the Extended ID Fields (addresses 192 to 222)
Vendor Specific ID Fields			
255-224	32	Vendor Specific	Vendor Specific EEPROM

5.15 IDENTIFIER

Byte 0 of the lower memory map contains the module identifier value. The identifier value specifies the physical device described by the serial ID information. This value is also included in the serial ID data table (01h). The defined identifier values are shown in Table 32. The XFP transceiver should use identifier 06h.

5.16 EXTENDED IDENTIFIER

The extended identifier value provides additional information about the basic transceiver types Table 47.

This field existed in the GBIC specification to identify the various module definitions. These definitions do not apply to the XFP. The space is used to identify whether the transceiver contains a CDR function and identifies its power dissipation class it belongs. The field also identifies whether a CLEI identifier code is present in Table 02h of the memory map (see Section 5.45)

Table 47 Extended Identifier values Byte 129

Bit	*Description of device type*
7-6	00: Power Level 1 Module (1.5 W max. power dissipation.) 01: Power Level 2 Module (2.5W Max) 10: Power Level 3 Module (3.5W max. power dissipation.) 11: Power Level 4 Module (>3.5W max. power dissipation.)
5	0: Module with CDR function 1: Non-CDR version of XFP
4	0: TX Ref Clock Input Required 1: TX Ref Clock Input Not Required
3	0: No CLEI code present in Table 02h 1: CLEI code present in Table 02h
2-0	Reserved

5.17 CONNECTOR

The Connector value indicates the external connector provided on the interface. This value shall be included in the serial data. The defined connector values are shown in Table 48. Note that some connectors in this table are mechanically incompatible with the XFP dimensions. This full list is included for compatibility with GBIC and SFP standards in the selection of potential future connector codes.

Table 48 Connector values Byte 130

Register	*Description of connector*
00h	Unknown or unspecified
01h	SC
02h	Fibre Channel Style 1 copper connector
03h	Fibre Channel Style 2 copper connector
04h	BNC/TNC
05h	Fibre Channel coaxial headers
06h	FiberJack
07h	LC
08h	MT-RJ
09h	MU
0Ah	SG
0Bh	Optical pigtail
0C-1Fh	Reserved
20h	HSSDC II
21h	Copper Pigtail
22h-7Fh	Reserved
80-FFh	Vendor specific

5.18 INTERFACE SPECIFICATION

The following bit significant indicators define the electronic or optical interfaces that are supported by the transceiver Table 49. At least one bit shall be set in this field. This table is not backward compatible with the GBIC/SFP serial ID definition.

Table 49 Transceiver codes

Addr	*Bit*	*Description of transceiver*	*Addr*	*Bit*	*Description of transceiver*
10 Gigabit Ethernet Compliance			*SONET/SDH Codes - Interconnect*		
131	7	10GBASE-SR	135	7	I-64.1r
131	6	10GBASE-LR	135	6	I-64.1
131	5	10GBASE-ER	135	5	I-64.2r
131	4	10GBASE-LRM	135	4	I-64.2
131	3	10GBASE-SW	135	3	I-64.3
131	2	10GBASE-LW	135	2	I-64.5
131	1	10GBASE-EW	135	1	Reserved
131	0	Reserved	135	0	Reserved
10 Gigabit Fibre Channel Compliance			*SONET/SDH Codes – Short Haul*		
132	7	1200-MX-SN-I	136	7	S-64.1
132	6	1200-SM-LL-L	136	6	S-64.2a
132	5	Extended Reach 1550 nm	136	5	S-64.2b
132	4	Intermediate Reach 1300 nm FP	136	4	S-64.3a
132	3	Reserved	136	3	S-64.3b
132	2	Reserved	136	2	S-64.5a
132	1	Reserved	136	1	S-64.5b
132	0	Reserved	136	0	Reserved
10 Gigabit Copper Links			*SONET/SDH Codes – Long Haul*		
133	7	Reserved	137	7	L-64.1
133	6	Reserved	137	6	L-64.2a
133	5	Reserved	137	5	L-64.2b
133	4	Reserved	137	4	L-64.2c
133	3	Reserved	137	3	L-64.3
133	2	Reserved	137	2	G.959.1 P1L1-2D2
133	1	Reserved	137	1	Reserved
133	0	Reserved	137	0	Reserved
Lower Speed Links			*SONET/SDH Codes – Very Long Haul*		
134	7	1000BASE-SX / 1xFC MMF	138	7	V-64.2a

Table 49 Transceiver codes

Addr	*Bit*	*Description of transceiver*	*Addr*	*Bit*	*Description of transceiver*
134	6	1000BASE-LX/1xFC SMF	138	6	V-64.2b
134	5	2xFC MMF	138	5	V-64.3
134	4	2xFC SMF	138	4	Reserved
134	3	OC 48-SR	138	3	Reserved
134	2	OC-48-IR	138	2	Reserved
134	1	OC-48-LR	138	1	Reserved
134	0	Reserved	138	0	Reserved

5.19 ENCODING

The encoding bits indicate the serial encoding mechanisms that are supported by the particular transceiver. A one in a given bit position indicates support of that encoding mechanism. The defined encoding support bits are shown in Table 50.

Table 50 Encoding Support Byte 139

Bit	*Description of encoding mechanism*
7	64B/66B
6	8B10B
5	SONET Scrambled
4	NRZ
3	RZ
2	Reserved
1	Reserved
0	Reserved

5.20 BR, MINIMUM

The minimum bit rate (BR, minimum) is specified in units of 100 Megabits per second, rounded off to the nearest 100 Megabits per second. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of 0 indicates that the minimum bit rate is not specified and must be determined from the transceiver technology. The actual information transfer rate will depend on the encoding of the data, as defined by the encoding value. Specific CDR rate support is indicated in Byte 164.

5.21 BR, MAXIMUM

The maximum bit rate (BR, maximum) is specified in units of 100 Megabits per second, rounded off to the nearest 100 Megabits per second. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of 0 indicates that the maximum bit rate is not specified and must be determined from the transceiver technology. The actual information transfer rate will depend on the encoding of the data, as defined by the encoding value. Specific CDR rate support is indicated in Byte 164.

5.22 LENGTH (STANDARD SINGLE MODE FIBER)-KM

This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using single mode fiber. The value is in units of kilometers. A value of 255 means that the transceiver supports a link length greater than 254 km. A length field value of 0 for XFP modules indicates that the length should be the operating length specified by the supported standard Table 49.

5.23 LENGTH (EXTENDED BANDWIDTH 50 MM MULTIMODE FIBER)

This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using 2000 MHz*km (850nm) extended bandwidth 50 micron core multimode fiber. The value is in units of 2 meters. A value of 255 means that the transceiver supports a link length greater than 508 m. A length field value of 0 for XFP modules indicates that the length should be the operating length specified by the supported standard Table 49.

5.24 LENGTH (50 UM MULTIMODE FIBER)

This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using 500 MHz*km (850 and 1310nm) 50 micron core multimode fiber. The value is in units of meters. A value of 255 means that the transceiver supports a link length greater than 254 m. A length field value of 0 for XFP modules indicates that the length should be the operating length specified by the supported standard Table 49.

5.25 LENGTH (62.5 UM MULTIMODE FIBER)

This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using 200 MHz*km (850 nm) / 500 MHz*km (1310 nm) 62.5 micron core multimode fiber. The value is in units of meters. A value of 255 means that the transceiver supports a link length greater than 254 m. A length field value of 0 for XFP modules indicates that the length should be the operating length specified by the supported standard Table 49.

5.26 LENGTH (COPPER)

This value specifies the minimum link length that is supported by the transceiver while operating in compliance with the applicable standards using copper cable. The value is in units of meters. A value of 255 means that the transceiver supports a link length greater than 254 meters. A value of zero means that the transceiver does not support copper cables or that the length information must be determined from the transceiver technology. Further information about the cable design, equalization, and connectors is usually required to guarantee meeting a particular length requirement. This also specifies the total cable length of copper cable assemblies with integrated XFP's.

5.27 DEVICE TECHNOLOGY

This byte contains information about the laser, detector and any cooling technology. The defined identifier values are shown in Table 51 and Table 52.

Table 51 Device Technology (Value of lower 4 bits of Byte 147)

Bits	*Description of physical device*
7-4	Transmitter technology (see Table 52)
3	0: No wavelength control 1: Active wavelength control
2	0: Uncooled transmitter device 1: Cooled transmitter
1	Detector Type 0: PIN detector 1: APD detector
0	0: Transmitter not Tunable 1: Transmitter Tunable

Table 52 Transmitter Technology (Value of top 4 bits of Byte 147)

Value	*Description of physical device*
0000b	850 nm VCSEL
0001b	1310 nm VCSEL
0010b	1550 nm VCSEL
0011b	1310 nm FP
0100b	1310 nm DFB
0101b	1550 nm DFB
0110b	1310 nm EML
0111b	1550 nm EML
1000b	Copper or others
1111b-1001b	Reserved

5.28 VENDOR NAME

The vendor name is a 16 character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

5.29 CDR SUPPORT

The nominal XFP design has CDR technology on both the transmit and receive path. Individual XFP devices may or may not support all the standard 10G bit rates. This Byte indicates which rates are supported by the CDR. A value of 0 indicates no CDR support. Table 53 defines the CDR support bits.

This Byte is also used to indicate which if any of the loopback modes are supported. A 1 in bit 0 indicates that XFI loopback is supported (controlled by the bits listed in Table 34). A 1 in bit 1 indicates that lineside (optical to optical) loopback is supported.

Table 53 CDR Support Byte 164

Bits	*Description of physical device*
7	CDR support for 9.95 Gb/s
6	CDR support for 10.3 Gb/s
5	CDR support for 10.5 Gb/s
4	CDR support for 10.7 Gb/s
3	CDR support for 11.1 Gb/s
2	Reserved
1	Lineside Loopback Mode Supported
0	XFI Loopback Mode Supported

5.30 VENDOR OUI

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

5.31 VENDOR PN

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

5.32 VENDOR REV

The vendor revision number (vendor rev) is a 2-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the 2-byte field indicates that the vendor PN is unspecified.

5.33 LASER WAVELENGTH

Nominal transmitter output wavelength at room temperature. 16 bit value with byte 186 as high order byte and byte 187 as low order byte. The laser wavelength is equal to the 16 bit integer value divided by 20 in nm (units of 0.05nm). This resolution should be adequate to cover all relevant wavelengths yet provide enough resolution for all expected DWDM applications. For accurate representation of controlled wavelength applications, this value should represent the center of the guaranteed wavelength range.

5.34 LASER WAVELENGTH TOLERANCE

The guaranteed +/- range of transmitter output wavelength under all normal operating conditions. 16 bit value with byte 188 as high order byte and byte 189 as low order byte. The laser wavelength is equal to the 16 bit integer value divided by 200 in nm (units of 0.005nm). Thus, the following two examples:

<u>Example 1:</u>
10GBASE-LR Wavelength Range = 1260 to 1355 nm

Nominal Wavelength in Bytes 186 - 187 = 1307.5 nm.
Represented as INT(1307.5 nm * 20) = 26150 = 6626h

Wavelength Tolerance in Bytes 188 - 189 = 47.5nm.
Represented as INT(47.5 nm * 200) = 9500 = 251Ch

Example 2:
ITU-T Grid Wavelength = 1534.25 nm (195.4 THz) with 0.236 nm (30 GHz) Tolerance

Nominal Wavelength in Bytes 186 - 187 = 1534.25 nm.
Represented as INT(1534.25nm * 20) = 30685 = 77DDh

Wavelength Tolerance in Bytes 188 - 189 = 0.236 nm.
Represented as INT(0.236 nm * 200) = 47 = 002Fh

5.35 MAXIMUM CASE TEMPERATURE

Allows specification of a maximum case temperature other than the MSA standard of 70C. Maximum case temperature is an 8-bit value in Degrees C.

5.36 CC_BASE

The check code is a one byte code that can be used to verify that the first 64 bytes of serial information in the XFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 128 to byte 190, inclusive.

5.37 POWER SUPPLY REQUIREMENTS

Bytes 192-195 contain information on the maximum current requirement of each of the four power supplies, as well as the maximum power dissipation of the modules. This information allows system vendors to do more careful power supply and thermal dissipation management. The data format for this information is described in Table 54

Table 54 Power Supply Related Fields

data address	*bits*	*Description of Fields*
192	7-0	Maximum Power Dissipation Max power is 8 bit value * 20 mW.
193	7-0	Maximum Total Power Dissipation in Power Down Mode Max Power is 8 bit value * 10 mW.
194	7-4	Maximum current required by +5V Supply. Max current is 4 bit value * 50 mA. [500 mA max]
194	3-0	Maximum current required by +3.3V Supply. Max current is 4 bit value * 100 mA.
195	7-4	Maximum current required by +1.8V Supply Max current is 4 bit value * 100 mA.
195	3-0	Maximum current required by -5.2V Supply. Max current is 4 bit value * 50 mA. [500 mA max]

5.38 VENDOR SN

The vendor serial number (vendor SN) is a 16 character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the transceiver. A value of all zero in the 16-byte field indicates that the vendor SN is unspecified.

5.39 DATE CODE

The date code is an 8-byte field that contains the vendor’s date code in ASCII characters. The date code is mandatory. The date code shall be in the format specified by Table 55.

Table 55 Date Code

Data Address	*Description of field*
212-213	ASCII code, two low order digits of year. (00 = 2000).
214-215	ASCII code, digits of month (01 = Jan. through 12 = Dec.)
216-217	ASCII code, day of month (01 - 31)
218-219	ASCII code, vendor specific lot code, may be blank

5.40 DIAGNOSTIC MONITORING TYPE

“Diagnostic Monitoring Type” is a 1 byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the particular transceiver. Bit indicators are detailed in Table 56.

Digital diagnostic monitors received power, transmitted power, bias current, supply voltage, and temperature. Additionally, alarm and warning thresholds must be written as specified in this document at locations 02 – 57 (see Table 35). Auxiliary monitoring fields are optional extensions to Digital Diagnostics

Unlike the system described in SFF-8472, the XFP digital diagnostics definition does not allow for the possibility of “external calibration”. All digital diagnostic values must be internally calibrated and reported in the units defined in this document.

Bit 3 indicates whether the received power measurement represents average input optical power or OMA. If the bit is set, average power is monitored. If it is not, OMA is monitored.

Table 56 Diagnostic Monitoring Type

Data Address	*Bits*	*Description*
220	7-5	Reserved
220	4	Module Respond to FEC BER 0= No BER Support, 1=BER Support
220	3	Received power measurement type 0 = OMA, 1 = Average Power
220	2	Reserved
220	1- 0	Reserved

5.41 ENHANCED OPTIONS

“Enhanced Options” is a 1 byte field with 8 single bit indicators which describe the optional digital control and diagnostic features implemented in the transceiver, as well as optional operating modes (see Table 57).

The optional digital controls are the Soft TX Disable and Power down functions which allow the functions to be actuated via the 2-wire serial control bus.

The optional operating modes indicate the ability of the module to perform active FEC and wavelength tunability functions, as well as the ability to support the optional Synchronous REFCLK mode.

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Table 57 Enhanced Options

Data Address	*Bits*	*Description*
221	7	Module Supports Optional VPS
221	6	Optional Soft TX_DISABLE implemented
221	5	Optional Soft P_down implemented
221	4	Supports VPS LV regulator mode
221	3	Supports VPS bypassed regulator Mode
221	2	Active FEC control functions implemented
221	1	Wavelength tunability implemented
221	0	Optional CMU Support Mode

5.42 AUXILIARY MONITORING

This standard defines two flexible auxiliary A/D monitoring channels. This Byte, defined in Table 58 and Table 59 describes which quantities are monitored by each auxiliary A/D channel.

Table 58 Auxiliary A/D Types Byte 222

Bits	*A/D Input*
7-4	Aux A/D Input 1 (see Table 59)
3-0	Aux A/D Input 2 (see Table 59)

Table 59 Auxiliary Input Types

Value	*Description of physical device*
0000b	Auxiliary monitoring not implemented
0001b	APD Bias Voltage (16 bit value is Voltage in units of 10 mV)
0010b	Reserved
0011b	TEC Current (mA) (16 bit value is Current in units of 100 uA)
0100b	Laser Temperature (Same encoding as module temperature)
0101b	Laser Wavelength (same Encoding as Bytes 186-187)
0110b	+5V Supply Voltage (Encoded as described in section 5.6)
0111b	+3.3V Supply Voltage (Encoded as described in section 5.6)
1000b	+1.8V Supply Voltage (Encoded as described in section 5.6)
1001b	-5.2V Supply Voltage (Absolute Value Encoded as primary Voltage Monitor)
1010b	+5V Supply Current (16 bit Value is Current in 100 uA)
1101b	+3.3V Supply Current (16 bit Value is Current in 100 uA)
1110b	+1.8V Supply Current (16 bit Value is Current in 100 uA)
1111b	-5.2V Supply Current (16 bit Value is Current in 100 uA)

5.43 CC_EXT

The check code is a one byte code that can be used to verify that the first 31 bytes of extended serial information in the XFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 192 to byte 222, inclusive.

5.44 VENDOR SPECIFIC ID FIELD

Bytes 224-255h of Table 01h may be used for Vendor Specific ID functions.

5.45 DESCRIPTION OF UPPER MEMORY MAP TABLE 02H – USER EEPROM DATA

Table 02h is provided as user writable EEPROM. The host system may read or write this memory for any purpose. If bit 3 of Table 01h Byte 129 is set, however, the first 10 bytes of Table 02h [128-137h] will be used to store the CLEI code for the module.

5.46 DESCRIPTION OF UPPER MEMORY MAP TABLES 03H – 7FH VENDOR SPECIFIC FUNCTIONS

Tables 03h-7Fh are reserved for Vendor Specific functions.

5.47 DESCRIPTION OF UPPER MEMORY MAP TABLES 80H – FFH RESERVED

Tables 80h-FFh are reserved.

CHAPTER 6: MECHANICAL AND BOARD DEFINITION

6.1 INTRODUCTION

The mechanical components defined in this section are illustrated in Figure 29. The module, clip and connector dimensions are constant for all applications. While the bezel, cage assembly, EMI gasket and heat sink can be designed and/or adjusted for the individual application.

The relatively small form factor of the XFP module combined with an adaptable heatsink option allows host system design optimization of module location, heatsink shape/dimension/fins design, and airflow control. The module can be inserted and removed from the cage with the heat sink and clip attached.

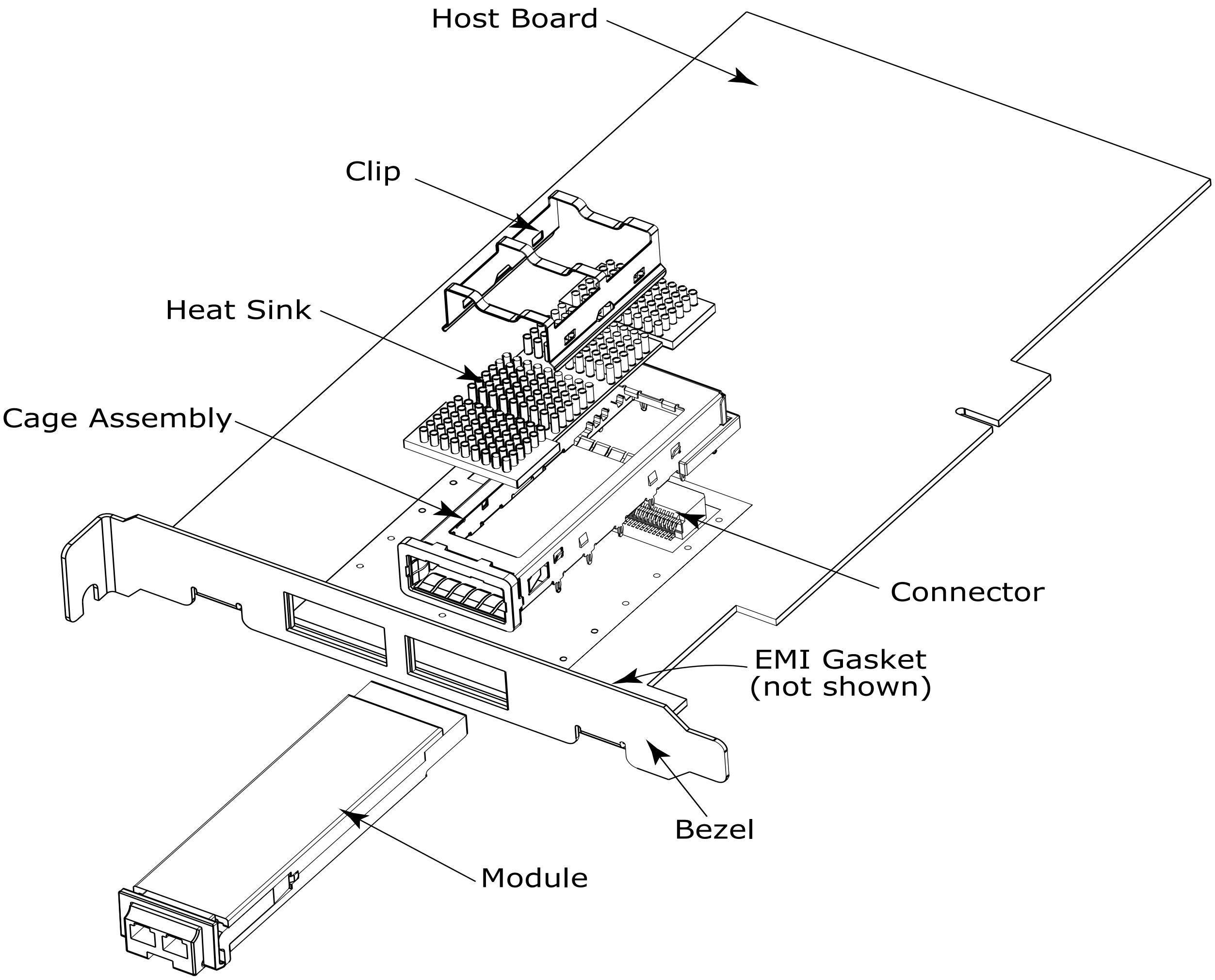


Figure 29 XFP Mechanical Components

6.2 XFP DATUMS AND COMPONENT ALIGNMENT

A listing of the datums for the various components is contained in Table 60 The alignments of some of the datums are noted. The relationship of the Transceiver, Cage, and Connector relative to the Host Board and Bezel is illustrated in Figure 30 by the location of the key datums of each of the components.

Table 60 Definition of Datums

Datum	*Description*	*Figure #*
A	Host Board Top Surface	Figure 35
B	Back surface of bezel (See Section 6.8)	Figure 37 & Figure 38
C	Distance between Connector alignment post thru holes on host board [1]	Figure 36
D	Hard stop on transceiver [2]	Figure 31
E	Width of transceiver [1]	Figure 31
F	Height of transceiver housing	Figure 31
G	Width of transceiver pc board [1]	Figure 33
H	Leading edge of transceiver pc board	Figure 33
J	Top surface of transceiver pc board	Figure 33
K	Host Board thru hole #1 to accept Connector alignment post [2]	Figure 35 & Figure 36
L	Host Board thru hole #2 to accept Connector alignment post [2]	Figure 35 & Figure 36
M	Width of bezel cut out [1]	Figure 37 & Figure 38
N	Connector alignment pin [2]	Figure 39
P	Width of inside of cage at EMI gasket (when fully compressed) [1]	Figure 41
R	Height of inside of cage at EMI gasket (when fully compressed)	Figure 41
S	Seating plane of cage on host board	Figure 41
T	Hard stop on cage [2]	Figure 41
U	Length of opening at top of cage to accept heat sink Datum Z	Figure 41
V	Length of clip	Figure 42
W	Surface of keep out area that clip contacts on heat sink	Figure 43
X & Y	Host board horizontal and depth datums established by customers' fiducials	Figure 35
Z	Length of boss on heat sink that fits inside of cage Datum U	Figure 43
AA	Width of heat sink surface that fits into clip [1]	Figure 43

1. Centerlines of datums C, E, G, M, P and AA are aligned on the same vertical axis
2. Datums D, K, L, N and T are aligned when assembled (see Figure 30)

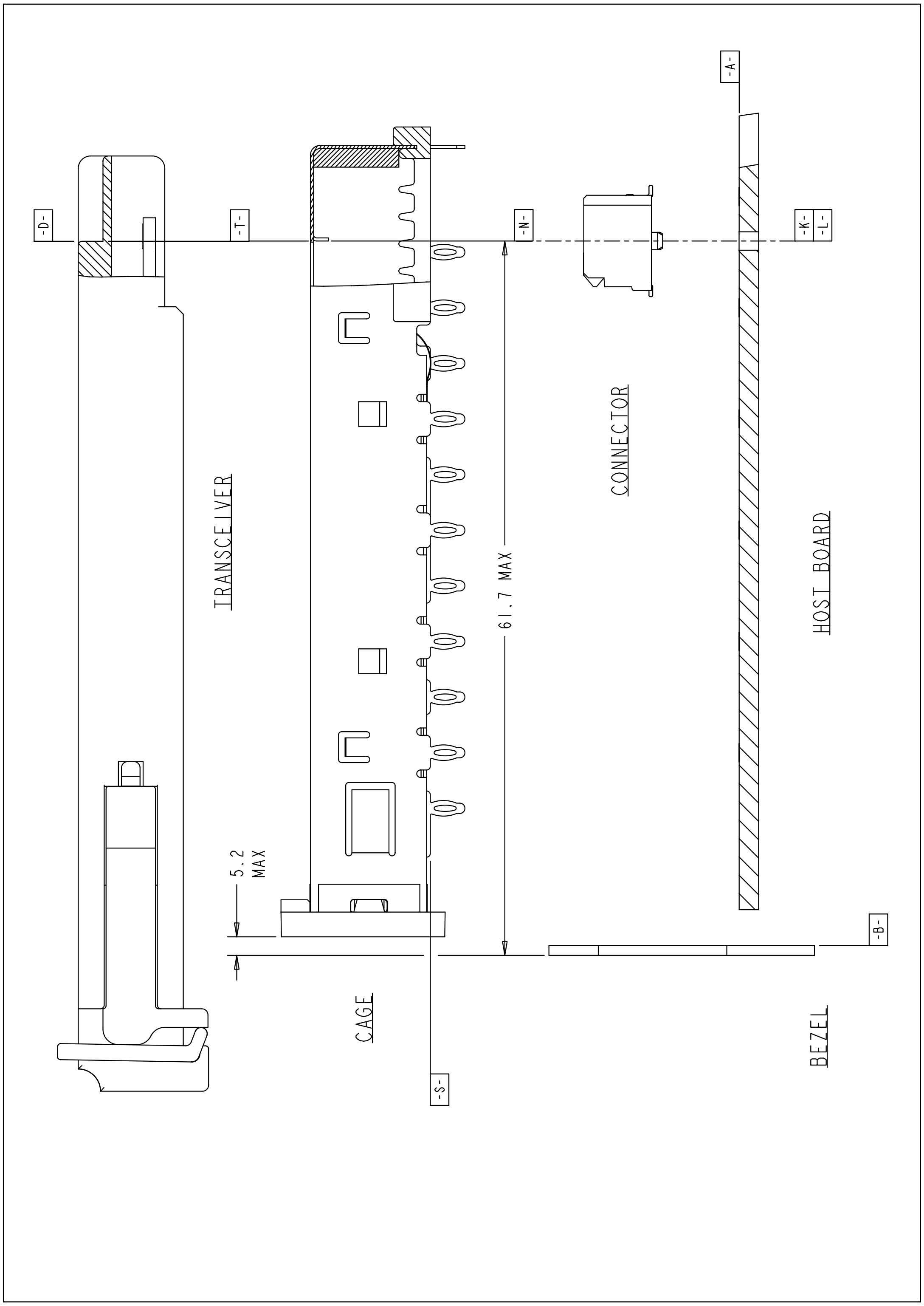
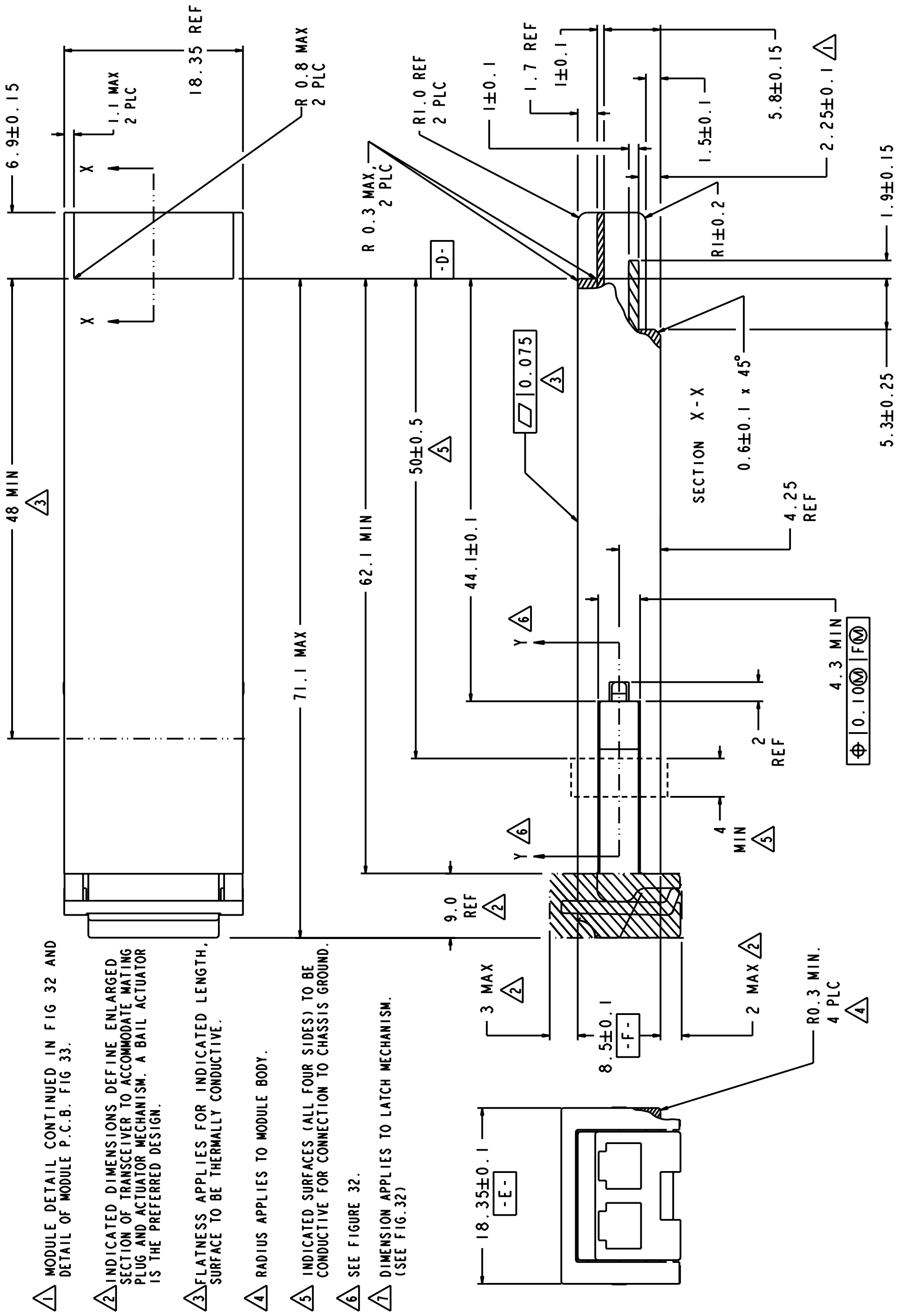


Figure 30 XFP Datum Alignment, Depth

6.3 XFP TRANSCEIVER PACKAGE DIMENSIONS

A common mechanical outline is used for all XFP transceivers. The preferred method of removing the transceiver from the cage assembly is by a bail type actuation method. The package dimensions for the XFP transceiver is defined in Figure 31 and Figure 32.



1. MODULE DETAIL CONTINUED IN FIG 32 AND DETAIL OF MODULE P.C.B. FIG 33.
2. INDICATED DIMENSIONS DEFINE ENLARGED SECTION OF TRANSCEIVER TO ACCOMMODATE MATING PLUG AND ACTUATOR MECHANISM. A BAIL ACTUATOR IS THE PREFERRED DESIGN.
3. FLATNESS APPLIES FOR INDICATED LENGTH, SURFACE TO BE THERMALLY CONDUCTIVE.
4. RADIUS APPLIES TO MODULE BODY.
5. INDICATED SURFACES (ALL FOUR SIDES) TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.
6. SEE FIGURE 32.
7. DIMENSION APPLIES TO LATCH MECHANISM. (SEE FIG.32)

Figure 31 Drawing of XFP Transceiver, Part 1

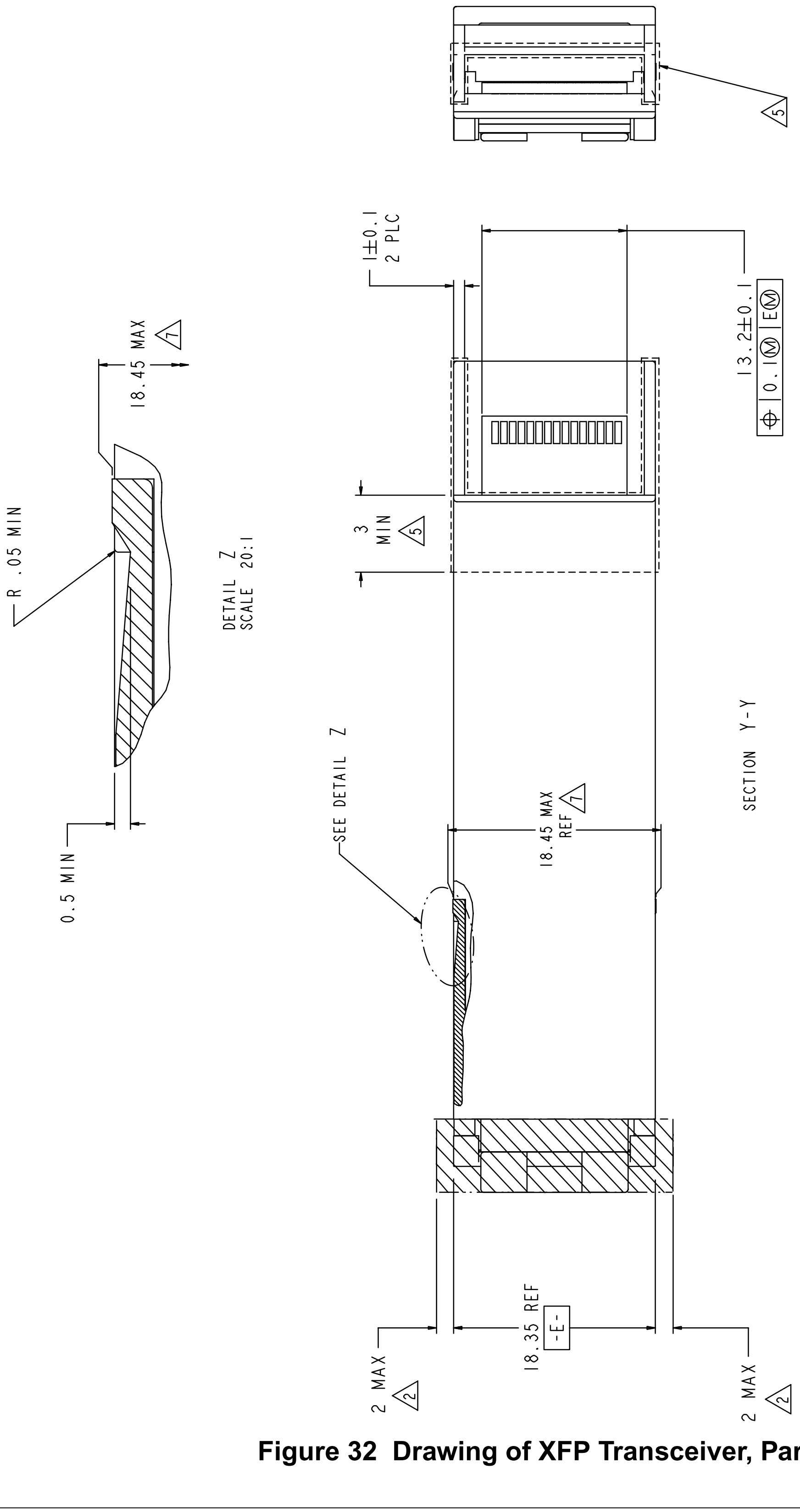


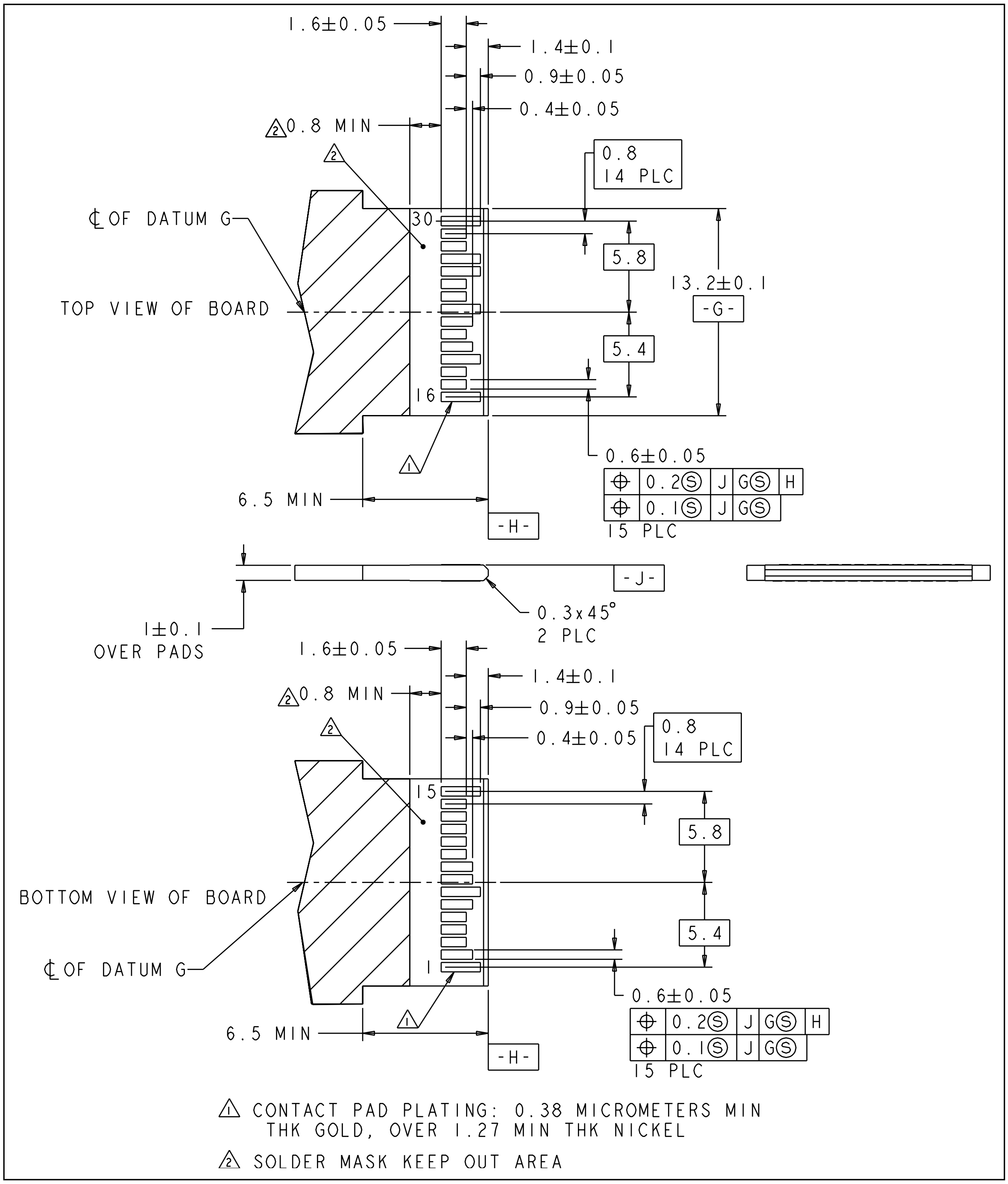
Figure 32 Drawing of XFP Transceiver, Part 2

6.4 MATING OF XFP TRANSCEIVER PCB TO XFP ELECTRICAL CONNECTOR

The XFP transceiver contains a printed circuit board that mates with the XFP electrical connector. The pads are designed for a sequenced mating:

- First mate – ground contacts
- Second mate – power contacts
- Third mate – signal contacts

The design of the mating portion of the transceiver printed circuit board is illustrated in Figure 33 and the electrical pad layout is illustrated in Figure 34. The recommended contact pad plating for the printed circuit board is 0.38 micrometers minimum gold over 1.27 micrometers minimum thick nickel.



1. CONTACT PAD PLATING: 0.38 MICROMETERS MIN THK GOLD, OVER 1.27 MIN THK NICKEL
2. SOLDER MASK KEEP OUT AREA

Figure 33 Recommended Pattern Layout for XFP Printed Circuit

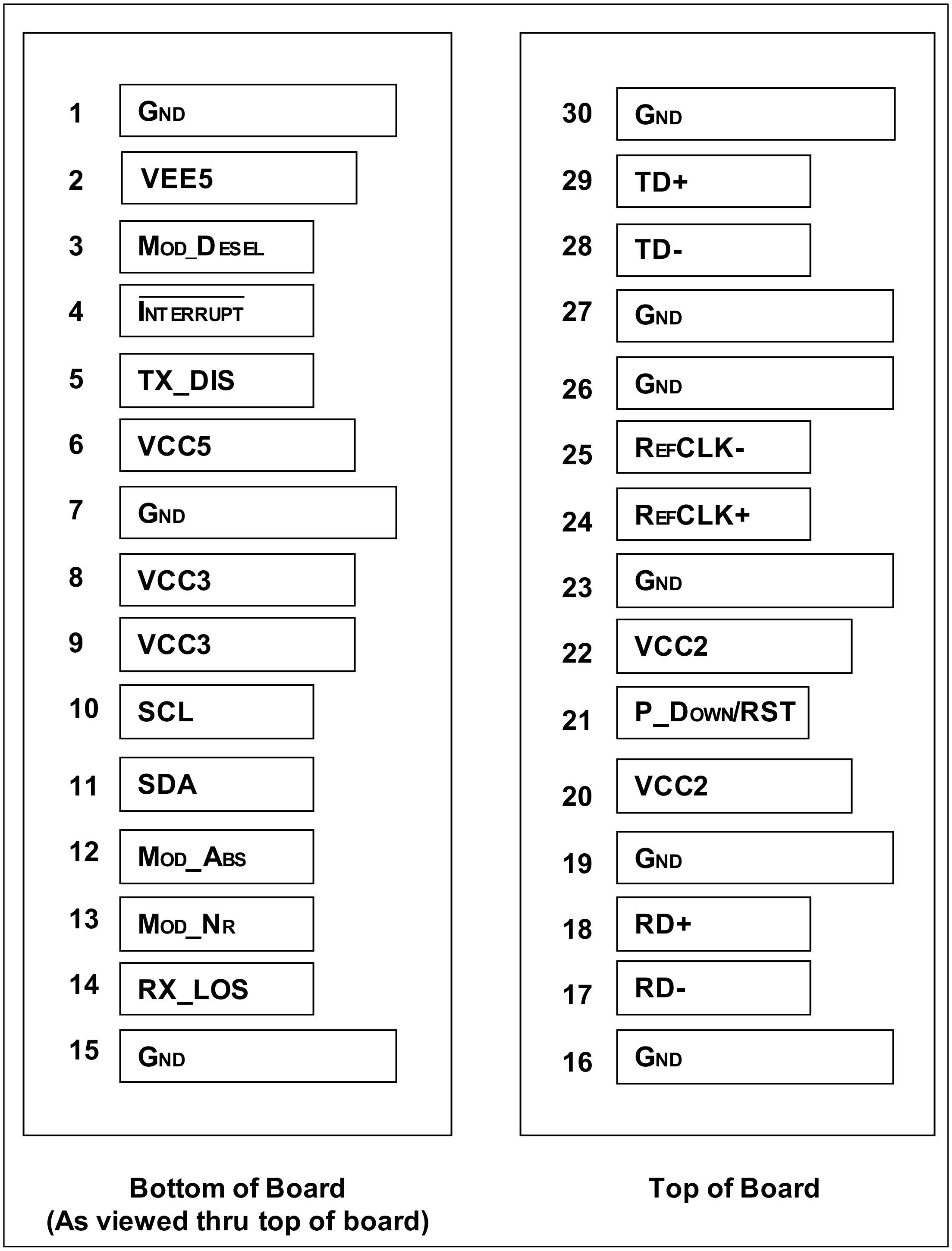
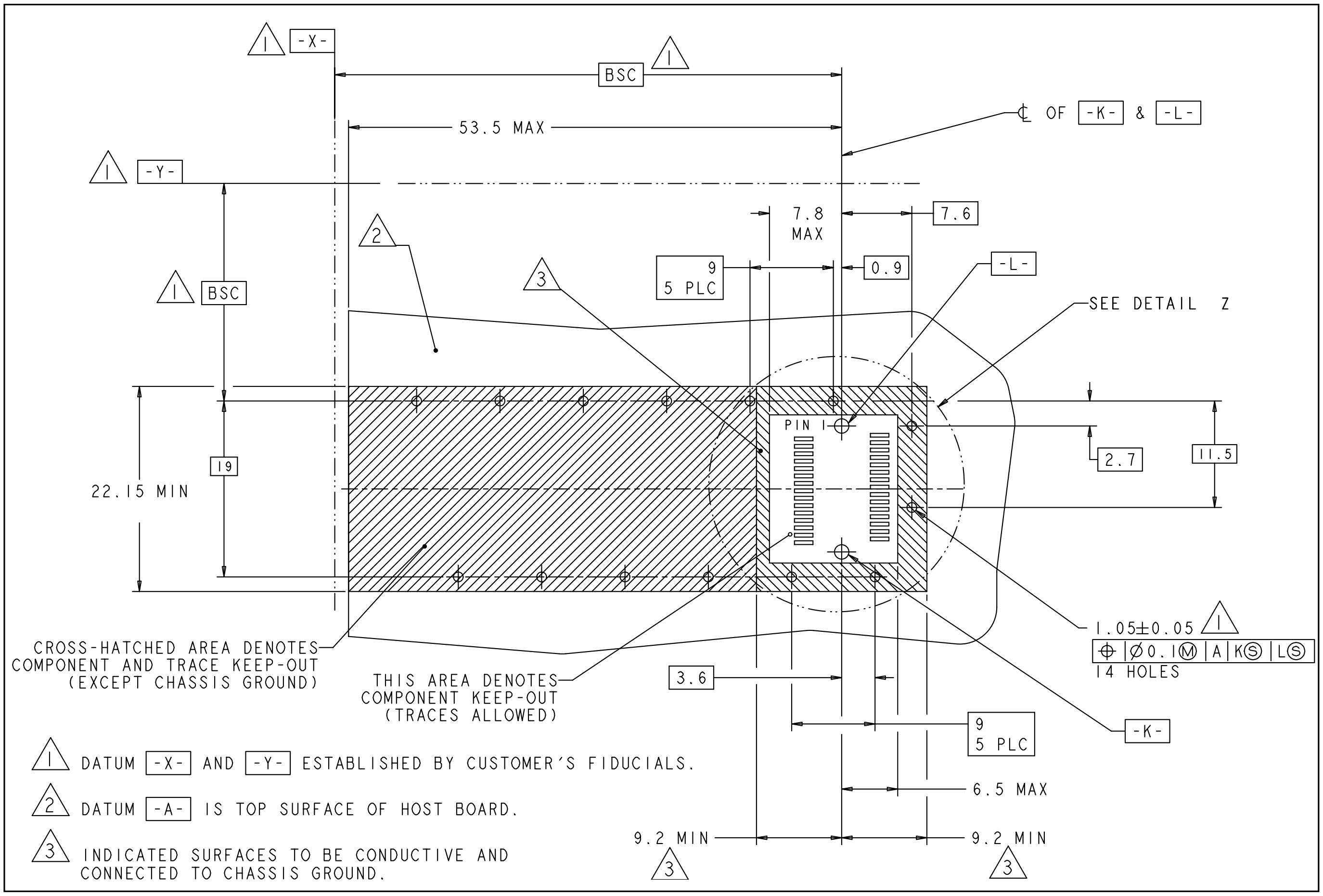


Figure 34 XFP Transceiver Electrical Pad Layout

6.5 HOST BOARD LAYOUT

Host board should be laid out in accordance with the specific connector Mfg. specifications. A typical host board mechanical layout for attaching the XFP Connector and Cage System is shown in Figure 35 and Figure 36. The location of the pattern can vary relative datums selected by the customers. Location of the pattern on the host board is application specific. See section 6.8 for further details.



1. DATUM -X- AND -Y- ESTABLISHED BY CUSTOMER'S FIDUCIALS.
2. DATUM -A- IS TOP SURFACE OF HOST BOARD.
3. INDICATED SURFACES TO BE CONDUCTIVE AND CONNECTED TO CHASSIS GROUND.

Figure 35 XFP Host Board Mechanical Layout

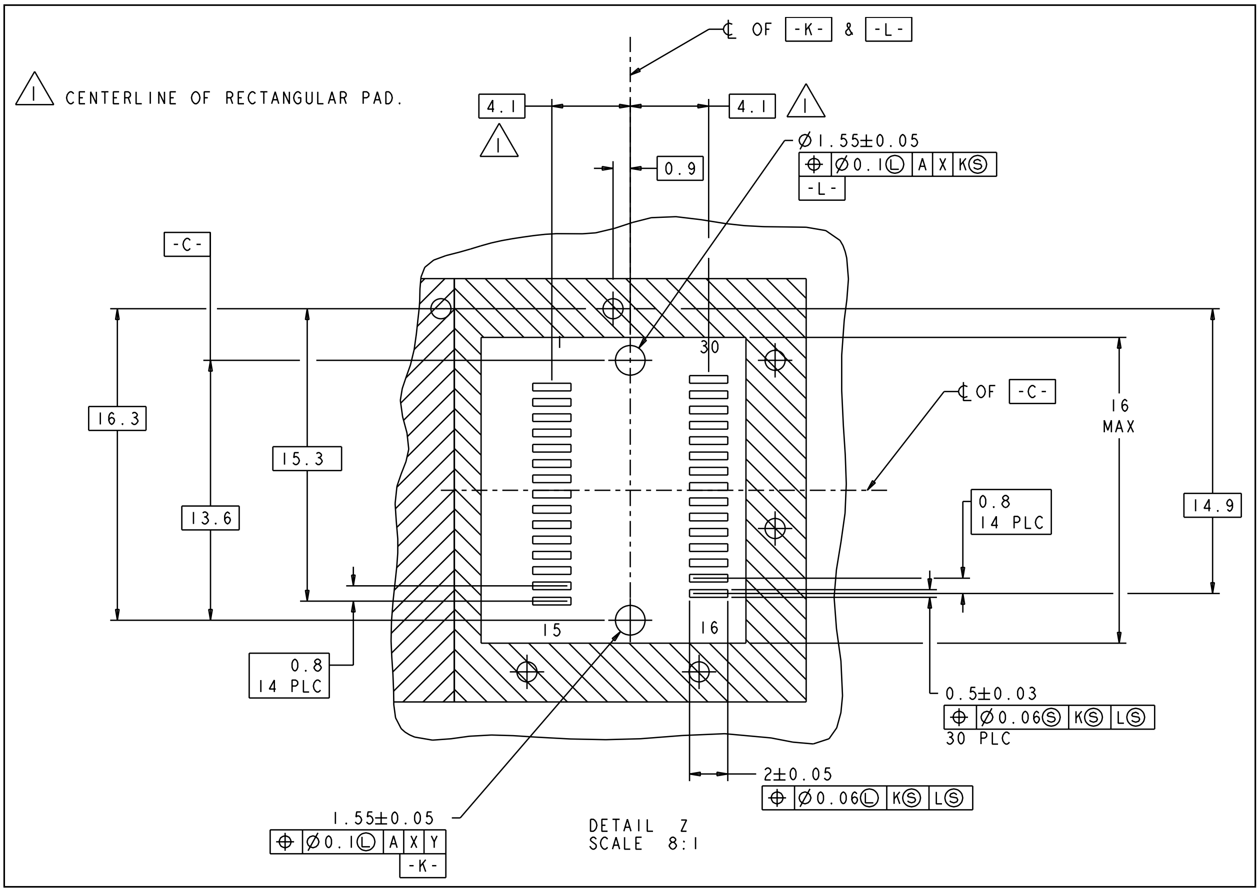


Figure 36 XFP Detail Host Board Mechanical Layout, Detail Z

6.6 Insertion, Extraction and Retention Forces for XFP Transceivers

The requirement for insertion forces, extraction forces and retention forces are specified in Table 61.

Architecture Note

The XFP cage and module design combination must ensure excessive force applied to a cable does not damage the XFP cage. If any part is damaged by excessive force, it should be the cable or the media module and not the cage which is part of the host system.

Table 61 Insertion, Extraction, and Retention Forces

Measurement	*Minimum*	*Maximum*	*Units*	*Comments*
XFP transceiver insertion	0	40	Newtons	
XFP transceiver extraction	0	30	Newtons	
XFP transceiver retention	90	N/A	Newtons	No damage to transceiver below 90N
Cage retention (Latch strength)	180	N/A	Newtons	No damage to the latch below 180N
Cage retention in Host Board	133	N/A	Newtons	Force to be applied in a vertical direction with no damage to the cage.
Insertion / removal cycles, connector/cage	100	N/A	cycles	
Insertion / removal cycles, XFP Transceiver	50	N/A	cycles	

6.7 COLOR CODING AND LABELING OF XFP TRANSCEIVERS

An exposed feature of the XFP transceiver (a feature or surface extending outside of the bezel) shall be color coded as follows:

- Beige for 850nm
- Blue for 1310nm
- White for 1550nm APD Receiver
- Red for 1550nm non-APD Receiver

Each XFP transceiver shall be clearly labeled. The complete labeling need not be visible when the XFP transceiver is installed and the bottom of the device is the recommended location of the label. Labeling shall include:

- Appropriate manufacturing and part number identification
- Appropriate regulatory compliance labeling
- A manufacturing traceability code

Also the label should include clear specification of the external port characteristics such as:

- Optical wavelength
- Required fiber characteristics
- Operating data rate
- Interface standards supported
- Link length supported.

The labeling shall not interfere with the mechanical, thermal and EMI features.

6.8 BEZEL AND EMI GASKET DESIGN FOR SYSTEMS USING XFP TRANSCEIVERS

Host enclosures that use XFP devices should provide appropriate clearances between the XFP transceivers to allow insertion and extraction without the use of special tools and a bezel enclosure with sufficient mechanical strength. For most systems a nominal centerline to centerline spacing of 23.5 mm (0.925") is sufficient. See Figure 37 and Figure 38 for the recommended bezel designs. Figure 37 illustrates the single sided mounting and Figure 38 illustrates the double sided mounting method. The minimum recommended host board thickness for double sided mounting of the assemblies is 3.0 mm minimum.

There are many options for a bezel EMI gasket that functions as a seal between the bezel and the front of the cage. The design of the bezel EMI gasket and the materials used for the gasket are application specific. The preferred method is to fasten the gasket to the back of the bezel with a pressure sensitive adhesive. Assembly of the host board to the bezel will compress the gasket to the recommended range specified by the bezel EMI gasket manufacturer. The surface in the back of the bezel that is in contact with the bezel EMI gasket must be low resistance and connected to ground.

The gasket thickness after compression can be calculated as follows:

GT = BKL - 56.3 ± 0.2mm.

Where:

- GT is gasket thickness in the compressed state.
- BKL is the distance from the back of the bezel Datum B to the centerline of Datums K & L. See Figure 35 and Figure 36 (Note: dimension from front of bezel to centerline of Datums K & L must not exceed 61.7mm, see Figure 30).
- The 56.3 ± 0.2mm dimension is the distance from the front of the cage to the hard stop, Datum T. See Figure 41.

The XFP transceiver insertion slot should be clear of nearby moldings and covers that might block convenient access to the latching mechanisms, the XFP transceiver, or the cables connected to the XFP transceiver.

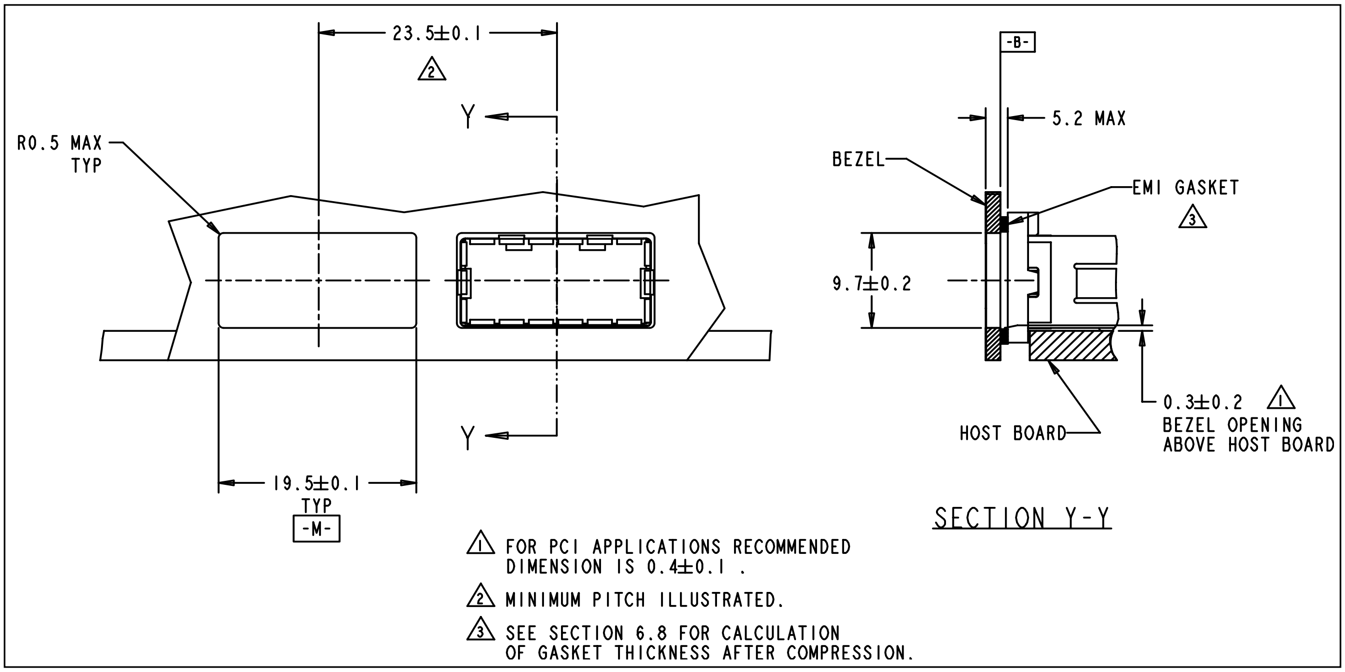


Figure 37 Recommended Single Sided Bezel Design

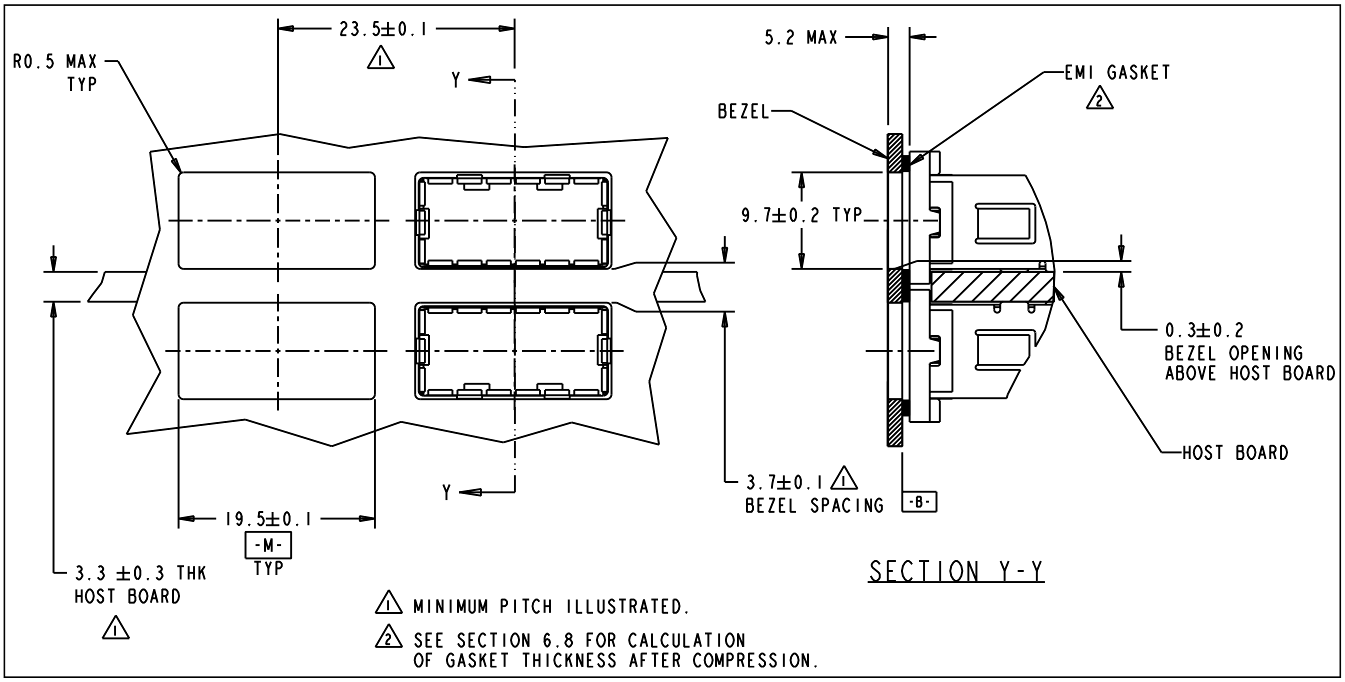


Figure 38 Recommended Double Side Mounting Bezel Design

6.9 XFP CONNECTOR MECHANICAL SPECIFICATIONS

The XFP Connector is a 30-contact, right angle surface mount connector and available from several manufacturers[1]. An example connector such as 788862-2 manufactured by Tyco is shown in Figure 39. Newer versions of this connector are available from Tyco, Molex, and Harting with improved electrical performance.

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[1] 788862C (Standard PT) and 1367500-1 (New Improved PT Version), Mfg. by Tyco Electronics, www.tycoelectronics.com.

Parecon 30 Mfg. by Harting-Electro-Optics, www.Harting-Electro-Optics.com.

74441, Mfg. by Molex Inc., www.molex.com.

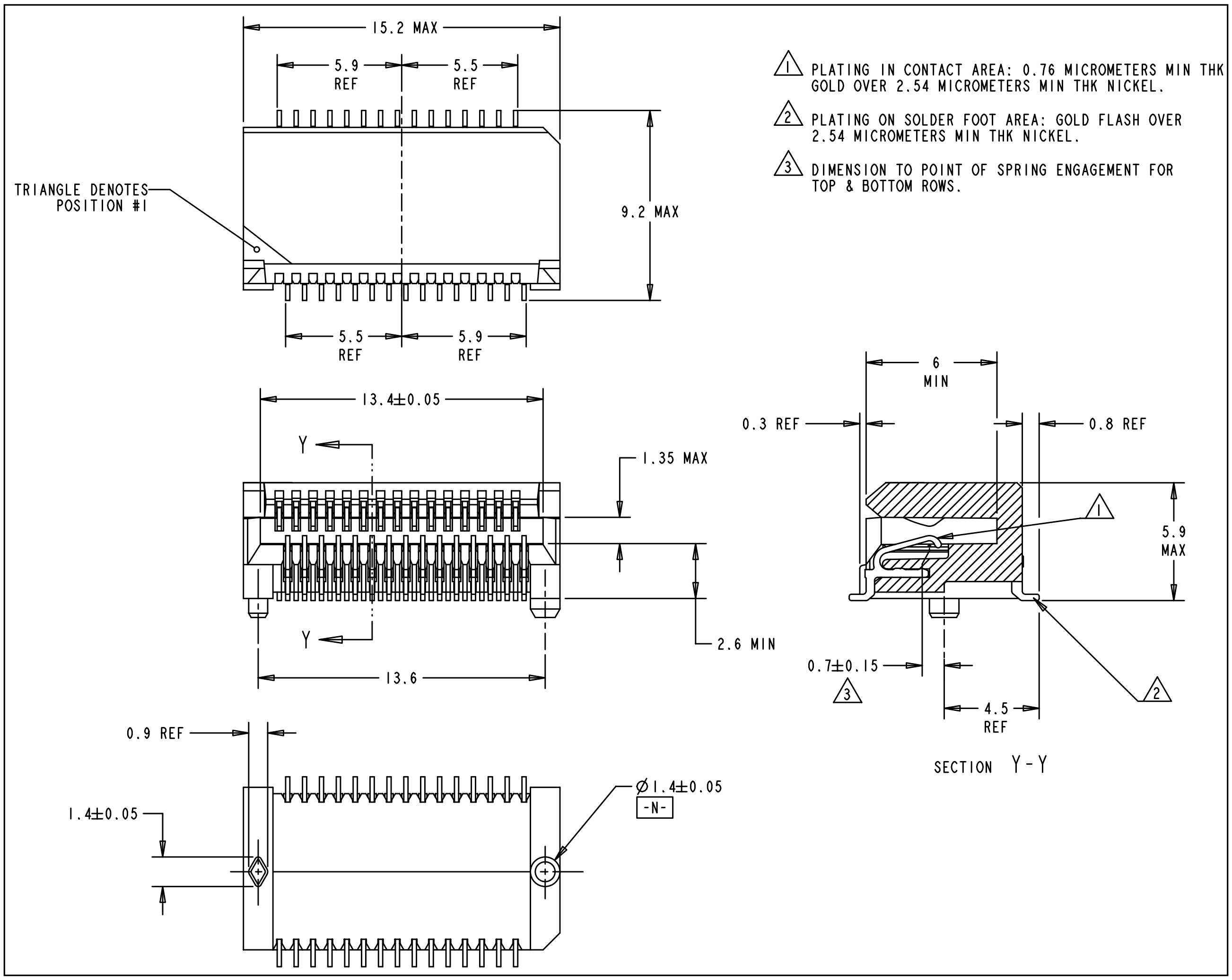

Figure 39 XFP Transceiver Connector Illustration

6.10 XFP CAGE ASSEMBLY DIMENSIONS

The Cage Assembly requires EMI shielding capability for both front and back portions of the cage along with providing guidance for the connector, retention of the transceiver and features for heat sink attachment. The location of the EMI gaskets for a reference design is illustrated in Figure 40 and a description of each EMI gasket is described in the sections below. The dimensional requirements for the cage are illustrated in Figure 41.

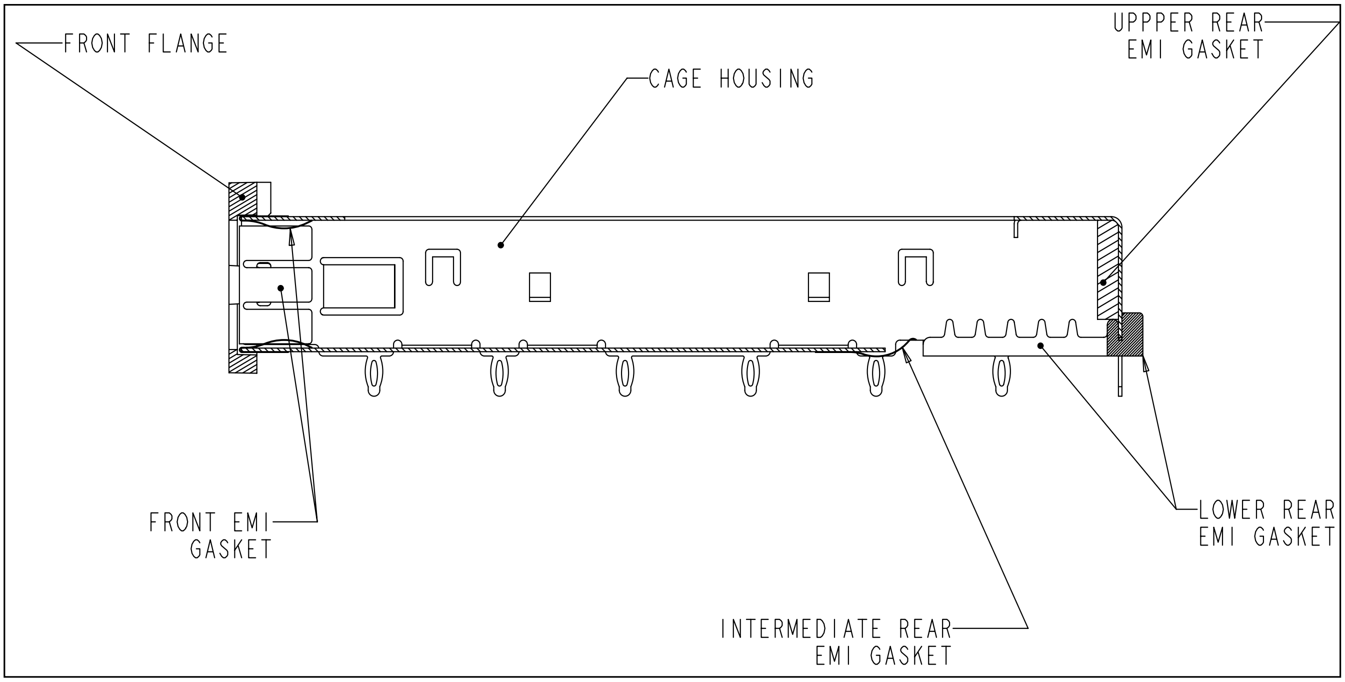

Figure 40 XFP Cage Components

6.10.1 XFP CAGE HOUSING

The metal cage has compliant leads for assembly to the host board. The cage material is copper alloy and the recommended plating options are:

- Tin-lead plate 2.54 micrometers minimum over copper flash
- Tin plate 2.54 micrometers minimum over 0.76 micrometers minimum nickel

or the equivalent materials.

6.10.2 XFP CAGE REAR EMI GASKETS

The purpose of the rear EMI Gaskets is to block any emissions that are emanating from the rear of the transceiver and carry them to chassis ground in the Host Board by directly contacting the transceiver.

6.10.2.1 XFP UPPER REAR EMI GASKET

The Upper Rear EMI Gasket is fastened to the rear inside surface of the cage with pressure sensitive adhesive. The recommended material for this gasket is conductive foam.

6.10.2.2 LOWER REAR EMI GASKET

The Lower Rear EMI Gasket is fastened to the bottom of the cage and contacts the bottom surface of the transceiver skirt. The recommended material for this gasket is a conductive elastomer.

6.10.2.3 XFP INTERMEDIATE REAR CAGE EMI GASKET (FINGER STOCK)

The Intermediate Rear EMI Gasket is fastened to the bottom of the cage and simultaneously contacts the transceiver and Host Board. The preferred design is illustrated as a series of metal springs consisting of a copper alloy material. The recommended plating options are:

- Tin-lead plate 2.54 micrometers minimum over copper flash
- Tin plate 2.54 micrometers minimum over copper flash
- or equivalent materials.

6.10.3 XFP CAGE FRONT CAGE EMI GASKET (FINGER STOCK)

The purpose of the Front EMI Gasket is to create a seal between the transceiver and the inside surface of the cage. The preferred design is illustrated as a series of metal springs that are fastened to the front of the cage and held in place by the front flange. The Front EMI Gasket material is copper alloy and the recommended plating options are:

- Tin-lead plate 2.54 micrometers minimum over copper flash
- Tin plate 2.54 micrometers minimum over copper flash
- or equivalent materials.

6.10.4 XFP FRONT FLANGE

The purpose of the front flange is to provide a flat surface to contact the Bezel EMI Gasket (customer supplied) that is mounted on the back side of the bezel. It also serves as a collar to retain the Front EMI Gasket and to provide strength to the cage housing. The front flange material is zinc alloy and the recommended plating options are:

- Tin-lead plate 2.54 micrometers minimum over copper flash
- Tin plate 2.54 micrometers minimum over 0.76 micrometers minimum nickel

or equivalent materials.

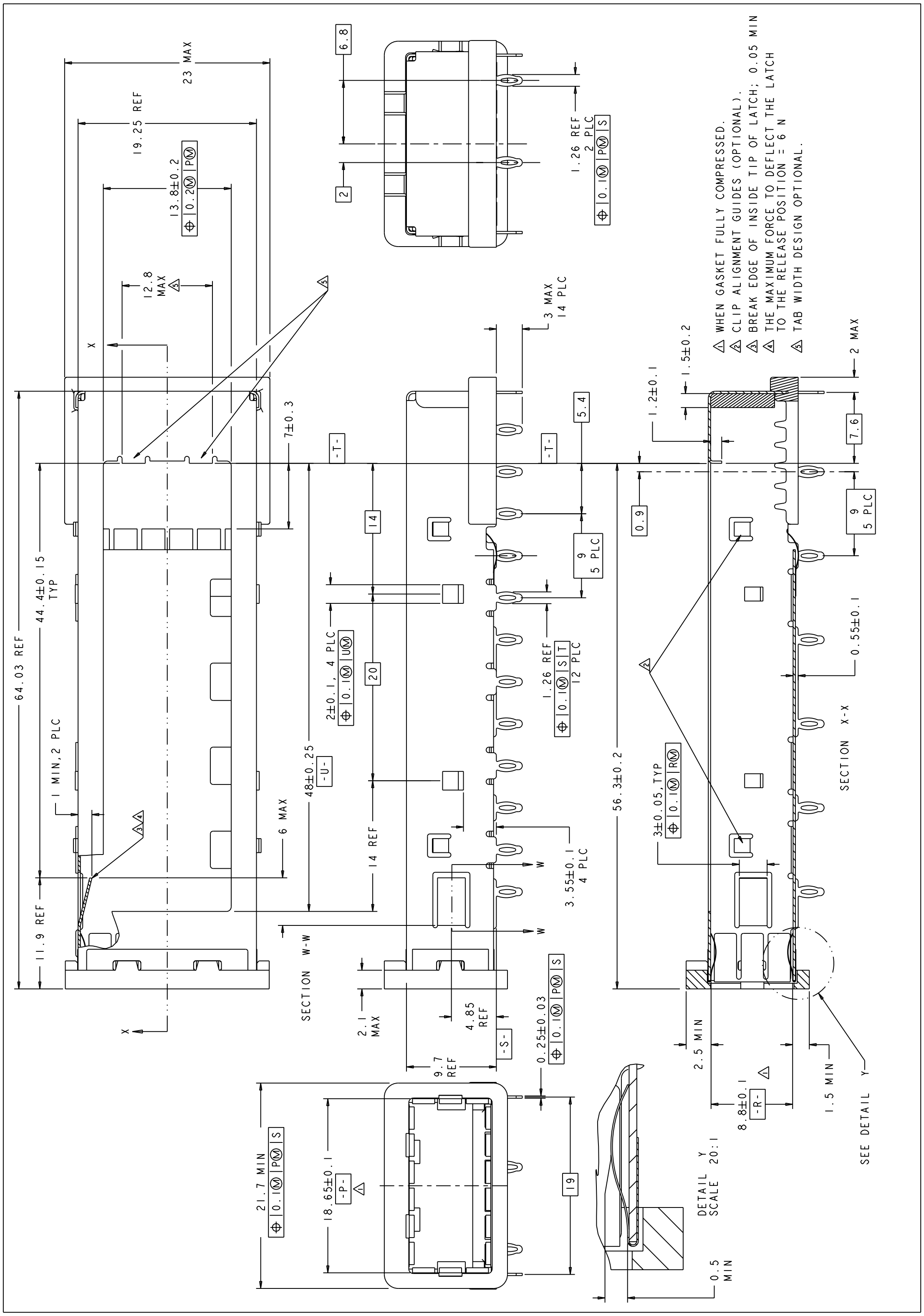

Figure 41 XFP Cage Assembly

6.11 XFP HEAT SINK CLIP DIMENSIONS

The heat sink clip is defined in Figure 42. When fastened to the cage, the clip will provide a minimum force of 5 Newtons at the interface of the heat sink and XFP transceiver. The clip is designed to permit a heat sink to be fastened to the cage and to expand slightly during transceiver insertion in order to maintain a contact force between the transceiver and heat sink.

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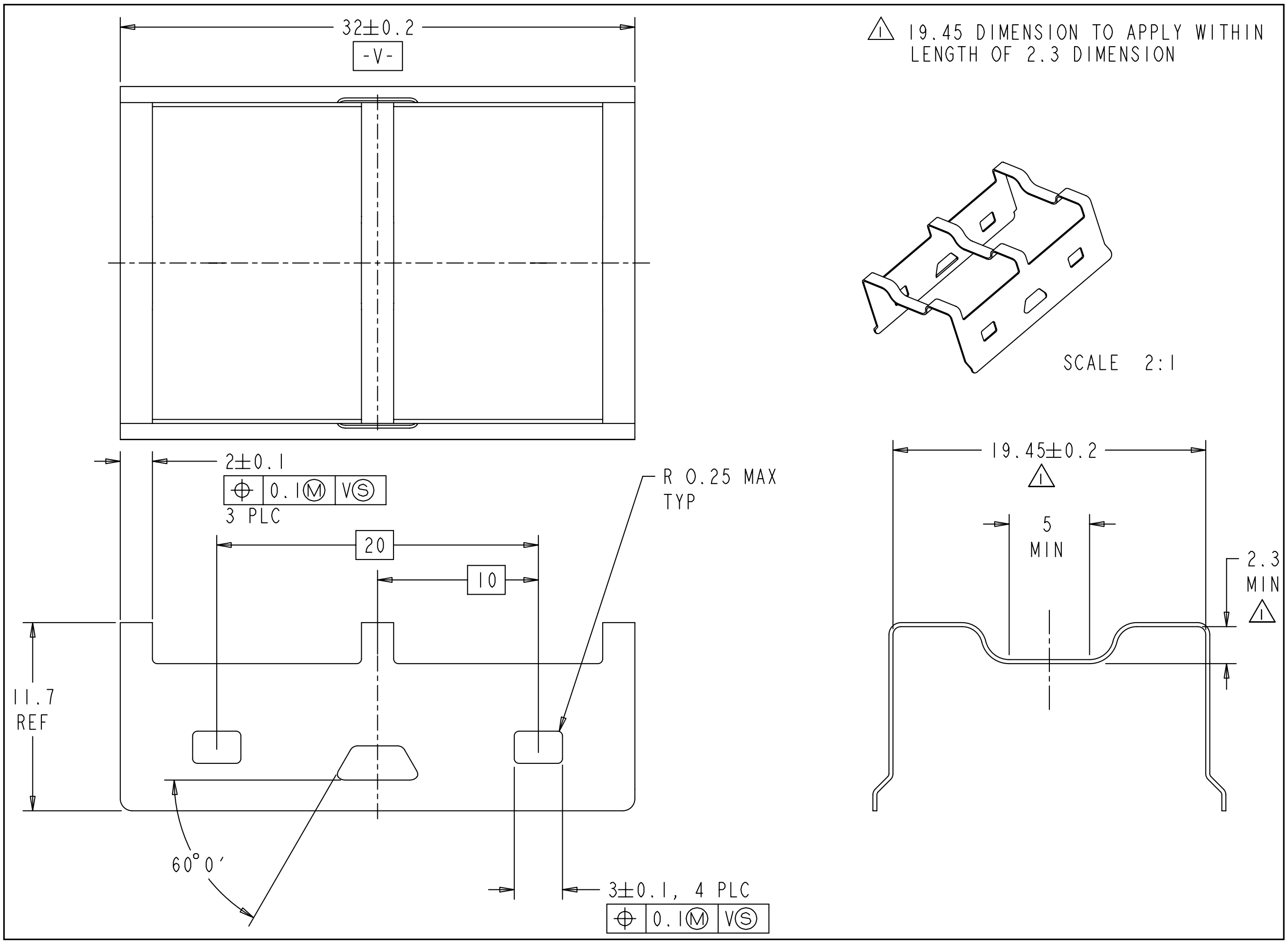

Figure 42 XFP Heat Sink Clip

6.12 An Example XFP Heat Sink

The heat sink is illustrated in Figure 43. Critical dimensions to insure that the heat sink will be compatible with the Heat Sink Clip are defined. The configuration of the fins or posts is application specific along with the outside envelope. The heat sink includes a beveled edge which “rides up” the leading edge of the transceiver as the transceiver is inserted into the cage assembly. The recommended material for the heat sink is aluminum and the surface treatment for the transceiver contacting surface can be anodizing or nickel plating.

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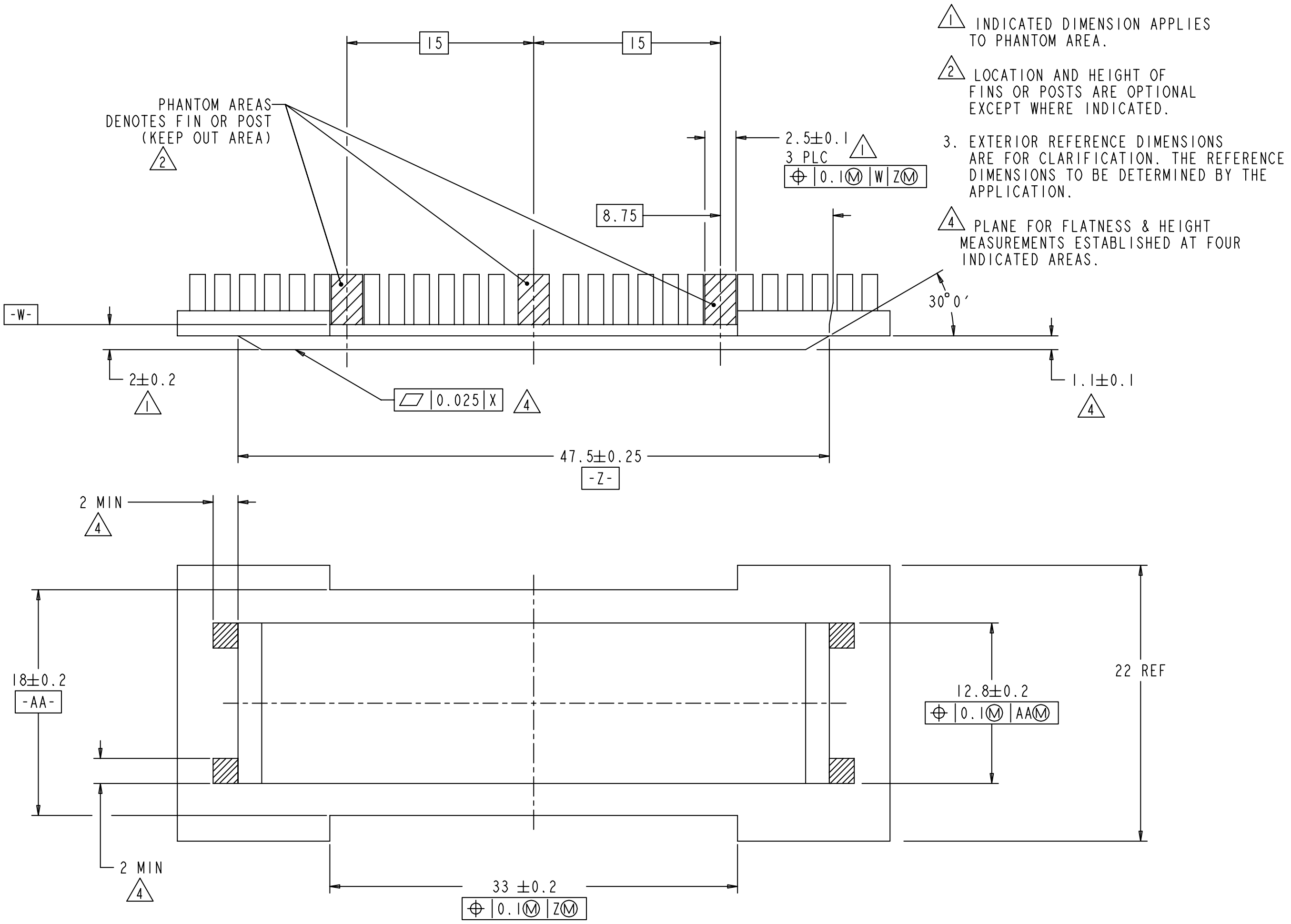


Figure 43 XFP Heat Sink

6.13 ENVIRONMENTAL AND THERMAL

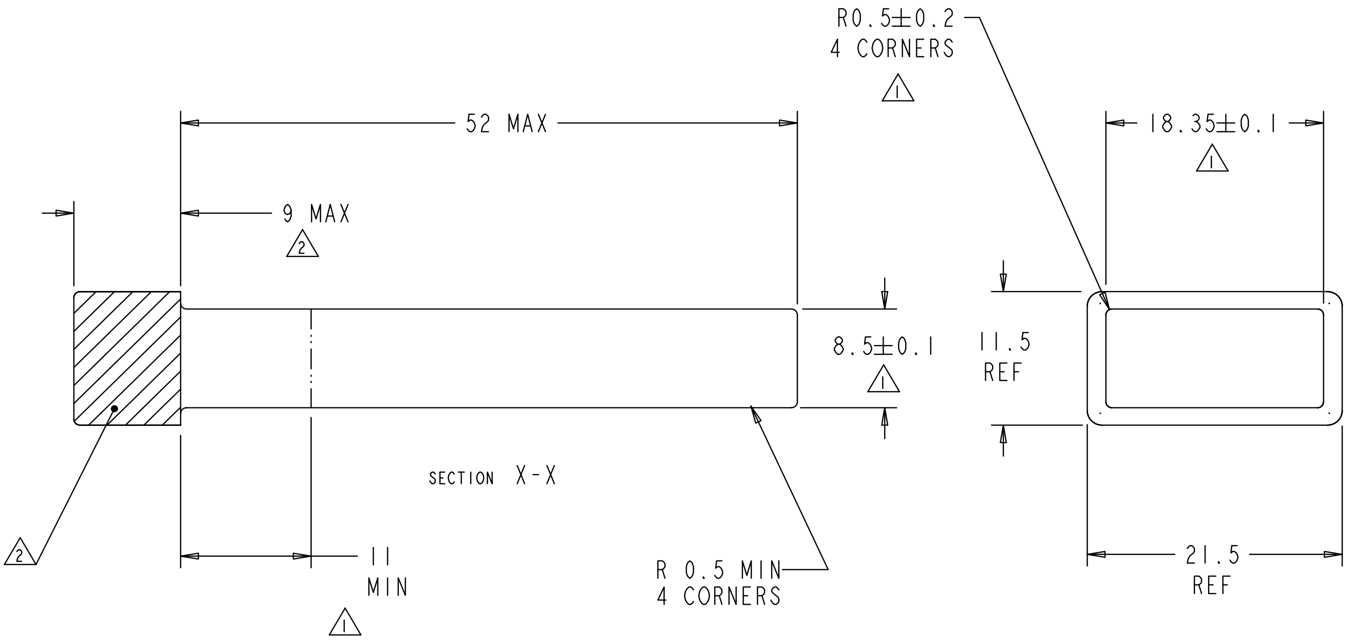
The XFP module electrical specifications shall be met at least from 0-70 degree C case temperature with an altitude range 0-3km.

The system designer is responsible for ensuring the maximum temperatures do not exceed requirements of IEC 60950 section 4.5.1 and table 4B. If case temperatures of the transceiver, cage, or heatsink exceed 70C, appropriate labeling must be attached per table 4B note 6.

See Appendix G: for recommended test parameters and guidelines used in characterization of module thermal performance.

6.14 DUST/EMI COVER

In order to prevent contamination of the internal components and to optimize EMI performance, it is recommended that a Dust/EMI Cover be inserted into cage assemblies when no transceiver is present. See Figure 44 for the recommended design. During installation, the front flange on the cover shall be seated against the front surface of the bezel to prevent dust from entering the equipment. The conductivity of the materials chosen for the Dust/EMI Cover to be sufficient to block EMI emissions.



1 DIMENSIONS APPLY FOR INDICATED LENGTH. REMAINING LENGTH MUST NOT EXCEED MAXIMUM OF SPECIFIED DIMENSIONS.

2 REMOVAL FEATURE TO BE INCORPORATED IN THIS AREA.

Figure 44 Dust/EMI Cover

APPENDIX A: APPLICATION REFERENCE MODEL

Application reference model defines a set of overlapping compliance and measurements point to validate components and system. The reference model objective are:

- Satisfy the need for interoperablity at the electrical level.
- Allow for independent validation of host board, Module, and ASIC/SerDes.

A.1 ASIC/SERDES COMPLIANCE TESTING

ASIC/SerDes transmitter and receiver are tested on a DUT board Figure 45 with minimum trace length to avoid degradation due to traces[1]. The compliance point are as the following:

- A: the ASIC/SerDes Output. The applicable measurements are:
  - Eye Mask
  - Output Jitter
  - Return Loss S22.
- D: the ASIC/SerDes Input. The applicable measurement are:
  - Input stress sensitivity
  - Jitter tolerance
  - Return Loss S11.

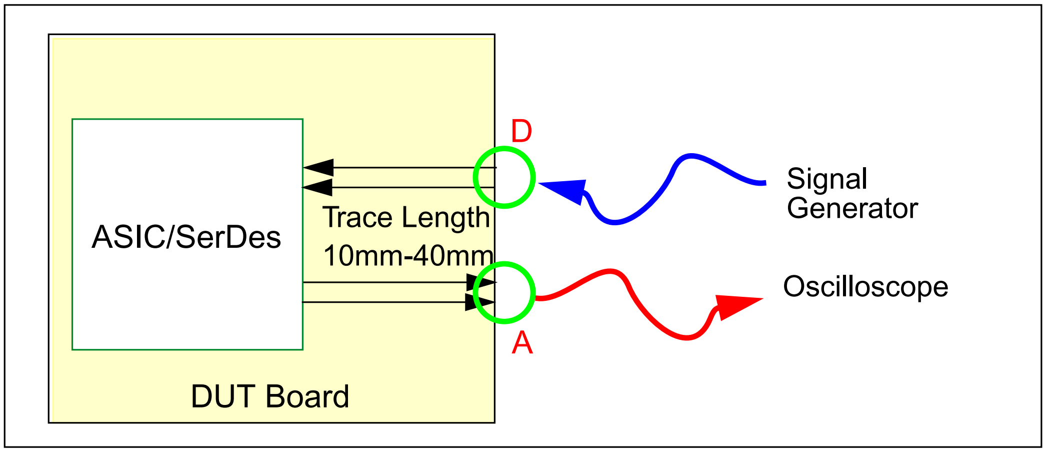


Figure 45 ASIC/SerDes Compliance Test Board

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[1] DUT board may use superior material to eliminate excess loss, but the construction should be manufacturable by standard PCB process. Trace length are recommended to be shorter than 40 mm and greater than 10mm.

A.2 HOST SYSTEM COMPLIANCE TESTING

Host system transmitter and receiver are tested by inserting a Host Test Board[1] Figure 46 in place of the XFP module. The compliance point are as the following:

- B: Host system Output. The applicable measurements are:
    - Eye Mask
    - Output Jitter
    - Return Loss S22.
- C: Host system Input. The applicable measurements are:
    - Input amplitude
    - Jitter tolerance
    - Return Loss S11.

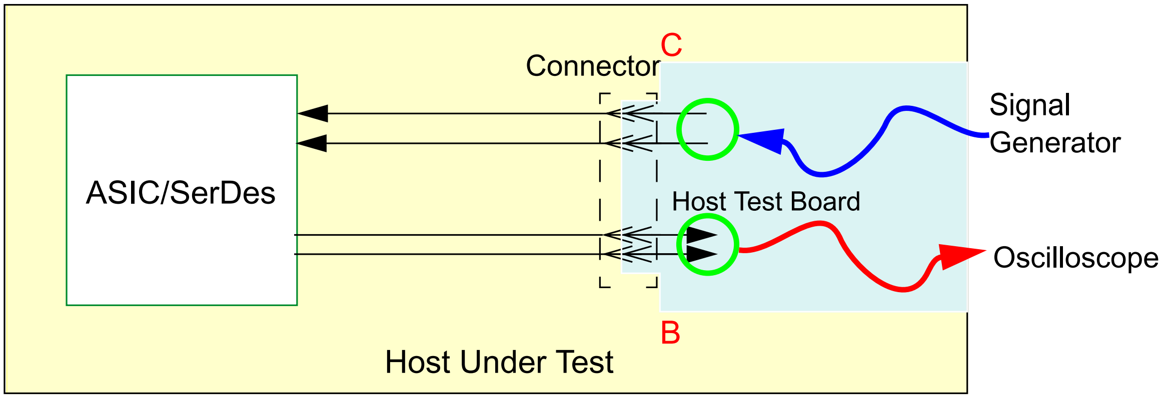


Figure 46 Host System Compliance Test Diagram

A.3 XFP MODULE COMPLIANCE TESTING

XFP modules are validated by testing them with a Module Compliance Test Board[2] Figure 47 with 30 position XFP connector. The compliance points are as the following:

- B': Host system Output. The applicable measurement are:
    - Input stress sensitivity
    - Jitter tolerance
    - Return Loss S11.

---

[1] Host Test Board is a passive or active device that can be inserted in place of the XFP module with negligible signal alteration.

[2] Module Compliance Test Board is test board with XFP 30 position connector and 10 mm-40mm of traces on low loss dielectric material.

- C: XFP module output. The applicable measurements are:
  - Eye Mask
  - Jitter output
  - Return Loss S22.

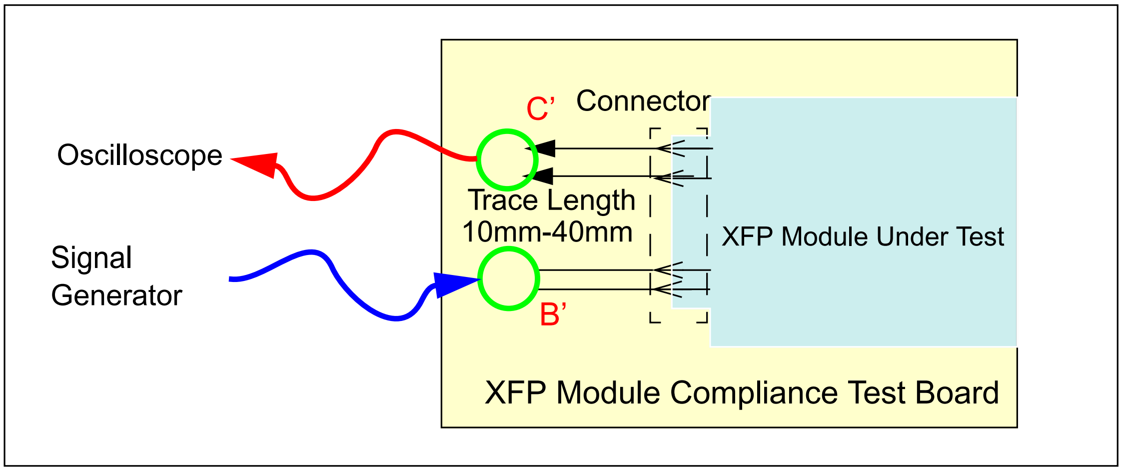


Figure 47 XFP Module Compliance Test Diagram

A.4 HOST SYSTEM COMPLIANCE TEST BOARD

Testing compliance to specifications in a high-speed system is delicate and requires thorough consideration. The measurement point must be low impedance and in many cases high impedance probing is prohibited and would result in unreliable results. Using a common Host Test Board that allows predictable, repeatable and consistent results among system vendors will help to assure consistency and true compliance in the testing of Host Systems. Host Compliance board provided courtesy of Intel Corporation.

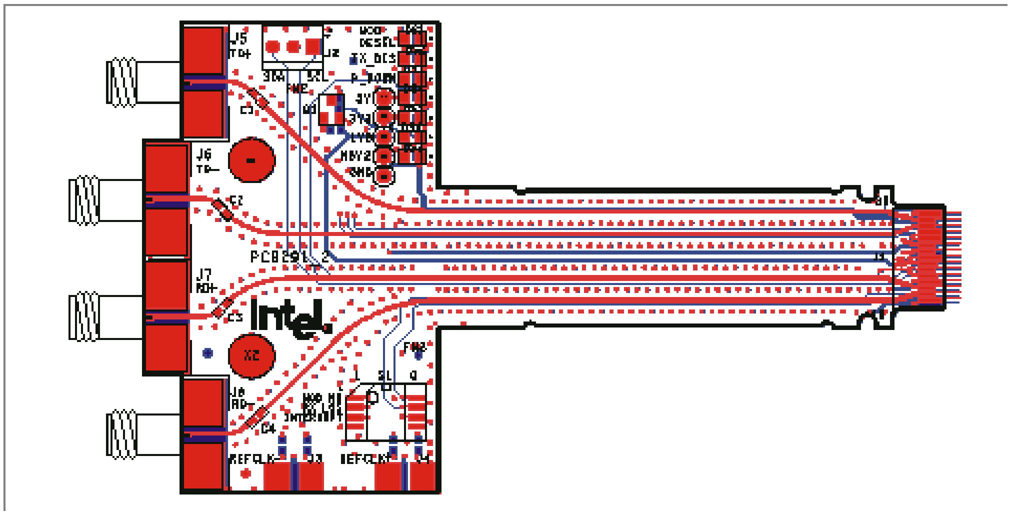


Figure 48 Host System compliance Test Board

A.4.1 HOST SYSTEM COMPLIANCE BOARD MATERIAL AND LAYER STACK-UP

Test board stack-up based on Nelco Roger3003/ FR4-6 with six layer shown below.

1. Layer	Primary Side
0.010" Rogers 3003	
2. Layer	Ground
0.006" FR4-6 Prepreg	
3. Layer	Signal 1
0.008" FR-4 Laminate	
4. Layer	Signal 2
0.006" FR4-6 Prepreg	
5. Layer	Power
0.010" Rogers 3003	
6. Layer	Secondary Side

Host System based on Roger3003 help reduce PCB loss, alternatively a short FR4-6 terminated in coaxial cable may be used.

A.4.2 HOST SYSTEM COMPLIANCE TEST BOARD PARTLIST

The host system compliance test board part list is given below.

Table 62 Host System Compliance Test Board Part List

Qty	*RefDes*	*Value*	*Description*
4	C1, C2, C3, C4, C5, C6, C7, C8	100nF	Capacitor Ceramic SMA 0603 10% 16V X7R
3	DS1, DS2, DS7		SMA LED Green
4	DS3, DS4, DS5, DS6		SMA LED Blue
1	J1		Non Component (30 Poled XFP Edge Connector)
1	J2		Molex Square Pin Header with friction lock 3 pin pitch 2.54 mm
2	J3, J4,		SMA Connector Edge SMD
4	J5, J6, J7, J8		SMA Connector Straight on RPC footprint, short center pin
1	Q1		General Purpose Silicon NPN BJT
3	R1, R2, R3	100R	Resistor SMD 0603 5%
3	R4, R7, R8	1K	Resistor SMD 0603 5%
1	R5	10R	Resistor SMD 0603 5%
1	R9	10K	Resistor SMD 0603 5%
1	S1		Dil SMD switch 4x2 pol spacing 1.27mm

A.4.3 SCHEMATIC OF HOST SYSTEM COMPLIANCE TEST BOARD

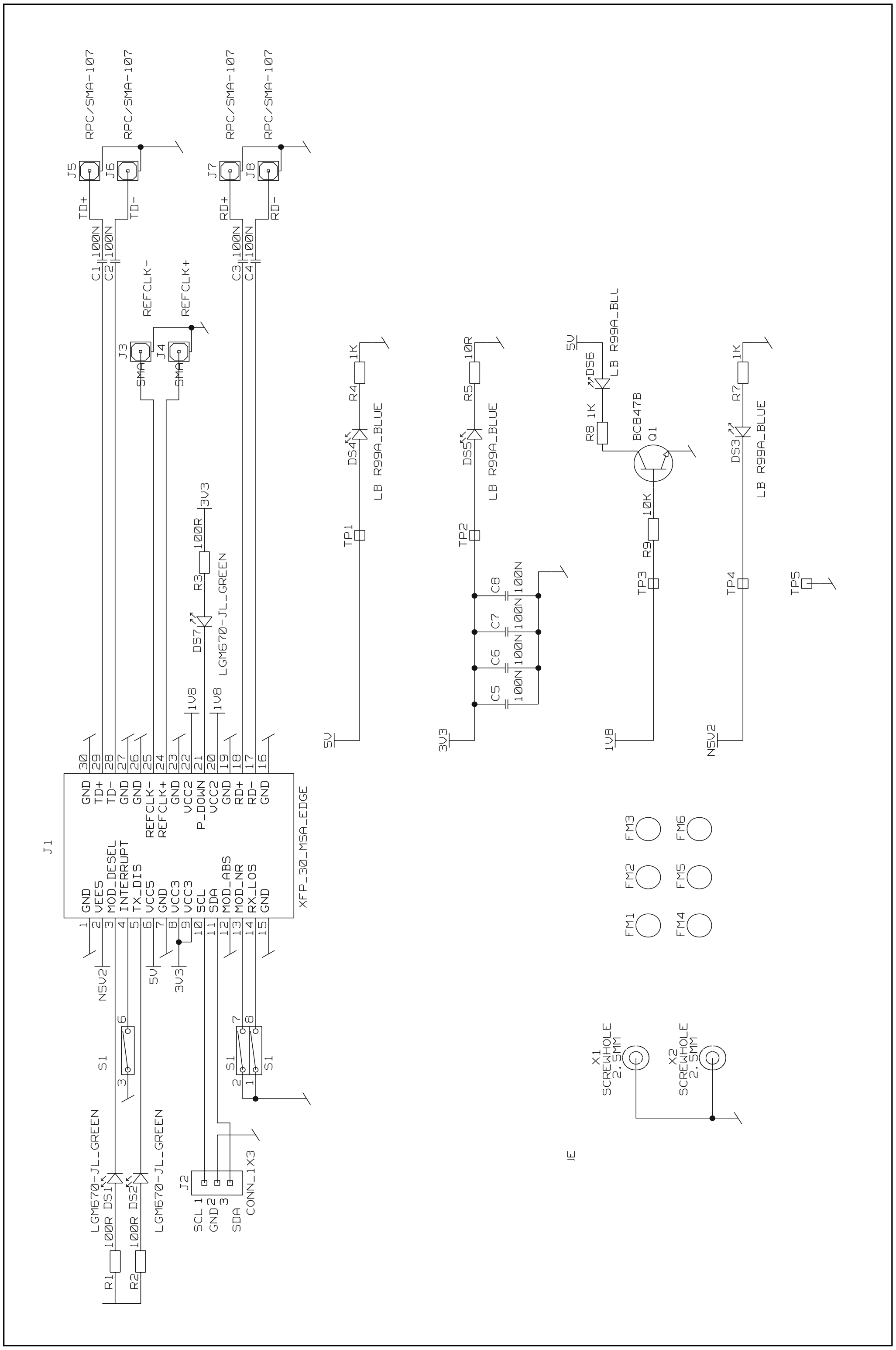


Figure 49 Schematic of Host System Compliance Test Board

A.4.4 GERBER FILE AND S PARAMETER MEASUREMENTS

Please see http://www.xfpmsa.org.

A.5 XFP MODULE COMPLIANCE TEST BOARD

The Module Compliance Test Board allows predictable, repeatable and consistent results among Module vendors and will help to assure consistency and true compliance in the testing of modules. Module Compliance Test provided courtesy of Intel Corporation.

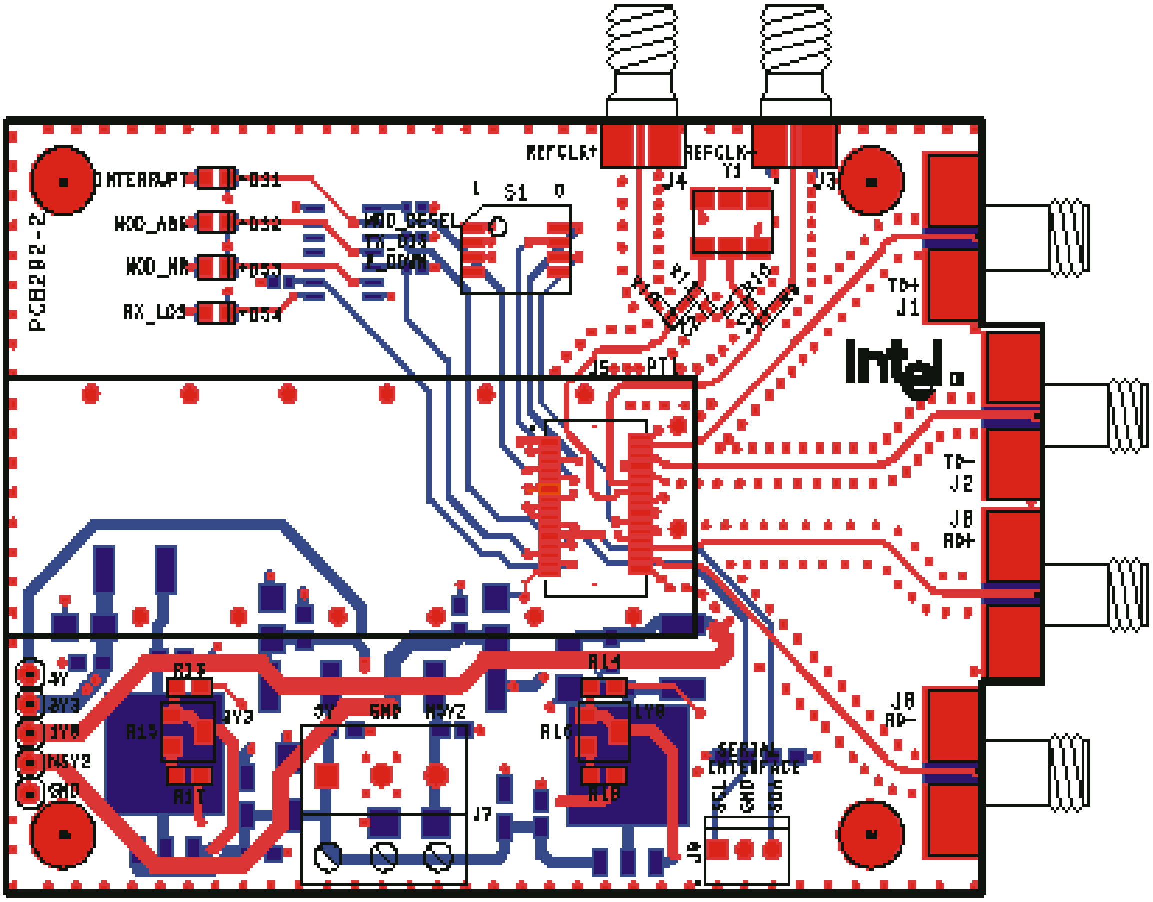


Figure 50 XFP Module Compliance test Board

A.5.1 XFP MODULE BOARD MATERIAL AND LAYER STACK-UP

XFP module compliance test board based on a four layer Rogers 3003 / FR4-6 material shown below:

1. Layer	Primary Side
0.010" Rogers 3003	
2. Layer	Ground
0.040" FR4-6 Prepreg	
3. Layer	Power
0.010" Rogers 3003	
4. Layer	Secondary side

A.5.2 XFP MODULE COMPLIANCE BOARD PARTLIST

Component part list for the XFP compliance test board is given below.

Table 63 XFP Module Compliance Test Board Part List

Qty	*RefDes*	*Value*	*Description*
4	C3, C4, C10, C14	22µF	Capacitor Tantalum SMD B 10% 10V
10	C5, C6, C7, C8, C9, C11, C12,	100 nF	Capacitor Ceramic SMA 0603 10% 16V X7R
2	C16, C17	2.2µF	Capacitor Tantalum SMD B 10% 10V
2	CR1, CR2		General Purpose Silicon Rectifier SMD Diode
3	DS1, DS2, DS3, DS4		SMA LED RED
4	J1, J2, J6, J8		SMA Connector Straight on RPC footprint, short center pin
2	J3, J4,		SMA Connector Edge SMD
1	J6		30 Pos XFP Right Angle SMD Host Connector with 0.8 mm Pitch
1	J7		Terminal Block PCB 3 Way
1	J9		Molex Square Pin Header with friction lock 3 pin pitch 2.54 mm pin
4	L1, L2, L3, L4	4.7µF	Inductor SMD 2220 4.7 µH 10%
1	PT1		XFP Cage for 30 Position PT Connector
4	R1, R3, R5, R6	10K	Resistor SMD 0603 5%
2	R9, R12	0R	Resistor SMD 0603 5%
1	R13	560R	Resistor SMD 0603 5%
1	R14	150R	Resistor SMD 0603 5%
2	R15, R16	100R	Resistor SMD 0603 5%
2	R17, R18	300R	Resistor SMD 0603 5%
2	R19, R20	10K	Resistor SMD 0603 5%
4	R2, R4, R7, R8	100R	Resistor SMD 0603 5%
5	TP1, TP2, TP3, TP4, TP5		Test pin 1mm Black
1	U1		74HCT04 Hex Inverting Gates SMD
2	U2, U3		1.5A Low Dropout Positive Regulator SMD
1	S1		Dil SMD switch 4x2 pol spacing 1.27mm
Optional Components			
2	C1, C2	100nF	Capacitor Ceramic SMA 0603 10% 16V X7R
2	R10, R11	330R	Resistor SMD 0603 5%
1	Y1		155.52 Crystal Oscillator (XO) Small SMD

A.5.3 SCHEMATIC OF THE XFP COMPLIANCE TEST BOARD

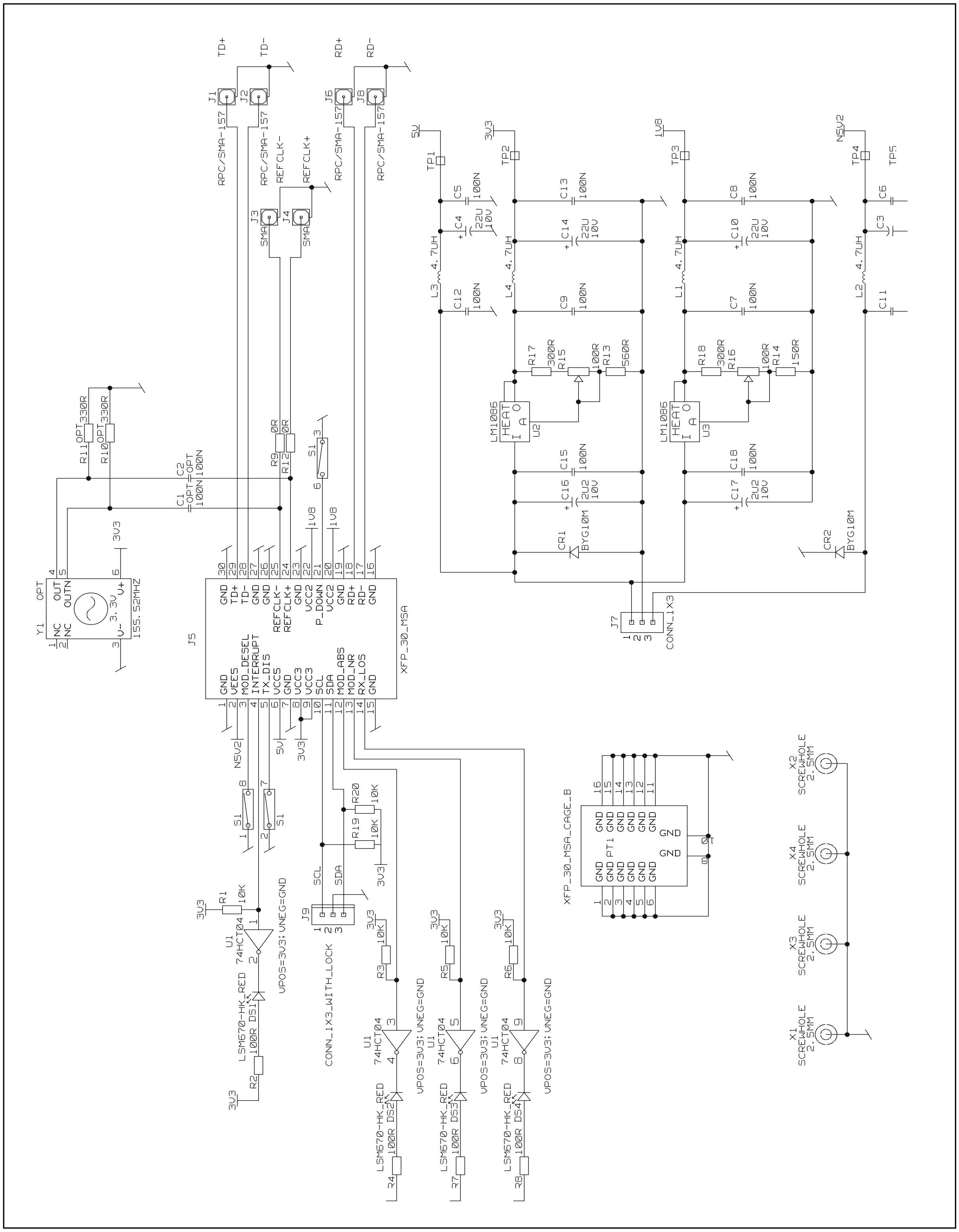


Figure 51 Schematic of the XFP Compliance Test Board

A.5.4 GERBER FILES AND MEASURED S-PARAMETERS

Please see http://WWW.xfpmsa.org.

APPENDIX B: XFI CHANNEL MEASUREMENTS AND MODELING

B.1 SYSTEM OVERVIEW

This Appendix provides design guidelines for the high-speed electrical interfaces found in XFP applications. A fundamental feature of the XFP specification is that the electrical transceiver ASIC is positioned on the system (Host) printed circuit board (PCB) rather than within the optical transceiver module. Figure 52 depicts a typical system block diagram of an end-to-end electrical channel for XFP applications. The block diagram includes a transceiver board that exists within the XFP module, a 30-pin hot swappable connector, a host board, and a BGA package. Although most host board designers will not have any direct control over the transceiver ASIC BGA package, it is nevertheless important to mention that the package can be simulated, designed, and included in channel simulations at 10Gb/s speeds.

Simulations and measurements of this electrical channel are discussed to provide guidelines on XFI design. Broadcom Corporation provided the transceiver board, host board, and electrical measurements; ASAT provided the BGA package model; Ansoft Corporation performed simulations.

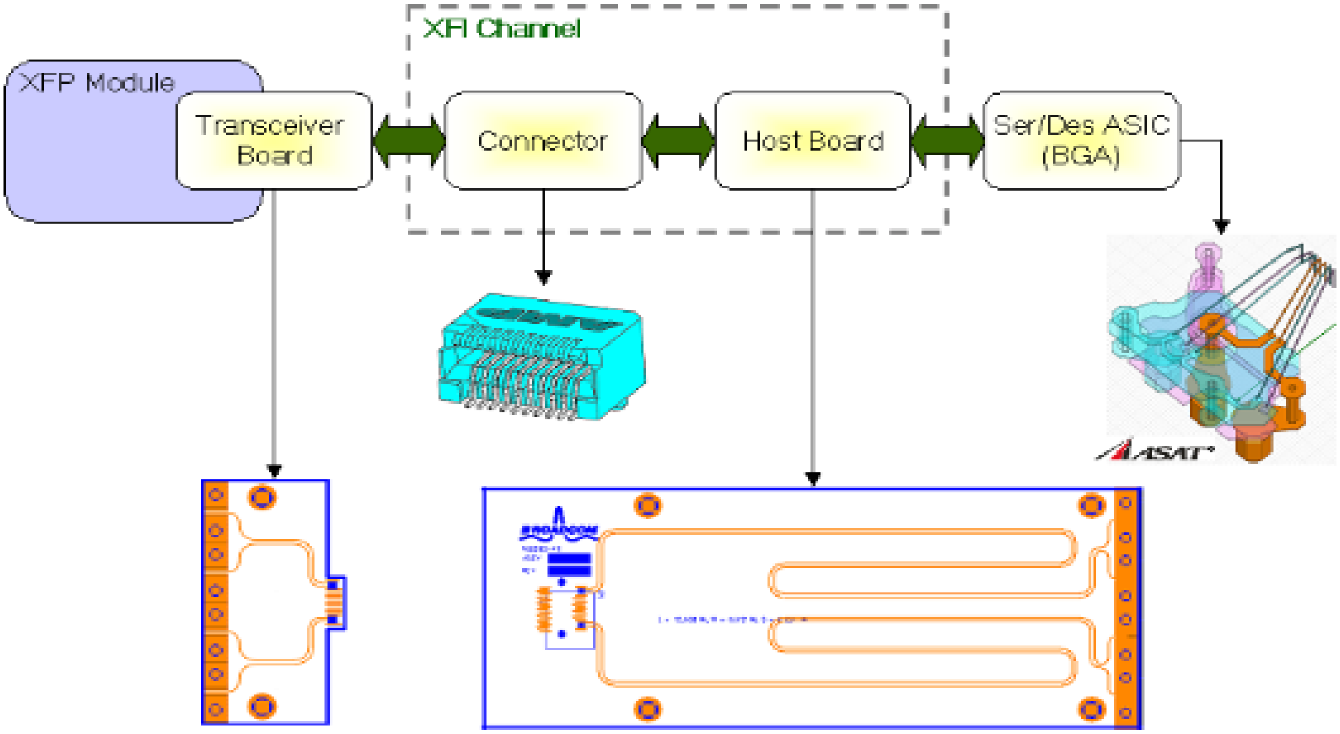


Figure 52 XFI Electrical Channel Definition

Figure 53 depicts the stack up for the Broadcom reference board. Total board thickness is 36mils and the board material is Nelco FR4-13 with εr = 4.0 and a loss tangent of 0.016. All traces are 1/2 oz. copper.

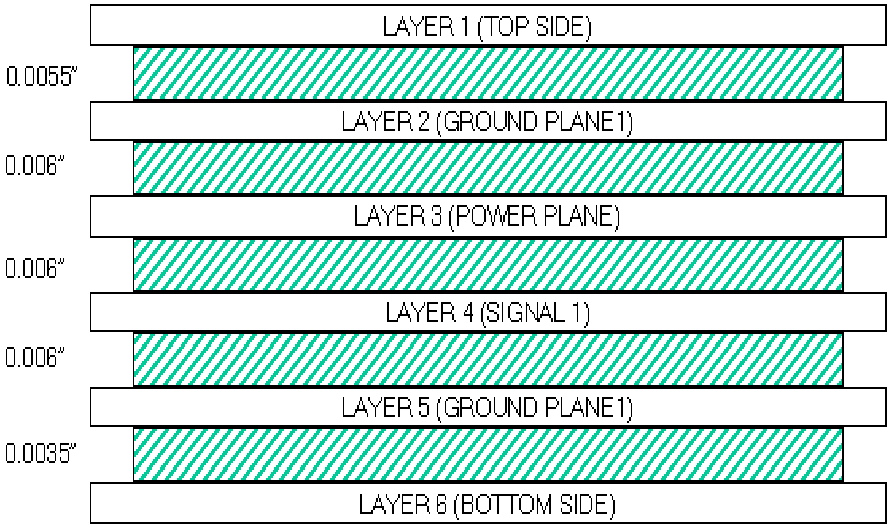


Figure 53 PCB Board Stack up

B.2 DESIGN GUIDELINE

- Keep differential pair traces on the same side of the PCB to minimize impedance discontinuities.
- When routing differential pairs, keep the trace length identical between the two traces. Differences in trace lengths translate directly into signal skew and can give rise to common mode reflections.
- Eliminate/reduce stub lengths of traces and vias.
- Reduce, if not eliminate, vias to minimize impedance discontinuities. Remember that vias and their clearance holes in the power/ground planes can cause impedance discontinuities in nearby signals. Keep vias away from traces by 10 times the trace width if possible, 2.5 times as a minimum.
- Use rounded corners rather than 90 or 45-degree corners.
- Keep signal traces far from other signals that might couple noise into the signals. A good rule of thumb is that “far” means ten times the width of the trace.
- Do not route digital signals from other circuits across the area of the transmitter and receiver.
- Do not cut up the power or ground planes in an effort to steer current paths. This usually produces more noise, not less. Furthermore, place vias and clearances so as to maintain the integrity of the plane. Groups of vias spaced closely together often overlap clearances that can form a large hole in the plane. Return currents are forced around the holes, increasing loop area and therefore, EMI emissions.
-

B.3 USING SYSTEM SIMULATION FOR CHANNEL MODELING

Figure 54 depicts the system simulator model for the XFP channel of Figure 52 including the transceiver board traces, the Tyco connector, and the host board traces. S-parameter models that were computed from the circuit and electromagnetic simulations are cascaded to allow evaluation of end-to-end system performance.

Figure 55 and Figure 56 contain comparisons of the simulated and measured differential s-parameters for SDD11 and SDD21, respectively. Although differences between the simulated and measured are observed (especially for SDD11), it is clear that the simulations have accurately depicted the trends for the overall system response.

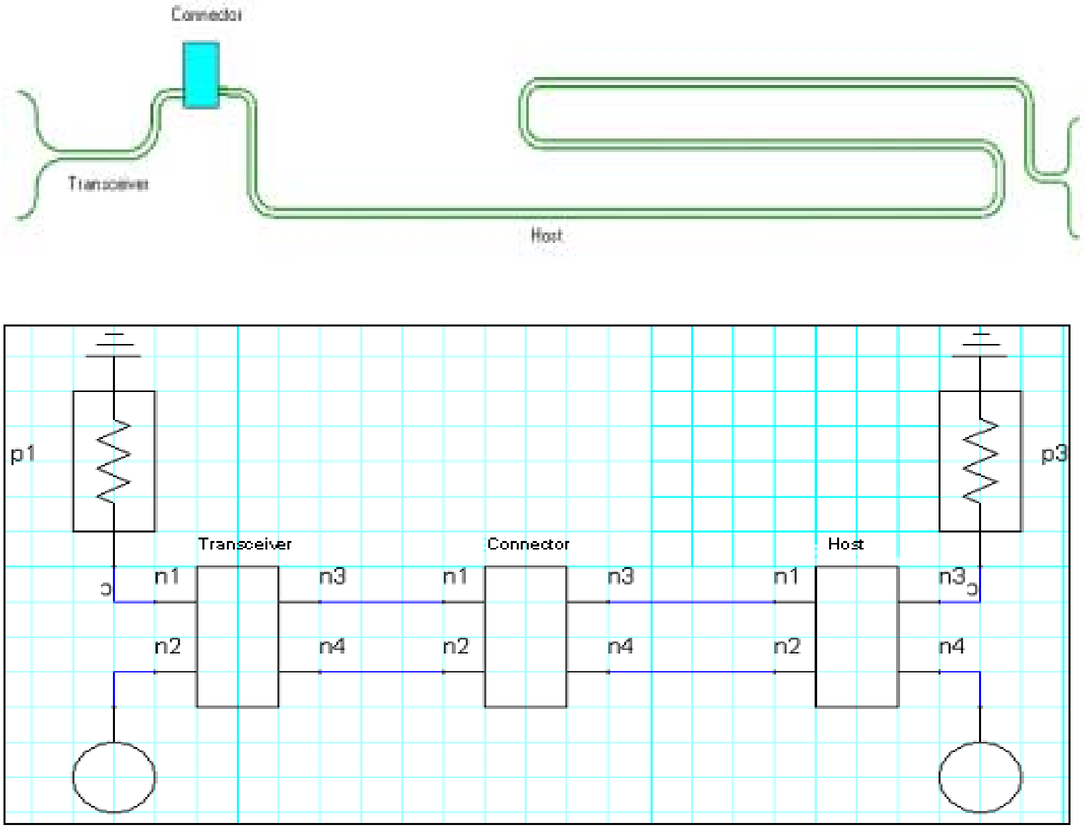


Figure 54 System model for the XFI Channel.

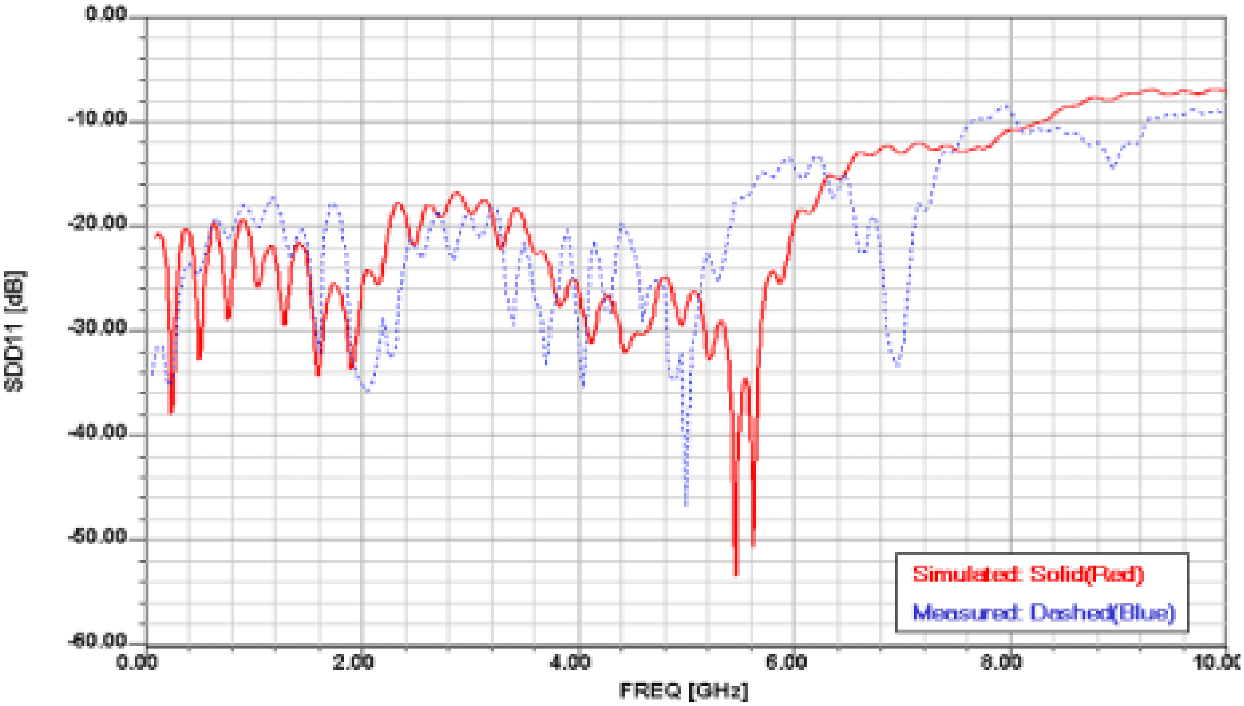


Figure 55 Comparison of simulated and measured differential s_{11}

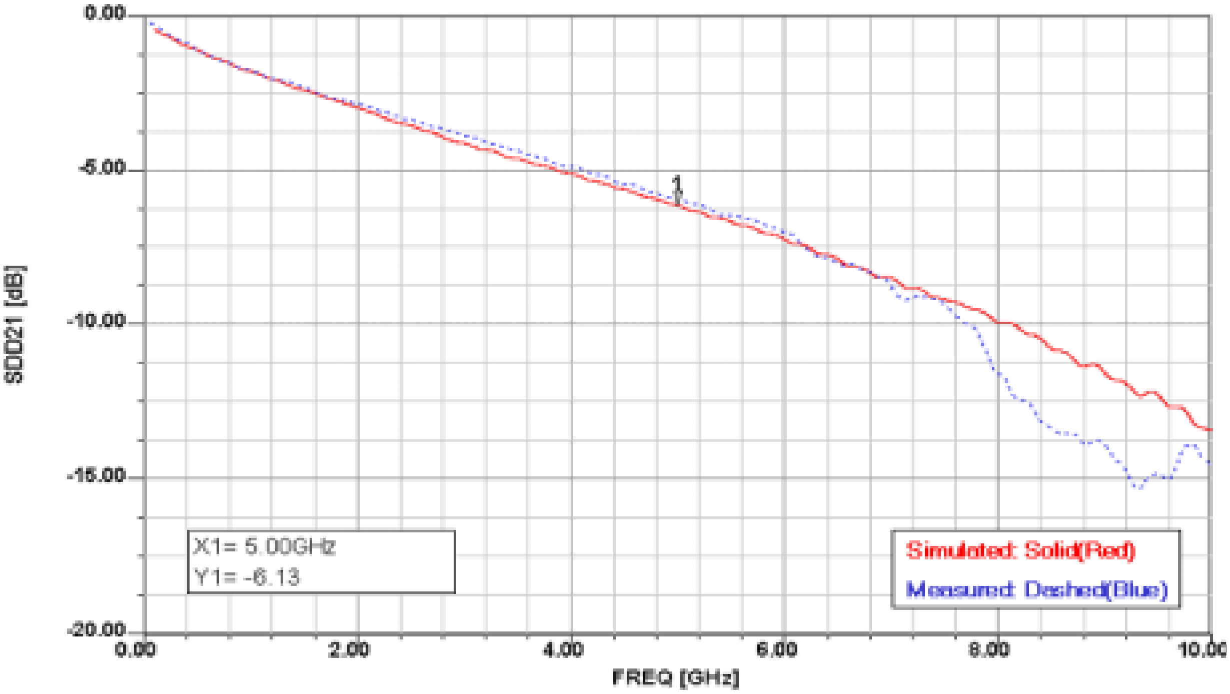


Figure 56 Comparison of simulated and measured differential s_{21}

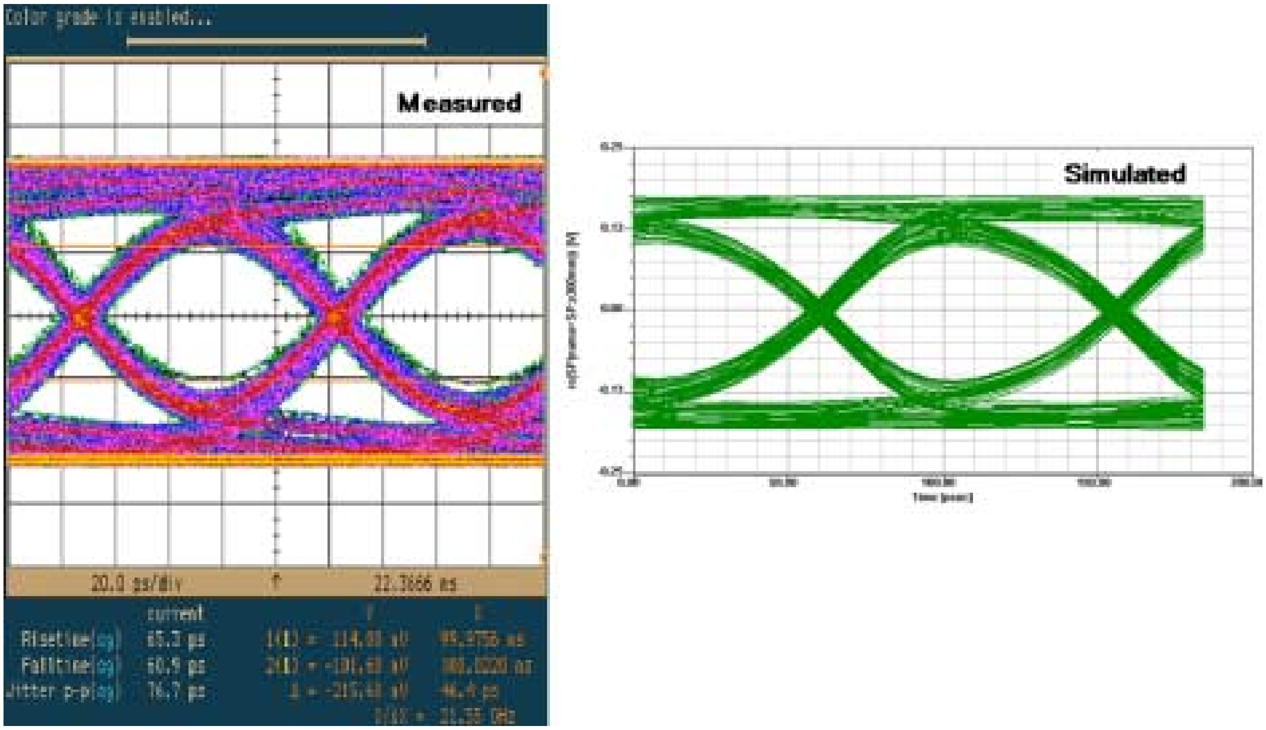


Figure 57   Measured and simulated eye diagram for the XFP channel

APPENDIX C: DIFFERENTIAL S-PARAMETERS AND TDR

C.1 CHOOSING S-PARAMETERS VS TDR

S-Parameters measured with a Vector Network Analyzer (VNA) provide a good match to the frequency and time response, but do not correlate to the location of discontinuity.

TDR response can isolate location of discontinuity from the measured response and allow isolation of signal integrity issues.

Advantage of VNA:

- Most accurate method of modeling passive networks
- High BW >50GHz

Advantages of TDR:

- Isolate signal integrity location
- Immediate view of DUT while measuring
- Intuitive display in anticipating eye pattern problems.

Disadvantage of VNA

- 4-port VNA required or conversion from two ports
- Measurement time

Disadvantage of TDR

- Not very accurate to provide spatial information
- Accuracy decreases as frequency increases due to reduced power in high frequency components.
- Using averaging of many pulses to reduce effective noise, a practical limit to usage is between 10 Ghz and 20 Ghz.
- TDR must be converted to S-parameters by FFT with tools such as: Tektronix IPA or NIST(free US govt) TDNACal

The choice between TDR and VNA should be made based on availability of equipment and tools as well as accuracy required.

C.2 DIFFERENTIAL IMPEDANCE

Stripline and microstrip transmission lines are transverse electromagnetic (TEM) and quasi-TEM structures, respectively. Waves that propagate on these structures have propagation constants that are predominantly linear with frequency and hence phase velocities that are nearly constant with frequency. In isolation, these lines exhibit a single-ended characteristic impedance, phase velocity, and attenuation. As a pair of these lines are moved closer together, coupling occurs that significantly alters the transmission line parameters and makes possible the propagation of differential and common-mode guided waves.

The odd-mode differential impedance observed on a symmetrical differential pair is twice the single-ended impedance of each individual line minus the mutual impedance due to electromagnetic coupling. Strong coupling between the conductors forming a balanced differential pair will lower the differential impedance. In contrast, the differential impedance of a loosely coupled pair appears as the sum of the two individual single-ended impedances. This is shown explicitly in the following equation

$$Z_{diff} = (Z_{11} - Z_{12} + Z_{22} - Z_{21})$$

For symmetrical structures may be given by

$$Z_{diff} = 2 \cdot (Z_{11} - Z_{12}) = 2 \cdot (Z_{22} - Z_{21})$$

where

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$$

Z_{diff} may is also given by

$$Z_{diff} = 2 \cdot Z_{odd}$$

where Z_{odd} is the odd impedance. Similarly the common mode impedance may be given by:

$$Z_{cm} = 0.5 \cdot Z_{even}$$

where Z_{even} is the even impedance.

C.3 4 PORT SINGLE-ENDED S-PARAMETER DEFINITION

Any 4 terminal device may be defined as the ratio of two normalized power wave (the response divided by the stimulus). A block diagram of a 4 port device is shown in Figure 58.

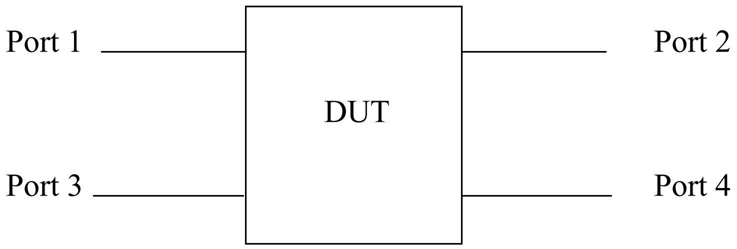


Figure 58 4 Port DUT

The 4 port S-Parameter matrix is given below.

$$Sxy = \begin{array}{cc} & \text{Stimulus Ports} \\ & \downarrow \\ \textit{Response}\ \text{Port} & \begin{bmatrix} S11 & S12 & S13 & S14 \\ S21 & S22 & S23 & S24 \\ S31 & S32 & S33 & S34 \\ S41 & S42 & S43 & S44 \end{bmatrix} \end{array}$$

C.4 2 PORT MIXED MODE DIFFERENTIAL S-PARAMETER DEFINITION

The single ended S-parameters are defined as voltages and currents in reference to ground. In the case of a 2 Port Differential DUT, differential and common mode voltages and currents are defined for each balanced port. A block diagram of a two port differential mixed mode is shown in Figure 59.

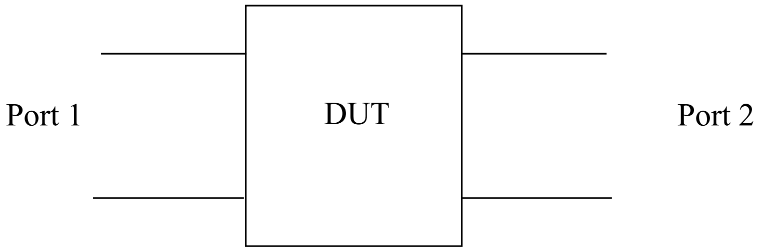
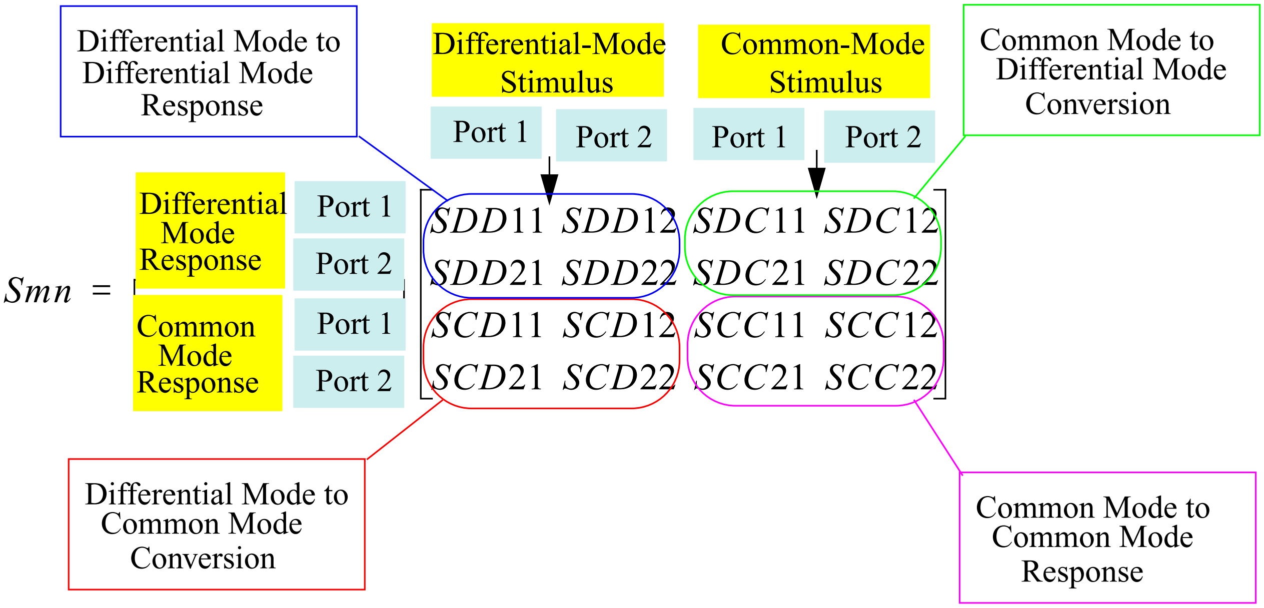


Figure 59 Differential 2 Port DUT

The mixed-mode differential S-Parameters can be organized similar to the single ended S-Parameters. The mixed mode differential S-matrix consists of common mode and differential responses. The 2 Port Differential S-Parameters (Mixed-Mode) are given below:



The differential mode to differential mode performance, SDDxx, are the pure differential mode operation. If differential coupling is small, then the differential mode parameters are reduced to a 2-port single ended S-parameters. The differential mode to common mode conversion, SCDxx, should ideally be equal to Zero with perfect symmetry as it relates to the generation of EMI. The common mode stimulus to differential mode conversion, SDCxx, indicates susceptibility of a device to EMI and should be ideally zero. Common mode stimulus to common mode response indicate performance of the device under common mode.

The mixed mode differential S-Parameters may be written in terms of the two port single ended S-Parameters as the following:

$$S^{mn} = \frac{1}{2}\left[\begin{array}{c|c|c|c} S11 - S31 - S13 + S33 & S12 - S32 - S14 + S34 & S11 - S31 + S13 - S33 & S12 - S32 + S14 - S34 \\ \hline S21 - S41 - S23 + S43 & S22 - S42 - S24 + S44 & S21 - S41 + S23 - S43 & S22 - S42 + S24 - S44 \\ \hline S11 + S31 - S13 - S33 & S12 + S32 - S14 - S34 & S11 + S31 + S13 + S33 & S12 + S32 + S14 + S34 \\ \hline S21 + S41 - S23 - S43 & S22 + S42 - S24 - S44 & S21 + S41 + S23 + S43 & S22 + S42 + S24 + S44 \end{array}\right]$$

A commonly available two ports Vector Network Analyzer with standard calibration technique and the above relationship can be used to test for compliance to the XFI channel. If a 4 port VNA is available then the differential and common mode parameters can be measured directly.

SDD21 is given by:

$$SDD21 = \frac{1}{2}(S21 - S41 - S23 + S43)$$

If the differential channels is symmetrical, then:

S21 = S43, S41 = S23, S12 = S34, S14 = S32, S11 = S33, S22 = S44

In a typical application where the channel meets the XFI specification for differential return loss SDD21 can be approximated by the single ended S-Parameter:

$$SDD21 \cong (S21 - S41) \cong S21.$$

APPENDIX D: OPTIMUM VIA DESIGN

D.1 VIAS

Via structures allow PCB designers to route circuit traces between layers of a multilayer board. Vias may be particularly useful to transition from the pins of a BGA or connector down to stripline traces within a host or transceiver board. The most common and inexpensive via structure is the so-called through-hole via. A through-hole via is manufactured by drilling all the way through the PCB followed by a plating process. The plating process provides electrical continuity to top and buried traces by virtue of signal pads located on the desired layers. Alternatives to the through-hole via are the blind via and the back-drilled via. Although these alternatives may provide higher performance, it is generally believed that most XFP adopters will use the lower cost through-hole via for volume manufacturing.

This section examines single-ended and differential through-hole vias for XFI implementation. Guidelines are provided for trace routing and for particular via dimensions.

D.2 SINGLE-ENDED VIAS

Figure 60 depicts a single-ended through-hole via that provides a transition from the top layer to the next adjacent layer in a 16-layer PCB. Only that portion of the via between the adjacent layers is used for electrical path. The remaining portion provides an electrically short open-circulated transmission line stub. The additional reactance that results tends to lower the characteristic impedance and hence causes reflections. A much better approach is to route traces as shown in Figure 61. By transitioning from the top layer to a layer near or on the opposite side of the board minimizes the size of the open circulated stub and hence minimizes electrical reflections.

Full-wave, 3D electromagnetic simulations were performed using Ansoft High Frequency Structure Simulator (Ansoft HFSS™). The simulations were used to evaluate the relative performance of via structures with and without open-circulated stubs. Figure 62 is a plot of the extracted s-parameters for transitions from the top layer to various layers of a 16-layer PCB. The red curve is for trace routing from the top to the bottom layer and yields the best performance (lowest reflections).

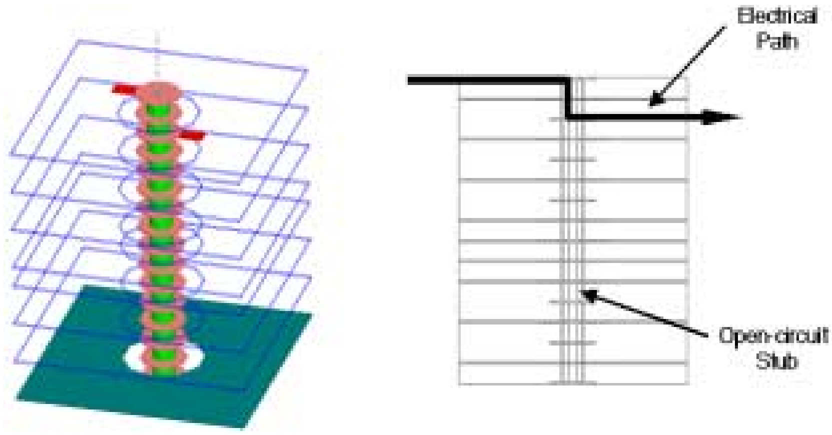


Figure 60 Single-ended via with electrical path between adjacent layers leaves an open-circuit stub causing poor impedance match.

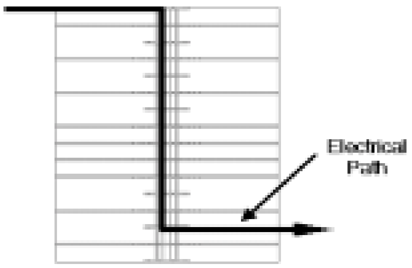


Figure 61 Preferred method for trace routing with vias. Routing the electrical path from the top layer to a layer near or on the opposite side of

the board minimizes the open-circuited stub.

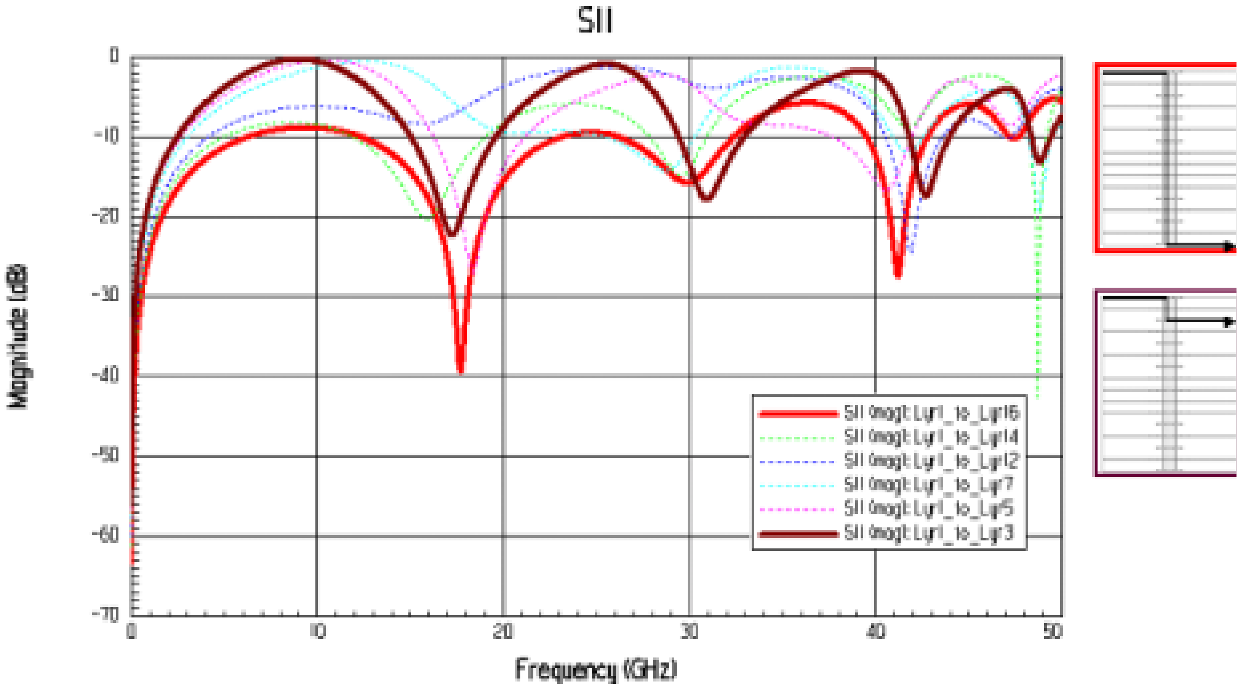


Figure 62 Simulated return loss (s_{11}))

D.3 DIFFERENTIAL VIAS

Because the XFI interface is differentially signaled, vias are generally expected to occur in pairs. These differential vias are used to route signals from top layer microstrip traces down to buried stripline traces. Figure 63 shows a differential via geometry with a pair of via structures traversing through several power and ground planes on a 100mil thick multilayer PCB. Critical dimensions are the via diameter (drill size), pad diameter, gap between the pad and the ground/power plane cutout, and via pitch. Fullwave 3D electromagnetic simulations were performed to identify dimensions that would minimize reflections and provide the best signal fidelity. The tunable parameters are the via pitch and gap as illustrated in the Figure 64.

Two board thicknesses were considered for the simulations: a 100 mil thick board and a 62 mil thick board. A parametric sweep of via pitch and gap revealed that the best performance was achieved using the dimensions outlined in Table 64. Interestingly, the dimensions for both board thicknesses are identical. This can be explained by considering the via structure as a transmission line with propagation along the dimension perpendicular to the PCB plane. It is intuitive that this transmission line should have a uniform cross-section that is independent of the length of the line (board thickness).

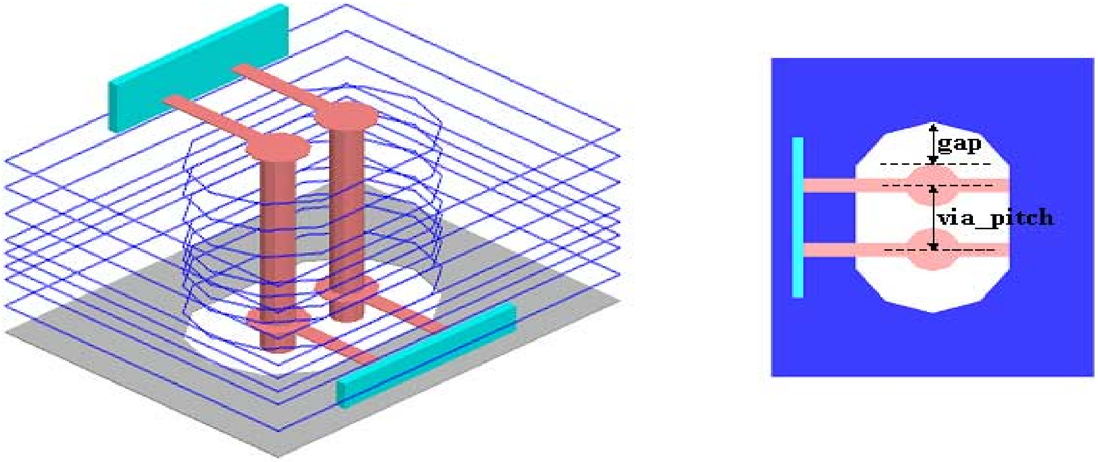
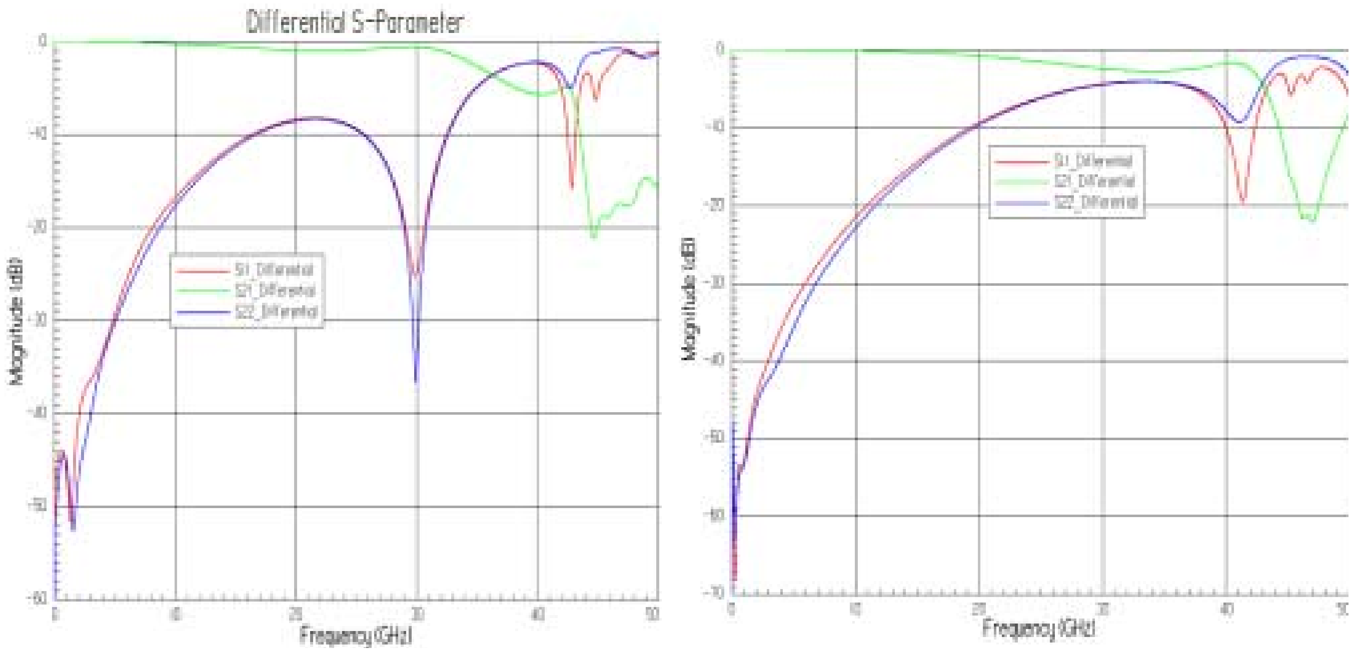


Figure 63 Differential via geometry a 100mil multilayer PCB.

Table 64 Optimized differential via geometry for 100 mil and 62 mil thick PCB

Parameter	*Gap (mm)*	*Via Pitch (mm)*	*Drill Size (mm)*	*Pad Diameter (mm)*
100 mil Board	0.52	0.8	0.3	0.56
62 mil Board	0.52	0.8	0.3	0.56



(a) 100 mil

(b) 62 mil

Figure 64 S-parameters for optimized via structures with dimensions given in Table 1. (a) 100 mil thick PCB. (B.) 62 mil thick board.

D.4 GSSG DIFFERENTIAL VIAS

An improvement to the traditional differential via is to utilize a ground-signal-signal-ground (GSSG) geometry. The GSSG differential via consists of four single-ended vias as shown in Figure 65. The two inner vias are the differential signal lines and the outer two vias are ground return lines. Although differential signaling generally provides for all return path currents, the GSSG geometry can support common-mode signals with a well-controlled return current path. Any common-mode signals that get coupled or generated can propagate through the via (rather than being scattered) and along the transmission line to the receiver where it is terminated.

Critical dimensions for the GSSG geometry are via diameter (drill size), pad diameter, gap between the pad and the ground/power plane cutout, via pitch, and via-to-ground via. With the additional conductors of the GSSG structure, there are more tunable parameters that can be used to provide optimal performance. Fullwave 3D electromagnetic simulations were performed to optimize the geometry on a 62-mil stack up. Table 65 provides four alternative GSSG via dimension combinations that provide acceptable performance.

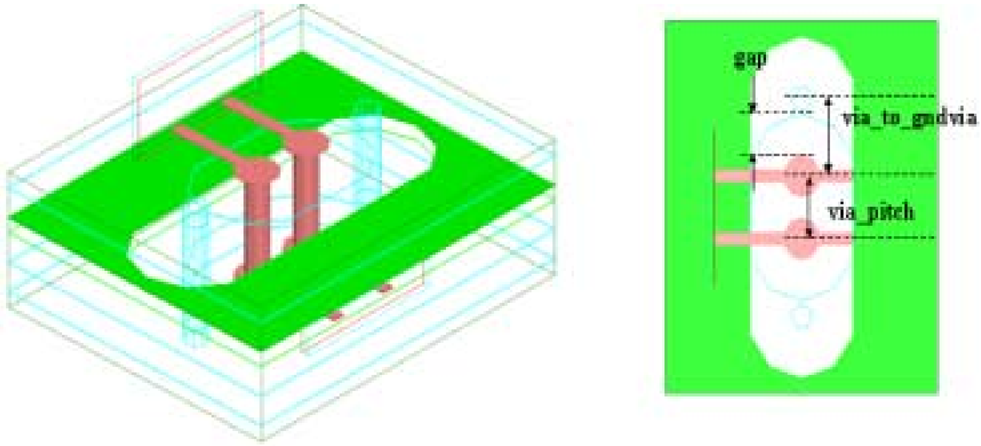
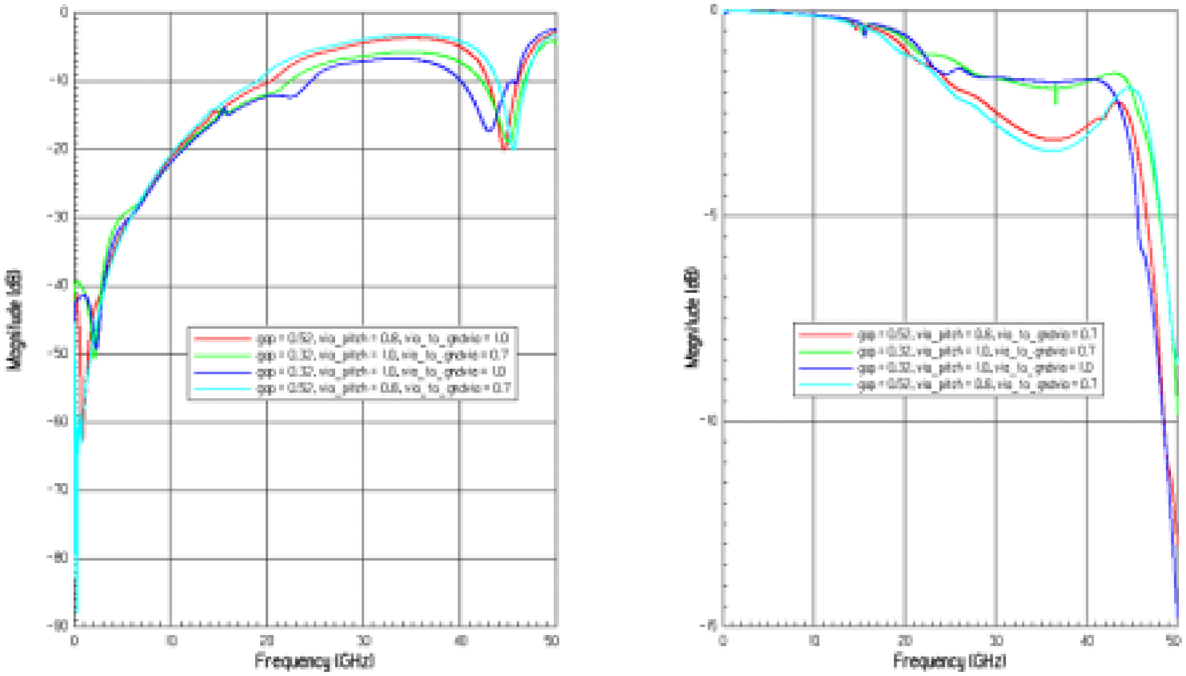


Figure 65 GSSG via structure

Table 65 Four alternative GSSG via dimension

Gap (mm)	*Via Pitch (mm)*	*Via-To_Ground (mm)*	*Drill Size (mm)*	*Pad Diameter (mm)*
0.32	1.0	0.7	0.3	0.56
0.32	1.0	1.0	0.3	0.56
0.52	0.8	0.7	0.3	0.56
0.52	0.8	1.0	0.3	0.56



(a)S_{11} (B)S_{21}

Figure 66 Extracted s-parameters for the four alternative GSSG via

APPENDIX E: JITTER METHODOLOGY AND MEASUREMENT

E.1 EYE MASK COMPLIANCE

This annex describes requirements for determining eyemask compliance. Mask templates and coordinates are given in the appropriate subclauses in clause 2.

- Compliance is to be assured during system operation. However, measurements with patterns such as PRBS23 or a valid 10GBASE-R or 10GBASE-W or OC192c or STM-64 signal are likely to give similar results.
- During test, both transmit and receive paths must be active to include the effects of crosstalk. Traffic in the other direction (than the one being tested) must use a asynchronous clock
- Compliance at higher rates can qualify for lower rates, however the opposite is not allowed.
- Testing may include guard banding, extrapolation, or other methods, but must ensure that mask violations do not occur at a rate above 1E-12.
- The eye template is to be measured differentially.
- If AC coupling is used, the 3dB corner frequency shall be set sufficiently low to avoid adding baseline wander into the measurement.
- All loads are specified at 100 ±5 Ω differential.
- Zero “0” and One “1” on the unit interval scale are to be determined by the eye crossing means measured at the average value (zero volts) of the eye pattern, as illustrated in Figure 67. The average value might not be at the jitter waist.

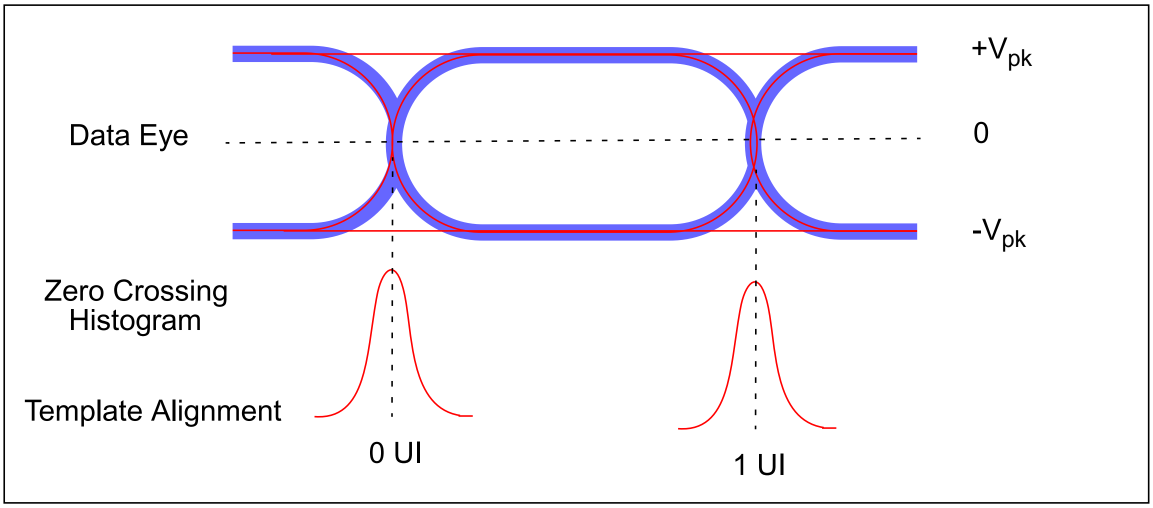


Figure 67 Eye Template Alignment

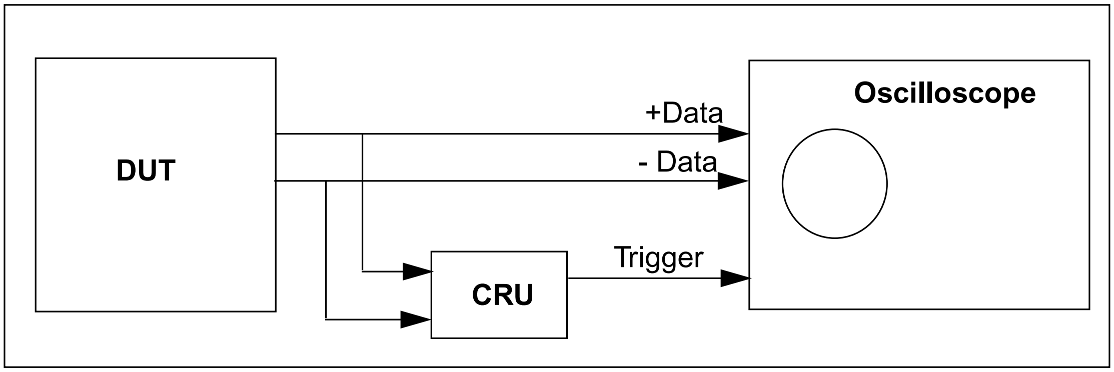


Figure 68 Eye mask measurement setup - block diagram.

A clock recovery unit (CRU) should be used to trigger the scope for mask measurements as shown in Figure 68. It should have a high frequency corner bandwidth of 4 MHz and a slope of –20 dB/decade with maximum peaking of 0.1 dB.

E.2 NON-EQJ JITTER EYE MASK

Compliance point B and D are required to have bounded non-EQJ jitter. This test guarantees that the total jitter is not overwhelmed by the DCD and random jitter. The setup is similar to the standard eye mask measurement but the eye is measured with and without the inverse channel filter. The block diagram of the measurement is shown in Figure 69.

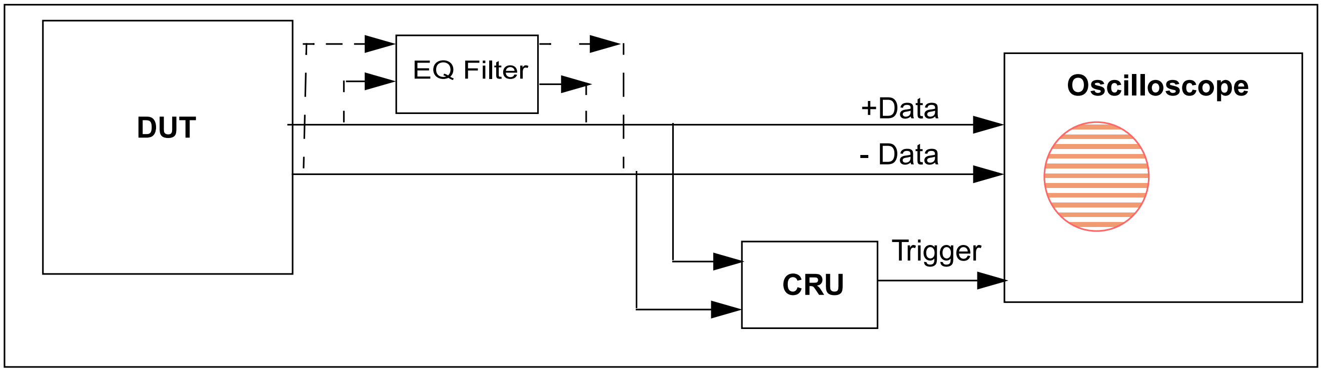


Figure 69 Eye mask measurement setup - block diagram.

EQ Filter is based on the inverse response of the channel, where the channel is specified in section 3.5. An approximate EQ filter may be constructed with following characteristics:

$$H(f) = \frac{fl + if}{fu + if}$$

Where: fl=2.5 GHz
fu=5 GHz

In addition the filter must meet:

- SDD21 accuracy must meet ± 1dB from 1MHz to 10 GHz.
- SDD11 > 20 dB from 1MHz to 10 GHz
- Differential Skew <5 ps

Alternatively the waveform may be captured and the above filter response may be applied by post processing. It is also expected some time in the future there will be Time Interval Analyzer (TIA), which can measure the non-EQJ jitter directly.

E.3 STRESS EYE TEST FOR RX TOLERANCE TESTING

E.3.1 INTRODUCTION

This clause provides guidance for jitter tolerance testing at compliance points B', C, and D with input jitter and vertical eye closure as specified respectively in Table 17, Table 15, and Table 11 as given in Chapter 3:.

The applied jitter combines ISI (equalizable portion of jitter) and non-EQJ jitter (non-equalizable portions of jitter). The receiver under test shall tolerate an additional sinuosidal jitter (SJ) term as defined by the appropriate Telecom and/or Datacom requirements in this document.

MJSQ[1] and OIF CEI[2] both provide further information on definitions, setups, calibration and methods for jitter tolerance testing.

E.3.2 TEST EQUIPMENT

Beyond calibrated jitter and eye closure properties, the test source should be within the requirements for common mode voltages, return loss, etc. that are given in Chapter 3:. Return loss of the test source should be near ideal.

Jitter generation mechanisms can be based on phase modulation at the clock source or pattern generator input or output. Any approach that modulates or creates the appropriate levels and frequencies of the jitter components is acceptable.

An RF attenuator or output amplitude control of the test source may be required to set the vertical eye opening of the stressed eye.

E.3.3 TYPES OF JITTER

The XFP specification allows variation and freedom in allocation and types of jitter within the bounds given in Table 17, Table 15, and Table 11. As such, there is no single tolerance test setup than can fully represent all the possibilities. However, some considerations are given below.

non-EQJ jitter can include duty cycle distortion (DCD), random jitter (RJ), and periodic jitter (PJ). Non-EQJ jitter is uncorrelated to the primary data

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[1] Information Technology - Fibre Channel - Methodologies for Jitter and Signal Quality Specification - MJSQ, Project 1316-DT/Rev 14, June 9, 2004.

[2] Optical Internetworking Forum - IA # OIF-CEI-02.0 - Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps and 11G+ bps I/O, February 28th, 2005

stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum.

Noticeable amounts of DCD are rare at compliance points B', C, and D. If DCD is used for compliance testing, it should not exceed 0.05 UI pk-pk. DCD can be viewed when transmitting a repeating 1010 pattern.

Moderate amounts of RJ are possible at compliance points B', C, and D, typically attributable to the clock source and/or a CMU. Large amounts of RJ are not common, though, and so if RJ is used for compliance testing, the following advice is given:

- the RJ magnitude should not exceed 0.2 UI pk-pk (at 1E-12 probability);
- the RJ should be filtered with a 10 MHz high-pass filter to reduce sensitivity to variations in CDR tracking;
- the upper cutoff frequency for the RJ should be at least 80 MHz.

Single frequency PJ is sinuosidal jitter, and can be considered as another form of non-EQJ jitter. However, single frequency PJ is not common in normal operation and is harsh as a form of non-EQJ jitter for compliance testing at B', C, and D. If single frequency PJ is used, its frequency(s) should be generally above the tracking bandwidth of the CDR of the port being tested. Note - this use of sinuosidal jitter is in addition and should not to be confused with the SJ tolerance mask templates specified in the document.

A versatile option for PJ is to employ multi-tone jitter created by a PRBS generator. PRBS jitter has a distributed spectrum and can be low-pass filtered to produce a more normal probability density function (pdf) for non-EQJ jitter. MJSQ and CEI have more information on this approach.

To create non-EQJ & ISI jitter, a section of PCB is recommended to emulate the behaviors expected in an application. The length and construction details are left to the user, but when completed, the required values for Total Jitter and non-EQJ jitter should be satisfied. Coaxial cable typically exhibits a different response, both in magnitude and phase.

E.3.4 CALIBRATION

The signal should be calibrated differentially through a standard compliance test fixture (see Appendix A:) and into standard instrumentation loads. If complementary single-ended signals are used, be sure they are carefully matched in both amplitude and phase.

Except for sinuosidal jitter, all calibration should use a single pole high-pass jitter filter with -3 dB frequency at 4 MHz.

The jitter is defined at a probability level of 1E-12, consistent with the requirements of Annex E.1. To calibrate the jitter, methods given in MSJQ and CEI are recommended. Given random jitter and the nature of the long test patterns, low probability jitter events may be present. A technique that can accurately measure low probability events is recommended to avoid an overly stressful test condition.

The vertical eye opening is defined at a probability level of 1E-12, consistent with the requirements of Annex E.1. Like jitter, low probability vertical closure may be present, and if not accurately measured and accounted for in calibration, could lead to an overly stressful test condition.

E.3.5 TESTING

Operate the system with the appropriate data pattern for the application - SONET, 10G Ethernet, 10GFC, or G.709 then test applicable compliance points B’, C, or D.

All signals and reference clocks that operate during normal operation shall be active during the test including the other signal path in the duplex pair. The other signal path shall be asynchronous and up to the maximum allowable differential PPM value given in the appropriate protocol specifications.

Apply the SJ tolerance masks, at each SJ tolerance frequency verify that the DUT provides a BER of at least 1E-12 at the applicable compliance points B’, C, or D.

E.4 JITTER PEAKING SPECIFICATIONS AND MEASUREMENTS

In Section 3.9 of the XFP MSA, module jitter peaking specifications are given for datacom and telecom modules for both the receiver and transmitter paths. In the case of telecom modules to be used for looptiming based regenerator applications, the jitter peaking below 120 KHz is limited to 0.03 dB for both receiver and transmitter. This last specification is derived from the need for the overall system jitter peaking to be kept below 0.1 dB for regenerator applications. While these requirements are believed to be practical for existing signal conditioner and module optics technology, verification of this performance presents considerable difficulties due to limitations of current measurement equipment. This annex describes these difficulties and suggests alternative characterization techniques to be used until appropriate measurement equipment becomes available.

Equipment exists today to do jitter transfer measurements on devices with electrical inputs and electrical outputs as well as for equipment with optical inputs and outputs. This type of equipment is able to achieve high accuracy by calibrating measurements against measurements made with the instrument looped back to itself. Making an equivalent measurement of a device with electrical input and optical output, or vice versa, is more problematic. Even if an instrument can make such a measurement, its accuracy would probably be limited to far worse than 0.03 dB because a direct input to output calibration would not be possible.

In order to do an electrical-to-optical or optical-to-electrical jitter transfer measurement with high accuracy, a reference optical receiver or transmitter with well-characterized jitter transfer characteristics is required. Such a reference device could be used to provide a reference calibration measurement against which to compare the device under test in a system configured to perform an electrical-to-optical or optical-to-electrical measurement. Alternatively, a reference receiver could be used to convert the optical output of a device under test to electrical allowing a precision electrical-to-electrical measurement of the combination from which the transfer characteristics of the reference receiver could be subtracted. Similarly, a reference transmitter could be used to stimulate an optical receiver path under test. At this writing, such well-characterized reference transmitters and receivers are not commercially available.

There are several means by which host system and module manufacturers can verify the required performance needed to meet the overall systems requirements. (Examples are given for the difficult 0.03 dB peaking case, but the same logic applies to the 1 dB peaking requirement for datacom modules).

5. Overall System Measurement

Host system manufacturers can qualify modules for jitter peaking by measuring them in the desired final system environment. A module under test can be placed in the target host system and the overall system optical-to-optical jitter transfer can be measured by placing the system in a looptiming loopback mode (which should be below 0.1 dB at 120 KHz or less). For further accuracy, the host system’s jitter peaking can be separately measured and subtracted from the total measurement to approximate the module’s total transmit and receive path peaking which should be less than 0.06 dB below 120 kHz. This measurement can be achieved by measuring the system’s electrical to electrical jitter peaking by substituting a host compliance test coupon for the module under test.

6. Module Total Jitter Peaking Measurement

A useful, but not complete measurement can be made of the module jitter peaking directly by testing the module with the optical output looped back using an electrical-to-electrical jitter peaking test, or by looping the electrical output back to the transmitter input and performing an optical to optical measurement. In this case a measure of the sum of the transmit and receive path peaking is made. This should be less than 0.06 dB below 120 KHz, though this still allows for the possibility that either the receive or transmit paths are greater than 0.03 dB.

7. Measurement of Module Signal Conditioner

It is expected that the low frequency jitter transfer characteristics of an XFP module will be dominated by the signal conditioners in the transmit and receive paths. While not a useful module compliance test, a module manufacturer can determine likely module jitter peaking performance by separately characterizing the performance of the signal conditioners used in the modules under likely worst-case conditions. Such measurements should be done with the signal conditioners in a test environment as similar as possible to that of the final module. These measurements do have the advantage that they can be used to separately characterize the module receive and transmitter paths.

While none of the above techniques is a perfect substitute to a direct compliance test of module jitter peaking, they probably provide a reasonable alternative until appropriate test equipment is developed.

E.5 AC COMMON MODE TEST

To minimize generation of common mode noise and associated EMI, XFI limits the maximum common mode voltage at the compliance point. The common mode voltage is measured by subtracting the differential output on the scope. The RMS value are calculated by applying the Histogram function to the common mode signal. Common mode measurement are specified for the following test point:

- A 15 mV RMS - Output
- B 25 mV RMS - Output
- C’ 15 mV RMS - Output
- D 25 mV RMS - Input.

E.6 TERMINATION MISMATCH

Termination mismatch is defined as the difference between the complimentary R_p and R_n resistors as shown in Figure 5. Measuring termination mismatch through an AC coupling capacitor requires access to the IC. Termination mismatch is defined as:

$$\Delta Z_M = 2 \times \frac{R_p - R_n}{R_p + R_n} \times 100$$

Alternatively, the termination mismatch can be measured by applying a low frequency test tone to the differential inputs as shown in Figure 70. The test frequency must be high enough to overcome the high pass effects of the AC coupling capacitor. Low frequency termination mismatch is then given by:

$$\Delta Z_M = 2 \times \frac{I_p - I_n}{I_p + I_n} \cdot \frac{R_{diff} + 100}{R_{diff}} \cdot 100$$

where I_p and I_n are the current flowing in to the XFI port as shown in Figure 70.

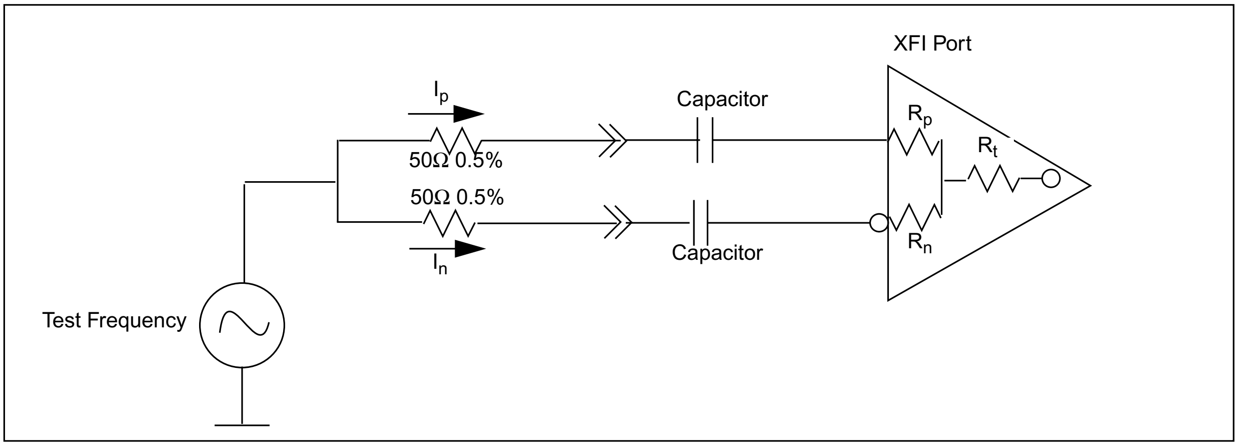


Figure 70 AC Termination Mismatch Measurement

E.7 POWER SUPPLY NOISE TESTING METHODOLOGY

E.7.1 POWER SUPPLY NOISE COMPLIANCE

The module is specified to tolerate 2% of broadband noise amplitude on the power supply at frequencies up to 1 MHz, then 3% for frequencies up to 10Mhz.   This methodology covers test methods to assure compliance to the XFP specification.

E.7.2 POWER SUPPLY NOISE METHODOLOGY

In this test noise is injected to the power supply rail from a function generator generating a sine wave. The noise measurement set up is shown in Figure 71. The noise is AC coupled into the test board and the DC power is coupled in through an inductor to keep the noise from sinking into the power supply. The inductor should be optimized for maximum noise at the test point over all frequencies tested. The amplitude should be measured at the connector on the test board with the module plugged in. This assures the noise induced into the module is filtered within the module regardless of amount of test board decoupling. The required amplitude of the noise signal generator will vary from different test boards due to decoupling and layout differences. The typical noise amplitudes are listed in Table 66. The worst case system noise is with the module plugged into the socket while achieving the desired amount of noise.

E.7.3 POWER SUPPLY NOISE METHODOLOGY

Tests for power supply noise compliance should include optical receiver sensitivity, which can be measured with SONET GR-253 or IEEE802.3ae methodologies. Also optical transmitter jitter with a worst-case electrical eye as an input (Table 13) should be measured. Transmitter jitter testing can be done with IEEE802.3ae eyemask and Tpd measurements, or SONET GR-253 jitter generation measurements. Testing should look at the difference of these parameters with and without the noise present. The noise source frequency should be varied from 0 to 10Mhz to determine if any frequency causes a parameter to fall out of the specification limit. In all cases, the parameters measured should pass the optical standards with the noise present over all frequencies specified.

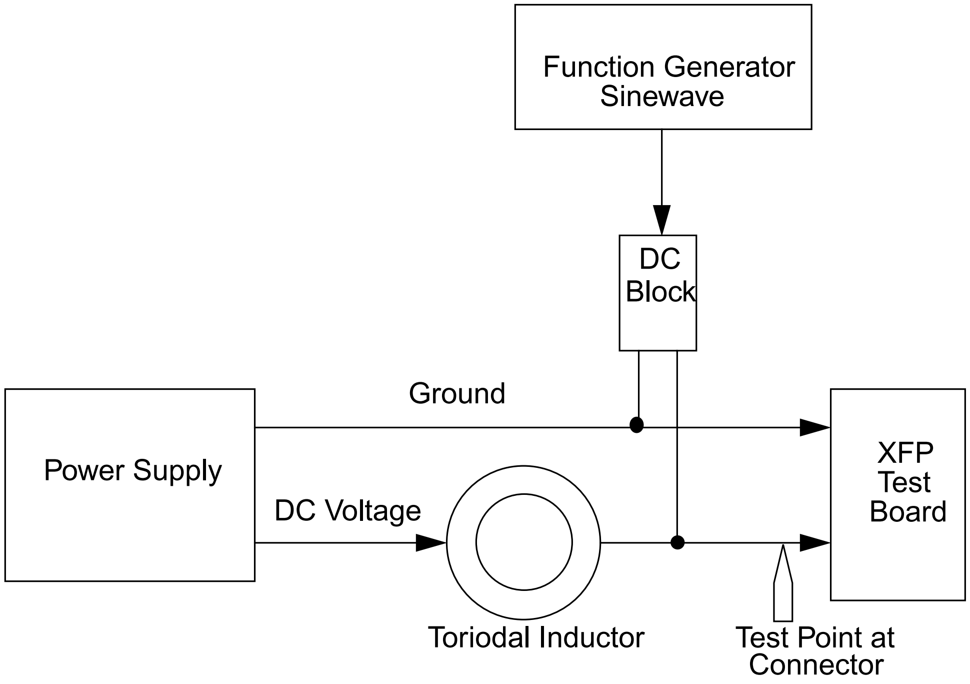


Figure 71 Power Supply Ripple Setup

Table 66 Noise Amplitude for XFP power supplies (Nominal)

Power Supply	*0-1 MHz (2%)*	*1-10 MHz (3%)*
5.0V	100mV	150mV
3.3V	66mV	99mV
1.8V	36mV	54mV
-5.2V	104mV	156mV

APPENDIX F: XFI IMPLEMENTATION FOR BER 1E-15

F.1 XFI ELECTRICAL IMPLEMENTATION FOR BER 1E-15

This Appendix describes a method to implement BER 1E-15 over XFI electrical interface and does not apply to optical link BER. To actually meet BER 1E-15 over XFI channel significant additional care and longer testing would be required to guarantee operation, which is beyond the scope of the MSA.

Starting with XFI electrical specifications of section 3.6, BER 1E-15 or better can be implemented by:

- Reduce the transmitter output jitter in conjunction with receiver jitter tolerance (Incompatible with standard XFI components)
- Reduce the interconnect jitter budget (Compatible with standard XFI components)

XFP MSA implementation for BER of 1E-15 is based on reducing the interconnect jitter budget. XFP MSA implementation relies upon by reducing the interconnect trace length by 20% as listed in Table 67.

Please use jitter tables in this Annex to implement XFI channel for BER 1E-15. These tables are replacement for associated jitter tables in Section 3.6. Jitter table in this Annex are adjusted in the following fashion to achieve BER 1E-15 and maintain compatibility with standard XFI specifications:

- Output jitter values are increased by adjusting for Q of 16 (BER 1E-15) but the total jitter is the same as section 3.6 for Q of 14 (BER 1E-12).
- Receiver input jitter values are reduced by adjusting for Q of 16 (BER 1E-15) but the total jitter is the same as section 3.6 for Q of 14 (BER 1E-12).

Table 67 Host Board Interconnect for BER 1E-15

Type	*Material*	*Trace Width (mm)*	*Loss Tan*	*Copper (oz)*	*Trace Length (mm)*
Microstrip	4000-6	0.3	0.025	1	160
	4000-13	0.3	0.016	1	240
Stripline	4000-6	0.125	0.025	1/2	120
	4000-13	0.125	0.016	1/2	160

F.1.1 XFI ASIC/SERDES TRANSMITTER OUTPUT JITTER SPECIFICATIONS AT A FOR BER 1E-15

Table 68 is replacement forTable 9 XFI ASIC/SerDes Transmitter Output Jitter Specifications at A.

Table 68 XFI ASIC/SerDes Transmitter Output Jitter Specifications at A for BER 1E-15

Transmitter - A	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Determinstic Jitter for Q of 16	DJ	See E.1, 1			0.15	UI (p-p)
Total Jitter for Q of 16	TJ	See E.1, 1			0.321	UI (p-p)
Eye Mask	X1				0.161	UI
Eye Mask	X2				0.4	UI
Eye Mask	Y1		180			mV
Eye Mask	Y2				385	mV
Jitter Generation for Telecom Applications		50KHz to 8 MHz see 2			6.5	mUI (RMS)

1. In loop timing mode, includes jitter that transfers through the ASIC from the receiver during any valid operational input conditions.
2. Measured with a filter with 50 KHz high-pass cutoff desinged frequency and 8 MHz low pass cut off frequency. The filter rolls off at least for one decade on each side of the passband with -20 dB/Dec Does not apply to a host designed with Optional Synchronous CMU clock, when used in conjunction with a Synchronous CMU module 3.10.1.

F.1.2 XFI ASIC/SERDES RECEIVER INPUT JITTER SPECIFICATIONS AT D FOR BER 1E-15

Table 69 is replacement forTable 11 XFI ASIC/SerDes Receiver Input Jitter Specifications at D.

Table 69 XFI ASIC/SerDes Receiver Input Jitter Specifications at D for BER 1E-15

Receiver- D	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Total Jitter for Q of 16	TJ	See E.1, E.2			0.65	UI (p-p)
Total non-EQJ Jitter for Q of 16[1]		See E.1, E.2			0.45	UI (p-p)
Sinusoidal Jitter Tolerance	SJ	E.3			see 2	
Eye Mask	X1	Note [3]			0.325	UI
Eye Mask	Y1		55			mV
Eye Mask	Y2	Note [4]			525	mV

1. Total Jitter less ISI.
2. Sinuosidal jitter tolerance for Telecom and Datacom respectively given by Figure 9 and Figure 10.
3. Mask coordinate X1=0.225 if total non-EQJ jitter is measured.
4. Out of 525 mV, 100 mV is allocated for multiple reflection.

F.1.3 XFI HOST TRANSMITTER OUTPUT JITTER SPECIFICATIONS AT B FOR BER 1E-15

Table 70 is replacement forTable 13 XFI Host Transmitter Output Jitter Specifications at B.

Table 70 XFI Host Transmitter Output Jitter Specifications at B for BER 1E-15

Receiver- B	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Total Jitter for Q of 16[1,]	TJ	See E.1			0.61	UI
Total non-EQJ Jitter for Q of 16 [1]		See E.1, E.2			0.41	UI
Eye Mask	X1	see 2			0.305	UI
Eye Mask	Y1		60			mV
Eye Mask	Y2	see 3			410	mV
Jitter Generation at B Telecom Applications		50KHz-8MHz, see 4			7	mUI (RMS)

1. In loop timing mode, includes jitter that transfers through ASIC from the receiver during any valid operational input conditions.
2. Mask cordinate X1=0.205 if total non-EQJ jitter is measured.
3. Out of 410 mV, 25 mV is allocated for multiple reflection.
4.Measured with a filter with 50 KHz high-pass cutoff desinged frequency and 8 MHz low pass cut off frequency. The filter rolls off at least for one decade on each side of the passband with -20 dB/Dec. Does not apply to a host designed with Optional Synchronous CMU clock, when used in conjunction with a Synchronous CMU Signal Conditioner module see 3.10.1.

F.1.4 XFI Host Receiver Input JITTER SPECIFICATIONS AT C FOR BER 1E-15

Table 71 is replacement forTable 15 XFI Host Receiver Input Jitter Specifications at C.

Table 71 XFI Host Receiver Input Jitter Specifications at C

Transmitter - C	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Determinstic Jitter	DJ	See E.1			0.18	UI (p-p)
Total Jitter for Q of 16	TJ	See E.1			0.363	UI (p-p)
Sinusoidal Jitter Tolerance	SJ	E.3			see 1	
Eye Mask	X1				0.181	UI
Eye Mask	X2				0.42	UI
Eye Mask	Y1		170			mV
Eye Mask	Y2	see 2			425	mV

1. Sinuosidal jitter tolerance for Telecom and Datacom respectively given by Figure 13 and Figure 14.
2. Out of 425 mV, 25 mV is allocated for multiple reflections.

F.1.5 FI Module Transmitter Input Jitter Specifications at B' FOR BER 1E-15

Table 72 is replacement forTable 16 XFI Module Transmitter Input Electrical Specifications at B'.

Table 72 XFI Module Transmitter Input Jitter Specifications at B' for BER 1E-15'

Receiver- B'	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Total Non-EQJ Jitter for Q of 16[1]	0.41	See E.1, E.2			0.41	UI (p-p)
Total Jitter for Q of 16	TJ	See E.1, E.2			0.61	UI (p-p)
Sinusoidal Jitter Tolerance	SJ	E.3			see 2	
Eye Mask	X1	see 2			0.305	UI
Eye Mask	Y1		60			mV
Eye Mask	Y2	see 3			410	mV

1. Sinuosidal jitter tolerance for Telecom and Datacom respectively given by Figure 16 and Figure 17.
2. Mask cordinate X1=0.205 if total non-EQJ jitter is measured.
3. Out of 410 mV, 50 mV is allocated for multiple reflection.

F.1.6 XFI Module Receiver Output Jitter Specifications at C' FOR BER 1E-15

Table 73 is replacement forTable 19 XFI Module Receiver Output Jitter Specifications at C'.

Table 73 XFI Module Receiver Output Jitter Specifications at C' for BER 1E-15

Transmitter - C	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Determinstic Jitter	DJ	See E.1, 1			0.18	UI (p-p)
Total Jitter for Q of 16	TJ	See E.1, 1			0.363	UI (p-p)
Eye Mask	X1				0.181	UI
Eye Mask	X2				0.42	UI
Eye Mask	Y1		170			mV
Eye Mask	Y2				425	mV

1. Includes jitter transfered from the optical receiver during any valid operational input condition.

APPENDIX G: MODULE THERMAL TESTING

G.1 MODULE THERMAL POWER CLASSES

XFP has four possible power classes:

- Power Level 1 modules – Up to 1.5 W
- Power Level 2 modules – Up to 2.5 W
- Power Level 3 modules – Up to 3.5 W
- Power Level 4 modules – Greater than 3.5 W

The module vendor is responsible to identify the power level of their module to the system designer.

G.2 THERMAL TEST RECOMMENDATION

The purpose of this appendix is to provide guidance to XFP module designers in creating a standard test environment for simulation and/or actual testing. It allows for “one” initial means of communication between module designers and system users.

XFP is designed with an adaptable approach to thermal management allowing use of a single module design in a wide variety of host environments. The tests described in this appendix focus on a module’s thermal performance within a defined system level environment. Host system designs will often optimize one or more of the following parameters to achieve lower XFP case temperatures: module spacing, heatsink shape/length/width/fin design, and airflow direction/mixing.

The tests defined in this appendix are intended to be easy to produce by module manufacturers. For example, the number of modules on a host card has been limited to 4 and a heat sink has been defined for this testing. Module manufacturers may choose to provide additional test data of their module in customer specific applications that may have more or less modules, other heat sinks, or environments.

Substantial variations in module thermal performance can occur depending on system level design. This appendix does not guarantee system level performance, as each system will be designed independent of this document per the end user system requirements. It is the responsibility of the system designer to ensure the thermal characteristics meet their individual system needs. All characterization results presented in this appendix are intended as examples only.

G.3 THERMAL TEST CONFIGURATION

There are two unique system environments anticipated for XFP transceivers. One environment is a PCI envelope with limited vertical space, minimal airflow, and 1-2 transceivers (System A). In this envelope sufficient space is not available for a cage mounted heat sink. A second environment has more vertical space and forced airflow across a larger number of transceivers (system B)

Information presented by the module vendor in relation to this document should be obtained from a 'confined or ducted flow' described as:

- A duct defined by the host board on the bottom, a plane above the host board Table 74, the host board bezel, and a vertical plane 81 mm from the host board bezel.
- PCB host board should have no copper content between planes except for grounding of the cage.
- An insulated duct housing with poor thermal conduction must be used i.e. a plastic.
- Dimensions of system should allow for 4 modules on 23.5 mm spacing.
- For the multiple module configurations, it is assumed that the test conditions drawn for module 1, will be duplicated for module n. i.e. the cage configuration.
- Multiple modules will be adjacent to one another with no gaps from empty module slots.
- The test chamber will be clear of obstruction for 30cm after the outlet.
- A steady state should be obtained to take measurements.
- A blower mounted so that the direction of airflow is side to side.
- Case temperature measurements points may be proprietary and vary from one module design to the next. Module vendors should identify these to the end user for verification in the system level environment.
- Airflow should be characterized using a calibrated hot wire anemometer placed at the airflow inlet
- Thermocouples should be used to measure case temperatures.
- An example of measurement data is shown in Figure 72.

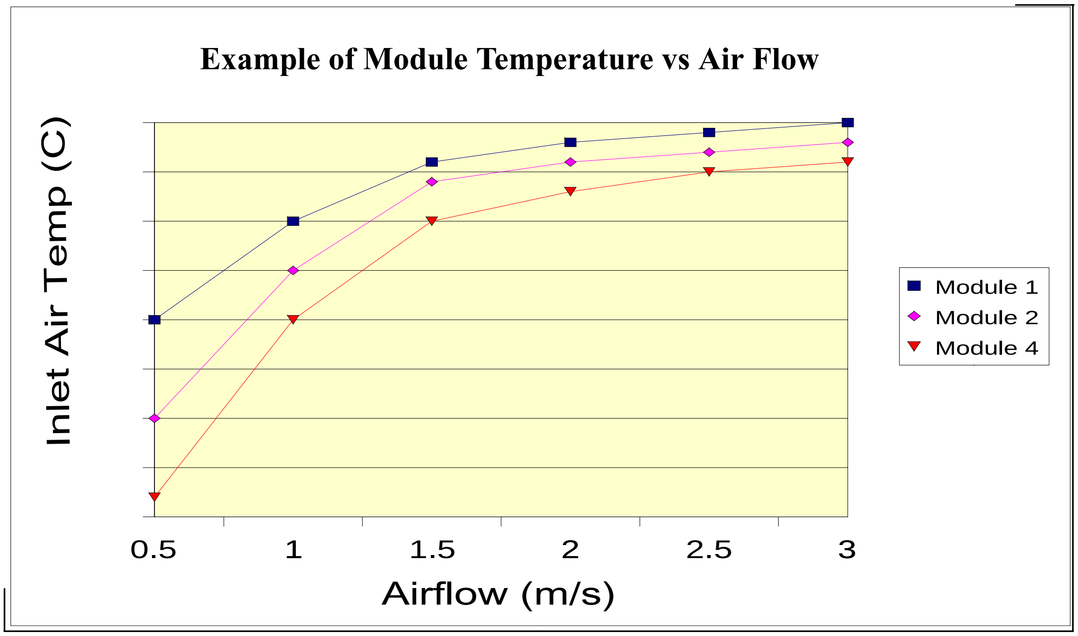


Figure 72 Airflow vs Inlet Air Temperature

- Identical module types will be expected to be characterized I.E. no mix of 850nm,1310nm, or 1550nm is mandated.
- When undergoing thermal evaluation, transceivers should output bi-directional data using a PRBS 2^{31}-1 data pattern.
- Other measurement data provided is at the discretion of the vendor.
- The system should provide uniform airflow across the vent opening and be of constant volume airflow.

The test conditions for system A and system B are defined Table 74.

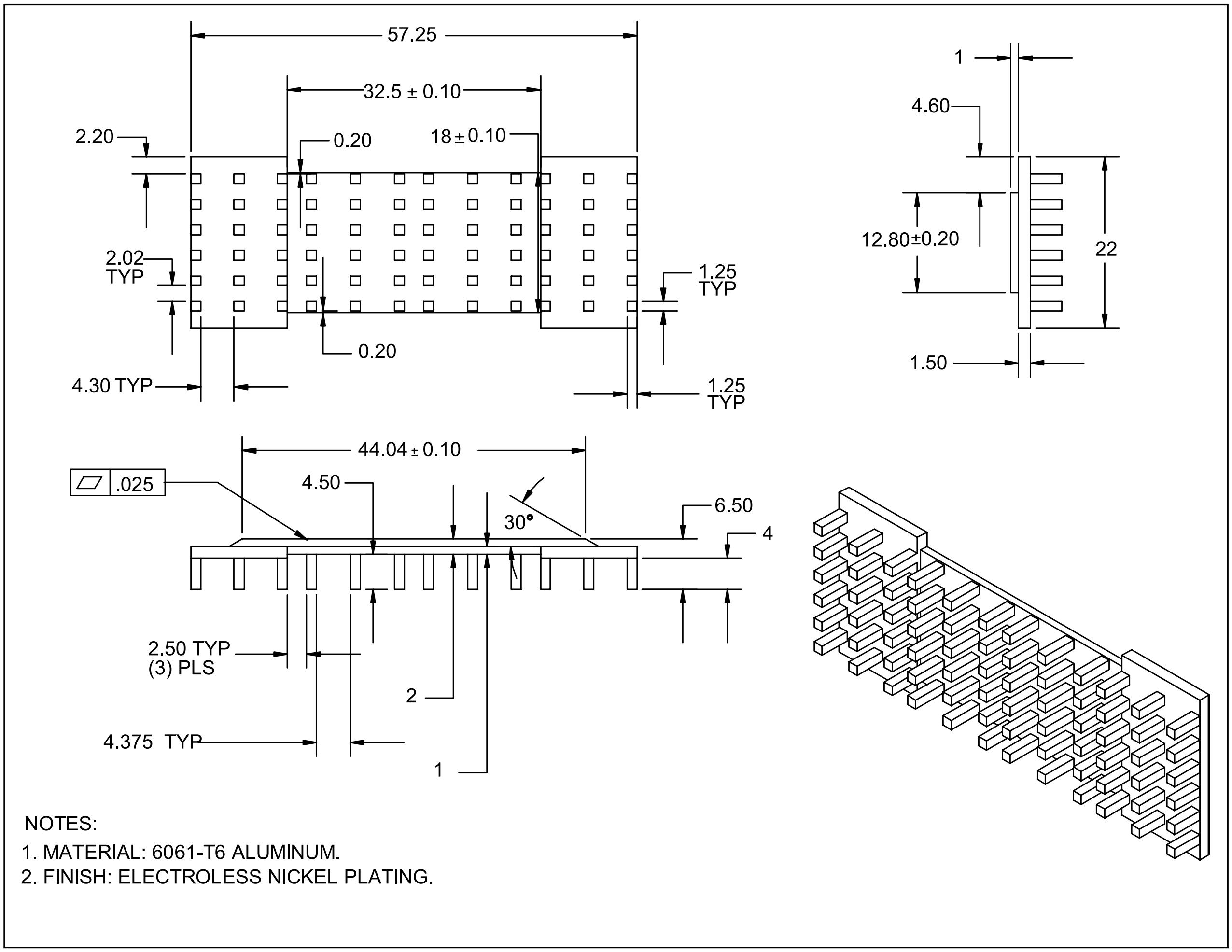
Table 74 Environmental Test Conditions

Parameter	*System A (PCI application)*	*System B (Switch application)*
Number of modules	1 or 2	1,2,4
Inlet air temperature	5˚C to 50˚C	5˚C to 40˚C
Altitude	Sea Level	3000 m
Air Humidity	40% to 60%	40% to 60%

Table 74 Environmental Test Conditions

Parameter	*System A (PCI application)*	*System B (Switch application)*
Minimum air flow	100 lfm	100 lfm
Maximum air flow	200 lfm	500 lfm
Free air space	14.5 mm	19 mm
MSA recommends cage mounted heat sink	No cage heat sink	Optional

For test purposes, the MSA recommended heat sink should be used to provide a consistent test methodologyFigure 73.



NOTES:
1. MATERIAL: 6061-T6 ALUMINUM.
2. FINISH: ELECTROLESS NICKEL PLATING.

Figure 73 Heat Sink Drawing for Module Thermal Testing

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