This specification was developed by the SFF Committee prior to it becoming the SFF TA (Technology Affiliate) TWG (Technical Working Group) of SNIA (Storage Networking Industry Association).

The information below should be used instead of the equivalent herein.

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If you are interested in participating in the activities of the SFF TWG, the membership application can be found at:
http://www.snia.org/sff/join

The complete list of SFF Specifications which have been completed or are currently being worked on can be found at:
http://www.snia.org/sff/specifications/SFF-8000.TXT

The operations which complement the SNIA's TWG Policies & Procedures to guide the SFF TWG can be found at:
http://www.snia.org/sff/specifications/SFF-8032.PDF

Suggestions for improvement of this specification will be welcome, they should be submitted to:
http://www.snia.org/feedback

SFF Committee

INF-8474i Specification for

Xenpak 10 Gigabit Ethernet Transceiver

Rev 3.0 September 18 2002

Secretariat: SFF Committee

Abstract: This specification describes the Xenpak 10 Gigabit Ethernet Transceiver. It was developed by the MSA (Multiple Source Agreement) group in which the following companies participated:

Agilent Technologies	Mitsubishi Electric
Blaze Network Products	Molex
ExceLight	NEC
Extreme Networks	OpNext
Finisar	Optillion
Hitachi Cable	PicoLight
Ignis Optics	Stratos Lightwave
Infineon Technologies	Tyco Electronics
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EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification.

The following member companies of the SFF Committee voted against this industry specification.

The following member companies of the SFF Committee voted to abstain on this industry specification.

SFF COMMITTEE

The SFF Committee is an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

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SFF Committee meetings are held during T10 weeks (see www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electrotechnical Commission).

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:

ftp://ftp.seagate.com/sff/SFF-8000.TXT

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:

ftp://ftp.seagate.com/sff/SFF-8032.TXT

If you are interested in participating or wish to follow the activities of the SFF Committee, the signup for membership and/or documentation can be found at:

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A Cooperation Agreement for 10 Gigabit Ethernet Transceiver Package

Issue 3.0

18th September 2002

1 Revision

Rev	Date	By	Purpose/Changes
1.0	1 May 2001	Antony Spilman	First Public Issue
2.0	26 September 2001	Antony Spilman	Finalize: mechanical dimensions, key functionality, electrical pin-outs, optical Interfaces
2.1	15th February 2002	Antony Spilman	Legal section split. Dimensional changes to Bezel. PCB thickness range reduced Adaptable power supply improved. Updates to XENPAK OUI. Updates to LASI . Updates to NVR control register. Reserved areas in NVR for intelligent power up and diagnostics.
3.0	18th September 2002	Antony Spilman	See below

Rev 3.0 Main changes

Feature Additions

- Major updates to Section 11 adding XENPAK Digital Optical monitoring functions
- Added Optional Low power startup to Section 10.4.2.

Mechanical Changes/Corrections

- Corrected JJ2 to 7 mm (TT2 with tolerance was causing interference with side flange of bezel)

Electrical Clarifications/Corrections

- Change fixed Power Steady State Voltage Accuracy to +/- 5% from +/- 3% Table 7, LASI is still +/- 3%.
- Changed minimum APS current limit to 100 mA from 400 mA.
- Corrected APS fault condition in Section 10.3
- Changed wording of paragraph 2 of 10.4 related to ramp up time of fixed PSUs.
- Added footnote to Fig 13. saying it gives an example of one termination method and the pin definition table should be read for detail.
- Clarified reset states and state transitions and initialization after reset in section 10.5.3.
- Updated references to 802.3ae in the OUI section 10.8.2
- Added 3rd paragraph to section 10.8.3 saying that NVR only uses least 8 significant bits of MDIO register for data.
- Fixed NVR control bit latching issue and added general clarification to section 10.9. State diagram and notes have been substantially updated.
- LASI section 10.13 has been substantially clarified and updated
- Created a new “optional capability” register at NVR location 32891, see 10.12.21. Flagged LPS ability in bit 0 of this register.

2 Summary of MSA Group Members

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7 Purpose of the MSA

This MSA is bound by the operating guidelines published at:

http://www.xenpak.org/MSA/XENPAK_MSA_Operating_Guidelines_R1.0.pdf

8 MSA Mechanical

Fig 1. Isometric Drawings

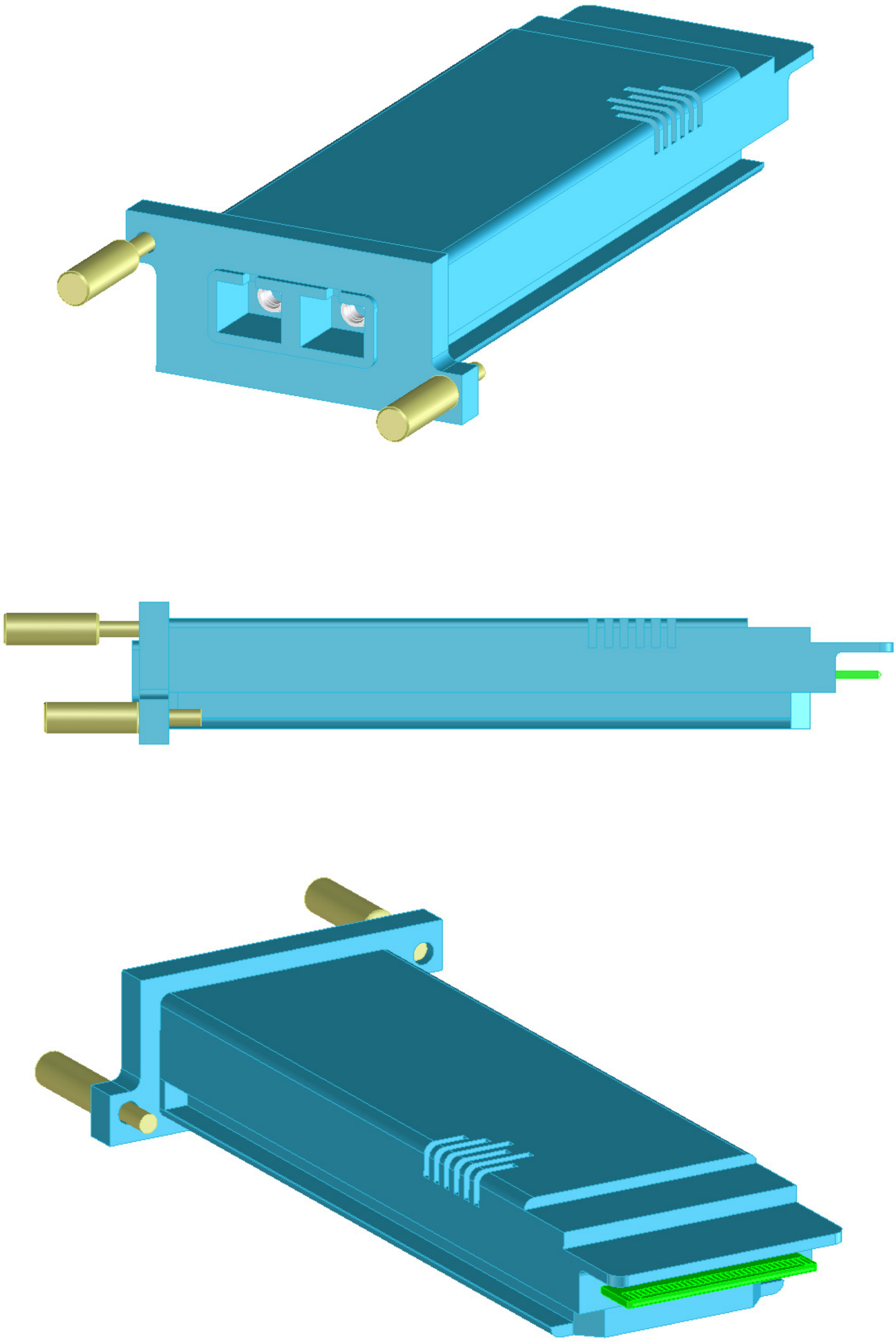
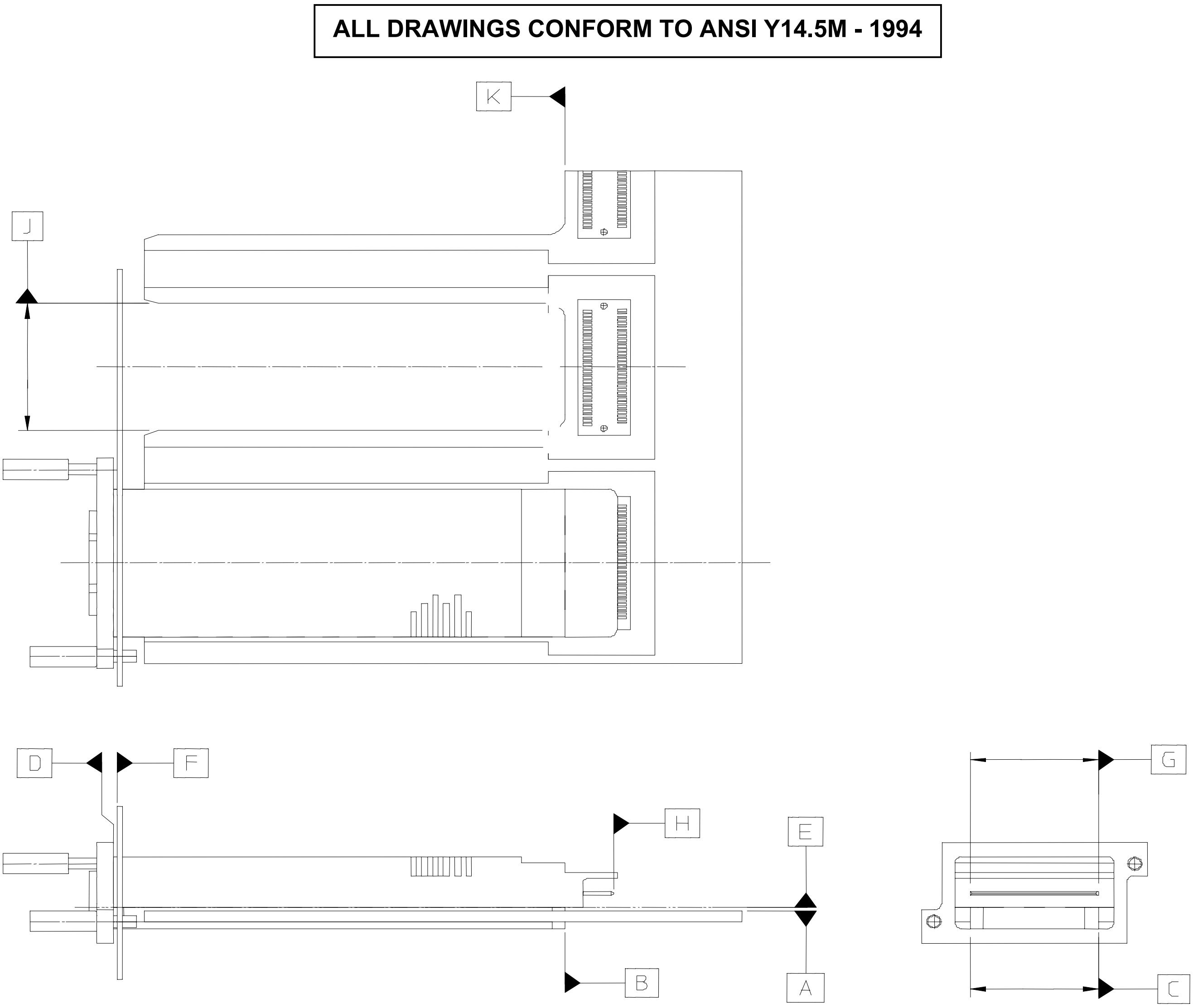


Fig 2. DATUM Legend figure updated



Definition of Datums

DATUM	DESCRIPTION TRANSCEIVER / LINECARD
A	CUSTOMER'S PCB TOP SURFACE
B	PHYSICAL HARD STOP FOR TRANSCEIVER
C	EDGE OF TRANSCEIVER SLOT
D	BACK SURFACE OF TRANSCEIVER BEZEL, SAFETY HARD STOP
E	TRANSCEIVER TOP SURFACE OF SLOT 'P1'
F	FRONT SURFACE OF CUSTOMER'S FACEPLATE
G	EDGE OF TRANSCEIVER'S PCB
H	LEADING EDGE OF TRANSCEIVER PCB
J	EDGE OF CUT-OUT IN CUSTOMER'S PCB
K	PHYSICAL HARD STOP ON CUSTOMER'S PCB

Fig 3. ORIENTATION KEYING OF TX AND RX ORIENTATION Vs PCB

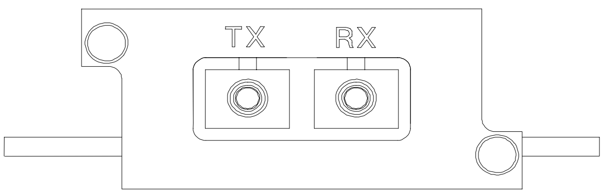
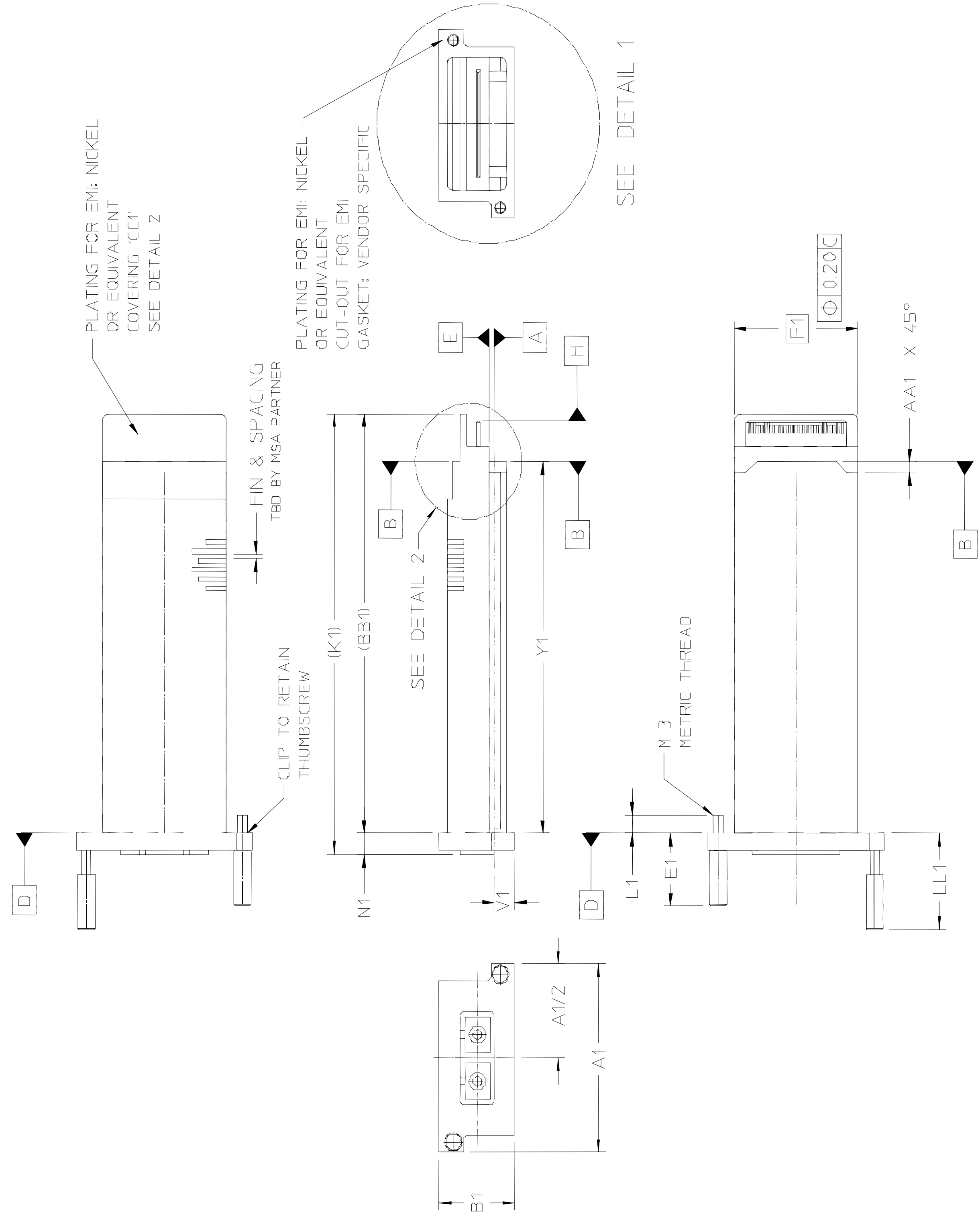
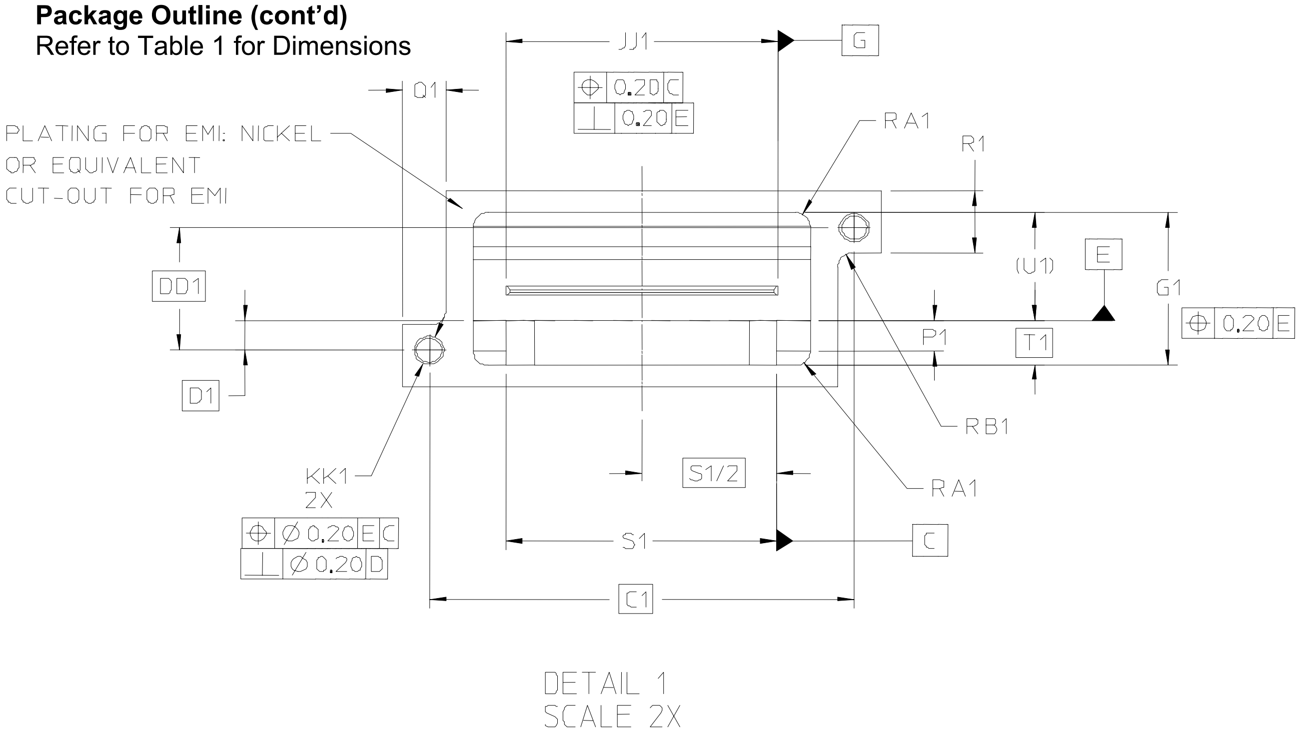


Fig 4. Package Outline

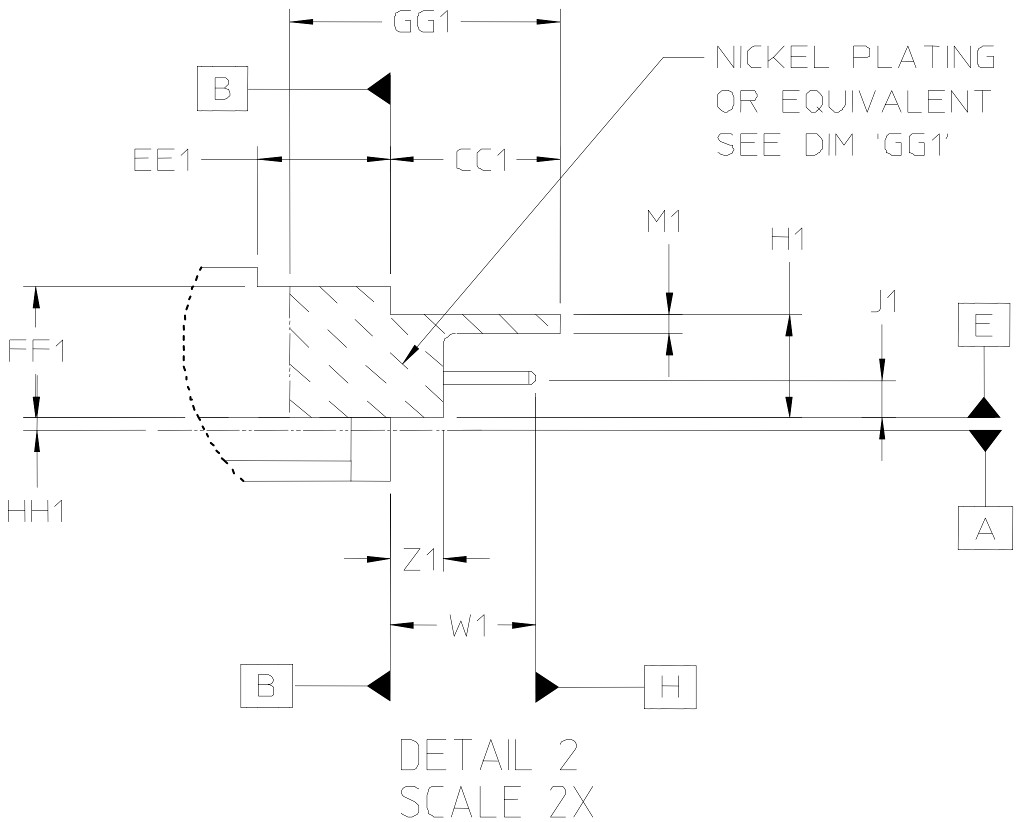
Refer to Table 1 for Dimensions



Package Outline (cont'd)
Refer to Table 1 for Dimensions



END VIEW OF TRANSCEIVER



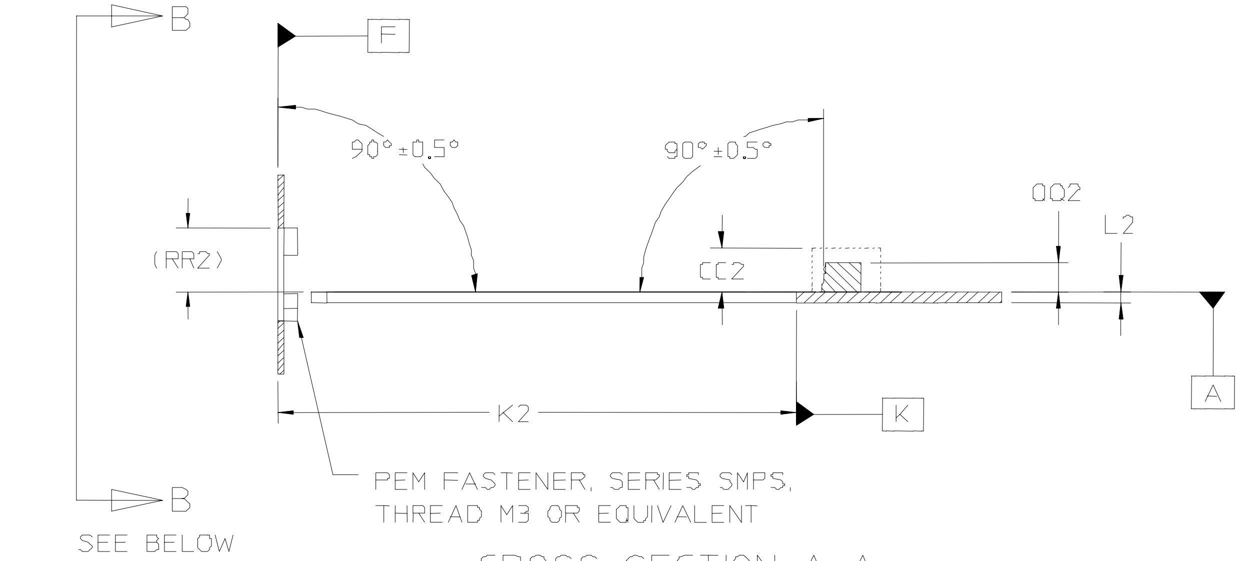
SIDE ELEVATION TRANSCEIVER

Table 1 Package Dimensions

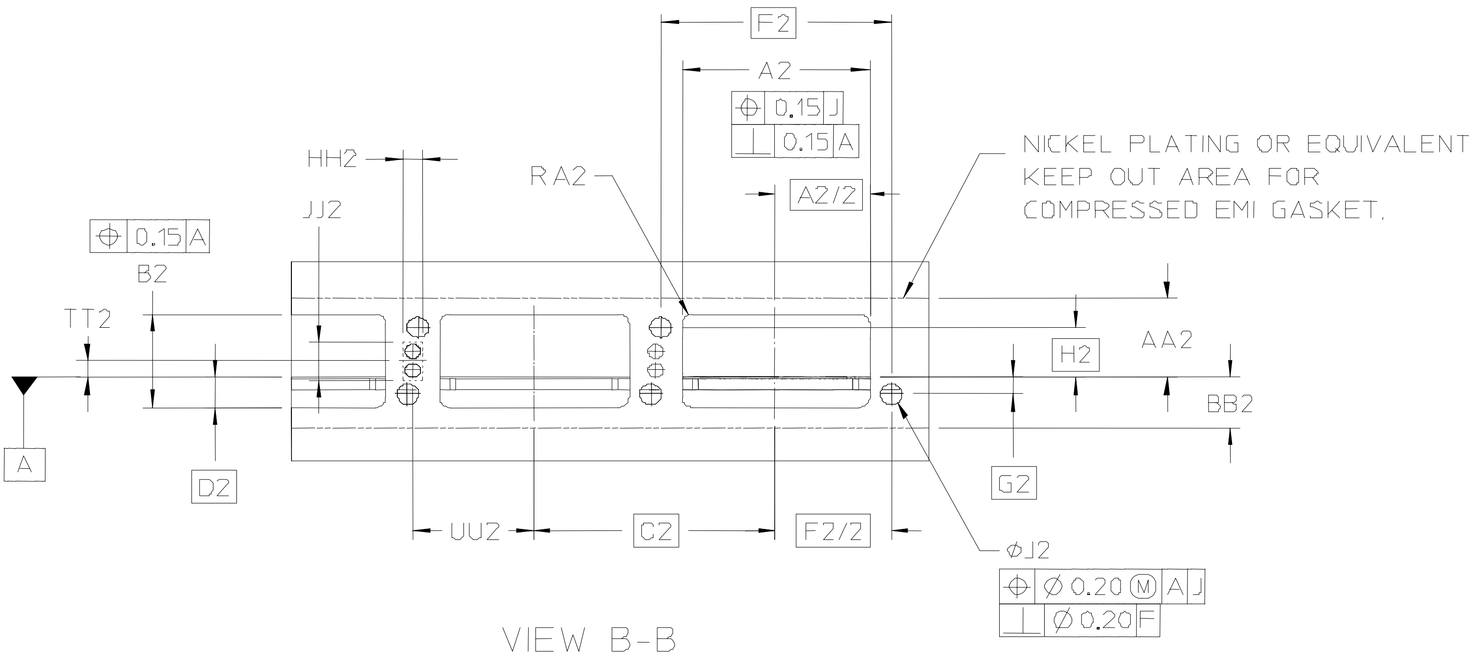
KEY	VALUES mm / inch		TOLERANCE mm	COMMENTS
A1	51.3	2.020	±0.20	Width of Bezel overall
B1	22.4	0.882	± 0.20	Height of Bezel overall
C1	45.5	1.791	BASIC	Distance between captive screws in 'X' axis (Horizontal)
D1	3.70	0.136	BASIC	Datum 'E' to lower captive screw
E1	20.75	0.817	Maximum	Extension of captive screw
F1	36.0	1.417	± 0.20	Width of Transceiver body
G1	17.4	0.685	± 0.20	Height of Transceiver body
H1	8.15	0.331	± 0.20	Datum 'E' to top of Over-hanging Ledge
J1	3.05	0.120	± 0.25	Datum 'E' to centerline of Transceiver PCB
K1	(121.0)	4.764	REF	Length of Transceiver overall minus protruding captive screw heads
L1	5.00	0.197	± 0.20	Length of captive screw from Datum 'D' to end of threaded end
M1	1.5	0.059	± 0.20	Thickness of Over-hanging Ledge
N1	5.8	0.228	± 0.20	Datum 'D' to front of Transceiver Bezel
P1	4.07	0.160	Minimum	Slot or channel formed by Interposer to accommodate Customer PCB range. Use of an Interposer spring is not a requirement of this specification.
Q1	4.65	0.183	± 0.20	Protrusion of side flange on Transceiver Bezel
R1	7.12	0.280	± 0.20	Height of side flange on Transceiver Bezel
S1	29.5	1.161	± 0.20	Width of Transceiver slot to accommodate rail or Customers PCB
T1	5.42	0.213	BASIC	Datum 'E' to Bottom of Transceiver
U1	(11.98)	0.481	REF	Datum 'E' to Top of Transceiver
V1	7.92	0.312	± 0.20	Datum 'E' to Bottom of Transceiver Bezel
W1	11.10	0.437	± 0.20	Datum 'B' to end of protruding Transceiver PCB
Y1	102.20	4.024	± 0.20	Datum 'D' to Datum 'B'
Z1	4.0	0.157	± 0.20	Datum 'B' to end of side protective shroud to mate with EMI/Conn. Shield
AA1	3.0	0.118	± 0.50	Datum 'B' to end of 45° chamfer
BB1	(115.2)	4.535	REF	Length of Module from Datum 'D' to rear Over-hanging Ledge
CC1	13.0	0.512	± 0.50	Datum 'B' to end of Over-hanging Ledge for EMI Plating
DD1	13.96	0.550	BASIC	Distance between captive screws in 'Y' axis (Vertical)
EE1	10.0	0.394	Minimum	Datum 'B' end of recess for insertion clearance
FF1	10.48	0.422	± 0.50	Datum 'E' to Top of recess for insertion clearance
GG1	20.0	0.787	Minimum	Length of Transceiver side wall for EMI plating
HH1	0.25	0.01	Basic	Datum 'A' to Datum 'E'
JJ1	29.2	1.150	± 0.10	Width of Transceiver PCB
KK1	3.0	0.118	N/A	Hole for 3mm screw Thumbscrew, tapped or clearance
LL1	25.8	1.016	Maximum	Length of Thumbscrew
RA1	1.25	0.049	Minimum	External radius or chamfer of Transceiver
RB1	1.5	0.059	Maximum	Internal radius or chamfer on exterior flange of Transceiver Bezel

Fig 5. Front Panel Opening and Host PCB

Refer to Table 2 for Dimensions



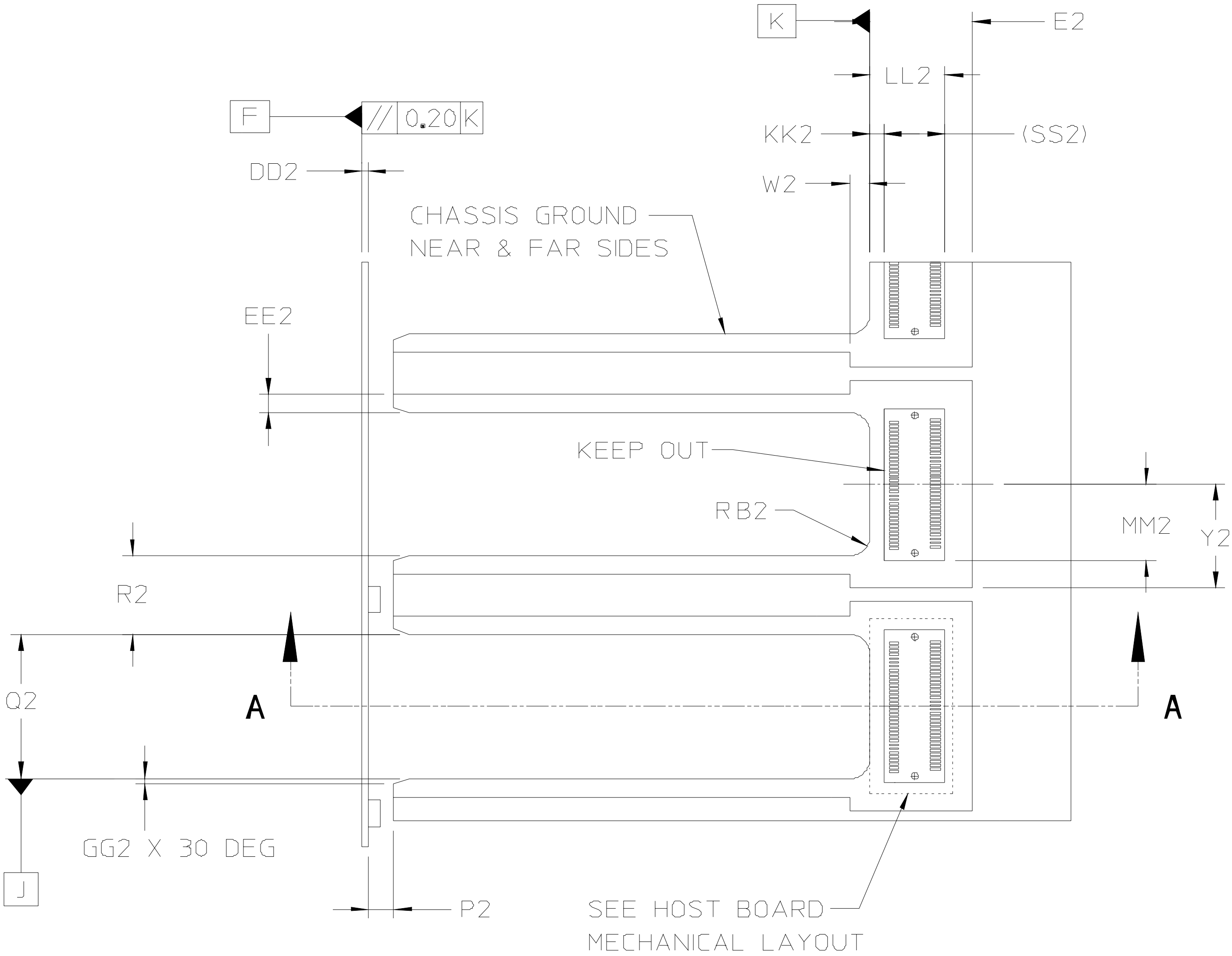
CROSS SECTION A-A
CUSTOMERS PCB AND FACEPLATE



VIEW B-B
CUSTOMERS PCB AND FACEPLATE
REFER TO CROSS SECTION AA

Fig 5(cont'd)

Refer to Table 2 for Dimensions



<u>PLAN VIEW CUSTOMERS PCB</u>

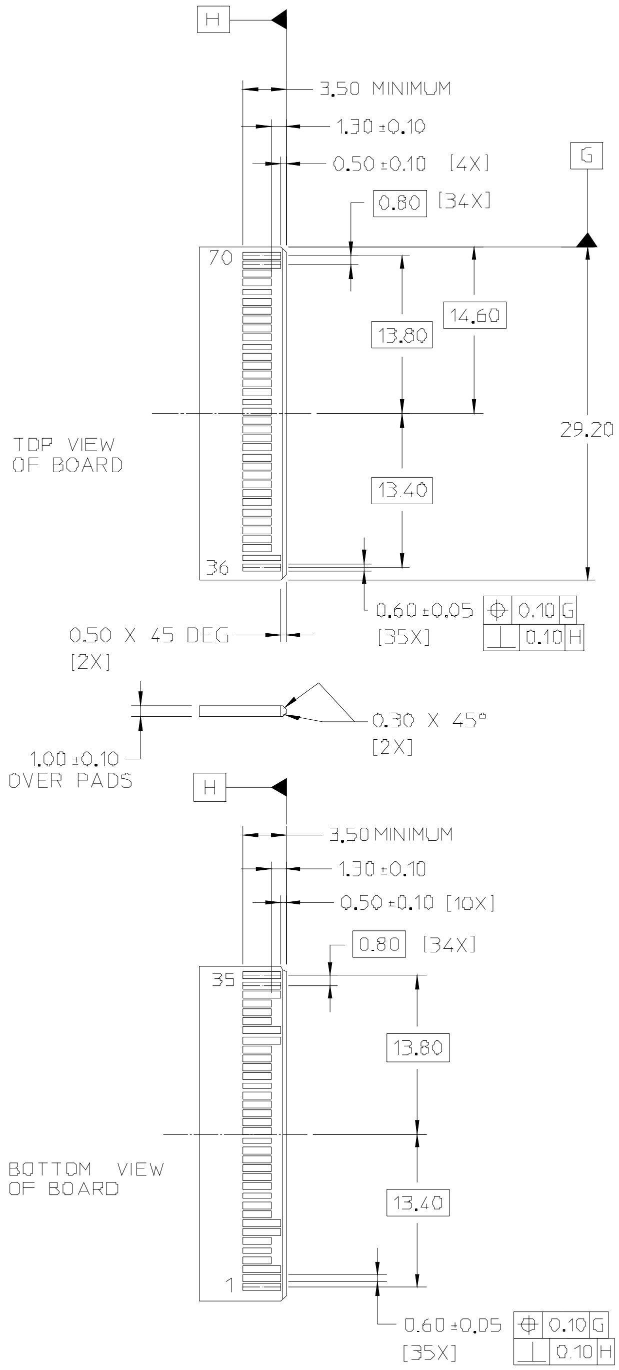
Table 2 Front Panel Opening and Host PCB Dimensions

KEY	VALUES mm / Inch		TOLERANCE mm	COMMENTS
A2	37.0	1.457	± 0.20	Width of cut-out of Customers sheet metal Faceplate
B2	18.6	0.732	± 0.20	Cut-out in Customers sheet metal Faceplate 'Y' Axis (Vertical)
C2	47.47	1.869	BASIC	Minimum Spacing of Modules in 'X' Axis (Horizontal)
D2	5.77	0.227	BASIC	Datum 'A' to bottom cut-out of the Customers sheet metal Faceplate
E2	20.59	0.811	± 0.30	Datum 'K' far side of Chassis Ground
F2	45.50	1.791	BASIC	Distance between holes for captive fastener in 'X' Axis (Horizontal)
G2	3.45	0.136	BASIC	Datum 'A' to lower mounting hole in Customers sheet metal Faceplate
H2	10.51	0.414	BASIC	Datum 'A' to upper mounting hole in Customers sheet metal Faceplate
J2	4.24	0.167	-0.0/+0.08	Diameter of hole for Self Clinching Nut
K2	101.6	4.00	± 0.50	Datum 'K' to front of Customers sheet metal Faceplate Datum F
L2	2.36 / 3.62	0.093/0.143	N/A	Customers PCB thickness range
M2	16.50	0.650	± 0.20	Datum 'K' to back of Keep-out for EMI Compliant Shield
N2	37.00	1.457	± 0.20	Width of inside surface of Connector/EMI Shield
P2	6.35	0.250	± 0.50	Distance from edge of customers PCB to inside surface of Customers S/M Faceplate
Q2	30.5	1.201	± 0.20	Width of Slot in Customers PCB
R2	16.72	0.658	Minimum	Width of support on Customers PCB
V2	9.00	0.354	BASIC	Datum 'K' to Connector mounting hole
W2	4.00	0.157	± 0.20	Datum 'K' to front keep-out pad for EMI Shield
Y2	22.30	0.878	± 0.20	Datum 'J' to side keep-out pad for EMI Shield
AA2	16.2	0.638	Minimum	Datum 'A' to upper Keep-out on Customers sheet metal Faceplate
BB2	9.2	0.362	Minimum	Datum 'A' to lower Keep-out on Customers sheet metal Faceplate
CC2	8.90	0.350	± 0.20	Datum 'A' to Top of Keep-out for EMI Compliant Shield
DD2	0.63 / 2.00	0.025/0.079	N/A	Thickness of Customers sheet metal Faceplate
EE2	4.00	0.157	Minimum	Width PCB Grounding; Proposed: Immersion Gold on Nickel; Near and Far side
FF2	1.55	0.061	± 0.05	Hole Diameter for mounting Connector
GG2	3.00	0.118	± 0.20	Lead in Chamfer on Customers PCB
HH2	4.00	0.157	± 0.30	Width of reserved space for LED bank
JJ2	7.00	0.275	± 0.30	Height of reserved space for LED bank
KK2	2.90	0.114	± 0.30	Datum 'K' to front of reserved space for Connector Pads
LL2	15.00	0.590	± 0.30	Datum 'K' to back of reserved space for Connector Pads
MM2	16.30	0.642	± 0.30	Datum 'J' to side of reserved space for Connector Pads
QQ2	5.90	0.232	Maximum	Datum 'A' to top of Connector
RR2	(12.83)	(0.505)	REF	Datum 'A' to top of cut-out in Customers Faceplate
SS2	(12.1)	(0.476)	REF	Depth of surface mount connector keep-out area.
TT2	3.50	0.138	BASIC	Height from Datum 'A' to centerline of LED bank
UU2	23.7	0.933	± 0.50	Distance from centerline of Customers Slot to centerline of LED bank
RA2	1.25	0.049	Maximum	Radius of opening in Customers sheet metal Faceplate
RB2	4.00	0.157	Maximum	Radius on Cut-out on Customers PCB

8.1 Transceiver Printed Circuit Board

A typical contact pad plating for the printed circuit board is 0.38 micrometers minimum hard gold over 1.27 micrometers minimum thick nickel. Other plating options that meet the performance requirements are acceptable. See Fig 17 for electrical signal pin out.

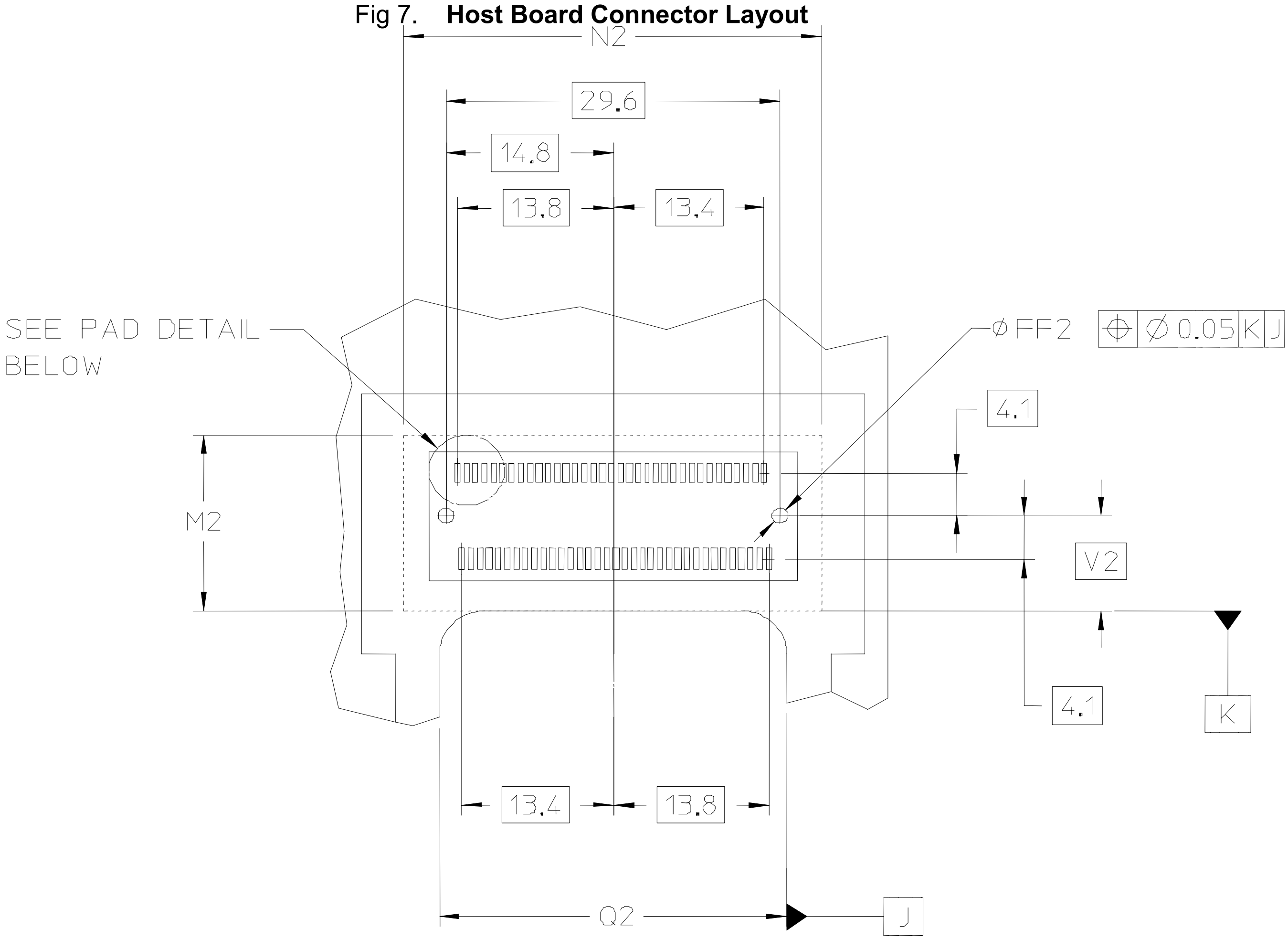
Fig 6. Transceiver Printed Circuit Board Connector

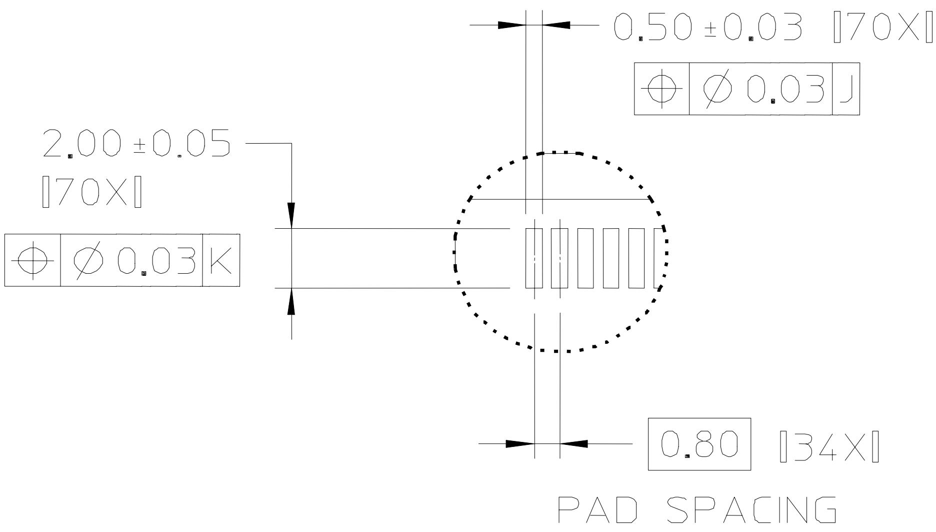


8.2 Host Board Mechanical Layout

See Fig 18 for electrical signal pin out.

Fig 7. **Host Board Connector Layout**





PAD DETAIL
Scale 4:1

8.3 Electrical Connector

See Fig 18 for electrical signal pin out.

Fig 8. Connector Drawing

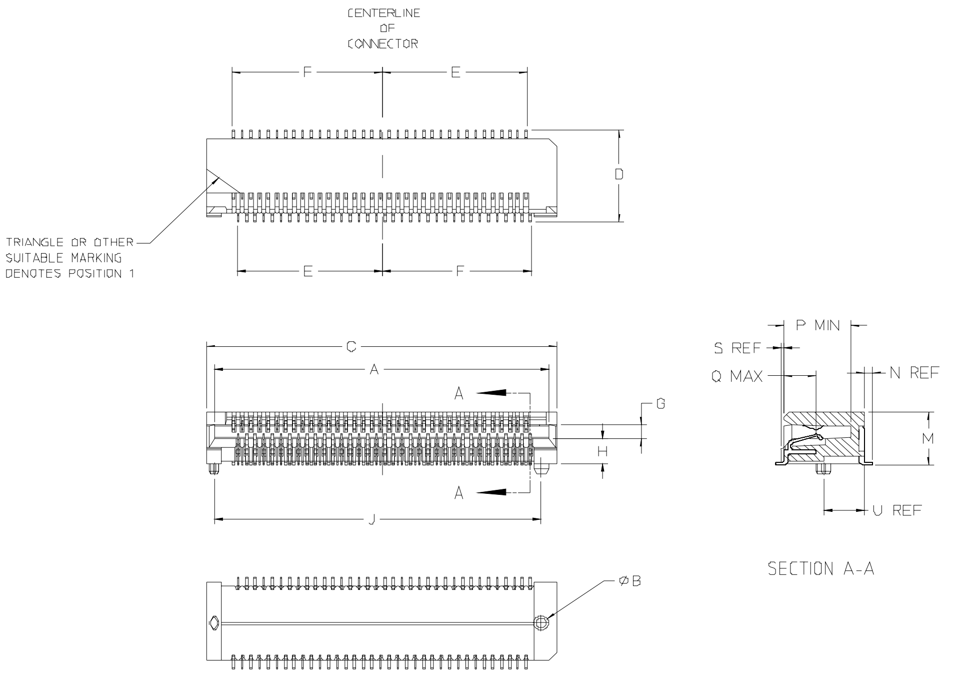


Table 3 Connector Dimensions

Key	Dim. (mm)	Tolerance	COMMENTS
A	29.4	±0.08	Connector card slot
B	1.4	±0.05	Guide pin diameter
C	31.2	Maximum	Connector width
D	9.2	Maximum	Connector Length
E	13.5	Reference	Distance from centerline of connector to outer contact
F	13.9	Reference	Distance from centerline of connector to outer contact
G	1.35	Maximum	Connector card slot height
H	2.6	Minimum	Height from bottom of connector to bottom of card slot
J	29.6	TP	Distance between guide pins
K	0.9	Reference	Diamond guide pin width, NOT SHOWN
L	1.4	±0.05	Diamond guide pin length, NOT SHOWN
M	5.9	Maximum	Connector height
N	0.8	Reference	Length of solder leads past housing, front and rear
P	6.0	Minimum	Depth of card slot from front face of housing
Q	3.0	Maximum	Depth of contact point from front face of connector
R	0.7	±0.01	Size of chamfer on top of connector, NOT SHOWN
S	0.3	Reference	Distance boss extends past front face of connector
T	0.6	Minimum	Size of chamfer at entry of card slot, all around, NOT SHOWN
U	4.5	Reference	Length from centerline of guide posts to end of solder lead

8.4 Optical Interface

The objective of this section is to specify the optical connector interface to sufficiently insure performance, inter-mateability and maximum supplier flexibility.

8.4.1 Optical Plug:

The optical interface shall use a duplex SC optical plug that conforms to IEC 61754-4. Only the floating duplex style connector plug shall be used. Rigid SC duplex connectors shall not be used. Connector keys are used for transmit / receive polarity.

NOTE: Floating Duplex SC Connectors use two simplex connectors and mechanically couple them together to create 1 connector that retains both, but allows both connectors to 'float', within the specified tolerance.

8.4.2 Optical Receptacle:

The SC Duplex Receptacle shall conform to the requirements of IEC 61754-4with the following clarification:
The distance between the centerline of the active optical bores (ref DB) shall be 12.25/13.15mm to match the floating duplex SC optical plug (ref Duplex optical plug table Note 8).

Increasing this tolerance avoids the restrictive manufacturing tolerance associated with rigid SC connectors.

8.5 Mechanical Forces

The following limits should be observed when designing for, or using, XENPAK transceivers:

Maximum insertion force = 80 N
(Includes connector, interposer and connector shield ground spring)

Maximum extraction force = 50 N

Minimum retention force (with screws engaged) = 130 N

Fastener Torque: 0.1 Nm (3mm captive screw)

8.6 Transceiver and Connector Durability

The following life ratings should be observed when designing for, or using, XENPAK transceivers and their associated connectors:

Minimum mate/de-mate cycles for transceiver = 50 cycles

Minimum mate/de-mate cycles for 70-pin connector = 100 cycles

9 XENPAK Thermal Requirements

9.1 Maximum power dissipation

Transceivers with 850nm or 1310nm PMD will dissipate a maximum of 6W.
Transceivers with 1550nm PMD will dissipate a maximum of 10W.

9.2 Maximum case temperature

Maximum case temperature for a XENPAK module is 70 C. Case temperature is as defined in IEC 60950 section 4.5.1 and table 4B

Maximum case temperature of 70°C is specified for systems with 8 or fewer adjacent 850nm or 1310nm modules.

Maximum case temperature of 70°C is specified for systems with 4 or fewer adjacent 1550nm modules.

Case temperature is not specified for systems with mixed PMD types (850/1310/1550nm). Individual characterization of systems with mixed PMD types is recommended.

See Appendix 1A for recommended test parameters used in verification of module thermal performance.

10 XENPAK Electrical Interface

A XENPAK module will be functionally operational within 5 second of insertion. Parametric performance (such as laser line width) may depend on thermal stabilization of the module and may take substantially longer and will depend on the thermal environment imposed by the host.

10.1 Power Supplies and Hot Swapping

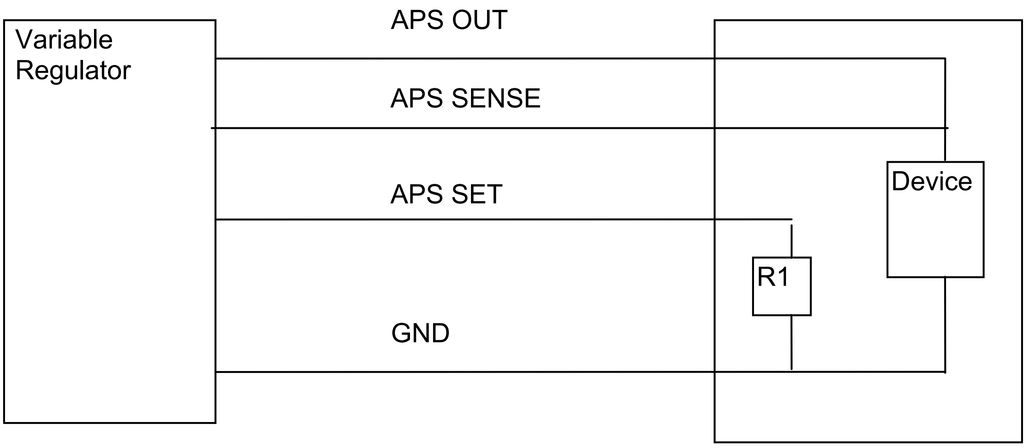
5.0V, 3.3V and an Adaptable Power Supply rail (APS) should be supplied to a XENPAK transceiver through the transceiver connector. During module insertion chassis ground connects first to the customer chassis via the chassis areas defined in **Fig 5** on the host board. The first electrical connector pins to make contact are Electrical Ground and APS power followed by VCC and Signal contacts. The 10G transceiver should tolerate biasing of signal contacts in the absence of VCC.

10.2 Grounding

Chassis and electrical ground will be DC-isolated. They may be connected in the host chassis at the option of the chassis designers.

10.3 Adaptable Power Supply

Fig 9. Adaptable Power Supply



The Back-plane will provide an adaptable power supply capable of adjusting from a high of 1.8 volts to a low of 0.9 volts.

The XENPAK module shall support a voltage sense pin for the APS on the “APS Sense” pin. The XENPAK module shall incorporate a resistor R1, between the “APS Set” pin and ground. Resistor values, corresponding to the required voltage, shall be as in Table 4.

If the pin used for APS SET is shorted to ground on the module, the APS will default to a fixed 1.8 volts.

The signal contact pin #14 “MOD DETECT” may be used to enable the APS power when the module is installed. The host design may also take control of the APS supply enable pin via software or some other mechanism.

The Adaptable supply can compensate for undesired voltage drops across the host PCB the XENPAK connector and potentially inside the XENPAK module itself (implementation dependent).

Because the APS sense does not compensate for voltage drops on the ground plane and ground pins of the connector, it is important that the ground path has a very low voltage drop, 1% is used in the tolerance analysis.

The host will provide < 200 mV to the adaptable voltage rail when no XENPAK module is installed and will ramp up to the requested voltage and be within specification within 500 ms of full insertion.

The APS is intended to default to a low voltage output if any single pin makes a poor connection, specifically:

- If the APS SET pin is connected and the APS Sense pin is open, the APS supply will put out near zero volts due to the 500 Ohm pull-up resistor to 3.3 volts (see Fig 10).
- If the APS Sense is connected and the APS SET connection is open,, the supply defaults to low voltage of 0.8 volts.
- If both the APS SET and APS Sense connections are open, the APS supply will put out near zero volts.

- The APS supply leads are elongated to prevent a condition where the SENSE lead connects before the APS supply leads and pulls down the SENSE pin resulting in an instantaneous high voltage from the APS, before the module is fully seated.

10.3.1 Adaptable Power supply reference

The APS supply on the host will regulate the APS voltage such that the voltage on the network labeled "Vfeedback" in Fig 10 becomes nominally 0.8 volts unless an APS voltage or current limiting
condition takes priority. The resistors in the following table are calculated using resistors available as 1% values. For tolerance purposes, it is recommended that 0.1% resistors are used to provide additional tolerance margin although 1% may be suitable for some applications. These values are subject to change after a host back-plane is built and tested.

Table 4 Resistor Values for APS operation.

Vnom volts	R1 ohms
0.9	6810
1	3160
1.1	1820
1.2	1180
1.3	806
1.4	536
1.5	348
1.6	210
1.7	97.6
1.8	0

The resistor values given in Table 4 place the nominal set-point slightly high, to help compensate for some of the anticipated ground plane drop.

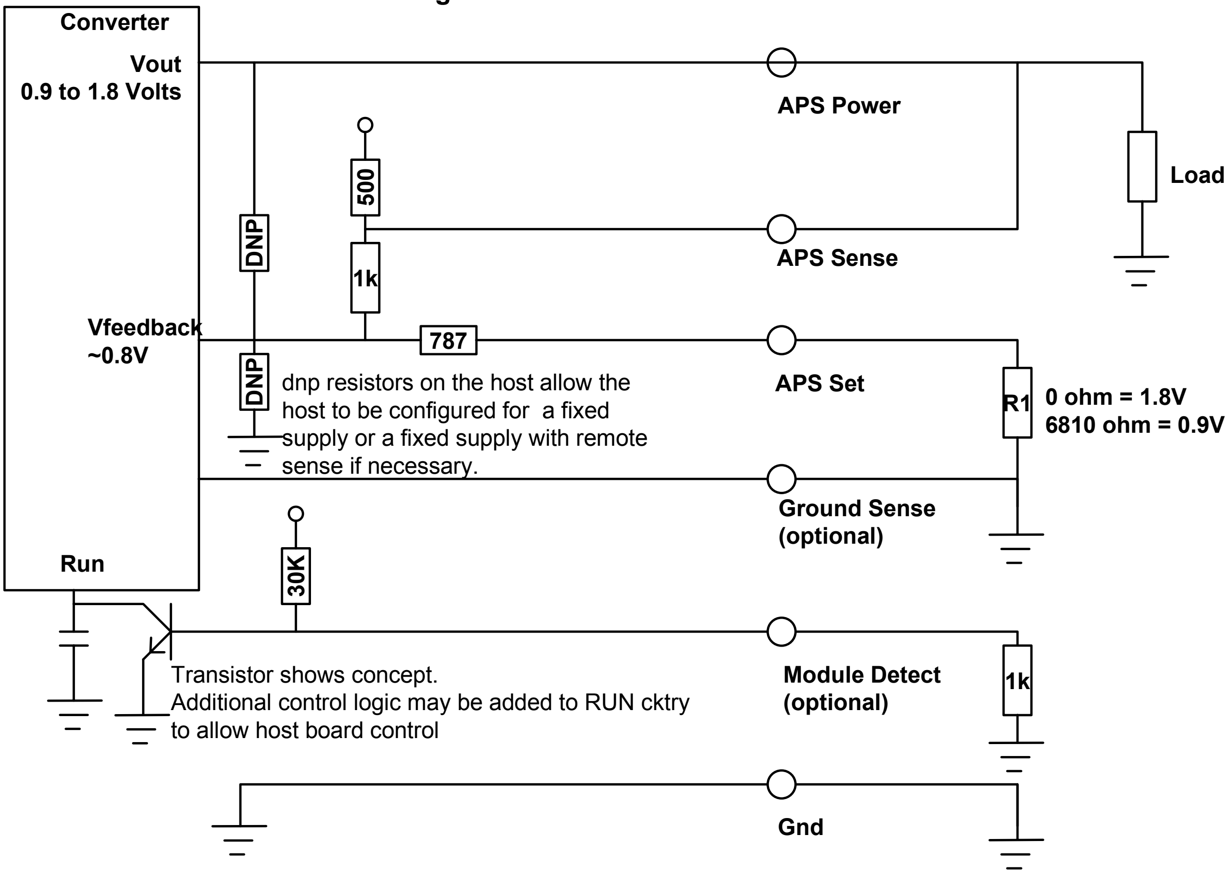
Table 5 Recommended Tolerances (+/-)

Supply precision	1.5%
Supply load regulation	0.3%
Ground plane and ground connector drop	1.0%
Resistor tolerances using 0.1% parts	0.3%
Margin	0.9%
Total APS tolerance (+/-)	4.0%

10.3.2 Voltage calculation

The circuit shown in Fig 10, depicts conceptually the design used to generate the APS voltage. Exact implementation and component values are not mandatory on the host. The APS implementer is responsible for ensuring that the XENPAK module is supplied in a manner which conforms to the APS tolerances stated in Table 5 for any given resistance between the module set pin and module ground.

Fig 10. APS Schematic



10.3.3 Current capability of the APS

The APS will provide from 0.1 to 1.8 amperes and will current limit at typically 2 to 4 amperes.

10.3.4 Adaptable Power Supply Specs/Requirements

The host PCB will provide a steady state voltage on the adaptable voltage power conforming to the specifications given in Table 5.

Table 6   APS Tolerances (+/-)

APS steady state RMS ripple	<40mV rms
APS tolerance for a given resistance from APS set to ground.	+/- 3%
APS max overshoot after insertion/host power up	3% of V steady state
APS min rated current	0.1 Amps
APS maximum rated current for any voltage	1.8 Amps
APS current limit	2 ->4 Amps
XENPAK total capacitance of transceiver APS power pins	<200 uF

10.4 Fixed Voltage Supply Specs and Inrush Currents

These specifications shall be applicable to the fixed 3.3V and 5.0V supply rails.
The inrush current on any fixed supply rail during hot plug or power up in host of a XENPAK module shall be limited by the XENPAK module to assure a maximum rate of change de fined in Table 7. The peak inrush currents to any supply rail shall not exceed the steady state currents for that rail by more than 50%.

Ramp up time controlled by the XENPAK module shall allow operation within 5 seconds after the adaptable power supply back-plane has stabilized as required above.

Table 7 Fixed Power Rail Tolerances (+/-)

Steady State Voltage Accuracy	+/-5% of rated
Steady state RMS ripple (max)	40mV rms
Stabilization time to rated tolerance (max)	< 500 ms
Inrush current during hot plug max	50 mA/ms
Inrush current (per power pin) max	<0.75A (150% x 0.5A steady state rating)

A XENPAK module inserted in this system shall inject <20mV rms ripple onto any fixed voltage rail when supplied from a “near ideal” voltage source followed by a 5 ohm series resistor.

10.4.1 Hot Swap and Transceiver Power-On-Reset Definition

When a 10G transceiver is inserted the ramp rate of supply current must also comply with the specification in Table 8. Control of inrush current (as shown in Fig 14) should be internal to the XENPAK transceiver
The 10G transceiver shall achieve a stable state of normal operation after mechanical insertion at time, t=0 according to the following specification.

Table 8 Power on Reset characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Icc Peak Inrush	Icc_{PEAK}	-	-	50	%
Icc Ramp rate	dICC/dt	-	-	50	mA/ms
Initialisation Time	t_{init}	-	-	5	s

10.4.2 Low Power Start-up (LPS) Mode

Low power startup is an optional feature of XENPAK modules. A transceiver will indicate it’s LPS ability by setting bit 0 of the Optional Capability Register (see Section 10.12.21) to 1 if implemented and 0 otherwise.

If LPS is implemented the module will only initialize the MDIO-functionality, and limit the power consumption to a fraction of normal levels, typical less than 1W.

For LPS to be invoked, the system shall pull the signal TX ON/OFF (pin 12) low, for all the empty module slots and hold it low after a module is inserted, until the system reads the modules registers and establishes what it’s respective thermal and power needs. The system can thereby establish if the newly inserted module causes it to exceed it’s thermal or power supply capacity and to reject the module, by holding it in a low power state until it does. Otherwise the system enables the module to commence normal operation, by raising the TX ON/OFF signal.

The XENPAK NVR contains pre-programmed power supply requirement information for an LPS enabled module, as detailed in Table 1.

The LPS feature is particularly relevant to longer reach XENPAKs which may load power supplies and cooling more than shorter reach parts, but which are not typically inserted into all ports of a line card.

Four measurements are made on a representative sample of part of a representative build standard in the MSA thermal test chamber described in Section 12.

Specific parameters are:

- 5V Stressed Environment Reference (100% = 1A)
- 3.3V Stressed Environment Reference (100% = 2A)
- APS Stressed Environment Reference (100% = 2A)
- Nominal APS Voltage

Under the following conditions:

One module is inserted in the test fixture middle slot (number four or five) with the remaining front openings closed with blanking plates. An inlet air temperature of 50°C and airspeed of 2 m/s shall be used for the single stressed environment current reference measurement on each rail.

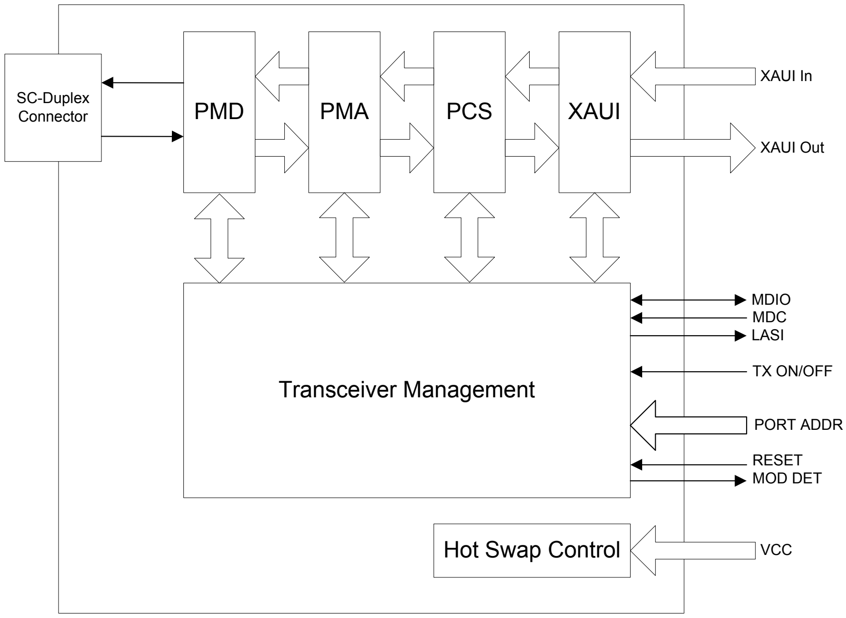
Mandatory reference values are written into the NVR Basic Space in the format shown in Table 1.

10.5 Transceiver Monitoring

Contacts are available on the module connector for Link Alarm Status Interrupt (LASI).
A module detect pin allows hardware detection of a module when it is inserted into a customer chassis. This pin is pulled through 1kΩ to GND inside the module and can be used to drive an interrupt for polling-free module detection.

The 2-wire Management Data I/O interface (802.3ae Clause 45) is mandatory in the XENPAK MSA. MDC provides clocking for the data that is passed on the MDIO line. Five further pins allow for loading of a Port Address (PRTAD0-4) into the module.

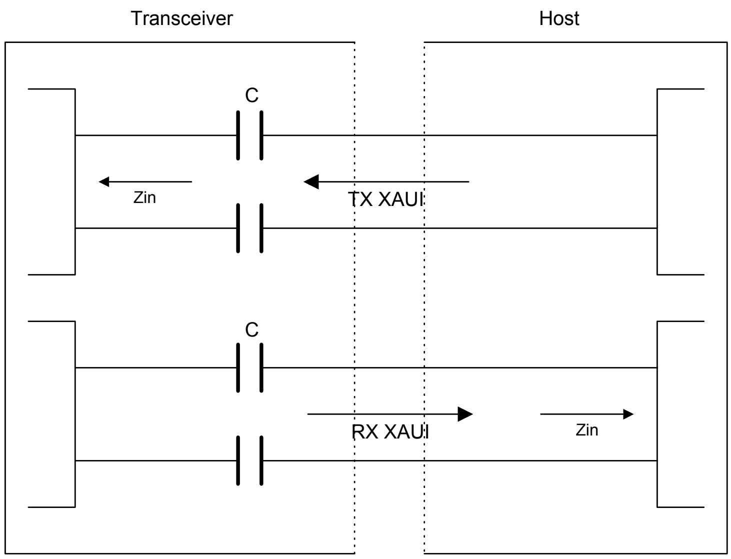
Fig 11. Functional Diagram of Typical XENPAK Style Transceiver



10.5.1 High Speed Signals

The XAUI transmit and receive data complies with IEEE802.3ae Clause 47 electrical specification, which should be referenced for actual values. AC coupling is provided inside the module for both transmit and receive directions as indicated in Fig 12. For clarity only one TX and RX XAUI lane is shown. The impedance of Zin is 100 Ohms differential.

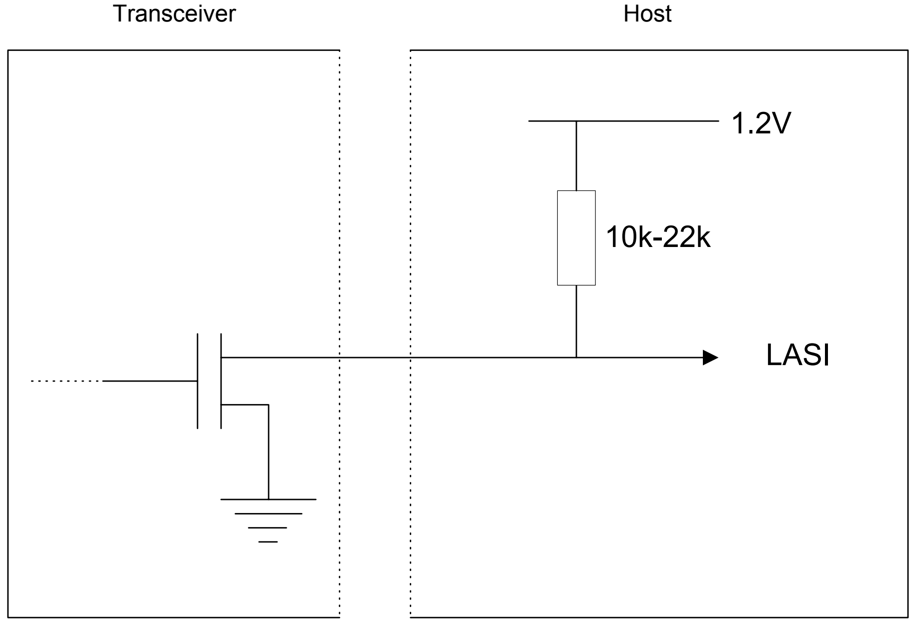
Fig 12. High Speed Signals



10.5.2 Low Speed Signals

Low Speed Signals, as indicated in Table 11, are open drain compatible to permit wired 'OR' connections. Pull up resistors are provided in the transceiver or on the host board according to Fig 13.

Fig 13. Example of Low Speed Output Configuration



Example of one termination configuration only is given. See Table 11 and Table 12 for exact description of terminations required for each signal.

Table 9 Electrical Characteristics of Low Speed Interface

Parameter	Min	Typ	Max	Units	Notes
$V_{IL(MAX)}$	-	-	0.36	V	1.2V CMOS
$V_{IH(MIN)}$	0.84	-	1.25	V	1.2V CMOS
Capacitance	-	-	320	pF	Maximum Fan-out of 32. 10pF per port
Pull Up Resistance	10k		22k	Ω	

10.5.3 Initialisation and Reset

After successful plug in and initialization sequence the transceiver should clear MDIO Bit register N.0.15 (Where N= any implemented device). A timing diagram is in Fig 14.
The transceiver may be reset in situ using the hardware reset pin or MDIO register bit 1.0.15 according to Table 10.
When reset using the hardware reset pin or by setting Bit 15 in MDIO register 1.0 the transceiver should initialize and then clear MDIO Bit N.0.15.

Fig 14. Initialisation and Hot Swap Timing Diagram

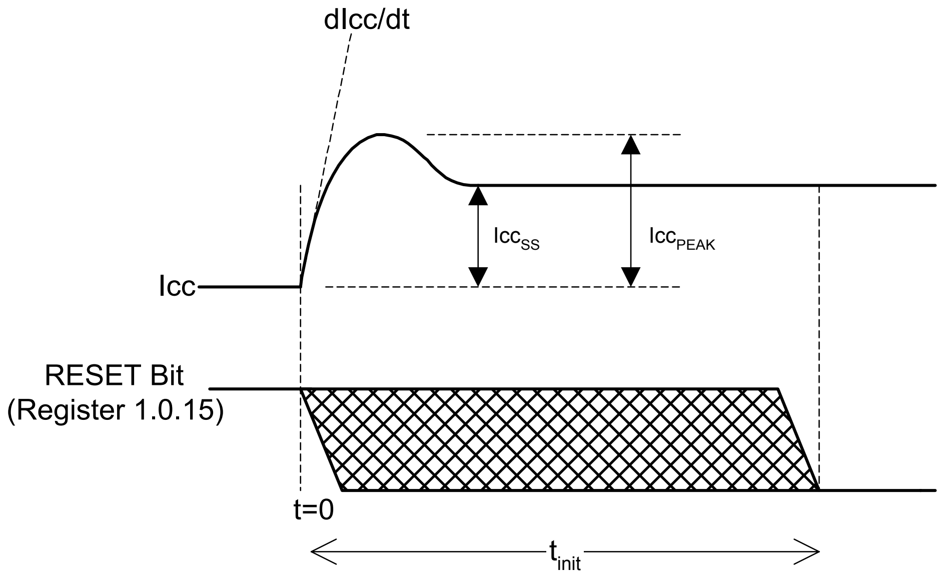


Table 10 Relationship between the TRANSCEIVER RESET pin and MDIO Reset Bit

RESET Pin	MDIO Register Condition 1.0.15	Transceiver Behavior
1	0	Normal operation
0	0	Transient state between RESET PIN low and 1.0.15 getting set
1	1	Reset State
0	1	State assumed shortly after Transceiver reset pin pulled low.

10.5.4 Tx On/Off

The timing relationship between Tx on/off and the optical output is shown in Fig 15. The optical output will turn off within 100us of Tx ON/OFF being pulled low.

Fig 15. Tx Off to Optical Output timing, normal operation.

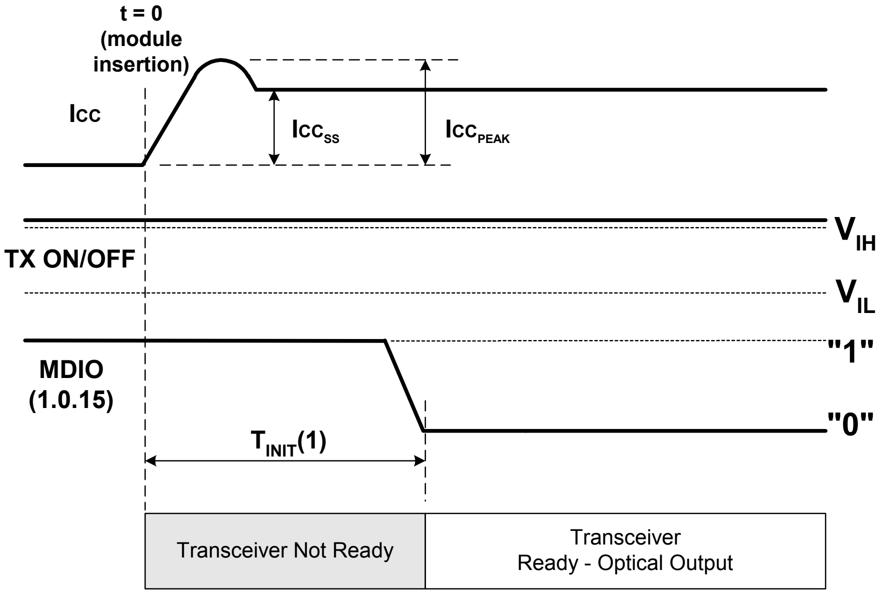
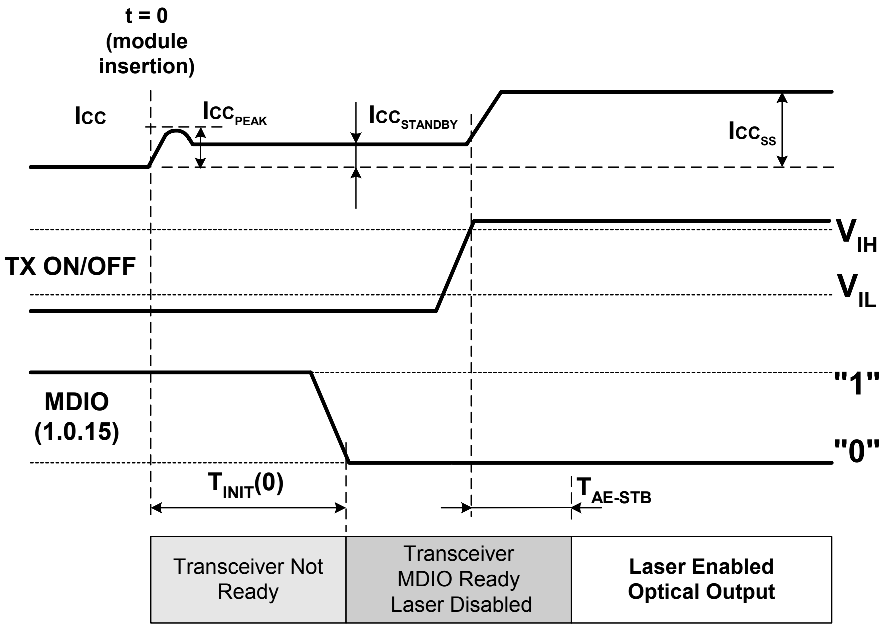


Fig 16. Tx Off to Optical Output timing.
See "Low Power Start-up", Section 10.4.2



10.6 Multiple PMD Support

This MSA aims to accommodate all four 10Gb PMDs and both LAN and WAN PHY variants (apart from LX4 which is not defined for WAN PHY).
LX4 Wavelengths will always be mapped to the XAUI per IEE 802.3ae, Clause 53, Table 53–5.

10.7 Electrical Connector

The XENPAK connector is a 70-way two-row connector, similar in style to the 20-way SFP connector. (examples are TycoAMP Part No. 1367337-1 and Molex Part No. 74441-0003, or equivalent. Exact choice of connectors may depend on environment, contact manufacturer for detail)
The 10G transceiver PCB forms one mating half of the connector.
Pin definitions are listed in Table 11 and Table 12.
Mechanical dimensions for the transceiver Electrical Pad Layout and Host board are shown in Fig 6, Fig 7 and Fig 8,. Signal layouts are shown in Fig 17 and Fig 18.

10.7.1 ESD

Human Body Model survivability is recommended to a minimum of 500V, measured to MIL STD 883 Method 3015.1. End of row contacts on the transceiver connector are ground connections so that I/O pins will not be subjected to the highest Charged Device Model (CDM) ESD test voltage, if applicable.

Table 11 Pin Function Definitions (Lower Row)

Pin No	Name	Dir	Function	Notes
1	GND		Electrical Ground	1
2	GND		Electrical Ground	1
3	GND		Electrical Ground	1
4	5.0V		Power	2
5	3.3V		Power	2
6	3.3V		Power	2
7	APS		Adaptive Power Supply	2
8	APS		Adaptive Power Supply	2
9	LASI		Open Drain Compatible 10K-22K pull up on host. Logic High: Normal Operation Logic Low: LASI Asserted	4
10	RESET	I	Open Drain compatible. 10-22K pull-up on transceiver Logic high = Normal operation Logic low = Reset Minimum reset assert time 1 ms	4
11	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
12	TX ON/OFF	I	Open Drain compatible. 10-22K pull-up on transceiver Logic high = Transmitter On (capable) Logic low = Transmitter Off (always)	4
13	RESERVED		Reserved	4
14	MOD DETECT	O	Pulled low inside module through 1k	
15	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
16	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
17	MDIO	I/O	Management Data IO	4, 5
18	MDC	I	Management Data Clock	4, 5
19	PRTAD4	I	Port Address Bit 4 (Low = 0)	4
20	PRTAD3	I	Port Address Bit 3 (Low = 0)	4
21	PRTAD2	I	Port Address Bit 2 (Low = 0)	4
22	PRTAD1	I	Port Address Bit 1 (Low = 0)	4
23	PRTAD0	I	Port Address Bit 0 (Low = 0)	4
24	VEND SPECIFIC		Vendor Specific Pin. Leave unconnected when not in use.	8
25	APS SET		Feedback input for APS	
26	RESERVED		Reserved for Avalanche Photodiode use.	8
27	APS SENSE		APS Sense Connection	
28	APS		Adaptive Power Supply	2
29	APS		Adaptive Power Supply	2
30	3.3V		Power	2
31	3.3V		Power	2
32	5.0V		Power	2
33	GND		Electrical Ground	1
34	GND		Electrical Ground	1
35	GND		Electrical Ground	1

Table 12 Pin Function Definitions (Upper Row)

Pin No	Name	Dir	Function	Notes
36	GND		Electrical Ground	1
37	GND		Electrical Ground	1
38	RESERVED		Reserved	
39	RESERVED		Reserved	
40	GND		Electrical Ground	1
41	RX LANE0+	O	Module XAUI Output Lane 0+	7
42	RX LANE0-	O	Module XAUI Output Lane 0-	7
43	GND		Electrical Ground	1
44	RX LANE1+	O	Module XAUI Output Lane 1+	7
45	RX LANE1-	O	Module XAUI Output Lane 1-	7
46	GND		Electrical Ground	1
47	RX LANE2+	O	Module XAUI Output Lane 2+	7
48	RX LANE2-	O	Module XAUI Output Lane 2-	7
49	GND		Electrical Ground	1
50	RX LANE3+	O	Module XAUI Output Lane 3+	7
51	RX LANE3-	O	Module XAUI Output Lane 3-	7
52	GND		Electrical Ground	1
53	GND		Electrical Ground	1
54	GND		Electrical Ground	1
55	TX LANE0+	I	Module XAUI Input Lane 0+	7
56	TX LANE0-	I	Module XAUI Input Lane 0-	7
57	GND		Electrical Ground	1
58	TX LANE1+	I	Module XAUI Input Lane 1+	7
59	TX LANE1-	I	Module XAUI Input Lane 1-	7
60	GND		Electrical Ground	1
61	TX LANE2+	I	Module XAUI Input Lane 2+	7
62	TX LANE2-	I	Module XAUI Input Lane 2-	7
63	GND		Electrical Ground	1
64	TX LANE3+	I	Module XAUI Input Lane 3+	7
65	TX LANE3-	I	Module XAUI Input Lane 3-	7
66	GND		Electrical Ground	1
67	RESERVED		Reserved	
68	RESERVED		Reserved	
69	GND		Electrical Ground	1
70	GND		Electrical Ground	1

Notes:

1) Ground connections are common for TX and RX.

2) All connector contacts are rated at 0.5A nominal.

4) 1.2V CMOS compatible.

5) MDIO and MDC timing must comply with IEEE802.3ae, Clause 45.3

7) XAUI output characteristics should comply with IEEE802.3ae Clause 47.

8) Transceivers will be MSA compliant when no signals are present on the vendor specific pins.

Fig 17. XENPAK Transceiver Electrical Pad Layout

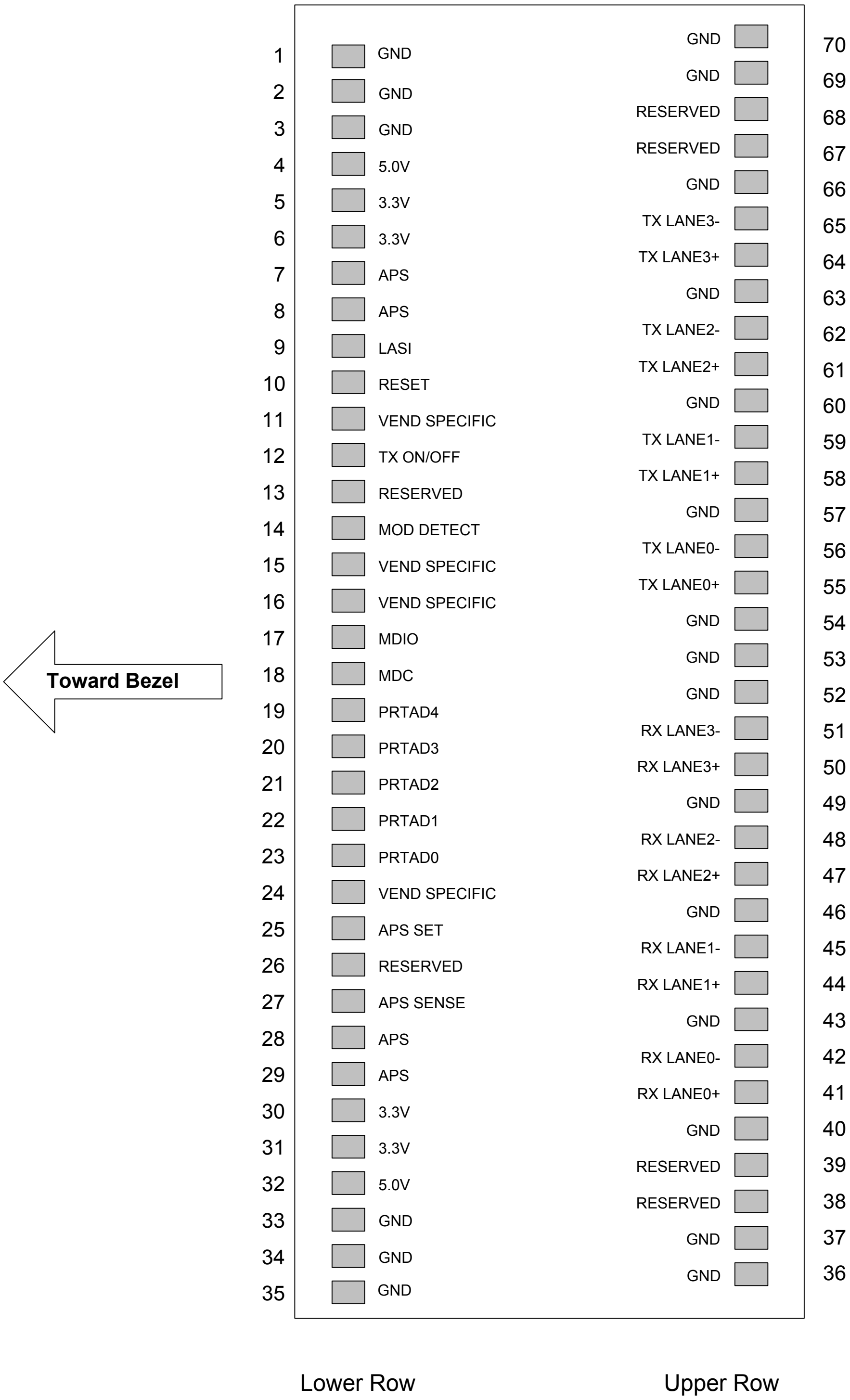
← Toward Bezel

Pin	Top of Transceiver PCB	Pin	Bottom of Transceiver PCB (as viewed through top)
70	GND	1	GND
69	GND	2	GND
68	RESERVED	3	GND
67	RESERVED	4	5.0V
66	GND	5	3.3V
65	TX LANE3-	6	3.3V
64	TX LANE3+	7	APS
63	GND	8	APS
62	TX LANE2-	9	LASI
61	TX LANE2+	10	RESET
60	GND	11	VEND SPECIFIC
59	TX LANE1-	12	TX ON/OFF
58	TX LANE1+	13	RESERVED
57	GND	14	MOD DETECT
56	TX LANE0-	15	VEND SPECIFIC
55	TX LANE0+	16	VEND SPECIFIC
54	GND	17	MDIO
53	GND	18	MDC
52	GND	19	PRTAD4
51	RX LANE3-	20	PRTAD3
50	RX LANE3+	21	PRTAD2
49	GND	22	PRTAD1
48	RX LANE2-	23	PRTAD0
47	RX LANE2+	24	VEND SPECIFIC
46	GND	25	APS SET
45	RX LANE1-	26	RESERVED
44	RX LANE1+	27	APS SENSE
43	GND	28	APS
42	RX LANE0-	29	APS
41	RX LANE0+	30	3.3V
40	GND	31	3.3V
39	RESERVED	32	5.0V
38	RESERVED	33	GND
37	GND	34	GND
36	GND	35	GND

Top of Transceiver PCB **Bottom of Transceiver PCB (as viewed through top)**

Note: Refer to Fig 6
Ground pins 1, 2, 3, 33, 34, 35, 36, 37, 69, 70 and APS power pins 7, 8, 28, 29, are extended so as to make contact first upon XENPAK insertion.

Fig 18. **10Gb Host Board Pad Layout and Names**



Note: Refer to Fig 7 and Fig 8

10.8 Management Interface

XENPAK transceivers support the MDIO interface specified in IEEE802.3ae Clause 45. In addition to the appropriate registers to support the IEEE standard there are some registers specific to XENPAK.

10.8.1 Transceiver Identification

Efficient use of XENPAK and its specific registers requires an end-user system to recognize a connected transceiver as being of the XENPAK type. The method described in section 10.8.2. utilizes the Organizationally Unique Identifier (OUI) as a means of identifying it as a XENPAK and also of communicating the device in which the XENPAK specific registers are located.
The XENPAK OUI is 00-08-BE,
For more info on OUIs see http://standards.ieee.org/regauth/oui/index.shtml

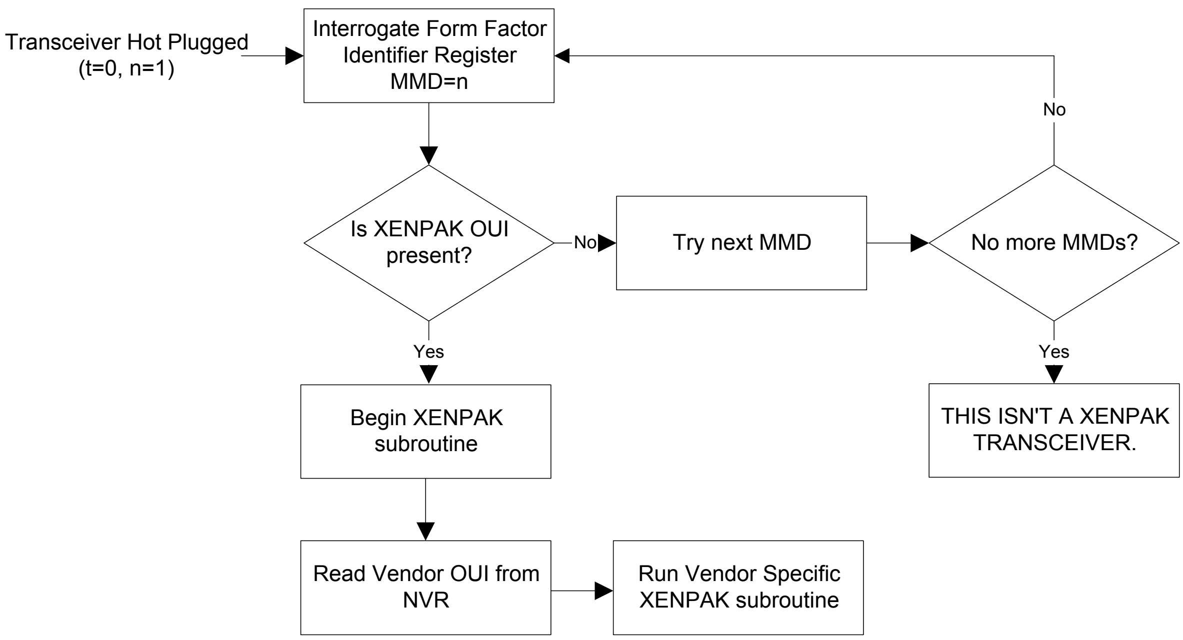
10.8.2 OUI Method

Following successful hot plugging of a XENPAK transceiver it indicates its presence by pulling module detect low and shows that it is a XENPAK transceiver by placing a XENPAK specific OUI into the
Package Identifier registers at locations D.14 and D.15, as defined in 802.3ae clauses 45.2.1.10 and 45.2.3.8. D may be device 1, 2, 3, 4, 30 or 31.

The system performs a simple search for the XENPAK OUI across devices 1, 2, 3, 4, 30 or 31. Upon finding the XENPAK OUI the system knows that the XENPAK registers reside in that device.. Once the XENPAK registers are located, and OUI indicating the transceiver manufacturer (called Vendor OUI) can be read from the XENPAK registers (see 10.12.15) and any vendor specific actions taken by software, if required.

Fig 19. shows diagrammatically how the XENPAK OUI and Vendor OUI are used. Section 10.12.14. shows the format of the XENPAK OUI and its relation to the Package Identifier registers.

Fig 19. Transceiver Identification after Hot Plugging



10.8.3 XENPAK Register Set

In addition to the standards related registers mandated by the IEEE in 802.3ae for each device, the XENPAK module shall maintain certain information in a set of non-volatile registers (NVRs) which can be read in the normal way via the MDC/MDIO management port. This memory is protected from writes by the system and is intended to be programmed at module manufacture.

The information defined for the NVRs may be required to use the module and shall have the location and format described in Table 1. Examples of information contained in the NVR include the indication of transceiver capabilities, manufacturer ID, and version number.

It should be noted that the NV Register set only uses the 8 least significant bits of the 16 bit MDIO register for data. Unlike 802.3ae registers which tend to use all 16 bits.

There is also an area of non-volatile memory in a XENPAK that can be read and written by the system.

Reads from this area are generally performed using standards MDIO reads from the specific address.

Writes to the customer area are volatile unless performed using the NVR Control/Status register, see Section 10.9 for more detail. A detailed layout of the NVR is given in Table 1 and details of it use given in 10.12.21 and 10.9

The exact implementation detail of the NVRs is beyond the scope of the MSA.

The high level layout of the XENPAK specific register areas is given in Table 13

A more detailed layout of the XENPAK non-volatile register use is given in Table 1

Table 13 XENPAK Register Set Overview

Address	# Bytes	Area Usage
0x8000	2055	NVR Control/Status
0x8001 to 0x8006		Vendor Specific
0x8007 to 0x8106		Non-Volatile Registers
0x8107 to 0x8806		Extended Vendor Specific Non Volatile area
0x8807 to 0x8FFF	2041	Reserved
0x9000 to 0x9005		LASI Control & Status
0x9006 to 0x9FFF		Reserved
0xA000 to 0xA0FF	256	Digital Optical Monitoring Functions
0xA100 to 0xA106	7	Digital Optical Monitoring Control and Status
0xA107 to 0xAFFF	3833	Reserved
0xB000 to 0xB07F	128	LSS Registers - Optional
0xB080 to 0xB07FF	1920	Reserved
0xB800 to 0xB80F	16	10 GFC Registers - Optional
0xB810 to 0xBFFF	2032	Reserved

Table 14 NVR Register Map

Field Group	Register Address Decimal	Register Address Hex	NVR Byte No.	Size	Name	Description	Value	7	6	5	4	3	2	1	0	Hex
Header	32775	8007	0	1	Version	XENPAK MSA Version supported		x	x	x	x	x	x	x	x	xx
	32776	8008	1	2	NVR_Size	NVR Size in bytes		x	x	x	x	x	x	x	x	xx
	32778	800A	3	2	Mem_Used	Number of bytes used		x	x	x	x	x	x	x	x	x
	32780	800C	5	1	Basic Addr	Basic Field Address		x	x	x	x	x	x	x	x	x
	32781	800D	6	1	Cust Addr	Customer Field Address		x	x	x	x	x	x	x	x	x
	32782	800E	7	1	Vend Addr	Vendor Field Address		x	x	x	x	x	x	x	x	x
	32783	800F	8	2	Ext Vend Addr	Extended Vendor Field Address		x	x	x	x	x	x	x	x	x
	32785	8011	10	1	Reserved			x	x	x	x	x	x	x	x	xx
Basic	32786	8012	11	1	Tcvr Type	Transceiver type	Unspecified	0	0	0	0	0	0	0	0	0
							XENPAK	0	0	0	0	0	0	0	1	1
							Reserved	x	x	x	x	x	x	x	x	xx
	32787	8013	12	1	Connector	Optical connector type	Unspecified	0	0	0	0	0	0	0	0	0
							SC	0	0	0	0	0	0	0	1	1
							LC	0	0	0	0	0	0	1	0	2
							MT-RJ	0	0	0	0	0	1	0	0	4
							MU	0	0	0	0	1	0	0	0	8
							FC/PC	0	0	0	1	0	0	0	0	10
							Pigtail	0	0	1	0	0	0	0	0	20
							Reserved	x	x	x	x	x	x	x	x	xx
	32788	8014	13	1	Encoding	Bit encoding	Unspecified	0	0	0	0	0	0	0	0	0
							NRZ	0	0	0	0	0	0	0	1	1
							FEC	0	0	0	0	0	0	1	0	2
							Reserved	x	x	x	x	x	x	x	x	xx
	32789	8015	14	2	Bit Rate	Nominal Bit Rate in multiples of 1Mb/s	Unspecified	0	0	0	0	0	0	0	0	0
							x	x	x	x	x	x	x	x	x	xx
	32791	8017	16	1	Protocol	Protocol Type	Unspecified	0	0	0	0	0	0	0	0	0
							10GbE	0	0	0	0	0	0	0	1	1
							10GFC	0	0	0	0	0	0	1	0	2
							WIS	0	0	0	0	0	1	0	0	4
							LSS	0	0	0	0	1	0	0	0	8
							SONET/SDH	0	0	0	1	0	0	0	0	10
							Reserved	x	x	x	x	x	x	x	x	xx
	32792	8018	17	10	Standards Compliance Codes	10GbE Code Byte 0	Unspecified	0	0	0	0	0	0	0	0	0
							10GBASE-SR	0	0	0	0	0	0	0	1	1
							10GBASE-LR	0	0	0	0	0	0	1	0	2
							10GBASE-ER	0	0	0	0	0	1	0	0	4
							10GBASE-LX4	0	0	0	0	1	0	0	0	8
							10GBASE-SW	0	0	0	1	0	0	0	0	10
							10GBASE-LW	0	0	1	0	0	0	0	0	20
							10GBASE-EW	0	1	0	0	0	0	0	0	40
							Reserved	1	0	0	0	0	0	0	0	80
						10GbE Code Byte 1	Reserved	x	x	x	x	x	x	x	x	xx

NVR Register Map (continued)

Basic	32792	8018	17	10	Standards Compliance Codes	SONET/SDH Code Byte 0	Unspecified	0	0	0	0	0	0	0	0	0
							S-64.1	0	0	0	0	0	0	0	1	1
							S-64.2a	0	0	0	0	0	0	1	0	2
							S-64.2b	0	0	0	0	0	1	0	0	4
							S-64.3a	0	0	0	0	1	0	0	0	8
							S-64.3b	0	0	0	1	0	0	0	0	10
							S-64.5a	0	0	1	0	0	0	0	0	20
							S-64.5b	0	1	0	0	0	0	0	0	40
							Reserved	1	0	0	0	0	0	0	0	80
						SONET/SDH Code Byte 1	Unspecified	0	0	0	0	0	0	0	0	0
							I-64.1r	0	0	0	0	0	0	0	1	1
							I-64.1	0	0	0	0	0	0	1	0	2
							I-64.2r	0	0	0	0	0	1	0	0	4
							I-64.2	0	0	0	0	1	0	0	0	8
							I-64.3	0	0	0	1	0	0	0	0	10
							I-64.5	0	0	1	0	0	0	0	0	20
							Reserved	0	1	0	0	0	0	0	0	40
							Reserved	1	0	0	0	0	0	0	0	80
						SONET/SDH Code Byte 2	Unspecified	0	0	0	0	0	0	0	0	0
							L-64.1	0	0	0	0	0	0	0	1	1
							L-64.2a	0	0	0	0	0	0	1	0	2
							L-64.2b	0	0	0	0	0	1	0	0	4
							L-64.2c	0	0	0	0	1	0	0	0	8
							L-64.3	0	0	0	1	0	0	0	0	10
							Reserved	0	0	1	0	0	0	0	0	20
							Reserved	0	1	0	0	0	0	0	0	40
							Reserved	1	0	0	0	0	0	0	0	80
						SONET/SDH Code Byte 3	Unspecified	0	0	0	0	0	0	0	0	0
							V-64.2a	0	0	0	0	0	0	0	1	1
							V-64.2b	0	0	0	0	0	0	1	0	2
							V-64.3	0	0	0	0	0	1	0	0	4
							Reserved	0	0	0	0	1	0	0	0	8
							Reserved	0	0	0	1	0	0	0	0	10
							Reserved	0	0	1	0	0	0	0	0	20
							Reserved	0	1	0	0	0	0	0	0	40
							Reserved	1	0	0	0	0	0	0	0	80
						10GFC Code Byte 0	Reserved	x	x	x	x	x	x	x	x	xx
						10GFC Code Byte 1	Reserved	x	x	x	x	x	x	x	x	xx
						10GFC Code Byte 2	Reserved	x	x	x	x	x	x	x	x	xx
						10GFC Code Byte 3	Reserved	x	x	x	x	x	x	x	x	xx

NVR Register Map (continued)

Basic	32802	8022	27	2	Range	Specifies transmission range in 10 m increments		x	x	x	x	x	x	x	x	xx
	32804	8024	29	2	Fibre Type	Fibre Type Byte 0	Unspecified	0	0	0	0	0	0	0	0	0
							MM, generic	0	0	0	0	0	0	0	1	1
							50/125 only	0	0	0	0	0	0	1	0	1
							62.5/125 only	0	0	0	0	0	1	0	0	4
							POF	0	0	0	0	1	0	0	0	8
							HPCF	0	0	0	1	0	0	0	0	10
							SM, generic	0	0	1	0	0	0	0	0	20
							NDSF only	0	1	0	0	0	0	0	0	40
							NZDSF only	1	0	0	0	0	0	0	0	80
						Fibre Type Byte 1	Unspecified	0	0	0	0	0	0	0	0	0
							Large core only	0	0	0	0	0	0	0	1	1
							PMF only	0	0	0	0	0	0	1	0	2
							Reserved	0	0	0	0	0	1	0	0	4
							Reserved	0	0	0	0	1	0	0	0	8
							Reserved	0	0	0	1	0	0	0	0	10
							Reserved	0	0	1	0	0	0	0	0	20
							Reserved	0	1	0	0	0	0	0	0	40
							Reserved	1	0	0	0	0	0	0	0	80
	32806	8026	31	3	Wavelength chan 0	Centre Optical Wavelength in 0.01nm steps - Channel 0		x	x	x	x	x	x	x	x	xx
	32809	8029	34	3	Wavelength chan 1	Centre Optical Wavelength in 0.01nm steps - Channel 1		x	x	x	x	x	x	x	x	xx
	32812	802C	37	3	Wavelength chan 2	Centre Optical Wavelength in 0.01nm steps - Channel 2		x	x	x	x	x	x	x	x	xx
	32815	802F	40	3	Wavelength chan 3	Centre Optical Wavelength in 0.01nm steps - Channel 3		x	x	x	x	x	x	x	x	xx
	32818	8032	43	4	Package OUI	Package Identifier OUI		x	x	x	x	x	x	x	x	xx
	32822	8036	47	4	Vendor OUI	Transceiver Vendor OUI		x	x	x	x	x	x	x	x	xx
	32826	803A	51	16	Vendor Name	Transceiver vendor name in ASCII		x	x	x	x	x	x	x	x	xx
	32842	804A	67	16	Vendor PN	Part number provided by transceiver vendor in ASCII		x	x	x	x	x	x	x	x	xx
	32858	805A	83	2	Vendor Rev	Revision level for part number provided by vendor ASCII		x	x	x	x	x	x	x	x	xx
	32860	805C	85	16	Vendor SN	Vendor serial number in ASCII		x	x	x	x	x	x	x	x	xx
	32876	806C	101	4	Date Code	Vendor manufacturing date code in ASCII	Year	x	x	x	x	x	x	x	x	xx
	32880	8070	105	2			Month	x	x	x	x	x	x	x	x	xx
	32882	8072	107	2			Day	x	x	x	x	x	x	x	x	xx
	32884	8074	109	2			Lot code	x	x	x	x	x	x	x	x	xx

NVR Register Map (continued)

32886	8076	111	1	Current Reference	5V Stressed Environment Reference 100%= 1A	5.0V not used	0	0	0	0	0	0	0	0	0
						20%29%	0	0	0	0	0	0	0	1	1
						30%39%	0	0	0	0	0	0	1	0	2
						40%49%	0	0	0	0	0	1	0	0	4
						50%59%	0	0	0	0	1	0	0	0	8
						60%69%	0	0	0	1	0	0	0	0	10
						70%79%	0	0	1	0	0	0	0	0	20
						80%89%	0	1	0	0	0	0	0	0	40
						90%99%	1	0	0	0	0	0	0	0	80
32887	8077	112	1		3.3V Stressed Environment Reference 100%= 2A	3.3V not used	0	0	0	0	0	0	0	0	0
						20%29%	0	0	0	0	0	0	0	1	1
						30%39%	0	0	0	0	0	0	1	0	2
						40%49%	0	0	0	0	0	1	0	0	4
						50%59%	0	0	0	0	1	0	0	0	8
						60%69%	0	0	0	1	0	0	0	0	10
						70%79%	0	0	1	0	0	0	0	0	20
						80%89%	0	1	0	0	0	0	0	0	40
						90%99%	1	0	0	0	0	0	0	0	80
32888	8078	113	1		APS Stressed Environment Reference 100%= 2A	APS not used	0	0	0	0	0	0	0	0	0
						20%29%	0	0	0	0	0	0	0	1	1
						30%39%	0	0	0	0	0	0	1	0	2
						40%49%	0	0	0	0	0	1	0	0	4
						50%59%	0	0	0	0	1	0	0	0	8
						60%69%	0	0	0	1	0	0	0	0	10
						70%79%	0	0	1	0	0	0	0	0	20
						80%89%	0	1	0	0	0	0	0	0	40
						90%99%	1	0	0	0	0	0	0	0	80
32889	8079	114	1	APS Voltage	Nominal APS Voltage	Unspecified	0	0	0	0	0	0	0	0	0
						0.9	0	0	0	0	0	0	0	1	1
						1	0	0	0	0	0	0	1	0	2
						1.2	0	0	0	0	0	1	0	0	4
						1.3	0	0	0	0	1	0	0	0	8
						1.5	0	0	0	1	0	0	0	0	10
						1.8	0	0	1	0	0	0	0	0	20
						C	0	1	0	0	0	0	0	0	40
						Reserved	1	0	0	0	0	0	0	0	80

NVR Register Map (continued)

	32890	807A	115	1	DOM Capability	Digital Optical Monitoring Capability Byte	Ext DOM Addr	x	x	x	x	x	x	x	x	xx
	32891	807B	116	1	Optional Capability	Low Power Start-up(LPS) Mode Capability Bit	LPS	x	x	x	x	x	x	x	1	xx
						Reserved	Reserved	x	x	x	x	x	x	x	x	xx
	32892	807C	117	1	Reserved			x	x	x	x	x	x	x	x	xx
	32893	807D	118	1	Basic Checksum	Basic Field Checksum		x	x	x	x	x	x	x	x	xx
Customer	32894	807E	119	48	Customer Area	Customer Writeable Area		x	x	x	x	x	x	x	x	xx
Vendor	32942	80AE	167	89	Vendor Specific	Vendor Specific		x	x	x	x	x	x	x	x	xx
Extended Vendor	33031	8107	256	n-256	Extended Vendor	Extended Vendor Specific		x	x	x	x	x	x	x	x	xx

10.9 NVR Control/Status Register (0x8000)

10.9.1 Overview

The NVR Control/Status Register provides facilities to read and write non-volatile memory in the XENPAK module (other uses may be made by the module manufacturer).

XENPAK registers may be read via standard MDC/MDIO transactions to address locations specified in Table 1 without using the NVR Control Register. .

Writes via MDIO are stored as volatile values in XENPAK register space, unless backed-up up with a write using the NVR Control/Status register.

The control status register can be used to write to the customer area of the non-volatile ram.

Upon power up or reset the entire user writeable and other NVR map will be restored to the customer area. The user may also force an update by performing a NVR 'read NVR' Command with the Extended 'read/write all NVR contents' set to 11. This will overwrite any non-volatile activity that has occurred since the last write to non-volatile memory.

The control/status register is located at offset 0x8000 with a structure described in Table 15

Table 15 NVR Control/Status Register (0x8000)

Bit	Description	Properties[1]
15:9	Vendor Specific	RW
8:6	Reserved	RO
5	Command[3] 0 = read NVR 1 = write NVR	RW[2]
4	Reserved (0)	RO
3:2	Command Status 00 = Idle 01 = Command completed successfully 10 = Command in progress/Queued 11 = Command failed	RO
1:0	Extended Commands 00 = Vendor Specific 01 = Vendor Specific 10 = Vendor Specific 11 = read/write all NVR contents	RW[2].

1 RW = read/write, RO = read only, Op = Optional.
2 Once a command has been invoked the values written to the 'Command' and 'Extended Command' bits are held until the state machine transitions back to and idle state.
3 User writes to the Control/Status Register are not valid, except if an idle state is observed in Command Status, see 10.9.2.
4 A read to the Control/Status Register after command complete is required to return to idle (reverts command status to 00). (Per note 3, further commands should not be issued without returning to idle).

10.9.2 Read/Write Command (bit 5)

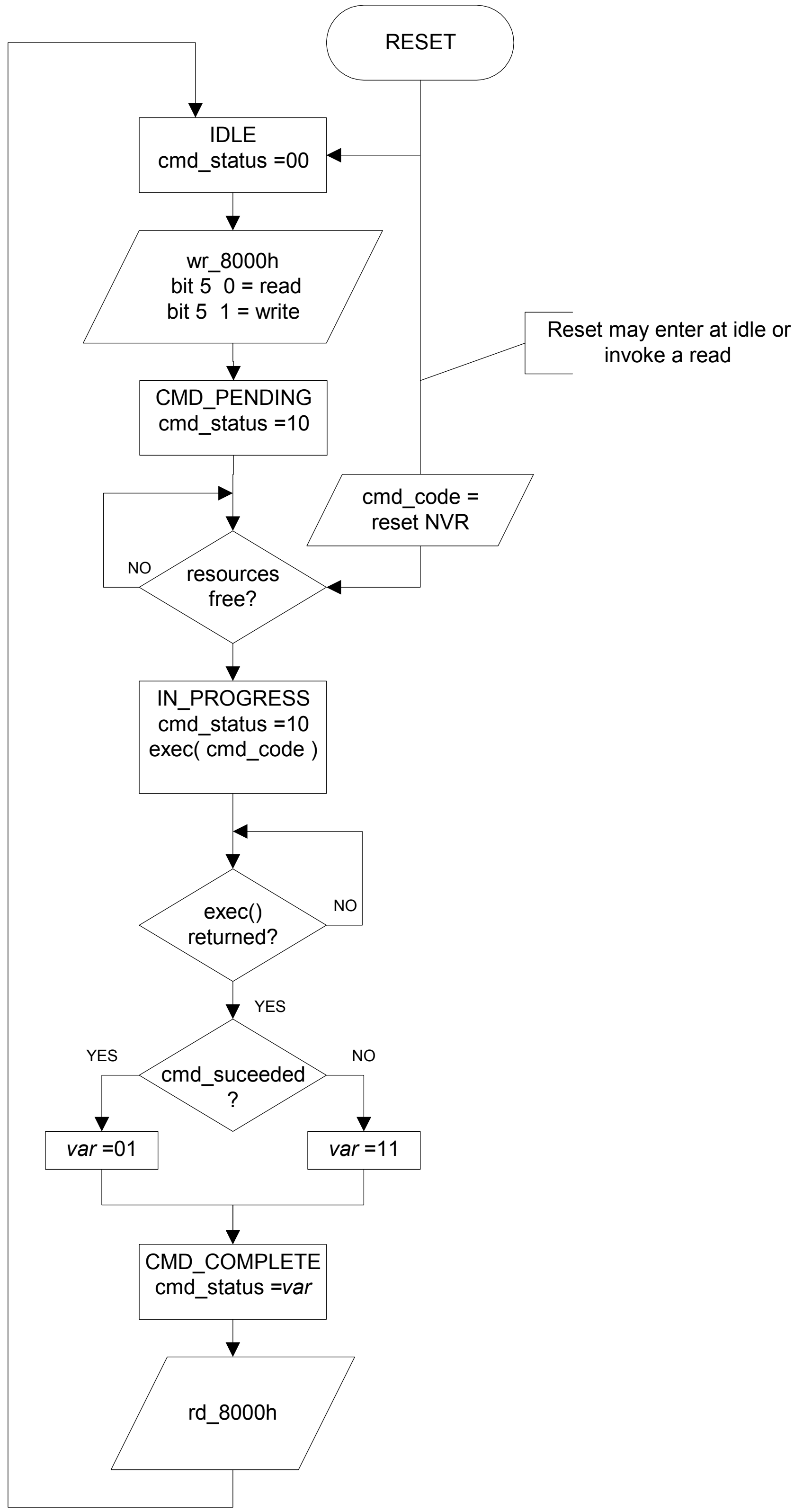
If in an idle state (see Fig 20), any write transaction to the NVR control/status register shall initiate an NVR transaction. A zero written to bit 5 initiates an NVR read. A one written to bit 5 initiates an NVR write. The extended command bits (1 and 0) determine the exact nature of the read/write operation.

Inclusion of this function permits implementations that maintain non-volatile storage in an independent location. The read function pulls the NVR contents out of non-volatile storage and maps them to the register locations specified in Table 1. The write function commits the contents of the NVRs to the corresponding external non-volatile storage locations (if writeable).

Once a command has been initiated further writes to the NVR control/status register will be ignored.

NVR and DOM sub-systems may share resources and therefore only one command can execute at a time. In this case if a command is initiated by one subsystem (e.g. NVR) but another sub-system (e.g. DOM) starts a command fractionally earlier, the former's command will be queued and executed later when the latter's sub-system releases the shared resources. A sub-system which is queuing a command will indicate "command in progress" in it's control/status register. A user should therefore ensure that the sub-system has returned to idle before he invokes another command on that subsystem.

Fig 20. NVR Access state diagram



1 Reset may initiate an EEPROM upload and cause state machine to enter CMD_COMPLETE with cmd_status set to 01 or 11 accordingly.

10.9.3 State Definitions

States supported by the NVR access state machine:

STATE	When Entered
IDLE:	Default state when no NVR read/writes are in progress or queued.
CMD_PENDING	State where command is queued pending availability of system resources,
IN_PROGRESS:	State assumed while NVR read or write is in process
CMD_COMPLETE:	State assumed after NVR read or write has occurred but before outcome has been read from the Command Status bits via MDIO.

10.9.4 State Transitions

State Transition	Invocation
From IDLE To CMD_PENDING:	Initiated by a write to the NVR control/status register.
From CMD_PENDING To IN_PROGRESS	Occurs when system resources are free to execute the requested command.
From IN_PROGRESS To CMD_COMPLETE:	Initiated by the NVR logic indicating that a read or write operation has been completed.
From CMD_COMPLETE To IDLE:	Initiated by a read of the NVR control/status register.

10.9.5 State Machine Function Definitions

wr_8000h = MDIO write to NVR Control/Status Register (0x8000)
rd_8000h = MDIO read from NVR Control/Status Register
exec(cmd_code) = perform command indicated by “cmd_code”
“cmd_code” defined by combination of bit 5 and bit 1:0 of NVR Control/Status Register.

10.9.6 Command Status (bits 3, 2)

Following a write to register 0x8000 (initiation of read/write command), bits 3 and 2 provide information on the status of the command. A value of 00 indicates an idle condition, 10 indicates that a command is pending or in progress, 01 indicates that the command completed successfully, and 11 indicated that the command failed.

10.9.7 Extended Commands (bits 1, 0)

Bits 1 and 0 supplement the basic read/write command (bit 5). A value of 11 reads and writes all NVR contents (subject to write protection, refer to10.11). All other values implement vendor specific commands.

10.10 NVR Error Detection

To protect against degradation in the non-volatile storage and potential errors in transfer, XENPAK data shall be protected by an 8-bit checksum as shown in Table 1. This checksum may be verified by a XENPAK module user prior to using the NVR contents.

The checksum shall cover the first 118 bytes of the NVR register map, from 8007h to 807Ch inclusive. The vendor specific and customer scratch areas are not covered by this checksum. Error detection capability for the vendor specific and customer writeable areas is beyond the scope of the MSA.

The format of the checksum shall be the low order 8 bits of the sum of the contents of all the bytes in the basic area.

It is not mandatory for the module to verify the checksum or report that the checksum is correct or incorrect. However, if the module operation is somehow defined by the NVR contents, it is strongly recommended that automatic verification be performed prior to using the stored information.

10.11 NVR Write Protection

The XENPAK basic region and vendor-specific regions are written at the time of module manufacture and shall not be altered by read/write commands. The customer writeable section shall be read/write enabled.

10.12 Non-Volatile Register Field Descriptions

This section explains the NVR field contents. In some cases clarification of field format is also provided, for example bit ordering. Register numbers are shown in decimal with hexadecimal values in parentheses.

10.12.1 Version

This register indicates the XENPAK MSA version number supported by the transceiver.
The 8 bits are used to represent version number times 10 - this yields max of 25.5 revisions.

EG. For version 3.0 this gives: 30(d) => 0001 1110(b)

10.12.2 NVR_Size

The total size of NVR, between 256 and 2048 bytes.

10.12.3 Mem_Used

The number of bytes used in the NVR including Vendor Specific bytes. For the purposes of calculating this field at manufacture it is assumed that all Customer Writeable bytes are in use.

10.12.4 Basic, Cust, Vend, Ext Vend Addr

The NVR start address in bytes for each field group; Basic, Customer Area, Vendor Specific and Extended Vendor Specific.

10.12.5 Transceiver Type

The default transceiver type for this MSA is "XENPAK"

10.12.6 Optical Connector Type

Indicates the optical connector type. For XENPAK the optical connector is SC-Duplex.

10.12.7 Bit Encoding

Coding method is indicated in the Bit Encoding field.

10.12.8 Bit Rate

Nominal bit rate in multiples of 1Mb/s is indicated in the Bit Rate field. A value of zero indicates that the value is unspecified.

Register (hex)	Bit	Bit Rate
32789 (8015)	7	Bit 15 (MSB)
	6	Bit 14
	5	Bit 13
	4	Bit 12
	3	Bit 11
	2	Bit 10
	1	Bit 9
	0	Bit 8
32790 (8016)	7	Bit 7
	6	Bit 6
	5	Bit 5
	4	Bit 4
	3	Bit 3
	2	Bit 2
	1	Bit 1
	0	Bit 0

10.12.9 Protocol Type

Protocol Type may be indicated in this field or must be inferred from the Standards Compliance Codes.

10.12.10 Standards Compliance Codes

Compatibility with recognized industry standards is indicated in the Standards Compliance Codes field. If the field is left unspecified the transceiver capability must be inferred from other information contained in NVR.

10.12.11 Range

Range specifies the link length supported by the transceiver in multiples of 10m up to a maximum of 655.36km. Bit order is as follows:

Register (hex)	Bit	Range Value
32802 (8022)	7	Bit 15 (MSB)
	6	Bit 14
	5	Bit 13
	4	Bit 12
	3	Bit 11
	2	Bit 10
	1	Bit 9
	0	Bit 8
32803 (8023)	7	Bit 7
	6	Bit 6
	5	Bit 5
	4	Bit 4
	3	Bit 3
	2	Bit 2
	1	Bit 1
	0	Bit 0

10.12.12 Fibre Type

The intended fiber type for use with the transceiver is indicated.

10.12.13 Centre Optical Wavelength

The wavelength is specified in multiples of 0.01nm. This resolution allows for future DWDM solutions. In the case of non-wavelength controlled transceivers the nominal center wavelength should be indicated.

Register (hex)	Bit	Wavelength Value
32806 (8026)	7	Bit 23 (MSB)
	6	Bit 22
	5	Bit 21
	4	Bit 20
	3	Bit 19
	2	Bit 18
	1	Bit 17
	0	Bit 16
32807 (8027)	7	Bit 15
	6	Bit 14
	5	Bit 13
	4	Bit 12
	3	Bit 11
	2	Bit 10
	1	Bit 9
	0	Bit 8
32808 (8028)	7	Bit 7
	6	Bit 6
	5	Bit 5
	4	Bit 4
	3	Bit 3
	2	Bit 2
	1	Bit 1
	0	Bit 0

10.12.14 Package Identifier OUI

The Package Identifier OUI is a 4 byte field that contains the XENPAK OUI.
Bit order for the OUI part of registers 0x8032 - 0x8034 follows the format of IEEE 802.3-2000, see figure 22.12 (clause 22.2.4.3.1) and IEEE 802-1990, see figure 5.2 and figure 5.3 (clause 5.1.2).

The XENPAK OUI is 00-08-BE

Register (hex)	Bit	Package OUI
32818 (8032)	7	XENPAK OUI Bit 3
	6	XENPAK OUI Bit 4
	5	XENPAK OUI Bit 5
	4	XENPAK OUI Bit 6
	3	XENPAK OUI Bit 7
	2	XENPAK OUI Bit 8
	1	XENPAK OUI Bit 9
	0	XENPAK OUI Bit 10
32819 (8033)	7	XENPAK OUI Bit 11
	6	XENPAK OUI Bit 12
	5	XENPAK OUI Bit 13
	4	XENPAK OUI Bit 14
	3	XENPAK OUI Bit 15
	2	XENPAK OUI Bit 16
	1	XENPAK OUI Bit 17
	0	XENPAK OUI Bit 18
32820 (8034)	7	XENPAK OUI Bit 19
	6	XENPAK OUI Bit 20
	5	XENPAK OUI Bit 21
	4	XENPAK OUI Bit 22
	3	XENPAK OUI Bit 23
	2	XENPAK OUI Bit 24
	1	NVR Dev Addr Bit 4
	0	NVR Dev Addr Bit 3
32821 (8035)	7	NVR Dev Addr Bit 2
	6	NVR Dev Addr Bit 1
	5	NVR Dev Addr Bit 0
	4	Revision No. Bit 3
	3	Revision No. Bit 2
	2	Revision No. Bit 1
	1	Revision No. Bit 0
	0	Reserved

10.12.15 Vendor OUI

The vendor organizationally unique identifier field (vendor OUI) is a 3 byte field that contains the IEEE Company Identifier for the transceiver vendor (as opposed to the OUI of any third party ICs which may be used therein). Bit order for the OUI follows the format of IEEE802.3 2000 Clause 22.2.4.3.1 and is therefore reversed in comparison to other non-volatile registers. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

Register (hex)	Bit	Vendor OUI
32822 (8036)	7	OUI Bit 3
	6	OUI Bit 4
	5	OUI Bit 5
	4	OUI Bit 6
	3	OUI Bit 7
	2	OUI Bit 8
	1	OUI Bit 9
	0	OUI Bit 10
32823 (8037)	7	OUI Bit 11
	6	OUI Bit 12
	5	OUI Bit 13
	4	OUI Bit 14
	3	OUI Bit 15
	2	OUI Bit 16
	1	OUI Bit 17
	0	OUI Bit 18
32824 (8038)	7	OUI Bit 19
	6	OUI Bit 20
	5	OUI Bit 21
	4	OUI Bit 22
	3	OUI Bit 23
	2	OUI Bit 24
	1	Model No. Bit 5
	0	Model No. Bit 4
32825 (8039)	7	Model No. Bit 3
	6	Model No. Bit 2
	5	Model No. Bit 1
	4	Model No. Bit 0
	3	Rev No. Bit 3
	2	Rev No. Bit 2
	1	Rev No. Bit 1
	0	Rev No. Bit 0

10.12.16 Vendor Name

The vendor name is a 16 byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid data.

10.12.17 Vendor PN

The vendor part number (vendor PN) is a 16 byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

10.12.18 Vendor Rev

The vendor revision number (vendor rev) is a 4 byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the 4-byte field indicates that the vendor Rev is unspecified.

10.12.19 Vendor Serial Number

The vendor serial number (vendor SN) is a 16 byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the 10G transceiver. A value of all zero in the 16-byte field indicates that the vendor SN is unspecified.

10.12.20 Date Code

The date code is a 10-byte field that contains the vendor's date code in ASCII characters.

Register (hex)	Date Value
32878 (806E)	Year in 1000's (bit 7=MSB, bit 0=LSB)
32879 (806F)	Year in 100's (bit 7=MSB, bit 0=LSB)
32880 (8070)	Year in 10's (bit 7=MSB, bit 0=LSB)
32881 (8071)	Year Units (bit 7=MSB, bit 0=LSB)
32882 (8072)	Month in 10's (bit 7=MSB, bit 0=LSB)
32883 (8073)	Month in units (bit 7=MSB, bit 0=LSB)
32884 (8074)	Day in 10's (bit 7=MSB, bit 0=LSB)
32885 (8075)	Day in Units (bit 7=MSB, bit 0=LSB)
32886 (8076)	Lot code in 10's (bit 7=MSB, bit 0=LSB)
32887 (8077)	Lot code in units (bit 7=MSB, bit 0=LSB)

10.12.21 Optional Capability.

This register is used to indicate support of optional XENPAK capabilities to the host.

Register (hex)	Bit	Optional Capability
32891	7:1	Reserved
	0	LPS Capability If one, the low power sequenced start-up functionality is implemented with the TX ON/OFF signal per section 10.4.2.

10.12.22 Customer Area

The "customer Area" is a block of non volatile memory that can be used by a XENPAK end user. This memory must be written via the NVR control register.10.9. Attempted writes directly to the Customer Area from MDIO will be volatile.

10.13 Link Alarm Status Interrupt (LASI)

10.13.1 Overview

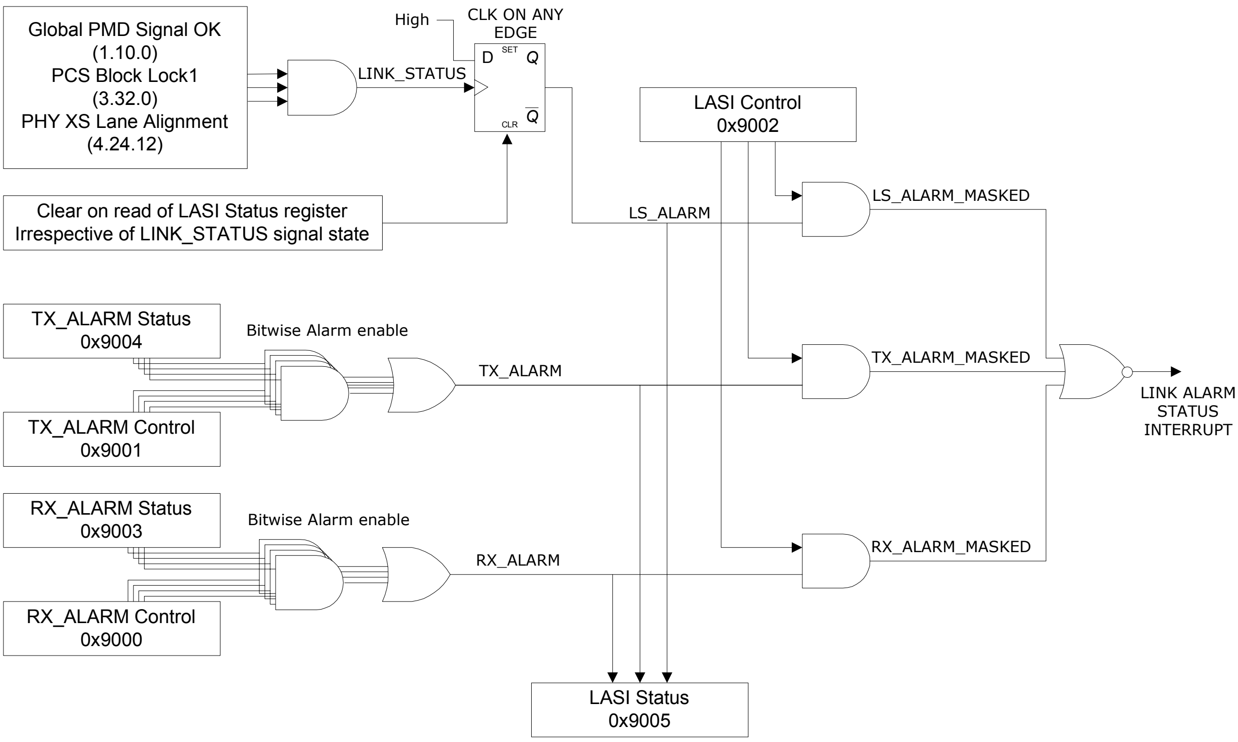
The link alarm status interrupt (LASI) is an active-low output (pin 9) from the XENPAK module that, when asserted, indicates a link fault condition has been asserted or has been cleared. Control registers are provided so that LASI may be programmed to assert only for specific fault conditions. A set of status registers are also provided to allow interrupt service routines to identify the source of the fault with a minimal number of register reads.

When XENPAK diagnostics (see Section 11) are included, the LASI function can incorporate diagnostic-based alarms to increase its fault isolation capabilities.

10.13.2 Operation

A top-level block diagram of LASI is shown in Fig 21

Fig 21. LASI Block Diagram



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10.13.3 RX_ALARM Status

Assertion of RX_ALARM indicates that a fault has occurred in the receive path of the XENPAK module. RX_ALARM shall be the logic OR of the bits in register 0x9003.

The contents of the RX_ALARM status register are shown in Table 16. Several bits in this register are linked to latch-high, clear on read bits in the IEEE standard register space (i.e. local fault bits). A read to either bit shall have the effect of clearing the status indicator in both locations.

For example, a PHY XS Receive Local Fault will cause both bit 4.8.10 and bit 0 of the RX_ALARM status register to latch high. A read to register 4.8 clears both 4.8.10 and bit 0 of the RX_ALARM status register. Similarly, a read to the RX_ALARM status register clears bit 0 and bit 4.8.10.

Table 16 RX_ALARM Status Register (0x9003)

Bit	Description	Properties[1]
15:11	Reserved (set to zero)	RO
10	Vendor Specific	—
9	WIS Local Fault (bit 2.1.7)	O/RO/LH
8:6	Vendor Specific	—
5	Receive Optical Power Fault	O/RO/LH
4	PMA/PMD Receiver Local Fault (bit 1.8.10)	O/RO/LH
3	PCS Receive Local Fault (bit 3.8.10)	RO/LH
2:1	Vendor Specific	—
0	PHY XS Receive Local Fault (bit 4.8.10)	RO/LH

1 O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

10.13.4 RX_ALARM Control

RX_ALARM may be programmed to assert only when specific receive path fault condition(s) are present. The programming is performed by writing the contents of a mask register located at offset 0x9000. The contents of register 0x9003 shall be AND'ed with the contents of register 0x9000 prior to application of the OR function that generates the RX_ALARM signal.

Table 17 RX_ALARM Control Register (0x9000)

Bit	Description	Default	Properties[1]
15:11	Reserved	0	RO
10	Vendor Specific	Note 3	RW
9	WIS Local Fault Enable	Note 2	Note 2
8:6	Vendor Specific	Note 3	RW
5	Receive Optical Power Fault Enable	Note 2	Note 2
4	PMA/PMD Receiver Local Fault Enable	Note 2	Note 2
3	PCS Receive Local Fault Enable	1	RW
2:1	Vendor Specific	Note 3	RW
0	PHY XS Receive Local Fault Enable	1	RW

1 O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

2 Optional features that are not implemented shall have their enable bit forced to zero. When implemented, the default value for the control bit shall be 1.

3 The default value for a vendor specific bit shall be vendor specific.

10.13.5 TX_ALARM Status

Assertion of TX_ALARM indicates that a fault has occurred in the transmit path of the XENPAK module. TX_ALARM shall be the logic OR of the bits in register 0x9004.

The contents of the TX_ALARM status register are shown in Table 18. Several bits in this register are linked to latch-high, clear on read bits in the IEEE standard register space (i.e. local fault bits). A read to either bit shall have the effect of clearing the status indicator in both locations (refer to 10.13.3 for an example).

Table 18 TX_ALARM Status Register (0x9004)

Bit	Description	Properties
15:11	Reserved (set to zero)	RO
10	Vendor Specific	—
9	Laser Bias Current Fault	O/RO/LH
8	Laser Temperature Fault	O/RO/LH
7	Laser Output Power Fault	O/RO/LH
6	Transmitter Fault	RO/LH
5	Vendor Specific	—
4	PMA/PMD Transmitter Local Fault (1.8.11)	O/RO/LH
3	PCS Transmit Local Fault (3.8.11)	RO/LH
2:1	Vendor Specific	—
0	PHY XS Transmit Local Fault (4.8.11)	RO/LH

1. O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

10.13.6 TX_ALARM Control

TX_ALARM may be programmed to assert only when specific transmit path fault condition(s) are present. The programming is performed by setting the contents of a mask register located at offset 0x9001. The contents of register 0x9004 shall be AND'ed with the contents of register 0x9001 prior to application of the OR function that generates the TX_ALARM signal.

Table 19 TX_ALARM Control Register (0x9001)

Bit	Description	Default	Properties[1]
15:11	Reserved	0	RO
10	Vendor Specific	Note 3	RW
9	Laser Bias Current Fault Enable	Note 2	Note 2
8	Laser Temperature Fault Enable	Note 2	Note 2
7	Laser Output Power Fault Enable	Note 2	Note 2
6	Transmitter Fault Enable	1	RW
5	Vendor Specific	Note 3	RW
4	PMA/PMD Transmitter Local Fault Enable	Note 2	Note 2
3	PCS Transmit Local Fault Enable	1	RW
2:1	Vendor Specific	Note 3	RW
0	PHY XS Transmit Local Fault Enable	1	RW

[1] O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).
[2] Optional features that are not implemented shall have their enable bit forced to zero. When implemented, the default value for the control bit shall be 1.
[3] The default value for a vendor specific bit shall be vendor specific.

10.13.7 LS_ALARM

The LS_ALARM shall be asserted each time Link Status, defined in 10.13.8, changes state. This feature eliminates the need to periodically poll a module for status.

A fault condition will assert TX_ALARM, RX_ALARM, and set Link Status to FALSE. TX_ALARM and RX_ALARM may be masked to prevent persistent interrupt. When the fault condition is removed, Link Status will change state to TRUE causing the assertion of the LS_ALARM. The interrupt service routine may then remove the mask on TX_ALARM and RX_ALARM to resume normal monitoring.

LS_ALARM may optionally assert each time there is a change of state on any of the Link Status input signals to allow more granular fault reporting by the XENPAK module.

In all cases LS_ALARM will be cleared by a read of the LASI Status register and will stay asserted until such a read has occurred.

10.13.8 Link Status Definition

Link Status is a real-time indicator of link health, generated internally by LASI, for use in the LS_ALARM interrupt definition. Link Status shall be the logic AND of the signals shown in Table 20

Table 20 Link Status Input Signals

Signal	Source
Global PMD Signal OK	1.10.0
PCS Block Lock[1]	3.32.0
PHY XS Lane Alignment	4.24.12

1. In the case of the 10GBASE-LX4 PCS, the Lane Alignment status bit (3.24.12) may be used rather than Block Lock.

Additional signals may be included in the Link Status definition but this is beyond the scope of this MSA. Inputs to Link Status shall not be latched signals.

10.13.9 LASI Status

Register 0x9005 contains a top-level of the cause of the interrupt. The contents of this register are given in Table 21.

Table 21 LASI Status Register (0x9005)

Bit	Description	Properties[1]
15:8	Reserved	RO
7:3	Vendor Specific	—
2	RX_ALARM	RO
1	TX_ALARM	RO
0	LS_ALARM	LH

1. O = optional, RW = read/write, RO = read only, LH = latch high, clear on read.

Note that the RX_ALARM and TX_ALARM indications are the logic OR of the contents of registers 0x9003 and 0x9004 respectively. Therefore, these alarms will persist until the bit(s) reflecting the source of interrupt are cleared.

10.13.10 LASI Control

Register 0x9002 is a LASI control register that allows global masking of the RX_ALARM, TX_ALARM, and LS_ALARM inputs. The contents of this register are given in Table 22

Table 22 LASI Control Register (0x9002)

Bit	Description	Default	Properties[1]
15:8	Reserved	0	RO
7:3	Vendor Specific	Note 2	RW
2	RX_ALARM Enable	0	RW
1	TX_ALARM Enable	0	RW
0	LS_ALARM Enable	0	RW

1 O = optional, RW = read/write, RO = read only, LH = latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

2 When implemented, the default value for the control bit shall be 0.

10.13.11 LASI Timing Requirements

LASI shall be asserted within 10 ms following the detection of a fault condition. LASI shall be cleared within 10 ms of the register read operation that clears the fault indicator.

10.13.12 Relationship between LASI and XENPAK Diagnostics

Receive optical power, laser output power, laser bias current, and laser temperature fault indications are optional inputs to the LASI function which are also covered by the XENPAK diagnostics. While this fault indications have a vendor specific definition, it is recommended that when XENPAK diagnostics are implemented, these fault indications are the logic OR of high/low alarms for the parameter of interest. For example, Receive Optical Power Fault would be the logic OR of the Receive Optical Power High and Receive Optical Power Low alarms from the XENPAK diagnostics.

When implemented according to this definition, an additional register read will be required to clear a diagnostic related interrupt. Since LASI fault indications are recommended to be the logic OR of latched diagnostics alarms, the interrupt cannot be cleared until the diagnostic alarm register is read. These additional register reads will not only clear the interrupt but also indicate whether the fault occurred due to high or low parameter levels.

11 XENPAK Diagnostics

11.1 Scope

This section of the MSA defines a Digital Optical Monitoring (DOM) interface for XENPAK transceivers that allows access to device operating parameters. The interface is a derivative of *SFF-8472: Digital Diagnostic Monitoring Interface for Optical Transceivers* appropriate to XENPAK transceivers. This specification defines a 256 byte block of register space that is accessible over the 2 wire serial MDIO/MDC interface. By defining a different register space than the XENPAK NVRs (Non-Volatile Registers) and providing the capability to address an additional external device, the interface is backward compatible with XENPAK Issue 2.1. Support for both serial and 4 lane PMD implementations as specified in the IEEE P802.3ae standard “10G Ethernet - Media Access Control (MAC) Parameters, Physical Layer, and Management Parameters for 10Gb/s Operation” is provided. Digital Optical Monitoring indicators are optional, but if implemented should conform to the format described below. In addition, Digital Optical Monitoring (DOM) indicators can be made inputs to the Link Alarm Status Interrupt (LASI) function.

11.2 Monitoring, General Overview.

This section describes the memory map used to access measurements of transceiver temperature, receive optical power, laser output power, and laser bias current through the 2 wire serial MDIO/MDC interface. These measurements are optional, and support is indicated through the capability registers (807A: DOM Capability and A06F: DOM Capability - Extended). The transceiver generates this monitoring data by digitization of internal analog signals. The digitized data is calibrated to absolute measurements that should be interpreted according to the sections below. Calibrated alarm and warning threshold data should be interpreted in the same manner and is written during device manufacture. Optional alarm/warning flags may be implemented for monitored quantities. Alarm flags are required if Digital Optical Monitoring (DOM) indicators are to be made inputs to the Link Alarm Status Interrupt (LASI) function.
Measured parameters are reported in 16 bit data fields (i.e. two concatenated bytes). The 16 bit data fields allow for wide dynamic range, and are not intended to imply that a 16 bit A/D system is recommended or required in order to achieve the accuracy goals stated below. It is recommended that any low-order data bits beyond the system’s specified accuracy be fixed to zero. The update of the multi-byte fields (i.e. two concatenated bytes) must not occur such that partially updated multi-byte fields are read over the MDIO interface.

Fig 22. XENPAK Digital Optical Monitoring MDIO Register Space

0xA000 to 0xA027	40	Alarm and Warning Thresholds
0xA028 to 0xA047	32	Vendor Specific
0xA048 to 0xA05F	24	Optional Alarm and Warning Thresholds for CWDM
0xA060 to 0xA077	24	Digital Optical Monitoring Interface
0xA078 to 0xA0BF	72	Vendor Specific
0xA0C0 to 0xA0FF	64	Optional Digital Optical Monitoring Interface for CWDM

11.2.1 Transceiver Temperature

Internally measured transceiver temperature. Represented as a 16 bit signed twos complement value in increments of 1/256 degrees Celsius valid between -40 C and +125 C. Temperature accuracy is vendor specific, but must be better than +/- 5 degrees Celsius over specified operating temperature and voltage. Temperature measurement location is vendor specific.

Table 23 Temperature Value

Temperature	Binary Value		Hexadecimal Value	
Value	MSB	LSB	MSB	LSB
-40.0 C*	11011000	00000000	D8	00
0.0 C	00000000	00000000	00	00
+125.0 C	01111101	00000000	7D	00

11.2.2 Laser Bias Current

Measured laser bias current in uA. Represented as a 16 bit unsigned integer with the current defined as the full 16 bit value (0 - 65535) with LSB equal to 2 uA. Total measurement range is from 0 mA to 131 mA. To accommodate long-reach applications, the value of the LSB can be changed to 10 uA. Total measurement range is then from 0 mA to 655 mA. The value of this Laser Bias Scale Factor is reported by bit 4 of NVR register 807A (Digital Optical Monitoring Capability). Accuracy is vendor specific, but must be better than +/- 10% of the manufacturer's nominal set-point over specified operating temperature and voltage.

Table 24 Current Value (LSB = 2 uA)

Current	Binary	Value	Hexadecimal	Value
Value	MSB	LSB	MSB	LSB
0.0 mA	00000000	00000000	00	00
50.0 mA	01100001	10101000	61	A8
131.07 mA	11111111	11111111	FF	FF

11.2.3 Laser Output Power

Measured laser output power in mW. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 - 65535) with LSB equal to 0.1 uW. Total measurement range is from 0 mW to 6.5535 mW (~-40 dBm to +8.2 dBm). Data presented is average fiber coupled power and factory calibrated using the most representative fiber type. Accuracy must be better than +/- 3dB over average transmit power range for application (see note below). Accuracy beyond this minimum requirement is vendor specific. Data is not valid when transmitter is disabled.

Table 25 Tx Power Value

Power	Binary	Value	Hexadecimal	Value
Value	MSB	LSB	MSB	LSB
0.0 mW	00000000	00000000	00	00
3.0 mW	01110101	00110000	75	30
6.5535 mW	11111111	11111111	FF	FF

Note: Valid range of transmit power is derived from the appropriate standard. Range extends from maximum average launch power to minimum average launch power (assuming infinite extinction ratio).

11.2.4 Receive Optical Power

Measured receive optical power in mW. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 - 65535) with LSB equal to 0.1 uW. Total measurement range is from 0 mW to 6.5535 mW (~-40 dBm to +8.2 dBm). Data presented is average receive power from the fiber into the transceiver. Accuracy must be better than +/- 3dB over average receive power range for application (see note below). Accuracy beyond this minimum requirement is vendor specific.

Table 26 Rx Power Value

Power	Binary	Value	Hexadecimal	Value
Value	MSB	LSB	MSB	LSB
0.0 mW	00000000	00000000	00	00
1.0 mW	00100111	00010000	27	10
6.5535 mW	11111111	11111111	FF	FF

Note: Valid range of receive power is derived from the appropriate standard. Range extends from lesser of maximum average launch power or maximum average receive power on the high end to minimum average launch power (assuming infinite extinction ratio) minus channel insertion loss on the low end.

11.2.5 Alarm and Warning Thresholds

Each supported A/D quantity has a corresponding high alarm, low alarm, high warning, and low warning threshold. These factory-preset values allow the user to determine when a particular value is outside of “normal” limits as programmed by the transceiver manufacturer. It is assumed that these values will vary with different technologies and different implementations. The values reported in the Alarm and Warning Threshold area may be temperature compensated or otherwise adjusted. Any compensation or adjustment is vendor specific and completely optional.

Table 27 Alarm and Warning Threshold Memory Map

Address	MDIO Registers	Size	Name	Description	Note
00-01	A000-A001	2	Transceiver Temp High Alarm	MSB at low address	1
02-03	A002-A003	2	Transceiver Temp Low Alarm	MSB at low address	1
04-05	A004-A005	2	Transceiver Temp High Warning	MSB at low address	1
06-07	A006-A007	2	Transceiver Temp Low Warning	MSB at low address	1
08-15	A008-A00F	8	Reserved		
16-17	A010-A011	2	Laser Bias Current High Alarm	MSB at low address	2
18-19	A012-A013	2	Laser Bias Current Low Alarm	MSB at low address	2
20-21	A014-A015	2	Laser Bias Current High Warning	MSB at low address	2
22-23	A016-A017	2	Laser Bias Current Low Warning	MSB at low address	2
24-25	A018-A019	2	Laser Output Power High Alarm	MSB at low address	1
26-27	A01A-A01B	2	Laser Output Power Low Alarm	MSB at low address	1
28-29	A01C-A01D	2	Laser Output Power High Warning	MSB at low address	1
30-31	A01E-A01F	2	Laser Output Power Low Warning	MSB at low address	1
32-33	A020-A021	2	Receive Optical Power High Alarm	MSB at low address	1
34-35	A022-A023	2	Receive Optical Power Low Alarm	MSB at low address	1
36-37	A024-A025	2	Receive Optical Power High Warning	MSB at low address	1
38-39	A026-A027	2	Receive Optical Power Low Warning	MSB at low address	1
72-73	A048-A049	2	Lane 1 Laser Bias Current High Alarm	MSB at low address	
74-75	A04A-A04B	2	Lane 1 Laser Bias Current Low Alarm	MSB at low address	
76-77	A04C-A04D	2	Lane 1 Laser Bias Current High	MSB at low address	

			Warning		
78-79	A04E-A04F	2	Lane 1 Laser Bias Current Low Warning	MSB at low address	
80-81	A050-A051	2	Lane 2 Laser Bias Current High Alarm	MSB at low address	
82-83	A052-A053	2	Lane 2 Laser Bias Current Low Alarm	MSB at low address	
84-85	A054-A055	2	Lane 2 Laser Bias Current High Warning	MSB at low address	
86-87	A056-A057	2	Lane 2 Laser Bias Current Low Warning	MSB at low address	
88-89	A058-A059	2	Lane 3 Laser Bias Current High Alarm	MSB at low address	
90-91	A05A-A05B	2	Lane 3 Laser Bias Current Low Alarm	MSB at low address	
92-93	A05C-A05D	2	Lane 3 Laser Bias Current High Warning	MSB at low address	
94-95	A05E-A05F	2	Lane 3 Laser Bias Current Low Warning	MSB at low address	

For WDM Implementation:

1. Alarm and warning threshold values are common for all WDM lanes.
2. Represents lane 0 values if laser bias current alarm and warning thresholds are unique for each WDM lane. In this case the remaining threshold values are found in A048-A05F. Otherwise, laser bias current alarm and warning threshold values are common for all WDM lanes. In this case, A010-A017 represent the common thresholds and the values in A048-A05F should be 0.

11.2.6 Monitored A/D Values

Supported measurements are calibrated to stated accuracies over vendor specified operating temperature and voltage and should be interpreted according to previous sections.

Table 28 Table 6. Monitored A/D Value Memory Map

Address	MDIO Registers	Size	Name	Description	Note
96-97	A060-A061	2	Transceiver Temp	MSB at low address	1
98-99	A062-A063	2	Reserved		
100-101	A064-A065	2	Laser Bias Current	MSB at low address	1
102-103	A066-A067	2	Laser Output Power	MSB at low address	1
104-105	A068-A069	2	Receive Optical Power	MSB at low address	1
106-109	A06A-A06D	4	Reserved		
192-193	A0C0-A0C1	2	Lane 0 Transceiver Temp	MSB at low address	2
194-195	A0C2-A0C3	2	Reserved		
196-197	A0C4-A0C5	2	Lane 0 Laser Bias Current	MSB at low address	2
198-199	A0C6-A0C7	2	Lane 0 Laser Output Power	MSB at low address	2
200-201	A0C8-A0C9	2	Lane 0 Receive Optical Power	MSB at low address	2
202-207	A0CA-A0CF	6	Reserved		
208-209	A0D0-A0D1	2	Lane 1 Transceiver Temp	MSB at low address	2
210-211	A0D2-A0D3	2	Reserved		
212-213	A0D4-A0D5	2	Lane 1 Laser Bias Current	MSB at low address	2
214-215	A0D6-A0D7	2	Lane 1 Laser Output Power	MSB at low address	2
216-217	A0D8-A0D9	2	Lane 1 Receive Optical Power	MSB at low address	2
218-223	A0DA-A0DF	6	Reserved		
224-225	A0E0-A0E1	2	Lane 2 Transceiver Temp	MSB at low address	2
226-227	A0E2-A0E3	2	Reserved		
228-229	A0E4-A0E5	2	Lane 2 Laser Bias Current	MSB at low address	2
230-231	A0E6-A0E7	2	Lane 2 Laser Output Power	MSB at low address	2
232-233	A0E8-A0E9	2	Lane 2 Receive Optical Power	MSB at low address	2
234-239	A0EA-A0EF	6	Reserved		
240-241	A0F0-A0F1	2	Lane 3 Transceiver Temp	MSB at low address	2
242-241	A0F2-A0F3	2	Reserved		
244-245	A0F4-A0F5	2	Lane 3 Laser Bias Current	MSB at low address	2
246-247	A0F6-A0F7	2	Lane 3 Laser Output Power	MSB at low address	2
248-249	A0F8-A0F9	2	Lane 3 Receive Optical Power	MSB at low address	2
250-255	A0FA-A0FF	6	Reserved		

For WDM Implementation:

1. If one or more of the measured WDM parameters is out of range (warning or alarm indication set), then the value in this location should be the value that is farthest out of range. Otherwise, this location should contain a representative (as defined by vendor) value of the measured parameter.
2. These values are optional and are only required if the WDM transceiver performs individual lane monitoring. The vendor should set register 807A bit 5 to indicate that these registers will contain valid data; otherwise the values should be 0.

11.2.7 DOM Status/Control Registers

Following register has been reserved in the XENPAK Non-Volatile Register (NVR) space for Digital Optical Monitoring (DOM) Capability.

Table 29 807A: Digital Optical Monitoring (DOM) Capability

Bit	Description	Properties
7	Digital Optical Monitoring Control/Status Register Implemented: 0 = Not Implemented 1 = Implemented	RO
6	Set when Digital Optical Monitoring Implemented	RO
5	WDM Lane by Lane DOM Capability: Setting this bit indicates that registers A0C0-A0FF are valid. Setting this bit will NOT override indications placed in register A06F (DOM Capability).	RO
4	Laser Bias Scale Factor: 0 = 2 uA 1 = 10 uA	RO
3	Reserved	RO
2:0	Address of External Digital Optical Monitoring Device (if required)	RO

1. RO - Read Only

Following registers have been reserved in the XENPAK Digital Optical Monitoring (DOM) register space for Optional Status and Extended Capability.

Table 30 A06E (110): Optional Status Bits

Bit	Description	Properties
7:1	Reserved	RO
0	Data_Ready_Bar: optional bit is high during module power up and prior to the first valid A/D reading. Once the first valid A/D reading occurs, the bit is set low until the device is powered down.	RO

1. RO - Read Only

Table 31 A06F (111): Digital Optical Monitoring (DOM) Capability - Extended

Bit	Description	Properties
7	Set to indicate transceiver temperature monitoring capable	RO
6	Set to indicate laser bias current monitoring capable	RO
5	Set to indicate laser output power monitoring capable	RO
4	Set to indicate receive optical power monitoring capable	RO
3	Set to indicate alarm flags implemented for monitored quantities	RO
2	Set to indicate warning flags implemented for monitored quantities	RO
1	Set to indicate monitored quantities are inputs to LASI function. If this bit is set, bit 3 must also be set (i.e. alarm flag support).	RO
0	Reserved	RO

2. RO - Read Only

The Optional DOM Control/Status Register (A100) provides facilities to update MDIO registers with DOM information:

Table 32 A100 (256): Optional Digital Optical Monitoring (DOM) Control/Status

Bit	Description	Properties
7:4	Reserved	RO
3:2	Command Status: 00 = Idle 01 = Command completed successfully 10 = Command in progress (indicates MDIO registers being updated with DOM information - See XENPAK MSA Figure 19 for additional information) 11 = Command failed	RO/LH
1:0	Update Commands: 00 = Write to bits initiates a single update of MDIO registers with all bytes of DOM information. Write of this bit combination also stops periodic update modes. 01 = Write to bits initiates a periodic update of MDIO registers with all bytes of DOM information. Frequency of update is vendor specific, but this bit combination provides the slowest rate of periodic update. 10 = Write to bits initiates periodic update of MDIO registers with all bytes of DOM information. Frequency of update is vendor specific, but this bit combination provides an intermediate rate of periodic update. 11 = Write to bits initiates periodic update of MDIO registers with all bytes of DOM information. Frequency of update is vendor specific, but this bit combination provides the fastest rate of periodic update.	RW

1. Operation per Table 15 and Fig 20, plus additional Update Commands (see note below)

General Notes regarding operation of DOM Control/Status register Update Commands:
Implementation of Control/Status register for periodic update is vendor specific.
Recommended operation:

Step 1. Station Management (STA) initiates periodic update: write to control bits <bit1:bit0>=[<0:1>,<1:0>,<1:1>].

Step 2. MDIO registers updated with all bytes of DOM information: status bits <bit3:bit2>=<1:0> during update.

Step 3. If update successful:
- Status bits <bit3:bit2>=<0:1>.
- STA capable of reading status bits <bit3:bit2> between periodic updates of MDIO registers.
- MDIO registers updated with all bytes of DOM information at next scheduled interval: during update status bits <bit3:bit2>=<1:0>, than are loaded with completion status (i.e. successful or failed).

Step 4. If update failed:
- Status bits <bit3:bit2>=<1:1>.
- Periodic update of MDIO registers stopped: STA capable of query through control/status bits.

11.3 Alarm and Warning Flags

Bytes 112 - 119 contain an optional set of alarm and warning flags. Alarm flags must be implemented for monitored quantities if they are to be inputs to the Link Alarm Status Interrupt (LASI) function. Implementation is vendor specific, but filtering (analog or digital) of the alarm flags is recommended to prevent false triggering or dithering if they are inputs to LASI. Alarm and warning flags only monitor A/D values in registers A060-A06D.

Two flag types are defined:

- Alarm flags associated with transceiver temperature, receive optical power, laser output power, and laser bias current. Alarm flags indicate conditions likely to be associated with an in-operational link and cause for immediate action.
- Warning flags associated with transceiver temperature, receive optical power, laser output power, and laser bias current. Warning flags indicate conditions outside the normally guaranteed bounds, but not necessarily causes of immediate link failures.

Table 33 Alarm and Warning Flag Memory Map

Address	MDIO Registers	Bits	Name	Description	Note
112	A070	7	Transceiver Temp High Alarm	Set when transceiver temp exceeds high alarm level	1
112	A070	6	Transceiver Temp Low Alarm	Set when transceiver temp is below low alarm level	1
112	A070	4-5	Reserved		
112	A070	3	Laser Bias Current High Alarm	Set when laser bias current exceeds high alarm level	1
112	A070	2	Laser Bias Current Low Alarm	Set when laser bias current is below low alarm level	1
112	A070	1	Laser Output Power High Alarm	Set when laser output power exceeds high alarm level	1
112	A070	0	Laser Output Power Low Alarm	Set when laser output power is below low alarm level	1
113	A071	7	Receive Optical Power High Alarm	Set when receive optical power exceeds high alarm level	1
113	A071	0-5	Reserved		
114-115	A072-A073	All	Reserved		
116	A074	7	Transceiver Temp High Warning	Set when transceiver temp exceeds high warning level	1
116	A074	6	Transceiver Low High Warning	Set when transceiver temp is below low warning level	1
116	A074	4-5	Reserved		
116	A074	3	Laser Bias Current High Warning	Set when laser bias current exceeds high warning level	1
116	A074	2	Laser Bias Current Low Warning	Set when laser bias current is below low warning level	1
116	A074	1	Laser Output Power High Warning	Set when laser output power exceeds high warning level	1
116	A074	0	Laser Output Power Low Warning	Set when laser output power is below low warning level	1
117	A075	7	Receive Optical Power High Warning	Set when receive optical power exceeds high warning level	1

117	A075	6	Receive Optical Power Low Warning	Set when receive optical power is below low warning level	1
117	A075	0-5	Reserved		
118-119	A076-A077	All	Reserved		

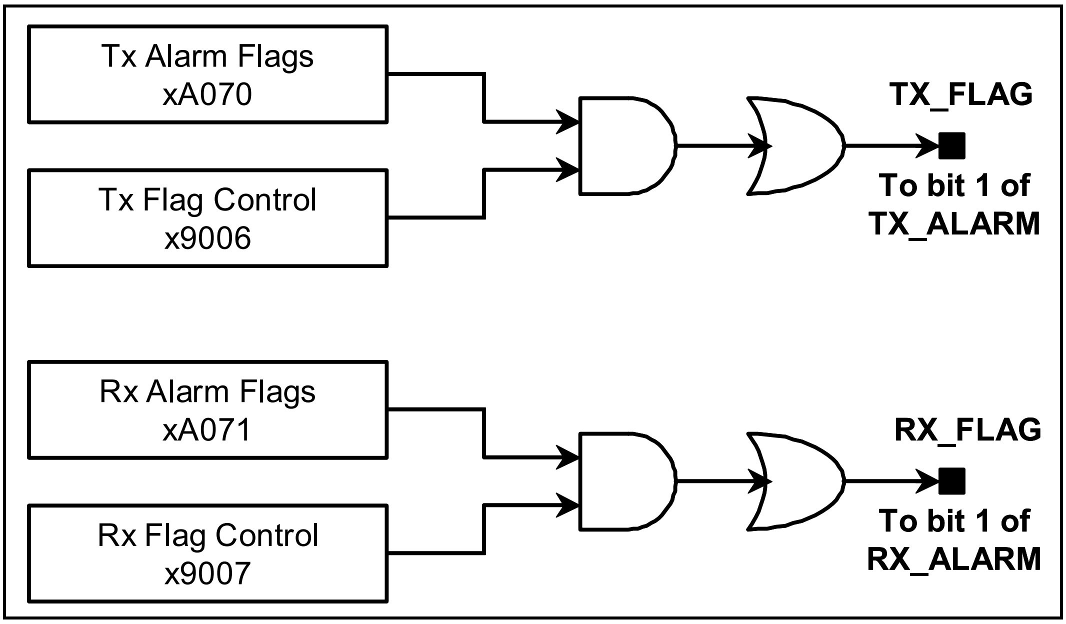
For WDM Implementation:

1. Alarm and warning flags only monitor A/D values in registers A060-A06D.Relationship between LASI and XENPAK Digital Optical Monitoring (DOM)

11.4 Operation

A top-level block diagram of Digital Optical Monitoring (DOM) incorporated into the Link Alarm Status Interrupt (LASI) function is shown below.

Fig 23. DOM/LASI Block Diagram



11.4.1 TX_FLAG Status

Assertion of TX_FLAG indicates that one or more of the transmitter operating parameters (transceiver temperature, laser bias current, or laser output power) exceeds the alarm levels. Tx alarm flags only monitor A/D values in registers A060-A06D. TX_FLAG shall be the logic OR of the bits in register xA070. The contents of the TX_FLAG status register are shown below. Bit 1 of TX_ALARM (TX_FLAG) will have the properties of latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

Table 34 xA070 (112): TX_FLAG Status Bits

Bit	Description	Properties
7	Transceiver Temperature High Alarm	O/RO
6	Transceiver Temperature Low Alarm	O/RO
5:4	Reserved	RO
3	Laser Bias Current High Alarm	O/RO
2	Laser Bias Current Low Alarm	O/RO
1	Laser Output Power High Alarm	O/RO
0	Laser Output Power Low Alarm	O/RO

1. O - Optional
2. RO - Read Only
3. This register may be optionally implemented optionally implemented as read/write

11.4.2 TX_FLAG Control

TX_FLAG may be programmed to assert only when specific transmit operation parameters exceed their alarm levels. The programming is performed by writing the contents of a mask register located at offset x9006. The contents of register xA070 shall be AND'ed with the contents of register x9006 prior to application of the OR function that generates the TX_FLAG signal.

Table 35 x9006: TX_FLAG Control Bits

Bit	Description	Default	Properties
7	Transceiver Temp High Alarm Enable	0	RW
6	Transceiver Temp Low Alarm Enable	0	RW
5:4	Reserved	0	RW
3	Laser Bias Current High Alarm Enable	0	RW
2	Laser Bias Current Low Alarm Enable	0	RW
1	Laser Output Power High Alarm Enable	0	RW
0	Laser Output Power Low Alarm Enable	0	RW

1. RW - Read/Write

11.4.3 RX_FLAG Status

Assertion of RX_FLAG indicates that one or more of the receiver operating parameters (receive optical power) exceeds the alarm levels. Rx alarm flags only monitor A/D values in registers A060-A06D. RX_FLAG shall be the logic OR of the bits in register xA071. The contents of the RX_FLAG status register are shown below. Bit 1 of RX_ALARM (RX_FLAG) will have the properties of latch high, clear on read (note that if the condition exists following register read, the bit will not be cleared).

Table 36 xA071 (113): RX_FLAG Status Bits

Bit	Description	Properties
7	Receive Optical Power High Alarm	O/RO
6	Receive Optical Power Low Alarm	O/RO
5:0	Reserved	RO

3. O - Optional
4. RO - Read Only, this register may be optionally implemented as read/write

11.4.4 RX_FLAG Control

RX_FLAG may be programmed to assert only when specific receive operation parameters exceed their alarm levels. The programming is performed by writing the contents of a mask register located at offset x9007. The contents of register xA071 shall be AND'ed with the contents of register x9007 prior to application of the OR function that generates the RX_FLAG signal.

Table 37 x9007: RX_FLAG Control Bits

Bit	Description	Default	Properties
7	Receive Optical Power High Alarm Enable	0	RW
6	Receive Optical Power Low Alarm Enable	0	RW
5:0	Reserved	0	RW

1. RW - Read/Write

12 Appendix 1A

12.1 Thermal Verification

The purpose of this appendix is to provide guidance to XENPAK suppliers to create a consistent test environment. This will identify the limiting or boundary conditions to help efficient thermal system design when using XENPAK modules.

Substantial variations in module thermal performance can occur depending on system level thermal design.

The parameters defined in this section shall enable clear communication of thermal simulation or thermal test data between module supplier and system vendor and will aid correlation between simulation and actual measured results

This document however does not guarantee system level performance or port density. This will be resolved on a system specific basis.

Any characterization results presented in this thermal section are given as examples only.

12.2 System design & assumptions for characterization, simulations and measurements

Information presented by the module vendor in relation to this document should be obtained from a 'confined or ducted flow' system as shown in Fig 24 and Fig 25.

A blower duct is mounted so that the direction of airflow is parallel to the heat sink fins.

Airflow measurement points are shown in Fig 26.

Airflow should be characterized using a calibrated hot wire anemometer placed at the airflow inlet (F1).

Thermocouples should be used to measure case temperatures at the worst-case location on a given design.

Each module vendor as a minimum requirement should provide measurement data, defined as recommended, in Fig 27

Identical PMD types will be expected to be characterized I.E. no mix of 850nm or 1310nm or 1550nm PMDs is mandated.

A minimum of 8 of 850nm or 1310nm PMDs will be tested whereas a minimum of 4, 1550nm parts are to be tested.

When undergoing thermal evaluation XENPAK transceivers should output idle patterns on both the XAUI and PMD outputs. The idle patterns for XAUI and PMD are described in IEEE802.3ae sections 48.2.4.2 and 49.2.4.7 respectively.

Other measurement data provided is at the discretion of the vendor.

12.2.1 Test Environment

- The system should provide uniform airflow across the vent opening and be of constant volume airflow.
- Altitude (sea level)
- Air humidity (50% ± 10)
- Inlet Air temperature (0°C to +50°C)
- Minimum airflow ($0.5ms^{-1}$)
- Maximum airflow ($3ms^{-1}$)

12.2.2 Test fixture

PCB motherboard must be 2.6 mm thick ±0.2mm and have no copper content between datum K and datum F (see Fig 2) except for a 4mm chassis ground, as shown in Fig 5.

- Space for an EMI shield as included in the MSA should be provided.
- A wind tunnel housing with poor thermal conduction will be used - a plastic (IR transparent to allow the potential use of an infrared camera) is recommended.
- Dimensions of system and other features are represented in the drawings documenting the test unit
- For the multiple module configurations it is assumed that the conditions drawn for module 1 will be duplicated for module 'N'. i.e. the EMI shield will be present for all modules.
- Blanking plates will be provided to close the front faceplate when modules are not inserted in test chamber slots but they will not fill the slot in the test PCB.
- For multiple module tests the modules will all be adjacent to one another with no gaps from empty test chamber slots. It is recommended to fill slots from the slot closest to the inlet and incrementally leewards as more modules are added.
- The test chamber will be clear of obstruction for 30cm after the outlet.

12.2.3 Module conditions

- A steady state should be obtained to take measurements.

Fig 24. Cross Section of Test Fixture

SEE Table 38 FOR DIMENSIONS

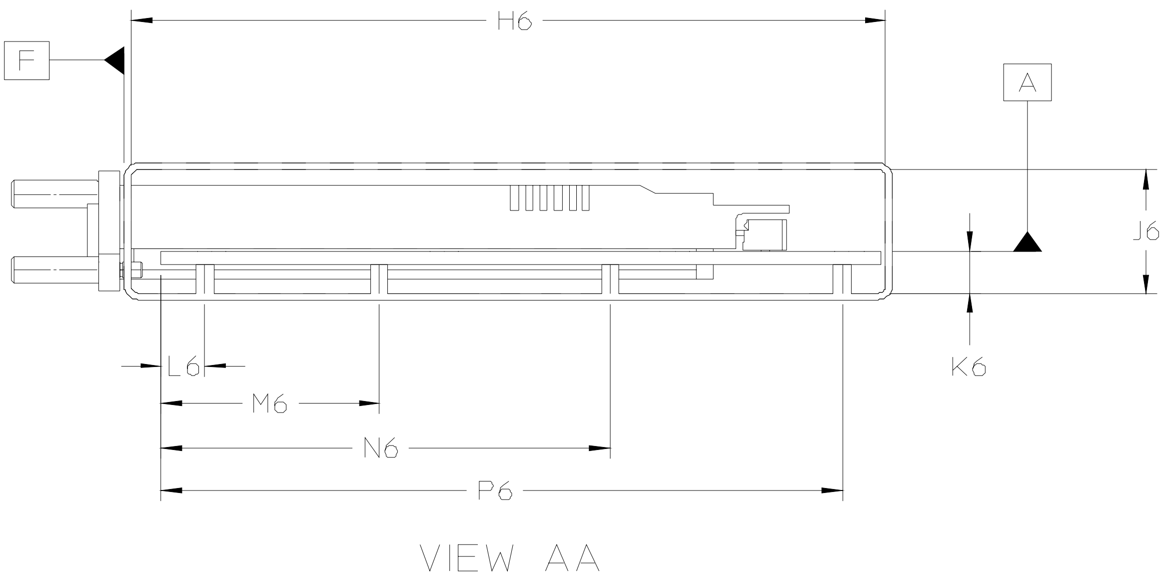
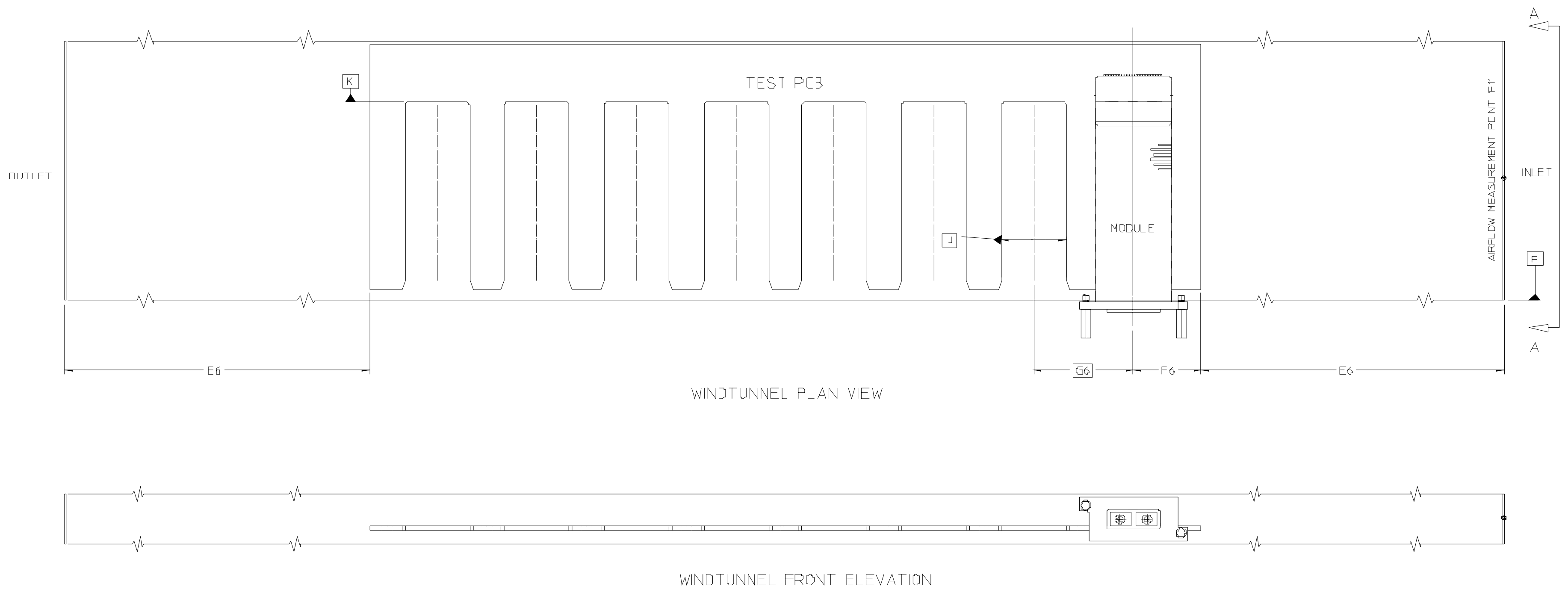


Fig 25. Plan and Side view of Test Fixture

SEE Table 38 FOR DIMENSIONS



12.2.4 Temperature measurement position.

The temperature should be measured at the worst-case location on a module for a given design, when measured under the conditions defined in this Appendix.

The results formats given in this MSA refer to results measured at this worst-case location.

12.2.5 Optional Airflow measurement points

To aid correlation of vendor simulation to vendor system test data, optional test points for airflow measurement have been defined, in close proximity to the module, as listed in Table 39 and are shown in Fig 26 below.

Fig 26. Optional air flow measurement points

SEE FOR Table 38 DIMENSIONS

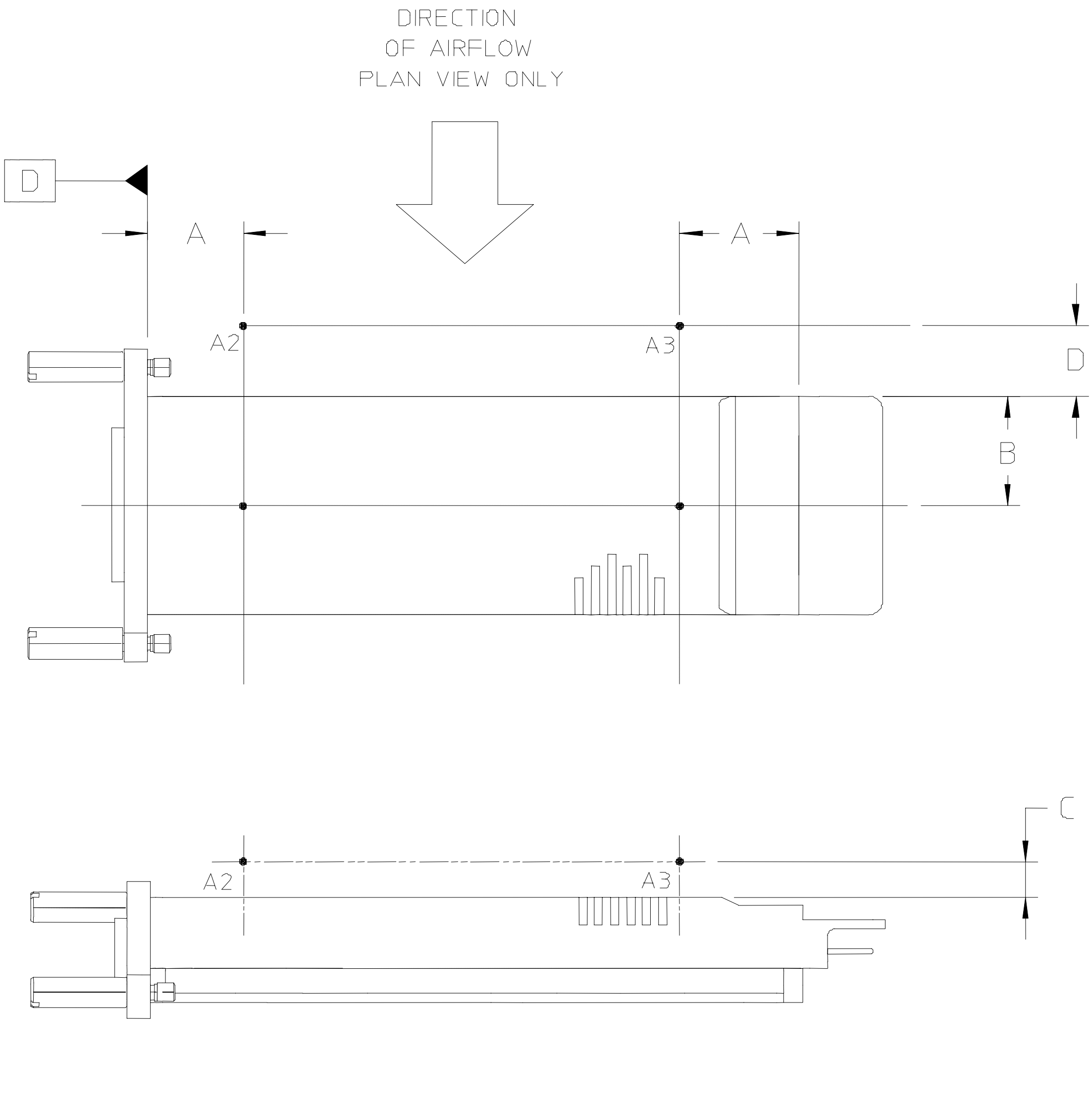


Table 38 Test chamber conditions and test-points locations

Key	Dim. (mm)	Tolerance	COMMENTS
A	25.0	± 2.0	
B	18	± 2.0	
C	2.0	± 0.5	
D	4.24	± 2.0	
E6	304.8	± 1.0	Spacing for measurement points
F6	32.0	± 1.0	Datum [-J-] to edge of customers PCB
G6	47.47	BASIC	Minimum Module spacing
H6	130.0	± 1.0	Width of inside Wind tunnel
J6	23.0	± 1.0	Height of Wind tunnel
K6	7.95	± 1.0	Datum [-A-] to bottom inside surface of Wind tunnel
L6	7.50	± 1.0	Mounting spacer
M6	37.50	± 1.0	Mounting spacer
N6	77.50	± 1.0	Mounting spacer
P6	117.50	± 1.0	Mounting spacer

Table 39 Optional Results for correlation.

A2, A3	-	-	Optional Air flow simulation or measurement test points

12.2.6 Example data

Example data collected according to 12.2.4 will be represented in chart as described in Fig 27.

Case temperature of the hottest module within in a multiple or single module configuration will conform to IEC 60950.

Fig 27. Case temperature vs Inlet air temperature and. airflow at reference point.