SFF-8472

Specification for

Management Interface for SFP+

Rev 12.4 March 31, 2021

SECRETARIAT: SFF TA TWG

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ABSTRACT: This specification defines an enhanced digital diagnostic monitoring interface for optical transceivers which allows real time access to device operating parameters, control and status registers.

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Change History

Rev.	Description	Date
1.0	Initial Submission of Document, Preliminary	2001-04-05
2.0	Draft Second Revision, Preliminary	2001-05-18
3.0	Draft Third Revision, Preliminary	2001-06-27
4.0	Draft Fourth Revision, Preliminary	2001-10-08
5.0	Draft Fifth Revision	2001-11-05
6.0	Draft Sixth Revision	2001-11-19
7.0	Draft Revision 7.0	2002-01-09
8.0	Draft Revision 8.0	2002-02-01
9.0	Draft Revision 9.0	2002-03-28
9.0	Revision 9.0 Approved for Technical Content	2002-05
9.2	Revision 9.2 Submitted for Publication	2002-05-30
9.3	Editorial Modifications to rev. 9.2. 9.3 Submitted for Publication	2002-08-01
9.4	Add extensions to include additional technologies. Results of Dec.5 03 discussions. Includes: Support for Multiple Application Selection Reserved values for SFF-8079 in Table 3.1, Table 3.10, Table 3.12, and Table 3.17. Additional transceiver type values in Table 3.5 Additional values in Table 3.1a, 3.5a and 3.5b Additional values in Table 3.12 General editorial modifications.	2004-05-26
9.5	Editorial Modifications to rev. 9.4. 9.5 Submitted for Publication.	2004-06-01
10.0	Add extensions to the following tables: Table 3.1b, 3.2, 3.4, 3.5, 3.5b, 3.7, 3.11, 3.12, 3.21 Editorial changes to the following tables: Table 3.2, 3.3, 3.4, 3.6, 3.7, 3.9, 3.10, 3.17 Add table 3.1a, 3.6a, 3.18a and references to 8079/8431.	2007-02-06
10.2	Editorial updates per ballot feedback. Technical update to Tables 3.1.	2007-06-01
10.3	Edits per SFF-8431	2007-12-07
10.4	Edits per SFF-8431, add bits in Table 3.5 and add Tables 3.6b and 3.6c for SFF-8431 and SFF-8461. Add Table 3.1c.	2009-01-30
11.0	Edits per FC-PI-5 (16GFC) to tables 3.6a,3.12,	2010-05-21
11.1	Table 3-2 Identifier Values and modified to point to SFF-8024 as the reference for later values and codes.	2012-10-26
11.2	Added FC-PI-6 to Table 3.6a Rate Identifier	2013-06-06
11.3	Added OM4 to Table 3.1 and Address A0h, Byte 18. Added 3200 MBytes to Table 3.5 Byte 10 Bit 3.	2013-06-11
11.4	Added optional support for: retimer/CDR in transceiver; Variable Receiver Decision Threshold; Rate Select logic for 10G/8G with bypassable CDRs; Table addressing in upper half of address A2h; Laser temperature and TEC current alarms and warnings; Compliance codes for OTN 2 km, 40 km and 80 km profiles in G.959.1.	2014-07-24
11.8	Introduced a major style change. The addition of Section, Figure, and Table numbering makes correlation of previous Change History difficult for readers, so a Cross Reference of Figures and Tables was prepared.	2014-07-31

Rev.	Description	Date
11.9	Re-defined byte 36 of Table 5-4 Transceiver Compliance Codes to be 'Extended Compliance Codes' Added definitions of the coding formats for optional laser temperature and TEC current to Section 9.2. Added Table 9-3 and Table 9-4 to illustrate the TEC current two's complement format. Corrected Table 10-2 Retimer/CDR Rate Select Logic Table 'Bit 64.1 of A2h' to be 'Bit 64.3 of A0h' Added Byte 64 Bit 5 in Table 8-3 to identify transceivers with Power Level 3 plus: o Renamed t_power_level2 to t_hpower_level in Table 8-7 and modified the contents of the parameter and conditions cells. o Changed the description for bits 1 and 0 in Table 10-1.	2014-08-14
11.9b	Moved CDR unlocked flags from byte A2h 115 to 119. Added Tx input EQ and RX output EMPH to bytes A2h 114-115 Added Tables 9-13 and 9-14 Tx input EQ and Rx output EMPH values.	2014-08-27
12.0	The mix of references to tables and pages was reduced to use only pages Consolidated the two figures in Section 4 into one. Corrected Table 4-4. Byte 12 G.959 value from 0Ah, to 6Bh Removed P1L1-2D1, P1S1-2D2, and P1L1-2D2 from Table 5-6	2014-08-28
12.1	During the review of Rev 12.0 it was recommended that: - the contents of Table 5-3 Connector Values be moved to SFF-8024. - the contents of Table 5-7 Encoding Values be returned to SFF-8024.	2014-09-12
12.2	Further updates to clarify operation of rate select with byte content 0Eh	2014-11-21
12.3	Added bits to support 64GFC speed negotiation Converted to SNIA template. Updated hyperlinks throughout.	2018-07-29
12.4	Replaced BR with Signaling rate and Gb/s with GBd throughout the document. Modified definition of bytes 14 and 15 in A0h, Table 4-1, to include copper cable attenuation values Added definition in Section 6.1 and 6.2. Modified definition of bytes 56-91 in A0h, Table 4-2, to be used for enhanced features when not used for External Calibration constants. Modified Fig.4-1 to show the new allocation. In Table 5-3 modified description for bit 1, byte 10 to refer to a secondary Fibre Channel Speed register 62. Added byte 62 to the table. Added value 20h in byte 13, Table 5-6 for Rate Select implementation based on PMDs. Modified name and definition of byte 19, in A0h to include cable length in base and multiplier format. Added Table 6-1. Added a High-Power Class declaration bit 6, byte 64 in Table 8-3. Added new value 09h in byte 94, Table 8-8 for SFF-8472, rev 12.4 compliance. Added Section 9.6 on Additional Enhanced Features, Table 9-11 with definitions for all bytes used, Tables 9-12 (Enhanced Control Advertisement), 9-13 (Enhanced Flag Advertisement), 9-14 (Enhanced Signal Integrity Control Advertisement), 9-15 (Enhanced Control). Modified name and definition of bit 0/byte110/A2h to clarify that this status refers to monitor data. Added bit 4, byte 118, A2h Adaptive Input EQ Fault indicator. Added bit 2, byte 118, A2h Enable Power Class 4. Modified definition of A2h, byte 119, bits 0,1,2,3 to be used for 50GE status. Added advertisement bit (A2h, byte 56, bit 4) and control bit (A2h, byte 72, bit 4) for ignoring the state of the HW RS0 and RS1 pins. Moved the RS0/1 ignore control from bit 4/ byte 72 to bit 4/ byte 73. Added bit 4/ byte 72 Rx Output Enhanced EQ Control Override control bit. Added Note 2 to Table 9-15 for recommended use of Tx Squelch Implementation control.	2021-03-31

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1. Scope

This document defines an enhanced memory map with a digital diagnostic monitoring interface for optical transceivers that allows pseudo real time access to device operating parameters.

The interface is an extension of the 2-wire interface ID interface defined in the GBIC specification as well as the SFP MSA. Both specifications define a 256 byte memory map which is accessible over a 2-wire serial interface at the 8 bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h), so the originally defined 2-wire interface ID memory map remains unchanged. The interface is backward compatible with both the GBIC specification and the SFP MSA.

In order to provide memory space for future extensions, multiple optional pages are defined for the upper 128 bytes of the A2h memory space.

2. References

INF-8074	SFP (Small Formfactor Pluggable) 1 Gb/s Transceiver
SFF-8024	SFF Module Management Reference Code Tables
SFF-8053	GBIC (Gigabit Interface Converter)
SFF-8079	SFP Rate and Application Selection
SFF-8089	SFP Rate and Application Codes
SFF-8418	SFP+ 10 Gb/s Electrical Interface
SFF-8419	SFP+ Power and Low Speed Interface
SFF-8431	SFP+ 10 Gb/s and Low Speed Electrical Interface
SFF-8690	Tunable SFP+ Memory Map for ITU Frequencies
INCITS FC-PI-4/5/6/7	Fibre Channel Physical Interface 4/5/6/7
IEEE Std 754	Standard for Floating-Point Arithmetic
IEEE Std 802.3	IEEE Standard for Ethernet

3. Enhanced Digital Diagnostic Interface - Introduction

The enhanced digital diagnostic interface is a superset of the MOD_DEF interface defined in the SFP MSA document dated September 14, 2000, later submitted to the SFF Committee as INF-8074. The 2-wire interface pin definitions, hardware, and timing was initially defined there. SFF-8431, later superseded by SFF-8419 define the low speed electrical and management interface specifications for SFP+.

This document describes an extension to the memory map defined in the SFP MSA (see Figure 4-1). The enhanced interface uses the 2-wire serial bus address 1010001X, commonly referred to as A2h, and where X can be 0 for a read operation or 1 for a write operation. Reads from this address provide diagnostic information about the module's present operating conditions. The transceiver generates this diagnostic data by digitization of internal analog signals. Calibration and alarm/warning threshold data is written during device manufacture.

All bits that are reserved for SFF-8472 shall be set to zero and/or ignored.

Bits labeled as reserved or optional for other usage, such as for SFF-8079, shall be implemented per such other documents, or set to zero and/or ignored if not implemented.

If optional features for SFF-8472 are implemented, they shall be implemented as defined in SFF-8472. If they are not implemented or not applicable to the device, then write bits shall be ignored, and status bits shall be set to zero.

Additional A0h and A2h memory allocations were provided in revision 9.5 to support multi-rate and application selection as defined in the SFF-8079 and SFF-8089 specifications.
Various extensions have been made in revisions since revision 10.4. These include adding new connectors, industry form factors, transceiver codes and controls for transceiver features.

4. Memory Organization

4.1 2-wire Interface Fields

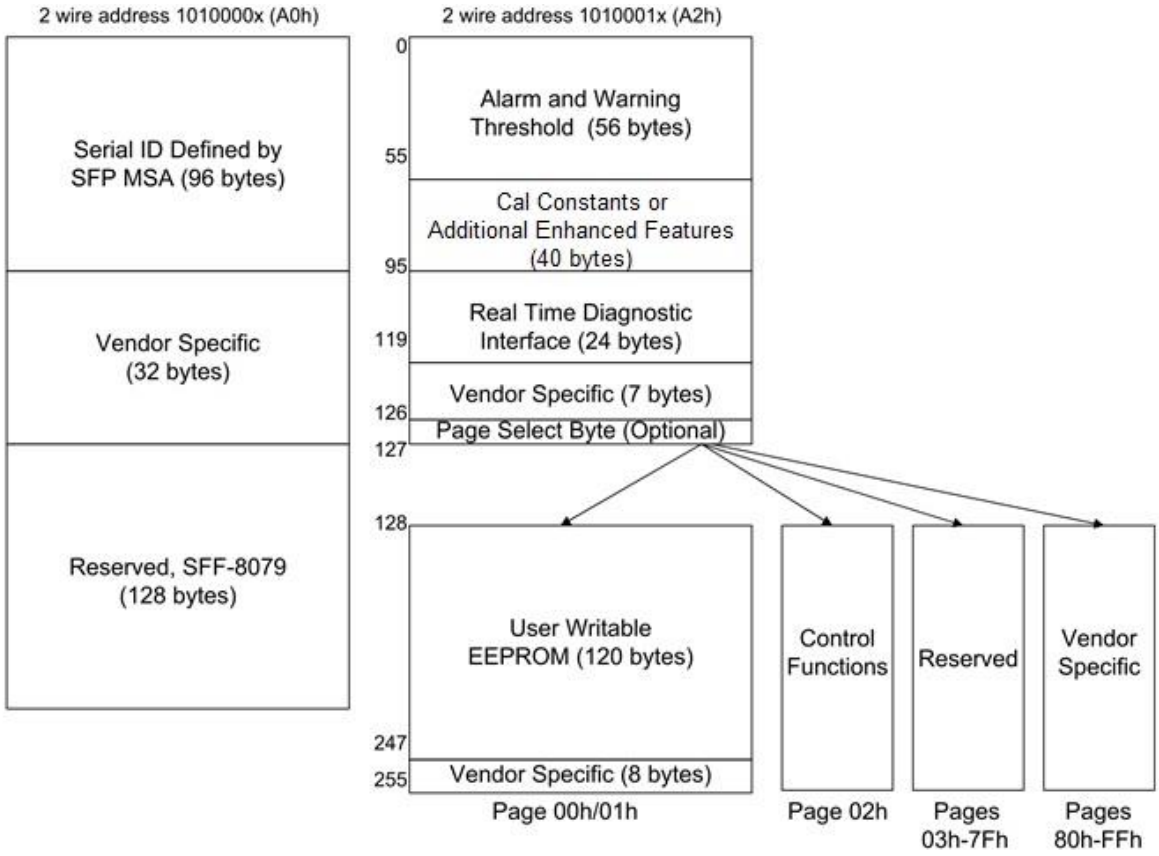

Figure 4-1 2-wire Interface Fields

4.2 Pages

The optional Page Select byte expands the range of information that can be provided by the manufacturer. Where used in this specification the Page ID is defined in hexadecimal. Note: Vendor Specific IDs may be password-protected.

4.3 Data Fields

Table 4-1 Data Fields - Address A0h

A0h	# Bytes	Name	Description
BASE ID FIELDS			
0	1	Identifier	Type of transceiver (see Table 5-1)
1	1	Ext. Identifier	Extended identifier of type of transceiver (see Table 5-2)
2	1	Connector	Code for connector type (see SFF-8024 SFF Module Management Reference Code Tables)
3-10	8	Transceiver	Code for electronic or optical compatibility (see Table 5-3)
11	1	Encoding	Code for high speed serial encoding algorithm (see SFF-8024 SFF Module Management Reference Code Tables)
12	1	Signaling Rate, Nominal	Nominal signaling rate, units of 100 MBd. (see details for rates > 25.4 GBd)
13	1	Rate Identifier	Type of rate select functionality (see Table 5-6)
14	1	Length (SMF,km) or Copper Cable Attenuation	Link length supported for single-mode fiber, units of km, or copper cable attenuation in dB at 12.9 GHz
15	1	Length (SMF) or Copper Cable Attenuation	Link length supported for single-mode fiber, units of 100 m, or copper cable attenuation in dB at 25.78 GHz
16	1	Length (50 um, OM2)	Link length supported for 50 um OM2 fiber, units of 10 m
17	1	Length (62.5 um, OM1)	Link length supported for 62.5 um OM1 fiber, units of 10 m
18	1	Length (OM4 or copper cable)	Link length supported for 50um OM4 fiber, units of 10 m. Alternatively, copper or direct attach cable, units of m
19	1	Length (OM3) or Cable length, additional	Link length supported for 50 um OM3 fiber, units of 10 m. Alternatively, copper or direct attach cable multiplier and base value
20-35	16	Vendor name	SFP vendor name (ASCII)
36	1	Transceiver	Code for electronic or optical compatibility (see Table 5-3)
37-39	3	Vendor OUI	SFP vendor IEEE company ID
40-55	16	Vendor PN	Part number provided by SFP vendor (ASCII)
56-59	4	Vendor rev	Revision level for part number provided by vendor (ASCII)
60-61	2	Wavelength	Laser wavelength (Passive/Active Cable Specification Compliance)
62	1	Fibre Channel Speed 2	Transceiver's Fibre Channel speed capabilities
63	1	CC_BASE	Check code for Base ID Fields (addresses 0 to 62)
EXTENDED ID FIELDS			
64-65	2	Options	Indicates which optional transceiver signals are implemented (see Table 8-3)
66	1	Signaling Rate, max	Upper signaling rate margin, units of % (see details for rates > 25.4 GBd)
67	1	Signaling Rate, min	Lower signaling rate margin, units of % (see details for rates > 25.4 GBd)
68-83	16	Vendor SN	Serial number provided by vendor (ASCII)
84-91	8	Date code	Vendor's manufacturing date code (see Table 8-4)
92	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the transceiver (see Table 8-5)
93	1	Enhanced Options	Indicates which optional enhanced features are implemented (if any) in the transceiver (see Table 8-6)
94	1	SFF-8472 Compliance	Indicates which revision of SFF-8472 the transceiver complies with. (see Table 8-8)
95	1	CC_EXT	Check code for the Extended ID Fields (addresses 64 to 94)
VENDOR SPECIFIC ID FIELDS			
96-127	32	Vendor Specific	Vendor Specific EEPROM
128-255	128	Reserved	Reserved (was assigned to SFF-8079)

Table 4-2 Data Fields - Address A2h

A2h	# Bytes	Name	Description
DIAGNOSTIC AND CONTROL/STATUS FIELDS			
0-39	40	A/W Thresholds	Diagnostic Flag Alarm and Warning Thresholds (see Table 9-5)
40-55	16	Optional A/W Thresholds	Thresholds for optional Laser Temperature and TEC Current alarms and warnings (see Table 9-5)
56-91	36	Ext Cal Constants or Additional Enhanced Features	Diagnostic calibration constants for optional External Calibration (see Table 9-6) if External Calibration bit, A0h, byte 92, bit 4 is 1 Additional Enhanced Features advertisement, control and status (see Table 9-11) if External Calibration bit, A0h, byte 92, bit 4 is 0
92-94	3	Reserved	
95	1	CC_DMI	Check code for Base Diagnostic Fields (addresses 0 to 94)
96-105	10	Diagnostics	Diagnostic Monitor Data (internally or externally calibrated) (see Table 9-16)
106-109	4	Optional Diagnostics	Monitor Data for Optional Laser temperature and TEC current (see Table 9-16)
110	1	Status/Control	Optional Status and Control Bits (see Table 9-16)
111	1	Reserved	Reserved (was assigned to SFF-8079)
112-113	2	Alarm Flags	Diagnostic Alarm Flag Status Bits (see Table 9-17)
114	1	Tx Input EQ control	Tx Input equalization level control (see Table 9-18)
115	1	Rx Out Emphasis control	Rx Output emphasis level control (see Table 9-19)
116-117	2	Warning Flags	Diagnostic Warning Flag Status Bits (see Table 9-17)
118-119	2	Ext Status/Control	Extended module control and status bytes (see Table 10-1)
GENERAL USE FIELDS			
120-126	7	Vendor Specific	Vendor specific memory addresses (see Table 10-3)
127	1	Table Select	Optional Page Select (see Table 10-3)

Table 4-3 Data Fields - Address A2h Page Tables

A2h	# Bytes	Name	Description
Page 00-01h			
128-247	120	User EEPROM	User writable non-volatile memory (see Table 10-4)
248-255	8	Vendor Control	Vendor specific control addresses (see Table 10-5)
Page 02h			
128-129	2	Reserved	Reserved for SFF-8690 (Tunable Transmitter)
130	1	Reserved	Reserved for future receiver controls
131	1	Rx Decision Threshold	RDT value setting
132-172	41	Reserved	Reserved for SFF-8690
173-255	83	Reserved	

The examples of transceiver and copper cable performance codes below are provided for illustration. Compliance to additional standards and technologies is possible so bits other than those indicated in each row may also be set to indicate compliance to these additional standards and technologies.

Table 4-4 Transceiver Identification/Performance Examples

		Address A0h						
		Rate and Distance Fields						Wave-length Fields
Transceiver Type	**Transceiver Description**	**Byte 12**	**Byte 14**	**Byte 15**	**Byte 16**	**Byte 17**	**Byte 18**	**Bytes 60 & 61**
100-M5-SN-I and 100-M6-SN-I	1062.5 MBd MM 850 nm 500m/50um, 300m/62.5um	0Bh	00h	00h	32h	1Eh	00h	0352h
200-SM-LC-L and 100-SM-LC-L	2125 MBd and 1062.5 MBd 10 km SM 1310 nm	15h[3]	0Ah[3]	64h[3]	00h	00h	00h	051Eh
400-M5-SN-I and 400-M6-SN-I 4	4250 MBd MM 850 nm 150m/50 um, 70m/62.5 um	2Bh[3]	00h	00h	0Fh[3]	07h[3]	00h	0352h
400-SM-LC-M	4250 MBd SM 1310 nm 4 km "medium" length	2Bh[3]	04h	28h	00h	00h	00h	051Eh
400-SM-LC-L	4250 MBd SM 1310 nm 10 km "long" length	2Bh[3]	0Ah	64h	00h	00h	00h	051Eh
200-SM-LL-V and 100-SM-LL-V	2125 MBd and 1062.5 MBd 50 km SM 1550 nm	15h[3]	32h	FFh	00h	00h	00h	060Eh
ESCON SM	200 MBd 20 km SM 1310 nm	02h	14h	C8h	00h	00h	00h	051Eh
100BASE-LX10	125 MBd 10 km SM 1310 nm	01h	0Ah	64h	00h	00h	00h	051Eh
1000BASE-T	1250 MBd 100 m Cat 5 Cable	0Dh[1]	00h	00h	00h	00h	64h	0000h
1000BASE-SX	1250 MBd 550 m MM 850 nm	0Dh[1]	00h	00h	37h[2]	1Bh[2]	00h	0352h
1000BASE-LX	1250 MBd 5 km SM 1310 nm	0Dh[1]	05h	32h	37h	37h	00h	051Eh
1000BASE-LX10	1250 MBd 10 km SM 1310 nm	0Dh[1]	0Ah	64h	00h	00h	00h	051Eh
1000BASE-BX10-D	1250 MBd 10 km SM 1490 nm downstream TX	0Dh[1]	0Ah	64h	00h	00h	00h	05D2h
1000BASE-BX10-U	1250 MBd 10 km SM 1310 nm upstream TX	0Dh[1]	0Ah	64h	00h	00h	00h	051Eh
OC3/STM1 SR-1	155 MBd 2 km SM 1310 nm	02h	02h	14h	00h	00h	00h	051Eh
OC12/STM4 LR-1	622 MBd 40 km SM 1310 nm	06h[3]	28h	FFh	00h	00h	00h	051Eh
OC48/STM16 LR-2	2488 MBd 80 km SM 1550 nm	19h[3]	50h	FFh	00h	00h	00h	060Eh
G959.1 P1I1-2D1	10709 MBd 2 km SM 1310 nm	6Bh	02h[5]	14h	00h	00h	00h	051Eh
G959.1 P1S1-2D2	10709 MBd 40 km SM 1550 nm	6Bh	28h[5]	FFh	00h	00h	00h	060Eh
G959.1 P1L1-2D2	10709 MBd 80 km SM 1550 nm	6Bh	50h[5]	FFh	00h	00h	00h	060Eh

NOTES:
1. By convention 1.25 GBd should be rounded up to 0Dh (13 in units of 100 MBd) for Ethernet 1000BASE-X.
2. Link distances for 1000BASE-SX variants vary between high and low bandwidth cable types per IEEE Std

802.3 Clause 38. The values shown are 270 m [275 m per 802.3] for 62.5 um / 200 MHz*km cable and 550 m for 50 um / 500 MHz*km cable.
3. For transceivers supporting multiple data rates (and hence multiple distances with a single fiber type) the highest data rate and the distances achievable at that data rate are to be identified in these fields.
4. In this example, the transceiver supports 400-M5-SN-I, 200-M5-SN-I, 100-M5-SN-I, 400-M6-SN-I, 200-M6-SN-I and 100-M6-SN-I.
5. These target distances are for classification and not for specification.

Table 4-5 Copper Cable Identification/Performance Examples

	Address A0h		
	Link Length and Transmitter Technology		Laser wavelength and Cable Specification Compliance
Cable Type	**Byte 7**	**Byte 8**	**Bytes 60 and 61**
Passive Cable compliant to SFF-8431 Appendix E.	00h	04h	0100h
Active cable compliant to SFF-8431 Appendix E	00h	08h	0100h
Active cable compliant to SFF-8431 limiting	00h	08h	0400h
Active cable compliant to both SFF-8431 limiting and FC-PI-4 limiting	00h	08h	0C00h

5. Identifiers and Codes

5.1 Physical Device Identifier Values [Address A0h, Byte 0]

The identifier value identifies the physical device described by 2-wire interface information. This value shall be included in the 2-wire interface data.

Table 5-1 Physical Device Identifier Values

A0h	Value	Description
0	00h	Unknown or unspecified
	01h	GBIC
	02h	Module soldered to motherboard (ex: SFF)
	03h	SFP or SFP+
	04-7Fh	Not used by this specification. These values are maintained in the Transceiver or Cable Management section of SFF-8024.
	80-FFh	Vendor specific

5.2 Physical Device Extended Identifier Values [Address A0h, Byte 1]

The extended identifier value provides additional information about the transceiver. The field should be set to 04h for all SFP modules indicating 2-wire interface ID module definition. In many cases, a GBIC elects to use MOD_DEF 4 to make additional information about the GBIC available, even though the GBIC is actually compliant with one of the six other MOD_DEF values defined for GBICs. The extended identifier allows the GBIC to explicitly specify such compliance without requiring the MOD_DEF value to be inferred from the other information provided.

Table 5-2 Physical Device Extended Identifier Values

A0h	Value	Description of connector
1	00h	GBIC definition is not specified or the GBIC definition is not compliant with a defined MOD_DEF. See product specification for details.
	01h	GBIC is compliant with MOD_DEF 1
	02h	GBIC is compliant with MOD_DEF 2
	03h	GBIC is compliant with MOD_DEF 3
	04h	GBIC/SFP function is defined by 2-wire interface ID only
	05h	GBIC is compliant with MOD_DEF 5
	06h	GBIC is compliant with MOD_DEF 6
	07h	GBIC is compliant with MOD_DEF 7
	08-FFh	Reserved

5.3 Connector Values [Address A0h, Byte 2]

The connector value indicates the external optical or electrical cable connector provided as the media interface. This value shall be included in the 2-wire interface data. These values are maintained in the Transceiver or Cable Management section of SFF-8024.

5.4 Transceiver Compliance Codes [Address A0h, Bytes 3 to 10, 36 and 62]

The following bit significant indicators in bytes 3 to 10 and code in byte 36 define the electronic or optical interfaces that are supported by the transceiver. At least one bit shall be set in this field. For Fibre Channel transceivers, the Fibre Channel speed, transmission media, transmitter technology, and distance capability shall all be indicated. SONET compliance codes are completed by including the contents of Table 5-4. Ethernet, ESCON and InfiniBand codes have been included to broaden the available applications of SFP transceivers.

Table 5-3 Transceiver Compliance Codes

A0h	Bit [1]	Description
Extended Specification Compliance Codes		
36	7-0	See SFF-8024 Table 4-4
10G Ethernet Compliance Codes		
3	7	10GBASE-ER
3	6	10GBASE-LRM
3	5	10GBASE-LR
3	4	10GBASE-SR
Infiniband Compliance Codes		
3	3	1X SX
3	2	1X LX
3	1	1X Copper Active
3	0	1X Copper Passive
ESCON Compliance Codes		
4	7	ESCON MMF, 1310nm LED
4	6	ESCON SMF, 1310nm Laser
SONET Compliance Codes		
4	5	OC-192, short reach [2]
4	4	SONET reach specifier bit 1
4	3	SONET reach specifier bit 2
4	2	OC-48, long reach [2]
4	1	OC-48, intermediate reach [2]
4	0	OC-48, short reach [2]
5	7	Reserved
5	6	OC-12, single mode, long reach [2]
5	5	OC-12, single mode, inter. reach [2]
5	4	OC-12, short reach [2]
5	3	Reserved
5	2	OC-3, single mode, long reach [2]
5	1	OC-3, single mode, inter. reach [2]
5	0	OC-3, short reach [2]
Ethernet Compliance Codes		
6	7	BASE-PX [3]
6	6	BASE-BX10 [3]
6	5	100BASE-FX
6	4	100BASE-LX/LX10
6	3	1000BASE-T
6	2	1000BASE-CX
6	1	1000BASE-LX [3]
6	0	1000BASE-SX

A0h	Bit [1]	Description
Fibre Channel Link Length		
7	7	very long distance (V)
7	6	short distance (S)
7	5	intermediate distance (I)
7	4	long distance (L)
7	3	medium distance (M)
Fibre Channel Technology		
7	2	Shortwave laser, linear Rx (SA) [7]
7	1	Longwave laser (LC) [6]
7	0	Electrical inter-enclosure (EL)
8	7	Electrical intra-enclosure (EL)
8	6	Shortwave laser w/o OFC (SN) [7]
8	5	Shortwave laser with OFC (SL) [4]
8	4	Longwave laser (LL) [5]
SFP+ Cable Technology		
8	3	Active Cable [8]
8	2	Passive Cable [8]
8	1-0	Reserved
Fibre Channel Transmission Media		
9	7	Twin Axial Pair (TW)
9	6	Twisted Pair (TP)
9	5	Miniature Coax (MI)
9	4	Video Coax (TV)
9	3	Multimode, 62.5um (M6)
9	2	Multimode, 50um (M5, M5E)
9	1	Reserved
9	0	Single Mode (SM)
Fibre Channel Speed		
10	7	1200 MBytes/sec
10	6	800 MBytes/sec
10	5	1600 MBytes/sec
10	4	400 MBytes/sec
10	3	3200 MBytes/sec
10	2	200 MBytes/sec
10	1	See byte 62 "Fibre Channel Speed 2"
10	0	100 MBytes/sec
Fibre Channel Speed 2		
62	7-1	Reserved
62	0	64 GFC

NOTES:

1. Bit 7 is the high order bit and is transmitted first in each byte.
2. SONET compliance codes require reach specifier bits 3 and 4 in Table 5-4 to completely specify transceiver capabilities.
3. Ethernet LX, PX and BX compliance codes require the use of the Signaling Rate, Nominal value (byte 12), link length values for single-mode and two types of multimode fiber (Bytes 14-17) and wavelength value for the laser (Bytes 60 and 61) as specified in Table 4-1 to completely specify transceiver capabilities. See Table 4-3 and Table 5-6 for examples of setting values for these parameters.
4. Open Fiber Control (OFC) is a legacy eye safety electrical interlock system implemented on Gigabit Link Module (GLM) type transceiver devices and is not considered relevant to SFP transceivers.
5. Laser type "LL" (long length) is usually associated with 1550 nm, narrow spectral width lasers capable of very long link lengths.
6. Laser type "LC" (low cost) is usually associated with 1310 nm lasers capable of medium to long link lengths.
7. Classes SN and SA are mutually exclusive. Both are without OFC. SN has a limiting Rx output, SA has a linear Rx output, per

A0h	Bit [1]	Description		A0h	Bit [1]	Description
FC-PI-4.						
8. Refer to bytes 60 and 61 for definitions of the application copper cable standard specification.						

5.4.1 SONET Reach Specifier Bits [Address A0h, Byte 4, bits 3-4]

The SONET compliance code bits allow the host to determine with which specifications a SONET transceiver complies. For each rate defined in Table 5-3 (OC-3, OC-12, OC-48), SONET specifies short reach (SR), intermediate reach (IR), and long reach (LR) requirements. For each of the three rates, a single short reach (SR) specification is defined. Two variations of intermediate reach (IR-1, IR-2) and three variations of long reach (LR-1, LR-2, and LR-3) are also defined for each rate. Byte 4, bits 0-2, and byte 5, bits 0-7 allow the user to determine which of the three reaches has been implemented - short, intermediate, or long. Two additional 'specifier' bits (byte 4, bits 3-4) are necessary to discriminate between different intermediate or long reach variations.

Table 5-4 SONET Reach Specifier Bits

Speed	Reach	Specifier bit 1 (Byte 4 bit 4)	Specifier bit 2 (Byte 4 bit 3)	Description
OC 3/OC 12/OC 48/OC 192	Short	0	0	SONET SR compliant [1]
OC 3/OC 12/OC 48/OC 192	Short	1	0	SONET SR-1 compliant [2]
OC 3/OC 12/OC 48	Intermediate	1	0	SONET IR-1 compliant
OC 3/OC 12/OC 48	Intermediate	0	1	SONET IR-2 compliant
OC 3/OC 12/OC 48	Long	1	0	SONET LR-1 compliant
OC 3/OC 12/OC 48	Long	0	1	SONET LR-2 compliant
OC 3/OC 12/OC 48	Long	1	1	SONET LR-3 compliant

NOTES:
1. OC 3/OC 12 SR is multimode based short reach
2. OC 3/OC 12 SR-1 is single-mode based short reach

5.4.2 Examples of Transceiver Compliance Codes [Address A0h, Bytes 3-10]

Table 5-5 provides examples of the contents of bytes 3 to 10 for several transceiver types.

Table 5-5 Transceiver Identification Examples

		Address A0h Transceiver Code Fields							
Transceiver Type	**Transceiver Description**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**	**Byte 8**	**Byte 9**	**Byte 10**
100-M5-SN-I and 100-M6-SN-I	1062.5 MBd MM 850 nm 500m/50um, 300m/62.5um	00h	00h	00h	00h	20h	40h	0Ch	01h
200-SM-LC-L and 100-SM-LC-L	2125 MBd 10 km SM 1310 nm	00h	00h	00h	00h	12h	00h	01h	05h
400-M5-SN-I and 400-M6-SN-I [1]	4/2/1 GBd MM 850 nm 150m/50um, 70m/62.5um	00h	00h	00h	00h	20h	40h	0Ch	15h
800-M5-SN-I and 800-M6-SN-I [1]	8/4/2 GBd MM 850 nm 50 um & 62.5 um	00h	00h	00h	00h	20h	40h	0Ch	54h
400-SM-LC-M [1]	4250 MBd SM 1310 nm 4 km "medium" length	00h	00h	00h	00h	0Ah	00h	01h	15h
400-SM-LC-L [1]	4250 MBd SM 1310 nm 10 km "long" length	00h	00h	00h	00h	12h	00h	01h	15h
200-SM-LL-V and 100-SM-LL-V	2125 MBd 50 km SM 1550 nm	00h	00h	00h	00h	80h	10h	01h	05h
1000BASE-T	1250 MBd 100 m Cat 5 Cable	00h	00h	00h	08h	00h	00h	00h	00h
1000BASE-SX	1250 MBd 550 m MM 850 nm	00h	00h	00h	01h	00h	00h	00h	00h
1000BASE-LX	1250 MBd 5 km SM 1310 nm	00h	00h	00h	02h[2]	00h	00h	00h	00h
1000BASE-LX10	1250 MBd 10 km SM 1310 nm	00h	00h	00h	02h[2]	00h	00h	00h	00h
10GBASE-SR	10.3125 GBd 300 m OM3 MM 850 nm	10h	00h	00h	00h	00h	00h	00h	00h
10GBASE-LR	10.3125 GBd 10 km SM 1310 nm	20h	00h	00h	00h	00h	00h	00h	00h
OC3/STM1 SR-1	155 MBd 2 km SM 1310 nm	00h	00h	01h	00h	00h	00h	00h	00h
OC12/STM4 LR-1	622 MBd 40 km SM 1310 nm	00h	10h	40h	00h	00h	00h	00h	00h
OC48/STM16 LR-2	2488 MBd 80 km SM 1550 nm	00h	0Ch	00h	00h	00h	00h	00h	00h
	10GE Passive copper cable with SFP ends [3,4]	00h	00h	00h	00h	00h	04h	00h	00h
	10GE Active cable with SFP ends [3,4]	00h	00h	00h	00h	00h	08h	00h	00h
	8/4/2G Passive copper cable with SFP ends[3]	00h	00h	00h	00h	00h	04h	00h	54h
	8/4/2G Active cable with SFP ends[3]	00h	00h	00h	00h	00h	08h	00h	54h

NOTES:

1. The assumption for this example is the transceiver is "4-2-1" compatible, meaning operational at 4.25 GBd, 2.125 GBd and 1.0625 GBd.
2. To distinguish between 1000BASE-LX and 1000BASE-LX10, A0h Bytes 12 to 18 must be used. See Table 4-1 and Table 4-2 for more information.
3. See A0h Bytes 60 and 61 for compliance of these media to industry electrical specifications.

		Address A0h Transceiver Code Fields							
Transceiver Type	**Transceiver Description**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**	**Byte 8**	**Byte 9**	**Byte 10**
4. For Ethernet and SONET applications, rate capability of a link is identified in A0h Byte 12 [nominal signaling rate identifier]. This is due to no formal IEEE designation for passive and active cable interconnects, and lack of corresponding identifiers in Table 5-3.									

5.5 Encoding [Address A0h, Byte 11]

The encoding value indicates the encoding mechanism that is the nominal design target of the particular transceiver. The value shall be contained in the 2-wire interface data. These values are maintained in the Transceiver or Cable Management section of SFF-8024.

5.6 Signaling rate, nominal [Address A0h, Byte 12]

The nominal signaling rate is specified in units of 100 MBd, rounded off to the nearest 100 MBd. The signaling rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of FFh indicates the signaling rate is greater than 25.4 GBd and addresses 66 and 67 are used to determine the signaling rate. A value of 0 indicates that the signaling rate is not specified and must be determined from the transceiver technology. The actual information transfer rate will depend on the encoding of the data, as defined by the encoding value.

5.7 Rate Identifier [Address A0h, Byte 13]

The rate identifier byte refers to several (optional) industry standard definitions of Rate_Select or Application_Select control behaviors, intended to manage transceiver optimization for multiple operating rates.

Table 5-6 Rate Identifier

A0h	Value	Description
13	00h	Unspecified
	01h	SFF-8079 (4/2/1G Rate_Select & AS0/AS1)
	02h	SFF-8431 (8/4/2G Rx Rate_Select only)
	03h	Unspecified *
	04h	SFF-8431 (8/4/2G Tx Rate_Select only)
	05h	Unspecified *
	06h	SFF-8431 (8/4/2G Independent Rx & Tx Rate_select)
	07h	Unspecified *
	08h	FC-PI-5 (16/8/4G Rx Rate_select only) High=16G only, Low=8G/4G
	09h	Unspecified *
	0Ah	FC-PI-5 (16/8/4G Independent Rx, Tx Rate_select) High=16G only, Low=8G/4G
	0Bh	Unspecified *
	0Ch	FC-PI-6 (32/16/8G Independent Rx, Tx Rate_Select) High=32G only, Low = 16G/8G
	0Dh	Unspecified *
	0Eh	10/8G Rx and Tx Rate_Select controlling the operation or locking modes of the internal signal conditioner, retimer or CDR, according to the logic table defined in Table 10-2, High Bit Rate (10G) =9.95-11.3 Gb/s; Low Bit Rate (8G) = 8.5 Gb/s. In this mode, the default value of bit 110.3 (Soft Rate Select RS(0), Table 9-16) and of bit 118.3 (Soft Rate Select RS(1), Table 10-1) is 1.
	0Fh	Unspecified *
	10h	FC-PI-7 (64/32/16G Independent Rx, Tx Rate Select) High = 32GFC and 64GFC. Low = 16GFC.
	11h	Unspecified *
	12h -1Fh	Reserved
	20h	Rate select based on PMDs as defined by A0h, byte 36 and A2h, byte 67 (Rx, Tx Rate Select) High = A0h, Byte 36 PMD, Low = A2h, Byte 67 PMD
	21h-FFh	Reserved
* To support legacy, the LSB is reserved for Unspecified or INF-8074 (value = 0) or 4/2/1G selection per SFF-8079 (value = 1). Other rate selection functionalities are not allowed to depend on the LSB.		

6. Link Length

6.1 Length (single mode, km) or Copper Cable Attenuation [Address A0h, Byte 14]

Addition to EEPROM data from original GBIC definition. This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using single-mode fiber. The value is in units of kilometers. A value of 255 means that the transceiver supports a link length greater than 254 km. A value of zero means that the transceiver does not support single-mode fiber or that the length information must be determined from the transceiver technology.

For copper cable assemblies, this field is used to record the cable attenuation (or apparent attenuation from the near end of the cable for active cables) at 12.9 GHz in units of 1 dB. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

6.2 Length (single mode, 100s m) or Copper Cable Attenuation [Address A0h, Byte 15]

This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using single-mode fiber. The value is in units of 100 meters. A value of 255 means that the transceiver supports a link length greater than 25.4 km. A value of zero means that the transceiver does not support single-mode fiber or that the length information must be determined from the transceiver technology.

For copper cable assemblies, this field is used to record the cable attenuation (or apparent attenuation from the near end of the cable for active cables) at 25.78 GHz in units of 1 dB. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

6.3 Length (50 um, OM2) [Address A0h, Byte 16]

This value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 50 micron multimode OM2 [500 MHz*km at 850 nm] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 50 micron multimode OM2 fiber or that the length information must be determined from the transceiver technology.

6.4 Length (62.5 um, OM1) [Address A0h, Byte 17]

This value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 62.5 micron multimode OM1 [200 MHz*km at 850 nm, 500 MHz*km at 1310 nm] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 62.5 micron multimode fiber or that the length information must be determined from the transceiver technology. It is common for a multimode transceiver to support OM1, OM2 and OM3 fiber.

6.5 Length (50 um, OM4) and Length (Active Cable or Copper) [Address A0h, Byte 18]

For optical links, this value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 50 micron multimode OM4 [4700 MHz*km] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 50 micron OM4 multimode fiber or that the length information must be determined from the transceiver codes specified in Table 5-3.

For copper links, this value specifies minimum link length in meters supported by the transceiver while operating in compliance with applicable standards using copper cable. For active cable, this value represents actual length. The value is in units of 1 meter. A value of 255 means the transceiver supports a link length greater than 254 meters. A value of zero means the transceiver does not support copper or active cables or that the length can be determined from transceiver technology. Further information about cable design, equalization, and connectors is usually required to guarantee meeting a particular length requirement.

6.6 Length (50 um, OM3) and Length (Active Cable or Copper), additional [Address A0h, Byte 19]

This value specifies link length that is supported by the transceiver while operating in compliance with applicable standards using 50 micron multimode OM3 [2000 MHz*km] fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 50 micron multimode OM3 fiber or that the length information must be determined from the transceiver technology.

For active cable or copper cable, this value specifies the physical interconnect length supported in the following format:

Table 6-1 Cable Length, Additional

A0h	Bit	Name	Description
19	7-6	Length multiplier field (copper or active cable)	Multiplier for value in bits 5-0. 00b – multiplier of 0.1 01b – multiplier of 1 10b - multiplier of 10 11b – multiplier of 100
	5-0	Base length field (copper or active cable)	Link length base value in meters. To calculate actual link length use multiplier in bits 7-6

7. Vendor Fields

7.1 Vendor name [Address A0h, Bytes 20-35]

The vendor name is a 16-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid data.

7.2 Vendor OUI [Address A0h, Bytes 37-39]

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

7.3 Vendor PN [Address A0h, Bytes 40-55]

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

7.4 Vendor Rev [Address A0h, Bytes 56-59]

The vendor revision number (vendor rev) is a 4-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the Vendor's product revision number. A value of all zero in the 4-byte field indicates that the vendor revision is unspecified.

8. Link Characteristics

8.1 Optical and Cable Variants Specification Compliance [Address A0h, Bytes 60-61]

For optical variants, as defined by having zeros in A0h Byte 8 bits 2 and 3, Bytes 60 and 61 denote nominal transmitter output wavelength at room temperature. 16-bit value with byte 60 as high order byte and byte 61 as low order byte. The laser wavelength is equal to the 16-bit integer value in nm. This field allows the user to read the laser wavelength directly, so it is not necessary to infer it from the Transceiver Codes A0h Bytes 3 to 10 (see Table 5-3). This also allows specification of wavelengths not covered in the Transceiver Codes, such as those used in coarse WDM systems.

For passive and active cable variants, a value of 00h for both A0h Byte 60 and Byte 61 denotes laser wavelength or cable specification compliance is unspecified.

Table 8-1 Passive Cable Specification Compliance (A0h Byte 8 Bit 2 set)

A0h	Bit	Description	A0h	Bit	Description
60	7	Reserved	61	7	Reserved
60	6	Reserved	61	6	Reserved
60	5	Reserved for SFF-8461	61	5	Reserved
60	4	Reserved for SFF-8461	61	4	Reserved
60	3	Reserved for SFF-8461	61	3	Reserved
60	2	Reserved for SFF-8461	61	2	Reserved
60	1	Compliant to FC-PI-4 Appendix H	61	1	Reserved
60	0	Compliant to SFF-8431 Appendix E	61	0	Reserved

Table 8-2 Active Cable Specification Compliance (A0h Byte 8 Bit 3 set)

A0h	Bit	Description	A0h	Bit	Description
60	7	Reserved	61	7	Reserved
60	6	Reserved	61	6	Reserved
60	5	Reserved	61	5	Reserved
60	4	Reserved	61	4	Reserved
60	3	Compliant to FC-PI-4 Limiting	61	3	Reserved
60	2	Compliant to SFF-8431 Limiting	61	2	Reserved
60	1	Compliant to FC-PI-4 Appendix H	61	1	Reserved
60	0	Compliant to SFF-8431 Appendix E	61	0	Reserved

8.2 CC_BASE [Address A0h, Byte 63]

The check code is a one-byte code that can be used to verify that the first 64 bytes of 2-wire interface information in the SFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 0 to byte 62, inclusive.

8.3 Option Values [Address A0h, Bytes 64-65]

The bits in the option field shall specify the options implemented in the transceiver.

Table 8-3 Option Values

A0h	Bit	Description
64	7	Reserved
	6	High Power Level Declaration (see SFF-8431 Addendum) Value of zero identifies standard Power Levels 1 ,2 and 3 as indicated by bits 1 and 5. Value of one identifies Power Level 4 requirement. Maximum power is declared in A2h, byte 66.
	5	High Power Level Declaration (see SFF-8431 Addendum) Value of zero identifies standard Power Levels 1 and 2 as indicated by bit 1. Value of one identifies Power Level 3 or Power Level 4 requirement.
	4	Paging implemented indicator. A value of 1 indicates that paging is implemented and byte 127d of device address A2h is used for page selection.
	3	Retimer or CDR indicator. A value of 1 indicates that the transceiver has an internal retimer or clock and data recovery (CDR) circuit.
	2	Cooled Transceiver Dedaration (see SFF-8431). Value of zero identifies a conventional uncooled (or unspecified) laser implementation. Value of one identifies a cooled laser transmitter implementation.
	1	Power Level Declaration (see SFF-8431). Value of zero identifies Power Level 1 (or unspecified) requirements. Value of one identifies Power Level 2 requirement. See Table 8-7 and Table 10-1 for control, status, timing. See Bit 5 for Power Level 3 declaration. See Bit 6 for Power Level 4 declaration.
	0	Linear Receiver Output Implemented (see SFF-8431). Value of zero identifies a conventional limiting, PAM4 or unspecified receiver output. Value of one identifies a linear receiver output.
65	7	Receiver decision threshold implemented. A value of 1 indicates that RDT is implemented.
	6	Tunable transmitter technology. A value of 1 indicates that the transmitter wavelength/frequency is tunable in accordance with SFF-8690.
	5	RATE_SELECT functionality is implemented NOTE: Lack of implementation does not indicate lack of simultaneous compliance with multiple standard rates. Compliance with particular standards should be determined from Transceiver Code Section (Table 5-3). Refer to Table 5-6 for Rate_Select functionality type identifiers.
	4	TX_DISABLE is implemented and disables the high speed serial output.
	3	TX_FAULT signal implemented. (See SFF-8419)
	2	Loss of Signal implemented, signal inverted from standard definition in SFP MSA (often called "Signal Detect"). NOTE: This is not standard SFP/GBIC behavior and should be avoided, since non-interoperable behavior results.
	1	Loss of Signal implemented, behavior as defined in SFF-8419 (often called "Rx_LOS").
	0	Reserved

8.4 Signaling Rate, max [Address A0h, Byte 66]

If address 12 is not set to FFh, the upper signaling rate limit at which the transceiver still meets its specifications (Signaling Rate, max) is specified in units of 1% above the nominal signaling rate. If address 12 is set to FFh, the nominal signaling rate (Signaling Rate, nominal) is given in this field in units of 250 MBd, rounded off to the nearest 250 MBd. A value of 00h indicates that this field is not used

8.5 Signaling Rate, min [Address A0h, Byte 67]

If address 12 is not set to FFh, the lower signaling rate limit at which the transceiver still meets its specifications (Signaling Rate, min) is specified in units of 1% below the nominal bit rate. If address 12 is set to FFh, the limit range of signaling rates specified in units of +/- 1% around the nominal signaling rate. A value of zero indicates that this field is not used.

8.6 Vendor SN [Address A0h, Bytes 68-83]

The vendor serial number (vendor SN) is a 16 byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the Vendor's serial number for the transceiver. A value of all zero in the 16-byte field indicates that the vendor SN is unspecified.

8.7 Date Code [Address A0h, Bytes 84-91]

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory.

Table 8-4 Date Code

A0h	Description
84-85	ASCII code, two low order digits of year. (00 = 2000).
86-87	ASCII code, digits of month (01 = Jan through 12 = Dec)
88-89	ASCII code, day of month (01-31)
90-91	ASCII code, vendor specific lot code, may be blank

8.8 Diagnostic Monitoring Type [Address A0h, Byte 92]

"Diagnostic Monitoring Type" is a one-byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the particular transceiver.

Note that if bit 6, address 92 is set indicating that digital diagnostic monitoring has been implemented, received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring must all be implemented. Additionally, alarm and warning thresholds must be written as specified in this document at locations 00 to 55 on 2-wire serial address 1010001X (A2h) (see Table 8-5).

Two calibration options are possible if bit 6 has been set indicating that digital diagnostic monitoring has been implemented. If bit 5, "Internally calibrated", is set, the transceiver directly reports calibrated values in units of current, power etc. If bit 4, "Externally calibrated", is set, the reported values are A/D counts which must be converted to real world units using calibration values read using 2-wire serial address 1010001X (A2h) from bytes 56 to 95. See "Diagnostics" section for details.

Bit 3 indicates whether the received power measurement represents average input optical power or OMA. If the bit is set, average power is monitored. If it is not, OMA is monitored.

8.9 Addressing Modes

Bit 2 indicates whether or not it is necessary for the host to perform an address change sequence before accessing information at 2-wire serial address A2h. If this bit is not set, the host may simply read from either address, A0h or A2h, by using that value in the address byte during the 2-wire communication sequence. If the bit is set, the following sequence must be executed prior to accessing information at address A2h. Once A2h has been accessed, it will be necessary to execute the address change sequence again prior to reading from A0h. The address change sequence is defined as the following steps on the 2-wire serial interface:

1) Host controller generates a Start condition, followed by address of 0b00000000.
   Note that the R/W bit of this address indicates transfer from host to device (`0'b).
2) Device responds with Ack
3) Host controller transfers 0b00000100 (04h) as the next 8 bits of data
   This value indicates that the device is to change its address
4) Device responds with Ack
5) Host controller transfers one of the following values as the next 8 bits of data:
   0bXXXXXX00 - specifies 2-wire interface ID memory page
   0bXXXXXX10 - specifies Digital Diagnostic memory page
6) Device responds with Ack
7) Host controller generates a Stop condition
8) Device changes address that it responds to, based on the Step 5 byte value above:
   0bXXXXXX00 - address becomes 0b1010000X (A0h)
   0bXXXXXX10 - address becomes 0b1010001X (A2h)

Table 8-5 Diagnostic Monitoring Type

A0h	Bit	Description
92	7	Reserved for legacy diagnostic implementations. Must be '0' for compliance with this document.
	6	Digital diagnostic monitoring implemented (described in this document).
	5	Internally calibrated
	4	Externally calibrated
	3	Received power measurement type 0 = OMA, 1 = average power
	2	Address change required see section above, "addressing modes"
	1-0	Reserved

8.10 Enhanced Options [Address A0h, Byte 93]

The Enhanced Options are a one-byte field with 8 single bit indicators which describe the optional digital diagnostic features implemented in the transceiver. Since transceivers do not necessarily implement all optional features described in this document, this field allows the host to determine which functions are available over the 2-wire serial bus. A '1' indicates that the particular function is implemented in the transceiver. Bits 3 and 6 of byte 110 (see Table 9-16) allow the host to control the Rate_Select and TX_Disable functions. If these functions are not implemented, the bits remain readable and writable, but the transceiver ignores them.

Note that "soft" functions of TX_DISABLE, TX_FAULT, RX_LOS, and RATE_SELECT do not meet timing requirements as specified in the SFP MSA section B3 "Timing Requirements of Control and Status I/O" and the GBIC Specification, revision 5.5, (SFF-8053), section 5.3.1, for their corresponding pins. The soft functions allow a host to poll or set these values over the 2-wire interface bus as an alternative to monitoring/setting pin values. Timing is vendor specific but must meet the requirements specified in Table 8-7. Asserting either the "hard pin" or "soft bit" (or both) for TX_DISABLE or RATE_SELECT results in that function being asserted.

Table 8-6 Enhanced Options

A0h	Bit	Description
93	7	Optional Alarm/warning flags implemented for all monitored quantities (see Table 9-17)
	6	Optional soft TX_DISABLE control and monitoring implemented
	5	Optional soft TX_FAULT monitoring implemented
	4	Optional soft RX_LOS monitoring implemented
	3	Optional soft RATE_SELECT control and monitoring implemented
	2	Optional Application Select control implemented per SFF-8079
	1	Optional soft Rate Select control implemented per SFF-8431
	0	Reserved

Table 8-7 I/O Timing for Soft Control and Status Functions

Parameter	Symbol	Min	Max	Unit	Conditions
TX_DISABLE assert time	t_off		100	ms	Time from TX_DISABLE bit set [1] until optical output falls below 10% of nominal
TX_DISABLE deassert time	t_on		100	ms	Time from TX_DISABLE bit cleared [1] until optical output rises above 90% of nominal
Time to initialize, including reset of TX_FAULT	t_init		300	ms	Time from power on or negation of TX_FAULT using TX_DISABLE until transmitter output is stable [2]
TX_FAULT assert time	t_fault		100	ms	Time from fault to TX_FAULT bit set.
RX_LOS assert time	t_loss_on		100	ms	Time from LOS state to RX_LOS bit set
RX_LOS deassert time	t_loss_off		100	ms	Time from non-LOS state to RX_LOS bit cleared
Rate select change time [3]	t_rate_select		100	ms	Time from change of state of Rate Select bit [1] until module is in conformance with the appropriate specification for the new rate
2-wire interface Clock rate	f_serial_clock		100	kHz	n/a
2-wire interface Diagnostic data ready time	t_data		1000	ms	From power on to data ready, bit 0 of byte 110 set
2-wire interface bus hardware ready time	t_serial		300	ms	Time from power on until module is ready for data transmission over the 2-wire bus.
Optional. High Power Level assert time (per SFF-8431)	t_hpower_level		300	ms	Time from High Power Level enable bit set until module operation is stable. See Table 10-1 for control bit.

NOTES:
1. Measured from falling clock edge after stop bit of write transaction.
2. See SFF-8053 GBIC (Gigabit Interface Converter)3. The T11.2 committee, as part of its FC-PI-2 standardization effort, has advised that a 1 ms maximum is required to be compatible with auto-negotiation algorithms documented in the FC-FS specification. For 64GFC this time is required to be 4 ms maximum.

8.11 SFF-8472 Compliance [Address A0h, Byte 94]

Byte 94 contains an unsigned integer that indicates which feature set(s) are implemented in the transceiver.

Table 8-8 SFF-8472 Compliance

A0h	Value	Interpretation
94	01h	Includes functionality described in Rev 9.3 of SFF-8472.
	02h	Includes functionality described in Rev 9.5 of SFF-8472.
	03h	Includes functionality described in Rev 10.2 of SFF-8472.
	04h	Includes functionality described in Rev 10.4 of SFF-8472.
	05h	Includes functionality described in Rev 11.0 of SFF-8472.
	06h	Includes functionality described in Rev 11.3 of SFF-8472.
	07h	Includes functionality described in Rev 11.4 of SFF-8472.
	08h	Includes functionality described in Rev 12.3 of SFF-8472.
	09h	Includes functionality described in Rev 12.4 of SFF-8472.
	0A - FFh	Reserved

8.12 CC_EXT [Address A0h, Byte 95]

The check code is a one-byte code that can be used to verify that the first 32 bytes of extended 2-wire interface information in the SFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 64 to byte 94, inclusive.

9. Diagnostics

9.1 Overview [Address A2h]

2-wire serial bus address 1010001X (A2h) is used to access measurements of transceiver temperature, internally measured supply voltage, TX bias current, TX output power, received optical power, and two optional DWDM quantities: laser temperature, and TEC current.

The values are interpreted differently depending upon the option bits set at address 92. If bit 5 "internally calibrated" is set, the values are calibrated absolute measurements, which should be interpreted according to the section "Internal Calibration" below. If bit 4 "externally calibrated" is set, the values are A/D counts, which are converted into real units per the subsequent section titled "External Calibration". The optional DWDM quantities are defined for internal calibration only.

Measured parameters are reported in 16-bit data fields, i.e., two concatenated bytes. The 16-bit data fields allow for wide dynamic range. This is not intended to imply that a 16-bit A/D system is recommended or required in order to achieve the accuracy goals stated below. The width of the data field should not be taken to imply a given level of precision. It is conceivable that the accuracy goals herein can be achieved by a system having less than 16 bits of resolution. It is recommended that any low-order data bits beyond the system's specified accuracy be fixed at zero. Overall system accuracy and precision is vendor dependent.

To guarantee coherency of the diagnostic monitoring data, the host is required to retrieve any multi-byte fields from the diagnostic monitoring data structure (e.g. Rx Power MSB - byte 104 in A2h, Rx Power LSB - byte 105 in A2h) by the use of a single two-byte read sequence across the 2-wire interface.

The transceiver is required to ensure that any multi-byte fields which are updated with diagnostic monitoring data (e.g. Rx Power MSB - byte 104 in A2h, Rx Power LSB - byte 105 in A2h) must have this update done in a fashion that guarantees coherency and consistency of the data. In other words, the update of a multi-byte field by the transceiver must not occur such that a partially updated multi-byte field can be transferred to the host. Also, the transceiver shall not update a multi-byte field within the structure during the transfer of that multi-byte field to the host, such that partially updated data would be transferred to the host.

Accuracy requirements specified below shall apply to the operating signal range specified in the relevant standard. The manufacturer's specification should be consulted for more detail on the conditions under which the accuracy requirements are met.

9.2 Internal Calibration

Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data.

1) Internally measured transceiver temperature. Represented as a 16-bit signed twos complement value in increments of 1/256 degrees Celsius, yielding a total range of -128°C to +128°C. Temperature accuracy is vendor specific but must be better than ±3 degrees over the specified operating temperature and voltage. Please see vendor specification for details on location of temperature sensor. See Table 9-1 and Table 9-2 below for examples of temperature format.
2) Internally measured transceiver supply voltage. Represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0-65535) with LSB equal to 100 uV, yielding a total range of 0 V to +6.55 V. Practical considerations to be defined by transceiver manufacturer tend to limit the actual bounds of the supply voltage measurement. Accuracy is vendor specific but must be better than ±3% of the manufacturer's nominal value over specified operating temperature and voltage. Note that in some transceivers, transmitter supply voltage and receiver supply voltage are isolated. In that case, only one supply is monitored. Refer to the device specification for more detail.
3) Measured TX bias current in uA. Represented as a 16-bit unsigned integer with the current defined as the full 16-bit value (0-65535) with LSB equal to 2 uA, yielding a total range of 0 to 131 mA. Accuracy is vendor specific but must be better than ±10% of the manufacturer's nominal value over specified operating temperature and voltage.
4) Measured TX output power in mW. Represented as a 16-bit unsigned integer with the power defined as the full 16-bit value (0-65535) with LSB equal to 0.1 uW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Data is assumed to be based on measurement of laser monitor photodiode current. It is factory calibrated to absolute units using the most representative fiber output type. Accuracy is vendor specific but must be better than ±3 dB over the specified temperature and voltage. Data is not valid when the transmitter is disabled.
5) Measured RX received optical power in mW. Value can represent either average received power or OMA depending upon how bit 3 of byte 92 (A0h) is set. Represented as a 16-bit unsigned integer with the power defined as the full 16-bit value (0-65535) with LSB equal to 0.1 uW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than ±3 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.
6) Measured optional laser temperature. For DWDM applications bytes 106-107 report laser temperature. The encoding is the same as for transceiver internal temperature defined in paragraph 1) above. The relative and absolute accuracy are vendor specific but relative laser temperature accuracy must be better than +/- 0.2 degrees Celsius. [Relative temperature accuracy refers to the accuracy of the reported temperature changes relative to the actual laser temperature changes].
7) Measured TEC current. For DWDM applications, bytes 108-109 report the measured TEC current. The format is signed two's complement with the LSB equal to 0.1 mA. Thus a range from -3276.8 to +3276.7 mA may be reported with a resolution of 0.1 mA. See Table 9-4 and Table 9-5 for further details. Reported TEC current is a positive number for cooling and a negative number for heating. The accuracy of the TEC current monitor is vendor specific but shall be better than +/- 15% of the maximum TEC current as stored in the TEC current high alarm threshold (bytes 48-49).

The tables below illustrate the 16-bit signed twos complement format used for temperature reporting. The most significant bit (D7) represents the sign, which is zero for positive temperatures and one for negative temperatures.

Table 9-1 Bit Weights (Degrees C) for Temperature Reporting Registers

Most Significant Byte (byte 96)								Least Significant Byte (byte 97)							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Sign	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

Table 9-2 Digital Temperature Format

Temperature		**Binary**		**Hexadecimal**	
Decimal	Fraction	High Byte	Low Byte	High Byte	Low Byte
+127.996	+127 255/256	01111111	11111111	7F	FF
+125.000	+125	01111101	00000000	7D	00
+25.000	+25	00011001	00000000	19	00
+1.004	+1 1/256	00000001	00000001	01	01
+1.000	+1	00000001	00000000	01	00
+0.996	+255/256	00000000	11111111	00	FF
+0.004	+1/256	00000000	00000001	00	01
0.000	0	00000000	00000000	00	00
-0.004	-1/256	11111111	11111111	FF	FF
-1.000	-1	11111111	00000000	FF	00
-25.000	-25	11100111	00000000	E7	00
-40.000	-40	11011000	00000000	D8	00
-127.996	-127 255/256	10000000	00000001	80	01

The tables below illustrate the 16-bit twos complement format used for TEC current reporting. The most significant bit (D7) represents the sign, which is zero for positive currents (cooling) and one for negative currents (heating).

Table 9-3 Bit Weights (mA) for TEC current Reporting Registers

Most Significant Byte (byte 108)								Least Significant Byte (byte 109)							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Sign	1638.4	819.2	409.6	204.8	102.4	51.2	25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1

Table 9-4 TEC Current Format

Current	Binary		Hexadecimal	
Decimal	High Byte	Low Byte	High Byte	Low Byte
+3276.7	01111111	11111111	7F	FF
+3200.0	01111101	00000000	7D	00
+640.0	00011001	00000000	19	00
+25.7	00000001	00000001	01	01
+25.6	00000001	00000000	01	00
+25.5	00000000	11111111	00	FF
+0.1	00000000	00000001	00	01
0.0	00000000	00000000	00	00
-0.1	11111111	11111111	FF	FF
-25.6	11111111	00000000	FF	00
-640.0	11100111	00000000	E7	00
-1024.0	11011000	00000000	D8	00
-3276.7	10000000	00000001	80	01
-3276.8	10000000	00000000	80	00

9.3 External Calibration

Measurements are raw A/D values and must be converted to real world units using calibration constants stored in EEPROM locations 56-95 at 2-wire serial bus address A2h. Calibration is valid over vendor specified operating temperature and voltage. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data.

After calibration per the equations given below for each variable, the results are consistent with the accuracy and resolution goals for internally calibrated devices.

1) Internally measured transceiver temperature. Module temperature, T, is given by the following equation:

   T(C) = T_slope * T_AD (16 bit signed twos complement value) + T_offset

   The result is in units of 1/256°C, yielding a total range of -128°C to +128°C. See Table 9-6 for locations of T_slope and T_offset. Temperature accuracy is vendor specific but must be better than +/-3 degrees Celsius over specified operating temperature and voltage. Please see vendor specification sheet for details on location of temperature sensor. Table 9-1 and Table 9-2 give examples of the 16-bit signed twos complement temperature format.
2) Internally measured supply voltage. Module internal supply voltage, V, is given in microvolts by the following equation:

   V(uV) = V_slope * V_AD (16-bit unsigned integer) + V_offset

   The result is in units of 100 uV, yielding a total range of 0 to 6.55 V. See Table 9-6 for locations of V_slope and V_offset. Accuracy is vendor specific but must be better than +/-3% of the manufacturer's nominal value over specified operating temperature and voltage. Note that in some transceivers, transmitter supply voltage and receiver supply voltage are isolated. In that case, only one supply is monitored. Refer to the manufacturer's specification for more detail.
3) Measured transmitter laser bias current. Module laser bias current, I, is given in microamps by the following equation:

   I (uA) = I_slope * I_AD (16 bit unsigned integer) + I_offset

   This result is in units of 2 uA, yielding a total range of 0 to 131 mA. See Table 9-6 for locations of I_slope and I_offset. Accuracy is vendor specific but must be better than +/-10% of the manufacturer's nominal value over specified operating temperature and voltage.
4) Measured coupled TX output power. Module transmitter coupled output power, TX_PWR, is given in uW by the following equation:

   TX_PWR (uW) = TX_PWR_slope * TX_PWR_AD (16-bit unsigned integer) + TX_PWR_offset.

   This result is in units of 0.1uW yielding a total range of 0 to 6.5 mW. See Table 9-6 for locations of TX_PWR_slope and TX_PWR_offset. Accuracy is vendor specific but must be better than +/-3 dB over specified operating temperature and voltage. Data is assumed to be based on measurement of a laser monitor photodiode current. It is factory calibrated to absolute units using the most representative fiber output type. Data is not valid when the transmitter is disabled.

5) Measured received optical power. Received power, RX_PWR, is given in uW by the following equation:

Rx_PWR (uW) = Rx_PWR(4) * Rx_PWR_ADe4 (16 bit unsigned integer) +
Rx_PWR(3) * Rx_PWR_ADe3 (16 bit unsigned integer) +
Rx_PWR(2) * Rx_PWR_ADe2 (16 bit unsigned integer) +
Rx_PWR(1) * Rx_PWR_AD (16 bit unsigned integer) +
Rx_PWR(0)

The result is in units of 0.1 uW yielding a total range of 0 to 6.5 mW. See Table 9-6 for locations of Rx_PWR(4-0). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than +/-3 dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.

9.4 Alarm and Warning Thresholds [Address A2h, Bytes 0-39]

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory preset values allow the user to determine when a particular value is outside of "normal" limits as determined by the transceiver manufacturer. It is assumed that these values vary with different technologies and different implementations. When external calibration is used, data may be compared to alarm and warning threshold values before or after calibration by the host. Comparison can be done directly before calibration. If comparison is to be done after calibration, calibration must first be applied to both data and threshold values.

The values reported in the alarm and warning thresholds area (see below) may be temperature compensated or otherwise adjusted when setting warning and/or alarm flags. Any threshold compensation or adjustment is vendor specific and optional. See Vendor's data sheet for use of alarm and warning thresholds.

Table 9-5 Alarm and Warning Thresholds

A2h	# Bytes	Name	Description
00-01	2	Temp High Alarm	MSB at low address
02-03	2	Temp Low Alarm	MSB at low address
04-05	2	Temp High Warning	MSB at low address
06-07	2	Temp Low Warning	MSB at low address
08-09	2	Voltage High Alarm	MSB at low address
10-11	2	Voltage Low Alarm	MSB at low address
12-13	2	Voltage High Warning	MSB at low address
14-15	2	Voltage Low Warning	MSB at low address
16-17	2	Bias High Alarm	MSB at low address
18-19	2	Bias Low Alarm	MSB at low address
20-21	2	Bias High Warning	MSB at low address
22-23	2	Bias Low Warning	MSB at low address
24-25	2	TX Power High Alarm	MSB at low address
26-27	2	TX Power Low Alarm	MSB at low address
28-29	2	TX Power High Warning	MSB at low address
30-31	2	TX Power Low Warning	MSB at low address
32-33	2	RX Power High Alarm	MSB at low address
34-35	2	RX Power Low Alarm	MSB at low address
36-37	2	RX Power High Warning	MSB at low address
38-39	2	RX Power Low Warning	MSB at low address

A2h	# Bytes	Name	Description
40-41	2	Optional Laser Temp High Alarm	MSB at low address
42-43	2	Optional Laser Temp Low Alarm	MSB at low address
44-45	2	Optional Laser Temp High Warning	MSB at low address
46-47	2	Optional Laser Temp Low Warning	MSB at low address
48-49	2	Optional TEC Current High Alarm	MSB at low address
50-51	2	Optional TEC Current Low Alarm	MSB at low address
52-53	2	Optional TEC Current High Warning	MSB at low address
54-55	2	Optional TEC Current Low Warning	MSB at low address

9.5 Calibration Constants for External Calibration Option [Address A2h, Bytes 56-91]

When External Calibration bit 4, byte 92 in A0h is set to 1, Bytes 56-94 are allocated to external calibration values as listed in Table 9-6.

Table 9-6 Calibration Constants for External Calibration Option

A2h	# Bytes	Name	Description
56-59	4	Rx_PWR(4)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 56 is MSB. Bit 0 of byte 59 is LSB. Rx_PWR(4) should be set to zero for "internally calibrated" devices.
60-63	4	Rx_PWR(3)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 60 is MSB. Bit 0 of byte 63 is LSB. Rx_PWR(3) should be set to zero for "internally calibrated" devices.
64-67	4	Rx_PWR(2)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 64 is MSB, bit 0 of byte 67 is LSB. Rx_PWR(2) should be set to zero for "internally calibrated" devices.
68-71	4	Rx_PWR(1)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 68 is MSB, bit 0 of byte 71 is LSB. Rx_PWR(1) should be set to 1 for "internally calibrated" devices.
72-75	4	Rx_PWR(0)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 72 is MSB, bit 0 of byte 75 is LSB. Rx_PWR(0) should be set to zero for "internally calibrated" devices.
76-77	2	Tx_I(Slope)	Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB. Tx_I(Slope) should be set to 1 for "internally calibrated" devices.
78-79	2	Tx_I(Offset)	Fixed decimal (signed two's complement) calibration data, laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB. Tx_I(Offset) should be set to zero for "internally calibrated" devices.
80-81	2	Tx_PWR(Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte 81 is LSB. Tx_PWR(Slope) should be set to 1 for "internally calibrated" devices.
82-83	2	Tx_PWR(Offset)	Fixed decimal (signed two's complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB. Tx_PWR(Offset) should be set to zero for "internally calibrated" devices.
84-85	2	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB. T(Slope) should be set to 1 for "internally calibrated" devices.
86-87	2	T (Offset)	Fixed decimal (signed two's complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB. T(Offset) should be set to zero for "internally calibrated" devices.
88-89	2	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage. Bit 7 of byte 88 is MSB, bit 0 of byte 89 is LSB. V(Slope) should be set to 1 for "internally calibrated" devices.
90-91	2	V (Offset)	Fixed decimal (signed two's complement) calibration data, internal module supply voltage. Bit 7 of byte 90 is MSB. Bit 0 of byte 91 is LSB. V(Offset) should be set to zero for "internally calibrated" devices.
92-94	3	Reserved	
95	1	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0-94.

The slope constants at addresses 76, 80,84, and 88, are unsigned fixed-point binary numbers. The slope will therefore always be positive. The binary point is in between the upper and lower bytes, i.e., between the eighth and ninth most significant bits. The most significant byte is the integer portion in the range 0 to +255. The least significant byte represents the fractional portion in the range of 0.00391 (1/256) to 0.9961 (255/256). The smallest real number that can be represented by this format is 0.00391 (1/256); the largest real number that can be represented using this format is 255.9961 (255 + 255/256). Slopes are defined, and conversion formulas found, in the "External Calibration" section. Examples of this format are illustrated below:

Table 9-7 Unsigned Fixed-Point Binary Format for Slopes

Decimal Value	Binary Value		Hexadecimal Value	
	MSB	LSB	High Byte	Low Byte
0.0000	00000000	00000000	00	00
0.0039	00000000	00000001	00	01
1.0000	00000001	00000000	01	00
1.0313	00000001	00001000	01	08
1.9961	00000001	11111111	01	FF
2.0000	00000010	00000000	02	00
255.9921	11111111	11111110	FF	FE
255.9961	11111111	11111111	FF	FF

The calibration offsets are 16-bit signed twos complement binary numbers. The offsets are defined by the formulas in the "External Calibration" section. The least significant bit represents the same units as described above under "Internal Calibration" for the corresponding analog parameter, e.g., 2 μA for bias current, 0.1 μW for optical power, etc. The range of possible integer values is from +32767 to -32768. Examples of this format are shown below.

Table 9-8 Format for Offsets

Decimal Value	Binary Value		Hexadecimal Value	
	MSB	LSB	High Byte	Low Byte
+32767	01111111	1111111	7F	FF
+3	00000000	00000011	00	03
+2	00000000	00000010	00	02
+1	00000000	00000001	00	01
0	00000000	00000000	00	00
-1	11111111	11111111	FF	FF
-2	11111111	11111110	FF	FE
-3	11111111	11111101	FF	FD
-32768	10000000	00000000	80	00

External calibration of received optical power makes use of single-precision floating-point numbers as defined by *IEEE Standard for Floating-Point Arithmetic*, IEEE Std 754. Briefly, this format utilizes four bytes (32 bits) to represent real numbers. The first and most significant bit is the sign bit; the next eight bits indicate an exponent (base 2) in the range of +126 to -127; the remaining 23 bits represent the mantissa. The 32 bits are therefore arranged as in the following table.

Table 9-9 IEEE-754 Single-Precision Floating Point Number Format

Function	Sign	Exponent								Mantissa																			
Bit	31	30							23	22																			0
Byte	3								2								1								0				
← Most Significant																												Least Significant →	

Rx_PWR(4), as an example, is stored as shown in Table 9-10:

Table 9-10 Example of Floating Point Representation

Byte Address	Contents	Significance
56	SEEEEEEE	Most
57	EMMMMMMM	Second Most
58	MMMMMMMM	Second Least
59	MMMMMMMM	Least
where S = sign bit; E = exponent bit; M = mantissa bit.		

Special cases of the various bit values are reserved to represent indeterminate values such as positive and negative infinity; zero; and "NaN" or not a number. NaN indicates an invalid result. As of this writing, explanations of the IEEE single precision floating point format were posted on the worldwide web at https://en.wikipedia.org/wiki/Single-precision_floating-point_format . The actual IEEE standard is available at www.IEEE.org .

9.6 Additional Enhanced Features

When External Calibration bit 4, byte 92 in A0h is set to 0, Bytes 56-94 are allocated to Additional Enhanced Features as listed in Table 9-11.

Table 9-11 Additional Enhanced Features

A2h	# Bytes	Name	Description
Capabilities			
56-57	2	Enhanced Controls Advertisements	Advertisement for Enhanced Controls Implementation (see Table 9-12)
58-59	2	Enhanced Status Advertisements	Advertisement for Enhanced Status Implementation (see Table 9-13)
60-65	6	Enhanced Signal Integrity Controls Advertisement	Advertisement for Signal Integrity Control Implementation (see Table 9-14)
66	1	Max Power Consumption	See A0, byte 64, bit 6 Max power consumption of the module, unsigned integer with LSB = 0.1 W
67	1	Secondary Extended Spec compliance	Secondary Extended Specification compliance code. See SFF-8024 Table 4-4
68	2	Reserved	Reserved for Future Advertisements
Status			
69-70	2	Reserved	Reserved for Future Status
Control			
71-74	4	Enhanced Control	Enhanced Control Registers (see Table 9-15)
75-94	20	Reserved	Reserved
95	1	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0-94

Table 9-12 Enhanced Control Advertisement

A2h	Bit	Name	Description
56	7-5	Reserved	Reserved
	4	RS0/1 pin status ignore	0b - RS0, RS1 pins status ignore bit not implemented 1b - RS0, RS1 pins status ignore bit implemented (see A2h, byte 72, bit4)
	3-2	Tx Squelch Implemented	00b - Tx Squelch not implemented 01b - Tx Squelch reduces OMA 10b - Tx Squelch reduces Pave 11b - User Control, both OMA and Pave supported
	1	Tx Force Squelch Implemented	0b - Tx Force Squelch not implemented 1b - Tx Force Squelch implemented
	0	Tx Squelch Disable Implemented	0b - Tx Squelch disable not implemented 1b - Tx Squelch disable implemented
57	7-2	Reserved	Reserved
	1	Rx Force Squelch Implemented	0b - Rx Force Squelch not implemented 1b - Rx Force Squelch implemented
	0	Rx Squelch disable Implemented	0b - Rx Squelch disable not implemented 1b - Rx Squelch disable implemented

Table 9-13 Enhanced Flags Advertisement

A2h	Bit	Name	Description
58	7-1	Reserved	Reserved
	0	Tx Adaptive Input EQ Fail Flag Implemented	0b – Tx Adaptive Input EQ Fail Flag not implemented 1b - Tx Adaptive Input EQ Fail Flag implemented
59	7-0	Reserved	Reserved

Table 9-14 Enhanced Signal Integrity Control Advertisement

A2h	Bit	Name	Description
60	7-5	Reserved	Reserved
	4-3	Tx Input EQ Store/Recall	00b - Tx Input EQ Store/Recall not implemented 01b - Tx Input EQ Store/Recall implemented 10b - Reserved 11b - Reserved
	2	Tx Input EQ Freeze Implemented	0b - Tx Input EQ Freeze not implemented 1b - Tx Input EQ Freeze implemented
	1	Adaptive Tx Input EQ Implemented	0b - Adaptive Tx Input EQ not implemented 1b - Adaptive Tx Input EQ implemented
	0	Tx Input EQ Manual Control Implemented	0b - Tx Input EQ manual control not implemented 1b - Tx Input EQ manual control implemented
61	7-0	Max Adaptive Tx Input EQ settling time	Maximum Time needed for adaptive algorithm to converge to appropriate setting, LSB = 100 ms
62	7-5	Reserved	Reserved
	4-3	Rx Output EQ Type	00b - Not Implemented, Constant Rx Amplitude p-p or no information 01b - Constant steady state amplitude 10b - Constant average of Rx Amplitude p-p and steady state amplitude 11b - Reserved
	2-1	Rx Enhanced Output EQ Control Implemented	00b - Rx Enhanced Output EQ control not implemented 01b - Rx Enhanced Output EQ pre-cursor control implemented 10b - Rx Enhanced Output EQ post-cursor control implemented 11b - Rx Enhanced Output EQ pre-cursor and post-cursor control implemented
	0	Rx Output Amplitude Control Implemented	0b - Rx Output Amplitude control not implemented 1b - Rx Output Amplitude control implemented
63	7	Rx Output Amplitude code 0011b Implemented	0b - Rx Out Amplitude code 0011b not implemented 1b - Rx Out Amplitude code 0011b implemented
	6	Rx Output Amplitude code 0010b Implemented	0b - Rx Out Amplitude code 0010b not implemented 1b - Rx Out Amplitude code 0010b implemented
	5	Rx Output Amplitude code 0001b Implemented	0b - Rx Out Amplitude code 0001b not implemented 1b - Rx Out Amplitude code 0001b implemented
	4	Rx Output Amplitude code 0000b Implemented	0b - Rx Out Amplitude code 0000b not implemented 1b - Rx Out Amplitude code 0000b implemented
	3-0	Max Tx Input EQ	Maximum supported value of the Tx Input EQ control for manual/fixed programming
64	7-4	Max Rx Output EQ Post-cursor	Maximum supported value of the Rx Output EQ Post-cursor control
	3-0	Max Rx Output EQ Pre-cursor	Maximum supported value of the Rx Output EQ Pre-cursor control
65	7-0	Reserved	Reserved

Table 9-15 Enhanced Control

A2h	Bit	Name	Description
71	7-4	Reserved	Reserved
	3	Tx Input EQ Adaptation Recall	0b - Do not recall 1b - Recall
	2	Tx Input EQ Adaptation Store	0b - Do not store 1b - Store
	1	Tx Input EQ Adaptation Freeze	0b - Adaptive Tx Input EQ no freeze 1b - Adaptive Tx Input EQ freeze
	0	Tx Input EQ Adaptation Enable	0b - Adaptive Tx Input EQ disable (use manual fixed EQ) 1b - Adaptive Tx Input EQ enable
72	7-5	RX Output EQ Control, pre-cursor	Rx Output EQ pre-cursor
	4	Rx Output Enhanced EQ Control Override	0b – When this bit is set to 0b, the host will use Rx Emphasis control register 115, A2h. See Table 9-17 and Table 9-19. 1b - When this bit is set to 1b, the host will use Rx Enhanced Output EQ control, register 72, A2h, as advertised by the module in register 62, A2h, bits 2-1. Default is 0b .
	3-0	RX Output EQ Control, post-cursor	Rx Output EQ post-cursor
73	7-5	Reserved	Reserved
	4	RS0/RS1 Pin State Ignore	0b - Do not ignore 1b - When this bit is set to 1b the state of the RS0 and RS1 hardware pins and A2h, byte 110, bits 4 and 5 are ignored by the module, rate is determined only by A2h, byte 110, bit 3 and byte 118, bit 3 [1]
	3-0	Output Amplitude Control	Rx Output Amplitude
74	7-6	Reserved	Reserved
	5	Rx Force Squelch	0b - No impact on Rx behavior 1b - Rx Output Squelch
	4	Rx Squelch disable	0b - Rx output squelch permitted 1b - Rx output squelch not permitted
	3	Reserved	Reserved
	2	Tx Squelch control [2]	0b -Tx Squelch reduces OMA 1b - Tx Squelch reduces Pave
	1	Tx Force Squelch	0b - No impact on Tx behavior 1b - Tx Output Squelch
	0	Tx Squelch Disable	0b – Tx output squelch permitted 1b – Tx output squelch not permitted

NOTE:
1. To support legacy modules that do not have the RS0/RS1 Pin State Ignore bit, the host needs to set the hardware rate select pins to a correct state.
2. If both options are supported, as advertised in bits 3-2, register 56, it is recommended that the host sets the squelch method based on knowledge of the relevant interface standard.

9.7 CC_DMI [Address A2h, Byte 95]

This check sum is a one-byte code that can be used to verify that the first 94 bytes of page A2h in the SFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes of page A2h from byte 0 to byte 94, inclusive.

9.8 Real Time Diagnostic and Control Registers [Address A2h, Bytes 96-111]

Table 9-16 A/D Values and Status Bits

A2h	Bit	Name	Description
Converted analog values. Calibrated 16-bit data.			
96	All	Temperature MSB	Internally measured module temperature.
97	All	Temperature LSB	
98	All	Vcc MSB	Internally measured supply voltage in transceiver.
99	All	Vcc LSB	
100	All	TX Bias MSB	Internally measured TX Bias Current.
101	All	TX Bias LSB	
102	All	TX Power MSB	Measured TX output power.
103	All	TX Power LSB	
104	All	RX Power MSB	Measured RX input power.
105	All	RX Power LSB	
106	All	Optional Laser Temp/Wavelength MSB	Measured laser temperature or wavelength
107	All	Optional Laser Temp/Wavelength LSB	
108	All	Optional TEC current MSB	Measured TEC current (positive is cooling)
109	All	Optional TEC current LSB	
Optional Status/Control Bits			
110	7	TX Disable State	Digital state of the TX Disable Input Pin. Updated within 100 ms of change on pin.
	6	Soft TX Disable Select	Read/write bit that allows software disable of laser. Writing '1' disables laser. See Table 8-7 for enable/disable timing requirements. This bit is "OR"d with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is zero/low.
	5	RS(1) State	Digital state of SFP input pin AS(1) per SFF-8079 or RS(1) per SFF-8431. Updated within 100 ms of change on pin. See A2h Byte 118, Bit 3 for Soft RS(1) Select control information.
	4	Rate_Select State [aka. "RS(0)"]	Digital state of the SFP Rate_Select Input Pin. Updated within 100 ms of change on pin. Note: This pin is also known as AS(0) in SFF-8079 and RS(0) in SFF-8431.
	3	Soft Rate_Select Select [aka. "RS(0)"]	Read/write bit that allows software rate select control. Writing '1' selects full bandwidth operation. This bit is "OR'd with the hard Rate_Select, AS(0) or RS(0) pin value. See Table 8-7 for timing requirements. Default at power up is 0/low, unless specifically redefined by value selected in Table 5-6. If Soft Rate Select is not implemented, the transceiver ignores the value of this bit. Note: Specific transceiver behaviors of this bit are identified in Table 5-6 and referenced documents. See Table 10-1, byte 118, bit 3 for Soft RS(1) Select.
	2	TX Fault State	Digital state of the TX Fault Output Pin. Updated within 100 ms of change on pin.
	1	Rx_LOS State	Digital state of the RX_LOS Output Pin. Updated within 100 ms of change on pin.
	0	Data_Not_Ready	Indicates free-side does not yet have valid monitor data. The bit remains high until valid data can be read at which time the bit goes low.
111	7-0	Reserved	Reserved (was assigned to SFF-8079).

The Data_Ready_Bar bit is high during module power up and prior to the first valid A/D reading. Once the first valid A/D reading occurs, the bit is set low until the device is powered down. The bit must be set low within 1 second of power up.

9.9 Alarm and Warning Flag Bits [Address A2h, Bytes 112-117]

Bytes 112 to 117 contain an optional set of alarm and warning flags. The flags may be latched or non-latched. Implementation is vendor specific, and the Vendor's specification sheet should be consulted for details. It is recommended that in either case, detection of an asserted flag bit should be verified by a second read of the flag at least 100 ms later. For users who do not wish to set their own threshold values or read the values in locations 0-55, the flags alone can be monitored. Two flag types are defined.

1. Alarm flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power as well as reserved locations for future flags. Alarm flags indicate conditions likely to be associated with an in-operational link and cause for immediate action.
2. Warning flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power as well as reserved locations for future flags. Warning flags indicate conditions outside the normally guaranteed bounds but not necessarily causes of immediate link failures. Certain warning flags may also be defined by the manufacturer as end-of-life indicators (such as for higher than expected bias currents in a constant power control loop).

Table 9-17 Alarm and Warning Flag Bits

A2h	Bit	Name	Description
Optional Alarm and Warning Flag Bits			
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
	6	Temp Low Alarm	Set when internal temperature is below low alarm level.
	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level.
	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level.
	3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
	2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
	1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
	0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
	6	RX Power Low Alarm	Set when Received Power is below low alarm level.
	5	Optional Laser Temp High Alarm	Set when laser temperature or wavelength exceeds the high alarm level.
	4	Optional Laser Temp Low Alarm	Set when laser temperature or wavelength is below the low alarm level.
	3	Optional TEC current High Alarm	Set when TEC current exceeds the high alarm level.
	2	Optional TEC current Low Alarm	Set when TEC current is below the low alarm level.
	1	Reserved Alarm	
	0	Reserved Alarm	
114	7-4	Tx input equalization control RATE=HIGH	Input equalization level control
	3-0	Tx input equalization control RATE=LOW	Input equalization level control
115	7-4	RX output emphasis control RATE=HIGH	Output emphasis level control
	3-0	RX output emphasis control RATE=LOW	Output emphasis level control
116	7	Temp High Warning	Set when internal temperature exceeds high warning level.
	6	Temp Low Warning	Set when internal temperature is below low warning level.

A2h	Bit	Name	Description
	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level.
	4	Vcc Low Warning	Set when internal supply voltage is below low warning level.
	3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
	2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
	1	TX Power High Warning	Set when TX output power exceeds high warning level.
	0	TX Power Low Warning	Set when TX output power is below low warning level.
117	7	RX Power High Warning	Set when Received Power exceeds high warning level.
	6	RX Power Low Warning	Set when Received Power is below low warning level.
	5	Optional Laser Temp High Warning	Set when laser temperature or wavelength exceeds the high warning level.
	4	Optional Laser Temp Low Warning	Set when laser temperature or wavelength is below the low warning level.
	3	Optional TEC current High Warning	Set when TEC current exceeds the high warning level.
	2	Optional TEC current Low Warning	Set when TEC current is below the low warning level.
	1	Reserved Warning	
	0	Reserved Warning	

Table 9-18 Input Equalization (Address A2h Byte 114)

Code	Transmitter Input Equalization	
	Nominal	Units
11xx	Reserved	
1011	Reserved	
1010	10	dB
1001	9	dB
1000	8	dB
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	No EQ

Table 9-19 Output Emphasis Control (Address A2h Byte 115)

Code	Receiver Output Emphasis At nominal Output Amplitude	
	Nominal	Units
1xxx	Vendor Specific	
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	1	dB
0000	0	No emphasis

10. Extended Information

10.1 Extended Module Control/Status Bytes [Address A2h, Bytes 118-119]

Addresses 118 and 119 are defined for extended module control and status functions. Depending on usage, the contents may be writable by the host. See Table 8-3 for power level declaration requirement in Byte 64, bit 1.

Table 10-1 Extended Module Control/Status Bytes

A2h	Bit	Name	Description
118	5-7	Reserved	
	4	Adaptive Input EQ Fail Flag	Tx Adaptive Input EQ fail status. 1b = Tx Adaptive Input EQ fail
	3	Soft RS(1) Select	Read/write bit that allows software Tx rate control. Writing '1' selects full speed Tx operation. This bit is "OR'd with the hard RS(1) pin value. See Table 8-7 for timing requirements. Default at power up is 0/low, unless specifically redefined by value selected in Table 5-6. If Soft RS(1) is not implemented, the transceiver ignores the value of this bit. Note: Specific transceiver behaviors of this bit are identified in Table 5-6 and referenced documents. See Table 9-16 , byte 110, bit 3 for Soft RS(0) Select.
	2	Power Level 4 Enable	Value of 1 enables Power Level 4 if listed in A0h, Byte 64.
	1	Power Level Operation State	Optional. SFF-8431 Power Level (maximum power dissipation) status. Value of zero indicates Power Level 1 operation (1.0 W max). Value of one indicates Power Level 2 or 3 operation (1.5 W or 2.0 W max), depending on the values in byte 64 of A0h. Refer to Table 8-3 for Power Level requirement declaration. Refer to Table 8-7 for timing.
	0	Power Level Select	Optional. SFF-8431 Power Level (maximum power dissipation) control bit. Value of zero enables Power Level 1 only (1.0 W max). Value of one enables Power Level 2 or 3 (1.5 W or 2.0 W max), depending on the values in byte 64 of A0h. Refer to Table 8-3 for Power Level requirement declaration. Refer to Table 8-7 for timing. If Power Levels 2 or 3 are not implemented, the SFP ignores the value of this bit.
119	7-5	Reserved	
	4	PAM4 Mode Tx Configured	This status bit indicates the module Tx logic has finished configuring itself to 64GFC mode at 28.9 GBd (if bit 2, 64GFC Mode is set) or 50G Ethernet mode at 26.5625GBd (If this rate is selected through module Rate Select).
	3	PAM4 Mode Rx Configured	This status bit indicates the module Rx logic has finished configuring itself to 64GFC mode at 28.9 GBd (if bit 2, 64GFC Mode is set) or 50G Ethernet mode at 26.5625 GBd (If this rate is selected through module Rate Select).
	2	64GFC Mode	Writing a 1 to this bit selects 64GFC speed of operation at 28.9 GBd. When this bit is set to 1, the rate select settings on the pins or in the registers shall be ignored. Default at power up for this bit is 0.
	1	Optional Tx CDR unlocked	Used when bit 64.3 (A0h) is set to 1. If the Tx side CDR is enabled, a value of 0 indicates that the CDR is locked, whereas a value of 1 indicates loss of lock of the CDR. If the CDR is in bypass mode, this bit is set to 0. In 64GFC or 50G Ethernet mode, if bit 4 of this byte is set to 1, a value of 0 indicates that the equalizer has finished adaptation and the CDR is locked to the PAM4 signal.

A2h	Bit	Name	Description
	0	Optional Rx CDR unlocked	Used when bit 64.3 (A0h) is set to 1. If the Rx side CDR is enabled, a value of 0 indicates that the CDR is locked, whereas a value of 1 indicates loss of lock of the CDR. If the CDR is in bypass mode, this bit is set to 0. In 64GFC or 50G Ethernet mode, if bit 3 of this byte is set to 1, a value of 0 indicates that the equalizer has finished adaptation and the CDR is locked to the PAM4 signal.

If the content of byte 13d of A0h is set 0Eh and bit 64.3 of page A0h is set to 1, bits 110.3 and bits 118.3 control the locking modes of the internal retimer or CDR. The retimer/CDR locking modes are set according to the logic table defined in Table 10-2. The default value of bits 110.3 and 118.3 is 1.

Table 10-2 Retimer/CDR Rate Select Logic Table

When byte 13d of A0h is set to 0Eh and bit 64.3 of A0h is set to 1			
Logic OR of RS0 pin and RS0 bit	**Logic OR of RS1 pin and RS1 bit**	**Receiver retimer/CDR**	**Transmitter retimer/CDR**
Low/0	Low/0	Lock at low bit rate	Lock at low bit rate
Low/0	High/1	Lock at high bit rate	Bypass
High/1	Low/0	Bypass	Bypass
High/1	High/1	Lock at high bit rate	Lock at high bit rate
NOTE: Low and high bit rates are defined in byte 13d of A0h.			

10.2 Vendor Specific Locations [Address A2h, Bytes 120-126]

Addresses 120-126 are defined for vendor specific memory functions. Potential usage includes vendor password field for protected functions, scratch space for calculations or other proprietary content.

10.3 Optional Page Select Byte [Address A2h, Byte 127]

In order to provide memory space for DWDM and CDR control functions and for other potential extensions, multiple Pages can be defined for the upper half of the A2h address space. At startup the value of byte 127 defaults to 00h, which points to the User EEPROM. This ensures backward compatibility for transceivers that do not implement the optional Page structure. When a Page value is written to byte 127, subsequent reads and writes to bytes 128-255 are made to the relevant Page.

This specification defines functions in Pages 00h to 02h. Pages 03h to 7Fh are reserved for future use. Writing the value of a non-supported Page shall not be accepted by the transceiver. The Page Select byte shall revert to 0 and read / write operations shall be to the unpaged A2h memory map.

Pages 80h-FFh are reserved for vendor specific functions.

Table 10-3 Optional Page Select Byte

A2h	# Bytes	Name	Description
120-126	7	Vendor Specific	Vendor specific memory addresses
127	1	Optional Page Select	Defines the page number for subsequent reads and writes to locations A2h<128-255>

10.4 User Accessible EEPROM Locations [Address A2h, Page 00h / 01h, Bytes 128-247]

For transceivers that do not support pages, or if the Page Select byte is written to 00h or 01h, addresses 128-247 represent 120 bytes of user/host writable non-volatile memory - for any reasonable use. Consult vendor datasheets for any limits on writing to these locations, including timing and maximum number of writes. Potential usage includes customer specific identification information, usage history statistics, scratch space for calculations, etc. It is generally not recommended this memory be used for latency critical or repetitive uses.

Table 10-4 User Accessible EEPROM Locations

A2h	# Bytes	Name	Description
128-247	120	User EEPROM	User writable EEPROM

10.5 Vendor Specific Control Function Locations [Address A2h, Page 00h / 01h, Bytes 248-255]

For transceivers that do not support pages, or if the Page Select byte is written to 00h or 01h, addresses 248-255 are defined for vendor specific control functions. Potential usage includes proprietary functions enabled by specific vendors, often managed in combination with addresses 120-127.

Table 10-5 Vendor Specific Control Function Locations

A2h	# Bytes	Name	Description
248-255	8	Vendor Specific	Vendor specific control functions

10.6 Variable Receiver Decision Threshold Control [Address A2h, Page 02h, Bytes 130-131]

Byte 131 of Page 02h is used to control the variable receiver decision threshold function. The availability of this function is indicated in address A0h, byte 65, bit 7. Byte 131 is a two's complement 7-bit value (-128 to +127). The decision threshold is given by:

Decision Threshold = 50% + [Byte (131) / 256] * 100%

where Decision Threshold is expressed as a percentage of the received eye amplitude.

The value of byte 131 defaults to 0 on power-up. This corresponds to a threshold of 50%.

Table 10-6 Variable Receiver Decision Threshold Control

Address	# Bytes	Name	Description
130	1	Reserved	Reserved for additional receiver controls
131	1	Optional RDT Control	Value sets the receiver decision threshold: 10000000b = -128d; threshold = 0% 00000000b = 0d; threshold = 50% 01111111b = +127d: threshold = 99.61%

---------- END OF DOCUMENT ----------