TRANSCEIVERS

Marvell Solutions

88E1112 Datasheet

Integrated 10/100/1000
Gigabit Ethernet Transceiver

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Document Status	
Advance Information	This document contains design specifications for initial product development. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
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Integrated 10/100/1000 Gigabit Ethernet Transceiver

Overview

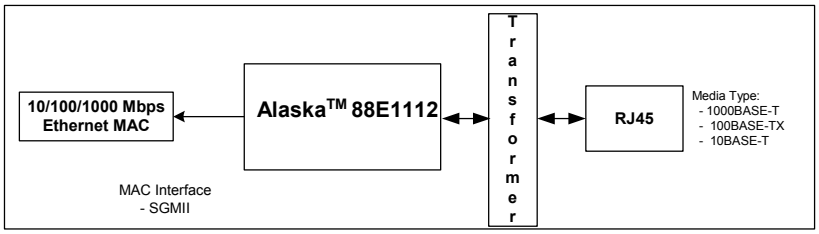
The Alaska 88E1112 Gigabit Ethernet Transceiver is a physical layer device for Ethernet 1000BASE-T, 100BASE-TX, and 10BASE-T applications. It is manufactured using standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 5 unshielded twisted pair.

The Alaska 88E1112 device supports the Serial Gigabit Media Independent Interface (SGMII) for direct connection to a MAC/Switch port. The 88E1112 device incorporates an additional 1.25 GHz SERDES (Serializer/Deserializer) which may be connected directly to a fiber-optic transceiver for 1000BASE-X applications. The SERDES is switchable to support 125 MHz operation for 100BASE-FX applications. Additionally, the 88E1112 device may be used to implement 10/100/1000BASE-T Gigabit Interface Converter (GBIC) or Small Form Factor Pluggable (SFP) modules.

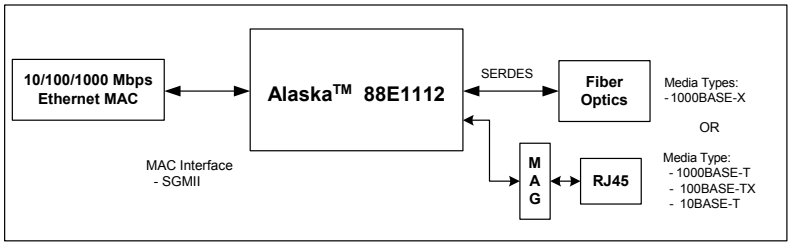
The 88E1112 device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The device achieves robust performance in noisy environments with very low power dissipation.

Features

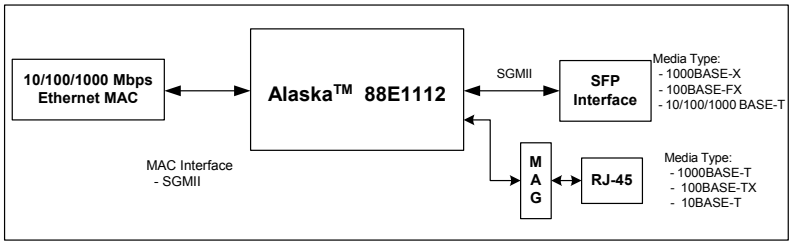
- 10/100/1000BASE-T IEEE 802.3 compliant
- Supports Serial Gigabit Media Independent Interface (SGMII)
- Integrated 1.25 GHz SERDES for 1000BASE-X fiber applications
- Integrated 125 MHz SERDES for 100BASE-FX fiber applications
- SGMII to SERDES mode supported
- SGMII to SGMII bridging supported
- Supports tri-speed GBIC/SFP applications
- Media Detection™ mode for copper and fiber support
- Integrated Virtual Cable Tester™ (VCT™) cable diagnostic feature
- 2-pair downshift feature
- Auto-MDI/MDIX feature when link partner Auto-Negotiation enabled or disabled
- Advanced diagnostics: CRC error checker, packet counter, pattern generator
- EEPROM support for PHY configuration
- Selectable MDC/MDIO interface or Two-Wire Serial Interface
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Requires only two supplies: 2.5V and 1.2V
- Very low power dissipation P_{AVE} = 0.75W
- Manufactured in a 64-Pin QFN, 9X9 mm package



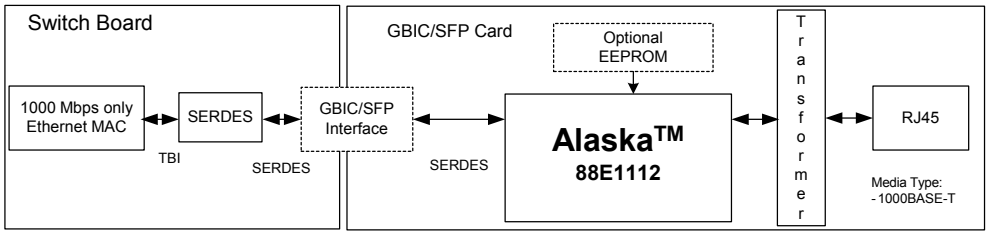
Alaska 88E1112 used in Copper Applications



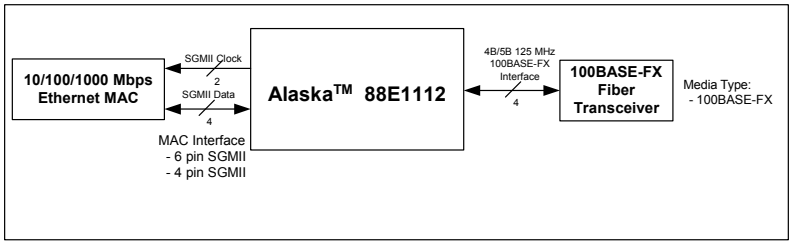
Alaska 88E1112 used in Media Detect ™ Applications (SERDES)



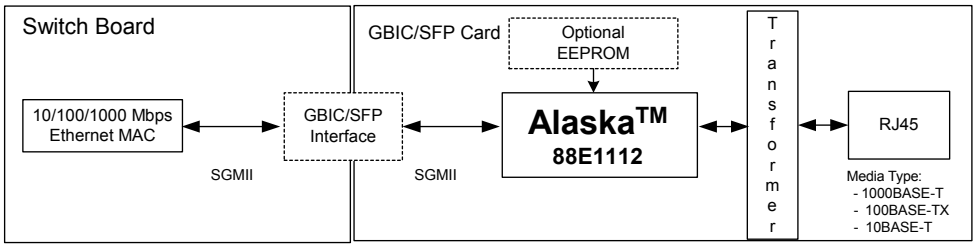
Alaska 88E1112 used in Media Detect ™ Applications (SGMII)



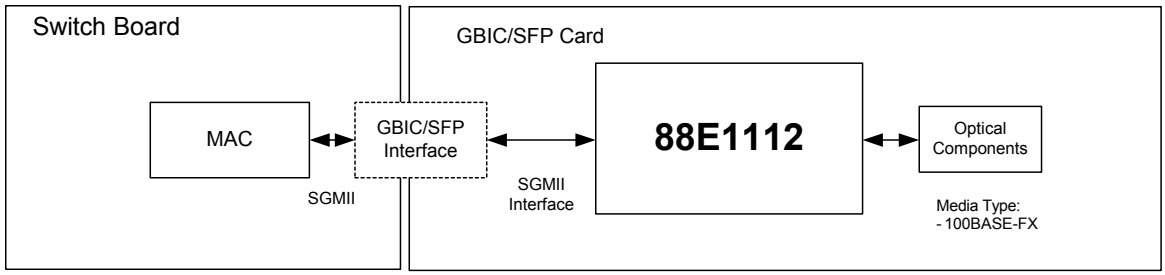
Alaska 88E1112 used in 1000BASE-T GBIC/ SFP Applications



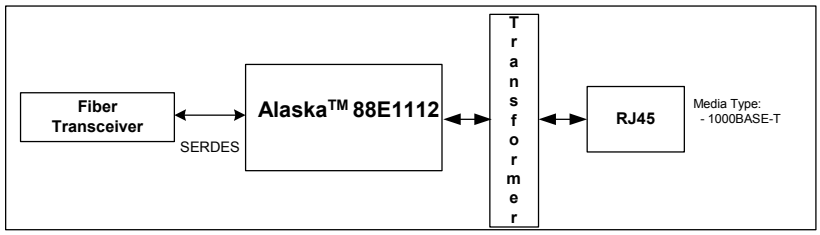
Alaska 88E1112 used in Traditional 100BASE-FX Applications



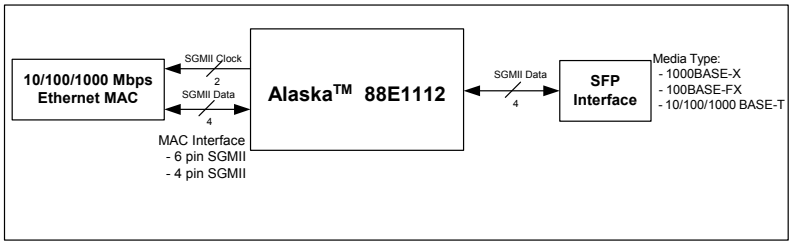
Alaska 88E1112 used in 10/100/1000BASE-T tri-speed GBIC/SFP Applications



Alaska 88E1112 used in 100BASE-FX GBIC/SFP Applications



Alaska 88E1112 used in Media Converter Applications



Alaska 88E1112 used in 4-pin SGMII to 6-pin SGMII Conversions

Table of Contents

Section 1. Signal Description

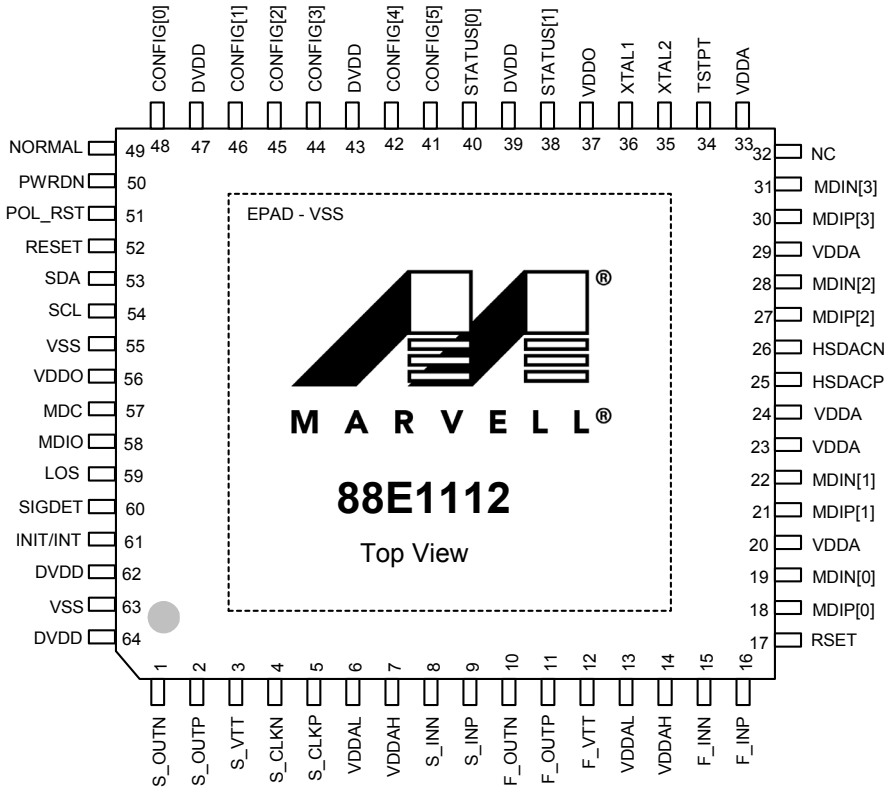
The 88E1112 device is a 10/100/1000BASE-T/1000BASE-X Gigabit Ethernet transceiver.

Note

The pinout and the pin names are subject to change.

1.1 88E1112 64-Pin QFN Package

Figure 1: 88E1112 64-Pin QFN Package (Top View)



1.2 Pin Description

1.2.1 Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

Table 1: Copper Interface

Pin #	Pin Name	Pin Type	Description
18 19	MDIP[0] MDIN[0]	I/O	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] correspond to BI_DA±. In MDIX configuration, MDIP/N[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. MDIP/N[0] should be tied to ground if not used.
21 22	MDIP[1] MDIN[1]	I/O	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] correspond to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. MDIP/N[1] should be tied to ground if not used.
27 28	MDIP[2] MDIN[2]	I/O	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. MDIP/N[2] should be tied to ground if not used.
30 31	MDIP[3] MDIN[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] correspond to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. MDIP/N[3] should be tied to ground if not used.

Table 2: Fiber Interface: 1000BASE-X/SGMII Media Interface/100BASE-FX

Pin #	Pin Name	Pin Type	Description
16 15	F_INP F_INN	I	1.25 GHz input - Positive and Negative (1000BASE-X and SGMII Media Interface 125 MHz Input - Positive and Negative (100BASE-FX) The fiber-optic transceiver's positive output connects to the F_INP. The fiber-optic transceiver's negative output connects to the F_INN.
60	SIGDET	I	SERDES signal detect 1 = Signal Detected 0 = No Signal Detected Polarity can be changed through register 16_1.9.
11 10	F_OUTP F_OUTN	O	1.25 GHz output - Positive and Negative (1000BASE-X and SGMII Media Interface 125 MHz output - Positive and Negative (100BASE-FX) The fiber-optic transceiver's positive input connects to the F_OUTP. The fiber-optic transceiver's negative input connects to the F_OUTN. Output amplitude can be adjusted via register 26_1.2:0.

Table 3: MAC Interface

Pin #	Pin Name	Pin Type	Description
9 8	S_INP S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
5 4	S_CLKP S_CLKN	O	SGMII 625 MHz Receive Clock output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0
2 1	S_OUTP S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0.
59	LOS	O	Loss of Signal/LED Status On hardware reset, LOS defaults to loss of signal where Hi-Z = Loss of Signal 0 = Media interface has link The LOS pin can be configured to output other status. Refer to the Section "LOS Output" on page 23.

Table 4: Management Interface/Control

Pin #	Pin Name	Pin Type	Description
57	MDC/SSCL[1]	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 8.3 MHz. When the 88E1112 device is connected to a Two-Wire Serial Interface (TWSI) bus, MDC is connected to a serial clock line (SSCL). Data is stable during the high portion of the clock.
58	MDIO/SSDA[1]	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm When 88E1112 device is connected to a Two-Wire Serial Interface (TWSI) bus, MDIO connects to the serial data lines (SSDA). These pins are open-drain and maybe be wire-ORed with any number of open-drain devices. SSDA requires 1.5 kohm to 10 kohm pull-up resistors.

1. SSCL and SSDA pins should not be confused by the SCL and SDA pins. The SSCL, SSDA pins act like slaves in the TWSI bus. The SCL and SDA pins act like masters in EEPROM interface. Refer to Table 25 and Table 26.

Table 5: EEPROM Interface

Pin #	Pin Name	Pin Type	Description
54	SCL	O	EEPROM Serial Clock
53	SDA	I/O	EEPROM Serial Data. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm

Table 6: Clock/Configuration/Reset/I/O Voltage Clamp Selection

Pin #	Pin Name	Pin Type	Description
48	CONFIG[0]	I	Configuration 0 pin
46	CONFIG[1]	I	Configuration 1 pin
45	CONFIG[2]	I	Configuration 2 pin
44	CONFIG[3]	I	Configuration 3 pin
42	CONFIG[4]	I	Configuration 4 pin
41	CONFIG[5]	I	Configuration 5 pin
38	STATUS[1]	O, mA	LED Status 1 pin
40	STATUS[0]	O, mA	LED Status 0 pin
61	INIT/INT	O	This is a triple function pin used for PHY Initialization, device interrupt, or LED Status. On hardware reset, INIT defaults to loss of signal where Hi-Z = PHY initialization is in process 0 = PHY registers initialized via EEPROM is complete The INIT pin can be configured to output other status. Refer to Section 2.19.4 "INIT Functionality" on page 69 for PHY initialization details. Refer to Section 2.20 "Interrupt" on page 69 for Interrupt pin functionality. Refer to Section 2.21 "LED" on page 70 for LED pin functionality.
36	XTAL1	I	25 MHz Clock Input 25 MHz ± 50 ppm tolerance crystal reference or oscillator input.
35	XTAL2	O	25 MHz Crystal Output. 25 MHz ± 50 ppm tolerance crystal reference. When the XTAL2 pin is not connected, it should be left floating.
52	RESET	I	Hardware reset. XTAL1 must be active for a minimum of 10 clock cycles before the rising edge of RESET. RESET must be in inactive state for normal operation. Reset Polarity is determined by POL_RST. See POL_RST below for details.
51	POL_RST	I, PU	Reset Polarity. If POL_RST = 1 or Unconnected 1 = Reset 0 = Normal operation If POL_RST = 0 1 = Normal operation 0 = Reset
50	PWRDN	I	1 = Power down 0 = Power up See Section "PWRDN Pin Functionality" on page 43 for details.
49	NORMAL	I, PU	Test Mode Control 0 = Test mode 1 = Normal

Table 7: Test

Pin #	Pin Name	Pin Type	Description
25 26	HSDACP HSDACN	O	AC Test Point. Positive and Negative. These pins should be left floating but brought out for probing.
34	TSTPT	O	DC Test Point

Table 8: Reference

Pin #	Pin Name	Pin Type	Description
17	RSET	I	Resistor Reference External 5.0 kohm 1% resistor connected to ground.

Table 9: Power & Ground

Pin #	Pin Name	Pin Type	Description
39 43 47 62 64	DVDD	Power	1.2V Digital Supply
12	F_VTT	Power	SERDES Output Supply See Section 2.6.3 "F_VTT and S_VTT" on page 42.
3	S_VTT	Power	SGMII Output Supply See Section 2.6.3 "F_VTT and S_VTT" on page 42.
20 23 24 29 33	VDDA	Power	2.5V Analog Supply.
37 56	VDDO	Power	1.5V, or 2.5V I/O Supply. **NOTE:** If crystal is used between XTAL1 and XTAL2 pins then refer to Table 4.2 on page 147 for details.
7 14	VDDAH	Power	2.5V Analog Supply.
6 13	VDDAL	Power	1.5V or 2.5V Analog Supply. 2.5V Analog Supply will draw more power.
EPAD 55 63	VSS	Ground	Ground. The 88E1112 device is contained in a 64 pin QFN package, which has an exposed die pad (E-PAD) at its base. The EPAD must be soldered to VSS. The location of the EPAD can be found in Section 5.1 "64 - Pin 9x9 mm QFN Package" on page 178 and Table 93, “64-Pin QFN Package Dimensions,” on page 179.
32	No Connect	NC	NC

1.3 64-Pin QFN Pin Assignment List - Alphabetical by Signal Name

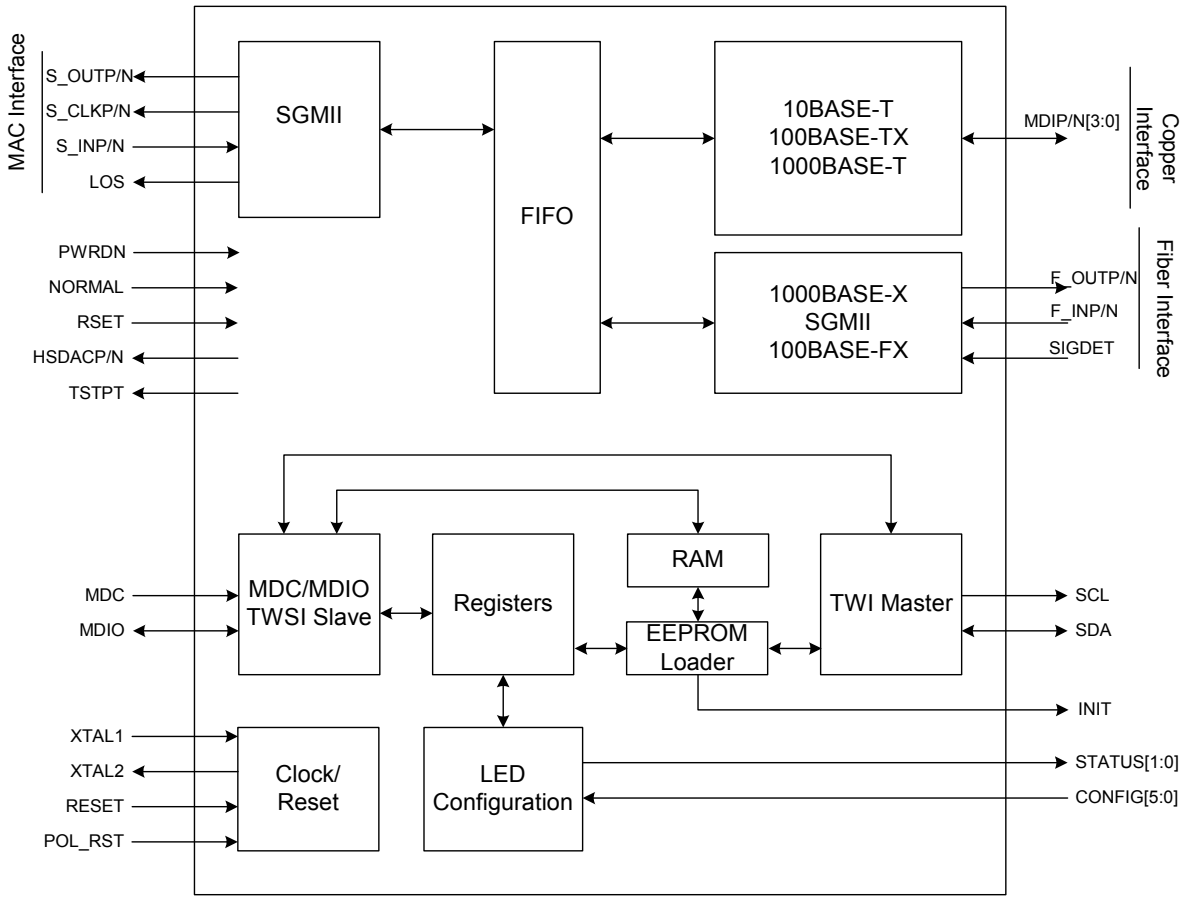
Pin #	Pin Name	Pin #	Pin Name
48	CONFIG[0]	50	PWRDN
46	CONFIG[1]	52	RESET
45	CONFIG[2]	17	RSET
44	CONFIG[3]	54	SCL
42	CONFIG[4]	4	S_CLKN
41	CONFIG[5]	5	S_CLKP
39	DVDD	53	SDA
43	DVDD	60	SIGDET
47	DVDD	8	S_INN
62	DVDD	9	S_INP
64	DVDD	1	S_OUTN
15	F_INN	2	S_OUTP
16	F_INP	3	S_VTT
10	F_OUTN	40	STATUS[0]
11	F_OUTP	38	STATUS[1]
12	F_VTT	34	TSTPT
26	HSDACN	20	VDDA
25	HSDACP	23	VDDA
61	INIT/INT	24	VDDA
59	LOS	29	VDDA
57	MDC	33	VDDA
19	MDIN[0]	7	VDDAH
18	MDIP[0]	14	VDDAH
22	MDIN[1]	6	VDDAL
21	MDIP[1]	13	VDDAL
28	MDIN[2]	37	VDDO
27	MDIP[2]	56	VDDO
31	MDIN[3]	EPAD	VSS
30	MDIP[3]	55	VSS
58	MDIO	63	VSS
32	NC	36	XTAL1
49	NORMAL	35	XTAL2
51	POL_RST		

Section 2. Functional Specifications

The 88E1112 device is a 10/100/1000BASE-T/1000BASE-X/100BASE-FX Gigabit Ethernet transceiver.

Figure 2 shows the functional block diagram of the 88E1112 device.

Figure 2: 88E1112 device Functional Block Diagram



2.1 Data Interfaces

The 88E1112 device has 3 different interfaces for transmitting and receiving packets. The interfaces are named after their most common mode of use.

MAC Interface

The MAC Interface consists of the pins S_OUTP/N, S_INP/N, S_CLKP/N, and LOS. Typically, this interface is used to connect to an SGMII or SERDES MAC. There are three modes of operation:

- SGMII
- GBIC
- Media Converter (GBIC mode without GBIC Auto-Negotiation)

Fiber Interface

The fiber Interface consists of the pins F_OUTP/N, F_INP/N, and SIGDET. There are three modes of operation

- 1000BASE-X
- 100BASE-FX
- SGMII (Media Interface)

Copper Interface

The copper interface consists of the MDIP/N[3:0] pins that connect to the physical media for 1000BASE-T, 100BASE-TX, and 10BASE-T modes of operation. The MDI pins should be terminated externally with 100 ohm differential impedance and connected to an RJ-45 connector through magnetics.

The CAT 5 UTP interface requires 100 ohm differential external terminations. See the "Alaska Reference Design Schematics for details".

2.1.1 MAC Interface

The MAC Interface consists of the pins S_OUTP/N, S_INP/N, S_CLKP/N, and LOS. Typically, this interface is used to connect to an SGMII or SERDES MAC. There are three modes of operation:

- SGMII
- GBIC
- Media Converter

The input and output buffers are internally terminated to 50 ohm impedance. The output swing can be adjusted by programming register 26_2.2:0.

The S_VTT power pin supplies the power to the transmitter. The S_VTT power pin should be left floating if internal regulation is desired. The required voltage will be regulated from the VDDAL supply. SEL_VTT should be set to 0 during hardware configuration if internal regulation is used.

In order to save additional power the S_VTT power pin can be supplied externally. This supply can be 1.2V or 1.5V. The relationship between the common mode voltage and S_VTT is described in Section 4.5.3

2.1.1.1 SGMII MAC Interface

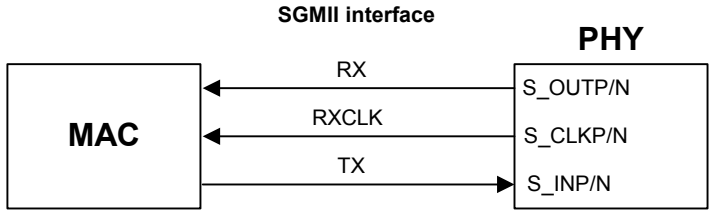
The 88E1112 device supports the SGMII MAC Interface. This interface supports 10, 100, and 1000 Mbps modes of operation. The 88E1112 device does not need a TXCLK input as it recovers this clock from the input data. This feature has the advantage of reducing pin count, the number of traces on the board, as well as EMI and noise generation.

On the receive side, 2 modes of operation: one with a receive clock supplied to the MAC, and one without. The serial interface with clock is selected by setting SGMII_CLK bit to 1 during hardware configuration. The serial interface without clock is selected by setting SGMII_CLK bit to 0. The receive clock is required for MACs that do not have clock recovery capability. The SGMII signal mapping is shown in Table 10.

Table 10: SGMII Serial Interface Pin Mapping

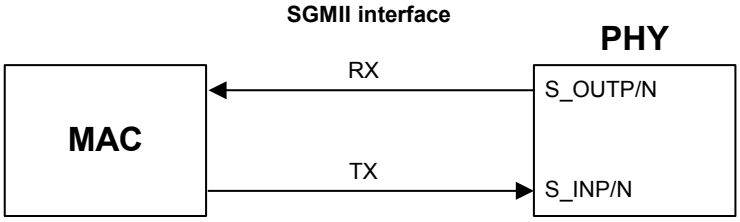
88E1112 Device Pin Name	SGMII Specification Pin Name	Description
S_OUTP/N	RX	1.25 Gbaud receive output - Positive and Negative
S_CLKP/N	RXCLK	625 MHz DDR receive clock
S_INP/N	TX	1.25 Gbaud transmit input - Positive and Negative

Figure 3: SGMII with Receive Reference Clock



A receive reference clock is available on the S_CLKP/N pins. This reference clock is for implementing SGMII for MACs without receive clock recovery.

Figure 4: SGMII without Receive Reference Clock



S_CLKP/N pins can be disabled to save power for MACs with clock recovery capability.

The operational speed of the SGMII MAC Interface is determined according to Table 11.

Table 11: SGMII Operational Speed MAC Interface

Link Status	Copper Auto-Neg 0_0.12	1000BASE-X or SGMII Media Interface Auto-Neg 0_1.12	SGMII MAC Interface Auto-Neg 0_2.12	SGMII MAC Interface Speed
No Link	Don't Care	Don't Care	Don't Care	Determined by speed setting of 0_2.6, 0_2.13
MAC Loopback	Don't Care	Don't Care	Don't Care	Determined by speed setting of 0_2.6, 0_2.13
1000BASE-T	Don't Care	Don't Care	Don't Care	1000 Mbps
100BASE-TX	Don't Care	Don't Care	Don't Care	100 Mbps
10BASE-T	Don't Care	Don't Care	Don't Care	10 Mbps
1000BASE-X	Don't Care	Don't Care	Don't Care	1000 Mbps
SGMII Media Interface 1000 Mbps	Don't Care	Enabled	Don't Care	1000 Mbps
SGMII Media Interface 100 Mbps	Don't Care	Enabled	Don't Care	100 Mbps
SGMII Media Interface 10 Mbps	Don't Care	Enabled	Don't Care	10 Mbps
SGMII Media Interface any speed	Don't Care	Disabled	Don't Care	Determined by speed setting of 0_2.6, 0_2.13
100BASE-FX	Not Applicable	Not Applicable	Don’t Care	100 Mbps

LOS Output

The LOS pin can be configured to indicate whether there is link on the media side. This is useful for SFP applications. See Application Notes "88E1112 SFP Applications".

The LOS is an open drain output. It drives low if any of the following condition occurs, otherwise it goes Hi-Z

1. 1000BASE-T link is up
2. 100BASE-TX link is up
3. 10BASE-T link is up
4. SIGDET pin is active AND 1000BASE-X link is up
5. SIGDET pin is active AND SGMII Media Interface locks to comma
6. SIGDET pin is active AND 100BASE-FX link is up
7. Any force link good register asserted.

Note that the register default for 16_3.15:12 = 0000 and 17_3.7:6 = 10 is required for the LOS functionality as described in this section. Changing these registers will reprogram the LOS pin to operate differently. See Section 2.21 for more details.

The LOS pin is configured to default to this functionality after hardware reset. The LOS can be programmed for other purposes by changing register 16_3.15:12 to some value other than 0000. The active polarity can be changed by setting register 17_3.6. The inactive state can be driven or hi-Z by setting register 17_3.7. See Section 2.21 "LED" on page 70 for more details.

Synchronizing FIFO

The 88E1112 device controls transmit and receive synchronizing FIFOs to reconcile frequency differences between the clocks of the SGMII MAC Interface and the media side. The depth of the transmit and receive FIFOs can be independently programmed by programming register bits 16_2.15:12. See the "Alaska Ultra FAQs" for details on how to calculate required FIFO depth and the details of the different clocks used for transmit and receive in each mode of operation.

The FIFO depths can be increased in length by programming Register 16_2.15:12 to support longer frames. The 88E1112 device can handle jumbo frame sizes up to 10 Kbytes with up to ± 150 PPM clock jitter. The deeper the FIFO depth, the higher the latency will be.

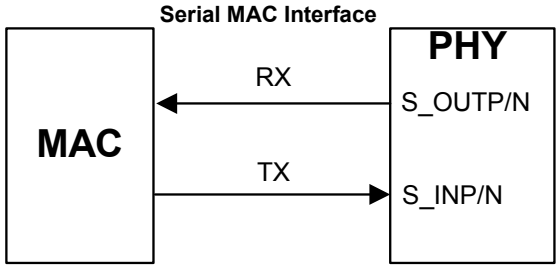
2.1.1.2 GBIC/SFP Interface

The GBIC interface only supports the 1000BASE-T copper interface. Auto-Negotiation information is transferred between the GBIC interface and the link partner attached to the 1000BASE-T interface. See Application Notes "88E1112 SFP Applications" for details.

Table 12: Serial MAC Interface Pin Mapping

88E1112 Device Pin Name	Serial MAC	Description
S_OUTP/N	RX	1.25 Gbaud transmit output - Positive and Negative
S_INP/N	TX	1.25 Gbaud receive input - Positive and Negative

Figure 5: Serial MAC Interface

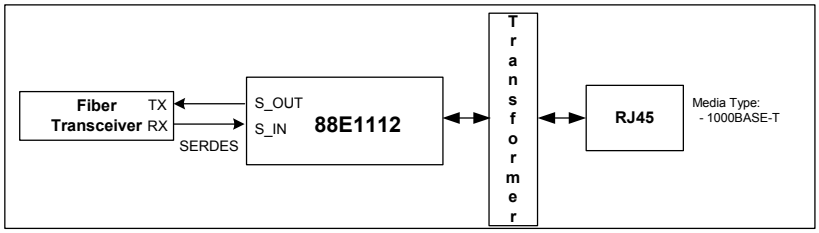


2.1.1.3 Media Converter MAC Interface

For media converter applications, the "MAC Interface" is actually used to connect to a fiber transceiver. S_INP/N and S_OUTP/N pins are connected to the fiber transceiver's receive data and transmit data respectively. This should not be confused with the fiber interface, which uses the F_INP/N and F_OUTP/N pins.

To use the media converter mode, GBIC mode should be selected 16_2.9:7 = 001 and then disable GBIC Auto-Negotiation by setting register 0_2.12 = 0.

Figure 6: Media Converter MAC Interface



2.1.2 Fiber Interface

The fiber Interface consists of the F_OUTP/N, F_INP/N, and SIGDET pins. There are three modes of operation

- 1000BASE-X
- 100BASE-FX
- SGMII (Media Interface)

The PHY can be configured to operate in1000BASE-X mode, 100BASE-FX mode, or in the tri-speed SGMII Media Interface mode.

In the 1000BASE-X mode, the fiber-optic module is connected to F_INP/N and F_OUTP/N pins.

In the100BASE-FX mode, the fiber-optic module is connected to F_INP/N and F_OUTP/N pins

The SGMII Media Interface mode is useful when the 88E1112 device is used as the host to an SFP module.

The input and output buffers are internally terminated to 50 ohm impedance. The output swing can be adjusted by programming register 26_1.2:0.

The F_VTT power pin supplies the power to the transmitter. The F_VTT power pin should be left floating if internal regulation is desired. The required voltage will be regulated from the VDDAL supply. SEL_VTT should be set to 0 during hardware configuration if internal regulation is used.

In order to save additional power the F_VTT power pin can be supplied externally. This supply can be 1.2V or 1.5V. The relationship between the common mode voltage and F_VTT is described in Section 4.5.3.

The signal detect input (SIGDET) is conventionally defined as High = Signal, Low = No signal and no glue logic is needed when interfaced to the optics module for 1000BASE-X or 100BASE-FX. However, when used with SGMII Media Interface the defined interface is the SFP interface where the loss of signal is defined as High = No signal and low = signal. Register 16_1.9 defines the polarity of the SIGDET pin.

16_1.9	SIGDET Low	SIGDET High
0	No signal	Signal
1	Signal	No signal

If signal detect status is not available then SIGDET must be tied to the active signal detect state. The SIGDET pin is a digital input pin.

2.2 88E1112 Device Modes of Operation

The 88E1112 device can be configured to operate in the various modes by setting register 16_2.9:7 as shown in Table 13.

Table 13: Modes of Operation

Mode of Operation	16_2.9:7
SGMII MAC Interface to 100BASE-FX only	000
GBIC to 1000BASE-T Only	001
SGMII MAC Interface to Auto media select (Copper/ SGMII Media Interface)	010
SGMII MAC Interface to Auto media select (Copper/ 1000BASE-X)	011
Reserved	100
SGMII MAC Interface to Copper Only	101
SGMII MAC Interface to SGMII (Media Interface) Only	110
SGMII MAC Interface to 1000BASE-X Only	111

2.2.1 SGMII MAC Interface to Auto Media Detect 10BASE-T/ 100BASE-TX/1000BASE-T/1000BASE-X

The SGMII MAC Interface to Auto media detect between 10/100/1000BASE-T and 1000BASE-X is selected by setting the MODE[1:0] to 11 during hardware configuration or by setting register 16_2.9:7 to 011. Two submodes with auto media detect turned off - SGMII MAC Interface to 10/100/1000BASE-T and SGMII MAC Interface to 1000BASE-X can be selected by setting 16_2.9:7 to 101 and 111 respectively.

When the fiber interface is running in 1000BASE-X mode, the serial 1.25 GHz SGMII MAC Interface encoding is identical to that found in 1000BASE-X.

When the copper interface is running in 1000BASE-T mode, the serial 1.25 GHz SGMII MAC Interface encoding is identical to that found in 1000BASE-X.

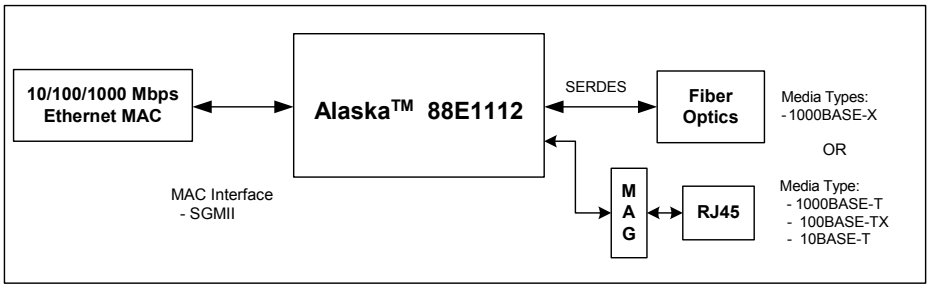
In 100BASE-TX and 10BASE-T modes, the SGMII interface still runs at 1.25 GHz using 1000BASE-X encoding. However, each byte of data in the packet is repeated 10 or 100 times, respectively.

The SGMII MAC Interface implements a modified 1000BASE-X Auto-Negotiation to indicate link, duplex, and speed to the MAC. The result of the Auto-Negotiation exchange on the copper/fiber side is encoded onto the SGMII MAC Interface via the modified Auto-Negotiation so that the MAC can adjust to the correct operating speed.

Note that the fiber interface side is running normal 1000BASE-X auto-negotiation and not the modified auto-negotiation used on the SGMII MAC Interface.

Figure 7 is an example of an device using the SGMII MAC Interface to 10/100/1000BASE-T/1000BASE-X.

Figure 7: Media Detect Applications (SERDES)



2.2.2 SGMII MAC Interface to Auto Media Detect 10BASE-T/ 100BASE-TX/1000BASE-T/SGMII Media Interface

The SGMII MAC Interface to Auto media detect between 10/100/1000BASE-T and SGMII Media Interface is selected by setting the MODE[1:0] to 10 during hardware configuration or by setting register 16_2.9:7 to 010. Two submodes with auto media detect turned off - SGMII MAC Interface to 10/100/1000BASE-T and SGMII MAC Interface to SGMII Media Interface can be selected by setting 16_2.9:7 to 101 and 110 respectively.

This mode is useful for applications that normally require a copper port but allows for the flexibility of plugging in a tri-speed SFP module. For example, 100BASE-FX can be supported by connecting an SGMII to 100BASE-FX SFP module to the SGMII Media Interface.

When the fiber interface is running in SGMII Media Interface mode, the serial 1.25 GHz SGMII MAC Interface encoding is identical to that found in 1000BASE-X. The SGMII Media Interface implements a modified 1000BASE-X auto-negotiation except that it implements the MAC side of the SGMII instead of the PHY side of the SGMII. Depending on the negotiated speed each byte of data in the packet is replicated 1, 10, or 100 times.

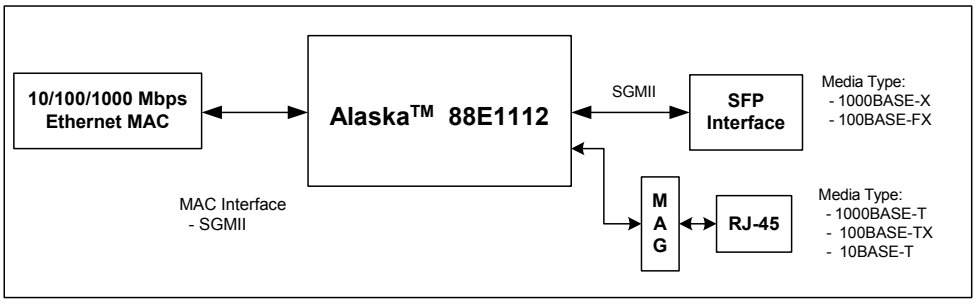
When the copper interface is running in 1000BASE-T mode, the serial 1.25 GHz SGMII MAC Interface encoding is identical to that found in 1000BASE-X.

In 100BASE-TX and 10BASE-T modes, the SGMII interface still runs at 1.25 GHz using 1000BASE-X encoding. However, each byte of data in the packet is repeated 10 or 100 times, respectively.

The SGMII MAC Interface implements a modified 1000BASE-X Auto-Negotiation to indicate link, duplex, and speed to the MAC. The result of the Auto-Negotiation exchange on the copper/fiber side is encoded onto the serial interface via the modified Auto-Negotiation so that multi-port devices can adjust to the correct operating speed.

Figure 8 is an example of an 88E1112 device using the SGMII MAC Interface to 10/100/1000BASE-T / SGMII Media Interface.

Figure 8: Media Detect Applications (SGMII)



2.2.3 GBIC to 1000BASE-T

In GBIC to 1000BASE-T mode is selected by setting the MODE[1:0] to 01 or by setting register 16_2.9:7 to 001.

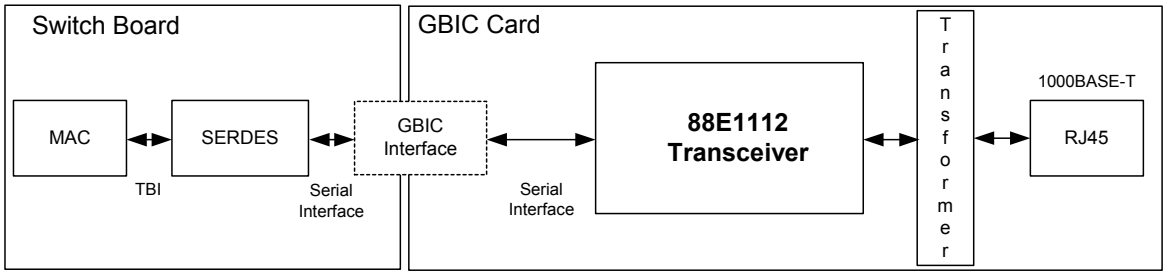
Figure 9 is an example of the device used for a GBIC application.The GBIC interface supports 1000 Mbps operation only.

The 1000BASE-X Auto-Negotiation information received from the MAC is used by the PHY to control what abilities the PHY advertises on the copper side. For example, if the MAC advertises only full-duplex, but the PHY is configured to advertise both full-duplex and half-duplex, the PHY only advertises full-duplex. The advertise register settings or the configuration pin strap option settings are not modified, although what is advertised on the line is now different.

After the copper Auto-Negotiation is complete, the copper side Auto-Negotiation results are sent to the MAC using 1000BASE-X Auto-Negotiation. For example, the link partner's abilities such as flow control and duplex are indicated to the MAC. The MAC, based on this information, will determine the mode of operation.

This Auto-Negotiation mechanism is different from the SGMII modified 1000BASE-X Auto-Negotiation. In SGMII, the Auto-Negotiation is completely done by the PHY. The PHY only reports the results of the Auto-Negotiation such as speed and duplex, as well as link status to the MAC. The only way the MAC can control Auto-Negotiation in SGMII mode is by register writes using the MDC/MDIO interface. In GBIC to 1000BASE-T mode, this process is automatic.

Figure 9: Typical GBIC Application



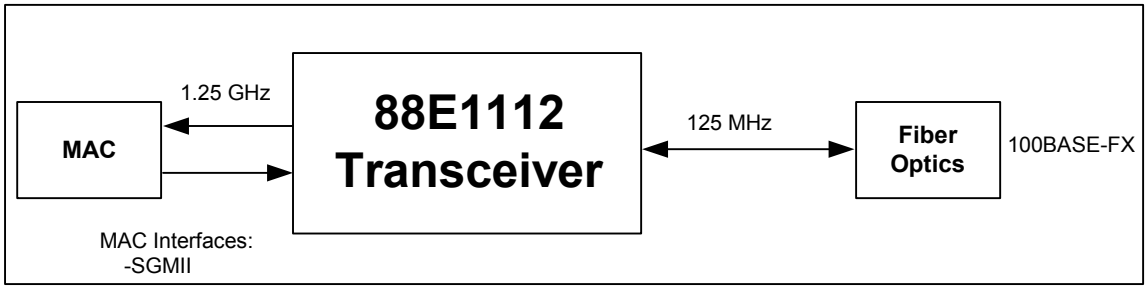
2.2.4 SGMII MAC Interface to 100BASE-FX

In the 100BASE-FX mode, the SGMII interface still runs at 1.25 GHz using 1000BASE-X encoding. However, each byte of data in the packet is repeated 10 times.

The SGMII MAC Interface implements a modified 1000BASE-X Auto-Negotiation to indicate link, duplex, and speed to the MAC. The result of the Auto-Negotiation exchange on the copper/fiber side is encoded onto the serial interface via the modified Auto-Negotiation so that multi-port devices can adjust to the correct operating speed.

Figure 10 is an example of an device using the SGMII MAC Interface to 100BASE-FX.

Figure 10: MAC to Copper Connection



2.3 Loopback

The 88E1112 device has 3 different interfaces for transmitting and receiving packets as discussed in Section 2.1:

- The MAC Interface
- The Copper Interface and
- The Fiber Interface.

Each interface can be tested in loopback mode.

Register 0 is used to enable loopback testing as well as setting the speed of the interface during loopback testing.

- Page 0 of register 0 is used to set the speed for the copper interface.
- Page 1 of register 0 is used to set the speed for the fiber interface
- Page 2 of register 0 is used to set the speed for the MAC interface

Caution

Register 0 bit 14 is used to enable loopback test mode. Care has to be taken to choose the correct page for the correct interface. The pages used differ from the speed setting discussed above.

- Page 0 or 1 of register 0.14 is used to enable loopback for the **MAC interface.**
- Page 2 of register 0.14 is used to enable loopback for the **Fiber or Copper interface.** The loopback will be done on the media interface that has the linkup. It is required to have linkup during fiber or copper interface loopback.

Note

The Copper and Fiber Interface loopback modes are also called line loopback modes since typically the data is coming from the "line", i.e., the copper or fiber cable.

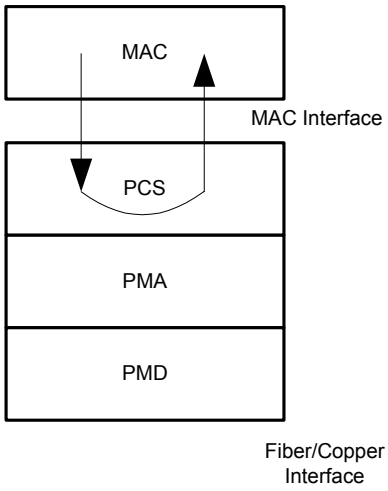
2.3.1 MAC Interface Loopback

The functionality, timing, and signal integrity of the MAC interface can be tested by placing the 88E1112 device in MAC interface loopback mode. This can be accomplished by setting register 0_0.14 = 1 or 0_1.14 = 1 (0_0.14 and 0_1.14 are physically the same register bit. Setting or resetting one also sets or resets the other register bit). In loopback mode, the data received from the MAC is not transmitted out on the media interface. Instead, the data is looped back and sent to the MAC. For copper media, during loopback, link will be lost and packets will not be received. When performing a register 0_0.14 or 0_1.14 MAC Interface loopback during a mode that uses copper medium, the copper receiver will be powered down, link will not come up and any data received will not be transferred. Idles will be transmitted out the copper transmitter.

If auto-negotiating and loopback is enabled, FLP Auto-Negotiation codes will be transmitted. If in forced 10BASE-T mode and loopback is enabled, 10BASE-T idle link pulses will be transmitted on the copper side. If in forced 100BASE-TX mode and loopback is enabled, 100BASE-TX idles will be transmitted on the copper side.

When performing a register 0_0.14 or 0_1.14 loopback during a mode that uses the fiber medium, the fiber transceiver will be powered up and sync status will be up if valid code groups are received. Any data received from the MAC will not be transmitted on the cable. Idles will be transmitted out the fiber transmitter.

Figure 11: MAC Interface Loopback Diagram



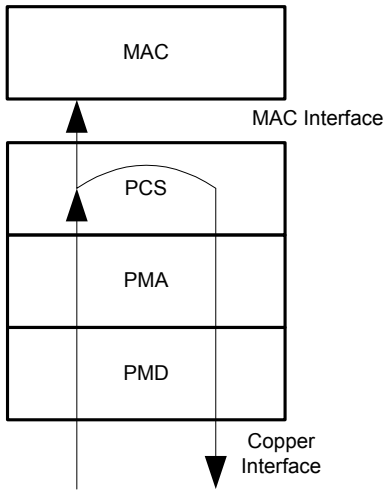
To perform MAC Interface loopback SGMII Auto-Negotiation should be disabled by writing to register 0_2.12 = 0. The MAC should also disable SGMII Auto-Negotiation during loopback.

The speed of the SGMII MAC Interface is determined by register 0_2.6 and 0_2.13 during loopback and link down. {0_2.6, 0_2.13} is 00 = 10 Mbps, 01 = 100 Mbps, 10 = 1000 Mbps. This is true regardless of whether 0_2.12 (auto-negotiation is enabled or disabled).

2.3.2 Copper Interface Loopback

Copper Interface loopback allows a link partner to send frames into the 88E1112 device to test the transmit and receive data path. Frames from a link partner into the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during line loopback. Refer to Figure 12. This allows the link partner to receive its own frames.

Figure 12: Copper Interface Data Path



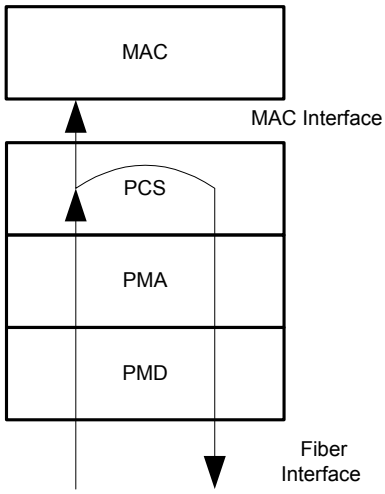
Before enabling the line loopback feature, the PHY must first establish link to another PHY link partner. If Auto-Negotiation is enabled, both link partners should advertise the same speed and full-duplex. If Auto-Negotiation is disabled, both link partners need to be forced to the same speed and full-duplex. Once link is established, enable the line loopback mode by writing to register 0_2.14

- 0_2.14 = 1 (Enable line loopback)
- 0_2.14 = 0 (Disables line loopback)

2.3.3 Fiber Interface Loopback

Fiber Interface loopback allows a link partner to send frames into the 88E1112 device to test the transmit and receive data path. Frames from a link partner into the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during fiber interface loopback. Refer to Figure 13. This allows the link partner to receive its own frames.

Figure 13: Fiber Interface Data Path



Before enabling the fiber interface loopback feature, link has to be first established on the fiber interface. Once link is established, enable the line loopback mode by writing to register 0_2.14

- 0_2.14 = 1 (Enable line loopback)
- 0_2.14 = 0 (Disables line loopback)

2.3.4 External Loopback

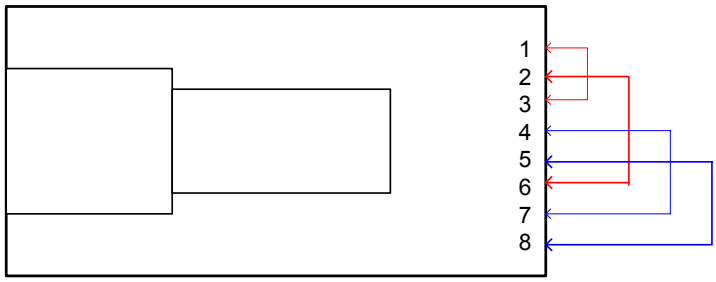
For production testing, an external loopback stub allows testing of the complete data path without need for a link partner.

2.3.4.1 Copper Media

The loopback stub consists of a plastic RJ-45 header, connecting RJ-45 pair 1,2 to pair 3,6 and connecting pair 4,5 to pair 7,8, as seen in Figure 14.

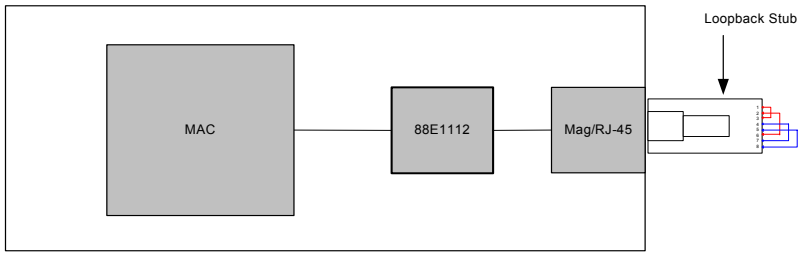
For 10BASE-T and 100BASE-TX modes, the loopback test requires no register writes. For 1000BASE-T mode, register 16_6.5 must be set to 1 to enable the external loopback. All copper modes require an external loopback stub.

Figure 14: Loopback Stub (Top View with Tab up)



The external loopback test setup requires the presence of a MAC that will originate the frames to be sent out through the PHY. Instead of a normal RJ-45 cable, the loopback stubs allows the PHY to self-link at 1000 Mbps. It also allows the actual external loopback. See Figure 15. The MAC should see the same packets it sent, looped back to it.

Figure 15: Test Setup for 10/100/1000 Mbps Modes using an External Loopback Stub

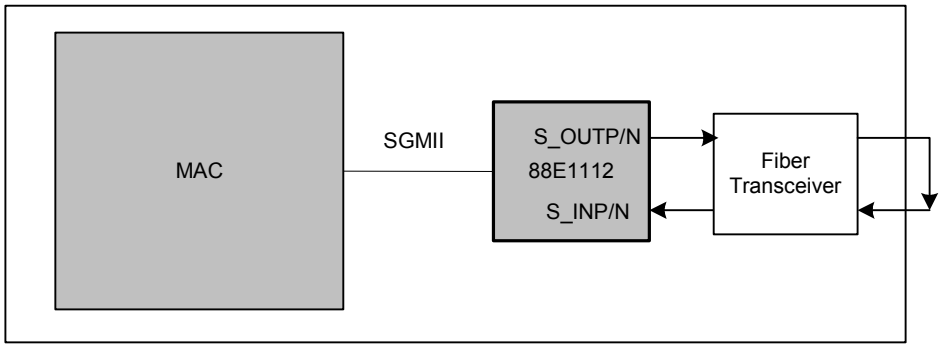


2.3.4.2 Fiber Media

For 1000BASE-X mode and 100BASE-FX mode, the loopback test requires no register writes. For SGMII Media Interface mode, the auto-negotiation must be turned off in order for the external loopback to work. This is because the SGMII auto-negotiation is not symmetrical. To turn off the SGMII Media Interface auto-negotiation register 0_1.12 should be set to 0.

If the SGMII Media Interface auto-negotiation is turned off then the speed is determined by 0_1.6 and 0_1.13, where {0_1.6, 0_1.13}= 00 is 10 Mbps, = 01 is 100 Mbps, and = 10 is 1000 Mbps.

Figure 16: Fiber External Loopback



2.4 Hardware Configuration

The RESET pin is active high or active low depending on the setting of POL_RST as listed in Table 14. The POL_RST pin has an internal pull-up resistor so the effect of leaving it floating has the same effect as tying it high.

If RESET is active low, it is backwards compatible to all previous PHY products.

Table 14: RESET Polarity

POL_RST	RESET = 0	RESET = 1
0	Reset	Normal
1 or floating	Normal	Reset

After the deassertion of RESET the 88E1112 device will be hardware configured. It is assumed that the majority of the PHY configuration will be set via the EEPROM or by the host. The hardware configuration sets up the minimal configuration that must be set before the EEPROM or the host can access the 88E1112 device.

The 88E1112 device is configured through the CONFIG[5:0] pins. Each pin is used to configure 2 bits. The 2-bit value is set depending on what is connected to the CONFIG pins soon after the deassertion of hardware reset. The 2-bit mapping is shown in Table 15.

Table 15: Two Bit Mapping

Pin	Bit1, Bit 0
VSS	00
STATUS[1]	01
STATUS[0]	10
VDDO	11

The 2 bits for each CONFIG[5:0] is mapped as shown in Table 16.

Table 16: Configuration Mapping

Pin	Bit 1	Bit 0
CONFIG[0]	PHYADR[1]	PHYADR[0]
CONFIG[1]	PHYADR[3]	PHYADR[2]
CONFIG[2]	SGMII_CLK	PHYADR[4]
CONFIG[3]	SEL_TWSI	SEL_VTT
CONFIG[4]	EEPROM[1]	EEPROM[0]
CONFIG[5]	MODE[1]	MODE[0]

Each bit in the configuration is defined as shown in Table 17.

Table 17: Configuration Definition

Bits	Definition
PHYADR[4:0]	PHY Address
SGMII_CLK[1]	0 = S_CLKP/N off
	1 = S_CLKP/N active
EEPROM[1:0]	00 = No EEPROM Read
	01 = Start reading from address 0
	10 = Start reading from address 96
	11 = Start reading from address 128
SEL_TWSI	0 = MDC/MDIO
	1 = Two Wire Serial Interface
SEL_VTT	0 = F_VTT and S_VTT are internally regulated (Leave F_VTT and S_VTT floating).
	1 = F_VTT and S_VTT are externally powered
MODE[1:0][2]	00 = SGMII MAC Interface to 100BASE-FX
	01 = GBIC to Copper
	10 = SGMII MAC Interface to Auto media select (Copper/SGMII Media Interface
	11 = SGMII MAC Interface to Auto media select (Copper/1000BASE-X)

1. Register 26_2.4 hardware reset default value is determined by the state of SCLK_SGMII.
2. Register 16_2.8:7 hardware reset default value is determined by MODE[1:0].

2.5 Copper Media Transmit and Receive Function

The transmit and receive paths for the 88E1112 device are described in the following sections.

2.5.1 Transmit Side Network Interface

2.5.1.1 Multi-mode TX Digital to Analog Converter

The 88E1112 device incorporates a multi-mode transmit DAC to generate filtered 4D PAM 5, MLT3, or Manchester coded symbols. The transmit DAC performs signal wave shaping to reduce EMI. The transmit DAC is designed for very low parasitic loading capacitances to improve the return loss requirement, which allows the use of low cost transformers.

2.5.1.2 Slew Rate Control and Waveshaping

In 1000BASE-T mode, partial response filtering and slew rate control is used to minimize high frequency EMI. In 100BASE-TX mode, slew rate control is used to minimize high frequency EMI. In 10BASE-T mode, the output waveform is pre-equalized via a digital filter.

2.5.2 Encoder

2.5.2.1 1000BASE-T

In 1000BASE-T mode, the transmit data bytes are scrambled to 9-bit symbols and encoded into 4D PAM 5 symbols. Upon initialization, the initial scrambling seed is determined by the PHY address. This prevents multiple 88E1112 devices from outputting the same sequence during idle, which helps to reduce EMI.

2.5.2.2 100BASE-TX

In 100BASE-TX mode, the transmit data stream is 4B/5B encoded, serialized, and scrambled.

2.5.2.3 10BASE-T

In 10BASE-T mode, the transmit data is serialized and converted to Manchester encoding.

2.5.3 Receive Side Network Interface

2.5.3.1 Analog to Digital Converter

The 88E1112 device incorporates an advanced high speed ADC on each receive channel with greater resolution than the ADC used in the reference model of the 802.3ab standard committee. Higher resolution ADC results in better SNR, and therefore, lower error rates. Patented architectures and design techniques result in high differential and integral linearity, high power supply noise rejection, and low metastability error rate. The ADC samples the input signal at 125 MHz.

2.5.3.2 Active Hybrid

The 88E1112 device employs a sophisticated on-chip hybrid to substantially reduce the near-end echo, which is the super-imposed transmit signal on the receive signal. The hybrid minimizes the echo to reduce the precision requirement of the digital echo canceller. The on-chip hybrid allows both the transmitter and receiver to use the same transformer for coupling to the twisted pair cable, which reduces the cost of the overall system.

2.5.3.3 Echo Canceller

Residual echo not removed by the hybrid and echo due to patch cord impedance mismatch, patch panel discontinuity, and variations in cable impedance along the twisted pair cable result in drastic SNR degradation on the receive signal. The 88E1112 device employs a fully developed digital echo canceller to adjust for echo impairments from more than 100 meters of cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

2.5.3.4 NEXT Canceller

The 1000BASE-T physical layer uses all 4 pairs of wires to transmit data to reduce the baud rate requirement to only 125 MHz. This results in significant high frequency crosstalk between adjacent pairs of cable in the same bundle. The 88E1112 device employs 3 parallel NEXT cancellers on each receive channel to cancel any high frequency crosstalk induced by the adjacent 3 transmitters. A fully adaptive digital filter is used to compensate for the time varying nature of channel conditions.

2.5.3.5 Baseline Wander Canceller

Baseline wander is more problematic in the 1000BASE-T environment than in the traditional 100BASE-TX environment due to the DC baseline shift in both the transmit and receive signals. The 88E1112 device employs an advanced baseline wander cancellation circuit to automatically compensate for this DC shift. It minimizes the effect of DC baseline shift on the overall error rate.

2.5.3.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.5.3.7 Digital Phase Lock Loop

In 1000BASE-T mode, the slave transmitter must use the exact receive clock frequency it sees on the receive signal. Any slight long-term frequency phase jitter (frequency drift) on the receive signal must be tracked and duplicated by the slave transmitter; otherwise, the receivers of both the slave and master physical layer devices have difficulty canceling the echo and NEXT components. In the 88E1112 device, an advanced DPLL is used to recover and track the clock timing information from the receive signal. This DPLL has very low long-term phase jitter of its own, thereby maximizing the achievable SNR.

2.5.3.8 Link Monitor

The link monitor is responsible for determining if link is established with a link partner. In 10BASE-T mode, link monitor function is performed by detecting the presence of valid link pulses (NLPs) on the MDIP/N pins.

In 100BASE-TX and 1000BASE-T modes, link is established by scrambled idles.

If Force Link Good register 16_0.10 is set high, the link is forced to be good and the link monitor is bypassed for 100BASE-TX and 10BASE-T modes. In the 1000BASE-T mode, register 16_0.10 has no effect.

2.5.3.9 Signal Detection

In 1000BASE-T mode, signal detection is based on whether the local receiver has acquired lock to the incoming data stream.

In 100BASE-TX mode, the signal detection function is based on the receive signal energy detected on the MDIP/N pins that is continuously qualified by the squelch detect circuit, and the local receiver acquiring lock.

2.5.4 Decoder

2.5.4.1 1000BASE-T

In 1000BASE-T mode, the receive idle stream is analyzed so that the scrambler seed, the skew among the 4 pairs, the pair swap order, and the polarity of the pairs can be accounted for. Once calibrated, the 4D PAM 5 symbols are converted to 9-bit symbols that are then descrambled into 8-bit data values. If the descrambler loses lock for any reason, the link is brought down and calibration is restarted after the completion of Auto-Negotiation.

2.5.4.2 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and converted to NRZ. The NRZ stream is descrambled and aligned to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded. The receiver does not attempt to decode the data stream unless the scrambler is locked. The descrambler “locks” to the *scrambler* state after detecting a sufficient number of consecutive idle code-groups. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The descrambler is always forced into the *unlocked* state when a link failure condition is detected, or when insufficient idle symbols are detected.

2.5.4.3 10BASE-T

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ, and then aligned. The alignment is necessary to insure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

2.6 Power Supplies

The 88E1112 devices require 2 power supplies: 2.5V, and 1.2V. However, more power saving can be achieved if more supplies are available.

2.6.1 VDDA, VDDAH

VDDA and VDDAH are used as the 2.5V analog supply.

2.6.2 VDDAL

VDDAL is used as an analog supply and can be set to 1.5V or 2.5V. The 88E1112 device will draw more power at higher voltages.

2.6.3 F_VTT and S_VTT

F_VTT and S_VTT supply the power to the fiber and SGMII MAC Interface transmitters and the termination bias for receivers, respectively. The F_VTT and S_VTT power pin should be left floating if internal regulation is desired. The required voltage will be regulated from the VDDAL supply. SEL_VTT should be set to 0 during hardware configuration if internal regulation is used.

In order to save additional power, the F_VTT and S_VTT power pin can be supplied externally. See Section 2.1.1 and Section 2.1.2 for details.

Note that F_VTT and S_VTT are actually independent supplies and can be set to different voltages.

2.6.4 DVDD

DVDD is used for the digital logic. DVDD is the 1.2V digital supply.

2.6.5 VDDO

VDDO supplies the digital I/O pins. The voltage is 1.5V, or 2.5V.

2.6.6 Power Supply Sequencing

On power-up, no special power supply sequencing is required.

2.7 Power Management

The 88E1112 device supports several advanced power management modes that conserve power.

2.7.1 Low Power Modes

Three low power modes are supported in the 88E1112 device.

- IEEE 22.2.4.1.5 compliant power down
- Energy Detect (Mode 1)
- Energy Detect+^{TM} (Mode 2)

IEEE 22.2.4.1.5 power down compliance allows for the PHY to be placed in a low-power consumption state by register control.

Energy Detect (Mode 1) allows the devices to wake up when energy is detected on the wire.

Energy Detect+^{TM} (Mode 2) is identical to Mode 1 with the additional capability to wake up a link partner. In Mode 2, the 10BASE-T link pulses are sent once every second while listening for energy on the line.

Details of each mode are described below.

2.7.2 Low Power Operating Modes

2.7.2.1 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting register 0_0.11 = 1, 0_1.11 = 1, or 0_2.11 = 1 (Registers 0_0.11, 0_1.11, and 0_2.11 are physically the same register. Setting or resetting any one register will cause the others to also set or reset). In this mode, the PHY does not respond to any SGMII MAC Interface signals except the MDC/MDIO. It also does not respond to any activity on the copper or fiber media.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the media. It can only wake up by setting registers 0_0.11, 0_1.11, or 0_2.11 to 0.

PWRDN Pin Functionality

The PWRDN pin controls registers 0_0.11, 0_1.11, and 0_2.11 which controls the power down of the copper media, fiber media, and SGMII interface respectively.

If the PWRDN pin transitions from 0 to 1 then registers 0_0.11, 0_1.11, and 0_2.11 will be set to 1.

If the PWRDN pin transitions from 1 to 0 then registers 0_0.11, 0_1.11, and 0_2.11 will be set to 0.

The initial value of registers 0_0.11, 0_1.11, and 0_2.11 is set to the value of PWRDN at the deassertion of hardware reset. Registers 0_0.11, 0_1.11, and 0_2.11 can be changed via register writes.

The most recently occurring event will take precedence. Event is defined to be either a software access to the registers or the toggling of the PWRDN pin.

2.7.2.2 Energy Detect Power Down Modes

The 88E1112 device can be placed in energy detect power down modes by selecting either of the two energy detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the CAT 5 cable. The energy detect modes only apply to the copper media. The energy detect modes will not work while Fiber/Copper Auto Select (Section 2.11 "Fiber/Copper Auto-Selection" on page 55) is enabled. The status of the energy detect is reported in register 17_0.4 and the energy detect changes are reported in register 19_0.4.

Energy Detect (Mode 1)

Energy Detect (Mode 1) is entered by setting register 16_0.9:8 to 10.

In Mode 1, only the signal detection circuitry and serial management interface are active. If the PHY detects energy on the line, it starts to Auto-Negotiate sending FLPs for 5 seconds. If at the end of 5 seconds the Auto-Negotiation is not completed, then the PHY stops sending FLPs and goes back to monitoring receive energy. If Auto-Negotiation is completed, then the PHY goes into normal 10/100/1000 Mbps operation. If during normal operation the link is lost, the PHY will re-start Auto-Negotiation. If no energy is detected after 5 seconds, the PHY goes back to monitoring receive energy.

Energy Detect +^{TM} (Mode 2)

Energy Detect (Mode 2) is entered by setting register 16_0.9:8 to 11.

In Mode 2, the PHY sends out a single 10 Mbps NLP (Normal Link Pulse) every one second. Except for this difference, Mode 2 is identical to Mode 1 operation. If the is in Mode 1, it cannot wake up a connected device; therefore, the connected device must be transmitting NLPs, or either device must be woken up through register access. If the is in Mode 2, then it can wake a connected device.

2.7.2.3 Normal 10/100/1000 Mbps Operation

Normal 10/100/1000 Mbps operation can be entered by turning off energy detect mode by setting register 16_0.9:8 to 00.

2.7.3 SGMII MAC Interface Effect on Low Power Modes

In some applications, the SGMII MAC Interface must run continuously regardless of the state of the PHY. Additional power will be required to keep this SGMII MAC Interface running during low power states.

If absolute minimal power consumption is required during the IEEE power down mode or the Energy Detect modes, then register 16_2.3 should be set to 0 to allow the SGMII MAC Interface to power down. Note that for these settings to take effect a software reset must be issued.

2.8 Management Interface

he management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3u clause 22. MDC is the management data clock input and, it can run from DC to a maximum rate of 8.3 MHz. At high MDIO fanouts the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm that pulls the MDIO high during the idle and turnaround.

PHY address is configured during the hardware reset sequence. Refer to “Hardware Configuration” on page 37 for more information on how to configure PHY addresses.

The SEL_TWSI must be set to 0 during hardware configuration to enable the MDC/MDIO functioning.

Typical read and write operations on the management interface are shown in Figure 17 and Figure 18. All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in the Register Description.

Figure 17: Typical MDC/MDIO Read Operation

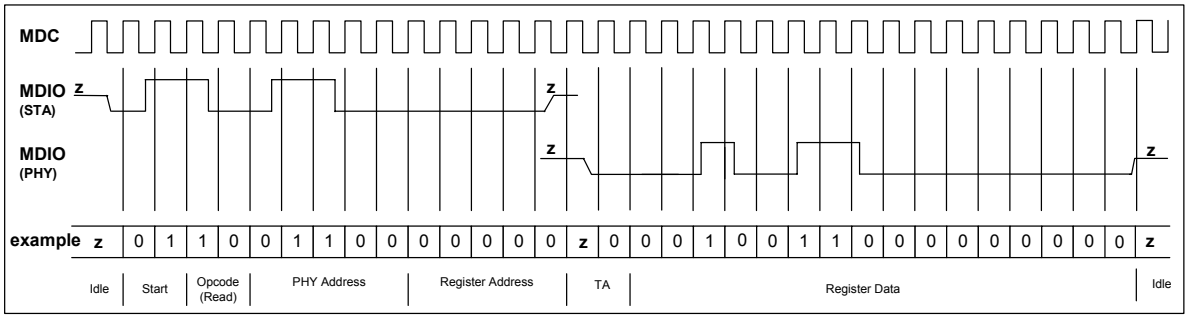


Figure 18: Typical MDC/MDIO Write Operation

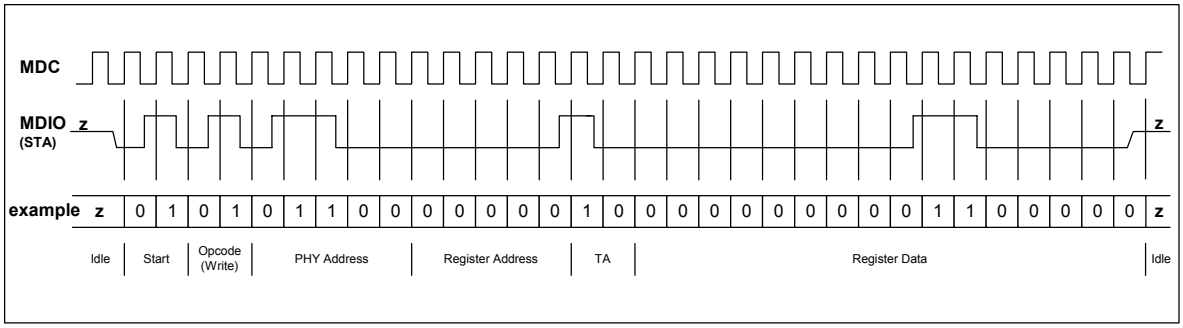


Table 18 is an example of a read operation.

Table 18: Serial Management Interface Protocol

32-Bit Preamble	Start of Frame	OpCode Read = 10 Write = 01	5-Bit PHY Device Address	5-Bit PHY Register Address (MSB)	2-Bit Turn around Read = z0 Write = 10	16-Bit Data Field	Idle
11111111	01	10	01100	00000	z0	0001001100000000	11111111

2.8.1 Extended Register Access

The IEEE defines only 32 registers address space for the PHY. In order to extend the number of registers address space available a paging mechanism is used. For register address 0 to 21, and 23 to 28 register 22 bits 7 to 0 are used to specify the page. For registers 30 and 31 register 29 bits 5:0 are used to specify the page. There is no paging for registers 22 and 29.

In this document, The short hand used to specify the registers take the form register_page.bit:bit, register_page.bit, register.bit:bit, or register.bit.

For example:

Register 0 page 1 bits 5 to 2 is specified as 0_1.5:2.

Register 0 page 1 bit 5 is specified as 0_1.5.

Register 2 bits 3 to 0 is specified as 2.3:0.

Note that in this context the setting of the page register (register 22) has no effect.

Register 2 bit 3 is specified as 2.3.

Note that in order for the paging mechanism to work correctly register 22.15 must be set to 0 to disable the automatic medium register selection.

2.8.2 Preamble Suppression

The 88E1112 device is permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

2.9 Two-Wire Serial Interface

The 88E1112 device supports Two-wire Serial Interface (TWSI). The TWSI operates with a serial data line (SSDA) and a serial clock line (SSCL). The SEL_TWSI must be set to 1 during hardware configuration to enable the Two Wire Serial Interface functionality. In this mode the SSDA uses the MDIO pin and the SSCL uses the MDC pin. Note that this Two-Wire Serial Interface is a slave interface and is separate and distinct from the two-wire serial interface used to interface to the EEPROM (Section 2.19 "EEPROM Interface" on page 65).

For the TWSI device address, the lower 5 bits (PHYADR[4:0]), are latched during hardware reset, and the device address bits ([6:5]) are fixed at '10'. The SSDA is a bi-directional line, while the SSCL line is not. SSDA requires a 1.5 kΩ pull-up resistor. The 88E1112 device operates as the Slave port of the bus interface.

The 88E1112 device will be available for read/write operations 5 ms after hardware reset.

Table 19 indicates the pin mapping of the 88E1112 device to the TWSI.

Table 19: 88E1112 to Two-wire Serial Interface Bus Signal Mapping

88E1112 Device Pins	100/400 Kbps Mode	Description
MDIO	SSDA	Serial data line
MDC	SSCL	Serial clock line

The 88E1112 device TWSI features are:

- 7-bit device address/8-bit data transfers
- 100 Kbps mode
- 400 Kbps mode

Multiple devices using the TWSI can share and lump up the MDC and MDIO lines, and are pulled up with a resistor ranging from 4.5 kohm to 10 kohm.

2.9.1 Bus Operation

The Master generates one clock pulse for each data bit transferred. The high or low state of the data line can only change when the clock signal on the SSCL line is low. A high to low transition on the SSDA line while SSCL is high defines a Start. A low to high transition on the SSDA line while the SSCL is high defines a Stop. Start (S), Repeated Start (Sr), and Stop (P) conditions are always generated by the Master. Acknowledge (A) and Not Acknowledge (A) can be generated by either the Slave or Master.

The Master continuously monitors for Start and Stop conditions. Whenever a Stop is detected, the 88E1112 device goes into standby mode, and the current operation is cancelled. The Slave recovers from this error condition, and waits for the next transfer to begin.

Data transfer with Acknowledge is always obligatory. The receiver must pull down the SSDA line during the Acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

If the Slave does not Acknowledge the device address, but some time later in the transfer cannot receive any more data bytes, the Master must abort the transfer. This is indicated by the Slave generating the Not Acknowledge on the first byte to follow. The Slave device then leaves the data line high, and the Master must generate a Stop or a Repeated Start condition. When the Slave is transmitting data on the bus and the Master responds with a Not Acknowledge, the Slave must receive a Stop or a Repeated Start condition. If neither is received, it is an error condition. The Slave recovers from this error condition and waits for the next transfer to begin.

The bus interface is also active in power down mode. (See "Power Management" on page 43 for power down mode details.) Whenever the Slave is addressed by the Master, the 88E1112 device comes out of power down mode if it is in power down mode. Read and Write operations are detailed in the following section.

2.9.2 Read and Write Operations

Write operations require an 8-bit Slave address followed by the register address and Acknowledgement. The Slave address is 7 bits long followed by an eighth bit. The first bit of a data transfer is the most significant bit (MSb). The eighth bit is the least significant bit (LSb), which is a direction bit (R/W) - Read = 1, Write = 0). Read operations are executed the same way as Write operations with the exception that the R/W bit is set to one.

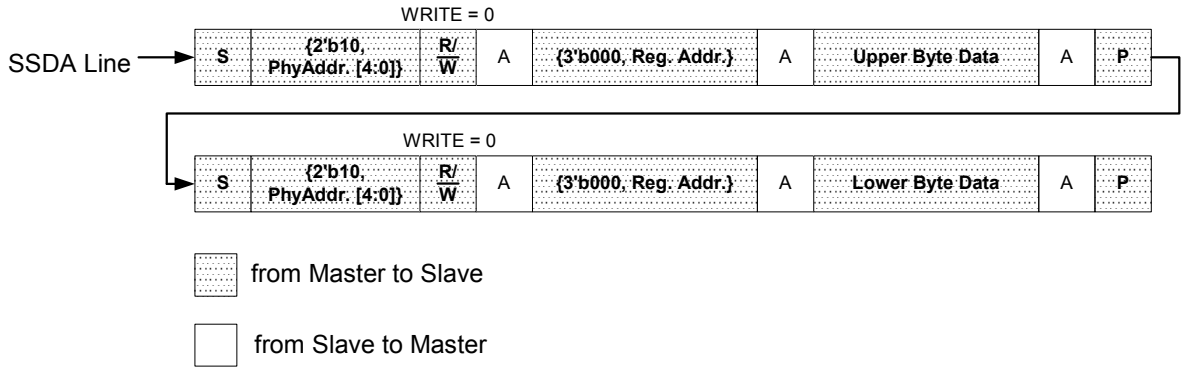
A complete byte write operation includes the upper and lower bytes. The upper byte is written first, followed by the lower byte.

The register address counter maintains the last address accessed during the last read or write operation, incremented by one. The address remains valid between operations as long as chip power is maintained. The register limit is 32 registers. Once the counter reaches the lower byte of register 31, it rolls over to the upper byte of register 0.

2.9.2.1 Random Write

For random writes, both the upper byte and lower byte must be written to the Slave before the data is written to the addressed register.

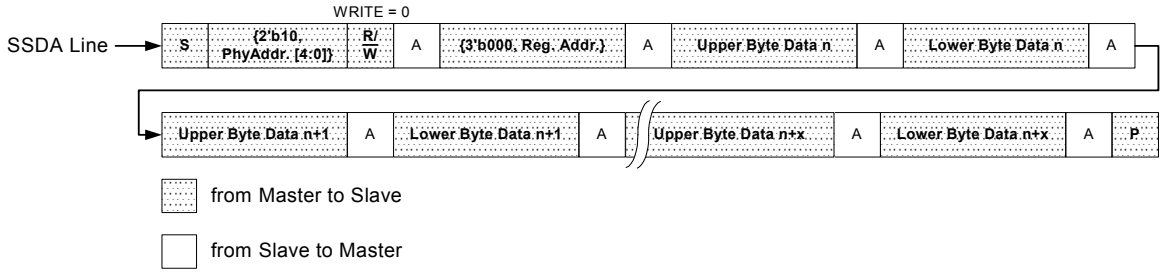
Figure 19: Random Write Operation



2.9.2.2 Sequential Write

A sequential write is started by a random address write. After the register address is received by the Slave, the Slave responds with an Acknowledge. The Slave generates an Acknowledge as long as the Master does not generate a Stop. In sequential write, only the even transfer of bytes is accepted by the 88E1112 device. If the last byte is odd, it is held internally by the Slave, but is not written to the Slave register.

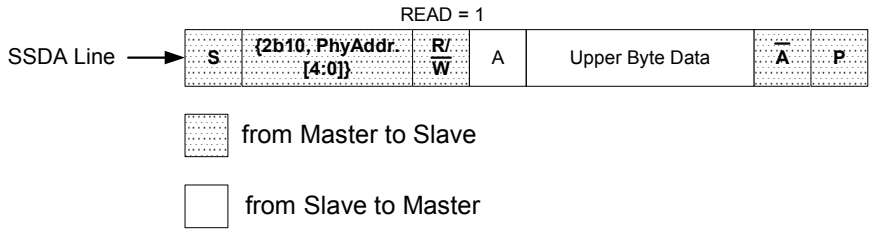
Figure 20: Sequential Write Operation



2.9.2.3 Current Address Read

A current address read is used to read the data at the current register address. A Start begins a current address read and resets the Slave to synchronize with the Master.

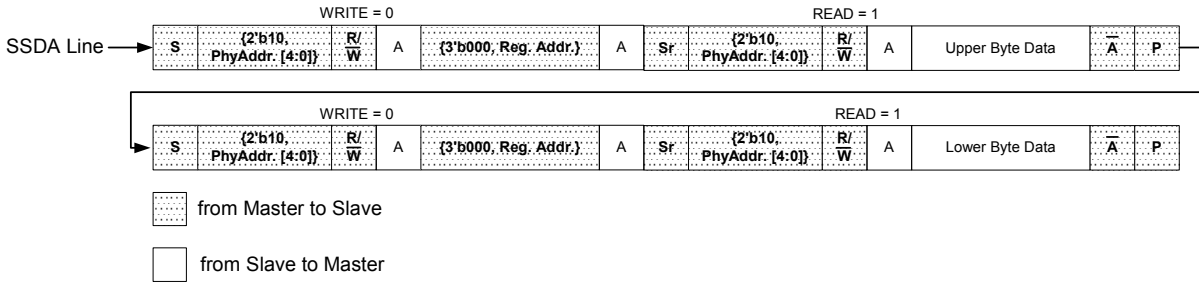
Figure 21: Current Address Read



2.9.2.4 Random Read

A random read is used to access any particular register. A “dummy” byte write is required to load in the data word address. When the device address and the data word address are Acknowledged, another Start condition must be generated. Figure 22 is an example of a random read.

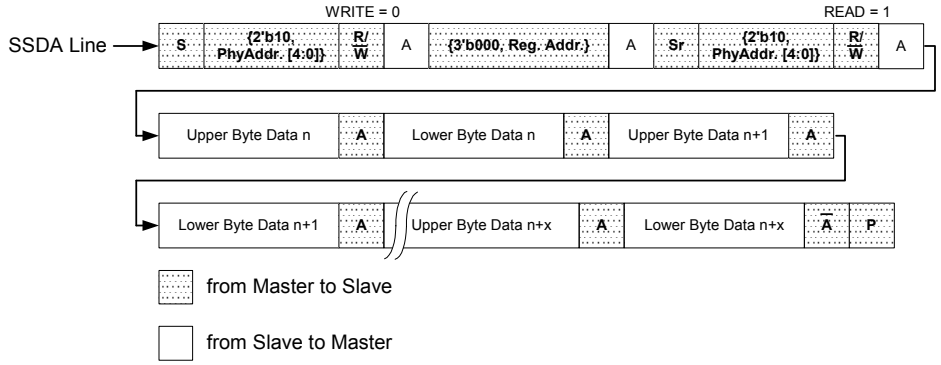
Figure 22: Random Read Operation



2.9.2.5 Sequential Read

A sequential read is used to read particular registers in their address order. A sequential read is initiated by either a current or random address read. After the Master receives the register data, it responds with an Acknowledge. As long as the Slave receives an Acknowledge, register data continues to be read incrementally. The sequential read operation is stopped when the Master does not respond with a zero, but does generate a Stop condition. Figure 23 is an example of a sequential read started by a random read.

Figure 23: Sequential Read Operation



2.10 Auto-Negotiation

The 88E1112 device supports 6 types of Auto-Negotiation.

- 10/100/1000BASE-T Copper Auto-Negotiation. (IEEE 802.3 Clauses 28 and 40)
- 1000BASE-X Auto-Negotiation (IEEE 802.3 Clause 37)
- SGMII Auto-Negotiation MAC Interface (Cisco specification)
- SGMII Auto-Negotiation Media Interface (Cisco specification)
- GBIC Mode Auto-Negotiation (Marvell patent)
- Auto Media Select Auto-Negotiation

Auto-Negotiation provides a mechanism for transferring information from the local station to the link partner to establish speed, duplex, and Master/Slave preference during a link session.

Auto-Negotiation for 1000BASE-X supports 1000 Mbps operation only.

Auto-Negotiation is initiated upon any of the following conditions:

- Power up reset
- Hardware reset
- Software reset (Register 0_0.15, 0_1.15, or 0_2.15)
- Restart Auto-Negotiation (Register 0_0.9 or 0_1.9)
- Transition from power down to power up (Register 0_0.11, 0_1.11, or 0_2.11)
- The link goes down

The option to select 10/100/1000BASE-T, 1000BASE-X, or SGMII Auto-Negotiation is determined by the mode that the device is in.

The following sections describe each of the Auto-Negotiation modes in detail.

2.10.1 10/100/1000BASE-T Auto-Negotiation

The 10/100/1000BASE-T Auto-Negotiation (AN) is based on Clause 28 and 40 of the IEEE802.3 specification. It is used to negotiate speed, duplex, and flow control over CAT5 UTP cable. Once Auto-Negotiation is initiated, the device determines whether or not the remote device has Auto-Negotiation capability. If the remote device has Auto-Negotiation capability then speed and duplex with which to operate are negotiated.

If the remote device does not have Auto-Negotiation capability, the device uses the parallel detect function to determine the speed of the remote device for 100BASE-TX and 10BASE-T modes. If link is established based on the parallel detect function, then it is required to establish link at half-duplex mode only. Refer to IEEE 802.3 clauses 28 and 40 for a full description of Auto-Negotiation.

After hardware reset, 10/100/1000BASE-T Auto-Negotiation can be enabled and disabled via Register 0_0.12. Auto MDI/MDIX and Auto-Negotiation may be disabled and enabled independently. When Auto-Negotiation is disabled, the speed and duplex can be set via registers 0_0.13, 0_0.6, and 0_0.8 respectively. When Auto-Negotiation is enabled the abilities that are advertised can be changed via registers 4_0 and 9_0.

Changes to registers 0_0.12, 0_0.13, 0_0.6 and 0_0.8 do not take effect unless one of the following takes place:

- Software reset (registers 0_0.15, 0_1.15, or 0_2.15)
- Restart Auto-Negotiation (register 0_0.9)
- Transition from power down to power up (register 0_0.11, 0_1.11, or 0_2.11)
- The copper link goes down

To enable or disable Auto-Negotiation, Register 0_0.12 should be changed simultaneously with either register 0_0.15 or 0_0.9. For example, to disable Auto-Negotiation and force 10BASE-T half-duplex mode, register 0_0 should be written with 0x8000.

Registers 4_0 and 9_0 are internally latched once every time the Auto-Negotiation enters the Ability Detect state in the arbitration state machine. Hence, a write into Register 4_0 or 9_0 has no effect once the PHY begins to transmit Fast Link Pulses (FLPs).This guarantees that sequences of FLPs transmitted are consistent with one another.

Register 7_0 is treated in a similar way as registers 4_0 and 9_0 during additional next page exchanges.

If 1000BASE-T mode is advertised, then the device automatically sends the appropriate next pages to advertise the capability and negotiate master/slave mode of operation. If the user does not wish to transmit additional next pages, then the next page bit (Register 4_0.15) can be set to zero, and the user needs to take no further action.

If next pages in addition to the ones required for 1000BASE-T are needed, then the user can set register 4_0.15 to one, and send and receive additional next pages via registers 7_0 and 8_0, respectively. The 88E1112 device stores the previous results from register 8_0 in internal registers, so that new next pages can overwrite register 8_0.

Note that 1000BASE-T next page exchanges are automatically handled by the 88E1112 device without user intervention, regardless of whether or not additional next pages are sent.

Once the 88E1112 device completes Auto-Negotiation, it updates the various status in registers 1_0, 5_0, 6_0, and 10_0. Speed, duplex, page received, and Auto-Negotiation completed status are also available in registers 17_0 and 19_0. See the “Register Description” on page 80.

2.10.2 1000BASE-X Auto-Negotiation

1000BASE-X Auto-Negotiation is defined in Clause 37 of the IEEE802.3 specification. It is used to auto-negotiate duplex and flow control over fiber cable. Registers 0_1, 4_1, 5_1, 6_1, 7_1, 8_1, and 17_1 are used to enable AN, advertise capabilities, determine link partner’s capabilities, show AN status, and show the duplex mode of operation respectively.

After hardware reset, 1000BASE-X Auto-Negotiation can be enabled and disabled via register 0_1.12. When Auto-Negotiation is disabled, the duplex can be set via register 0_1.8. When Auto-Negotiation is enabled, the abilities that are advertised can be changes via register 4_1.

Auto-Negotiation can be also be configured via registers 0_1 and 4_1. Changes to registers 0_1.12 and 0_1.8 do not take effect unless one of the following takes place:

- Software reset (register 0_0.15, 0_1.15, or 0_2.15)
- Restart Auto-Negotiation register 0_1.9)
- Transition from power down to power up (registers 0_0.11, 0_1.11, or 0_2.11)
- The fiber link goes down

To enable or disable Auto-Negotiation, register 0_1.12 should be changed simultaneously with either register 0_1.15 or 0_1.9.

Register 4_1 is internally latched once every time the Auto-Negotiation enter the Ability Detect state in the arbitration state machine. Hence, a write into register 4_1 has no effect once the 88E1112 device begins to transmit configuration order sets. This guarantees that sequences of ordered sets are consistent with one another.

Register 7_1 is treated in a similar way as register 4_1 during additional next page exchanges.

If next pages in addition to the ones required for 1000BASE-X are needed, then the user can set register 4_1.15 to 1, and send and receive additional next pages via registers 7_1 and 8_1 respectively. The 88E1112 device stores the previous results from register 8_1 in internal registers, so that new next pages can overwrite register 8_1.

Note that 1000BASE-X next page exchanges are automatically handled by the 88E1112 device without user intervention, regardless of whether or not additional next pages are sent.

Once the 88E1112 device completes Auto-Negotiation, it updates the various status in register 1_1,5_1,6_1. Speed, duplex, page received, and Auto-Negotiation completed status are also available in register 17_1 and 19_1. See the “Register Description” on page 80.

2.10.3 SGMII Auto-Negotiation

SGMII Auto-Negotiation differs from copper or 1000BASE-X Auto-Negotiation. For the latter two, two link partners advertise their capabilities and decide on the mode of operation. They are peers with equal roles in the negotiation process.

During SGMII Auto-Negotiation, the PHY tells the MAC the link speed and duplex status. It is not a real Auto-Negotiation, the MAC takes the information given by the PHY to configure itself. Nothing is negotiated.

The 88E1112 device has 2 SGMII interfaces. The SGMII MAC Interface acts like a PHY telling the MAC the status. The SGMII Media Interface acts like a MAC expecting whatever is connected to it to send link speed and duplex status (e.g., An SFP Module with an SGMII interface. See page 4.

2.10.3.1 SGMII MAC Interface Auto-Negotiation

SGMII is a de facto standard designed by Cisco. SGMII uses 1000BASE-X coding to send data as well as Auto-Negotiation information between the PHY and the MAC. However, the contents of the SGMII Auto-Negotiation are different than the 1000BASE-X Auto-Negotiation. See the “Cisco SGMII Specification” and the “MAC Interfaces and Auto-Negotiation” application note for further details.

The 88E1112 device supports SGMII MAC Interface with and without Auto-Negotiation. Auto-Negotiation can be enabled or disabled by writing to Register 0_2.12 followed by a soft reset. If SGMII MAC Interface Auto-Negotiation is disabled, the MAC interface link, speed, and duplex status (determined by the media side) cannot be conveyed to the MAC from the PHY. The user must program the MAC with this information in some other way (e.g., by reading PHY registers for link, speed, and duplex status). However, the operational speed of the SGMII MAC Interface will follow the speed of the media. (See Table 11 on page 22). Regardless of whether the Auto-Negotiation is enabled or disabled. If there is no link on the media then the speed of operation on the MAC Interface can be set by programming register 0_2.6 and 0_2.13 regardless of whether Auto-Negotiation is enabled or disabled.

Flow control Enhancement to SGMII Auto-Negotiation

During standard SGMII Auto-Negotiation the PHY passes the link, speed, and duplex information to the MAC. The flow control information is not communicated. Typically the MAC will have to read the registers of the PHY to find out the flow control capability of the link partner. The 88E1112 device has added in-line flow control information by using some of the reserved bits of the Auto-Negotiation base page as defined by the SGMII specification. This feature is optional. The user can select the standard SGMII Auto-Negotiation or the enhanced mode as described in Table 21. Table 20 shows the bit definitions for the enhanced mode.

Bit 9 corresponds to register 17_0.9 and bit 8 corresponds to register 17_0.8.

Register 16_2.2 will enable this feature (Table 21). 0 = set bits 9:7 always to 000, 1 = set bits 9:7 according to Table 20. The default is disabled.

Table 20: Enhanced SGMII PHY Status

Bit Number	TX_CONFIG_REG[15:0]
15	1 = Link Up, 0 = Link Down
14	Acknowledge
13	0 = Reserved

Table 20: Enhanced SGMII PHY Status

Bit Number	TX_CONFIG_REG[15:0]
12	0 = Half-Duplex 1 = Full-Duplex
11:10	00 = 10BASE-T 01 = 100BASE-TX, 100BASE-FX 10 = 1000BASE-T, 1000BASE-X 11 = Reserved
9	0 = Disabled 1 = Transmit pause enabled
8	0 = Disabled 1 = Received pause enabled
7	0 - 10/100/1000BASE-T 1 = 100BASE-FX/1000BASE-X
6	0 - Reserved
0	Always 1

Table 21: MAC Specific Control Register 1

Register	Function	Setting	Mode	HW Rst	SW Rst
16_2.2	Enhanced SGMII	1 = Pass flow control bits through SGMII Auto-Negotiation 0 = Do not pass flow control bits through SGMII Auto-Negotiation	R/W	0	Update

2.10.3.2 SGMII Media Interface Auto-Negotiation

SGMII is a de facto standard designed by Cisco. SGMII uses 1000BASE-X coding to send data as well as Auto-Negotiation information between the 88E1112 device and the SFP module. However, the contents of the SGMII Auto-Negotiation are different than the 1000BASE-X Auto-Negotiation. See the “CISCO SGMII Specification” and the “MAC Interfaces and Auto-Negotiation” application note for further details.

The 88E1112 device supports SGMII Media Interface with and without Auto-Negotiation. Auto-Negotiation can be enabled or disabled by writing to Register 0_1.12 followed by a soft reset. If SGMII Media Interface Auto-Negotiation is disabled, the SGMII Media Interface operates at the speed defined by register 0_1.6 and 0_1.13.

Register 1_1, 4_1, 6_1, 7_1, and 8_1 has no meaning in SGMII Media Interface mode.

Register 5_1 reflects the SGMII Auto-Negotiation exchange between the 88E1112 device and the SFP module.

2.10.4 GBIC Mode Auto-Negotiation

GBIC Auto-Negotiation is a Marvell® proprietary feature which translates 1000BASE-X Auto-Negotiation from the MAC side to and from 10/100/1000BASE-T Auto-Negotiation on the copper side. If GBIC mode is selected, Auto-

Negotiation can be enabled and disabled by writing to register 0_2.12 followed by a soft reset. See Application Note GBIC/SFP Applications for details.

2.10.5 Auto-Media Detect Auto-Negotiation

The 88E1112 device supports two separate media interfaces: fiber interface and copper interface. It can monitor both interfaces simultaneously and establish link with whatever media is connected. In this mode of operation the 88E1112 device simultaneously carries on 10/100/1000BASE-T Auto-Negotiation on the copper interface and 1000BASE-X or SGMII Auto-Negotiation on the Fiber interface depending on the mode of operation selected for the Fiber interface. (If register 16_2.9:7=011 then 1000BASE-X is selected for the Fiber interface while if 16_2.9:7=010 then SGMII is selected for the Fiber interface.) The first media to complete Auto-Negotiation and establish link will be enabled and the other media will be powered down to save power. There is an option to over write this and give preference to one media over another. See Section 2.11.1 for details.

Since the copper Auto-Negotiation registers are in page 0 and the fiber Auto-Negotiation register are in page 1 there should be no confusion as to which media register is being accessed.

2.10.6 Serial Interface Auto-Negotiation Bypass Mode

The IEEE standard Auto-Negotiation state machine, per the 802.3X Clause 37 1000BASE-X, requires that both link partners support Auto-Negotiation before link is established. If one link partner implements the Auto-Negotiation function and the other does not, two-way communication is not possible unless Auto-Negotiation is manually disabled and both sides are configured to work in the same operational modes. To solve this problem, the 88E1112 device implements the Serial Interface Auto-Negotiation Bypass Mode.

Register 26_1.15 = 1 enables the bypass on the 1000BASE-X or SGMII Media Interface

Register 26_2.15 = 1 enables the bypass on the SGMII MAC Interface or GBIC.

If link is established due to bypassing Auto-Negotiation, then the duplex mode of operation will be determined by what is advertised in the Auto-Neg ability register. If full-duplex is advertised and Auto-Neg was bypassed, then link will be established in full duplex mode. Else, the link will be established in half-duplex mode. Care must be taken to avoid establishing link with both link partners having different duplex mode of operation.

2.11 Fiber/Copper Auto-Selection

The 88E1112 device has a patented feature to automatically detect and switch between fiber and copper cable connections. The auto-selection operates in one of two modes: Copper /1000BASE-X and Copper/ SGMII Media Interface.

The 88E1112 device monitors the signals of the F_INP/N and SIGDET and the MDIP/N[3:0] lines. If a fiber optic cable is plugged in, the 88E1112 device will adjust itself to be in fiber mode. If an RJ-45 cable is plugged in, the 88E1112 device will adjust itself to be in copper mode. If both cables are connected then the first media to establish link will be enabled. The media which is not enabled will turn off to save power. If the link on the first media is lost, then the inactive media will be powered up, and both media will once again start searching for link.

It is important that the SIGDET pin not be permanently tied to the active state as this signal is used to control whether the SERDES is powered up or down. The SIGDET should be tied to the signal detect of the optics module or the LOS signal of the SFP module. The active polarity of the SIGDET pin can be programmed via register 16_1.9.

2.11.1 Preferred Media

The 88E1112 device can be programmed to give one media priority over the other. In other words if the non-preferred media establishes link first and subsequently energy is detected on the preferred media, the PHY will drop link on the non-preferred media for 4 seconds and give the preferred media a chance to establish link. Register 16_2.11:10 selects the preferred media.

- 00 = Link with the first media to establish link
- 01 = Prefer fiber media
- 10 = Prefer copper media

The determination of when to switch from one media to another can also be managed under software instead of being done automatically. Register 16_2.11:10 can be set to 00 to not give any media any preference. The software then polls register 17_0.4 and 17_1.4 to see if energy is detected on the copper or fiber media respectively. If link is already up for one media but the second media indicate energy is being detected via register 17_0.4 or 17_1.4 then the management software has the option of setting 16_2.11:10 to prefer the second media when it is ready. Once link is established on the second media register 16_2.11:10 can then be set back to 00.

Registers 19_0.4 and 19_1.4 are sticky bits that report when the energy detect on the copper or fiber media respectively has changed.

If the Prefer Fiber Media option is selected and there is fiber link, then the copper energy will not the monitored since the port already has the preferred link. Register 17_0.4=1 indicates that there is no copper energy. Prefer copper operation is different. Since fiber energy is indicated to the 88E1112 by the signal detect input pin, it is simple for the 88E1112 to indicate that fiber energy is detected. So 17_1.4=0 indicates fiber energy detected in this case.

2.11.2 Definition of link in SGMII Media Interface in the context of auto media selection

In the conventional copper/1000BASE-X definition of link, 1000BASE-X link is defined to be auto-negotiation complete if 1000BASE-X auto-negotiation is turned on, or the acquisition of comma if 1000BASE-X auto-negotiation is off. No link is defined to be when the SIGDET is deasserted or the comma is not seen for some amount of time, or when auto-negotiation restarts.

In the copper/SGMII Media Interface definition of link, the SGMII Media Interface link is up only if bit 15 of the SGMII auto-negotiation indicates that link is up. Completing auto-negotiation is not sufficient to bring the link up. With SGMII auto-negotiation turned off or in the link down case the link definition is identical to the 1000BASE-X case.

2.11.3 Notes on Determining which Media Linked Up

Since there are two sets of IEEE registers (one for copper and the other for fiber) the software needs to be aware of register 22.7:0 so that the correct set of registers are selected. In general the sequence is as follows.

1. Set the auto-negotiation registers of the copper medium. (This step may not be necessary if the hardware defaults are acceptable.)
2. Set the auto-negotiation registers of the fiber medium. (This step may not be necessary if the hardware defaults are acceptable.)
3. Poll for link status.Go to step 4 if there is link.
4. Once there is link determine whether the link is copper or fiber medium.
5. Look at the auto-negotiation results for the medium that established link.
6. Poll for link status. If link status goes down then go back to step 3.

There are 2 general methods for polling.

2.11.3.1 Polling Method 1

Method 1 is the preferred method of polling since there is less change of making a mistake when implementing this method.

1. Write register 22.15:0 to 0000 to point to the copper medium.Write the appropriate auto-negotiation registers to advertise the desired capabilities.
2. Write register 22.15:0 to 0001 to point to the fiber medium. Write the appropriate auto-negotiation registers to advertise the desired capabilities.
3. If one medium is preferred over the other then write register 22.15:0 to 0002 to point to the MAC registers. Set 16_2.11:10 to the preferred media.
4. Write 0_0.15, 0_1.15, or 0_2.15 to 1 to issue software reset. This causes the auto-negotiation settings to take effect.
5. Write register 22.15:0 to 0000 to point to the copper medium. Read the copper link status register 1_0.2. Write register 22.15:0 to 0001 to point to the fiber medium. Read the fiber link status register 1_1.2. Keep doing this until one of the link comes up. It should be clear which link goes up. When link is up go to the next step. An alternative to reading 1_0.2 and 1_1.2 is to read 17_0.3 or 17_1.3. 17_0.3 and 17_1.3 are the same physical register so it does not matter which one is read. The register will be set to 1 when any link is established. Register 17_0.7 or 17_1.7 will indicate whether the link is copper or fiber. Again it does not matter which one is read since 17_0.7 and 17_1.7 are the same physical register. (Note that the other bits in registers 17_0 and 17_1 are not physically the same register.)
6. Once the link is up set register 22 to 0000 if the copper medium is up, or 0001 if the fiber medium is up. Read the auto-negotiation registers for the auto-negotiation status if needed. Alternatively register 17_0 or 17_1 will summarize the status including speed, duplex, and pause resolution bits.
7. Poll register 1_0.2 or 1_1.2 depending on copper or fiber link. If link goes down go back to step 5.

2.11.3.2 Polling Method 2

Method 2 is available for simple unmanaged systems that may not be aware of the proprietary registers (i.e. register 22 and 17_0 and 17_1.) It is assumed that the default auto-negotiation settings in the PHY are acceptable for the unmanaged system.

When the PHY is in hardware reset register 22.15 defaults to a 1. With this bit set to 1, register 22.7:0 will automatically be set to 0 to point to page 0 if copper link is established, and set to 1 to point to page 1 if fiber link is established. This way when the unmanaged system reads the link status bit in register 1 bit 2 the correct page is automatically set.

Method 2 is not the preferred method to do things since it is very limited.

2.12 Downshift Feature

Without the downshift feature enabled, connecting between two Gigabit link partners requires a four-pair RJ-45 cable to establish 10, 100, or 1000 Mbps link. However, there are existing cables that have only two-pairs, which are used to connect 10 Mbps and 100 Mbps Ethernet PHYs. With the availability of only pairs 1, 2 and 3,6, Gigabit link partners can Auto-Negotiate to 1000 Mbps, but fail to link. The Gigabit PHY will repeatedly go through the Auto-Negotiation but fail 1000 Mbps link and never try to link at 10 Mbps or 100 Mbps.

With the Marvell® downshift feature enabled, the 88E1112 device is able to Auto-Negotiate with another Gigabit link partner using cable pairs 1,2 and 3,6 to downshift and link at 10 Mbps or 100 Mbps, whichever is the next highest advertised speed common between the two Gigabit PHYs.

In the case of a three pair cable (additional pair 4,5 or 7,8 - but not both) the same downshift function for two-pair cables applies.

By default, the downshift feature is turned off. Refer to register 16_0.14:11 which describe how to enable this feature and how to control the downshift algorithm parameters.

To enable the downshift feature, the following registers must be set:

- Register 16_0.11 = 1 - enables downshift
- Register 16_0.14:12 - sets the number of link attempts before downshifting

2.13 Virtual Cable Tester™ (VCT™)

The 88E1112 device Virtual Cable Tester™ feature uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics.

The 88E1112 device transmits a signal of known amplitude (+1V) down each of the four pairs of an attached cable. It will conduct the cable diagnostic test on each pair, testing the MDIP/N[0], MDIP/N[1], MDIP/N[2], and MDIP/N[3] pairs sequentially. The transmitted signal will continue down the cable until it reflects off of a cable imperfection. The magnitude of the reflection and the time it takes for the reflection to come back on MDIP/N[0], MDIP/N[1], MDIP/N[2], and MDIP/N[3] are shown in register 16_5.12:8, 17_5.12:8, 18_5.12:8, and 19_5.12:8 and 16_5.7:0, 17_5.7:0, 18_5.7:0, and 19_5.7:0 respectively.

Using the information from registers 16_5, 17_5, 18_5, and 19_5 the distance to the problem location and the type of problem can be determined. For example, the time it takes for the reflection to come back, can be converted to distance using Figure 24. The polarity and magnitude of the reflection together with the distance will indicate the type of discontinuity. For example, a +1V reflection will indicate an open close to the PHY and a -1V reflection will indicate a short close to the PHY.

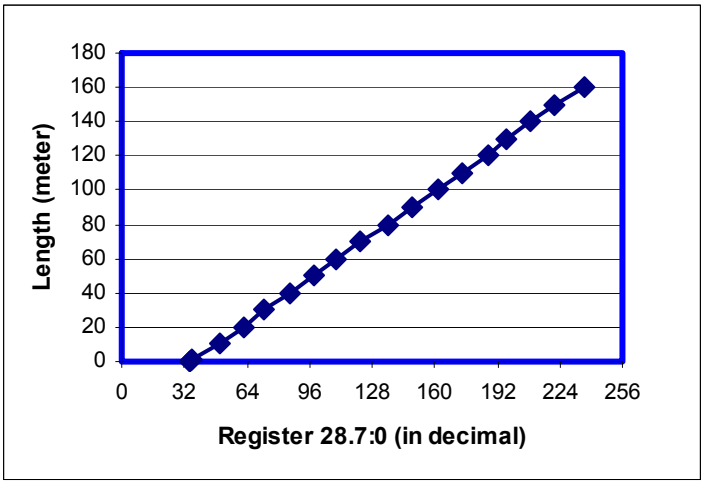
If the cable is properly terminated and there are no discontinuities, then there will be no reflections. If there are no reflections cable length can not be determined by TDR methods. Instead, if there is good link then DSP algorithms are used to determine cable length as indicated by register 26_5.2:0.

When the cable diagnostic feature is activated by setting Register 16_5.15=1, a pre-determined amount of time elapses before a test pulse is transmitted. This is to ensure that the link partner loses link, so that it stops sending 1000BASE-T or 100BASE-TX idles or 10 Mbit data packets. If it is known before hand that there is no active link partner, the pre-determined wait time can be skipped by setting register 17_5.15 = 1.

The TDR test can be performed either when there is no link partner or when the link partner is Auto-Negotiating or sending 10 Mbit idle link pulses. If the 88E1112 device receives a continuous signal for 125 ms, it will declare test failure because it cannot start the TDR test. In the test fail case, the received data is not valid. The results of the test are also summarized in register bit 16_5.14:13, 17_5.14:13, 18_5.14:13, and 19_5.14:13.

- 11 = Test fail (The TDR test could not be run for reasons explained above)
- 00 = valid test, normal cable (no short or open in cable)
- 10 = valid test, open in cable (Impedance > 333 ohms)
- 01 = valid test, short in cable (Impedance < 33 ohms)

Figure 24: Cable Fault Distance Trend Line



Register 20_5 reports the pair skew of each pair of wire relative to each other.

Register 21_5.3:0 reports the polarity of each pair of wire.

Register 21_5.5:4 reports the crossover status

Register 20_5 and 21_5 are not valid unless register 21_5.6 is set to 1.

2.14 Data Terminal Equipment (DTE) Detect

The 88E1112 device supports the Data Terminal Equipment (DTE) power function. The DTE power function is used to detect if a link partner requires power supplied by the device.

The DTE power function can be enabled by writing to register 26_0.8. When DTE is enabled, the device will first monitor for any activity transmitted by the link partner. If the link partner is active, then the link partner has power and power from the device is not required. If there is no activity coming from the link partner, DTE power engages, and special pulses are sent to detect if the link partner requires DTE power. If the link partner has a low pass filter (or similar fixture) installed, the link partner will be detected as requiring DTE power.

The DTE power status register (Register 17_0.2) immediately comes up as soon as link partner is detected as a device requiring DTE power. Register 19_0.2 is a bit that reports the DTE power status has changed states.

If a link partner that requires DTE power is unplugged, the DTE power status (register 17_0.2) will drop after a user controlled delay (default is 20 seconds - Register 26_0.7:4) to avoid DTE power status register drop during the link partner powering up (for most applications), since the low pass filter (or similar fixture) is removed during power up. If DTE power status drop is desired to be reported immediately, write register 26_0.7:4 to 4'b0000.

A detailed description of the register bits used for DTE power detection for the devices are shown in Table 22.

Table 22: Registers for DTE Power

Register	Description
26_0.8 - Enable power over Ethernet detection	1 = Enable DTE detect 0 = Disable DTE detect A soft reset is required to enable this feature HW reset: 0x0 SW reset: Update
17_0.2 - Power over Ethernet detection status	1 = Need power 0 = Do not need power HW reset: 0 SW reset: 0
19_0.2 - Power over Ethernet detection state changed	1 = Changed 0 = No change HW reset: 0 SW reset: 0
26_0.7:4 - DTE detect status drop	Once the PHY no longer detects that the link partner filter, the PHY will wait a period of time before clearing the power over Ethernet detection status bit (17_0.2). The wait time is 5 seconds multiplied by the value of these bits. Example: (5 * 0x4 = 20 seconds) Default at HW reset: 0x4 At SW reset: retain

2.15 CRC Error Counter and Packet Counter

The CRC counter and packet counters, normally found in MACs, are available in the 88E1112 device. The error counter and packet counter features are enabled through register writes and each counter is stored in eight register bits. The counting is done at the output of the receive FIFO.

2.15.1 Enabling The CRC Error Counter and Packet Counter

To enable both counters to count, set 16_6.4 to 1.

To disable and clear both counters, set 16_6.4 to 0.

To read the CRC counter and packet counter, read register 17_6.

17_6.15:8 (Packet count is stored in these bits)

17_6.7:0 (CRC error count is stored in these bits)

The counter does not clear on a read command. To clear the CRC error counter, disable and enable the counters.

The packet counter should be read after the packet transfers are completed.

2.16 Packet Generator

The 88E1112 device contains a very simple packet generator. When enabled the input into the SGMII MAC Interface is ignored. Link should be established first prior to enabling the packet generator. The generator will generate packets at the speed of the established link.

Once enabled, fixed length packet of 64 or 1518 byte frame (including CRC) will be transmitted continuously separated by 12 bytes of IPG. The preamble length will be 8 bytes. The payload of the frame is either a fixed 5A, A5, 5A, A5 pattern or a pseudo random pattern. A correct IEEE CRC is appended to the end of the frame. An error packet can also be generated.

The registers are as follows:

16_6.3 Packet generation enable. 0 = normal operation, 1 = enable internal packet generator

16_6.2 Payload type. 0 = pseudo random, 1 = fixed 5A, A5, 5A, A5, ...

16_6.1 Packet length. 0 = 64 bytes, 1 = 1518 bytes

16_6.0 Error packet. 0 = Good CRC, 1 = Symbol error and corrupt CRC.

2.17 MDI/MDIX Crossover

The 88E1112 device automatically determines whether or not it needs to cross over between pairs as shown in Table 23 so that an external crossover cable is not required. If the 88E1112 device interoperates with a device that cannot automatically correct for crossover, the 88E1112 device makes the necessary adjustment prior to commencing Auto-Negotiation. If the 88E1112 device interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 clause 40.4.4 determines which device performs the crossover.

When the 88E1112 device interoperates with legacy 10BASE-T devices that do not implement Auto-Negotiation, the 88E1112 device follows the same algorithm as described above since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the 88E1112 device uses signal detect to determine whether or not to crossover.

The auto MDI/MDIX crossover function can be disabled via register 16_0.6:5.

The pin mapping in MDI and MDIX modes is shown in Table 23.

Table 23: Media Dependent Interface Pin Mapping

Pin	MDI			MDIX		
	1000BASE-T	100BASE-TX	10BASE-T	1000BASE-T	100BASE-TX	10BASE-T
MDIP/N[0]	BI_DA±	TX±	TX±	BI_DB±	RX±	RX±
MDIP/N[1]	BI_DB±	RX±	RX±	BI_DA±	TX±	TX±
MDIP/N[2]	BI_DC±	unused	unused	BI_DD±	unused	unused
MDIP/N[3]	BI_DD±	unused	unused	BI_DC±	unused	unused

Note

Table 23 assumes no crossover on PCB.

The MDI/MDIX status is indicated by Register 17_0.6. This bit indicates whether the receive pairs (3,6) and (1,2) are crossed over. In 1000BASE-T operation, the device can correct for crossover between pairs (4,5) and (7,8) as shown in the table above. However, this is not indicated by Register 17_0.6.

If 1000BASE-T link is established, pairs (1,2) and (3,6) crossover is reported in register 21_5.4, and pairs (4,5) and (7,8) crossover is reported in register 21_5.5.

2.18 Polarity Correction

The 88E1112 device automatically corrects polarity errors on the receive pairs in 1000BASE-T and 10BASE-T modes. In 100BASE-TX mode, the polarity does not matter.

In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-T link is up. The polarity becomes unlocked when link is down.

The polarity correction status is indicated by Register 17_0.1. This bit indicates whether the receive pair (3,6) is polarity reversed in MDI mode of operation. In MDIX mode of operation, the receive pair is (1,2) and Register 17_0.1 indicates whether this pair is polarity reversed. Although all pairs are corrected for receive polarity reversal, Register 17_0.1 only indicates polarity reversal on the pairs described above.

If 1000BASE-T link is established register 21_5.3:0 reports the polarity on all 4 pairs.

2.19 EEPROM Interface

The 88E1112 device supports the ability to read an EEPROM in order to automatically initialize the internal PHY registers. The 88E1112 device can also act as a bridge so that the EEPROM can be accessed via the MDC/MDIO interface of the PHY.

2.19.1 EEPROM to RAM to MDIO Transfers

If the host communicates with the 88E1112 device via the MDC/MDIO interface that is configured to operate as a Two-Wire Serial Interface, then the 88E1112 device has direct access to the EEPROM via a second Two-Wire Serial Interface. We will call the first Two-Wire Serial Interface the host interface, and the second interface the EEPROM interface.

Upon the deassertion of hardware reset and the completion of hardware configuration the 88E1112 device reads the EEPROM and stores the values into a RAM in the PHY. The contents of the EEPROM can be reloaded into RAM by writing register 18_4.11 to a 1. This bit is self-clearing. The result of the reload can be read via register 17_4.10:8.

The maximum size EEPROM that can be handled is 256 bytes. If the EEPROM is smaller than 256 bytes the unused bytes are filled with all ones, assuming the EEPROM does not respond for invalid address locations. The expected device type and device page selection in the slave address of the EEPROM is 1010000. Any other value will result in the EEPROM not being read.

At the same time that the RAM is being loaded, the PHY registers are initialized based on the values stored in the EEPROM. See 2.19.2 "PHY Register Initialization" for more details.

Note that if register 18_4.11:10 is set to 11 the PHY register initialization will restart.

After the PHY register initialization, the host can access the PHY registers or the contents of the RAM via the Two-Wire Serial Interface. The host also has the ability to issue read and write commands to the EEPROM interface via PHY registers. Usually this direct access capability is not required, but it can be useful should the host require access to non-EEPROM devices that may also be attached to the EEPROM interface.

For detailed description of how the MDC/MDIO functions in the Two-Wire Serial Interface mode please refer to “Two-Wire Serial Interface” on page 47.

However the following points should be noted.

The device type and device page selection presented on the host interface to access the RAM in the PHY is 1010000. This value make the EEPROM appear to be directly connected to the host.

The device type and device page selection presented on the host interface to access all PHY registers other than the RAM is 10, PHYADR[4:0]. Note that if PHYADR[4:0] is set to 10000 then there is a conflict between accessing the PHY registers and the RAM. In this case, the PHY registers takes precedence and the RAM will not be accessible.

When accessing the RAM, data is passed one byte at a time. When accessing the PHY registers data must be passed in pairs since all PHY registers are 16 bits long.

Figure 25: Two-Wire Serial Interface to Two-Wire Serial Interface Bridging

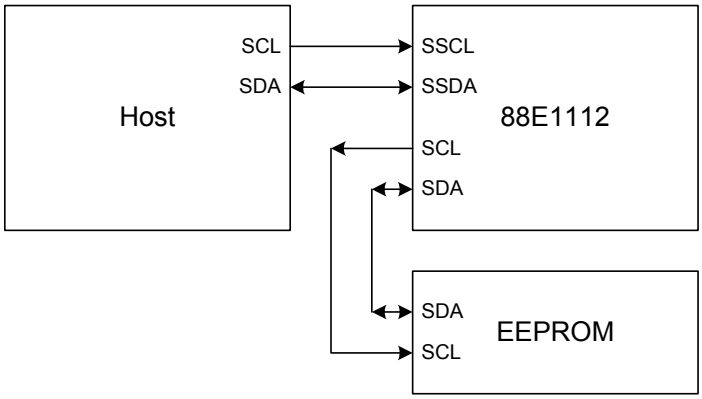
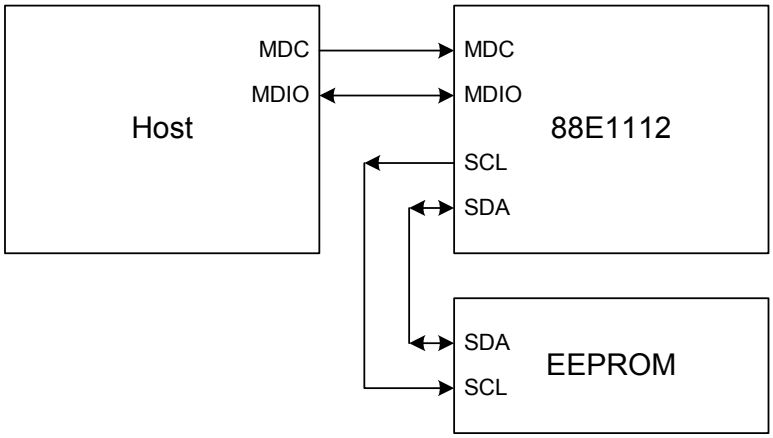


Figure 25 is identical to the operation in Figure 26 except the MDC/MDIO pins of the 88E1112 device is configured to operate in the MDC/MDIO mode.

In this mode of operation, the access to the RAM must be indirectly addressed since there are not enough IEEE registers. Register 20_4.7:0 sets the RAM address. A read to register 19_4.7:0 reads the contents in the RAM at the address specified by 20_4.7:0.

Figure 26: MDC/MDIO Bridging



2.19.2 PHY Register Initialization

Each four bytes of the EEPROM will update one 16-bit PHY register. The first byte of each four bytes starts at an EEPROM address location that is divisible by 4 (i.e. 0, 4, 8, etc.). The fields of these four bytes are defined in Table 24 (N is divisible by 4).

Table 24: EEPROM Byte Mapping

EEPROM Byte	Bit Mapping
Byte N bits 7:0	PAGE[7:0]
Byte N+1 bits 7:5	010 = Valid Location
	All other values terminate EEPROM register update.
Byte N+1 bits 4:0	REGADR[4:0]
Byte N+2 bits 7:0	DATA[15:8]
Byte N+3 bits 7:0	DATA[7:0]

Since the 88E1112 device only has 32 registers, a paging mechanism is use to extend the address space. For PHY registers 0 to 28 the paging is controlled by register 22. For registers 30 and 31 the paging is controlled by register 29. For example, in a normal MDC/MDIO write of page 1 register 0 the following sequence will take place:

1. Write 1 to register 22 to set the page.
2. Write register 0 to put the desired 16 bits into page 1 register 0.

The four byte field shown in allows the page and register to be specified at the same time so there is no need to write registers 22 or 29 prior to writing the target register.

Note that the loader does not match the PHYADR[4:0] of the PHY since it is assumed that only 1 PHY is attached to the EEPROM.

After the RAM is loaded the 88E1112 device will read the EEPROM starting from EEPROM address location 0, 96, or 128 depending on the setting of the EEPROM[1:0] bits during hardware configuration (Section 2.4 "Hardware Configuration" on page 37). The reading of the EEPROM will continue four bytes at a time until a stop byte is read from the EEPROM or until the EEPROM does not respond to a read request. The stop byte is defined to be byte N+1 bits 7:5 not set to 010.

The order of the PHY register update is dependent on the sequence presented by the EEPROM. This is useful since some register updates will not take effect unless the software reset bit is set.

Note that only hardware reset will cause the EEPROM loader to read the EEPROM. A software reset will not cause the EEPROM loader to do anything. A reload can be initiated by setting register 18_4.11:10 to 11. These bits are self-clearing. The result of the reload can be read via register 17_4.10:8.

2.19.3 Bridging Function

The bridging function allows the contents of the EEPROM to be accessed directly via the MDC/MDIO. The access is through a series of reads and writes to the PHY register. Note that the access is not limited to the EEPROM but also to any device that is attached to the Two-Wire Serial Interface.

Since other devices may be connected to the Two-Wire Serial Interface where the slave address is not necessarily 1010xxx, there must be a hook to access the Two-Wire Serial Interface device directly from the MDIO. Registers 16_4, 17_4, and 18_4 give direct access between the MDIO and the Two-Wire Serial Interface.

2.19.3.1 Read from Two-Wire Serial Interface slave device to the MDIO

When a read operation to theTwo-Wire Serial Interface is required, the slave address and byte address is written to register 16_4.15:9 and 16_4.7:0 respectively with register 16_4.8 set to 1 indicating read. Once register 16_4 is written a read operation on the Two-Wire Serial Interface commences only if the Two-Wire Serial Interface is free, otherwise a read operation on the Two-Wire Serial Interface is never issued. The byte that is read is stored in register 17_4.7:0. The status of the read operation is stored in register 17_4.10:8.

While the read operation is pending register 17_4.10:8 is set to 010. Once the read operation is completed and the Two-Wire Serial Interface slave sends all acknowledges register 17_4.10:8 is set to 001 indicating the read operation completed without error. A 101 is returned if the read command is aborted when the Two-Wire Serial Interface slave does not acknowledge properly. A 111 is returned if the Two-Wire Serial Interface is busy when register 16_4 was written.

Note that other than the 010 setting (command in progress) a read to 17_4 will cause bits 10:8 to clear to 000.

2.19.3.2 Write from MDIO into the Two-Wire Serial Interface slave device

Write commands into the EEPROM are always available through the MDIO. If write access should be disabled, the EEPROM itself should be configured to ignore write commands from the 88E1112 device.

When a write operation to the Two-Wire Serial Interface is required, the byte data should first be written into 18_4.7:0. The slave address and byte address is written to register 16_4.15:9 and 16_4.7:0 respectively with register 16_4.8 set to 0 indicating write. Once register 16_4 is written a write operation to the Two-Wire Serial Interface commences. If the read back bit is set in register 18_4.9 then a read operation to the same address is performed after the write. The byte that is read is stored in register 17_4.7:0. The status of the write operation is stored in register 17_4.10:8.

While the write operation is pending register 17_4.10:8 is set to 010. Once the write operation is completed and optionally the read back command and the Two-Wire Serial Interface slave sends all acknowledges, register 17_4.10:8 is set to 001 indicating the write operation completed without error. A 011 is returned if the write operation is successfully completed but the read back command is aborted. A 101 is returned if the write command is aborted when the Two-Wire Serial Interface slave does not acknowledge properly. A 111 is returned if the Two-Wire Serial Interface is busy when register 16_4 was written. Note that other than the 010 setting (command in progress) a read to 17_4 will cause bits 10:8 to clear to 000.

Since it may take some time for the write to take effect in the external device, the 88E1112 device should wait for some amount of time as programmed in register 18_4.15:12 after the write operation before issuing a read back command.

2.19.4 INIT Functionality

The INIT pin outputs a status of whether the EEPROM contents are loaded into the PHY RAM and the PHY registers completed initialization. A hi-Z indicates that the PHY is currently loading the RAM and PHY register initialization is not completed, a zero indicates that the RAM loading and PHY register initialization is completed.

Note that the INIT pin transitioning from hi-Z to 0 is a one-time event for each hardware reset. For example if register 18_4.11 is set to 1 to reload the contents of the EEPROM into the RAM, the INIT pin will remain 0.

Note that the Register default for 16_3.11:8 = 0010 and 17_3.5:4 = 10 is required for the INIT functionality as described in this section. Changing these registers will reprogram the INIT pin to operate differently. See Section 2.21 for more details.

2.20 Interrupt

The interrupt function is enabled when register 16_3.11:8 is set to 1110. The INIT pin functions as the interrupt pin. The polarity of the interrupt pin is defined by register 17_3.5:4. An active interrupt is defined as "On" and inactive interrupt is defined as "Off".

The interrupt enable bits in registers 18_0, 18_1, and 18_2 correspond to the status bits in registers 19_0, 19_1, and 19_2 respectively.

The various pages of register 18 are used to select the interrupt events that can activate the interrupt pin. The interrupt pin will be activated if any of the selected events on any page of register 18 occur.

If a certain interrupt event is not selected by register 18, it will still be indicated by the corresponding register 19 bits if the interrupt event happens. However, the unselected events will not cause the Interrupt pin to be activated.

2.21 LED

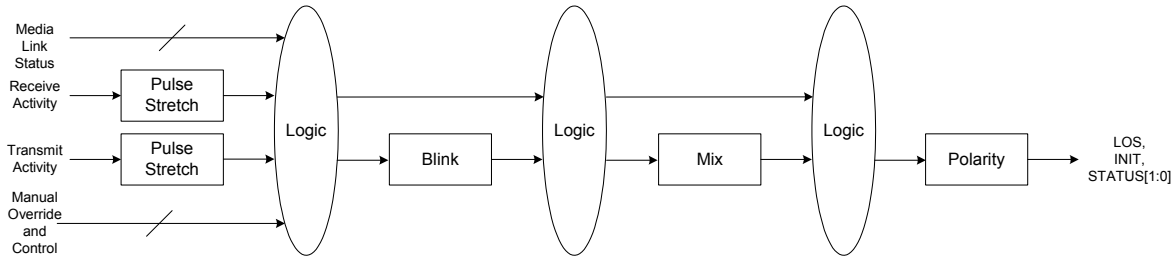
The LOS, INIT, and STATUS[1:0] pins can be used to drive LED pins. Registers 16_3, 17_3, and 18_3 controls the operation of the LED pins. When register 16_3.15:12 is set to 0000 the LOS pin operates as described in Section "LOS Output" on page 23. When register 16_3.11:8 is set to 0010 the INIT pin operates as described in section Section 2.19.4 "INIT Functionality" on page 69. When Register 16_3.11:8 is set to 1110, the INIT pin operates as described in Section 2.20 "Interrupt" on page 69. STATUS[1:0] is used to configure the PHY per section Section 2.4 "Hardware Configuration" on page 37. After the configuration is completed, STATUS[1:0] will operate per the setting in 16_3.7:0.

In general 16_3.15:12 controls the LOS pins, 16_3.11:8 controls the INIT pin, 16_3.7:4 controls the STATUS[1] pin, and 16_3.3:0 controls the STATUS[0] pin. These are referred to single LED modes.

However, there are some LED modes where LOS and INIT pins operate as a unit, and STATUS[1:0] pins operate as a unit. These are entered when 16_3.11:10 is set to 11, or 16_3.3:2 is set to 11 respectively. These are referred to as dual LED modes. In dual LED modes register 16_3.15:12 have no meaning when 16_3.11:10 is set to 11, and 16_3.7:4 have no meaning when 16_3.3:2 is set to 11.

Figure 27 shows the general chaining of function for the LEDs. The various functions are described in the following sections.

Figure 27: LED Chain



2.21.1 LED Polarity

There are a variety of ways to hook up the LEDs. Some examples are shown in Figure 28. In order to make things more flexible registers 17_3.7:6, 17_3.5:4, 17_3.3:2, and 17_3.1:0 specify the output polarity for the LOS, INIT, STATUS[1], and STATUS[0] respectively. The lower bit of each pair specified the on (active) state of the LED, either high or low. The upper bit of each pair specifies whether the off state of the LED should be driven to the opposite level of the on state or Hi-Z. The Hi-Z state is useful in cases such the LOS and INIT function where the inactive state is Hi-Z.

Figure 28: Various LED Hookup Configurations

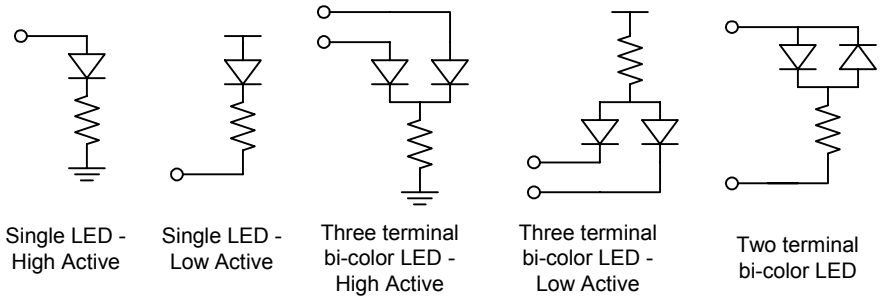


Table 25: LED Polarity

Register	Pin	Definition
17_3.7:6	LOS Polarity	00 = On - drive LOS low, Off - drive LOS high 01 = On - drive LOS high, Off - drive LOS low 10 = On - drive LOS low, Off - tristate LOS 11 = On - drive LOS high, Off - tristate LOS
17_3.5:4	INIT Polarity	00 = On - drive INIT low, Off - drive INIT high 01 = On - drive INIT high, Off - drive INIT low 10 = On - drive INIT low, Off - tristate INIT 11 = On - drive INIT high, Off - tristate INIT
17_3.3:2	STATUS[1] Polarity	00 = On - drive STATUS[1] low, Off - drive STATUS[1] high 01 = On - drive STATUS[1] high, Off - drive STATUS[1] low 10 = On - drive STATUS[1] low, Off - tristate STATUS[1] 11 = On - drive STATUS[1] high, Off - tristate STATUS[1]
17_3.1:0	STATUS[0] Polarity	00 = On - drive STATUS[0] low, Off - drive STATUS[0] high 01 = On - drive STATUS[0] high, Off - drive STATUS[0] low 10 = On - drive STATUS[0] low, Off - tristate STATUS[0] 11 = On - drive STATUS[0] high, Off - tristate STATUS[0]

2.21.2 Pulse Stretching and Blinking

Register 18_3.14:12 specifies the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require blinking instead of a solid on. Register 18_3.10:8 specifies the blink rate. Note that the pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse.

The stretched/blinked output will then be mixed if needed (Section 2.21.3) and then inverted/Hi-Z according to the polarity described in section (Section 2.21.1)

Table 26: Pulse Stretching and Blinking

Register	Pin	Definition
18_3.14:12	Pulse stretch duration	000 = no pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
18_3.10:8	Blink Rate	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved

2.21.3 Bi-Color LED Mixing

In the dual LED modes the mixing function allows the 2 colors of the LED to be mixed to form a third color. This is useful since the PHY is tri speed and the three colors each represent one of the speeds. Register 17_3.15:12 control the amount to mix in the LOS and STATUS[1] pins. Register 17_3.11:8 control the amount to mix in the INIT and STATUS[0] pins. The mixing is determined by the percentage of time the LED is on during the active state. The percentage is selectable in 12.5% increments.

Note that there are two types of bi-color LEDs. There is the three terminal type and the 2 terminal type. For example, the third and fourth LED block from the left in Figure 28 illustrate three terminal types, and the one on the far right is the two terminal type. In the three terminal type the both of the LEDs can be turned on at the same time. Hence the sum of the percentage specified by 17_3.15:12 and 17_3.11:8 can exceed 100%. However, in the two terminal type the sum should never exceed 100% since only 1 LED can be turned on at any given time.

The mixing only applies when register 16_3.11:8 or 16_3.3:0 are set to 11xx. There is no mixing in single LED modes.

Table 27: Bi-Color LED Mixing

Register	Function	Definition
17_3.15:12	LOS, STATUS[1] mix percentage	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
17_3.11:8	INIT, STATUS[0] mix percentage	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5%, . . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved

2.21.4 Modes of Operation

The LEDs function takes some statuses of the PHY and presents it in a certain way on the LEDs. Most of the single LED modes are self-explanatory from the register map of register 16_3. We will cover the non-obvious ones in this section.

Table 28: Modes of Operation

Register	Pin	Definition
16_3.15:12	LOS Control	If 16_3.11:9 is set to 110 then 16_3.15:12 has no effect 0000 = Normal LOS operation 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - 10 Mbps or 1000 Mbps Master, Off - Else 0111 = On - Fiber Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
16_3.11:8	INIT Control	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = Normal INIT operation 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - 10/1000 Mbps Link, Off - Else 0111 = On - 10 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 1101 = MODE 2 1110 = Interrupt 1111 = Reserved

Table 28: Modes of Operation (Continued)

Register	Pin	Definition
16_3.7:4	STATUS[1] Control	If 16_3.3:2 is set to 11 then 16_3.7:4 has no effect 0000 = On - Copper Link, Off - Else 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - 100 Mbps Link or Fiber Link, Off - Else 0110 = On - 100/1000 Mbps Link, Off - Else 0111 = On - 100 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
16_3.3:0	STATUS[0] Control	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mbps 2 blinks - 100 Mbps 1 blink - 10 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 1101 = MODE 2 1110 = MODE 3 1111 = MODE 4

2.21.4.1 Compound Single LED Statuses

Compound LED status are defined in Table 29.

Table 29: Compound LED Status

Compound Status	Description
Activity	Transmit Activity OR Receive Activity
Link	10BASE-T link OR 100BASE-TX Link OR 1000BASE-T Link OR 100BASE-FX link OR 1000BASE-X Link
Fiber Link	100BASE-FX link OR 1000BASE-X Link
Copper Link	10BASE-T link OR 100BASE-TX Link OR 1000BASE-T Link

Note that there are some other odd looking compound status such as 10 Mbps Link OR 1000 Mbps Master (16_3.15:12 = 0110) and 100 Mbps Link OR Fiber Link (16_3.7:4 = 0101). These strange ones allow for the 3 LED link/speed statuses seen in 88E1040/88E1145 device to be recreated on 88E1112 device.

2.21.4.2 Speed Blink

When 16_3.3:0 is set to 0010 the STATUS[0] pin take on the following behavior.

STATUS[0] outputs the sequence shown in depending on the status of the link. The sequence consists of 8 segments. If a 1000 Mbps link is established the STATUS[0] outputs 3 pulses, 100 Mbps 2 pulses, 10 Mbps 1 pulse, and no link 0 pulses. The sequence repeats over and over again indefinitely.

The duration of the on pulse is specified in 18_3.1:0. The duration between pulses is specified in 18_3.3:2.

Table 30: Speed Blinking Sequence

Segment	10Mbps	100Mbps	1000Mbps	No Link	Duration
1	On	On	On	Off	18_3.1:0
2	Off	Off	Off	Off	18_3.3:2
3	Off	On	On	Off	18_3.1:0
4	Off	Off	Off	Off	18_3.3:2
5	Off	Off	On	Off	18_3.1:0
6	Off	Off	Off	Off	18_3.3:2
7	Off	Off	Off	Off	18_3.1:0
8	Off	Off	Off	Off	18_3.3:2

Table 31: Speed Blink

Register	Pin	Definition
18_3.3:2	Speed Off Pulse Period	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
18_3.1:0	Speed On Pulse Period	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

2.21.4.3 Manual Override

When 16_3.15:14, 16_3.11:10, 16_3.7:6, and 16_3.3:2 are set to 10 the LOS, INIT, STATUS[1], and STATUS[0] are respectively manually forced. Registers 16_3.13:12, 16_3.9:8, 16_3.5:4, and 16_3.1:0 then select whether the LEDs are to be on, off or Hi-Z.

If bi-color LEDs are used, the manual override will select only one of the 2 colors. In order to get the third color by mixing MODE 1 and MODE 2 should be used (Section 2.21.4.4).

2.21.4.4 MODE 1, MODE 2, MODE 3, MODE 4

MODE 1 to 4 are dual LED modes. These are used to mix to a third color using bi-color LEDs.

When 16_3.3:0 is set to 11xx then one of the 4 modes are enabled.

When 16_3.11:8 is set to 110x then one of MODE 1 or MODE 2 are enabled.

MODE 1 – Solid mixed color. The mixing is discussed in Section 2.21.3.

MODE 2 – Blinking mixed color. The mixing is discussed in Section 2.21.3. The blinking is discussed in section Section 2.21.2.

MODE 3 – Behavior according to Table 32.

MODE 4 – Behavior according to Table 33.

Note that MODE 4 is the same as MODE 3 except the 10 Mbps and 100 Mbps are reversed.

Table 32: MODE 3 Behavior

Status	STATUS[1]	STATUS[0]
1000 Mbps Link - No Activity	Off	Solid On
1000 Mbps Link - Activity	Off	Blink
100 Mbps Link - No Activity	Solid Mix	Solid Mix
100 Mbps Link - Activity	Blink Mix	Blink Mix
10 Mbps Link - No Activity	Solid On	Off
10 Mbps Link - Activity	Blink	Off
No link	Off	Off

Table 33: MODE 4 Behavior

Status	STATUS[1]	STATUS[0]
1000 Mbps Link - No Activity	Off	Solid On
1000 Mbps Link - Activity	Off	Blink
100 Mbps Link - No Activity	Solid On	Off
100 Mbps Link - Activity	Blink	Off
10 Mbps Link - No Activity	Solid Mix	Solid Mix
10 Mbps Link - Activity	Blink Mix	Blink Mix
No link	Off	Off

Section 3. Register Description

The IEEE defines only 32 registers address space for the PHY. In order to extend the number of registers address space available a paging mechanism is used. For register address 0 to 21, and 23 to 28 register 22 bits 7 to 0 are used to specify the page. For registers 30 and 31 register 29 bits 5:0 are used to specify the page. There is no paging for registers 22 and 29.

In this document, the short hand used to specify the registers take the form register_page.bit:bit, register_page.bit, register.bit:bit, or register.bit.

For example:

Register 0 page 1 bits 5 to 2 is specified as 0_1.5:2.

Register 0 page 1 bit 5 is specified as 0_1.5.

Register 2 bits 3 to 0 is specified as 2.3:0.

Note that in this context the setting of the page register (register 22) has no effect.

Register 2 bit 3 is specified as 2.3.

For registers that have multiple pages, if the page is not indicated, the bits shown are common to all pages.

e.g., Register 0.15 means 0_0.15 or 0_1.15 or 0_2.15.

Note that in order for the paging mechanism to work correctly register 22.15 must be set to 0 to disable the automatic medium register selection.

Table 34: Register Map Summary

Register Address	Page Address 0	Page Address 1	Page Address 2	Page Address 3	Page Address 4	Page Address 5	Page Address 6	Page Address 7 to 255
0	Copper Control	Fiber Control	MAC Control					
1	Copper Status	Fiber Status						
2	PHY Identifier 1							
3	PHY Identifier 2							
4	Autonegotiation Copper Advertisement	Autonegotiation Fiber Advertisement						
5	Autonegotion Copper Link Partner Ability - Base Page	Autonegotion Fiber Link Partner Ability - Base Page						
6	Autonegotiation Copper Expansion	Autonegotiation Fiber Expansion						
7	Autonegotiation Copper Next Page Transmit Register	Autonegotiation Fiber Next Page Transmit Register						
8	Autonegotiation Copper Link Partner Next Page	Autonegotiation Fiber Link Partner Next Page						
9	1000BASE-T Control							
10	1000BASE-T Status							
11	Reserved							
12	Reserved							
13	Reserved							
14	Reserved							
15	Extended Status							
16	Copper Specific Control Register 1	Fiber Specific Control Register 1	MAC Specific Control Register 1	LOS, INIT, STATUS[1:0] Function Control Register	Non-Volatile Memory Address	VCT Status MDI[0]	Packet Generation/Stub loopback	
17	Copper Specific Status Register 1	Fiber Specific Status Register 1	MAC Specific Status Register 1	LOS, INIT, STATUS[1:0] Polarity Control Register	Non-Voltile Memory Read Data and Status	VCT Status MDI[1]	CRC checker	
18	Copper Interrupt Enable Register	Fiber Interrupt Enable Register	MAC Interrupt Enable Register	LOS, INIT, STATUS[1:0] Timer Control Register	Non-Voltile Memory Write Data and Control	VCT Status MDI[2]		
19	Copper Specific Status Register 2	Fiber Specific Status Register 2	MAC Specific Status Register 2		Non-Voltile Memory Write Data and Control	VCT Status MDI[3]		
20					Non-Volatile Memory Address	VCT Skew		
21	Receive Error Counter					VCT Pair Swap and Polarity		
22	Page Address							
23	Reserved							
24	Reserved							
25	Reserved							
26	Copper Specific Control Register 2	Fiber Specific Control Register 2	MAC Specific Control Register 2			VCT DSP Distance		
27	Reserved							
28	Reserved							
29	Factory Test Modes							
30	Factory Test Modes							
31	Factory Test Modes							

Table 35 defines the register modes used in the following register map.

Table 35: Register Mode Definitions

Register Types	
Type	Description
LH	Register field with latching high function. If status is high, then the register bit is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register bit is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to a register field does take effect without a software reset.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only.
ROC	Read only clear. After read, register field is cleared.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, register field is cleared to zero.
RWR	Read/Write reset. All field bits are readable and writable. After reset, register field is cleared to zero.
RWS	Read/Write set. All field bits are readable and writable. After reset, register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete.
Update	Value written to the register field doesn't take effect until soft reset is executed. The value can still be read after it is written.
WO	Write only. Reads to this type of register field return undefined data.

For all binary equations appearing in the register map, the symbol | is equal to a binary OR operation.

Table 36: Register Map

Register Name	Register Address	Table and Page
Control Register - Copper	Page 0, Register 0	Table 37, p. 85
Control Register - Fiber	Page 1, Register 0	Table 38, p. 88
Control Register - MAC	Page 2, Register 0	Table 39, p. 91
Status Register - Copper	Page 0, Register 1	Table 40, p. 92
Status Register - Fiber	Page 1, Register 1	Table 41, p. 95
PHY Identifier 1	Page Any, Register 2	Table 42, p. 97
PHY Identifier 2	Page Any, Register 3	Table 43, p. 97
Auto-Negotiation Advertisement Register - Copper	Page 0, Register 4	Table 44, p. 98
Auto-Negotiation Advertisement Register - Fiber	Page 1, Register 4	Table 45, p. 101
Link Partner Ability Register - Base Page, Copper	Page 0, Register 5	Table 46, p. 104
Link Partner Ability Register - Base Page, Fiber	Page 1, Register 5	Table 47, p. 105
Auto-Negotiation Expansion Register - Copper	Page 0, Register 6	Table 48, p. 107
Auto-Negotiation Expansion Register - Fiber	Page 1, Register 6	Table 49, p. 108
Next Page Transmit Register - Copper	Page 0, Register 7	Table 50, p. 109
Next Page Transmit Register - Fiber	Page 1, Register 7	Table 51, p. 109
Link Partner Next Page Register - Copper	Page 0, Register 8	Table 52, p. 110
Link Partner Next Page Register - Fiber	Page 1, Register 8	Table 53, p. 110
1000BASE-T Control Register	Page 0, Register 9	Table 54, p. 111
1000BASE-T Status Register	Page 0, Register 10	Table 55, p. 112
Extended Status Register	Page 0,1, Register 15	Table 56, p. 113
Copper Specific Control Register 1	Page 0, Register 16	Table 57, p. 114
Fiber Specific Control Register 1	Page 1, Register 16	Table 58, p. 115
MAC Specific Control Register 1	Page 2, Register 16	Table 59, p. 116
LOS, INIT, STATUS[1:0] Function Control Register	Page 3, Register 16	Table 60, p. 118
Non-Volatile Memory Address Register	Page 4, Register 16	Table 61, p. 119
MDI[0] Virtual Cable Tester™ Status Register	Page 5, Register 16	Table 62, p. 120
Packet Generation	Page 6, Register 16	Table 63, p. 120
Copper Specific Status Register 1	Page 0, Register 17	Table 64, p. 121
Fiber Specific Status Register 1	Page 1, Register 17	Table 65, p. 123

Table 36: Register Map (Continued)

Register Name	Register Address	Table and Page
MAC Specific Status Register 1	Page 2, Register 17	Table 66, p. 125
LOS, INIT, STATUS[1:0] Polarity Control Register	Page 3, Register 17	Table 67, p. 126
Non-Volatile Memory Read Data and Status Register	Page 4, Register 17	Table 68, p. 127
MDI[1] Virtual Cable Tester™ Status Register	Page 5, Register 17	Table 69, p. 129
CRC Counters	Page 6, Register 17	Table 70, p. 129
Interrupt Enable Register - Copper	Page 0, Register 18	Table 71, p. 130
Interrupt Enable Register - Fiber	Page 1, Register 18	Table 72, p. 131
Interrupt Enable Register - MAC	Page 2, Register 18	Table 73, p. 132
LOS, INIT, STATUS[1:0] Timer Control Register	Page 3, Register 18	Table 74, p. 133
Non-Volatile Memory Write Data and Control Register	Page 4, Register 18	Table 75, p. 133
MDI[2] Virtual Cable Tester™ Status Register	Page 5, Register 18	Table 76, p. 134
Copper Specific Status Register 2	Page 0, Register 19	Table 77, p. 135
Fiber Specific Status Register 2	Page 1, Register 19	Table 78, p. 137
MAC Specific Status Register 2	Page 2, Register 19	Table 79, p. 138
Non-Volatile Memory Write Data and Control Register	Page 4, Register 19	Table 80, p. 138
MDI[3] Virtual Cable Tester™ Status Register	Page 5, Register 19	Table 81, p. 139
Non-Volatile Memory Address Register	Page 4, Register 20	Table 82, p. 139
1000 BASE-T Pair Skew Register	Page 5, Register 20	Table 83, p. 140
Receive Error Counter Register	Page 0,1, Register 21	Table 84, p. 140
1000 BASE-T Pair Swap and Polarity	Page 5, Register 21	Table 85, p. 141
Page Address	Page Any, Register 22	Table 86, p. 142
Copper Specific Control Register 2	Page 0, Register 26	Table 87, p. 142
Fiber Specific Control Register 2	Page 1, Register 26	Table 88, p. 143
MAC Specific Control Register 2	Page 2, Register 26	Table 89, p. 144
VCT™ DSP Distance	Page 5, Register 26	Table 90, p. 145

Table 37: Control Register - Copper
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x0	SC	PHY Software Reset. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. This bit is identical to 0_1.15 and 0_2.15. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on S_IN+/- is looped back to S_OUT+/- internally. Link is broken when loopback is enabled. Loopback speed is determined by the mode the device is in Registers 0_2.13 and 0_2.6. This bit is identical to 0_1.14. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps

Table 37: Control Register - Copper (Continued)
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Auto-Negotiation Enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 is set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	Power Down	R/W	0x0	Retain	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_0.15, 0_1.15, or 0_2.15) and Restart Auto-Negotiation (0_0.9) are not set by the user. IEEE power down shuts down the chip except for the SGMII MAC interface if 16_2.3 is set to 1. If 16_2.3 is set to 0, then the SGMII MAC interface also shuts down. This bit is identical to 0_1.11 and 0_2.11. 1 = Power down 0 = Normal operation
10	Isolate	RO	0x0	0x0	This bit has no effect.
9	Restart Copper Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0_0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation

Table 37: Control Register - Copper (Continued)
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Copper Duplex Mode	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation 1 = Full-duplex 0 = Half-Duplex
7	Collision Test	RO	0x0	0x0	This bit has no effect.
6	Speed Selection (MSB)	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
5:0	Reserved	RO	Always 000000	Always 000000	Will always be 0. These bit are identical to 0_1.5:0.

Table 38: Control Register - Fiber
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W	0x0	SC	PHY Software Reset. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. This bit is identical to 0_0.15 and 0_2.15. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on S_IN+/- is looped back to S_OUT+/- internally. Link is broken when loopback is enabled. Loopback speed is determined by the mode the device is in Registers 0_2.13 and 0_2.6. This bit is identical to 0_0.14. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	RO	See Descr	See Descr	Bits 0_1.6, 0_1.13 indicate the fixed speed for 100BASE-FX or 1000BASE-X modes of operation. To configure the SGMII media side interface speed when 0_1.12 disables Auto-Negotiation, use 0_2.6, 0_2.13. Value in 16_2.9:7 0_1.6, 0_1.13 000 01 else 10 bit 6,13 10 = 1000 Mbps 01 = 100Mbps

Table 38: Control Register - Fiber (Continued)
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Auto-Negotiation Enable	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation For SGMII media interface mode of operation (and 1000BASE-X mode of operation), this bit enables/disables Auto-Negotiation. Note that if 16_2.9:7 = 000 then this bit is read only and forced to 0. Upon hardware reset this bit defaults as follows: MODE[1:0] Bit 6,13 00 0 Else 1 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	Power Down	R/W	0x0	Retain	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when Reset (0_0.15, 0_1.15, or 0_2.15) and Restart Auto-Negotiation (0_1.9) are not set by the user. IEEE power down shuts down the chip except for the SGMII MAC interface if 16_2.3 is set to 1. If 16_2.3 is set to 0, then the SGMII MAC interface also shuts down. This bit is identical to 0_0.11 and 0_2.11. 1 = Power down 0 = Normal operation
10	Isolate	R/W	0x0	0x0	This bit has no effect.
9	Restart Fiber Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0_1.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation

Table 38: Control Register - Fiber (Continued)
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Fiber Duplex Mode	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation This bit has no effect when in SGMII media interface mode. 1 = Full-duplex 0 = Half-Duplex
7	Collision Test	R/W	0x0	0x0	This bit has no effect.
6	Speed Selection (MSB)	RO	See Descr	See Descr	See bit 13
5:0	Reserved	RO	Always 000000	Always 000000	Will always be 0. These bit are identical to 0_0.5:0.

Table 39: Control Register - MAC Page 2, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x0	SC	PHY Software Reset. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. This bit is identical to 0_0.15 and 0_1.15. 1 = PHY reset 0 = Normal operation
14	Line Loopback	R/W	0x0	0x0	1 = Enable Line Loopback 0 = Normal Operation
13	Default MAC Interface and SGMII Media Interface Speed (LSB)	R/W	See Descr	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 0_2.6, 0_2.13 set the speed of the SGMII Media Interface when 0_1.12 = 0 (which disables SGMII Media Interface Auto-Negotiation) or when link is down. The SGMII MAC Interface speed will always match the SGMII Media Interface speed. Upon hardware reset this bit defaults as follows: MODE[1:0] Bit 6,13 00 01 Else 10 00 = 10 Mbps 01 = 100 Mbps 1X = 1000 Mbps
12	SGMII MAC Interface or GBIC Auto-Negotiation Enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Power down (Register 0.11) transitions from power down to normal operation 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process

Table 39: Control Register - MAC (Continued)
Page 2, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Power Down	R/W	0x0	Retain	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0_0.9, 0_1.9) are not set by the user. IEEE power down shuts down the chip except for the MAC interface if 16_2.3 is set to 1. If 16_2.3 is set to 0, then the MAC interface also shuts down. This bit is identical to 0_0.11 and 0_1.11. 1 = Power down 0 = Normal operation
10:7	Reserved	RO	Always 0000	Always 0000	Will always be 0000.
6	Default MAC Interface and SGMII Media Interface Speed (MSB)	R/W	See Descr	Update	See bit 13
5:0	Reserved	RO	Always 000000	Always 000000	Will always be 0.

Table 40: Status Register - Copper
Page 0, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0	Always 0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 1_0.14 001 0 11x 0 else 1 1 = PHY able to perform full-duplex 100BASE-X 0 = PHY not able to perform full-duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 1_0.13 001 0 11x 0 else 1 1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X

Table 40: Status Register - Copper (Continued)
Page 0, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
12	10 Mbps Full-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 1_0.12 00x 0 11x 0 else 1 1 = PHY able to perform full-duplex 10BASE-T 0 = PHY not able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 1_0.11 00x 0 11x 0 else 1 1 = PHY able to perform half-duplex 10BASE-T 0 = PHY not able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform half-duplex
8	Extended Status	RO	Always 1	Always 1	1 = Extended status information in Register 15
7	Reserved	RO	Always 0	Always 0	Must always be 0.
6	MF Preamble Suppression	RO	Always 1	Always 1	1 = PHY accepts management frames with preamble suppressed
5	Copper Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete
4	Copper Remote Fault	ROC,LH	0x0	0x0	The Remote Fault bit is set when the following condition occurs: 10BASE-T/100BASE-T/1000BASE-T Auto-Negotiation is enabled and the link partner indicates the remote fault condition by setting D12 and D13 of the Auto-Negotiation base page (IEEE802.3 clause 37.2.1.5). In this case, the device will set Register 5_0.13 and this bit to 1. 1 = Remote fault condition detected 0 = Remote fault condition not detected
3	Auto-Negotiation Ability	RO	Always 1	Always 1	1 = PHY able to perform Auto-Negotiation

Table 40: Status Register - Copper (Continued)
Page 0, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Copper Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_0.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Jabber Detect	RO,LH	0x0	0x0	1 = Jabber condition detected 0 = Jabber condition not detected
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 41: Status Register - Fiber
Page 1, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0	Always 0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 1_1.14 001 0 11x 0 else 1 1 = PHY able to perform full-duplex 100BASE-X 0 = PHY not able to perform full-duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 1_1.13 001 0 11x 0 else 1 1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X
12	10 Mb/s Full Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 1_1.12 00x 0 11x 0 else 1 1 = PHY able to perform full-duplex 10BASE-T 0 = PHY not able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 1_1.11 00x 0 11x 0 else 1 1 = PHY able to perform half-duplex 10BASE-T 0 = PHY not able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform half-duplex
8	Extended Status	RO	Always 1	Always 1	1 = Extended status information in Register 15
7	Reserved	RO	Always 0	Always 0	Must always be 0.
6	MF Preamble Suppression	RO	Always 1	Always 1	1 = PHY accepts management frames with preamble suppressed

Table 41: Status Register - Fiber (Continued)
Page 1, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
5	Fiber Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete
4	Fiber Remote Fault/ Far End Fault Indication	ROC,LH	0x0	0x0	The Fiber Remote Fault bit is set when the following condition occurs: When 1000BASE-X Auto-Negotiation is enabled and the link partner indicates the remote fault condition by set¦ting D12 and D13 of the Auto-Negotiation base page (IEEE802.3 clause 37.2.1.5). In this case, the device will set Register 5_1.13:12 and this bit to 1. 1 = Remote fault condition detected 0 = Remote fault condition not detected When in 100BASE-FX mode this bit indicates far end fault indication when the following condition occurs: FEFI is enabled in the device and FEFI idle patterns are received from the link partner. The device will drop link and set this bit to 1. 1 = FEFI condition detected 0 = FEFI condition not detected
3	Auto-Negotiation Ability	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 1_1.11 000 0 else 1 1 = PHY able to perform Auto-Negotiation 0 = PHY not able to perform Auto-Negotiation
2	Fiber Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_1.10 Link Real Time. This bit has no meaning when in SGMII media interface mode. 1 = Link is up 0 = Link is down
1	Reserved	RO,LH	Always 0	Always 0	Must be 0
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 42: PHY Identifier 1
Page Any, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organization-ally Unique Identifier Bits 3:18	RO	0x0141	0x0141	Marvell® OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18

Table 43: PHY Identifier 2
Page Any, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	Always 000011	Organizationally Unique Identifier bits 19:24 00 0011 ^.....^ bit 19...bit24
9:4	Model Number	RO	Always 001001	Always 001001	Model Number 001001
3:0	Revision Num-ber	RO	See Descr	See Descr	Rev Number Contact Marvell FAEs for information on the device revi-sion number.

Table 44: Auto-Negotiation Advertisement Register - Copper Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4_0.15 should be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised
14	Ack	RO	Always 0	Always 0	Must be 0.
13	Remote Fault	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. 1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Reserved	R/W	0x0	Retain	This bit must be read and left unchanged when performing a write.
11	Asymmetric Pause	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. 1 = Asymmetric Pause 0 = No asymmetric Pause

Table 44: Auto-Negotiation Advertisement Register - Copper (Continued)
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Pause	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	R/W	0x0	Retain	0 = Not capable of 100BASE-T4
8	100BASE-TX Full-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: MODE[1:0] Bit 4_0.8 0x 0 1x 1 1 = Advertise 0 = Not advertised

Table 44: Auto-Negotiation Advertisement Register - Copper (Continued)
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
7	100BASE-TX Half-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: MODE[1:0] Bit 4_0.7 0x 0 1x 1 1 = Advertise 0 = Not advertised
6	10BASE-TX Full-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: MODE[1:0] Bit 4_0.6 0x 0 1x 1 1 = Advertise 0 = Not advertised

Table 44: Auto-Negotiation Advertisement Register - Copper (Continued)
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
5	10BASE-TX Half-Duplex	R/W	See Descr	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. Upon hardware reset this bit defaults as follows: MODE[1:0] Bit 4_0.5 0x 0 1x 1 1 = Advertise 0 = Not advertised
4:0	Selector Field	R/W	0x01	Retain	Selector Field mode 00001 = 802.3

Note

Register 4_0 is valid only when register 16_2.9:7 = 001, 010, 011, or 101

Table 45: Auto-Negotiation Advertisement Register - Fiber
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Fiber link goes down. This bit has no effect when in SGMII media interface or 100BASE-FX mode. 1 = Advertise 0 = Not advertised

Table 45: Auto-Negotiation Advertisement Register - Fiber (Continued)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
14	Reserved	RO	Always 0	Always 0	Must be 0.
13:12	Remote Fault 2 Remote Fault 1	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Fiber link goes down. This bit has no effect when in SGMII media interface or 100BASE-FX mode. Device has no ability to detect remote fault. 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	0x0	0x0	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Fiber link goes down. This bit has no effect when in SGMII media interface mode. Reserved bit is R/W to allow for forward compatibility with future IEEE standards.
8:7	Pause	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Fiber link goes down. This bit has no effect when in SGMII media interface or 100BASE-FX mode. 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.

Table 45: Auto-Negotiation Advertisement Register - Fiber (Continued)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
6	1000BASE-X Half-Duplex	R/W	0x1	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Fiber link goes down. This bit has no effect when in SGMII media interface or 100BASE-FX mode. 1 = Advertise 0 = Not advertised
5	1000BASE-X Full-Duplex	R/W	0x1	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Fiber link goes down. This bit has no effect when in SGMII media interface or 100BASE-FX mode. 1 = Advertise 0 = Not advertised
4:0	Reserved	RO	0x00	0x00	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Fiber link goes down. This bit has no effect when in SGMII media interface or 100BASE-FX mode. Reserved bit is R/W to allow for forward compatibility with future IEEE standards.

Table 46: Link Partner Ability Register - Base Page, Copper
Page 0, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
13	Remote Fault	RO	0x0	0x0	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
12	Technology Ability Field	RO	0x0	0x0	Received Code Word Bit 12
11	Asymmetric Pause	RO	0x0	0x0	Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	Pause Capable	RO	0x0	0x0	Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
9	100BASE-T4 Capability	RO	0x0	0x0	Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
8	100BASE-TX Full-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
7	100BASE-TX Half-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
6	10BASE-T Full-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
5	10BASE-T Half-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
4:0	Selector Field	RO	0x00	0x00	Selector Field Received Code Word Bit 4:0

Table 47: Link Partner Ability Register - Base Page, Fiber Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page (1000BASE-X) / Link (SGMII media interface)	RO	0x0	0x0	1000BASE-X Mode - Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page SGMII media interface Mode - Link 1 = Link Up 0 = Link Down This bit has no effect when in 100BASE-FX mode.
14	Acknowledge	RO	0x0	0x0	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability This bit has no effect when in 100BASE-FX mode.
13:12	Remote Fault (1000BASE-X) / Duplex (SGMII media interface)	RO	0x0	0x0	1000BASE-X Mode - Received Code Word Bit 13:12 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error SGMII media interface Mode Bit 13 - Reserved Bit 12 - 1 = Full Duplex, 0 = Half Duplex This bit has no effect when in 100BASE-FX mode.
11:10	Reserved (1000BASE-X) / Speed (SGMII media interface)	RO	0x0	0x0	1000BASE-X Mode - Received Code Word Bit 11:9 Reserved SGMII media interface Mode 00 = 10Mb/s 01 = 100Mb/s 10 = 1000Mb/s 11 = Reserved This bit has no effect when in 100BASE-FX mode.
9	Reserved	RO	0x0	0x0	Reserved

Table 47: Link Partner Ability Register - Base Page, Fiber (Continued)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
8:7	Asymmetric Pause (1000BASE-X) / Reserved (SGMII media interface)	RO	0x0	0x0	1000BASE-X Mode - Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device. SGMII media interface Mode Reserved This bit has no effect when in 100BASE-FX mode.
6	1000BASE-X Half-Duplex (1000BASE-X) / Reserved (SGMII media interface)	RO	0x0	0x0	1000BASE-X Mode 1 = Link partner capable of 1000BASE-X half-duplex. 0 = Link partner not capable of 1000BASE-X half-duplex. SGMII media interface Mode Reserved This bit has no effect when in 100BASE-FX mode.
5	1000BASE-X Full-Duplex (1000BASE-X) / Reserved (SGMII media interface)	RO	0x0	0x0	1000BASE-X Mode 1 = Link partner capable of 1000BASE-X full-duplex. 0 = Link partner not capable of 1000BASE-X full-duplex. SGMII media interface Mode Reserved This bit has no effect when in 100BASE-FX mode.
4:0	Reserved	RO	0x00	0x00	Reserved

Table 48: Auto-Negotiation Expansion Register - Copper Page 0, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x000	0x000	Reserved. Must be 00000000000.
4	Parallel Detection Fault	RO,LH	0x0	0x0	Register 6_0.4 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function
3	Link Partner Next page Able	RO	0x0	0x0	Register 6_0.3 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	0x1	0x1	Register 6_0.2 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Local Device is Next Page able 0 = Local Device is not Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6_0.1 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	Register 6_0.0 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 49: Auto-Negotiation Expansion Register - Fiber
Page 1, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	Reserved. Must be 00000000000.
3	Link Partner Next page Able	RO	0x0	0x0	Register 6_0.3 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. This bit has no meaning when in SGMII media interface or 100BASE_FX mode. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	Always 1	Always 1	This bit has no meaning when in SGMII media interface or 100BASE_FX mode. 1 = Local Device is Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6_1.1 is not valid until the Auto-Negotiation complete bit (Reg 1_1.5) indicates completed. 1 = A New Page has been received 0 = A New Page has not been received This bit has no effect when in 100BASE-FX mode.
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	Register 6_1.0 is not valid until the Auto-Negotiation complete bit (Reg 1_1.5) indicates completed. This bit has no meaning when in SGMII media interface or 100BASE_FX mode. 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 50: Next Page Transmit Register - Copper Page 0, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7_0 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Link fail will clear Reg 7_0. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Note

Register 7_0 is valid only when register 16_2.9:7 = 001, 010, 011, or 101

Table 51: Next Page Transmit Register - Fiber Page 1, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7_1 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Link fail will clear Reg 7_1. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Note

Register 7_1 is valid only when register 16_2.9:7 = 011 or 111

Table 52: Link Partner Next Page Register - Copper
Page 0, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Note

Register 8_0 is valid only when register 16_2.9:7 = 001, 010, 011, or 101

Table 53: Link Partner Next Page Register - Fiber
Page 1, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Note

Register 8_1 is valid only when register 16_2.9:7 = 011 or 111

Table 54: 1000BASE-T Control Register
Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Test Mode	R/W	0x0	Retain	TX_CLK comes from the RX_CLK pin for jitter testing in test modes 2 and 3. After exiting the test mode, hardware reset or software reset (Register 0.15) should be issued to ensure normal operation. A restart of Auto-Negotiation will clear these bits. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved
12	MASTER/ SLAVE Manual Configuration Enable	R/W	0x0	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration
11	MASTER/ SLAVE Configuration Value	R/W	0x1	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE
10	Port Type	R/W	0x1	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. Register 9_0.10 is ignored if Register 9_0.12 is equal to 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)

Table 54: 1000BASE-T Control Register (Continued)
Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
9	1000BASE-T Full-Duplex	R/W	0x1	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
8	1000BASE-T Half-Duplex	R/W	0x1	Retain	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15, 0_1.15, or 0_2.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 0_1.11, or 0_2.11) transitions from power down to normal operation Copper link goes down. 1 = Advertise 0 = Not advertised
7:0	Reserved	R/W	0x00	Retain	0

Table 55: 1000BASE-T Status Register
Page 0, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MASTER/ SLAVE Configuration Fault	RO,LH	0x0	0x0	This register bit will clear on read. 1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected
14	MASTER/ SLAVE Configuration Resolution	RO	0x0	0x0	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE
13	Local Receiver Status	RO	0x0	0x0	1 = Local Receiver OK 0 = Local Receiver is Not OK
12	Remote Receiver Status	RO	0x0	0x0	1 = Remote Receiver OK 0 = Remote Receiver Not OK
11	Link Partner 1000BASE-T Full-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T full-duplex 0 = Link Partner is not capable of 1000BASE-T full-duplex

Table 55: 1000BASE-T Status Register (Continued)
Page 0, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Link Partner 1000BASE-T Half-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T half-duplex 0 = Link Partner is not capable of 1000BASE-T half-duplex
9:8	Reserved	RO	0x0	0x0	Reserved
7:0	Idle Error Count	RO, SC	0x00	0x00	MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.

Table 56: Extended Status Register
Page 0,1, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 15_0.15/15_1.15 x1x 1 else 0 1 =1000BASE-X full-duplex capable 0 = not 1000BASE-X full-duplex capable
14	1000BASE-X Half-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 15_0.14/15_1.14 x1x 1 else 0 1 =1000BASE-X half-duplex capable 0 = not 1000BASE-X half-duplex capable
13	1000BASE-T Full-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 15_0.13/15_1.13 001 1 010 1 011 1 101 1 else 0 1 =1000BASE-T full-duplex capable 0 = not 1000BASE-T full-duplex capable

Table 56: Extended Status Register (Continued)
Page 0,1, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
12	1000BASE-T Half-Duplex	RO	See Descr	See Descr	Value in this register is set as follows: Value in 16_2.9:7 15_0.12/15_1.12 001 1 010 1 011 1 101 1 else 0 1 =1000BASE-T half-duplex capable 0 = not 1000BASE-T half-duplex capable
11:0	Reserved	RO	0x000	0x000	000000000000

Table 57: Copper Specific Control Register 1
Page 0, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Disable Link Pulses	R/W	0x0	0x0	1 = Disable Link Pulse 0 = Enable Link Pulse
14:12	Downshift counter	R/W	0x6	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1x, 2x, ...8x is the number of times the PHY attempts to establish Gigabit link before the PHY downshifts to the next highest speed. 000 = 1x 100 = 5x 001 = 2x 101 = 6x 010 = 3x 110 = 7x 011 = 4x 111 = 8x
11	Downshift Enable	R/W	0x0	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1 = Enable downshift. 0 = Disable downshift.
10	Force Copper Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. In 1000BASE-T mode this has no effect. 1 = Force link good 0 = Normal operation
9:8	Energy Detect	R/W	0x0	Update	0x = Off 10 = Sense only on Receive (Energy Detect) 11 = Sense and periodically transmit NLP (Energy Detect+TM)

Table 57: Copper Specific Control Register 1 (Continued)
Page 0, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
7	Enable Extended Distance	R/W	0x0	Retain	When using cable exceeding 100m, the 10BASE-T receive threshold must be lowered in order to detect incoming signals. 1 = Lower 10BASE-T receive threshold 0 = Normal 10BASE-T receive threshold
6:5	MDI Crossover Mode	R/W	0x3	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Reserved	R/W	0x0	Retain	Write 0
3	Copper Transmitter Disable	R/W	0x0	Retain	1 = Transmitter Disable 0 = Transmitter Enable
2	Reserved	R/W	0x0	Retain	Write 0
1	Polarity Reversal	R/W	0x0	Retain	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled
0	Disable Jabber	R/W	0x0	Retain	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function

Table 58: Fiber Specific Control Register 1
Page 1, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	Write 0000
11	FEFI Enable	R/W	0x0	Retain	100BASE-FX FEFI 1 = Enable 0 = Disable
10	Force Fiber Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. 1 = Force link good 0 = Normal operation

Table 58: Fiber Specific Control Register 1 (Continued)
Page 1, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
9	SIGDET Polarity	R/W	0x0	Retain	0 = SIGDET high means signal, low means no signal 1 = SIGDET low means signal, high means no signal
8:4	Reserved	R/W	0x00	Retain	Write 00000
3	Fiber Transmitter Disable	R/W	0x0	Retain	1 = Transmitter Disable 0 = Transmitter Enable
2:0	Reserved	R/W	0x0	Retain	Write 000

Table 59: MAC Specific Control Register 1
Page 2, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Transmit FIFO Depth	R/W	0x0	Retain	1000BASE-T 10/100BASE-T 00 = +/- 16 Bits 00 = +/- 8 Bits 01 = +/- 24 Bits 01 = +/- 12 Bits 10 = +/- 32 Bits 10 = +/- 16 Bits 11 = +/- 40 Bits 11 = +/- 20 Bits
13:12	Receive FIFO Depth	R/W	0x0	Retain	1000BASE-T 10/100BASE-T 00 = +/- 16 Bits 00 = +/- 8 Bits 01 = +/- 24 Bits 01 = +/- 12 Bits 10 = +/- 32 Bits 10 = +/- 16 Bits 11 = +/- 40 Bits 11 = +/- 20 Bits
11:10	Autoselect preferred media	R/W	0x0	Retain	00 = No Preference for Media 01 = Preferred Fiber Medium 10 = Preferred Copper Medium 11 = Reserved
9:7	Mode select		0x0	0x0	000 = 100BASE-FX 001 = Copper GBIC 010 = Auto Copper/SGMII media interface 011 = Auto Copper/1000BASE-X 100 = Reserved 101 = Copper only 110 = SGMII media interface only 111 = 1000BASE-X only Upon hardware reset bits 9:7 takes on the following values MODE[1:0] bits 9:7 00 000 01 001 10 010 11 011
6:4	Reserved	R/W	0x0	Retain	Write 000

Table 59: MAC Specific Control Register 1 (Continued)
Page 2, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SGMII MAC Interface Power Down	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. This bit determines whether the SGMII MAC interface powers down when Register 0_0.11, 0_1.11, or 0_2.11 are used to power down the device or when the PHY enters the energy detect state. 1 = Always power up 0 = Can power down
2	Enhanced SGMII	R/W	0x0	Update	1 = Pass flow control bits through SGMII Auto-Negotiation 0 = Do not pass flow control bits through SGMII Auto-Negotiation
1:0	Reserved	R/W	0x0	Retain	Write 00

Table 60: LOS, INIT, STATUS[1:0] Function Control Register
Page 3, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	LOS Control	R/W	0x0	Retain	If 16_3.11:9 is set to 110 then 16_3.15:12 has no effect 0000 = Normal LOS operation 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - 10Mb/s or 1000Mb/s Master, Off - Else 0111 = On - Fiber Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
11:8	INIT Control	R/W	0x2	Retain	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = Normal INIT operation 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - 10/1000Mb/s Link, Off - Else 0111 = On - 10Mb/s Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 1101 = MODE 2 1110 = Interrupt 1111 = Reserved
7:4	STATUS[1] Control	R/W	0x1	Retain	If 16_3.3:2 is set to 11 then 16_3.7:4 has no effect 0000 = On - Copper Link, Off - Else 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - 100Mb/s Link or Fiber Link, Off - Else 0110 = On - 100/1000Mb/s Link, Off - Else 0111 = On - 100Mb/s Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved

Table 60: LOS, INIT, STATUS[1:0] Function Control Register (Continued)
Page 3, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	STATUS[0] Control	R/W	0xE	Retain	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000Mb/s 2 blinks - 100Mb/s 1 blink - 10Mb/s 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000Mb/s Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 1101 = MODE 2 1110 = MODE 3 1111 = MODE 4

Table 61: Non-Volatile Memory Address Register
Page 4, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Slave Address	R/W	0x00	Retain	Slave Address
8	Read/Write	R/W	0x1	Retain	A write to 16_4 will initiate a read or write command on the two-wire interface if the two-wire interface is free, otherwise the read or write command will be ignored. Make sure register 17_4.10:8 is not equal to 010 (command in progress) prior to writing register 16_4. A read to 16_4 will not trigger any action. Register 18_4.7:0 must be set to the value to be written prior to issuing a write command. 1 = Read, 0 = Write
7:0	Byte Address	R/W	0x00	Retain	Byte Address

Table 62: MDI[0] Virtual Cable Tester™ Status Register
Page 5, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Run VCT™ Test	R/W, SC	0x0	Retain	Page 5 registers 16, 17, 18, 19 bits 14:0 are valid only after the completion of VCT (16_5.15 is 0). 1 = Run VCT test 0 = VCT test completed
14:13	Status	RO	0x0	Retain	MDI[0] +/- VCT test result 00 = Valid test, normal cable (no short or open in cable) 01 = Valid test, short in cable (Impedance < 33 ohms) 10 = Valid test, open in cable (Impedance greater than 330 ohms) 11 = Test Fail
12:8	Amplitude	RO	0x00	Retain	Amplitude of reflection on pair MDI[0]+/-. These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude (+1) 0x10 = Zero amplitude 0x00 = Maximum negative amplitude (-1)
7:0	Distance	RO	0x00	Retain	Approximate distance (+/- 1m) to the open/short location on Pair MDI[0]+/-, measured at nominal conditions (room temperature and typical VDDs). Please see the VCT How to Use TDR Results application note for distance to fault details.

Table 63: Packet Generation
Page 6, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	R/W	0x000	Retain	Write 0000000000
5	Enable Stub Test	R/W	0x0	Retain	1 = Enable stub test 0 = Normal Operation
4	Enable CRC checker	R/W	0x0	Retain	1 = Enable CRC checker 0 = Disable/reset CRC checker
3	Enable Packet Generator	R/W	0x0	Retain	1 = Enable packet generator 0 = Normal Operation
2	Payload of packet to transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = 5A,A5,5A,A5,...
1	Length of packet to transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes

Table 63: Packet Generation (Continued)
Page 6, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
0	Transmit an Errored packet	R/W	0x0	Retain	1 = Tx packets with CRC errors & Symbol Error 0 = No error

Table 64: Copper Specific Status Register 1
Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x0	Retain	These status bits are valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled, ignore this bit. 1 = Resolved 0 = Not resolved
10	Copper Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable

Table 64: Copper Specific Status Register 1
Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
7	Fiber/Copper resolution	RO	0x0	Retain	Bit indicates the resolution of the Fiber/Copper Auto Detection. This bit is valid only when 17_0.3 = 1. This register is identical to 17_1.7. 1 = Fiber link 0 = Copper link
6	MDI Crossover Status	RO	0x0	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI
5	Downshift Status	RO	0x0	0x0	1 = Downshift 0 = No Downshift
4	Copper Energy Detect Status	RO	0x0	0x0	1 = No copper energy detected 0 = Copper energy detected
3	Global Link Status	RO	0x0	0x0	This register is identical to 17_1.3 1 = Fiber link is up or Copper link is up 0 = Fiber link is down and Copper link is down
2	DTE power status	RO	0x0	Retain	1 = Link partner needs DTE power 0 = Link partner does not need DTE power
1	Polarity (real time)	RO	0x0	0x0	1 = Reversed 0 = Normal
0	Jabber (real time)	RO	0x0	0x0	1 = Jabber 0 = No jabber

Table 65: Fiber Specific Status Register 1
Page 1, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	100 FX Speed	RO	See Descr.	See Descr.	For the SGMII Media Interface Mode, see 5_1.11:10 for the speed status. Value in this register is set as follows: Value in 16_2.9:7 17_1.15:14 000 01 else 00 01 =100 FX mode value 00 = default for all other modes (reserved)
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set to 1 when Auto-Negotiation is completed, Auto-Negotiation is disabled or when using 100 FX mode. This status bit follows the value of 0_1.8 for 100 FX mode. This bit is not valid in SGMII Media Interface Mode. See 5_1.12 for this status. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	When using 100 FX mode, this bit is always 0. This bit is not valid in SGMII Media Interface Mode. 1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled or using 100 FX mode, ignore this bit. This bit is not valid in SGMII media interface mode. 1 = Resolved 0 = Not resolved
10	1000BASE-X/ 100 FX Link (real time)	RO	0x0	0x0	This bit is not valid in SGMII media interface mode. See 5_1.15 for this status. 1 = Link up 0 = Link down
9	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is not valid in SGMII media interface mode. 1 = Transmit pause enabled 0 = Transmit pause disable

Table 65: Fiber Specific Status Register 1 (Continued)
Page 1, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is not valid in SGMII media interface mode. 1 = Receive pause enabled 0 = Receive pause disabled
7	Fiber/Copper resolution	RO	0x0	Retain	Bit indicates the resolution of the Fiber/Copper Auto Detection. This bit is valid only when 17_1.3 = 1. This register is identical to 17_0.7. 1 = Fiber link 0 = Copper link
6	Reserved	RO	Always 0	Always 0	0
5	1000BASE-X/ SGMII media interface Auto-Negotiation bypass status	RO	0x0	Retain	1 = 1000BASE-X/SGMII media interface came up because bypass mode timer timed out and fiber Auto-Negotiation was bypassed. 0 = 1000BASE-X/SGMII media interface came up because regular fiber Auto-Negotiation completed. If the bypass logic brings up the SGMII media interface link, gigabit speed will be passed to the MAC.
4	Autoselect Fiber Energy Detect Status	RO	0x1	0x1	This bit is valid only when auto detect is enabled. 1 = No Fiber energy detected (also the default for all other modes) 0 = Fiber energy detected
3	Global Link Status	RO	0x0	0x0	This register is identical to 17_0.3 1 = Fiber link is up or Copper link is up 0 = Fiber link is down and Copper link is down
2:0	Reserved	RO	Always 000	Always 000	000

Table 66: MAC Specific Status Register 1
Page 2, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	Always 000	Always 000	0000000000
5	SGMII MAC interface Auto-Negotiation bypass status	RO	0x0	Retain	1 = SGMII MAC interface came up because bypass mode timer timed out and fiber Auto-Negotiation was bypassed. 0 = SGMII MAC interface came up because regular fiber Auto-Negotiation completed. If the bypass logic brings up the SGMII MAC interface link, copper Auto-Negotiation will restart and advertise only gigabit speed.
4:0	Reserved	RO	Always 00	Always 00	00000

Table 67: LOS, INIT, STATUS[1:0] Polarity Control Register
Page 3, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	LOS, STATUS[1] mix percentage	R/W	0x4	Retain	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0%, 0001 = 12.5%, ..., 0111 = 87.5%, 1000 = 100% 1001 to 1111 = Reserved
11:8	INIT, STATUS[0] mix percentage	R/W	0x4	Retain	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0%, 0001 = 12.5%, ..., 0111 = 87.5%, 1000 = 100% 1001 to 1111 = Reserved
7:6	LOS Polarity	R/W	0x2	Retain	00 = On - drive LOS low, Off - drive LOS high 01 = On - drive LOS high, Off - drive LOS low 10 = On - drive LOS low, Off - tristate LOS 11 = On - drive LOS high, Off - tristate LOS
5:4	INIT Polarity	R/W	0x2	Retain	00 = On - drive INIT low, Off - drive INIT high 01 = On - drive INIT high, Off - drive INIT low 10 = On - drive INIT low, Off - tristate INIT 11 = On - drive INIT high, Off - tristate INIT
3:2	STATUS[1] Polarity	R/W	0x0	Retain	00 = On - drive STATUS[1] low, Off - drive STATUS[1] high 01 = On - drive STATUS[1] high, Off - drive STATUS[1] low 10 = On - drive STATUS[1] low, Off - tristate STATUS[1] 11 = On - drive STATUS[1] high, Off - tristate STATUS[1]
1:0	STATUS[0] Polarity	R/W	0x0	Retain	00 = On - drive STATUS[0] low, Off - drive STATUS[0] high 01 = On - drive STATUS[0] high, Off - drive STATUS[0] low 10 = On - drive STATUS[0] low, Off - tristate STATUS[0] 11 = On - drive STATUS[0] high, Off - tristate STATUS[0]

Table 68: Non-Volatile Memory Read Data and Status Register Page 4, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	RAM Status	RO	0x0	0x0	Register 17_4.15:13 is the status in response to setting 18_4.11 to 1. Register 17_4.15:13 will remain at 010 until the command is completed. Once the command is completed the status 001, 100, 101, or 111 will remain until register 17_4 is read. The register will clear on read. If a new command is issue by writing register 18_4.11 without reading register 17_4 for a previous command, the status of the previous command will be lost. If a command initiated by writing register 18_4.11 to 1 is still in progress and a second command is issued, the status register 17_4.15:13 will reflect the first command. The second command is ignored but register 17_4.15:13 will not be set to 111. 000 = Ready 001 = Command completed successfully for all 256 bytes 010 = Command in progress 011 = Reserved 100 = Command completed successfully for first 128 bytes but at least one byte of second 128 bytes failed 101 = At least one byte of first 128 bytes failed 110 = Reserved 111 = Interface busy, command ignored
12:11	Reserved	RO	0x0	0x0	00

Table 68: Non-Volatile Memory Read Data and Status Register (Continued)
Page 4, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
10:8	TWI Status	RO, LH	0x0	0x0	Register 17_4.10:8 is the status in response to setting to writing register 16_4. Register 17_4.10:8 will remain at 010 until the command is completed. Once the command is completed the status 001, 011, 100, 101, or 111 will remain until register 17_4 is read. The register will clear on read. If a new command is issue by writing register 16_4 without reading register 17_4 for a previous command, the status of the previous command will be lost. If a command initiated by writing register 16_4 is still in progress and a second command is issued, the status register 17_4.10:8 will reflect the first command. The second command is ignored but register 17_4.10:8 will not be set to 111. Command Done - No Error is set when the I2C slave properly responds with ACK. In the case of a write command with automatic read back a Command Done - No Error status will be returned even if the read back data does not match the written data or if the I2C slave does not respond with ACK during the read back. Register 17_4.7:0 is valid only when register 17_4.10:8 is set to 001. 000 = Ready 001 = Command Done - No Error 010 = Command in Progress 011 = Write done but readback failed 100 = Reserved 101 = Command Failed 110 = Reserved 111 = two-wire interface Busy, Command Ignored
7:0	Read Data	RO	0x00	0x00	Read Data Register 17_4.7:0 is valid only when register 17_4.10:8 is set to 001.

Table 69: MDI[1] Virtual Cable Tester™ Status Register
Page 5, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Disable waiting period	R/W	0x0	Retain	1=Start VCT™ without waiting to bring link down 0=Wait for link down before starting VCT test
14:13	Status	RO	0x0	Retain	MDI[1] +/- VCT test result 00 = Valid test, normal cable (no short or open in cable) 01 = Valid test, short in cable (Impedance < 33 ohms) 10 = Valid test, open in cable (Impedance greater than 330 ohms) 11 = Test Fail
12:8	Amplitude	RO	0x00	Retain	Amplitude of reflection on pair MDI[1]+/-.These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude (+1) 0x10 = Zero amplitude 0x00 = Maximum negative amplitude (-1)
7:0	Distance	RO	0x00	Retain	Approximate distance (+/- 1m) to the open/short location on Pair MDI[1]+/-, measured at nominal conditions (room temperature and typical VDDs). Please see the VCT How to Use TDR Results application note for distance to fault details.

Table 70: CRC Counters
Page 6, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	CRC Packet Count	RO	0x00	Retain	0x00 = no packets received 0xFF = 256 packets received (max count). Bit 16_6.4 must be set to 1 in order for register to be valid.
7:0	CRC Error Count	RO	0x00	Retain	0x00=no CRC errors detected in the packets received. 0xFF = 256 CRC errors detected in the packets received (max count). Bit 16_6.4 must be set to 1 in order for register to be valid.

Table 71: Interrupt Enable Register - Copper
Page 0, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Auto-Negotiation Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
14	Copper Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Copper Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Copper Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Copper Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Copper Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Copper Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	Copper False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	Reserved	R/W	0x0	Retain	0
6	MDI Crossover Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
5	Downshift Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 71: Interrupt Enable Register - Copper (Continued)
Page 0, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
4	Energy Detect Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
3	Reserved	R/W	0x0	Retain	Always write 00
2	DTE power detection status changed interrupt enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1	Polarity Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Jabber Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 72: Interrupt Enable Register - Fiber
Page 1, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	Always 00	Always 00	00
13	Fiber Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Fiber Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Fiber Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Fiber Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 72: Interrupt Enable Register - Fiber (Continued)
Page 1, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
9	Fiber Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	Fiber False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7:5	Reserved	RO	Always 000	Always 000	000
4	Fiber Energy Detect Interrupt Enable	R/W	0x0	Retain	Register 1.0018.4 has effect only when auto-media detect is enabled. 1 = Interrupt enable 0 = Interrupt disable
3:0	Reserved	RO	Always 0000	Always 0000	Always 0000

Table 73: Interrupt Enable Register - MAC
Page 2, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	Always 00	Always 00	00000000
7	FIFO Over/ Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6:0	Reserved	RO	Always 00	Always 00	0000000

Table 74: LOS, INIT, STATUS[1:0] Timer Control Register
Page 3, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	0
14:12	Pulse stretch duration	R/W	0x4	Retain	000 = no pulse stretching 001 = 21 ms to 42ms 010 = 42 ms to 84ms 011 = 84 ms to 170ms 100 = 170 ms to 340ms 101 = 340 ms to 670ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
11	Reserved	R/W	0x0	Retain	0
10:8	Blink Rate	R/W	0x1	Retain	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7:4	Reserved	R/W	0x0	Retain	0000
3:2	Speed Off Pulse Period	R/W	0x1	Retain	00 = 84ms 01 = 170ms 10 = 340ms 11 = 670ms
1:0	Speed On Pulse Period	R/W	0x1	Retain	00 = 84ms 01 = 170ms 10 = 340ms, 11 = 670ms

Table 75: Non-Volatile Memory Write Data and Control Register
Page 4, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	EEPROM Write Time	R/W	0xA	Retain	0000 = EEPROM takes 0ms to write 0001 = 1.05ms .... 1110 = 14.68ms 1111 = 15.73ms

Table 75: Non-Volatile Memory Write Data and Control Register (Continued)
Page 4, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
11:10	Reload EEPROM values	R/W, SC	0x0	Retain	Status presented in 17_4.10:8. Note that the EEPROM must never set 18_4.11:10 to 11. 0x = Normal 10 = Reload RAM only 11 = Reload RAM and re initialize PHY registers
9	Automatic read back after write	R/W	0x0	Retain	If read back is enabled then data will always be read back after a write. The read data is stored in register 17_4.7:0 1 = Read back, 0 = no read back
8	Reserved	R/W	0x0	Retain	0
7:0	Write Data	R/W	0x00	Retain	Write Data

Table 76: MDI[2] Virtual Cable Tester™ Status Register
Page 5, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	Reserved
14:13	Status	RO	0x0	Retain	MDI[2] +/- VCT™ test result 00 = Valid test, normal cable (no short or open in cable) 01 = Valid test, short in cable (Impedance < 33 ohms) 10 = Valid test, open in cable (Impedance greater than 330 ohms) 11 = Test Fail
12:8	Amplitude	RO	0x00	Retain	Amplitude of reflection on pair MDI[2]+/-.These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude 0x10 = Zero amplitude 0x00 = Maximum negative amplitude
7:0	Distance	RO	0x00	Retain	Approximate distance (+/- 1m) to the open/short location on Pair MDI[2]+/-, measured at nominal conditions (room temperature and typical VDDs). Please see the VCT How to Use TDR Results application note for distance to fault details.

Table 77: Copper Specific Status Register 2
Page 0, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Auto-Negotiation Error	RO,LH	0x0	0x0	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation Error 0 = No Auto-Negotiation Error
14	Copper Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Copper Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed
12	Copper Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Copper Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Copper Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Copper Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	Copper False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7	Reserved	RO	Always 0	Always 0	0
6	MDI Crossover Changed	RO,LH	0x0	0x0	1 = Crossover changed 0 = Crossover not changed
5	Downshift Interrupt	RO,LH	0x0	0x0	1 = Downshift detected 0 = No down shift
4	Energy Detect Changed	RO,LH	0x0	0x0	1 = Energy Detect state changed 0 = No Energy Detect state change detected
3	Reserved	RO	Always 0	Always 0	0
2	DTE power detection status changed interrupt	RO,LH	0x0	0x0	1 = DTE power detection status changed 0 = No DTE power detection status change detected

Table 77: Copper Specific Status Register 2 (Continued)
Page 0, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
1	Polarity Changed	RO,LH	0x0	0x0	1 = Polarity Changed 0 = Polarity not changed
0	Jabber	RO,LH	0x0	0x0	1 = Jabber 0 = No jabber

Table 78: Fiber Specific Status Register 2
Page 1, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	Always 00	Always 00	00
13	1000BASE-X Duplex Changed	RO,LH	0x0	0x0	This bit is not valid in SGMII media interface mode. 1 = Duplex changed 0 = Duplex not changed
12	1000BASE-X Page Received	RO,LH	0x0	0x0	This bit is not valid in SGMII media interface mode. 1 = Page received 0 = Page not received
11	1000BASE-X Auto-Negotiation Completed	RO,LH	0x0	0x0	This bit is not valid in SGMII media interface mode. 1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	1000BASE-X Link Status Changed	RO,LH	0x0	0x0	This bit is not valid in SGMII media interface mode. 1 = Link status changed 0 = Link status not changed
9	1000BASE-X Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	1000BASE-X False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7:5	Reserved	RO	Always 000	Always 000	000
4	1000BASE-X Energy Detect Changed	RO,LH	0x0	0x0	1 = Fiber Energy Detect state changed 0 = No Fiber Energy Detect state change detected
3:0	Reserved	RO	Always 0000	Always 0000	0000

Table 79: MAC Specific Status Register 2
Page 2, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	Always 00	Always 00	00000000
7	FIFO Over/ Underflow	RO,LH	0x0	0x0	1 = Over/Underflow Error 0 = No FIFO Error
6:0	Reserved	RO	Always 00	Always 00	0000000

Table 80: Non-Volatile Memory Write Data and Control Register
Page 4, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	00000000
7:0	RAM data	R/W	xx	Retain	A read to this register will place the value in the RAM into 19_4.7:0. The RAM location is specified by 20_4.7:0. Register 20_4.7:0 should be set correctly prior to accessing register 19_4.

Table 81: MDI[3] Virtual Cable Tester™ Status Register
Page 5, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	Reserved
14:13	Status	RO	0x0	Retain	MDI[3] +/- VCT™ test result 00 = Valid test, normal cable (no short or open in cable) 01 = Valid test, short in cable (Impedance < 33 ohms) 10 = Valid test, open in cable (Impedance greater than 330 ohms) 11 = Test Fail
12:8	Amplitude	RO	0x00	Retain	Amplitude of reflection on pair MDI[3]+/-.These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude 0x10 = Zero amplitude 0x00 = Maximum negative amplitude
7:0	Distance	RO	0x00	Retain	Approximate distance (+/- 1m) to the open/short location on Pair MDI[3]+/-, measured at nominal conditions (room temperature and typical VDDs). Please see the VCT How to Use TDR Results application note for distance to fault details.

Table 82: Non-Volatile Memory Address Register
Page 4, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	00000000
7:0	RAM Byte Address	R/W	0x00	Retain	RAM Byte Address

Table 83: 1000 BASE-T Pair Skew Register
Page 5, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Pair 7,8 (MDI[3]+/-)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within +/- 8ns. The contents of 20_5.15:0 are valid only if Register 21_5.6 = 1
11:8	Pair 4,5 (MDI[2]+/-)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within +/- 8ns.
7:4	Pair 3,6 (MDI[1]+/-)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within +/- 8ns.
3:0	Pair 1,2 (MDI[0]+/-)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within +/- 8ns.

Table 84: Receive Error Counter Register
Page 0,1, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported.

Table 85: 1000 BASE-T Pair Swap and Polarity
Page 5, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	
6	Register 21_4 and 21_5 valid	RO	0x0	0x0	The contents of 21_5.15:0 are valid only if Register 28_5.6 = 1 1= Valid . 0 = Invalid
5	C, D Crossover	RO	0x0	0x0	1 = Channel C received on MDI[2]+/- Channel D received on MDI[3]+/- 0 = Channel D received on MDI[2]+/- Channel C received on MDI[3]+/-
4	A, B Crossover	RO	0x0	0x0	1 = Channel A received on MDI[0]+/- Channel B received on MDI[1]+/- 0 = Channel B received on MDI[0]+/- Channel A received on MDI[1]+/-
3	Pair 7,8 (MDI[3]+/-) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
2	Pair 4,5 (MDI[2]+/-) Polarity		0x0	0x0	1 = Negative 0 = Positive
1	Pair 3,6 (MDI[1]+/-) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
0	Pair 1,2 (MDI[0]+/-) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive

Table 86: Page Address
Page Any, Register 22

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Disable/Enable Automatic Medium Register Selection	R/W	0x1	Retain	1 = Enable automatic medium register selection 0 = Disable automatic medium register selection
14:8	Reserved	RO	Always 00	Always 00	0000000
7:0	Page select for registers 0 to 28	R/W	0x00	Retain	Page Number

Table 87: Copper Specific Control Register 2
Page 0, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Transmitter type	R/W	0x0	Retain	0 = Class B, 1 = Class A
14:9	Reserved	R/W	0x00	Retain	Write 000000
8	DTE detect enable	R/W	0x0	Retain	1 = Enable DTE detection 0 = Disable DTE detection
7:4	DTE detect status drop hysteresis	R/W	0x4	Retain	0000: report immediately 0001: report 5s after DTE power status drop ... 1111: report 75s after DTE power status drop
3:2	100 MB test select	R/W	0x0	Retain	0x = Normal Operation 10 = Select 112 ns sequence 11 = Select 16 ns sequence
1	10 BT polarity force	R/W	0x0	Retain	1 = Force negative polarity 0 = Normal Operation
0	Reserved	R/W	0x0	Retain	Write 0

Table 88: Fiber Specific Control Register 2
Page 1, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X/ SGMII media interface Auto-Negotiation bypass enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. 1 = Enable Bypass 0 = Disable Bypass
14:13	SGMII media interface Auto-Negotiation Timer	R/W	0x0	Retain	00 = 1.6 to 2.0ms 01 = 0.50 to 0.60us 10 = 0.98 to 1.2us 11 = 2.1 to 2.3us
12:8	Reserved	R/W	0x00	Retain	Write 00000
7	Enable External Fiber Signal Detect Input	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by a software reset to take effect. 1 = Use external hardware pins for signal detect 0 = Force signal detect to be good
6:3	Reserved	R/W	0x0	Retain	Write 0000
2:0	1000BASE-X / SGMII media interface Output Amplitude (100 ohm differential load)	R/W	0x3	Retain	0.50V - 1.20V = Differential voltage peak-to-peak measured with 100 ohm differential load. 000 = 0.50V, 001 = 0.60V, 010 = 0.70V, 011 = 0.80V, 100 = 0.90V, 101 = 1.00V, 110 = 1.10V, 111 = 1.20V

Table 89: MAC Specific Control Register 2
Page 2, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SGMII MAC interface Auto-Negotiation bypass enable	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. 1 = Enable Bypass 0 = Disable Bypass
14:13	SGMII MAC interface Auto-Negotiation Timer	R/W	0x0	Retain	00 = 1.6 to 2.0ms 01 = 0.50 to 0.60us 10 = 0.98 to 1.2us 11 = 2.1 to 2.3us
12:8	Reserved	R/W	0x00	Retain	Write 00000
7	Force fiber link down when copper link down	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by a software reset to take effect. This bit has effect only if 0_2.12 is set to 0 (Auto-Negotiation off). 0 = Fiber sends idles when copper link down 1 = Fiber send zeros when copper link down
6:5	Reserved	R/W	0x0	Retain	Write 00
4	SGMII MAC interface Clock Enable	R/W	See Descr	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. Upon hardware reset this bit defaults as follows: SGMII_CLK bit 26_2.4 0 0 1 1 0 = Clock Disable 1 = Clock Enable
3	Reserved	R/W	0x0	Retain	Write 0
2:0	SGMII MAC interface Output Amplitude (100 ohm differential load)	R/W	0x0	Retain	0.50V - 1.20V = Differential voltage peak-to-peak measured with 100 ohm differential load. 000 = 0.50V, 001 = 0.60V, 010 = 0.70V, 011 = 0.80V, 100 = 0.90V, 101 = 1.00V, 110 = 1.10V, 111 = 1.20V

Table 90: VCT™ DSP Distance
Page 5, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	R/W	0x0000	0x0000	0000000000000
2:0	Cable Length (1000 mode only)	RO	0x0	0x0	Cable length measurement is only a rough estimate. Actual value depends on the attenuation of the cable, output levels of the remote transceiver, connector impedance, etc. 000 = < 50m 001 = 50 - 80m 010 = 80 - 110m 011 = 110 - 140m 100 = greater than 140m

Section 4.Electrical Specifications

4.1. Absolute Maximum Ratings[1]

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
V_{DDA}	Power Supply Voltage on VDDA with respect to VSS		TBD		V
V_{DDAL}	Power Supply Voltage on VDDAL with respect to VSS		TBD		V
V_{DDAH}	Power Supply Voltage on VDDAH with respect to VSS		TBD		V
V_{TT}	Power Supply Voltage on F_VTT and S_VTT with respect to VSS		TBD		V
V_{DD}	Power Supply Voltage on DVDD with respect to VSS		TBD		V
V_{DDO}	Power Supply Voltage on VDDO with respect to VSS		TBD		V
V_{PIN}	Voltage applied to any digital input pin	TBD		TBD	V
$T_{STORAGE}$	Storage temperature	-55		+125[2]	°C

1. On power-up, no special power supply sequencing is required.
2. 125 °C is only used as bake temperature for not more than 24 hours. Long term storage (e.g weeks or longer) should be kept at 85 °C or lower.

4.2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDA}[1]	VDDA supply	For VDDA	2.35	2.5	2.65	V
V_{DDAL}[1]	VDDAL supply	For VDDAL 1.5V	1.43	1.5	1.58	V
		For VDDAL 2.5V	2.35	2.5	2.65	V
V_{DDAH}[1]	VDDAH supply	For VDDAH	2.35	2.5	2.65	V
V_{TT}[1]	F_VTT and S_VTT supply	For F_VTT and S_VTT	0.95		1.57	V
V_{DD}[1]	DVDD supply	For DVDD	1.14	1.2	1.26	V
V_{DDO}[1]	VDDO supply	For VDDO (If Oscillator is used at the XTAL1 input)	1.4	1.5	1.58	V
	VDDO supply	For VDDO (If crystal is used at the XTAL1 and XTAL2 inputs)	2.375	2.5	2.65	V
RSET	Internal bias reference	Resistor connected to V_{SS}		5000 ± 1% Tolerance		Ω
T_A	Commercial Ambient operating temperature		0		70[2]	°C
T_J	Maximum junction temperature				125[3]	°C

1. Maximum noise allowed on supplies is 50 mV peak-peak.
2. The important parameter is maximum junction temperature. As long as the maximum junction temperature is not exceeded, the device can be operated at any ambient temperature. Refer to White Paper on "TJ Thermal Calculations" for more information.
3. Refer to white paper on TJ Thermal Calculations for more information.

4.3. Package Thermal Information

Table 91: Thermal Conditions for 64-Pin QFN Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance - junction to ambient for the 88E1112 device 64-Pin QFN package $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		24.50		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		21.40		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		20.40		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		19.80		°C/W
ψ_{JT}	Thermal characteristic parameter[a] - junction to top center of the 88E1112 device 64-Pin QFN package $\psi_{JT} = (T_J - T_{top})/P$. P = Total power dissipation, T_{top}: Temperature on the top center of the package.	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.23		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.32		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.39		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		0.44		°C/W
θ_{JC}	Thermal resistance[a] - junction to case for the 88E1112 device 64-Pin QFN package $\theta_{JC} = (T_J - T_C)/ P_{top}$ P_{top} = Power dissipation from the top of the package	JEDEC with no air flow		9.21		°C/W
θ_{JB}	Thermal resistance[a] - junction to board for the 88E1112 device 64-Pin QFN package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		12.29		°C/W

4.4. Current Consumption

4.4.1 Current Consumption VDDO

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{VDDO}	1.5V, or 2.5V I/O Supply	VDDO	Power Down		0		mA
			Energy Detect (Mode 1)		0		mA
			Energy Detect+™ (Mode 2)		0		mA
			No Link (sleep mode disabled)		1		mA
			10BASE-T Tx/Rx over SGMII		0		mA
			Idle, 10 Mbps		0		mA
			100BASE-TX Tx/Rx over SGMII		0		mA
			Idle, 100 Mbps		0		mA
			100BASE-FX Tx/Rx over SGMII		--		mA
			Idle, 100 Mbps		--		mA
			1000BASE-T Tx/Rx over SGMII		1		mA
			Idle, 1000 Mbps		1		mA
			Fiber over SGMII 1000 Mbps		1		mA
			Fiber over SGMII; Idle 1000 Mbps		1		mA

4.4.2 Current Consumption VDDAH

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{VDDAH}	2.5V Power to analog core	VDDAH	Power Down		15		mA
			Energy Detect (Mode 1)		28		mA
			Energy Detect+^{TM} (Mode 2)		28		mA
			No Link (sleep mode disabled)		28		mA
			10BASE-T Tx/Rx over SGMII		15		mA
			Idle, 10 Mbps		15		mA
			100BASE-TX Tx/Rx over SGMII		15		mA
			Idle, 100 Mbps		15		mA
			100BASE-FX Tx/Rx over SGMII		--		mA
			Idle, 100 Mbps		--		mA
			1000BASE-T Tx/Rx over SGMII		15		mA
			Idle, 1000 Mbps		15		mA
			Fiber over SGMII 1000 Mbps		28		mA
			Fiber over SGMII; Idle 1000 Mbps		28		mA

4.4.3 Current Consumption VDDAL

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{VDDAL}	1.5V or 2.5V power to analog core (1.5V or 2.5V current consumption will be the same)	VDDAL	Power Down		16		mA
			Energy Detect (Mode 1)		24		mA
			Energy Detect+™ (Mode 2)		24		mA
			No Link (sleep mode disabled)		24		mA
			10BASE-T Tx/Rx over SGMII		16		mA
			Idle, 10 Mbps		16		mA
			100BASE-TX Tx/Rx over SGMII		16		mA
			Idle, 100 Mbps		16		mA
			100BASE-FX Tx/Rx over SGMII		--		mA
			Idle, 100 Mbps		--		mA
			1000BASE-T Tx/Rx over SGMII		16		mA
			Idle, 1000 Mbps		16		mA
			Fiber over SGMII 1000 Mbps		24		mA
			Fiber over SGMII; Idle 1000 Mbps		24		mA

4.4.4 Current Consumption VDDA (Center Tap)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{VDDA}	2.5V analog supply	VDDA	Power Down		4		mA
			Energy Detect (Mode 1)		8		mA
			Energy Detect+™ (Mode 2)		8		mA
			No Link (sleep mode disabled)		24		mA
			10BASE-T Tx/Rx over SGMII		103		mA
			Idle, 10 Mbps		45		mA
			100BASE-TX Tx/Rx over SGMII		76		mA
			Idle, 100 Mbps		76		mA
			100BASE-FX Tx/Rx over SGMII		--		mA
			Idle, 100 Mbps		--		mA
			1000BASE-T Tx/Rx over SGMII		239		mA
			Idle, 1000 Mbps		240		mA
			Fiber over SGMII 1000 Mbps		20		mA
			Fiber over SGMII; Idle 1000 Mbps		20		mA

4.4.5 Current Consumption DVDD

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{DVDD}	1.2V digital supply	DVDD	Power Down		17		mA
			Energy Detect (Mode 1)		16		mA
			Energy Detect+^{TM} (Mode 2)		16		mA
			No Link (sleep mode disabled)		25		mA
			10BASE-T Tx/Rx over SGMII		21		mA
			Idle, 10 Mbps		23		mA
			100BASE-TX Tx/Rx over SGMII		43		mA
			Idle, 100 Mbps		45		mA
			100BASE-FX Tx/Rx over SGMII		--		mA
			Idle, 100 Mbps		--		mA
			1000BASE-T Tx/Rx over SGMII		295		mA
			Idle, 1000 Mbps		277		mA
			Fiber over SGMII 1000 Mbps		25		mA
			Fiber over SGMII; Idle 1000 Mbps		27		mA

4.4.6 Current Consumption F_VTT

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{F_VTT}	1000BASE-X Output Supply	F_VTT	Fiber over SGMII		24		mA
			Fiber over SGMII; Idle		24		mA

4.4.7 Current Consumption S_VTT

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I_{S_VTT}	SGMII MAC Interface Output Supply	S_VTT	Power Down		17		mA
			Energy Detect (Mode 1)		23		mA
			Energy Detect+™ (Mode 2)		23		mA
			No Link (sleep mode disabled)		24		mA
			10BASE-T Tx/Rx over SGMII		17		mA
			Idle, 10 Mbps		17		mA
			100BASE-TX Tx/Rx over SGMII		17		mA
			Idle, 100 Mbps		17		mA
			100BASE-FX Tx/Rx over SGMII		--		mA
			Idle, 100 Mbps		--		mA
			1000BASE-T Tx/Rx over SGMII		17		mA
			Idle, 1000 Mbps		17		mA

4.5. DC Operating Conditions

4.5.0.1 Digital Pins

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VIH	Input high voltage	All digital inputs					V
			VDDO = 2.5V	1.75			V
			VDDO = 1.5V	1.05			V
VIL	Input low voltage	All digital inputs					
			VDDO = 2.5V			0.75	V
			VDDO = 1.5V			0.45	V
VOH	High level output voltage	All digital outputs	IOH = -8 mA	VDDO - 0.4V			V
VOL	Low level output voltage	All digital outputs	IOL = 8 mA			0.4	V
I_{ILK}	Input leakage current	With internal pull-up resistor				10 -50	uA
		All others without resistor				10	uA
CIN	Input capacitance	All pins				5	pF

4.5.1 Internal Resistor Description

64-QFN Pin #	Pin Name	Resistor
51	POL_RST	Internal Pull-up
49	NORMAL	Internal Pull-up

4.5.2 IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.
-10BASE-T IEEE 802.3 Clause 14
-100BASE-TX ANSI X3.263-1995

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	MDIP/N[1:0]	10BASE-T no cable	2.2	2.5	2.8	V
		MDIP/N[1:0]	10BASE-T cable model	585[1]			mV
		MDIP/N[1:0]	100BASE-TX mode	0.950	1.0	1.050	V
		MDIP/N[3:0]	1000BASE-T[2]	0.67	0.75	0.82	V
	Overshoot[2]	MDIP/N[1:0]	100BASE-TX mode	0		5%	V
	Amplitude Symmetry (positive/ negative)	MDIP/N[1:0]	100BASE-TX mode	0.98x		1.02x	V+/V-
V_{IDIFF}	Peak Differential Input Voltage	MDIP/N[1:0]	10BASE-T mode	585[3]			mV
	Signal Detect Assertion	MDIP/N[1:0]	100BASE-TX mode	1000	460[4]		mV peak-peak
	Signal Detect De-assertion	MDIP/N[1:0]	100BASE-TX mode	200	360[5]		mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. IEEE 802.3ab Figure 40 -19 points A&B.
3. The input test is actually a template test ; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The 88E1112 device will accept signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI-PMD specification requires that any received signal with peak-to-peak differential amplitide less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The Alaska Single will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

4.5.3 Fiber and MAC Interface

4.5.3.1 Transmitter DC Characteristics

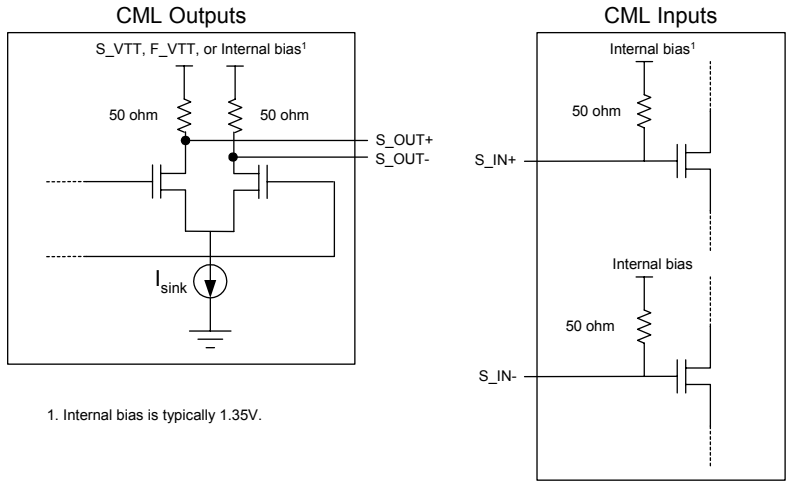
Symbol	Parameter[1]	Min	Typ	Max	Units
V_{OH}	Output Voltage High			1625	mV
V_{OL}	Output Voltage Low	875			mV
V_{RING}	Output Ringing			10	mV
$\|V_{OD}\|^2$	Output Voltage Swing (differential, peak)	Programmable - see Table 92.			mV peak
V_{OS}	Output Offset Voltage (also called Common mode voltage)	Variable - see 4.5.3.2 for details.			mV
R_O	Output Impedance (single-ended) (50 ohm termination)	40		60	Ω
Delta R_O	Mismatch in a pair			10	%
Delta V_{OD}	Change in V_{OD} between 0 and 1			25	mV
Delta V_{OS}	Change in V_{OS} between 0 and 1			25	mV
I_{S+}, I_{S-}	Output current on short to VSS			40	mA
I_{S+-}	Output current when S_OUT+ and S_OUT- are shorted			12	mA
I_{X+}, I_{X-}	Power off leakage current			10	mA

1. See Section 2.21.4.1 for details. Parameters are measured with outputs AC connected with 100 ohm differential load.
2. Output amplitude is programmable by writing to Register 26.2:0.

Table 92: Programming SGMII Output Amplitude

Register 26_2 and/or 26_1 Bits	Field	Description
2:0	1000BASE-X / SGMII Media Interface Output Amplitude (100 ohm differential load)	0.50V - 1.20V = Differential voltage peak-to-peak measured with 100 ohm differential load. 000 = 0.50V 001 = 0.60V 010 = 0.70V 011 = 0.80V 100 = 0.90V 101 = 1.00V 110 = 1.10V 111 = 1.20V

Figure 29: CML I/Os



1. Internal bias is typically 1.35V.

4.5.3.2 Common Mode Voltage (Voffset) Calculations

There are four different main configurations for the SGMII/Fiber interface connections. These are:

- DC connection to an LVDS receiver
- AC connection to an LVDS receiver
- DC connection to an CML receiver
- AC connection to an CML receiver

If AC coupling or DC coupling to an LVDS receiver is used, the DC output levels are determined by the following:

- Internal bias, or S_VTT or F_VTT, whichever option is used. See section 2.1.1 "MAC Interface" and Figure 29 for details. (If VDDAL is used to generate the internal bias, the internal bias value will typically be 1.4V.)
- The output voltage swing is programmed by Register 26_2.2:0 (see Table 92).

Voffset(i.e., common mode voltage) = AVDDT (or internal bias) - single-ended peak-peak voltage swing. See Figure 30 for details.

If DC coupling is used with a CML receiver, then the DC levels will be determined by a combination of the MACs output structure and the 88E1112 input structure shown in the CML Inputs diagram in Figure 31. Assuming the same MAC CML voltage levels and structure, the common mode output levels will be determined by:

Voffset(i.e., common mode voltage) = AVDDT (or internal bias) - single-ended peak-peak voltage swing/2. See Figure 31 for details.

If DC coupling is used, the output voltage DC levels are determined by the AC coupling considerations above, plus the I/O buffer structure of the MAC.

Figure 30: AC connections (CML or LVDS receiver) or DC connection LVDS receiver

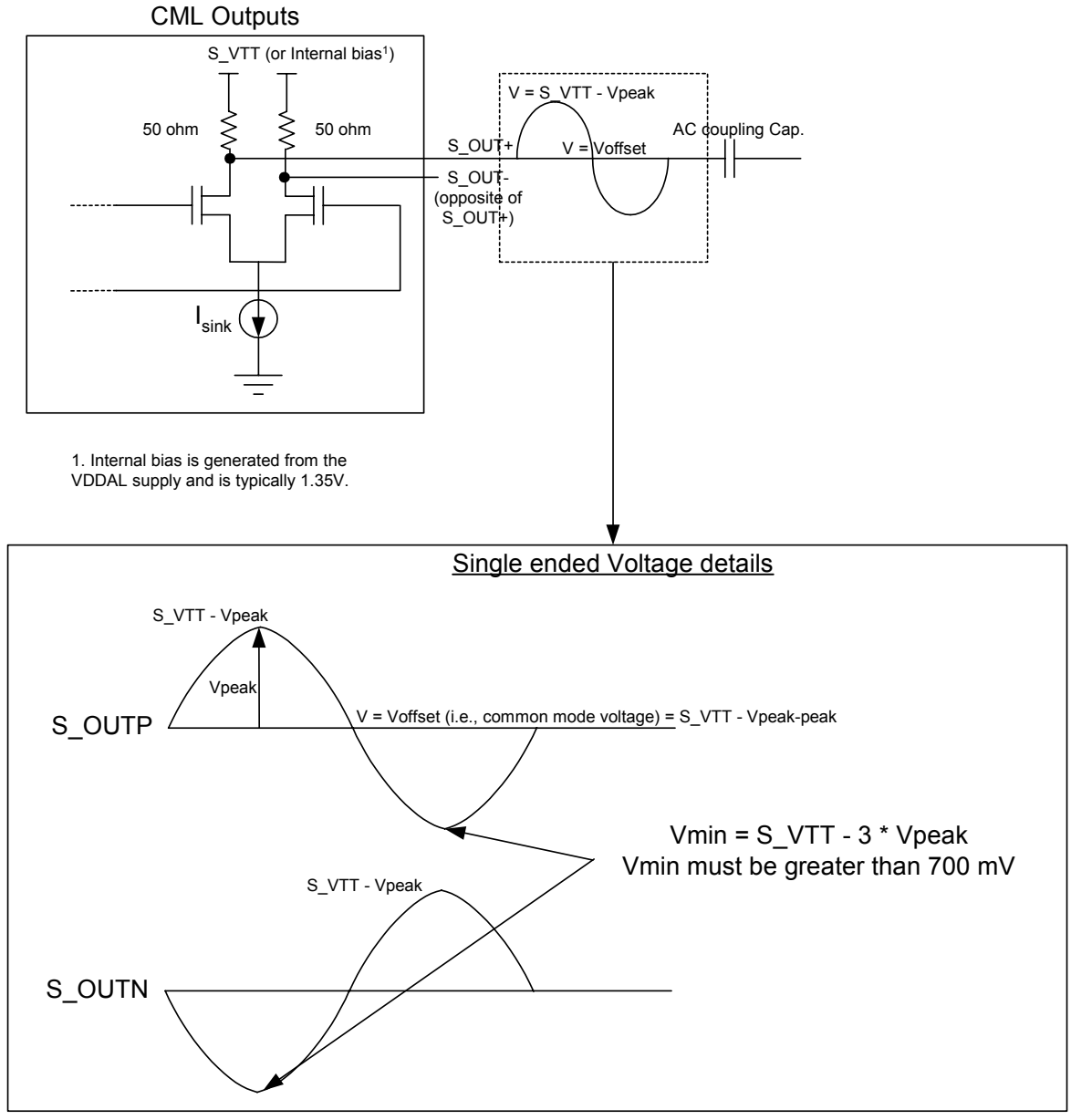
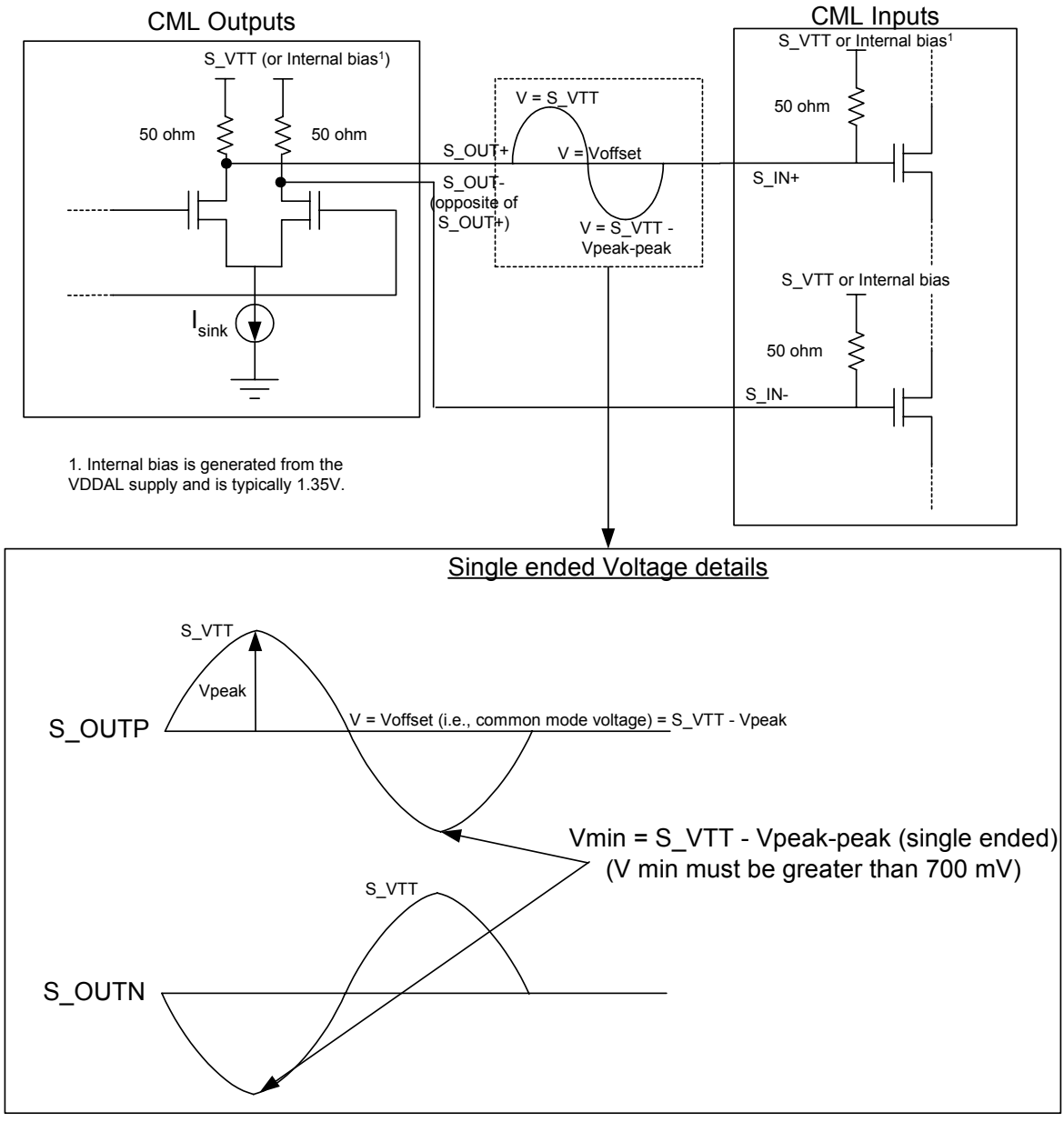


Figure 31: DC connection to a CML receiver

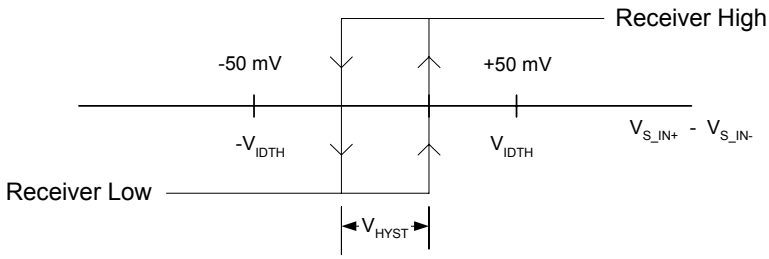


4.5.3.3 Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_I	Input DC Voltage range S_IN+ or S_IN-	675		1725	mV
V_{IDTH}[1]	Input Differential Threshold |S_IN+ - S_IN-|, |SD+ - SD-|	200		2100	mV (peak-peak differential)
V_{HYST}[1]	Input Differential Hysteresis	25			mV
R_{IN}	Receiver 100 ohm Differential Input Impedance	80		120	ohm

1. Receiver is at high level when VS_IN+ - VS_IN- is greater than VIDTH(min) and is at low level when VS_IN+ - VS_IN- is less than -VIDTH(min). A minimum hysteresis of VHYST is present between -VIDTH and +VIDTH as shown in the figure. When the fiber link is down, an offset is applied to prevent false signal detect due to noise. When the fiber link is up, the offset circuit is disabled.

Figure 32: Input Differential Hysteresis



4.6. AC Electrical Specifications

4.6.1 Reset Timing

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESET de-asserted		10			ms
T_{SU_XTAL1}	Number of valid XTAL1 cycles prior to RESET de-asserted		10			clks
T_{RESET}	Minimum reset pulse width during normal operation		10			ms

Figure 33: Reset Timing (Active Low)

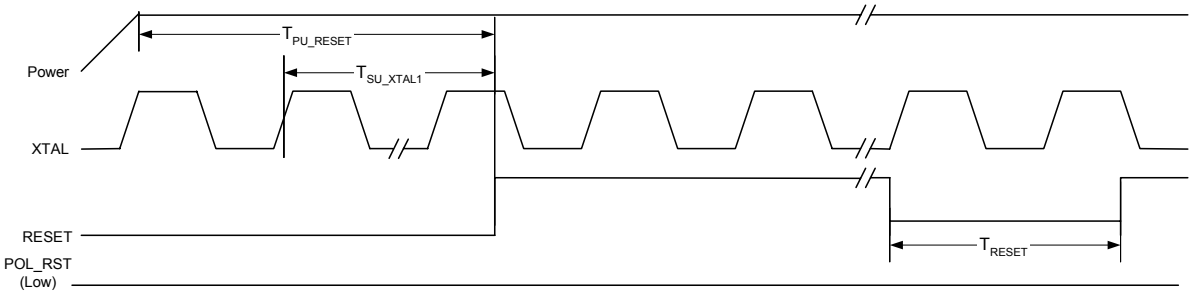


Figure 34: Reset Timing (Active High)

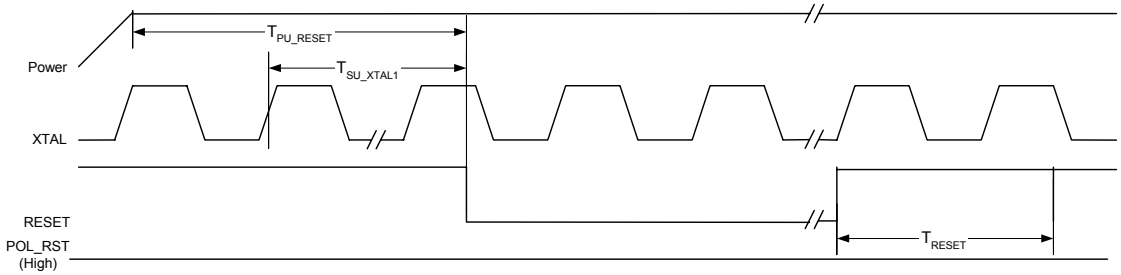


Figure 35: Reset Timing (Controlled by POL_RST)

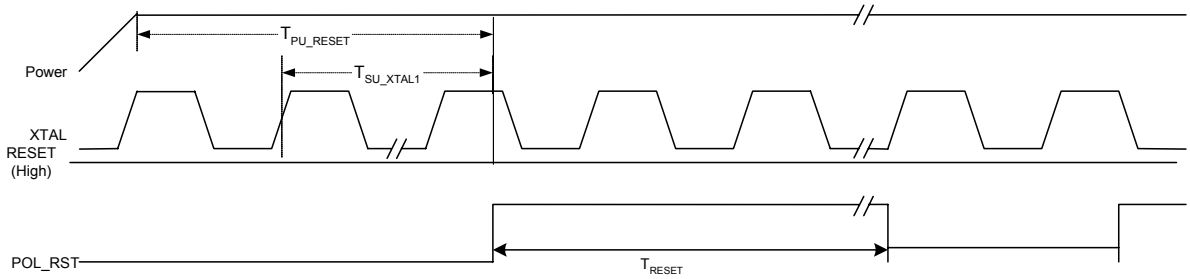
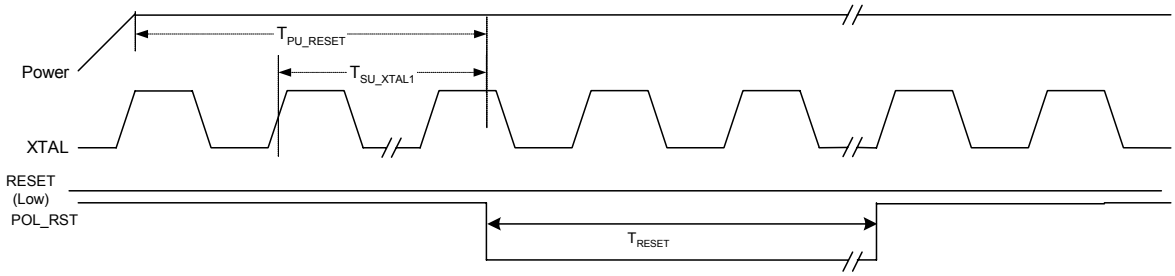


Figure 36: Reset Timing (Controlled by POL_RST)



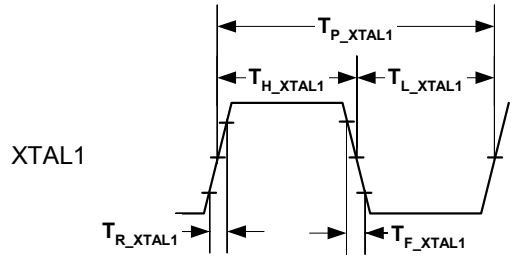
4.6.2 XTAL1/XTAL2 Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_XTAL1}	XTAL1 Period		40 -50 ppm	40	40 +50 ppm	ns
T_{H_XTAL1}	XTAL1 High time		13	20	27	ns
T_{L_XTAL1}	XTAL1 Low time		13	20	27	ns
T_{R_XTAL1}	XTAL1 Rise	10% to 90%	-	-	3.0	ns
T_{F_XTAL1}	XTAL1 Fall	90% to 10%	-	-	3.0	ns
T_{J_XTAL1}	XTAL1 total jitter[1]		-	-	200	ps[2]

1. PLL generated clocks are not recommended as input to XTAL1 since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
2. Broadband peak-peak = 200 ps, Broadband rms = 3 ps, 12 kHz to 20 MHz rms = 1 ps.

Figure 37: XTAL1/XTAL2 Timing

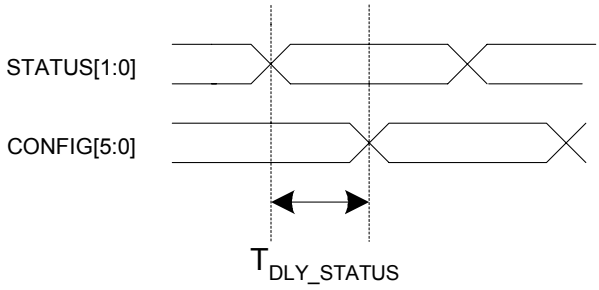


4.6.3 STATUS[1:0] to CONFIG[5:0] Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_STATUS}[1]	STATUS to CONFIG Delay		0		25	ns

1. Maximum delay allowed on any external logic added between STATUS [1:0] and CONFIG[5:0]

Figure 38: STATUS to CONFIG Timing



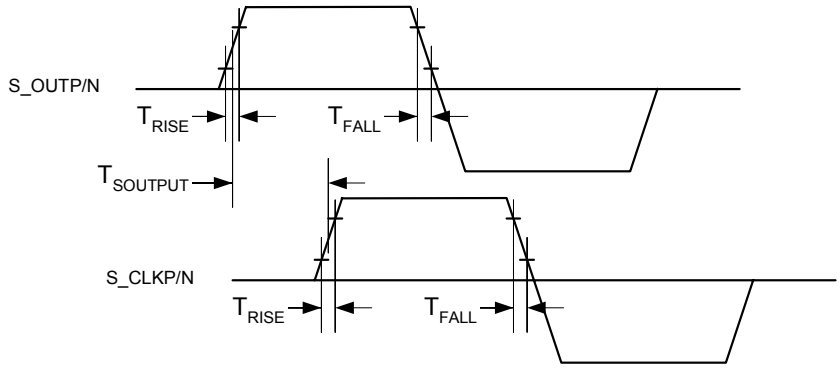
4.7. SGMII MAC Interface Timing

4.7.1 Serial Interface and SGMII Output AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_{FALL}	V_{OD} Fall time (20% - 80%)	100		200	ps
T_{RISE}	V_{OD} Rise time (20% - 80%)	100		200	ps
CLOCK	Clock signal duty cycle @ 625 MHz	48		52	%
T_{SKEW1}[1]	Skew between two members of a differential pair			20	ps
$T_{SOUTPUT}$[2]	SERDES output to RxClk_P/N	360	400	440	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14*rms Random)		127		ps

1. Skew measured at 50% of the transition.
2. Measured at 50% of the transition.

Figure 39: Serial Interface Rise and Fall Times



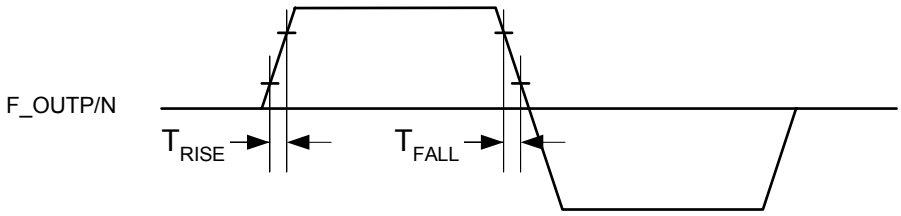
4.7.2 Serial Interface and SGMII Input AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14*rms Random)			599	ps

4.8. 1000BASE-X,SGMII Media Interface and 100BASE-FX Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{FALL}	VOD Fall time (20% - 80%)	100		200	ps
T_{RISE}	VOD Rise time (20% - 80%)	100		200	ps

Figure 40: 1000BASE-X and SGMII Media Interface Rise and Fall Times



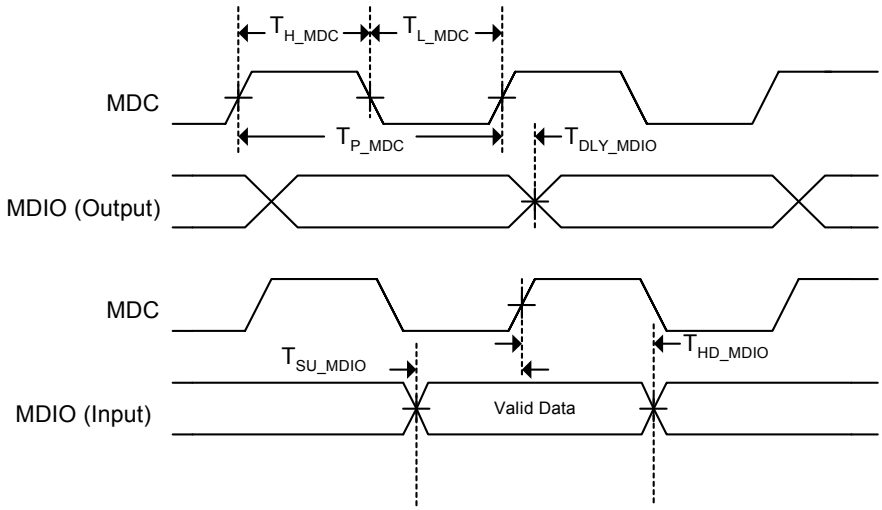
4.9. MDC/MDIO Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time		0		20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time		10			ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time		10			ns
T_{P_MDC}	MDC Period		120			ns[1]
T_{H_MDC}	MDC High		30			ns
T_{L_MDC}	MDC Low		30			ns

1. Maximum frequency = 8.333 MHz.

Figure 41: MDC/MDIO Timing

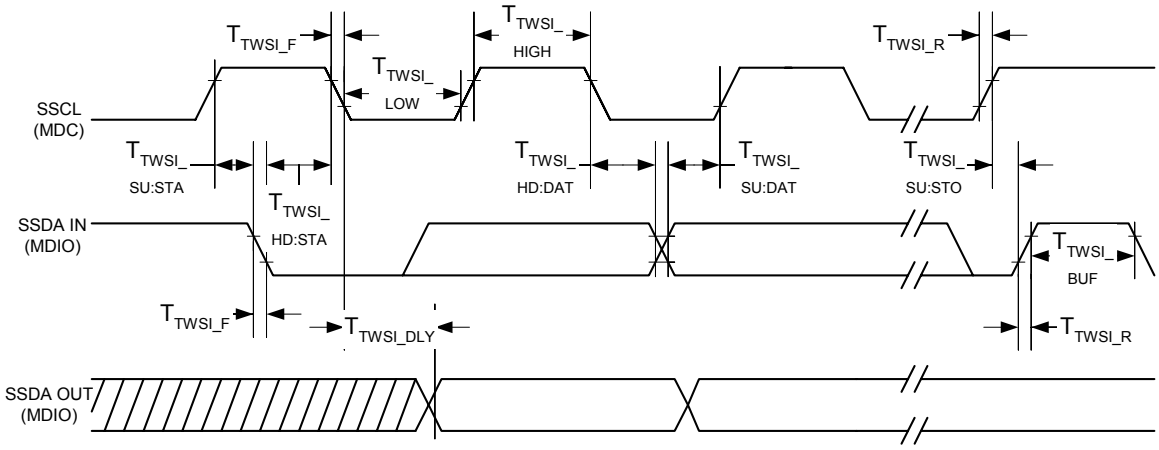


4.10. Two-Wire Serial Interface (Slave) Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{TWSI_SSCL}	SSCL Clock Frequency	100 kHz			100	kHz
		400 kHz			400	
T_{TWSI_NS}	Noise Suppression Time at SSCL, SSDA Inputs	100 kHz			80	ns
		400 kHz			80	
T_{TWSI_R}	SSCL/SSDA Rise time	100 kHz			1000	ns
		400 kHz			300	
T_{TWSI_F}	SSCL/SSDA Fall Time	100 kHz			300	ns
		400 kHz			300	
T_{TWSI_HIGH}	Clock High Period	100 kHz	4000			ns
		400 kHz	600			
T_{TWSI_LOW}	Clock Low Period	100 kHz	4700			ns
		400 kHz	1300			
$T_{TWSI\_SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	100 kHz	4700			ns
		400 kHz	600			
$T_{TWSI\_HD:STA}$	Start Condition Hold Time	100 kHz	4000			ns
		400 kHz	600			
$T_{TWSI\_SU:STO}$	Stop Condition Setup Time	100 kHz	4000			ns
		400 kHz	600			
$T_{TWSI\_SU:DAT}$	Data in Setup Time	100 kHz	250			ns
		400 kHz	100			
$T_{TWSI\_HD:DAT}$	Data in Hold Time	100 kHz	300			ns
		400 kHz	300			
T_{TWSI_BUF}	Bus Free Time	100 kHz	4700			ns
		400 kHz	1300			
T_{TWSI_DLY}	SSCL Low to SSDA Data Out Valid	100 kHz	40		200	ns
		400 kHz	40		200	

Figure 42: TWSI Slave Timing

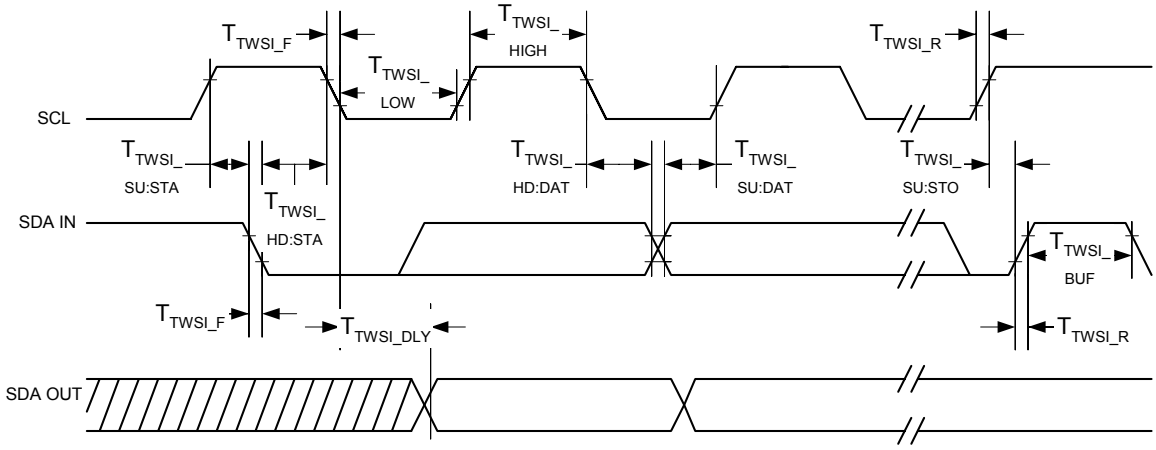


4.11. Two-Wire Serial Interface (Master) Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{TWSI_SCL}	SSCL Clock Frequency	100 kHz				kHz
T_{TWSI_NS}	Noise Suppression Time at SSDA Inputs	100 kHz			80	ns
T_{TWSI_R}	SSCL/SSDA Rise time	100 kHz			1000	ns
T_{TWSI_F}	SSCL/SSDA Fall Time	100 kHz			300	ns
T_{TWSI_HIGH}	Clock High Period	100 kHz				ns
T_{TWSI_LOW}	Clock Low Period	100 kHz				ns
$T_{TWSI\_SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	100 kHz				ns
$T_{TWSI\_HD:STA}$	Start Condition Hold Time	100 kHz				ns
$T_{TWSI\_SU:STO}$	Stop Condition Setup Time	100 kHz				ns
$T_{TWSI\_SU:DAT}$	Data in Setup Time	100 kHz				ns
$T_{TWSI\_HD:DAT}$	Data in Hold Time	100 kHz				ns
T_{TWSI_BUF}	Bus Free Time	100 kHz				ns
T_{TWSI_DLY}	SSCL Low to SSDA Data Out Valid	100 kHz				ns

Figure 43: TWSI Master Timing



4.12. IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:
-10BASE-T IEEE 802.3 Clause 14-2000
-100BASE-TX ANSI X3.263-1995
-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall Time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
$T_{RISE/TFALL}$ Symmetry		MDIP/N[1:0]	100BASE-TX	0		0.5	ns
DCD	Duty Cycle Distortion	MDIP/N[1:0]	100BASE-TX	0		0.5[1]	ns, peak-peak
Transmit Jitter		MDIP/N[1:0]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3

4.13. Latency Timing

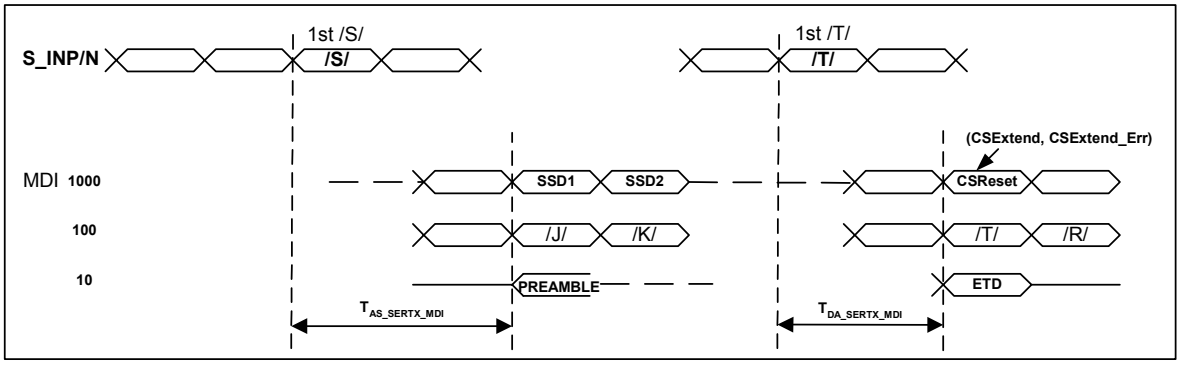
4.13.1 SGMII MAC Interface/GBIC to 10/100/1000BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SERTX\_MDI\_1000}$	S_INP/N Start of Packet / S/ to MDI SSD1		124[1]		148	ns
$T_{DA\_SERTX\_MDI\_1000}$	S_INP/N /T/ to MDI CSReset, CSExtend, CSExtend_Err		124[1,2]		148	ns
$T_{AS\_SERTX\_MDI\_100}$	S_INP/N Start of Packet / S/ to MDI /J/		250[1]		310	ns
$T_{DA\_SERTX\_MDI\_100}$	S_INP/N /T/ to MDI /T/		250[1,2]		310	ns
$T_{AS\_SERTX\_MDI\_10}$	S_INP/N Start of Packet / S/ to MDI Preamble		1200[1]		2000	ns
$T_{DA\_SERTX\_MDI\_10}$	S_INP/N /T/ to MDI ETD		1200[1,2]		2000	ns

1. Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and the received signal on S_INP/N. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 44: SGMII to 10/100/1000BASE-T Transmit Latency Timing



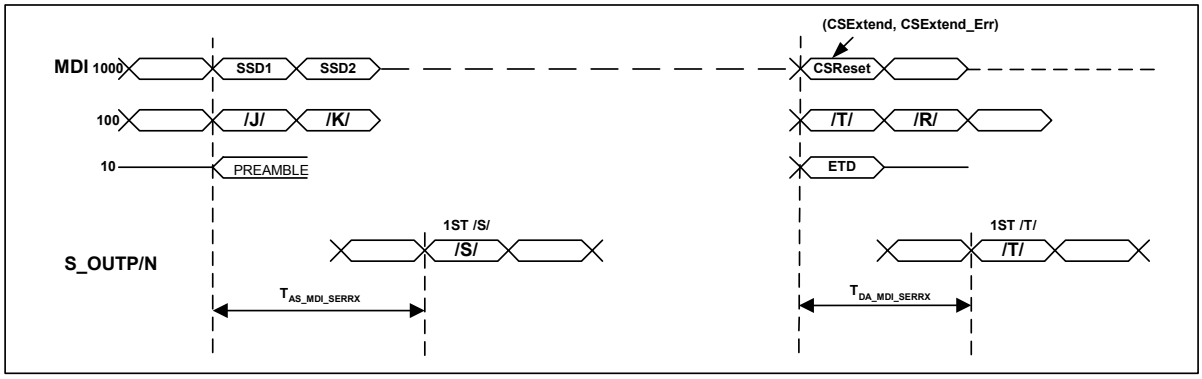
4.13.2 10/100/1000BASE-T to SGMII MAC Interface/GBIC Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_SERRX\_1000}$	MDI SSD1 to S_OUTP/N Start of Packet		248[1,2]		296	ns
$T_{DA\_MDI\_SERRX\_1000}$	MDI CSReset, CSExtend, CSExtend_Err to S_OUTP/N /T/		248[1,2,3]		296	ns
$T_{AS\_MDI\_SERRX\_100}$	MDI /J/ to S_OUTP/N Start of Packet		370[2]		434	ns
$T_{DA\_MDI\_SERRX\_100}$	MDI /T/ to S_OUTP/N /T/		370[2,3]		434	ns
$T_{AS\_MDI\_SERRX\_10}$	MDI Preamble to S_OUTP/N Start of Packet			2700[2,4]		ns
$T_{DA\_MDI\_SERRX\_10}$	MDI ETD to S_OUTP/N /T/			2700[2,3,4]		ns

1. In 1000BASE-T the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDIP/N[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
3. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on MDI and S_OUTP/N, which is based on XTAL1. The worst case variation will be outside these limits if there is a frequency difference.
4. Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

Figure 45: 10/100/1000BASE-T to SGMII Receive Latency Timing



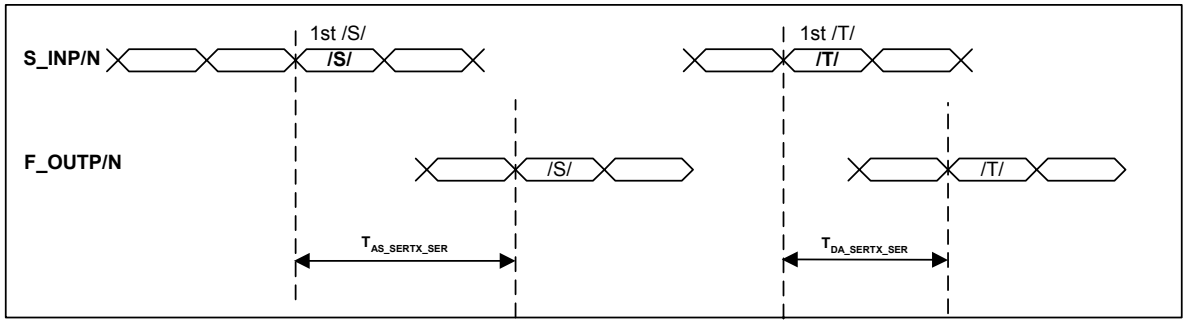
4.13.3 SGMII MAC Interface to SGMII Media Interface/1000BASE-X Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SERTX\_SER\_1000}$	S_INP/N Start of Packet /S/ to F_OUTP/N Start of Packet /S/ 1000 Mbps		TBD[1]		TBD	ns
$T_{DA\_SERTX\_SER\_1000}$	S_INP/N /T/ to F_OUTP/N /T/ 1000 Mbps		TBD[1,2]		TBD	ns
$T_{AS\_SERTX\_SER\_100}$	S_INP/N Start of Packet /S/ to F_OUTP/N Start of Packet /S/ 100 Mbps		TBD[1]		TBD	ns
$T_{DA\_SERTX\_SER\_100}$	S_INP/N /T/ to F_OUTP/N /T/ 100 Mbps		TBD[1,2]		TBD	ns
$T_{AS\_SERTX\_SER\_10}$	S_INP/N Start of Packet /S/ to F_OUTP/N Start of Packet /S/ 10 Mbps		TBD[1]		TBD	ns
$T_{DA\_SERTX\_SER\_10}$	S_INP/N /T/ to F_OUTP/N /T/ 10 Mbps		TBD[1,2]		TBD	ns

1. Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on F_OUTP/N and the received signal on S_INP/N. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 46: SGMII MAC Interface to SGMII Media Interface/1000BASE-X Transmit Latency Timing



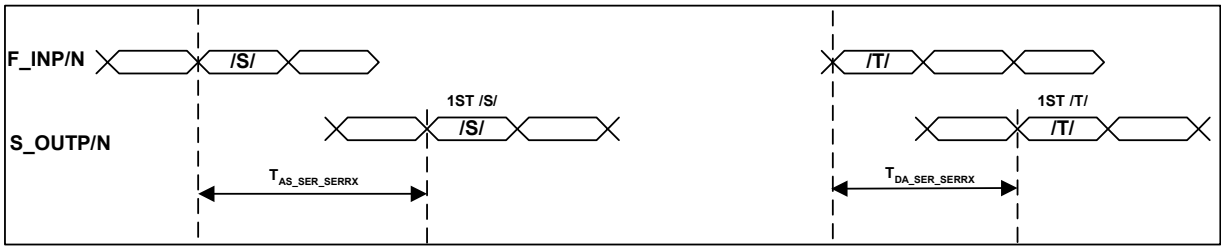
4.13.4 SGMII Media Interface/1000BASE-X to SGMII MAC Interface Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SER\_SERRX\_1000}$	F_INP/N Start of Packet to S_OUTP/N Start of Packet 1000 Mbps		TBD[1]	TBD	TBD	ns
$T_{DA\_SER\_SERRX\_1000}$	F_INP/N /T/ to S_OUTP/N /T/ 1000 Mbps		TBD[1,2]		TBD	ns
$T_{AS\_SER\_SERRX\_100}$	F_INP/N Start of Packet to S_OUTP/N Start of Packet 100 Mbps		TBD[2]		TBD	ns
$T_{DA\_SER\_SERRX\_100}$	F_INP/N /T/ to S_OUTP/N /T/ 100 Mbps		TBD[1,2]		TBD	ns
$T_{AS\_SER\_SERRX\_10}$	F_INP/N Start of Packet to S_OUTP/N Start of Packet 10 Mbps		TBD[1]	TBD	TBD	ns
$T_{DA\_SER\_SERRX\_10}$	F_INP/N /T/ to S_OUTP/N /T/ 10 Mbps		TBD[1,2]	TBD	TBD	ns

1. Assumes Register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
2. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on F_INP/N and S_OUTP/N, which is based on XTAL1. The worst case variation will be outside these limits if there is a frequency difference.

Figure 47: SGMII Media Interface/1000BASE-X to SGMII MAC Interface Receive Latency Timing



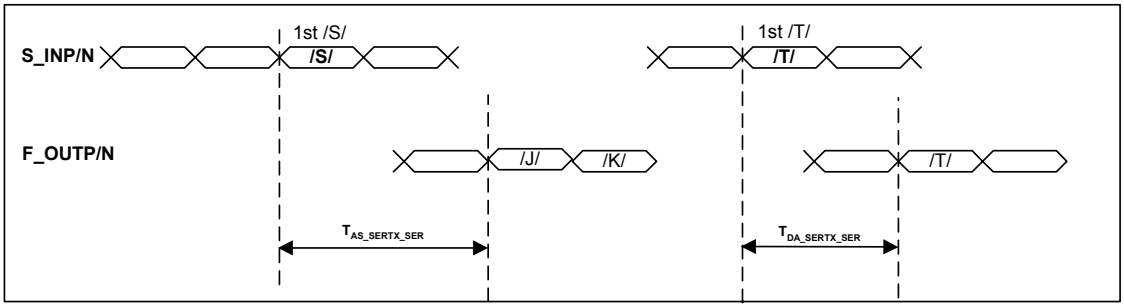
4.13.5 SGMII MAC Interface to 100BASE-FX Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SERTX\_SER}$	S_INP/N Start of Packet /S/ to F_OUTP/N Start of Packet /J/		TBD[1]		TBD	ns
$T_{DA\_SERTX\_SER}$	S_INP/N /T/ to F_OUTP/N /T/		TBD[1, 2]		TBD	ns

1. Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 40 ns of latency.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on F_OUTP/N and the received signal on S_INP/N. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 48: SGMII MAC Interface to 100BASE-FX Transmit Latency Timing



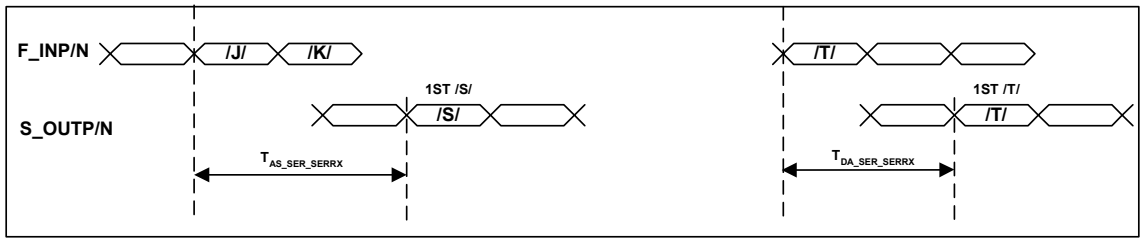
4.13.6 100BASE-FX to SGMII MAC Interface Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_SER\_SERRX}$	F_INP/N Start of Packet to S_OUTP/N Start of Packet		TBD[1]		TBD	ns
$T_{DA\_SER\_SERRX}$	F_INP/N /T/ to S_OUTP/N /T/		TBD[1,2]		TBD	ns

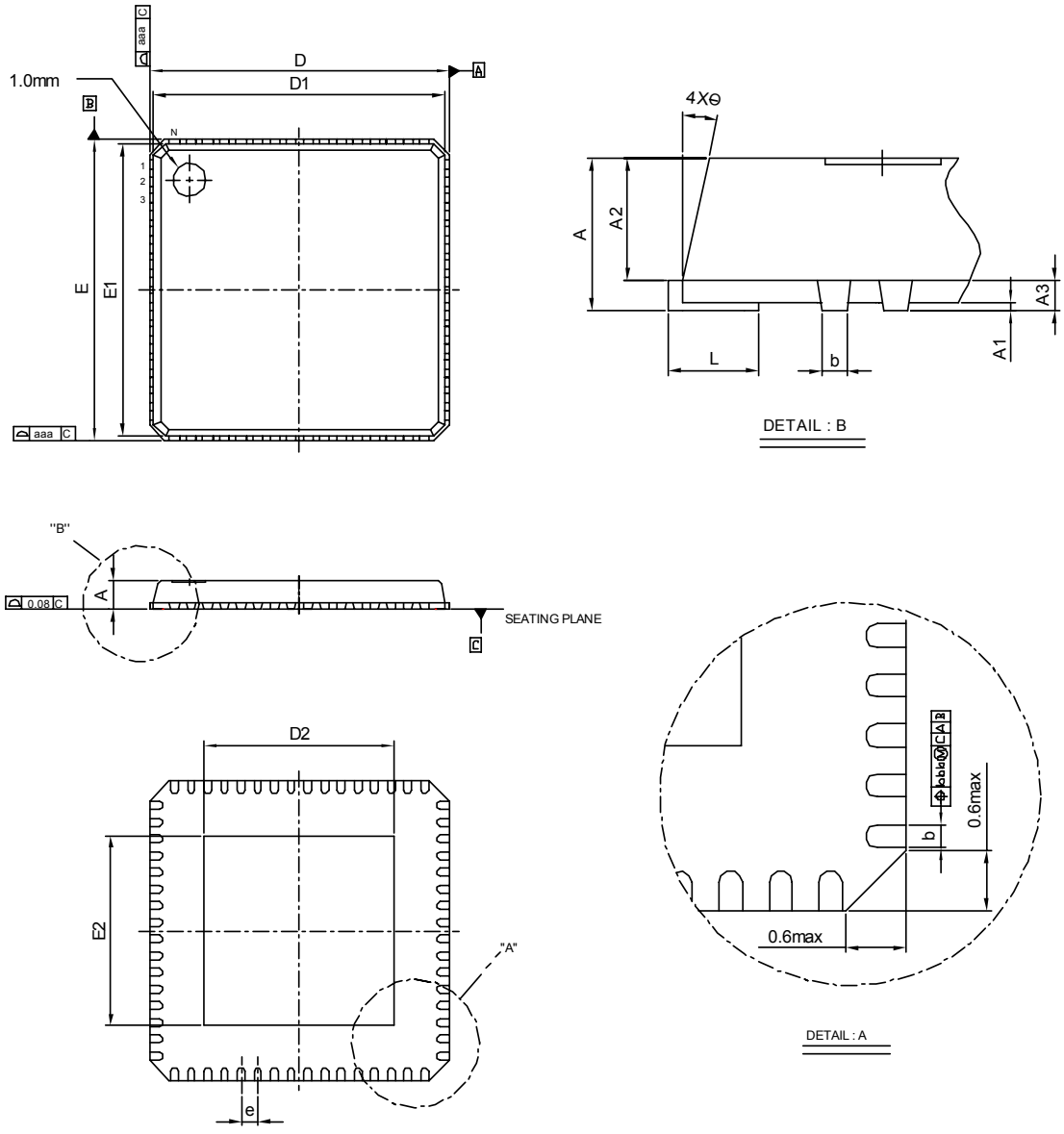
1. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on F_INP/N and the transmitted signal on S_OUTP/N. The worst case variation will be outside these limits, if there is a frequency difference.
2. Assumes register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 40 ns of latency.

Figure 49: 100BASE-FX to SGMII MAC Interface Receive Latency Timing



Section 5. Mechanical Drawings

5.1 64 - Pin 9x9 mm QFN Package



(All Dimensions in mm.)

Table 93: 64-Pin QFN Package Dimensions

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A2	---	0.65	1.00
A3	0.20 REF		
b	0.18	0.23	0.30
D	9.00 BSC		
D1	8.75 BSC		
E	9.00 BSC		
E1	8.75 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
Θ	0°	---	12°
aaa	---	---	0.25
bbb	---	---	0.10
chamfer	---	---	0.60

Die Pad Size	
Symbol	Dimension in mm
D_2	5.21 ± 0.20
E_2	6.25 ± 0.20

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

Section 6. Order Information

6.1 Ordering Part Numbers and Package Markings

Figure 50 shows the ordering part numbering scheme for the 88E1112 device. Contact Marvell FAEs or sales representatives for complete ordering information.

Figure 50: Sample Part Number

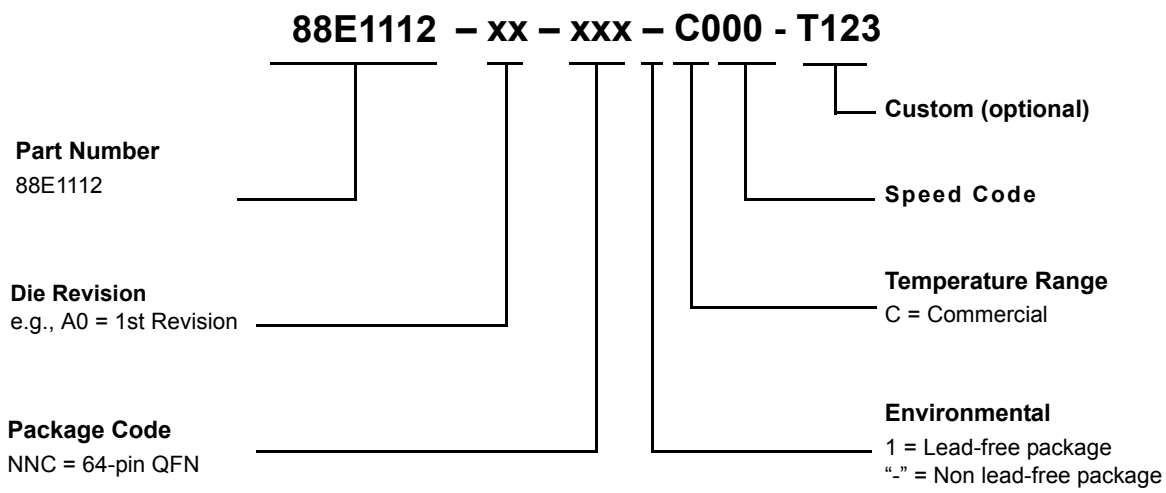


Table 94: 88E1112 Part Order Option - Lead-free Package

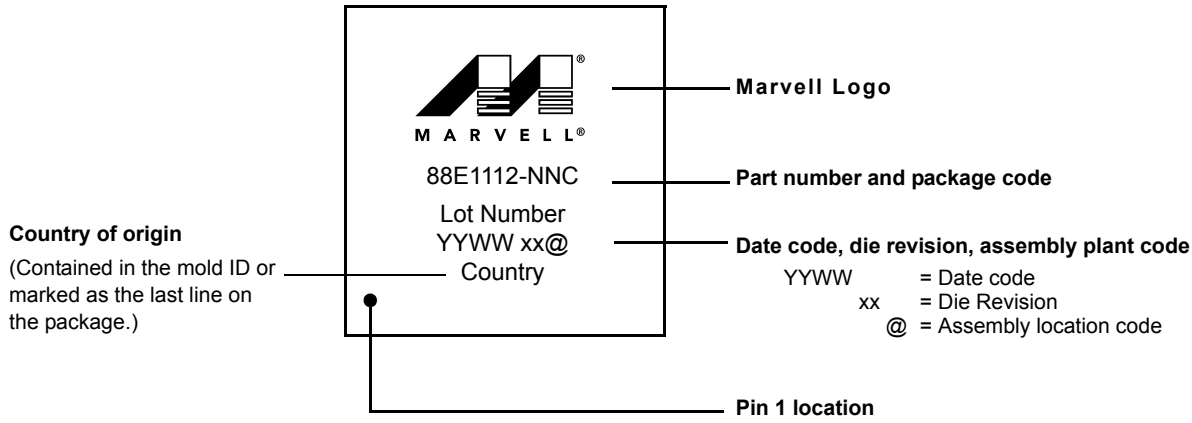
Package Type	Part Order Number
88E1112 64-pin QFN - Commercial	88E1112-XX-NNC1C000

Table 95: 88E1112 Part Order Option - Non Lead-free Package

Package Type	Part Order Number
88E1112 64-pin QFN - Commercial	88E1112-XX-NNC-C000

Figure 51 is an example of the package marking and pin 1 location for the 88E1112 64-pin QFN Commercial package.

Figure 51: 88E1111 64-pin QFN Commercial Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

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