SFF documents are available at http://www.snia.org/sff/specifications.

INF-TA-1003

Information Document for

400 Gb/s (16 x 25 Gb/s) Pluggable Transceiver

Rev 1.1 August 3, 2018

SECRETARIAT: SFF TA TWG

The content contained in this information document was created by an external group. The content was provided to the SFF TA TWG so that it can continue to be publicly available. The content has not been changed by the SFF TA TWG.

The description of a connector in this specification does not assure that the specific component is available from connector suppliers. If such a connector is supplied, it must comply with the specification to achieve interoperability between suppliers.

ABSTRACT: This specification defines the characteristics of the pluggable 16 x 25 Gb/s CDFP module/ direct attach cable plug and connector.

POINTS OF CONTACT:

Jay Neer
Technical Editor
Molex LLC
2222 Wellington Court
Lisle, IL 60532
Ph: 561-251-8016
Email: jay_dot_neer_at_molex_dot_com

Chairman SFF TA TWG
Email: SFF-Chair@snia.org

CDFP MSA

For

400 Gb/s (16 X 25 Gb/s) PLUGGABLE TRANSCEIVER

Rev 3.0 March 20, 2015

Abstract: This specification defines the characteristics of the pluggable 16 x 25 Gb/s CDFP Module/direct attach cable plug and connector.

This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

POINTS OF CONTACT:

Tom Palkert	Nathan Tracy	Scott Kipp
Technical Editor	Chairman	Secretary
Molex	TE Connectivity	Brocade
2222 Wellington Court	3101 Fulling Mill Rd	130 Holger Way
Lisle, IL 60532-1682	Middletown, PA 17057	San Jose, CA 95134
Ph: 952-200-8542	Ph: 717-986-7546	Ph: 408-333-4000
tpalkert at molex.com	ntracy at te.com	skipp at brocade.com

EXPRESSION OF SUPPORT BY MANUFACTURERS

The following are Promoter member companies of the CDFP MSA.

Avago Technologies
Brocade Communications Systems, Inc.
IBM
JDS Uniphase Corporation
Juniper Networks
Molex Incorporated
TE Connectivity

The following are contributing member companies of the CDFP MSA.

FCI
Finisar
Huawei
Inphi
Ixia
Mellanox
MoSys
Nextron
Oclaro, Inc.
Semtech
Sumitomo Electric
Xilinx
Yamaichi

Change History:

Revision	Date	Changes
1.0	March 8 2014	First public release
2.0	September 18, 2014	2nd public release
3.0	March 20, 2015	Added Style 3

Foreword

The development work on this specification was done by the CDFP MSA, an industry group. The membership of the committee since its formation in May 2013 has included a mix of companies which are leaders across the industry.

TABLE OF CONTENTS

List of Figures

List of Tables

CDFP – 400 Gb/s (16 X 25 Gb/s) Pluggable Transceiver

1 Scope

In an effort to broaden the applications for a 400G interface, a multisource agreement group (MSA) was formed. Members include companies representing system integrators and suppliers with an interest in a common form factor solution.

1.1 Description of Clauses

Clause 1 contains the Scope and Purpose

Clause 2 contains Referenced and Related Standards and Specifications

Clause 3 contains the Introduction

Clause 4 contains Electrical Specifications

Clause 5 contains Mechanical Specifications and Printed Circuit Board Recommendations

Clause 6 contains Environmental and Thermal Considerations

Clause 7 is a description of the Management Interface and Management Register contents.

Appendix A contains management register contents and firmware upgrade methodology

2 References

The CDFP MSA supports the requirements of the data center industry, and the MSA is expected to implement several standards.

2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification.

- GR-253-CORE
- OIF CEI 3.1 clause 13
- IEEE Std 802.3bm annex 83E
- IEEE Std 802.3bs
- InfiniBand Architecture Specifications
- INCITS T11.2 FC-PI-6
- SAS 4.0
- SFF-8679 QSFP (Quad SFP) 25 Gbs 4X Transceiver
- SFF-8636 Cables Common Management Interface
- SFF-8472 Diagnostic Monitoring Interface for Optical Transceivers
- SFF-8431 Enhanced Small Form Factor Pluggable Module SFP+
- JESD22A114-B ESD specifications

2.2 SFF Specifications

It is the intention of the MSA to create appropriate SFF specifications based on this MSA.

2.3 Sources

This document can be obtained via the CDFP-MSA.org web site.

3 Introduction

This Specification covers the following items:

a) Electrical interfaces (including pinouts for data control, status, configuration and test signals) and the electrical connector and recommended host PCB layout requirements.

b) Management interfaces encompassing features from the current SFF 8636 and SFF 8472 specifications. Features include support for multiple physical media (copper, optics etc), specific multi-data rate and multi-protocol implementations.

c) Optical interfaces (including the optical connector receptacle and mating fiber optic connector plug and recommended breakout cable assembly.) The optical specifications are left to the applicable standards for each protocol.

d) Mechanical including package outline with latching detail and optical connector receptacle detail, electrical connector mechanical details for both the module and host PCB halves, front panel cut-out recommended dimensions.

e) Thermal requirements

f) Electromagnetic interference (EMI) recommendations(including necessary shielding features to seal the OEM chassis front panel output with and without the CDFP module installed in the cage.)

g) Electrostatic discharge (ESD) requirements solely to the extent disclosed in the Specification where the sole purpose of such disclosure is to enable products to operate, connect or communicate as defined within the Specifications.

The overall package dimensions shall conform to the indicated dimensions and tolerances indicated in clause 5. The mounting features shall be located such that the products are mechanically interchangeable with the cage and connector system. In addition, the overall dimensions and mounting requirements for the cage and connector system on a circuit board shall be configured such that the products are mechanically and electrically interchangeable and the overall dimensions and insertion requirements for the optical connector and corresponding fiber optic cable plug shall be such that the products are mechanically and optically interchangeable.

This Specification is intended to support applications defined by Ethernet IEEE 802.3 (400Gigabit, 100Gigabit and 25Gigabit Ethernet), Infiniband Architecture Specifications (FDR and EDR), Fibre Channel-PI-6 (32GFC) and FC-PI-6p (128GFC). Electrical and optical specifications are defined by the appropriate standard and as such are beyond the scope of this document.

The Specifications will provide a common solution for combined 16-channel ports that support OTN, Ethernet and/or InfiniBand and/or Fibre Channel specifications. The CDFP interface can support pluggable modules or direct attach cables based on multimode fiber, single mode fiber or copper cables.
An application reference Model, See Figure 1 for Style 1/Style 2 and Figure 2 for Style 3, shows the high-speed data interface between an ASIC (SerDes) and the CDFP module. Parallel MPO16 fiber connectors can be used for the optical interface.

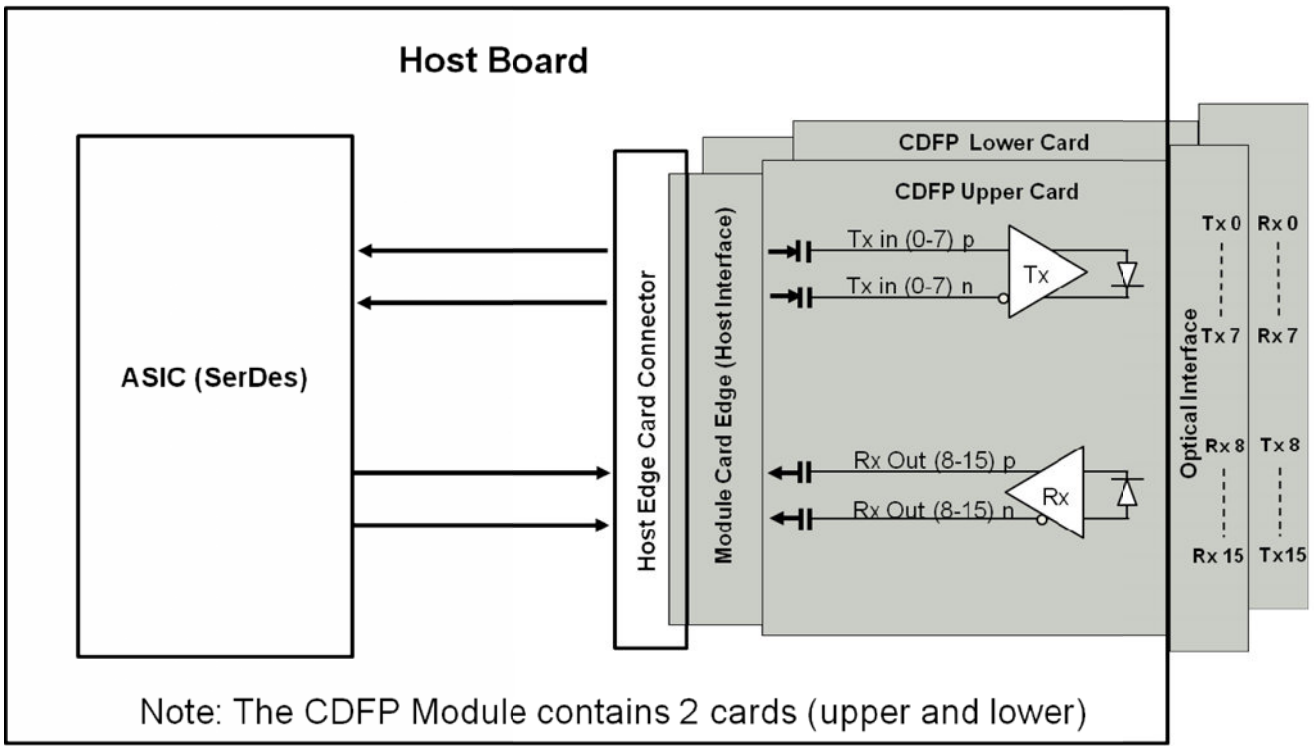


Figure 1: Style 1/Style 2CDFP Reference Architecture

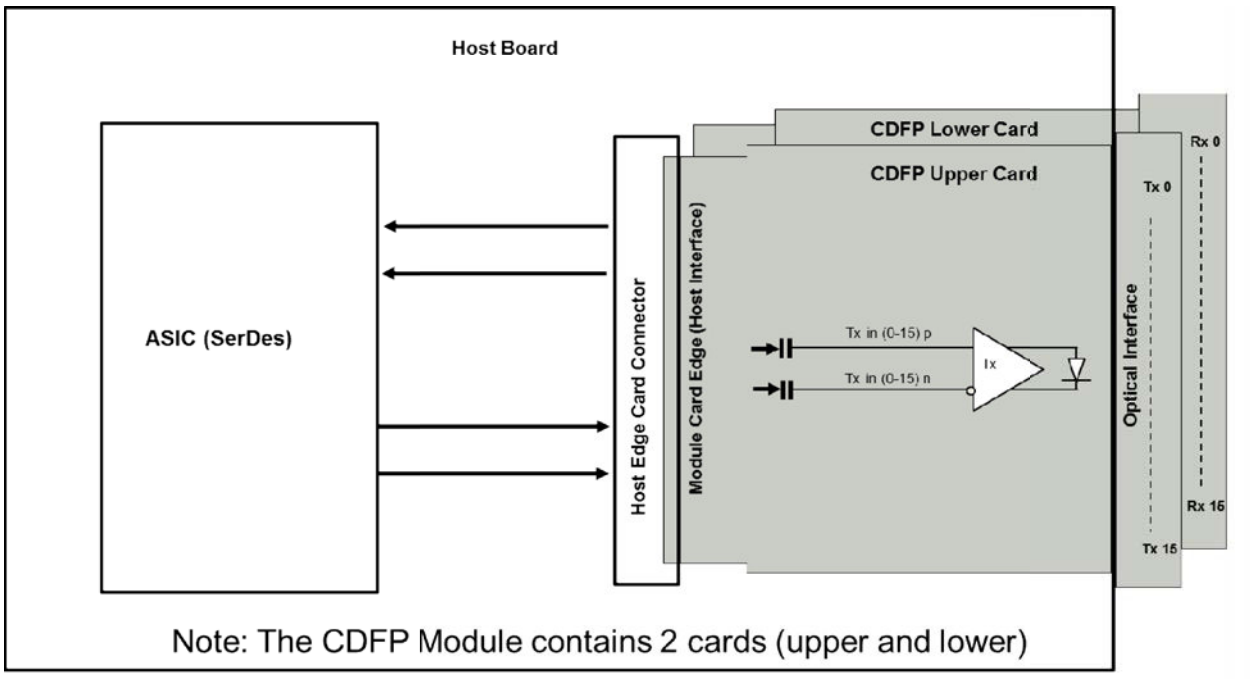


Figure 2: CDFP Style 3 Reference Architecture

Note: For high speed electrical signals the compliance board methodology of IEEE802.3bm, OIF CEI-28G-VSR should be used. Measurements taken with CDFP compliance boards should be corrected for any difference between the loss of these compliance boards and the loss of the compliance boards specified in the standard.

4 Electrical Specification

This clause contains pin definition data for the CDFP Module. The pin definition data is generic for applications such as Fibre Channel, InfiniBand, Ethernet and OTN. Compliance Points for high-speed signal electrical measurements are defined with the inclusion of compliance boards. Compliance Points for all other electrical signals are at comparable points at the host edge card connector.

4.1 Module Pin Definitions

The CDFP Pluggable Module Edge Connector consists of two parallel paddle cards with 30 contacts on the top and bottom of each paddle card for a total of 120 circuits. Figures 3 and 4 show the signal symbols and contact numbering for the CDFP Module edge connector used for Style 1 and Style 2. Figures 5 and 6 show the signal symbols and contact numbering for the CDFP Module edge connector used for Style 3. The diagrams show the module PCB edge as a top and bottom view. There are 120 contacts intended for high speed, low speed signals, power and ground connections. Table 1and Table 2 provide more information about each of the 120 contacts.

For EMI protection the signals to the connector should be shut off when the CDFP Module is removed. Standard board layout practices such as connections to Vcc and GND with Vias, use of short and equal-length differential signal lines, use of microstrip-lines and 50 Ohm terminations are recommended. The chassis ground (case common) of the CDFP module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

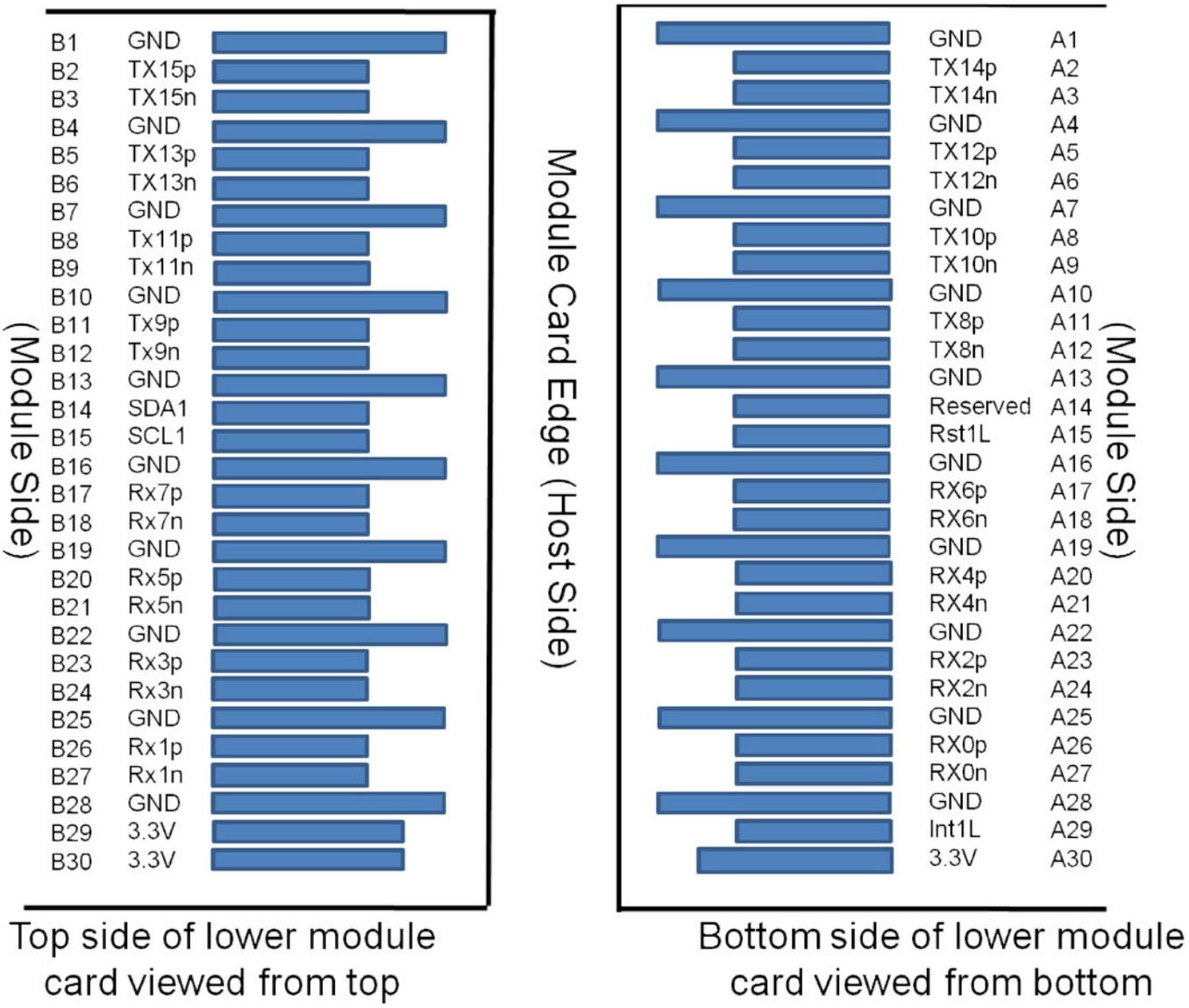


Figure 3: Lower Card (Card 1) Pin outs Style 1/Style 2

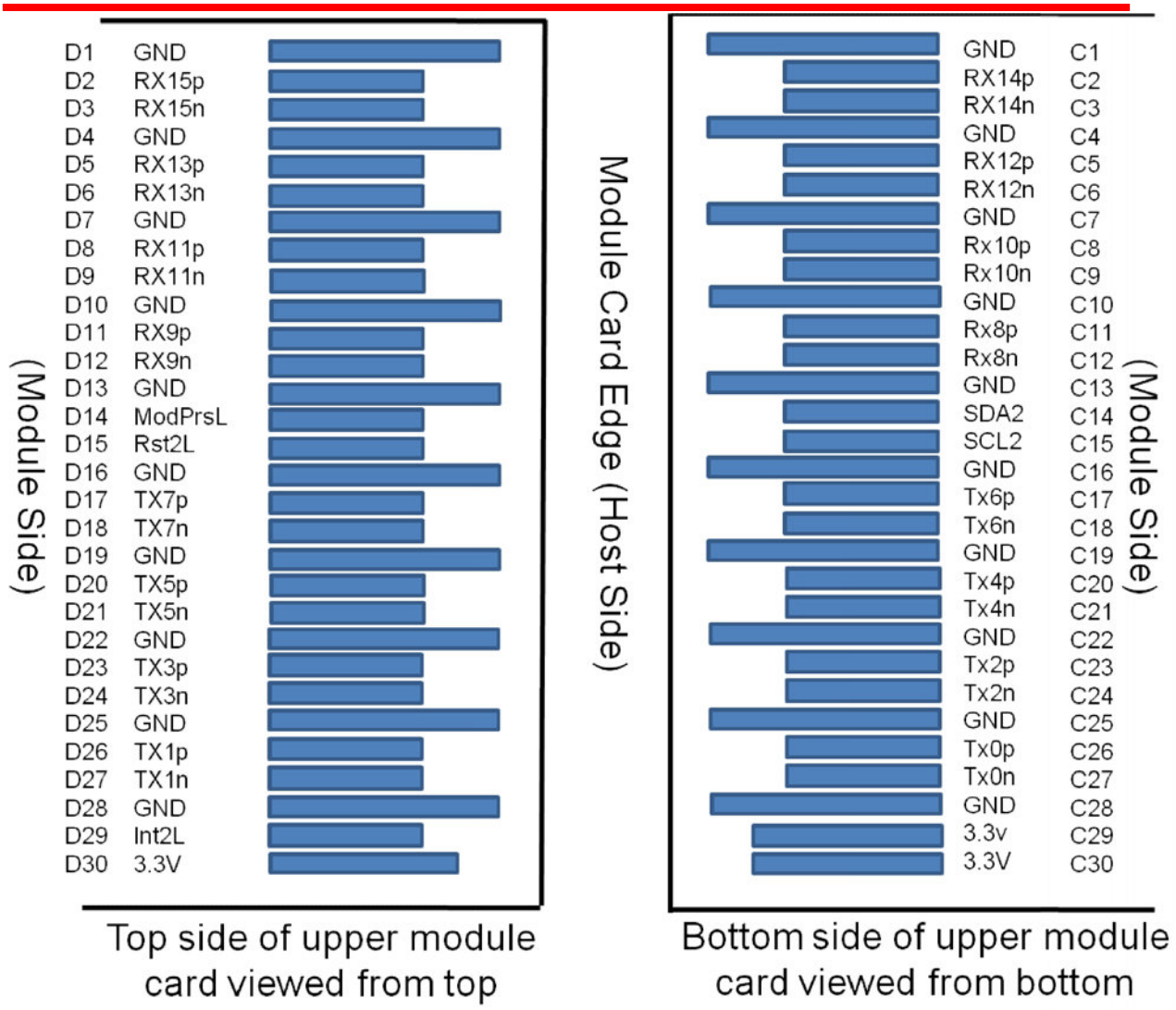


Figure 4: Upper Card (Card 2) Pin outs Style 1/Style 2

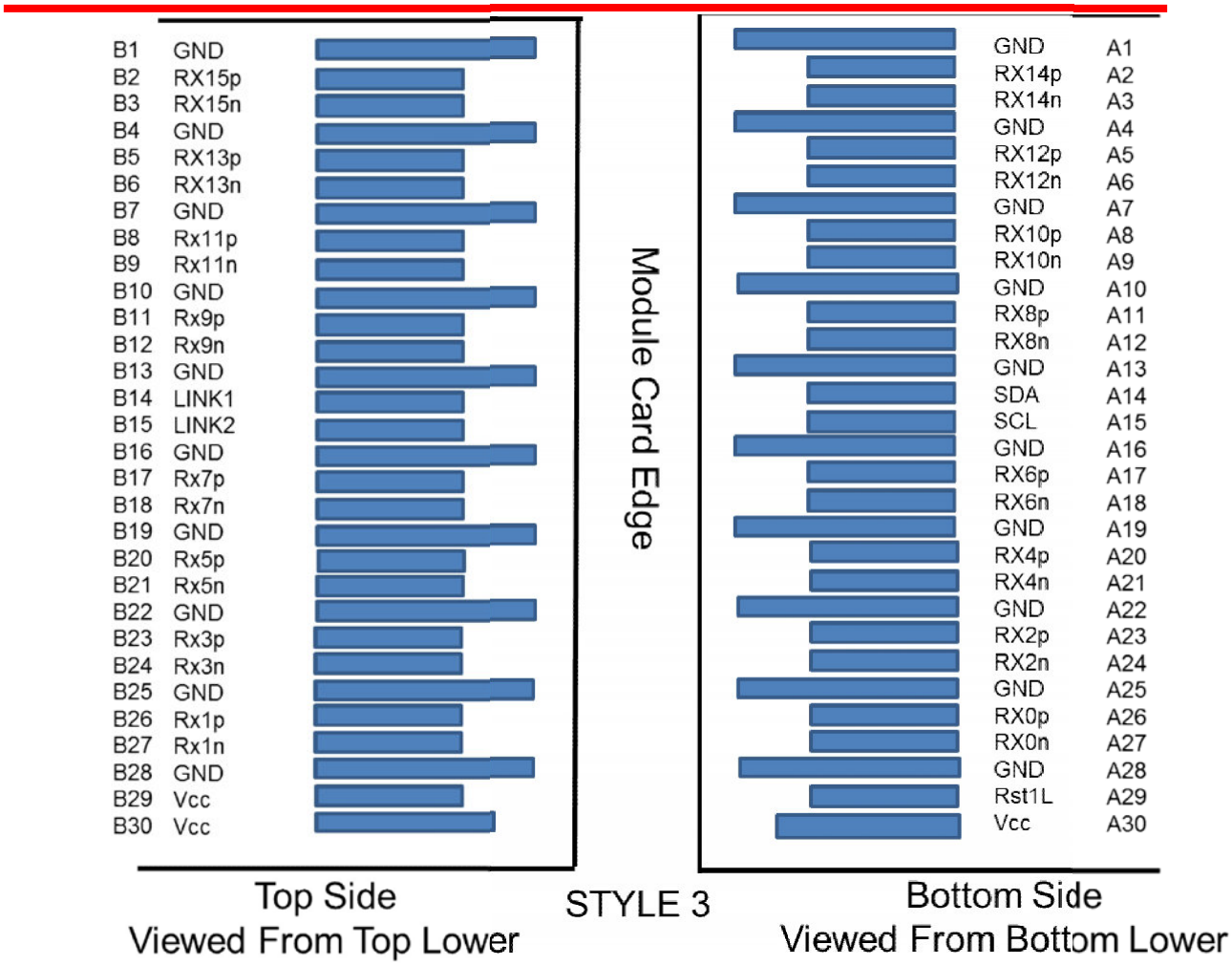


Figure 5: Lower Card (Card 1) Pin outs Style 3

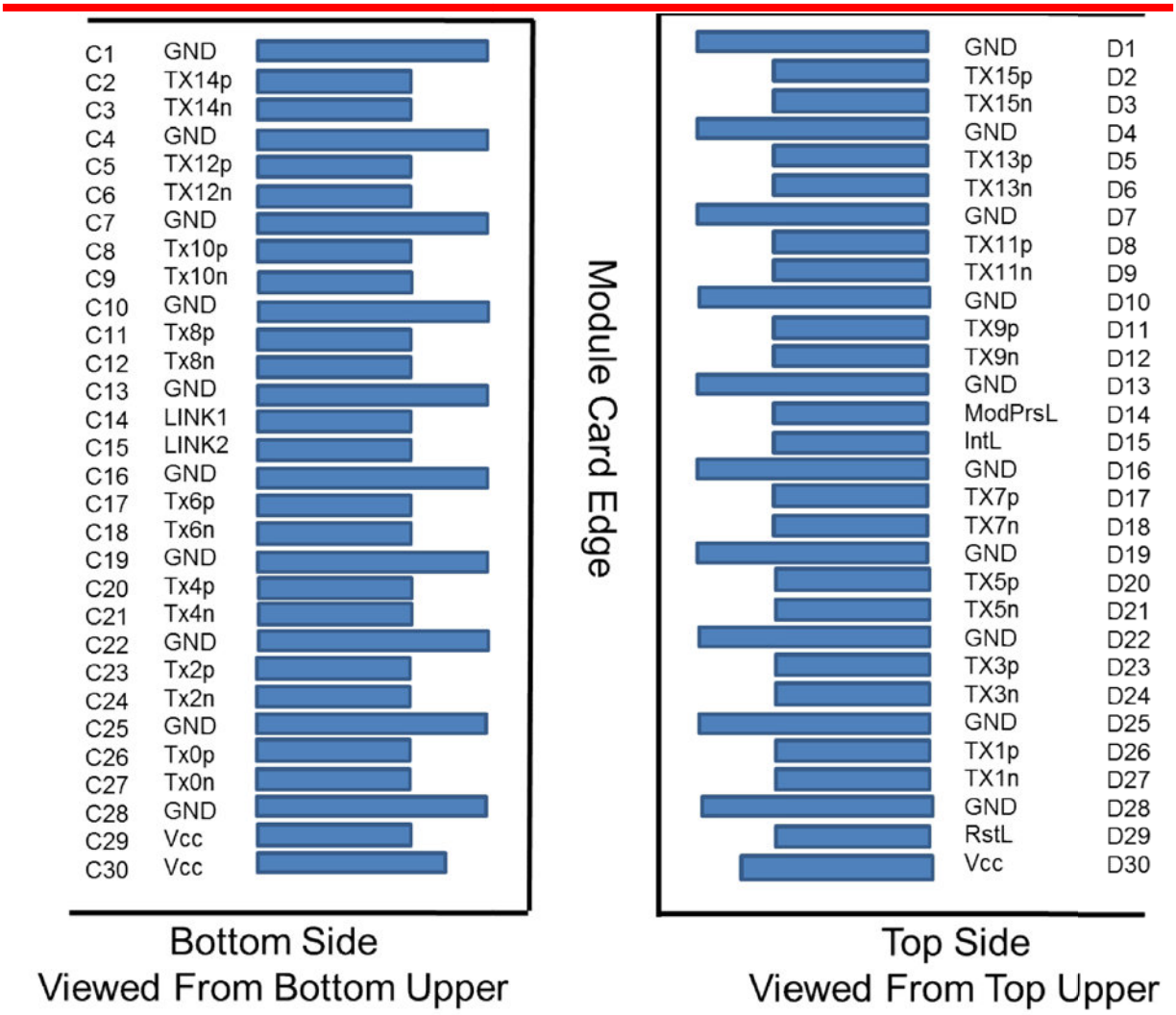


Figure 6: Upper Card (Card 2) Pin outs Style 3

Table 1: Style 1/Style 2 Pin Function Definition

Module Pad	Host pin	Logic	Symbol	Description	Plug Sequence	Notes
A1	G1		GND	Ground	1	1
A2	A1X	CML-I	Tx14p	Transmitter Inverted Data Input	3	
A3	A1Y	CML-I	Tx14n	Transmitter Non-Inverted Data Input	3	
A4	G2		GND	Ground	1	1
A5	A2X	CML-I	Tx12p	Transmitter Inverted Data Input	3	
A6	A2Y	CML-I	Tx12n	Transmitter Non-Inverted Data Input	3	
A7	G3		GND	Ground	1	1
A8	A3X	CML-I	Tx10p	Transmitter Inverted Data Input	3	
A9	A3Y	CML-I	Tx10n	Transmitter Non-Inverted Data Input	3	
A10	G4		GND	Ground	1	1
A11	A4X	CML-I	Tx8p	Transmitter Inverted Data Input	3	
A12	A4Y	CML-I	Tx8n	Transmitter Non-Inverted Data Input	3	
A13	G5		GND	Ground	1	1
A14	A5X		Reserved			
A15	A5Y	LVTTL-I	Rst1L	Module Reset for lower card	3	
A16	G6		GND	Ground	1	1
A17	A6X	CML-O	Rx6p	Receiver Non-Inverted Data Output	3	
A18	A6Y	CML-O	Rx6n	Receiver Inverted Data Output	3	
A19	G7		GND	Ground	1	1
A20	A7X	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
A21	A7Y	CML-O	Rx4n	Receiver Inverted Data Output	3	
A22	G8		GND	Ground	1	1
A23	A8X	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
A24	A8Y	CML-O	Rx2n	Receiver Inverted Data Output	3	
A25	G9		GND	Ground	1	1
A26	A9X	CML-O	Rx0p	Receiver Non-Inverted Data Output	3	
A27	A9Y	CML-O	Rx0n	Receiver Inverted Data Output	3	
A28	G10		GND	Ground	1	1
A29	A10X	LVTTL-O	Int1L	Interrupt for lower card	3	
A30	A10Y		Vcc	+3.3V Power supply	2	2
B1	G11		GND	Ground	1	1
B2	B1X	CML-I	Tx15p	Transmitter Inverted Data Input	3	
B3	B1Y	CML-I	Tx15n	Transmitter Non-Inverted Data Input	3	
B4	G12		GND	Ground	1	1
B5	B2X	CML-I	Tx13p	Transmitter Inverted Data Input	3	
B6	B2Y	CML-I	Tx13n	Transmitter Non-Inverted Data Input	3	
B7	G13		GND	Ground	1	1
B8	B3X	CML-I	Tx11p	Transmitter Inverted Data Input	3	
B9	B3Y	CML-I	Tx11n	Transmitter Non-Inverted Data Input	3	
B10	G14		GND	Ground	1	1
B11	B4X	CML-I	Tx9p	Transmitter Inverted Data Input	3	
B12	B4Y	CML-I	Tx9n	Transmitter Non-Inverted Data Input	3	
B13	G15		GND	Ground	1	1
B14	B5X	LVCMOS-I/O	SDA1	two-wire serial interface data for lower card	3	
B15	B5Y	LVCMOS-I/O	SCL1	two-wire serial interface clock for lower card	3	
B16	G16		GND	Ground	1	1
B17	B6X	CML-O	Rx7p	Receiver Non-Inverted Data Output	3	
B18	B6Y	CML-O	Rx7n	Receiver Inverted Data Output	3	
B19	G17		GND	Ground	1	1
B20	B7X	CML-O	Rx5p	Receiver Non-Inverted Data Output	3	
B21	B7Y	CML-O	Rx5n	Receiver Inverted Data Output	3	
B22	G18		GND	Ground	1	1

B23	B8X	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
B24	B8Y	CML-O	Rx3n	Receiver Inverted Data Output	3	
B25	G19		GND	Ground	1	1
B26	B9X	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
B27	B9Y	CML-O	Rx1n	Receiver Inverted Data Output	3	
B28	G20		GND	Ground	1	1
B29	B10X		Vcc	+3.3V Power supply	2	2
B30	B10Y		Vcc	+3.3V Power supply	2	2
C1	G31		GND	Ground	1	1
C2	C1X	CML-O	Rx14p	Receiver Non-Inverted Data Output	3	
C3	C1Y	CML-O	Rx14n	Receiver Inverted Data Output	3	
C4	G32		GND	Ground	1	1
C5	C2X	CML-O	Rx12p	Receiver Non-Inverted Data Output	3	
C6	C2Y	CML-O	Rx12n	Receiver Inverted Data Output	3	
C7	G33		GND	Ground	1	1
C8	C3X	CML-O	Rx10p	Receiver Non-Inverted Data Output	3	
C9	C3Y	CML-O	Rx10n	Receiver Inverted Data Output	3	
C10	G34		GND	Ground	1	1
C11	C4X	CML-O	Rx8p	Receiver Non-Inverted Data Output	3	
C12	C4Y	CML-O	Rx8n	Receiver Inverted Data Output	3	
C13	G35		GND	Ground	1	1
C14	C5X	LVCMOS-I/O	SDA2	two-wire serial interface data for upper card	3	
C15	C5Y	LVCMOS-I/O	SCL2	two-wire serial interface clock for upper card	3	
C16	G36		GND	Ground	1	1
C17	C6X	CML-I	Tx6p	Transmitter Inverted Data Input	3	
C18	C6Y	CML-I	Tx6n	Transmitter Non-Inverted Data Input	3	
C19	G37		GND	Ground	1	1
C20	C7X	CML-I	Tx4p	Transmitter Inverted Data Input	3	
C21	C7Y	CML-I	Tx4n	Transmitter Non-Inverted Data Input	3	
C22	G38		GND	Ground	1	1
C23	C8X	CML-I	Tx2p	Transmitter Inverted Data Input	3	
C24	C8Y	CML-I	Tx2n	Transmitter Non-Inverted Data Input	3	
C25	G39		GND	Ground	1	1
C26	C9X	CML-I	Tx0p	Transmitter Inverted Data Input	3	
C27	C9Y	CML-I	Tx0n	Transmitter Non-Inverted Data Input	3	
C28	G40		GND	Ground	1	1
C29	C10X		Vcc	+3.3V Power supply	2	2
C30	C10Y		Vcc	+3.3V Power supply	2	2
D1	G41		GND	Ground	1	1
D2	D1X	CML-O	Rx15p	Receiver Non-Inverted Data Output	3	
D3	D1Y	CML-O	Rx15n	Receiver Inverted Data Output	3	
D4	G42		GND	Ground	1	1
D5	D2X	CML-O	Rx13p	Receiver Non-Inverted Data Output	3	
D6	D2Y	CML-O	Rx13n	Receiver Inverted Data Output	3	
D7	G43		GND	Ground	1	1
D8	D3X	CML-O	Rx11p	Receiver Non-Inverted Data Output	3	
D9	D3Y	CML-O	Rx11n	Receiver Inverted Data Output	3	
D10	G44		GND	Ground	1	1
D11	D4X	CML-O	Rx9p	Receiver Non-Inverted Data Output	3	
D12	D4Y	CML-O	Rx9n	Receiver Inverted Data Output	3	
D13	G45		GND	Ground	1	1
D14	D5X	LVTTL-O	ModPrsL	Module Present	3	
D15	D5Y	LVTTL-I	Rst2L	Module Reset for upper card	3	
D16	G46		GND	Ground	1	1
D17	D6X	CML-I	Tx7p	Transmitter Inverted Data Input	3	

D18	D6Y	CML-I	Tx7n	Transmitter Non-Inverted Data Input	3	
D19	G47		GND	Ground	1	1
D20	D7X	CML-I	Tx5p	Transmitter Inverted Data Input	3	
D21	D7Y	CML-I	Tx5n	Transmitter Non-Inverted Data Input	3	
D22	G48		GND	Ground	1	1
D23	D8X	CML-I	Tx3p	Transmitter Inverted Data Input	3	
D24	D8Y	CML-I	Tx3n	Transmitter Non-Inverted Data Input	3	
D25	G49		GND	Ground	1	1
D26	D9X	CML-I	Tx1p	Transmitter Inverted Data Input	3	
D27	D9Y	CML-I	Tx1n	Transmitter Non-Inverted Data Input	3	
D28	G50		GND	Ground	1	1
D29	D10X	LVTTL-O	Int2L	Interrupt for upper card	3	
D30	D10Y		Vcc	+3.3V Power supply	2	2
	Note 1: GND is the symbol for signal and supply (power) common for the CDFP module. All are common within the CDFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.					
	Note 2: Vcc are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 5. Recommended host board power supply filtering is shown in Figure 7. Vcc may be internally connected within the CDFP Module in any combination. The Vcc connector pins are each rated for a maximum current of 1 A.					

Figure 7 (Style 1/Style 2) and Figure 8 (Style 3) show examples of complete CDFP host PCB schematics with connections to SerDes and control ICs.

Table 2: Pin Function Definition Style 3

Module Pad	Host pin	Logic	Symbol	Description	Plug Sequence	Notes
A1	G1		GND	Ground	1	1
A2	A1X	CML-O	Rx14p	Receiver Non-Inverted Data Output	3	
A3	A1Y	CML-O	Rx14n	Receiver Inverted Data Output	3	
A4	G2		GND	Ground	1	1
A5	A2X	CML-O	Rx12p	Receiver Non-Inverted Data Output	3	
A6	A2Y	CML-O	Rx12n	Receiver Inverted Data Output	3	
A7	G3		GND	Ground	1	1
A8	A3X	CML-O	Rx10p	Receiver Non-Inverted Data Output	3	
A9	A3Y	CML-O	Rx10n	Receiver Inverted Data Output	3	
A10	G4		GND	Ground	1	1
A11	A4X	CML-O	Rx8p	Receiver Non-Inverted Data Output	3	
A12	A4Y	CML-O	Rx8n	Receiver Inverted Data Output	3	
A13	G5		GND	Ground	1	1
A14	A5X	LVCMOS-I/O	SDA1	two-wire serial interface data for lower card	3	
A15	A5Y	LVCMOS-I/O	SCL1	two-wire serial interface clock for lower card	3	
A16	G6		GND	Ground	1	1
A17	A6X	CML-O	Rx6p	Receiver Non-Inverted Data Output	3	
A18	A6Y	CML-O	Rx6n	Receiver Inverted Data Output	3	
A19	G7		GND	Ground	1	1
A20	A7X	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
A21	A7Y	CML-O	Rx4n	Receiver Inverted Data Output	3	
A22	G8		GND	Ground	1	1
A23	A8X	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
A24	A8Y	CML-O	Rx2n	Receiver Inverted Data Output	3	
A25	G9		GND	Ground	1	1
A26	A9X	CML-O	Rx0p	Receiver Non-Inverted Data Output	3	
A27	A9Y	CML-O	Rx0n	Receiver Inverted Data Output	3	
A28	G10		GND	Ground	1	1
A29	A10X	LVTTL-I	Rst1L	Module Reset for lower card	3	
A30	A10Y		Vcc	+3.3V Power supply	2	2
B1	G11		GND	Ground	1	1
B2	B1X	CML-O	Rx15p	Receiver Non-Inverted Data Output	3	
B3	B1Y	CML-O	Rx15n	Receiver Inverted Data Output	3	
B4	G12		GND	Ground	1	1
B5	B2X	CML-O	Rx13p	Receiver Non-Inverted Data Output	3	
B6	B2Y	CML-O	Rx13n	Receiver Inverted Data Output	3	
B7	G13		GND	Ground	1	1
B8	B3X	CML-O	Rx11p	Receiver Non-Inverted Data Output	3	
B9	B3Y	CML-O	Rx11n	Receiver Inverted Data Output	3	
B10	G14		GND	Ground	1	1
B11	B4X	CML-O	Rx9p	Receiver Non-Inverted Data Output	3	
B12	B4Y	CML-O	Rx9n	Receiver Inverted Data Output	3	
B13	G15		GND	Ground	1	1
B14	B5X	LVTTL-O	Int1L	Interrupt for lower card	3	
B15	B5Y		Reserved			
B16	G16		GND	Ground	1	1
B17	B6X	CML-O	Rx7p	Receiver Non-Inverted Data Output	3	
B18	B6Y	CML-O	Rx7n	Receiver Inverted Data Output	3	
B19	G17		GND	Ground	1	1
B20	B7X	CML-O	Rx5p	Receiver Non-Inverted Data Output	3	
B21	B7Y	CML-O	Rx5n	Receiver Inverted Data Output	3	
B22	G18		GND	Ground	1	1

B23	B8X	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
B24	B8Y	CML-O	Rx3n	Receiver Inverted Data Output	3	
B25	G19		GND	Ground	1	1
B26	B9X	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
B27	B9Y	CML-O	Rx1n	Receiver Inverted Data Output	3	
B28	G20		GND	Ground	1	1
B29	B10X		Vcc	+3.3V Power supply	2	2
B30	B10Y		Vcc	+3.3V Power supply	2	2
C1	G31		GND	Ground	1	1
C2	C1X	CML-I	Tx14p	Transmitter Inverted Data Input	3	
C3	C1Y	CML-I	Tx14n	Transmitter Non-Inverted Data Input	3	
C4	G32		GND	Ground	1	1
C5	C2X	CML-I	Tx12p	Transmitter Inverted Data Input	3	
C6	C2Y	CML-I	Tx12n	Transmitter Non-Inverted Data Input	3	
C7	G33		GND	Ground	1	1
C8	C3X	CML-I	Tx10p	Transmitter Inverted Data Input	3	
C9	C3Y	CML-I	Tx10n	Transmitter Non-Inverted Data Input	3	
C10	G34		GND	Ground	1	1
C11	C4X	CML-I	Tx8p	Transmitter Inverted Data Input	3	
C12	C4Y	CML-I	Tx8n	Transmitter Non-Inverted Data Input	3	
C13	G35		GND	Ground	1	1
C14	C5X	LVCMOS-I/O	SDA2	two-wire serial interface data for upper card	3	
C15	C5Y	LVCMOS-I/O	SCL2	two-wire serial interface clock for upper card	3	
C16	G36		GND	Ground	1	1
C17	C6X	CML-I	Tx6p	Transmitter Inverted Data Input	3	
C18	C6Y	CML-I	Tx6n	Transmitter Non-Inverted Data Input	3	
C19	G37		GND	Ground	1	1
C20	C7X	CML-I	Tx4p	Transmitter Inverted Data Input	3	
C21	C7Y	CML-I	Tx4n	Transmitter Non-Inverted Data Input	3	
C22	G38		GND	Ground	1	1
C23	C8X	CML-I	Tx2p	Transmitter Inverted Data Input	3	
C24	C8Y	CML-I	Tx2n	Transmitter Non-Inverted Data Input	3	
C25	G39		GND	Ground	1	1
C26	C9X	CML-I	Tx0p	Transmitter Inverted Data Input	3	
C27	C9Y	CML-I	Tx0n	Transmitter Non-Inverted Data Input	3	
C28	G40		GND	Ground	1	1
C29	C10X		Vcc	+3.3V Power supply	2	2
C30	C10Y		Vcc	+3.3V Power supply	2	2
D1	G41		GND	Ground	1	1
D2	D1X	CML-I	Tx15p	Transmitter Inverted Data Input	3	
D3	D1Y	CML-I	Tx15n	Transmitter Non-Inverted Data Input	3	
D4	G42		GND	Ground	1	1
D5	D2X	CML-I	Tx13p	Transmitter Inverted Data Input	3	
D6	D2Y	CML-I	Tx13n	Transmitter Non-Inverted Data Input	3	
D7	G43		GND	Ground	1	1
D8	D3X	CML-I	Tx11p	Transmitter Inverted Data Input	3	
D9	D3Y	CML-I	Tx11n	Transmitter Non-Inverted Data Input	3	
D10	G44		GND	Ground	1	1
D11	D4X	CML-I	Tx9p	Transmitter Inverted Data Input	3	
D12	D4Y	CML-I	Tx9n	Transmitter Non-Inverted Data Input	3	
D13	G45		GND	Ground	1	1
D14	D5X	LVTTL-O	ModPrsL	Module Present	3	
D15	D5Y	LVTTL-O	Int2L	Interrupt for upper card	3	
D16	G46		GND	Ground	1	1
D17	D6X	CML-I	Tx7p	Transmitter Inverted Data Input	3	

D18	D6Y	CML-I	Tx7n	Transmitter Non-Inverted Data Input	3	
D19	G47		GND	Ground	1	1
D20	D7X	CML-I	Tx5p	Transmitter Inverted Data Input	3	
D21	D7Y	CML-I	Tx5n	Transmitter Non-Inverted Data Input	3	
D22	G48		GND	Ground	1	1
D23	D8X	CML-I	Tx3p	Transmitter Inverted Data Input	3	
D24	D8Y	CML-I	Tx3n	Transmitter Non-Inverted Data Input	3	
D25	G49		GND	Ground	1	1
D26	D9X	CML-I	Tx1p	Transmitter Inverted Data Input	3	
D27	D9Y	CML-I	Tx1n	Transmitter Non-Inverted Data Input	3	
D28	G50		GND	Ground	1	1
D29	D10X	LVTTL-I	Rst2L	Module Reset for upper card	3	
D30	D10Y		Vcc	+3.3V Power supply	2	2
	Note 1: GND is the symbol for signal and supply (power) common for the CDFP module. All are common within the CDFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.					
	Note 2: Vcc are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 5. Recommended host board power supply filtering is shown in Figure 8. Vcc may be internally connected within the CDFP Module in any combination. The Vcc connector pins are each rated for a maximum current of 1 A.					

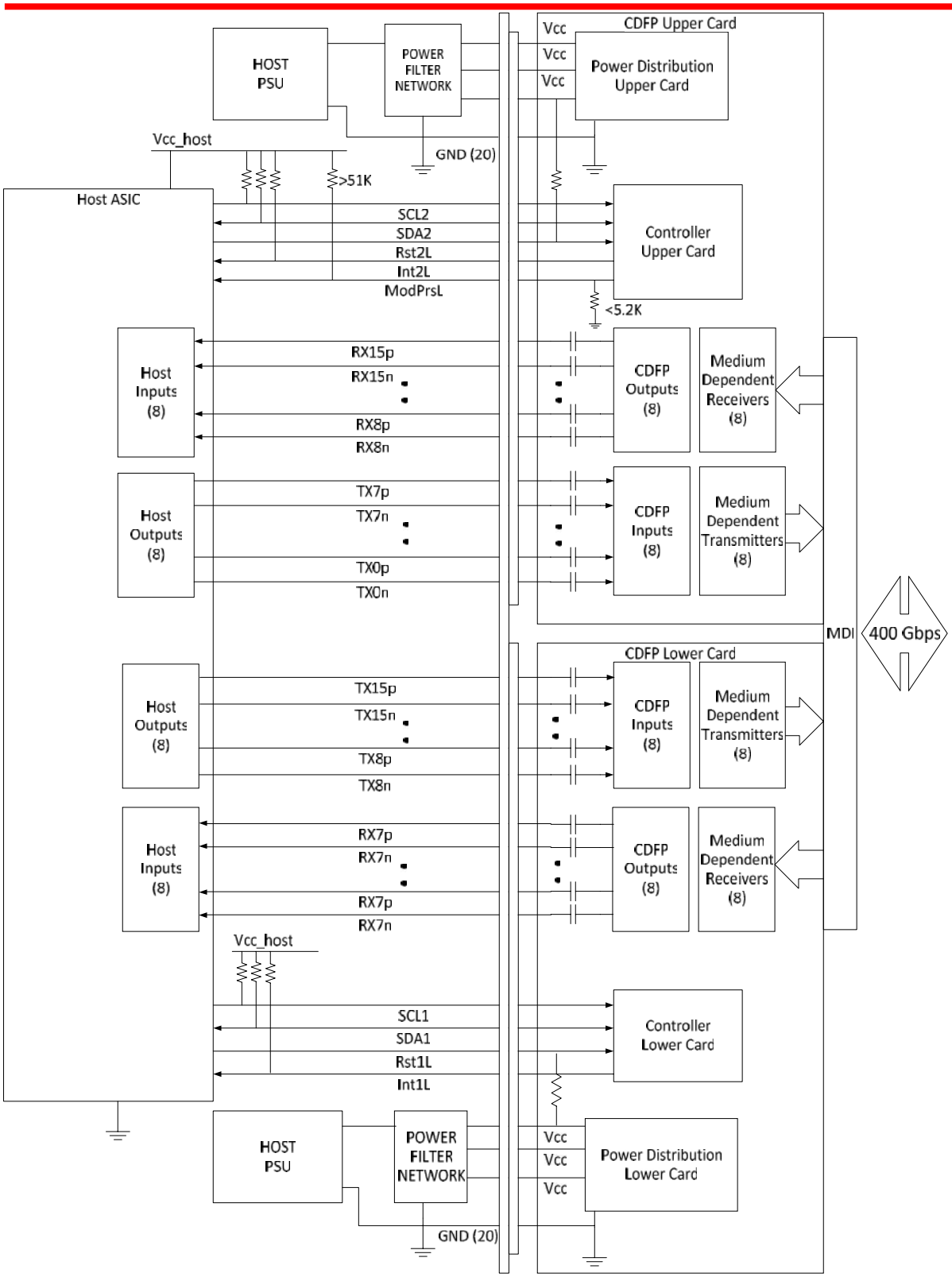


Figure 7: CDFP Host Card Style 1/Style 2

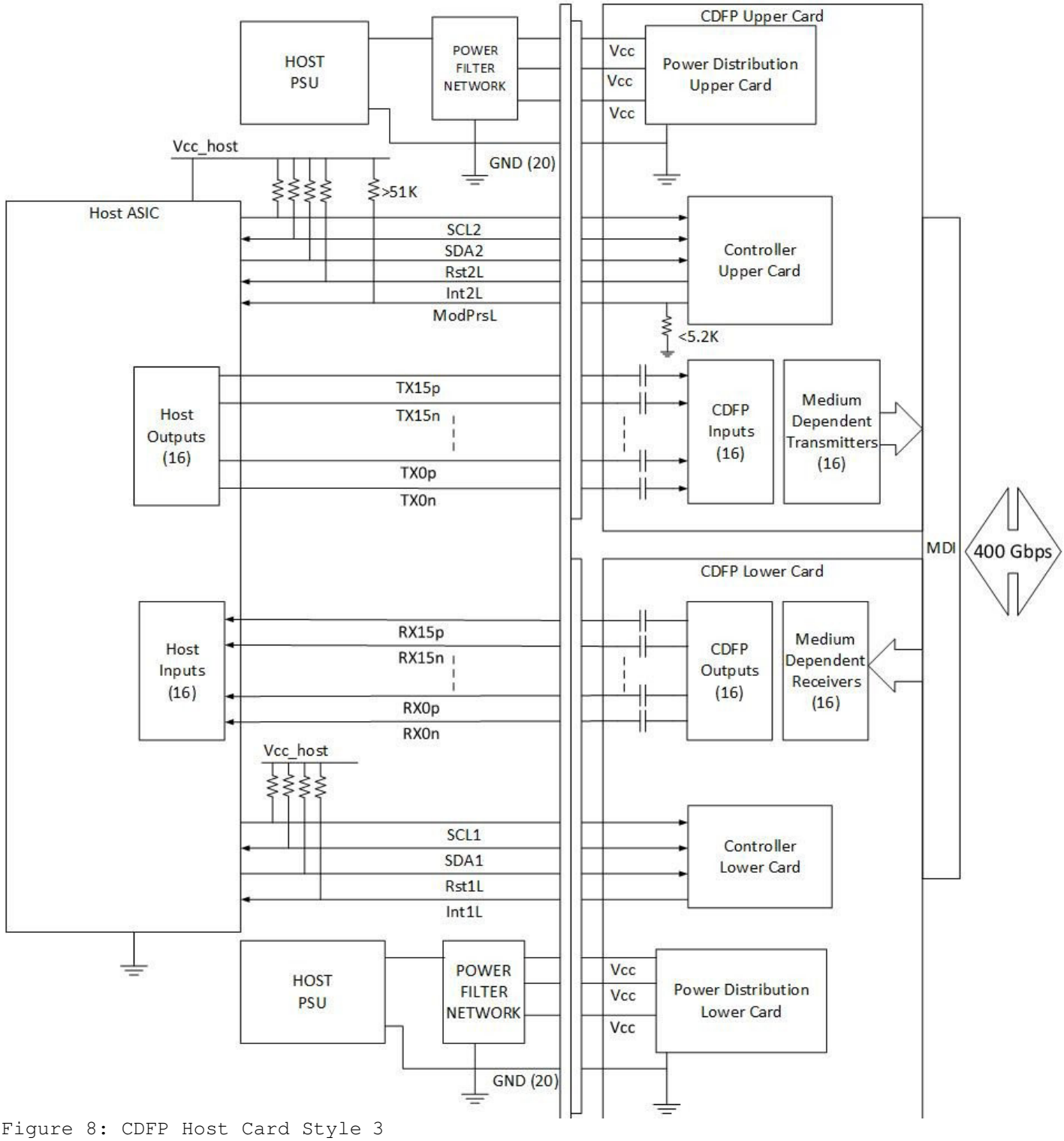


Figure 8: CDFP Host Card Style 3

4.1.1 Low Speed Electrical Hardware Pins

In addition to the two-wire serial interface the module has the following low speed pins for control and status:

- Rst1L and Rst2L
- ModPrsL
- Int1L and Int2L

4.1.1.1Rst1L and Rst2L

The RstL pins must be pulled to Vcc in the CDFP module. A low level on anRstL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module card reset, returning all user module card settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the RstL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module card indicates a completion of the reset interrupt. The module card indicates this by asserting "low" an IntL signal with the DataNotReady bit negated. Note that on power up (including hot insertion) the module card should post this completion of reset interrupt without requiring a reset.

4.1.1.2 ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and pulled down in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

4.1.1.3Int1L and Int2L

IntL is an output pin. When "Low", it indicates a possible module card operational fault or a status critical to the host system. The host identifies the source of the interrupt using the two-wire serial interface. The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The IntL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (DataNotReady) is read with a value of '0' and the flag field is read (see Table 13 Section 7.3.3).

4.1.2 Low Speed Electrical Specification

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the 3.3V supply pins of the module or to a separate host Vcc voltage. Hosts shall use a pull-up resistor connected to Vcc_host on each of the two-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface.

Note 1-Timing diagrams for SCL and SDA are included in Sub clause7.2.2.

The CDFP low speed electrical specifications are given in Table 3. This specification ensures compatibility between host bus masters and the two-wire interface.

Table 3: Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc + 0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k Ohms Pullup resistor, max
			200	pF	1.6 k Ohms pullup resistor max
Rst1L and Rst2L	VIL	-0.3	0.8	V	|Iin|<=125 uA for 0V<Vin,Vcc
	VIH	2	VCC+0.3	V	
ModPrsL,Int1L and Int2L	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	

4.1.3 High Speed Electrical Specification

4.1.3.1 Rx(n) (p/n)

Rx(n)(p/n) are CDFP module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the CDFP module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to the limit in the relevant standard.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the two-wire serial interface. Rx Squelch Disable is an optional function. For specific details refer to Sub clause8.3.5 Control Fields.

4.1.3.2 Tx(n)(p/n)

Tx(n)(p/n) are CDFP module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the CDFP module. The AC coupling is inside the CDFP module and not required on the Host board. The input signal complies with the relevant standard at the module input.

Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched or disabled and the associated TxLOS flag set.

Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the

transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the two-wire serial interface. Tx Squelch Disable is an optional function. For specific details refer to Subclause8.3.5 Control Fields.

4.2 CDFP Power Requirements

The two circuit cards in a CDFP module each have three designated power pins, labeled Vcc. When the CDFP module is "hot plugged" into a connector with power already present, the three pins have power applied concurrently. The module is responsible for limiting the inrush current surge during a hot plug event. The host power supply is responsible for supplying up to the maximum inrush current limits during a hot plug event without causing disturbance to other modules and components on the same power supply.

4.2.1 CDFP Power Classes and Maximum Power Consumption

CDFP modules are categorized into several power classes as listed in Table 4. Power classes apply to each of the two module circuit cards and are advertised in upper page 00h of the management interface, byte 129 (81h).

Table 4: CDFP Maximum Power Class

Power Class	Maximum power dissipation per module card (W)	Maximum total power dissipation per module (W)
1	3.0	6.0
2	4.0	8.0
3	5.0	10.0
4	6.0	12.0
5	>6.0 as defined in page 00, byte 145	>12.0 as defined in page 00, byte 145

The specification of the host power supply filtering network is beyond the scope of this MSA, particularly because of the wide range of CDFP module power classes. An example power configuration is shown in Figure 9. Each module card power supply has a supply filter for the purpose of filtering out high frequency noise and ripple from host-to-module. During a hot-plug event, the filter network limits any voltage drop on the host supply so that neighboring modules sharing the same supply stay within their specified supply voltage limits.

A host board together with the CDFP module(s) forms an integrated power system. The host supplies stable power to the modules. Each module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion. All specifications shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion. Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification.

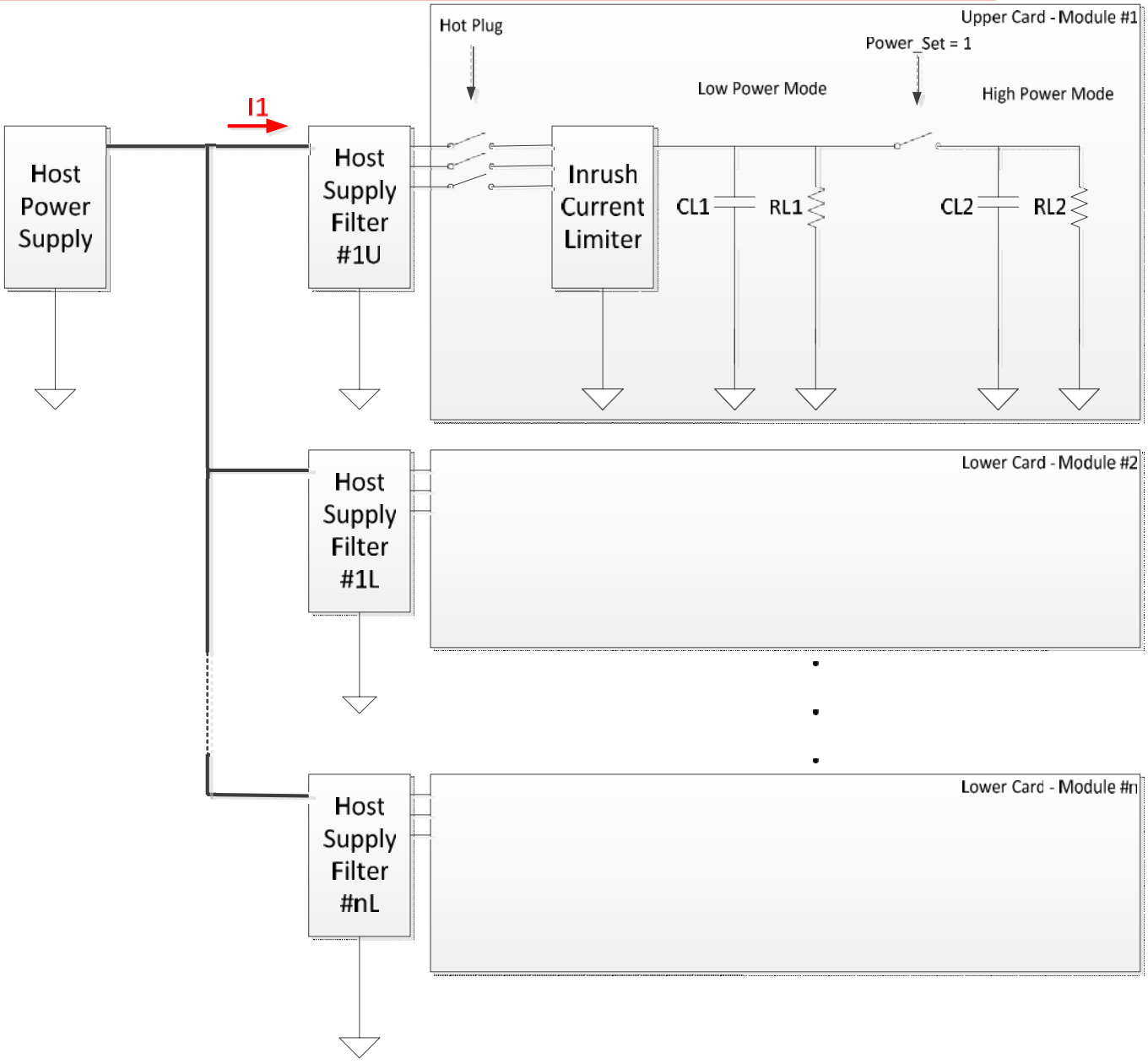


Figure 9: Schematic of multiple CDFP power supply arrangement (example)

4.2.2 CDFP Module Power Supply Requirements

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all CDFP modules shall power up in power class 1, designated as "Low Power Mode". CDFP modules that are class 1 will be fully functional after initialization and remain in low power mode during system operation. All other CDFP modules will only reach fully functional operation after the host system enables "High Power Mode". High power mode is defined as the maximum power class as advertised in page 00, byte 129 and will only be enabled by the host if the host can supply sufficient power to the module. A host system enables high power mode by writing a 1 to the Power Set control bit in byte 93 (5Dh), bit 1. A state transition diagram showing the two power states is shown in 10.

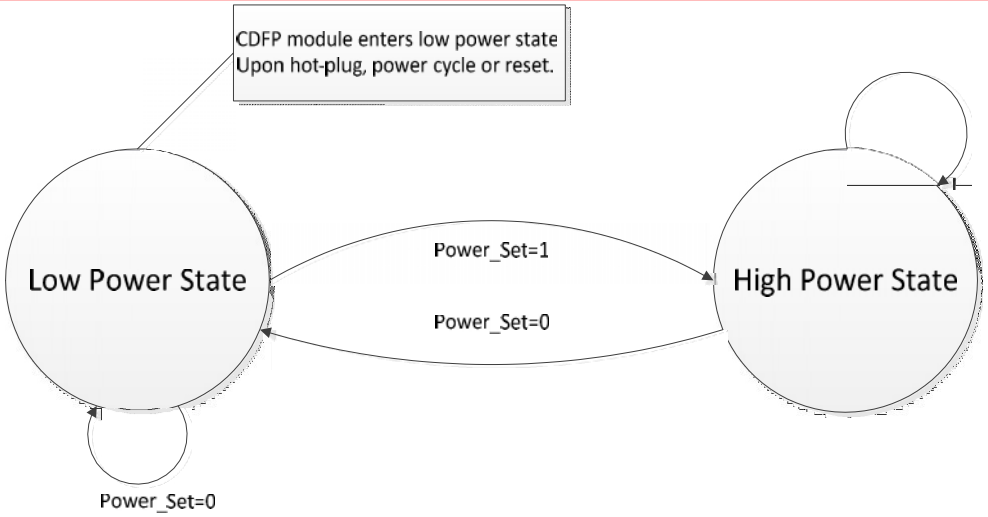


Figure 10: CDFP Power Mode State transition diagram

CDFP modules operate from the host supplied voltage at the three power pins per module card. To protect the host and system operation, each CDFP module during hot plug and normal operation shall follow the requirements listed in Table 5and illustrated in Figure 11. The test configuration for measuring the supply current is a module compliance board (MCB) with reference power supply filters, similar to the circuit shown in SFF-8431, Appendix D and Figure 56. The CDFP MCB can have a single filter per module card or separate filters for each power pin on each module card, depending on the power class and module design. The current limits in Table 5 refer to the current supplied to each module card.

An example current waveform into a host filter, labeled I1 in Figure 9 is plotted in Figure 11. This figure also shows the timing of the initial module turn-on in low power mode, and the later transition to high power mode after the host system has enabled it via the two-wire interface.

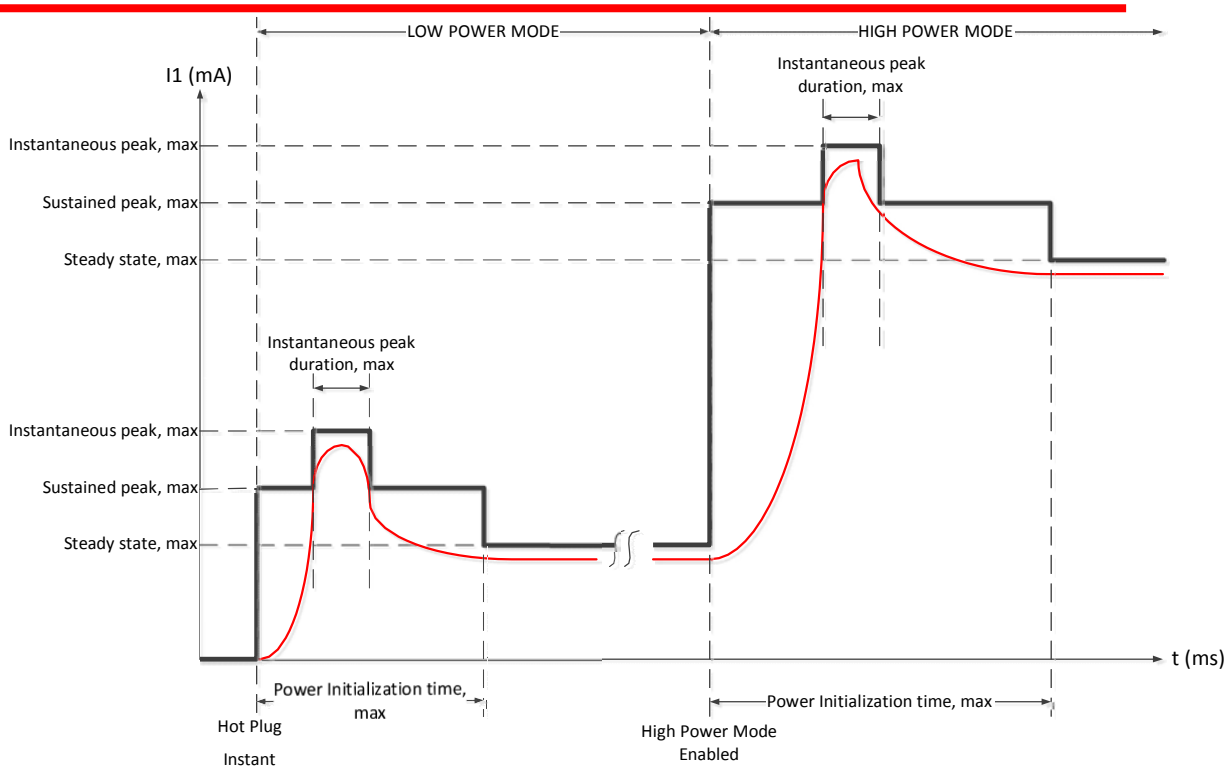


Figure 11: Timing of CDFP inrush currents

Table 5: CDFP Module Power Supply Specification

Parameter	*Symbol*	*Min*	*Nom*	*Max*	*Unit*
Host power supply voltages including ripple, droop and noise below 100 kHz	Vcc_Host	3.135	3.3	3.465	V
Host RMS noise output 10 Hz-10 MHz	e_{N_Host}			25	mV
Module RMS noise output 10 Hz - 10 MHz	e_{N_Mod}			15	mV
Module power supply noise tolerance 10 Hz-10 MHz	$PSNR_{Mod}$			66	mV (p-p)
Module inrush - instantaneous peak duration	T_ip	-	-	50	µs
Module inrush - Power initialization time	PT_init	-	-	500	ms
Power class 1 module card *and low power mode for other modules*					
Power consumption	P_1	-	-	3.0	W
Instantaneous peak current at hot plug	Icc_ip_1	-	-	1200	mA
Sustained peak current at hot plug	Icc_sp_1	-	-	990	mA
Steady state current	Icc_1	-	-	865.8	mA
Power class 2 module card					
Power consumption	P_2	-	-	4.0	W
Instantaneous peak current at hot plug	Icc_ip_2	-	-	1600	mA
Sustained peak current at hot plug	Icc_sp_2	-	-	1320	mA
Steady state current	Icc_2	-	-	1154.4	mA
Power class 3 module card					
Power consumption	P_3	-	-	5.0	W
Instantaneous peak current at hot plug	Icc_ip_3	-	-	2000	mA
Sustained peak current at hot plug	Icc_sp_3	-	-	1650	mA
Steady state current	Icc_3	-	-	1443.0	mA
Power class 4 module card					
Power consumption	P_4	-	-	6.0	W
Instantaneous peak current at hot plug	Icc_ip_4	-	-	2400	mA
Sustained peak current at hot plug	Icc_sp_4	-	-	1980	mA
Steady state current	Icc_4	-	-	1731.6	mA
Power class 5 module card					
Power consumption	P_5	-	-	>6.0	W
Instantaneous peak current at hot plug	Icc_ip_5	-	-	>2400	mA
Sustained peak current at hot plug	Icc_sp_5	-	-	>1980	mA
Steady state current	Icc_5	-	-	>1731.6	mA

4.2.3 CDFP Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the value in Table 5 when tested by the methods of SFF-8431, section D.17.1.

4.2.4 CDFP Module Power Supply Noise Output

The CDFP module shall generate less than the value in Table 5 when tested by the methods of SFF-8431, section D.17.2.

4.2.5 CDFP Module Power Supply Noise Tolerance

The CDFP module shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 5, swept from 10 Hz to 10 MHz according to the methods of SFF-8431, section D.17.3. This emulates the worst case noise output of the host.

4.3 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the CDFP module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case. The CDFP module and host high speed signal contacts shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The CDFP module and all host contacts with exception of the module and host high speed signal contacts shall withstand 2 kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

5 Mechanical and Board Definition

5.1 Introduction

The modules defined in this clause are illustrated in Figures 12 and 13. All pluggable modules and direct attach cable plugs must mate to the connector and cage design defined in this specification. There are two module/cage designs defined as 'Style 1' and 'Style 2/Style 3'. Style 1 is a short body module (shown in Figure 12) and Style 2/Style 3 is a longer body module (shown in Figure 13). Style 1, Style 2 and Style 3 modules/cages are mechanically keyed. Therefore style 1, style 2 and style 3 modules/cages are not intermateable. The CDFP optical interface shall meet the dimensional specifications of the MPO16 per IEC 61754-7 interface 7-3. Other optical interface solutions such as MXC are left to the discretion of the optical module supplier. The MPO16 adapter shall optically mate with the plug on the optical fiber cabling. Heat sink/clip thermal designs are application specific and not specifically defined by this specification; however a general design is given as an example.

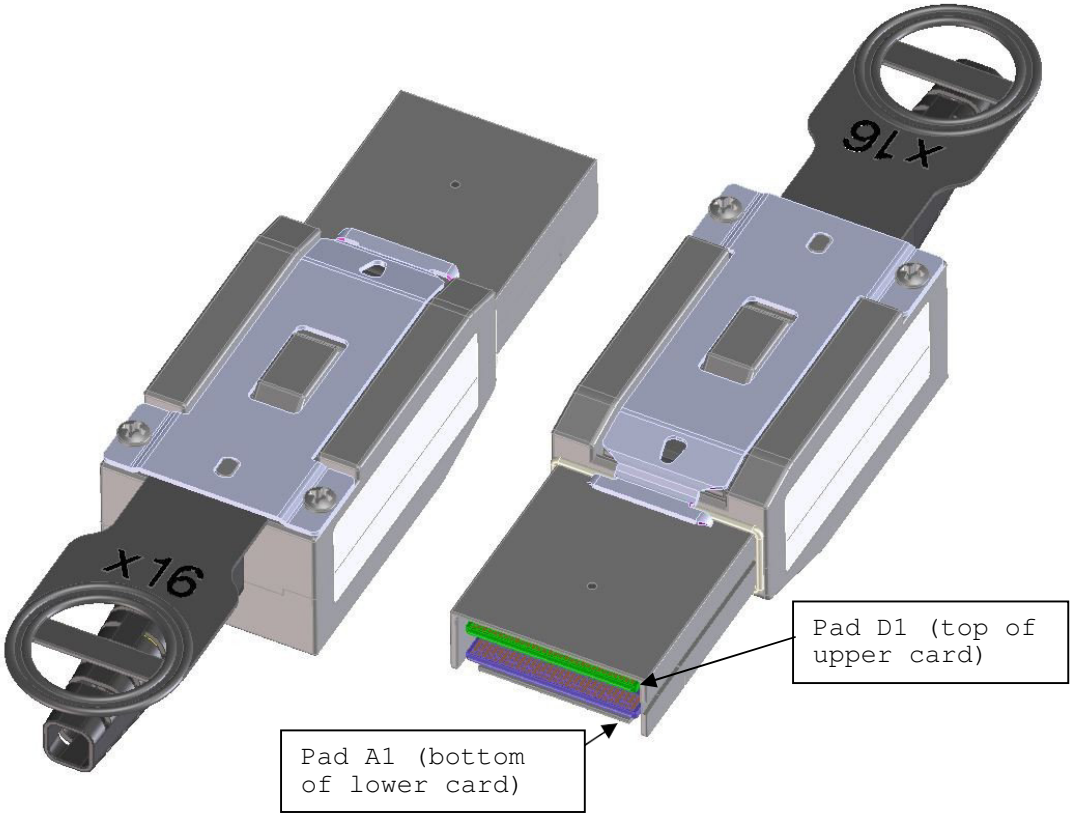


Figure 12: CDFP Style 1 direct attach module rendering

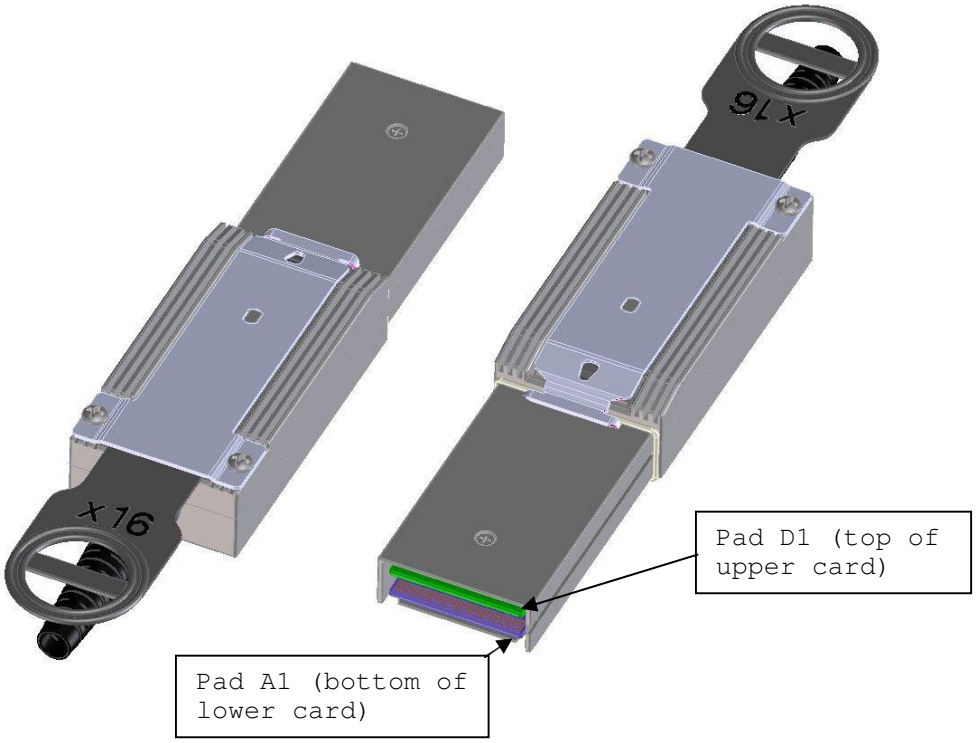


Figure 13: CDFP Style 2 and Style 3 direct attach module rendering

5.2 CDFP Datum's and Component Alignment

A listing of the datum's for the various components is contained in Table 6. The alignments of some of the datum's are noted. The relationship of the Module, Cage, and Connector relative to the Host Board and Bezel is illustrated in Figures 14 and 15 by the location of the key datum's of each of the components. In order to reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified.

Table 6: Definition of Datum’s

Datum	Description
A	Host Board Top Surface
B	Inside surface of bezel
C	**Distance between Connector terminal thru holes on host board
D	*Hard stop on Module
E	**Width of Module
F	Height of Module housing
G	**Width of Module pc board
H	Leading edge of signal contact pads on Module pc board
J	Top surface of Module pc board
K	*Host board thru hole #1 to accept connector guide post
L	*Host board thru hole #2 to accept connector guide post
M	**Width of bezel cut out
N	*Connector alignment pin
P	**Width of inside of cage at EMI gasket (when fully compressed)
R	Height of inside of cage at EMI gasket (when fully compressed)
S	Seating plane of cage on host board
T	*Hard stop on cage
V	Length of heat sink clip
W	Seating surface of the heat sink on the cage
X & Y	Host board horizontal and depth datum’s
Z	**Width of heat sink surface that fits into clip
AA	**Connector slot width
BB	Seating plane of cage on host board
CC	Length of boss on heat sink that fits inside of the cage
DD	Top surface of connector back shell
*Datum’s D, K, L, N and T are aligned when assembled (see figures 14 and 15) **Centerlines of datum’s AA, C, E, G, M, P and Z are aligned on the same vertical axis	

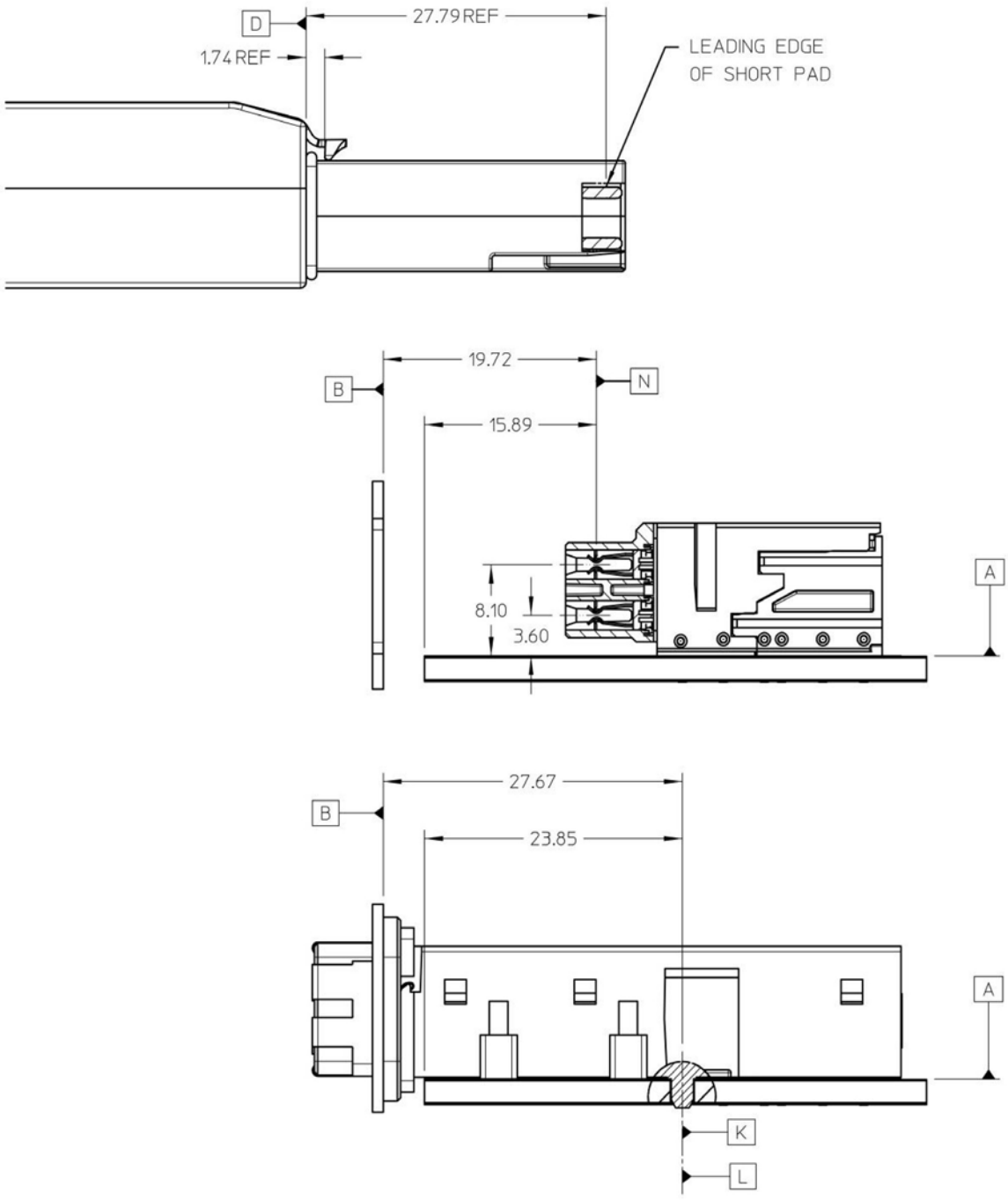


Figure 14: CDFP Style 1 Datum Alignment, Depth

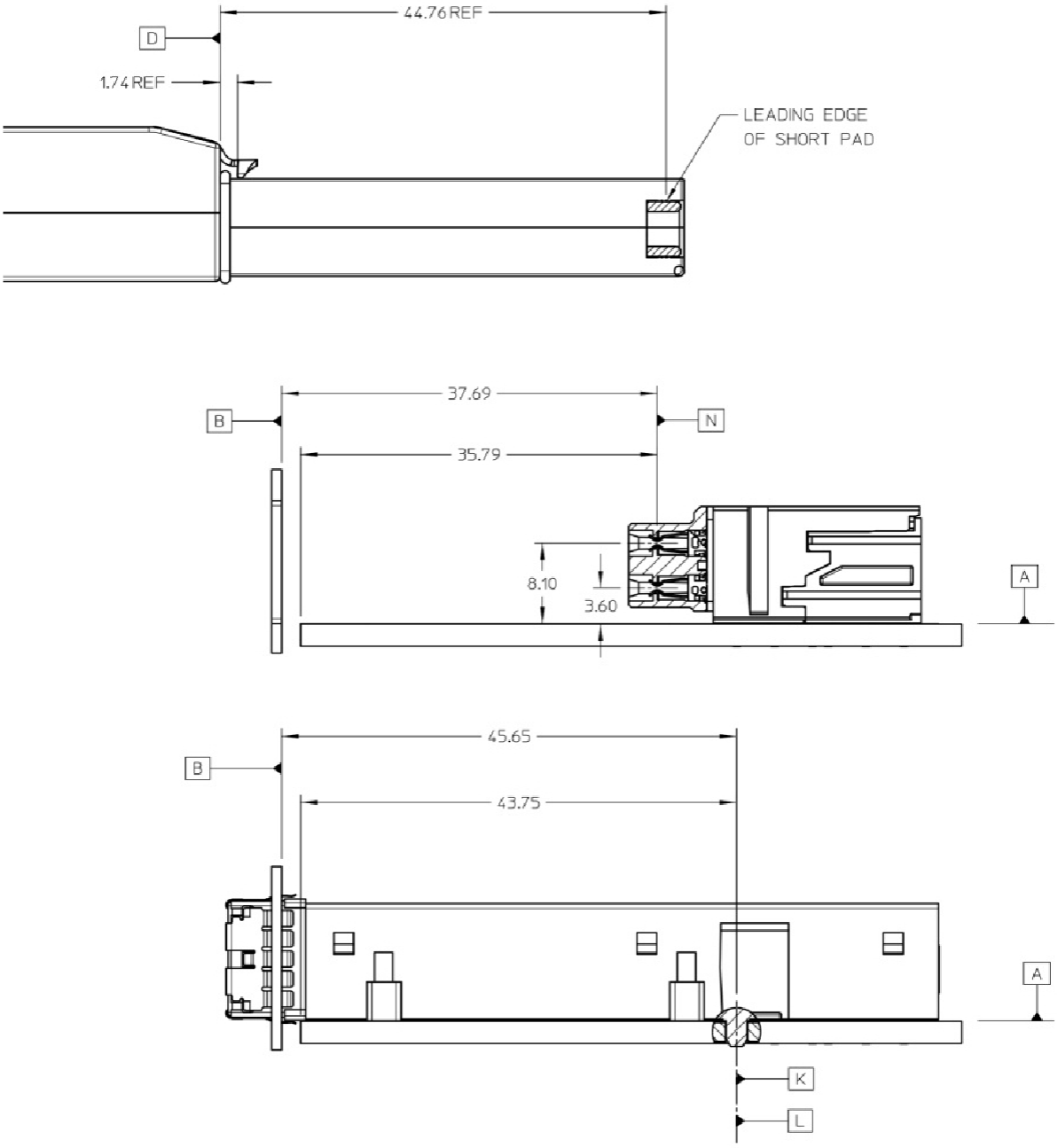


Figure 15: CDFP Style 2 and Style 3 Datum Alignment, Depth

5.3 CDFP Module Mechanical Package Dimensions

A mechanical outline is used for all CDFP Modules and direct attach cables. The preferred method of removing the module from the cage assembly is by a pull tab type actuation method. The module shall provide a means to self-lock with the cage upon insertion. The package dimensions for the CDFP Module are defined in Figures 16, 19 and 23. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions in Figures 16, 19 and 23. Note: All dimensions are in mm.

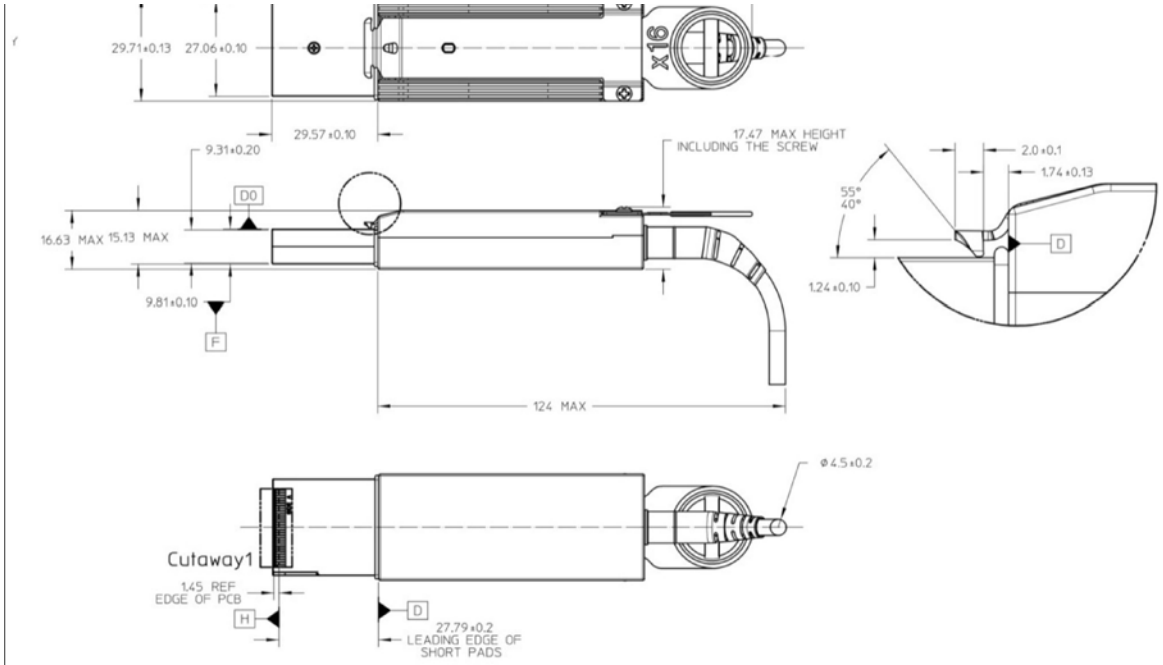
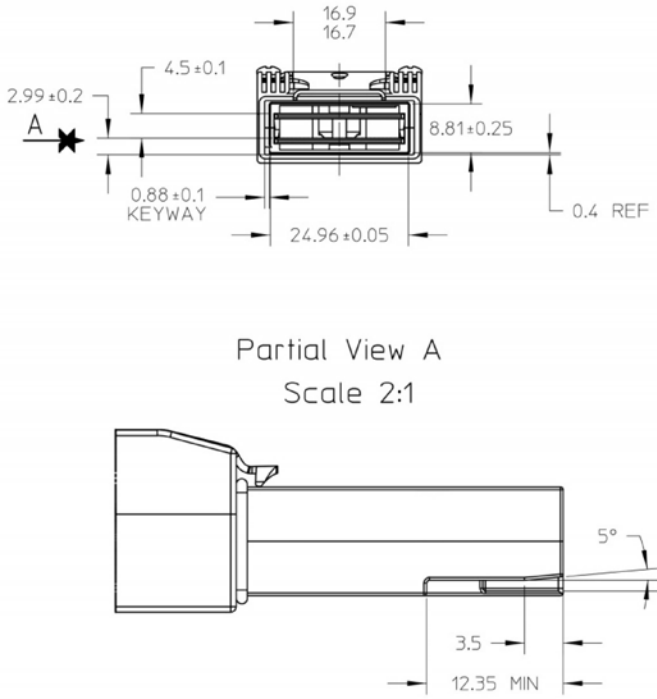


Figure 16: Drawing of CDFP Style 1 Module



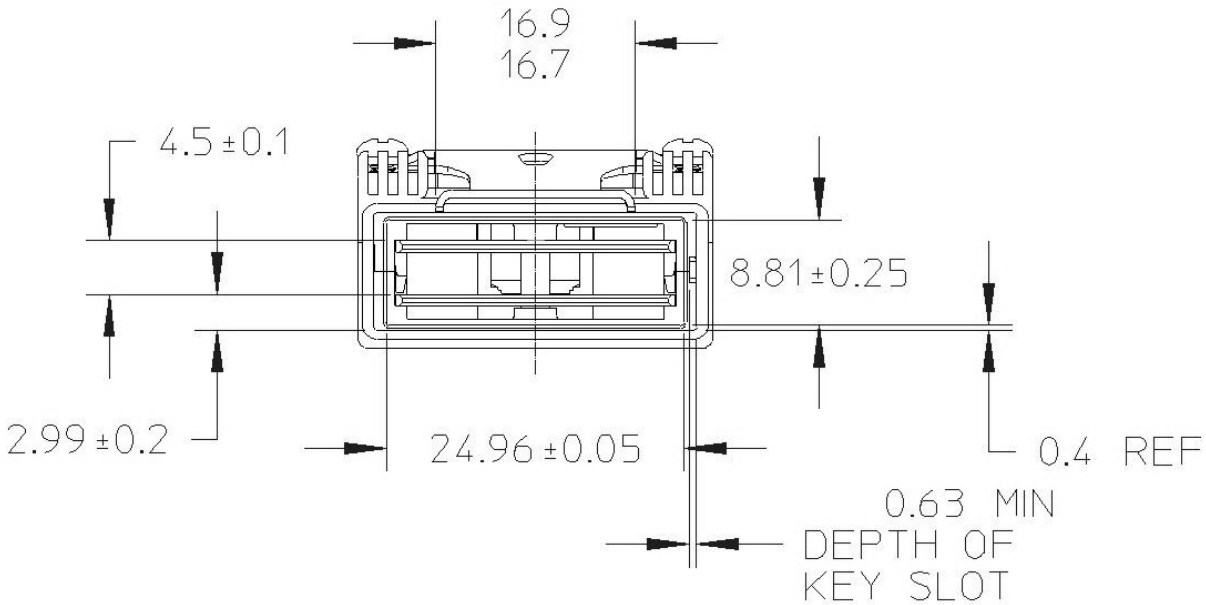
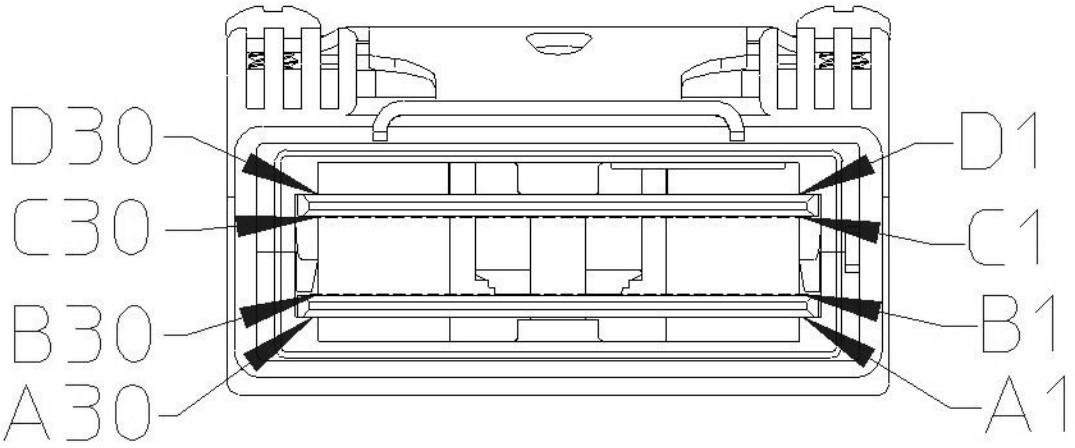


Figure 17: View of module plug Style 1



\

Figure 18: Plug pin assignments Style 1 Module

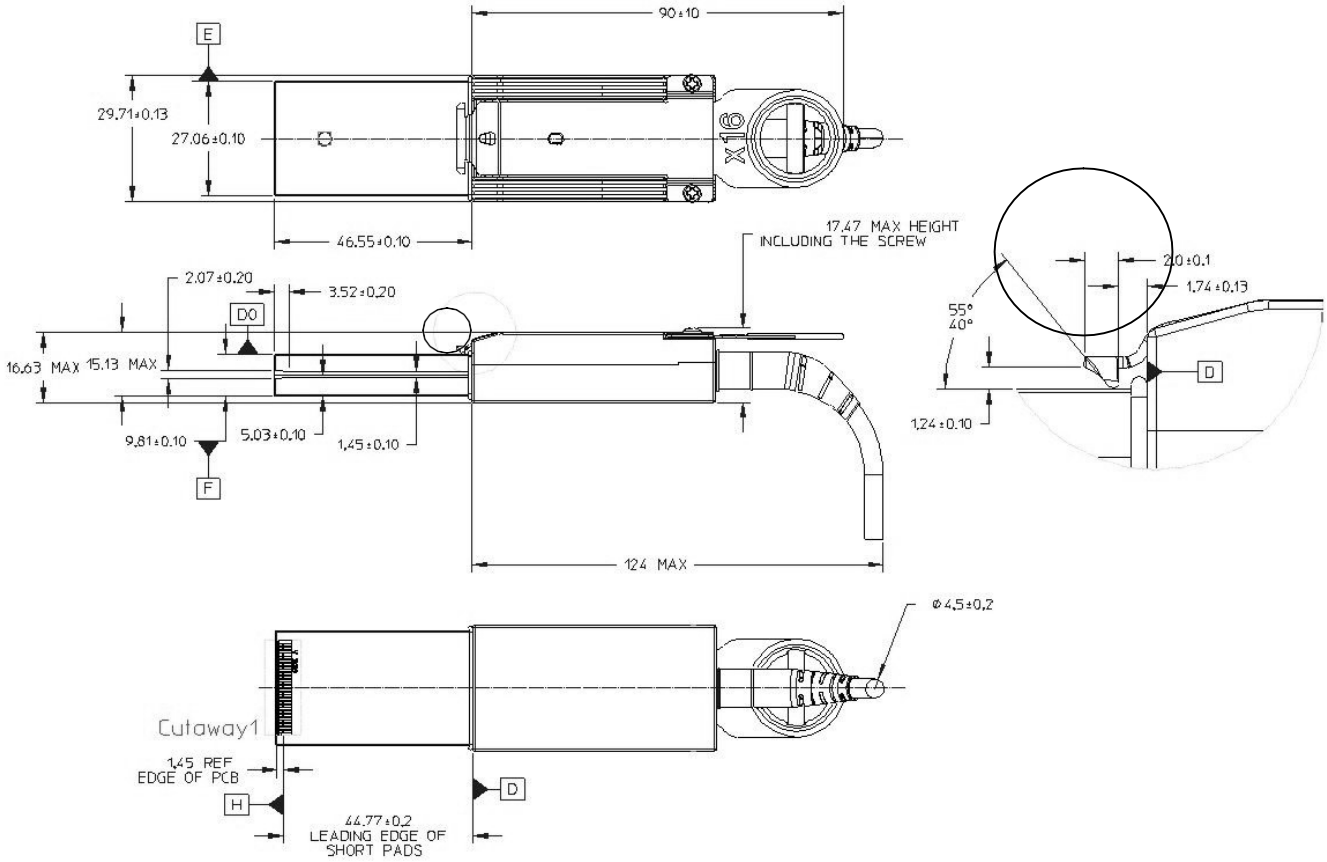


Figure 19: Drawing of CDFP Style 2 Module

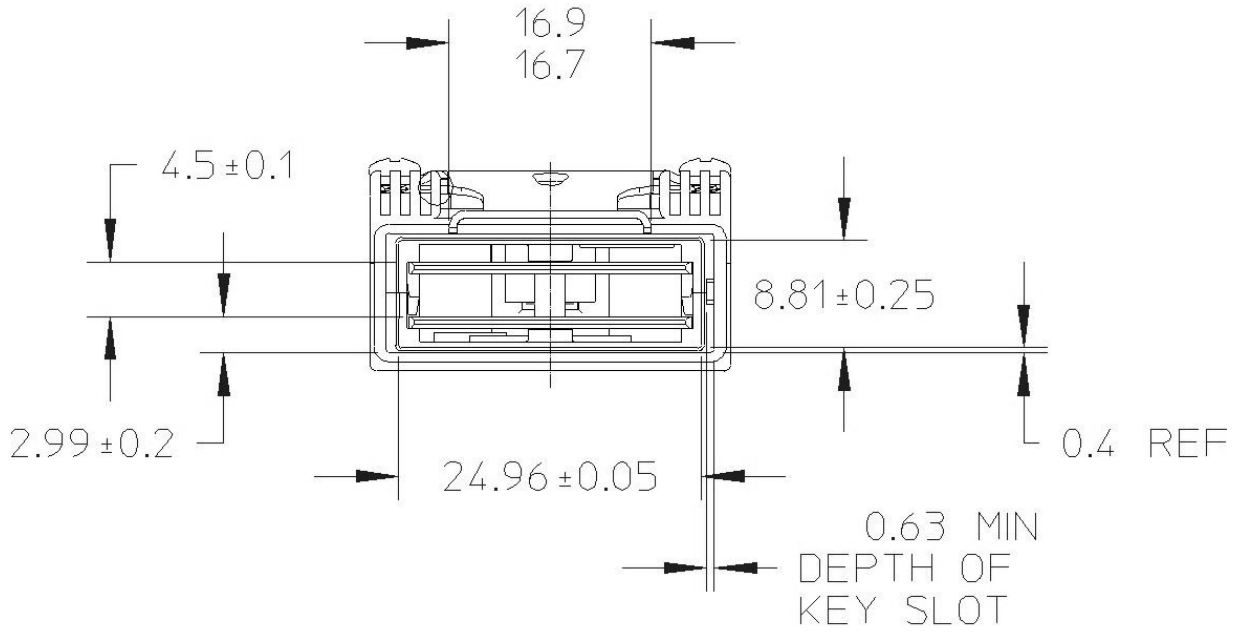


Figure 20: View of module plug Style 2

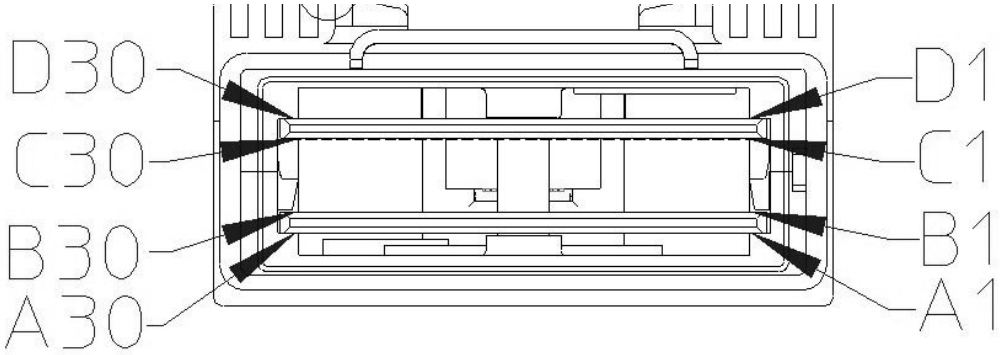


Figure 21: Plug pin assignments Style 2 Module

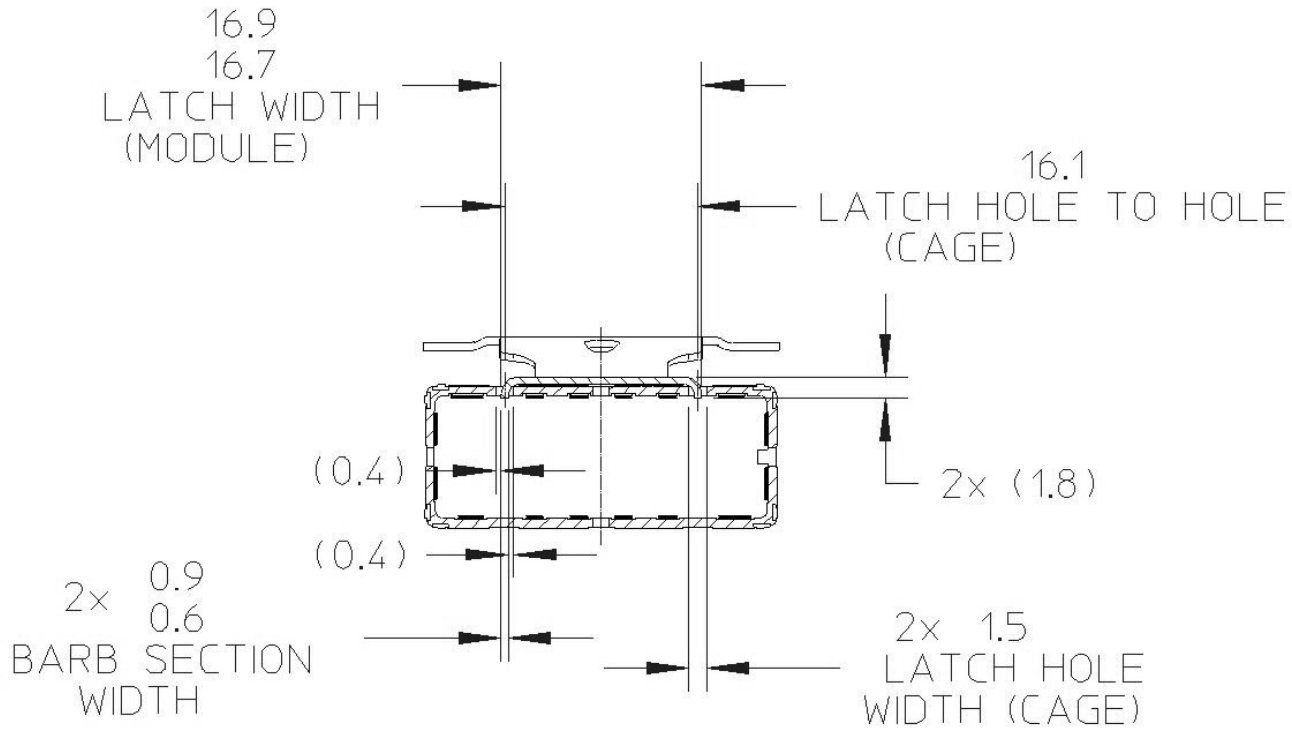


Figure 22: Latch Definition Style 1/Style 2/Style 3

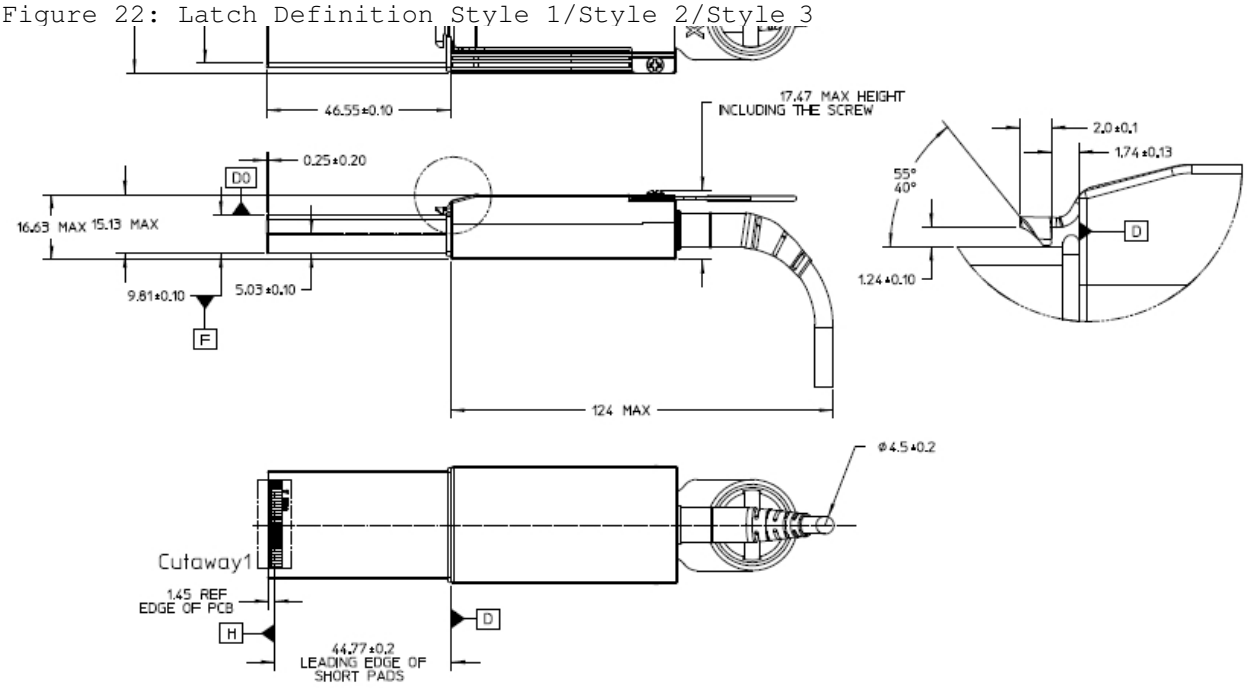


Figure 23: Drawing of CDFP Style 3 Module

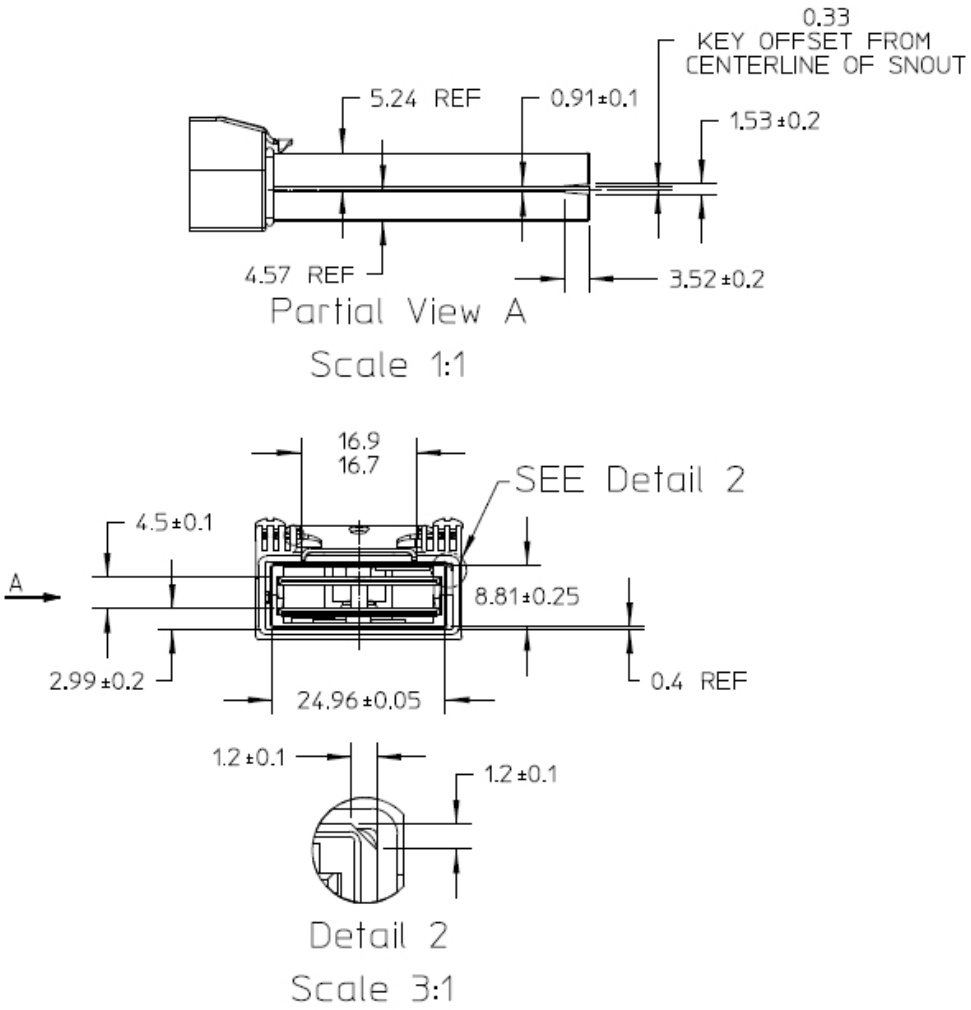


Figure 24: View of module plug Style 3

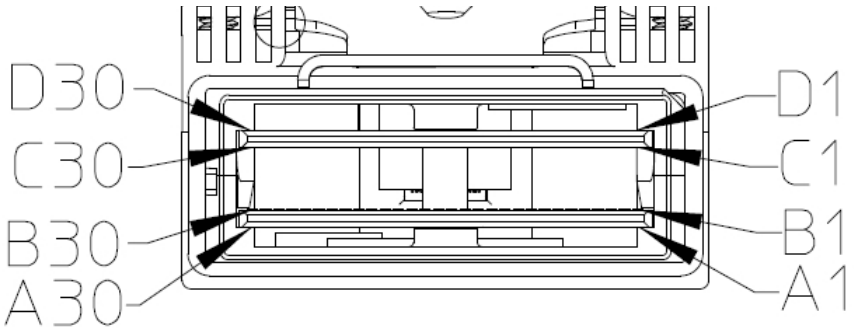


Figure 25: Plug pin assignments Style 3 Module

5.3.1 Mating of CDFP Module PCB to CDFP Electrical Connector

The CDFP Module contains a printed circuit board that mates with the CDFP electrical connector. The pads are designed for a sequenced mating:

First mate – ground contacts
Second mate – power contacts
Third mate – signal contacts

The pattern layout for the CDFP Printed Circuit Board is shown in Figure 19.

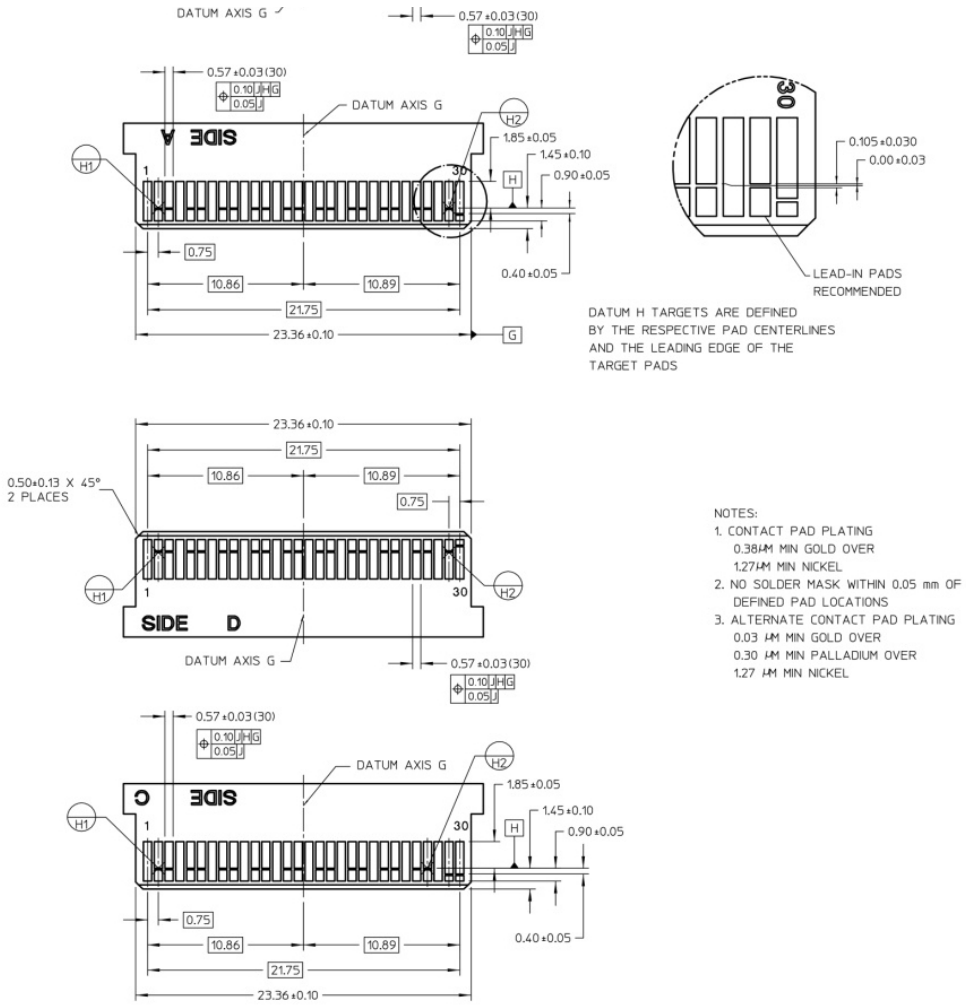


Figure 26: Pattern Layout for CDFP Style 1/Style 2/Style 3 Printed Circuit Board

5.4 Host PCB Layout

A typical host board mechanical layout for attaching the CDFP Host Connector and Cage System is shown in
Figure 27 and Figure 28. Location of the pattern on the host board is application specific. See Sub clause 5.6 for details on the location of the pattern relative to the bezel.

To achieve 25 Gb/s performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.

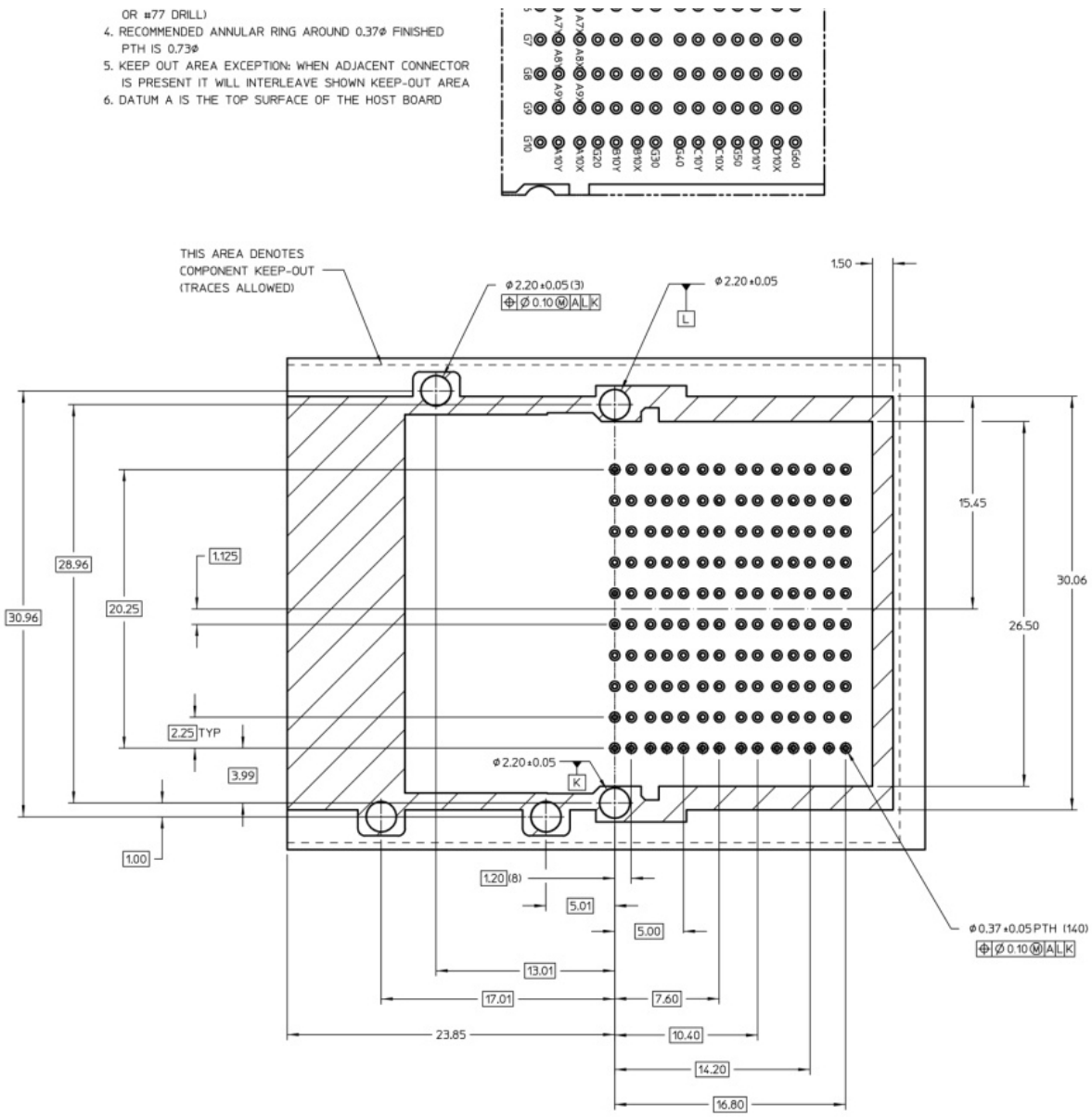


Figure 27: CDFP Style 1 Host PCB Mechanical Layout

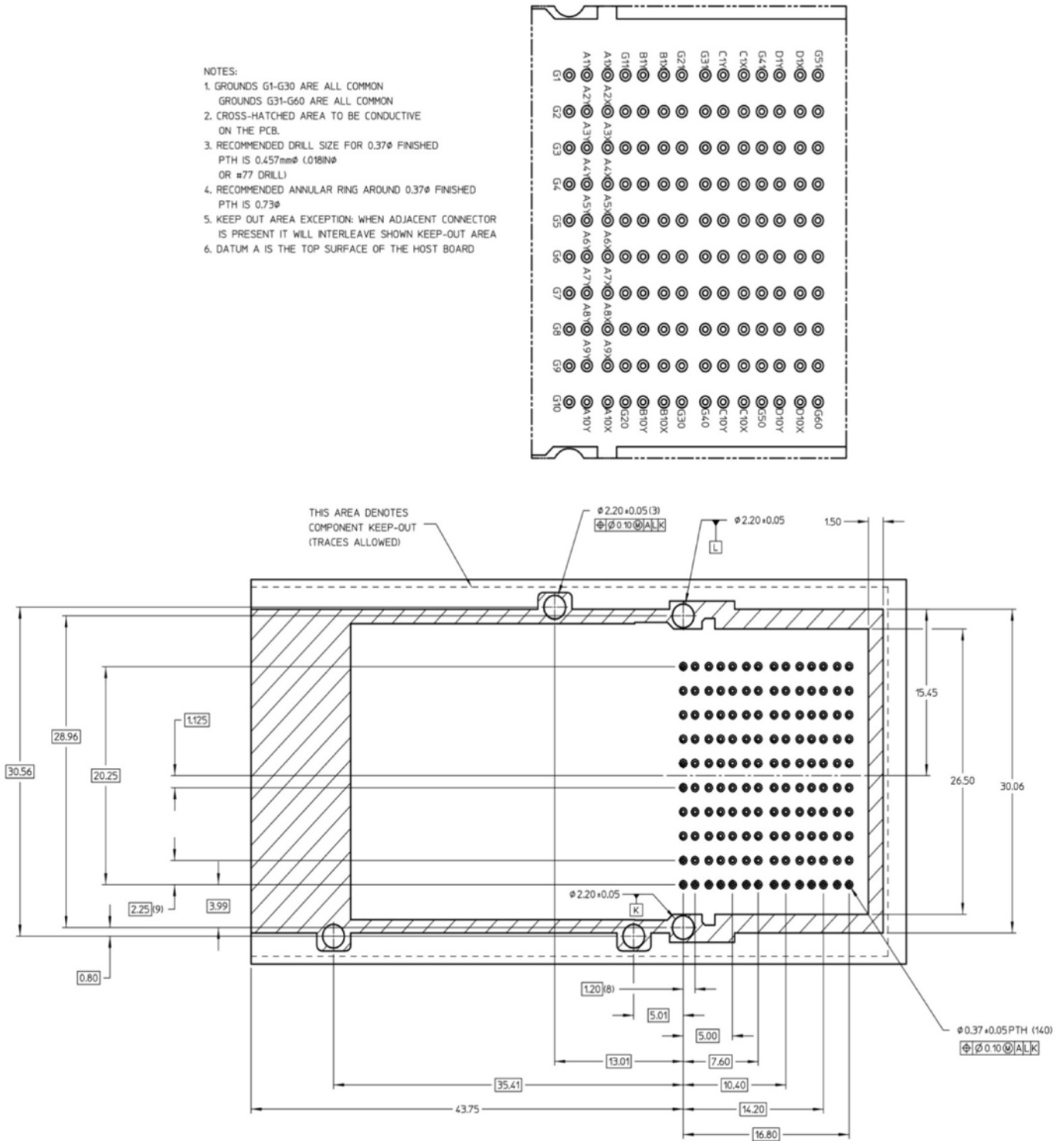


Figure 28: CDFP Style 2 and Style 3 Host PCB Mechanical Layout

5.4.1 Insertion, Extraction and Retention Forces for CDFP Modules

The requirements for insertion forces, extraction forces and retention forces are specified in Table 7. The CDFP cage and module design combinations must ensure excessive force applied to a cable does not damage the CDFP cage or host connector. If any part is damaged by excessive force, it should be the cable or media module and not the cage or host connector which is part of the host system.

Table 7: Insertion, Extraction and Retention Forces

Measurement	Min	Max	Units	Comments
CDFP Module insertion	0	40	N	
CDFP Module extraction	0	30	N	
CDFP Module retention	90	N/A	N	No damage to module below 90N
Cage retention (Latch strength)	180	N/A	N	No damage to latch below 180N
Cage retention in Host Board	114	N/A	N	Force to be applied in a vertical direction, no damage to cage
Insertion / removal cycles, connector / cage	100	N/A	Cycles	Number of cycles for the connector and cage with multiple modules.
Insertion / removal cycles, CDFP Module	50	N/A	Cycles	Number of cycles for an individual module.

5.5 Bezel for Systems Using CDFP Modules

Host enclosures that use CDFP devices should provide appropriate clearances between the CDFP Modules to allow insertion and extraction without the use of special tools and a bezel enclosure with sufficient mechanical strength. The CDFP Module insertion slot should be clear of nearby moldings and covers that might block convenient access to the latching mechanisms, the CDFP Module, or the cables that plug directly into the cage.

The minimum recommended host board thickness for belly-to-belly mounting of the assemblies is defined in 5.5.1.

The bezel thickness range shall be 0.8 mm to 2.6 mm.

5.5.1 Cage Assembly

The front surface of the cage assembly passes through the bezel.

The bezel surfaces must be conductive and connected to chassis ground.

The minimum recommended host board thickness for belly to belly mounting of the connector and cage assemblies is 2.2mm minimum.

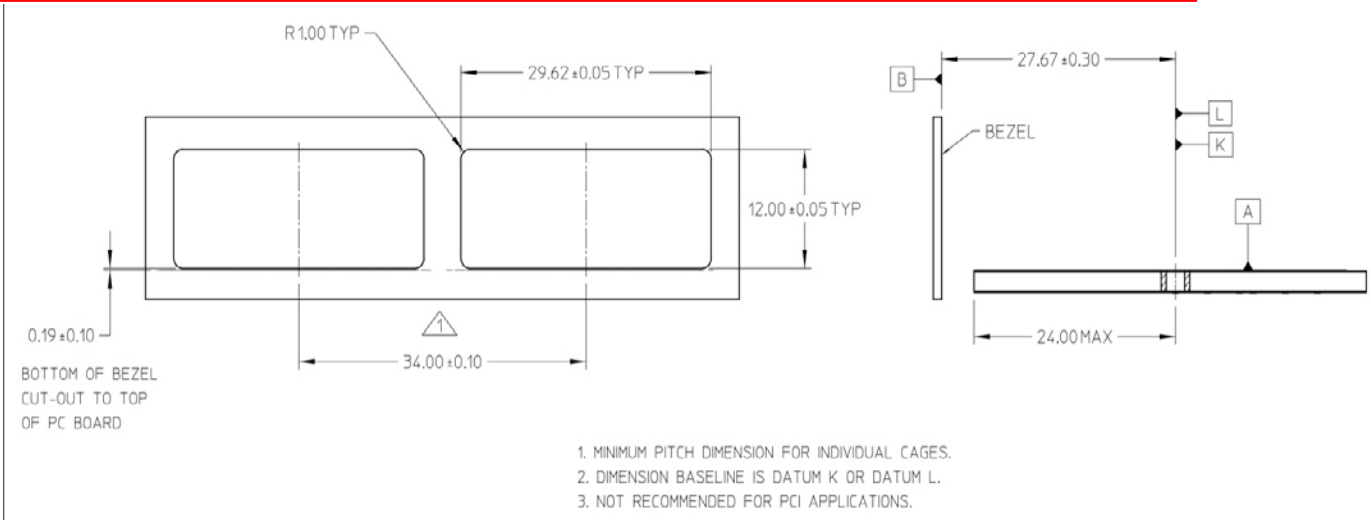


Figure 29: CDFP Style 1 Recommended Bezel Design

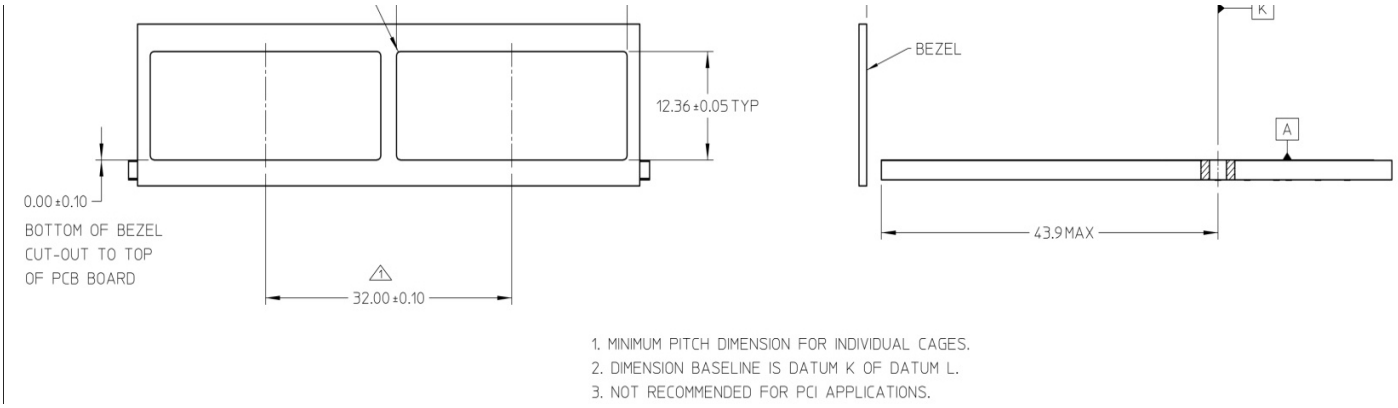


Figure 30: CDFP Style 2 and Style 3 Recommended Bezel Design

5.6 CDFP Host Electrical Connector and Cage

Figure 31 shows the host connector in a Style 1 cage assembly. Figure 32 shows the host connector in a Style 2 cage assembly. Figure 33 shows the host connector in a Style 3 cage assembly.

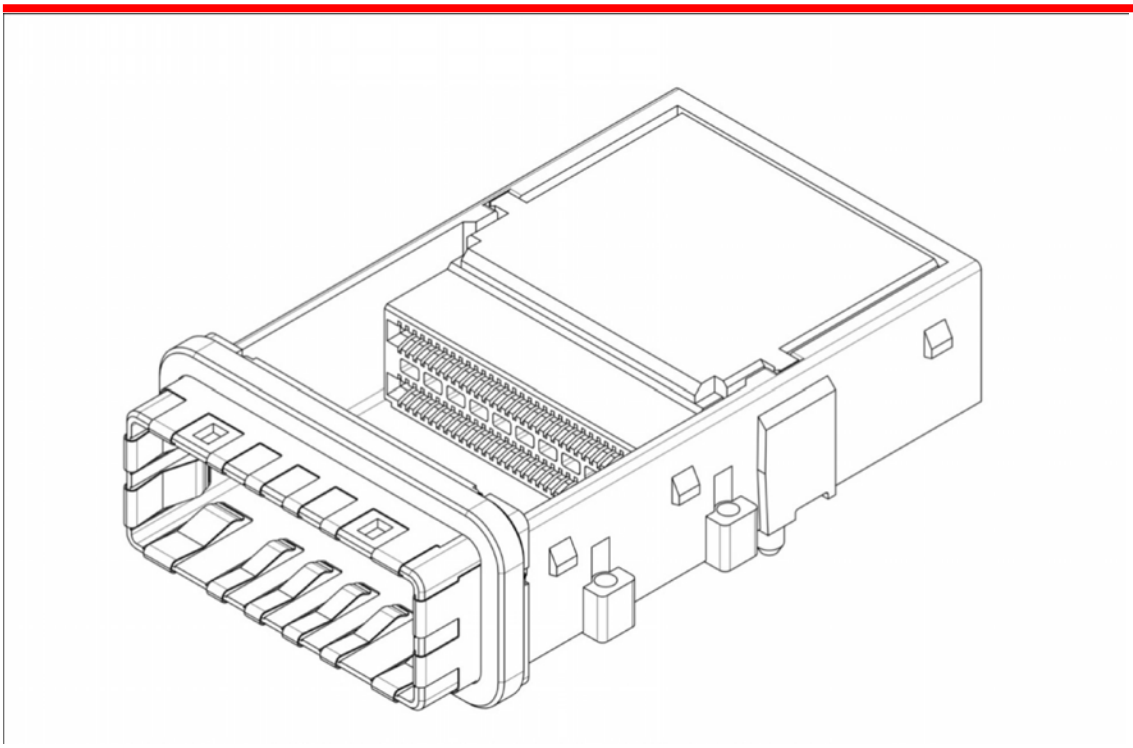


Figure 31: CDFP Style 1 Host Electrical Connector and Cage Illustration

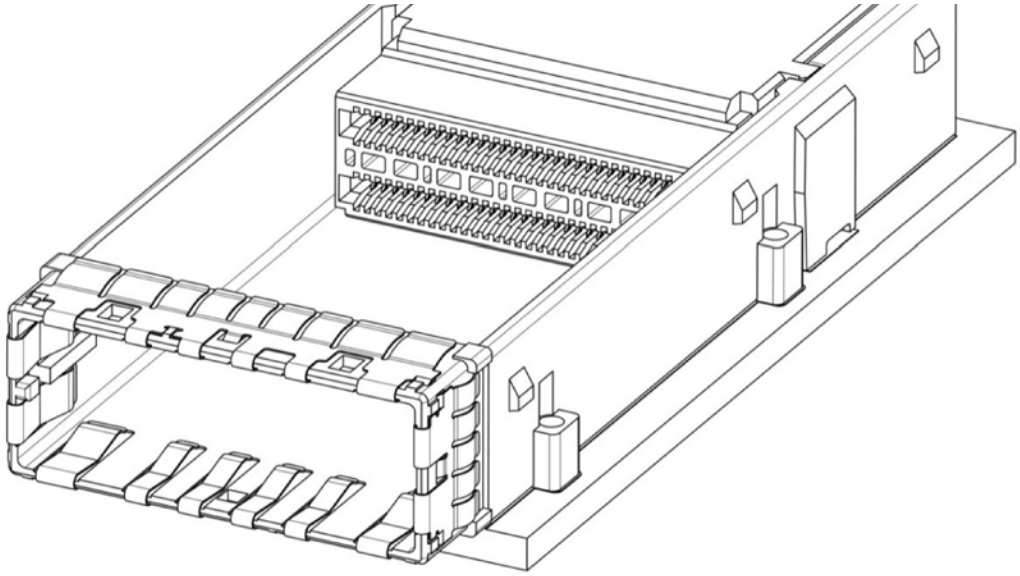


Figure 32: CDFP Style 2 Host Electrical Connector and Cage Illustration

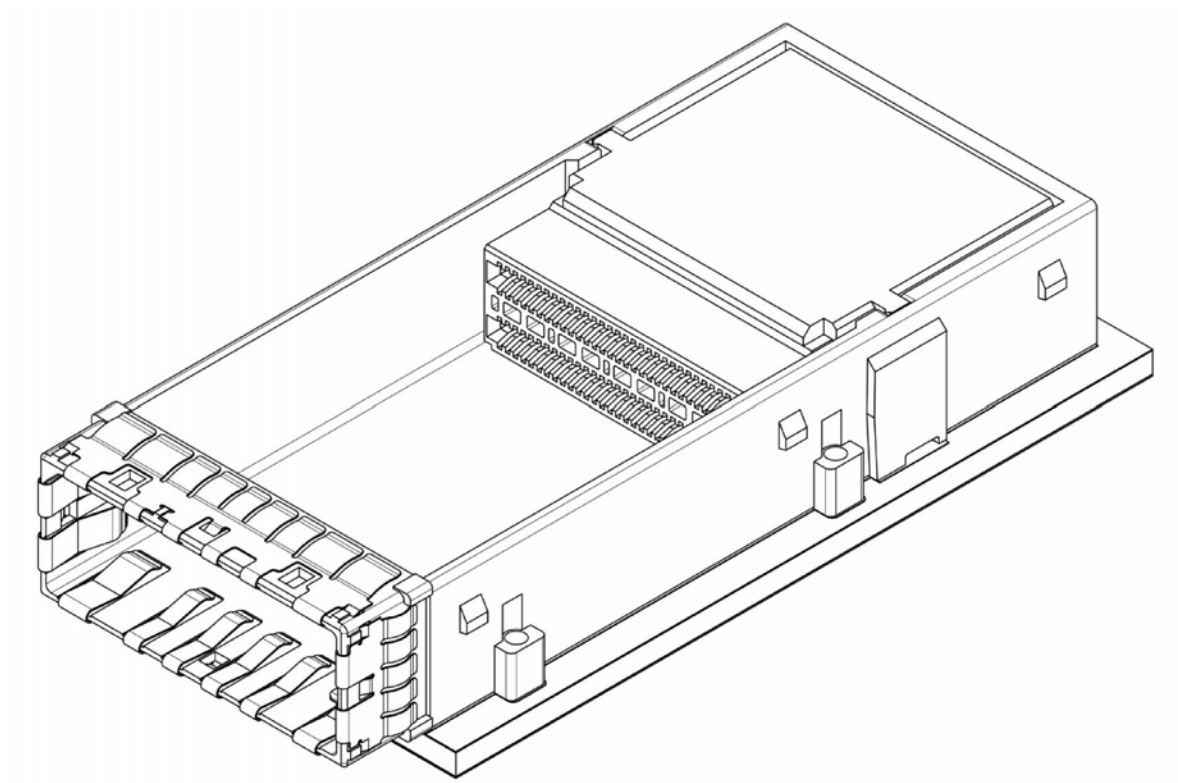


Figure 33: CDFP Style 3 Host Electrical Connector and Cage Illustration

5.7 CDFP Host Electrical Connector

The CDFP host electrical connector is a 120-contact, right angle press-fit connector. The mechanical specifications for the connector are listed in Table 6 and shown in Figure 34. Note: The connector shown is identical for Style 1, Style 2 and Style 3.

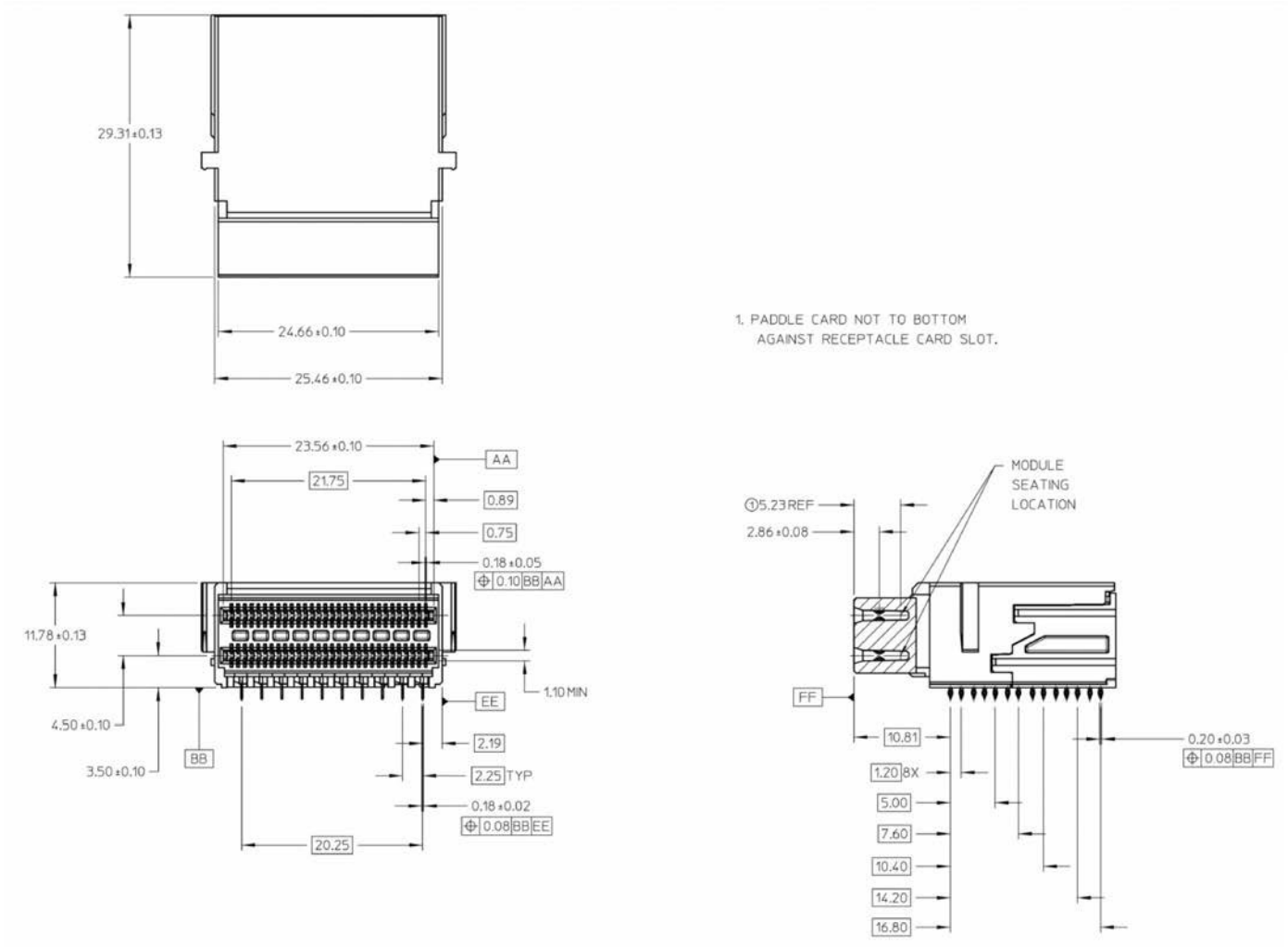


Figure 34: CDFP Host Electrical Connector Specification

5.8 Individual CDFP Cage Assembly Versions

There are three Styles for cage assemblies: Style 1 uses a gasket ring for EMI suppression. Style 2 and Style 3 use spring fingers for EMI suppression. An exploded view of the Style 1 cage assembly is shown in Figure 35. An exploded view of the Style 2 cage assembly is shown in Figure 36 and an exploded view of the Style 3 cage assembly is shown in Figure 37. Style 1 cages are mechanically keyed to only accept Style 1 modules. Style 2 cages are mechanically keyed to only accept Style 2 modules. Style 3 cages are mechanically keyed to only accept Style 3 modules.

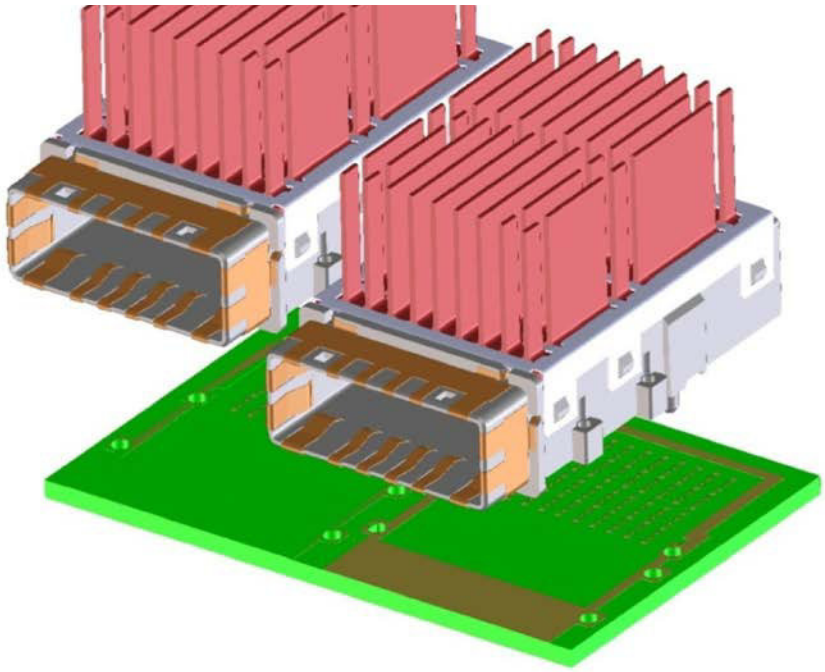


Figure 35: Style 1 Cage and Optional Heat Sink Design (exploded view)

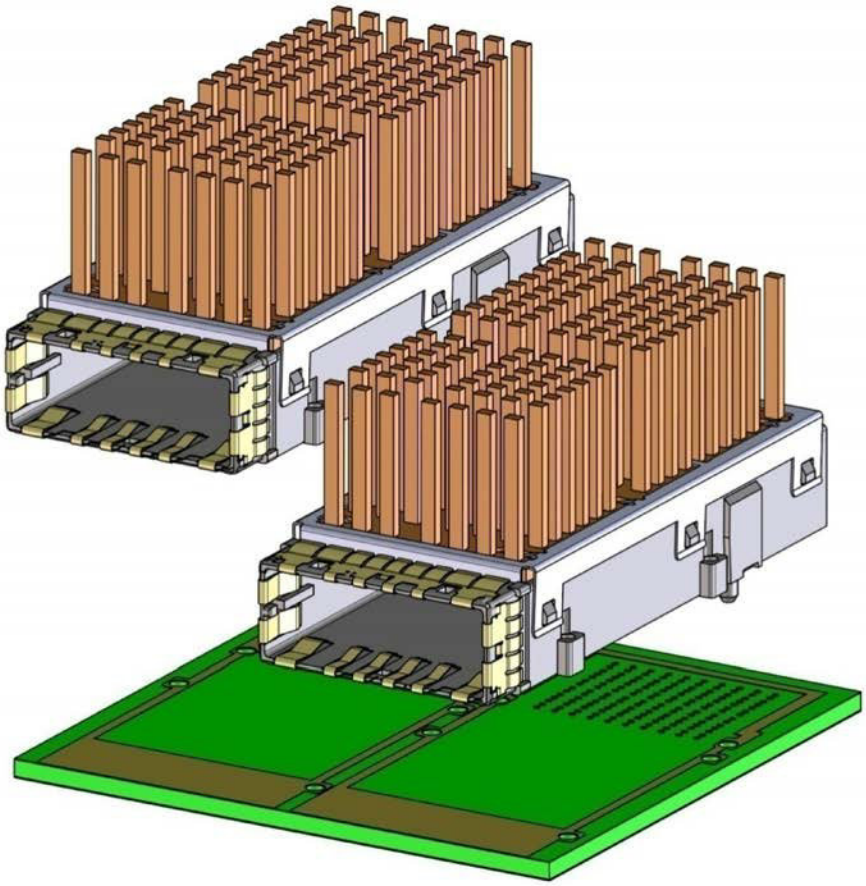


Figure 36: Style 2 Cage and Optional Heat Sink Design (exploded view)

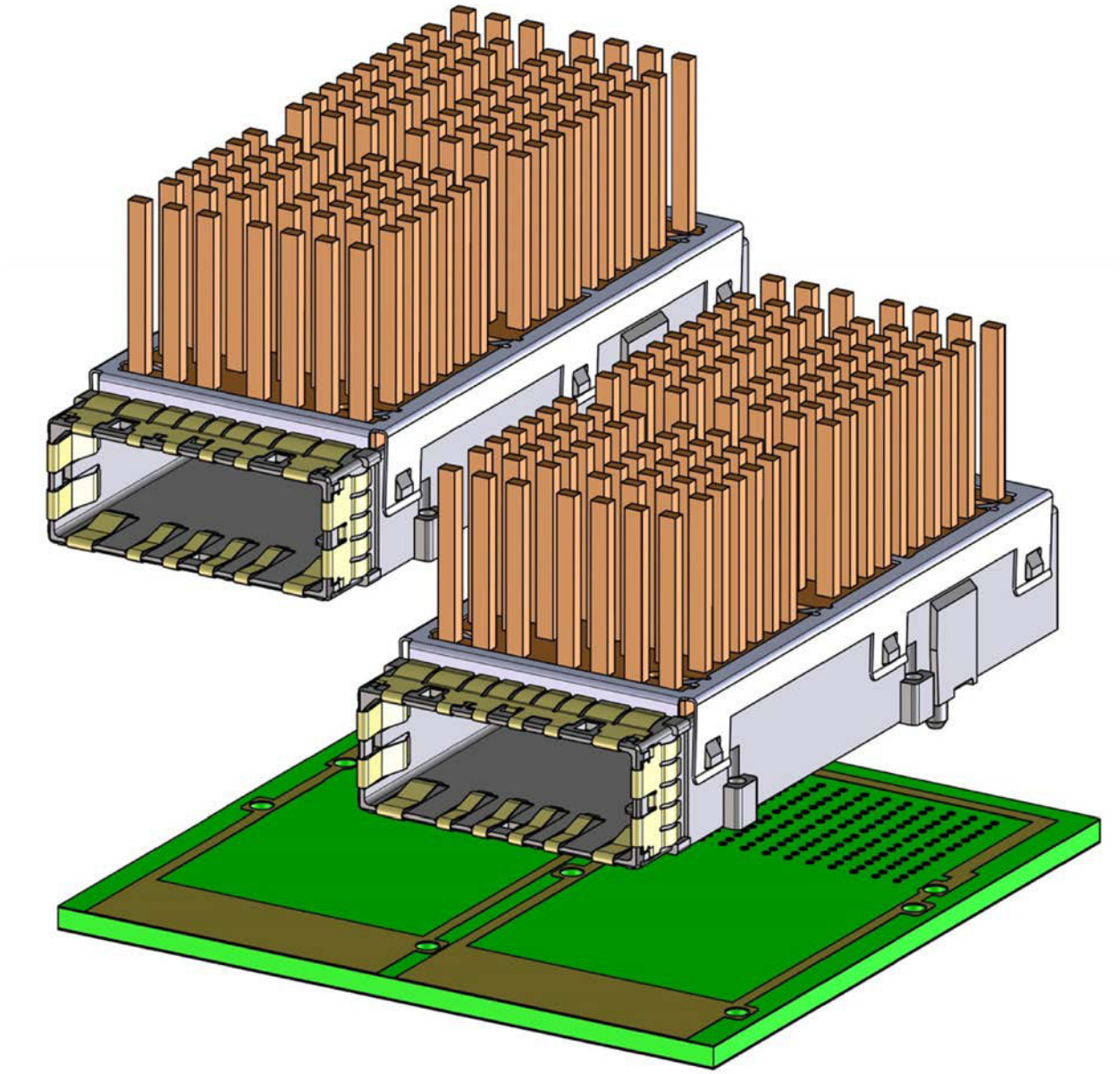


Figure 37: Style 3 Cage and Optional Heat Sink Design (exploded view)

The detailed drawings for the Style 1, Style 2 and Style 3 cage assemblies are shown in Figures 38, 39 and 40.

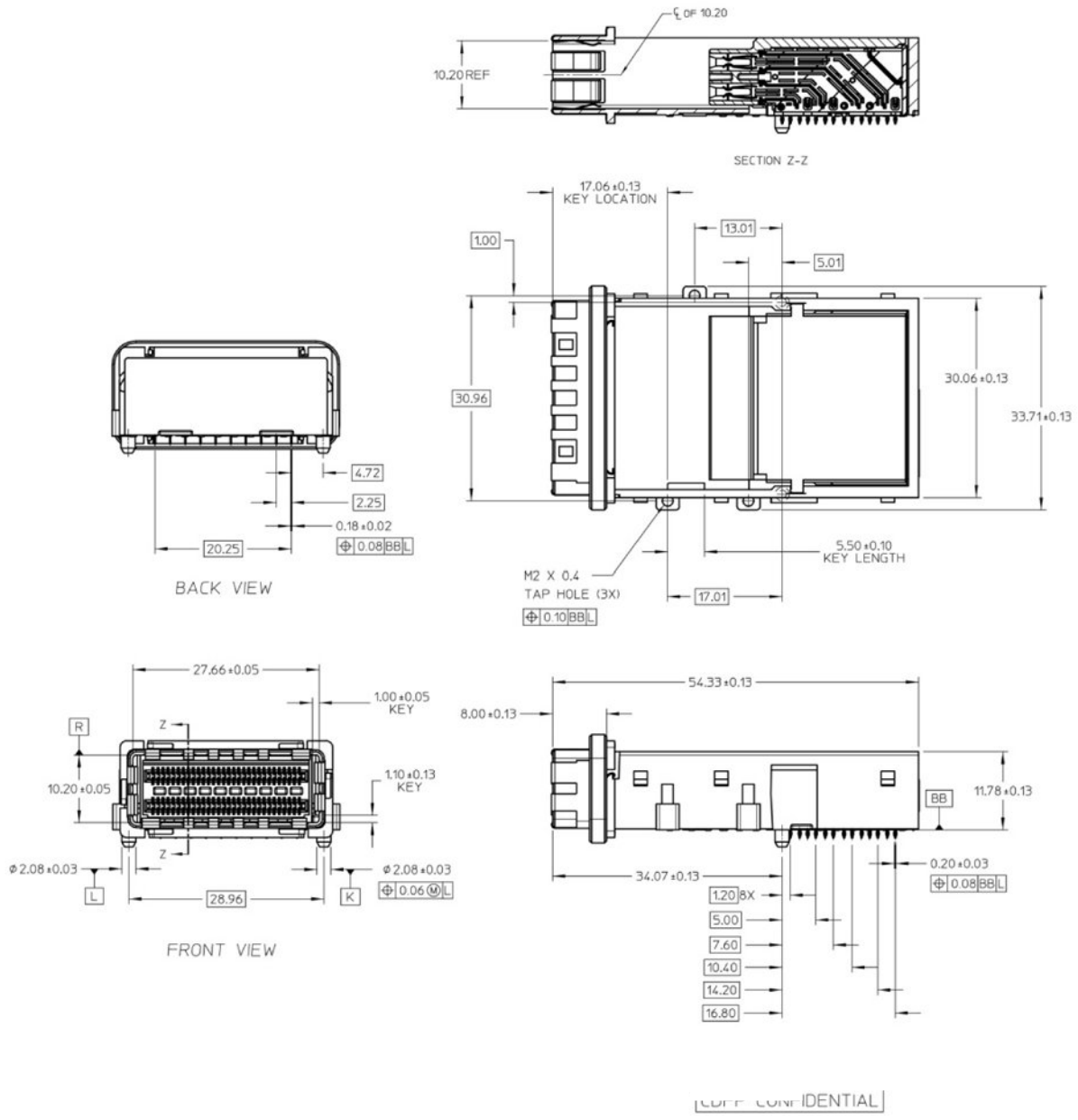


Figure 38: Style 1 1-by-1 Cage Design

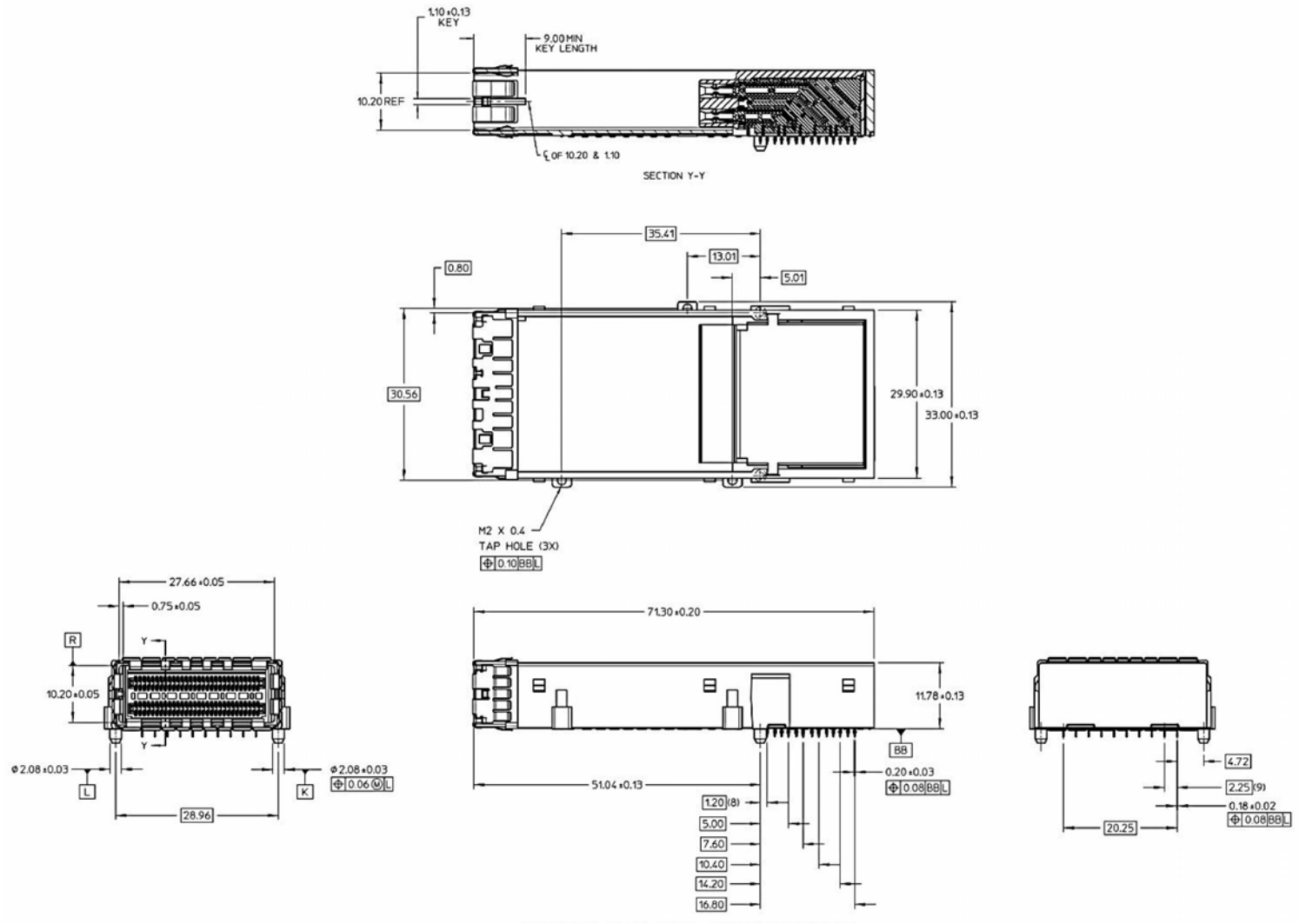


Figure 39: Style 2 1-by-1 Cage Design

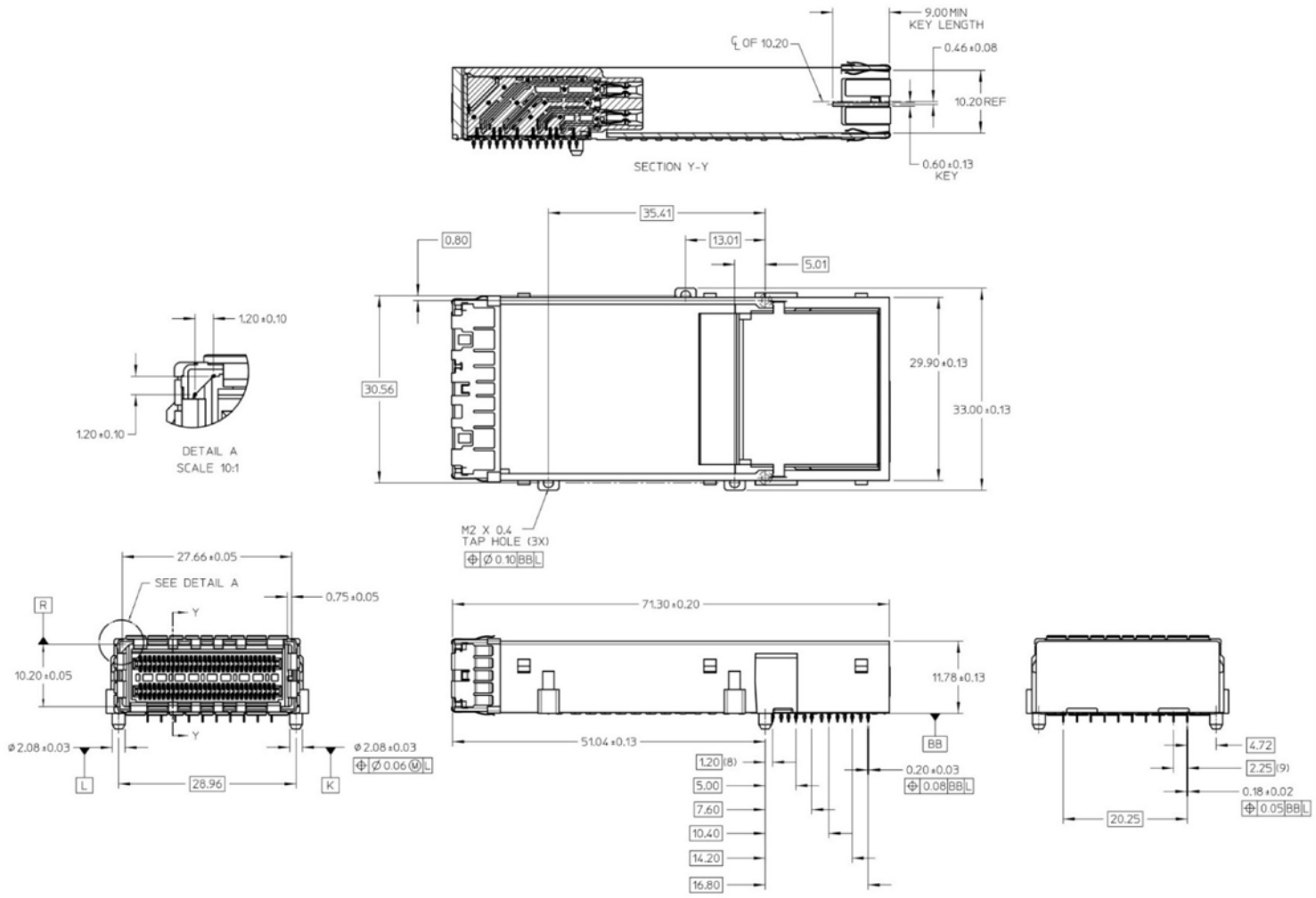


Figure 40: Style 3 1-by-1 Cage Design

5.8.1 CDFP Heat Sink Clip Dimensions

The heat sink clip and attachment points defined in Figures 41-44 are for reference only. The design of the heat sink clip, heat sink and their attachment features on the connector/cage assembly are vendor specific and not defined in this document. When fastened to the cage, the clip will provide a minimum force of 5 Newtons at the interface of the heat sink and CDFP Module. The clip is designed to permit a heat sink to be fastened into the clip then assembled to the cage and to expand slightly during module insertion in order to maintain a contact force between the module and heat sink.

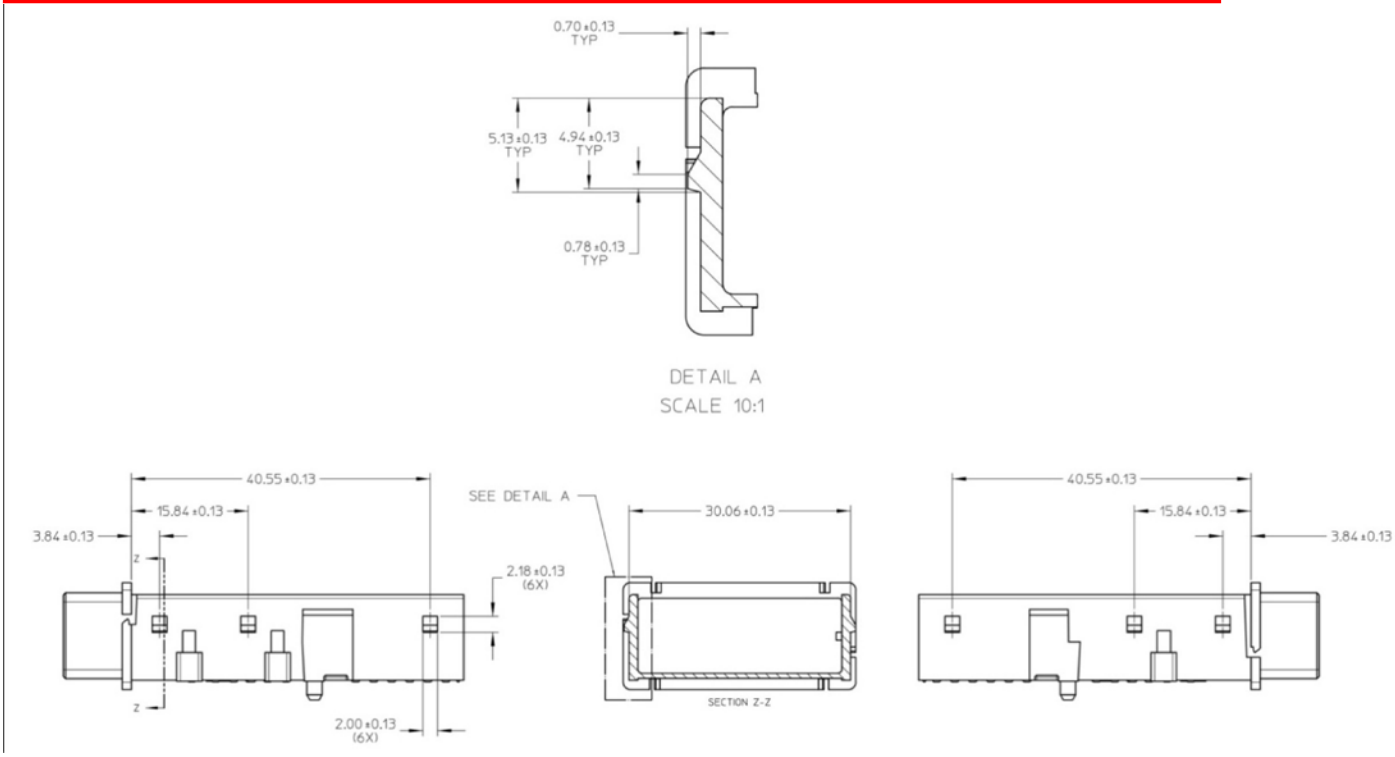


Figure 41: CDFP Style 1 Latch dimensions for heat sink clip

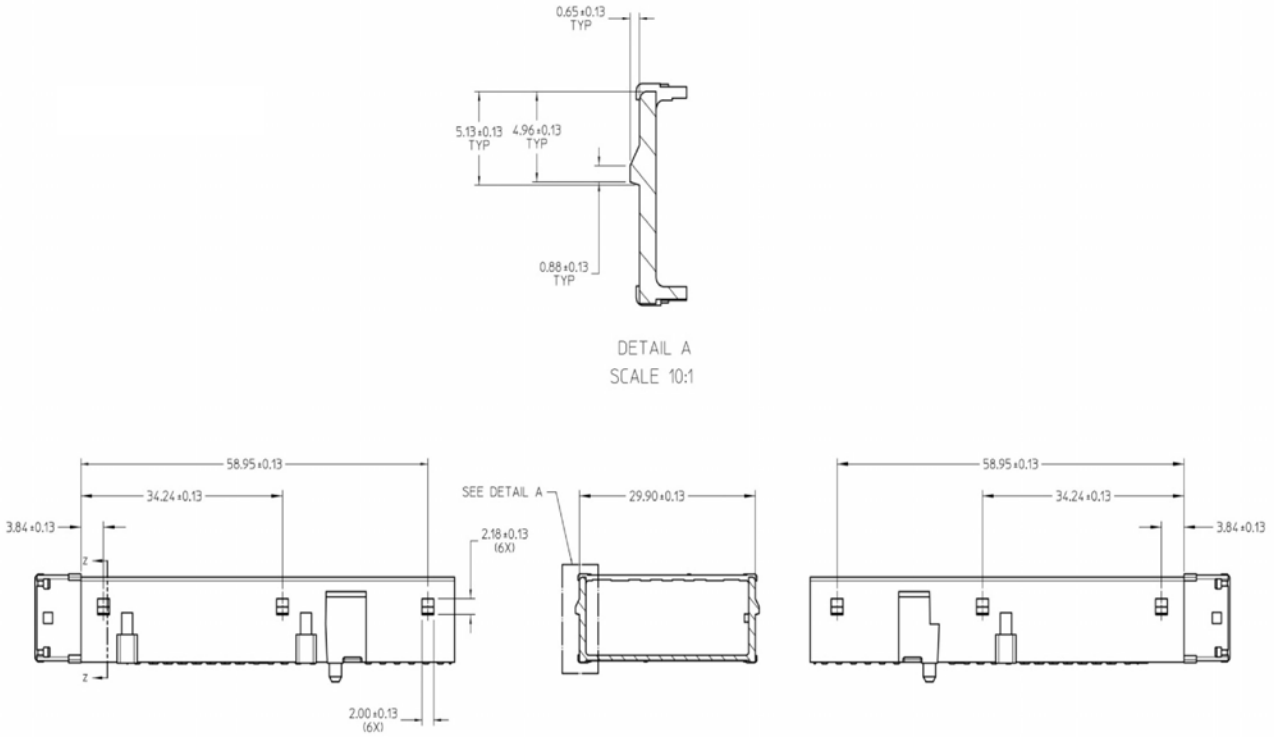


Figure 42: CDFP Style 2 and Style 3 Latch dimensions for heat sink clip

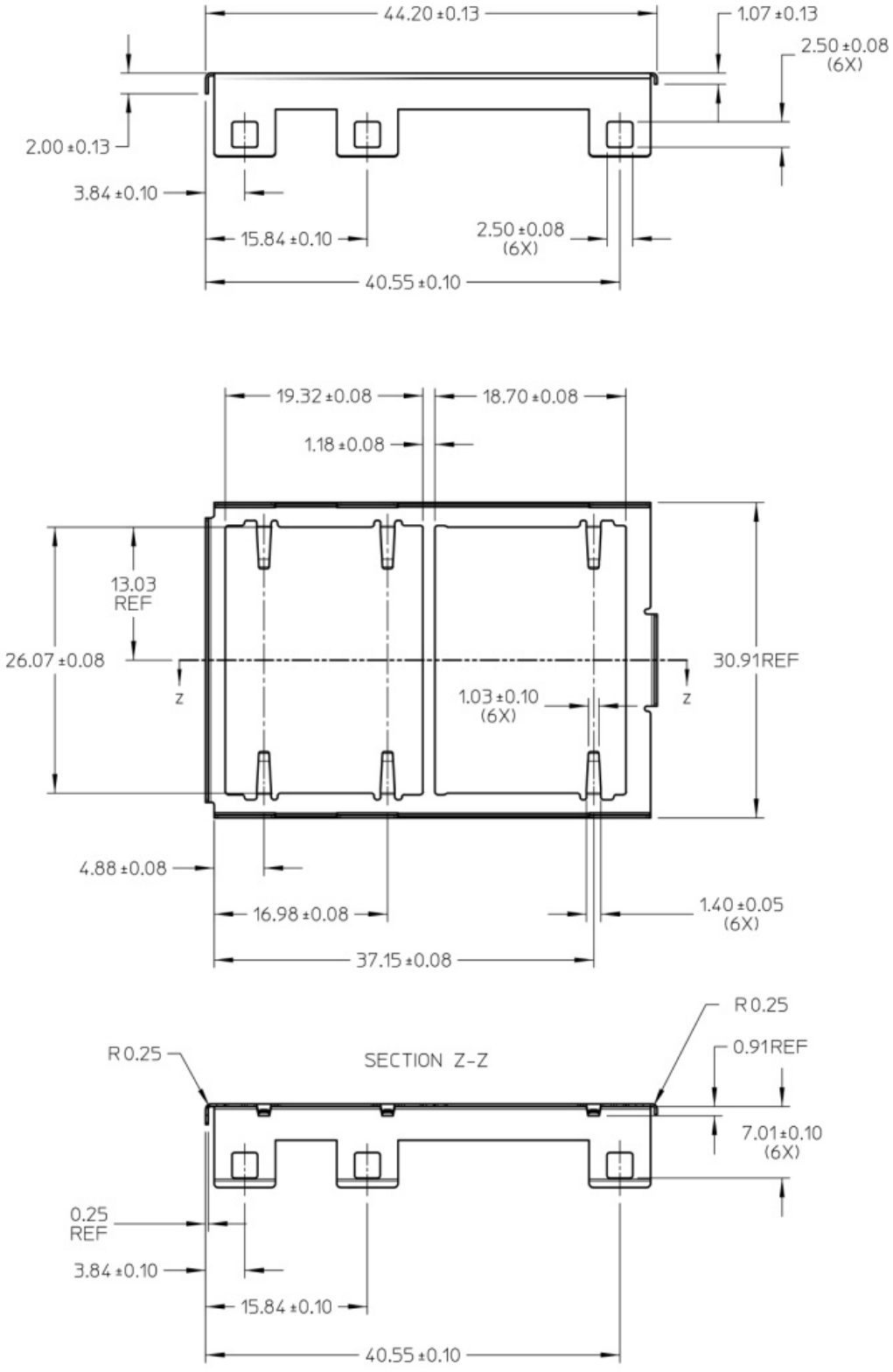


Figure 43: CDFP Style 1 heat sink clip

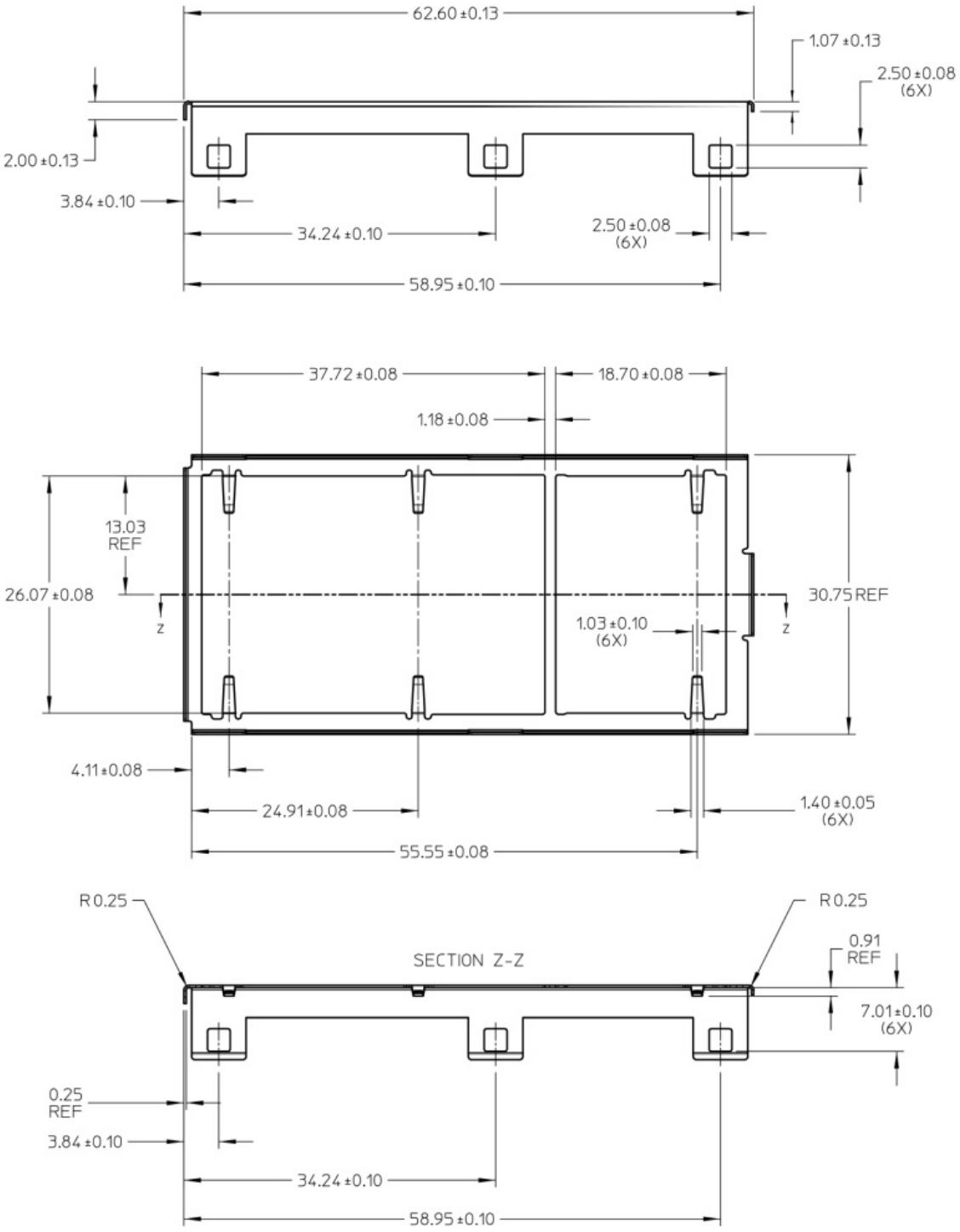


Figure 44: CDFP Style 2 and Style 3 heat sink clip

5.8.2 Light Pipes

The use of light pipes to indicate status of the module is application specific and not defined in this document.

5.9 Thermal interface

To provide optimal thermal management performance of the CDFP module/AOC, the portion of the module housing that is in contact with the heat sink should have mechanical properties that allow maximum thermal transfer. Figures 45thru 48 provide the mechanical flatness and roughness that is required on the CDFP modules and the specific regions of the module where these mechanical specifications apply. Note that the roughness specification applies to new modules since application of the module into the connector and heat sink can cause scratches, which although they are considered cosmetic to performance, could change the roughness measurement.

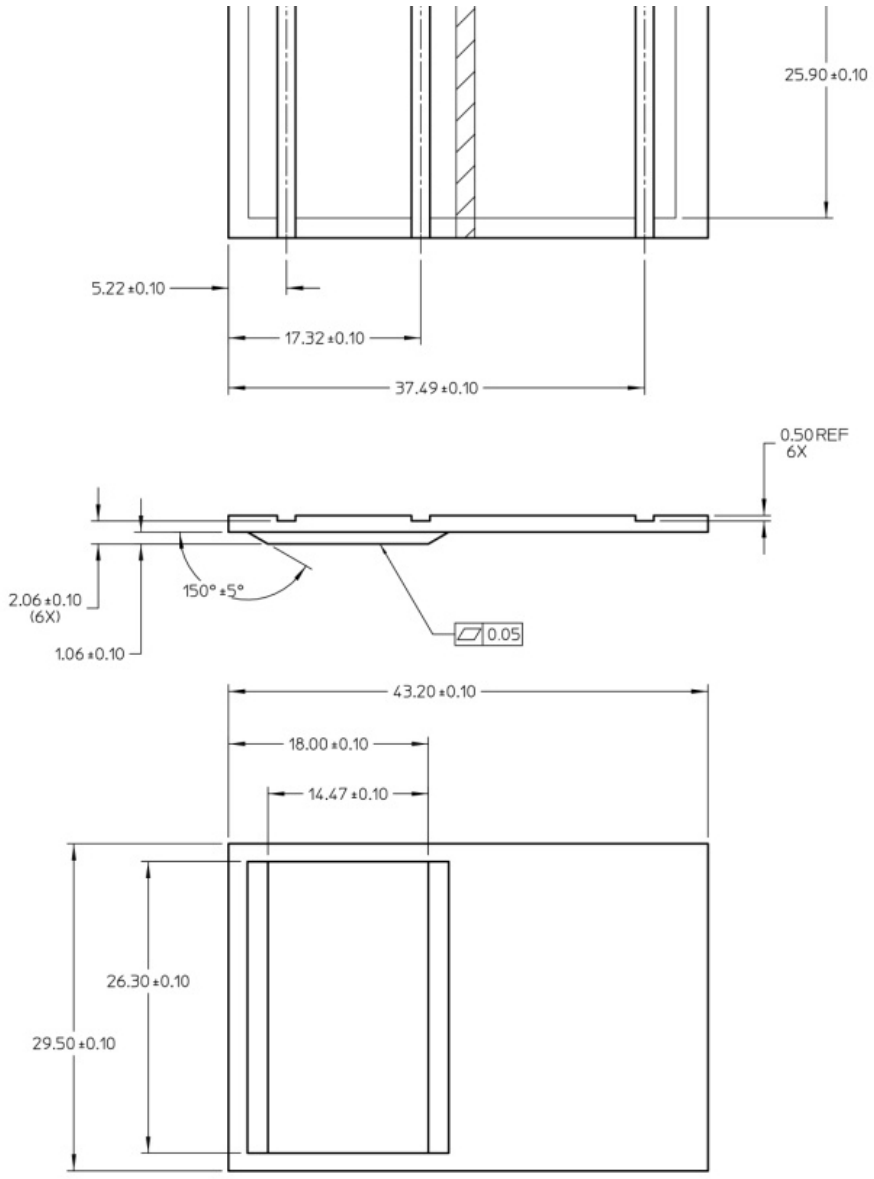


Figure 45: CDFP Style 1 heat sink thermal interface

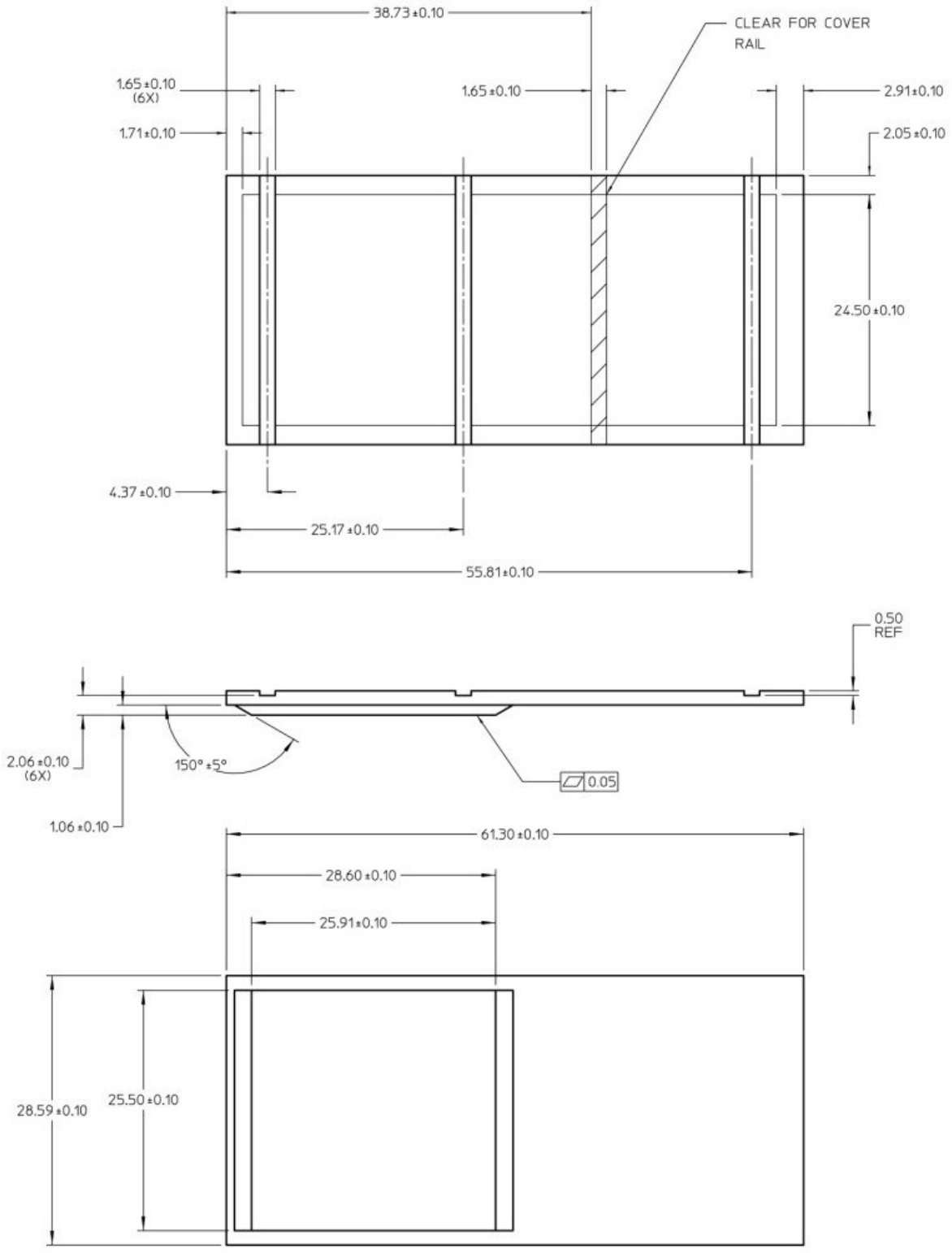


Figure 46: CDFP Style 2 and Style 3 heat sink thermal interface

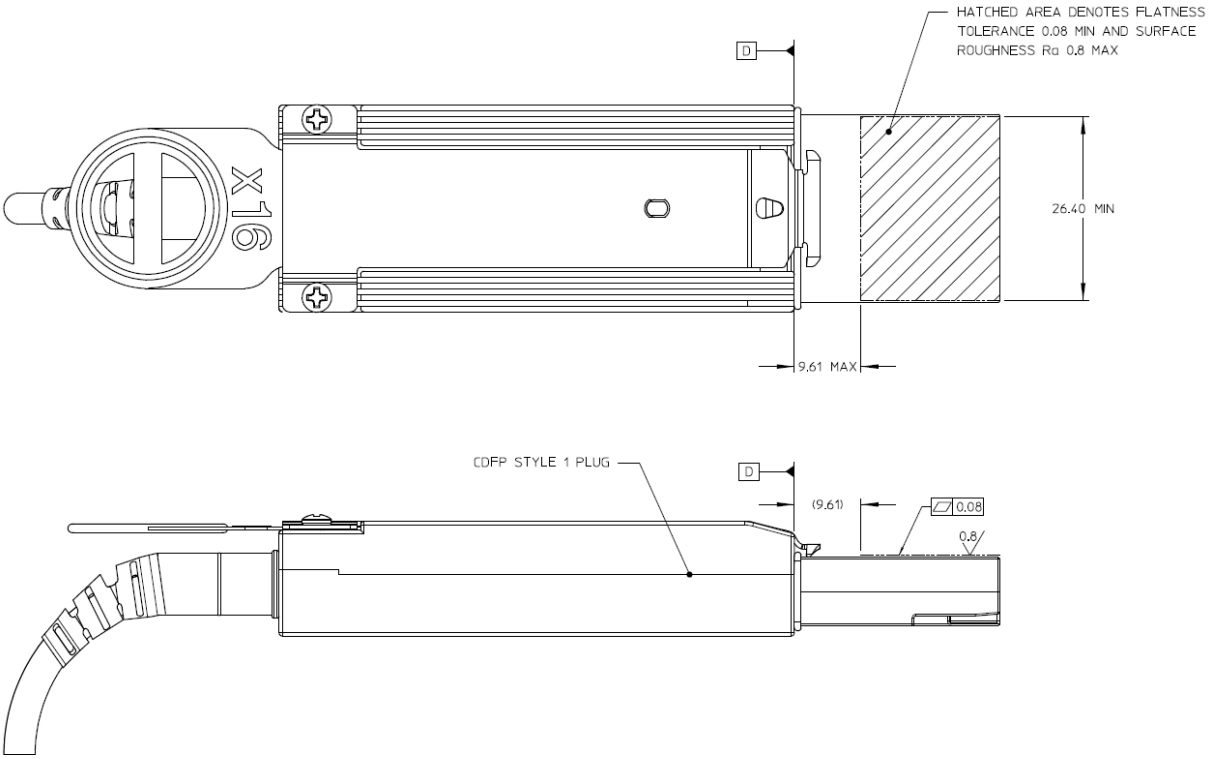


Figure 47: CDFP Style 1 surface flatness and roughness areas

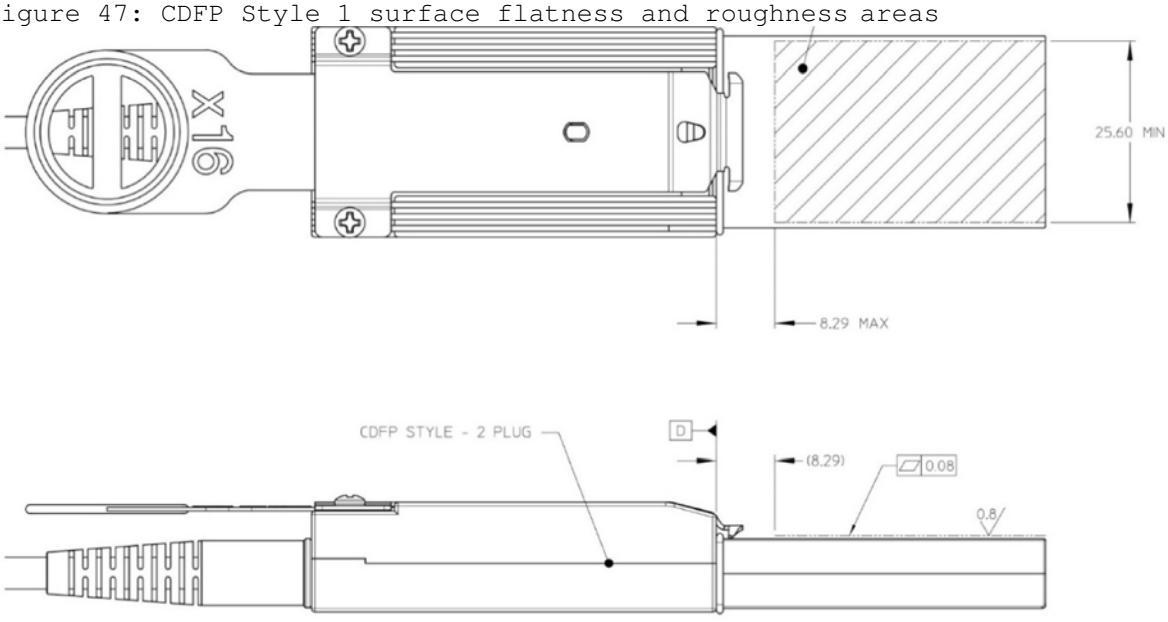


Figure 48: CDFP Style 2and Style 3 surface flatness and roughness areas

5.10 Dust / EMI Cover

In order to prevent contamination of the internal components and to optimize EMI performance, it is recommended that a Dust/EMI Cover be inserted into the cage assembly when no module is present. During installation, the front flange on the cover shall be seated against the front surface of the bezel to prevent dust from entering the equipment. The conductivity of the materials should be chosen for the Dust/EMI Cover to block EMI emissions.

5.11 Optical Interface

The CDFP optical interface port shall be either a male MPO16 connector as specified in IEC 61754-7 (see Figures 49, 50 and 51) or a dual LC as specified in IEC 61754-20. Other optical interfaces are left to the discretion of the module vendor.
For Style 1 and Style 2 the eight fiber positions on the upper right as shown in Figure 49, with the key up, are used for the optical transmit signals (Channel 0 through 7). The fiber positions on the lower right are used for the optical receive signals (Channel 0 through 7). The eight fiber positions on the lower left are used for the optical transmit signals (Channel 8 through 15). The fiber positions on the upper left are used for the optical receive signals (Channel 8 through 15). Note: Two alignment pins are present.
For Style 3 the sixteen fiber positions in the upper row as shown in Figure 50 with the key up are used for the optical transmit signals. (Channel 0 through 15). The fiber positions in the lower row as shown in Figure 50 are used for the optical receive signals (Channels 0-15). Note: Two alignment pins are present.

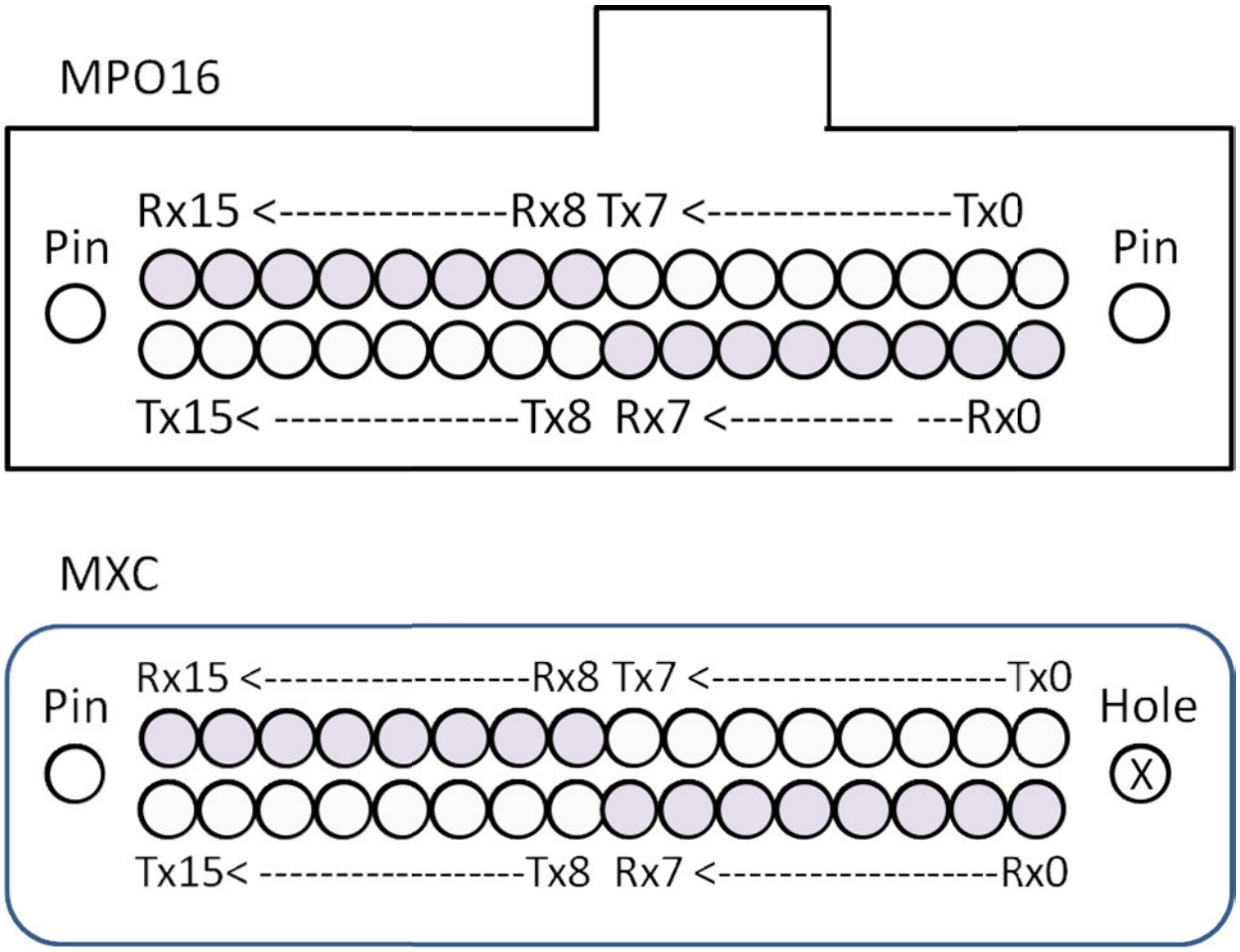


Figure 49: CDFP Style 1/Style 2 Optical Receptacle and Channel Orientation for MPO16 and MXC connector

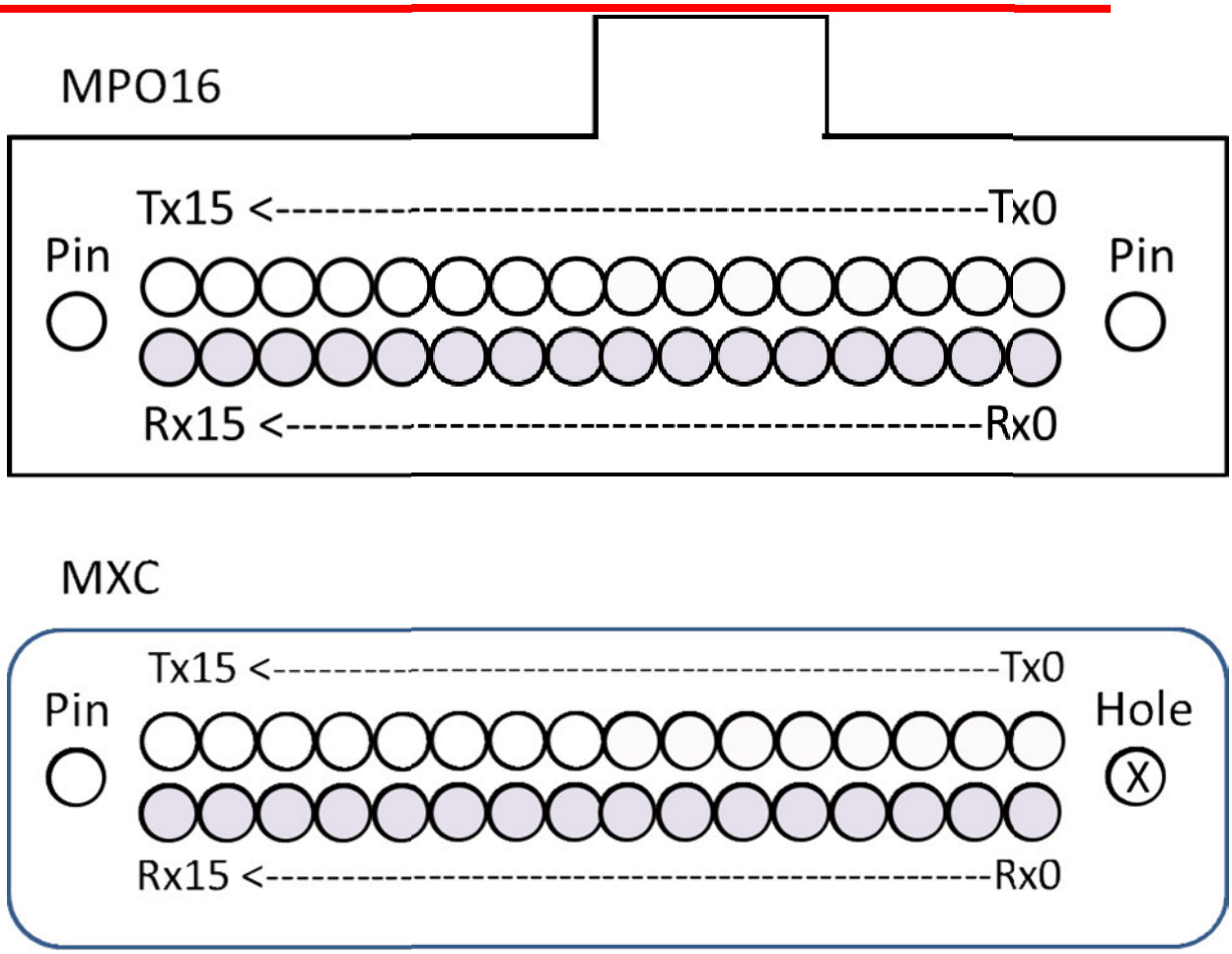


Figure 50: CDFP Style 3 Optical Receptacle and Channel Orientation for MPO16 and MXC connector

MPO16 Optical Cable connection

Aligned key (Type B) MPO16 patch cords should be used to ensure alignment of the signals between the modules. The aligned key patch cord is defined in TIA-568 and shown in Figure 51. The optical connector is orientated such that the keying feature of the MPO16 receptacle is on the top.

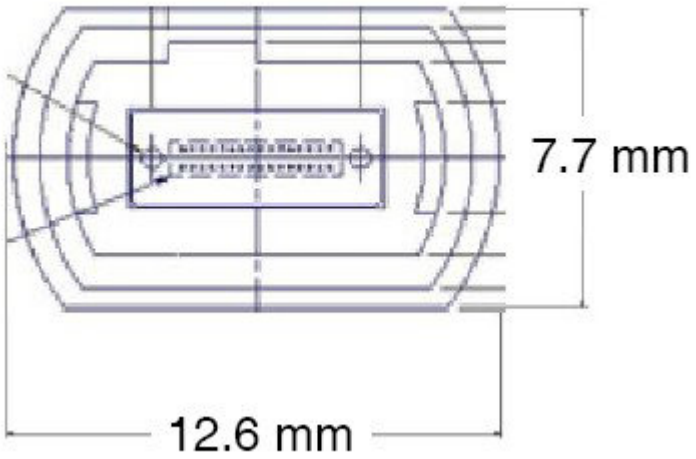


Figure 51: CDFP MPO16 Cable Plug

Dual LC Optical Cable connection

The Dual LC optical cable patch cord is defined in TIA/EIA-604-10A.

6 Environmental and Thermal

6.1 Thermal Requirements

The CDFP module shall operate within one or more of the case temperatures ranges defined in Table 8. The temperature ranges are applicable between 60m below sea level and 1800m above sea level, (Ref. NEBS GR-63) utilizing the host systems designed airflow.

Table 8: Temperature Range Class of operation

Class	**Case Temperature Range**
Standard	0 through 70C
Extended	-5 through 85C
Industrial	-40 through 85C

CDFP is designed to allow for up to 13 adjacent modules, in a standard 19 in. rack, with the appropriate thermal design for cooling/airflow. (Ref. NEBS GR-63)

7 CDFP Style 1/Style 2 Management Interface

7.1 Introduction

A management interface, as already commonly used in other form factors like GBIC, SFP, and XFP, is specified in order to enable flexible use of the module by the user. The specification has been changed in order to adopt the use of a multi-channel module. Some timing requirements are critical especially for a multi-channel device, so the interface speed has been increased. This CDFP specification is based on the SFF-8636 specification however it is not backward compatible. Address 128 Page00 is used to indicate the use of the CDFP memory map rather than the QSFP memory map.

7.2 Timing Specification

7.2.1 Introduction

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to a Vcc_host on the two-wire interface SCL (clock) and SDA (Data) signals. Detailed electrical specification is given in Sub clause 4.1.2. Nomenclature for all registers more than 1 bit long is MSB-LSB.

7.2.2 Management Interface Timing Specification

In order to support a multi-channel device a higher clock rate for the serial interface is considered. The timing requirements are shown in Figure 43 and specified in Table 8. CDFP is positioned to leverage two-wire timing (Fast Mode devices) to align the use of related cores on host ASICs. This sub clause closely follows the XFP MSA specification.

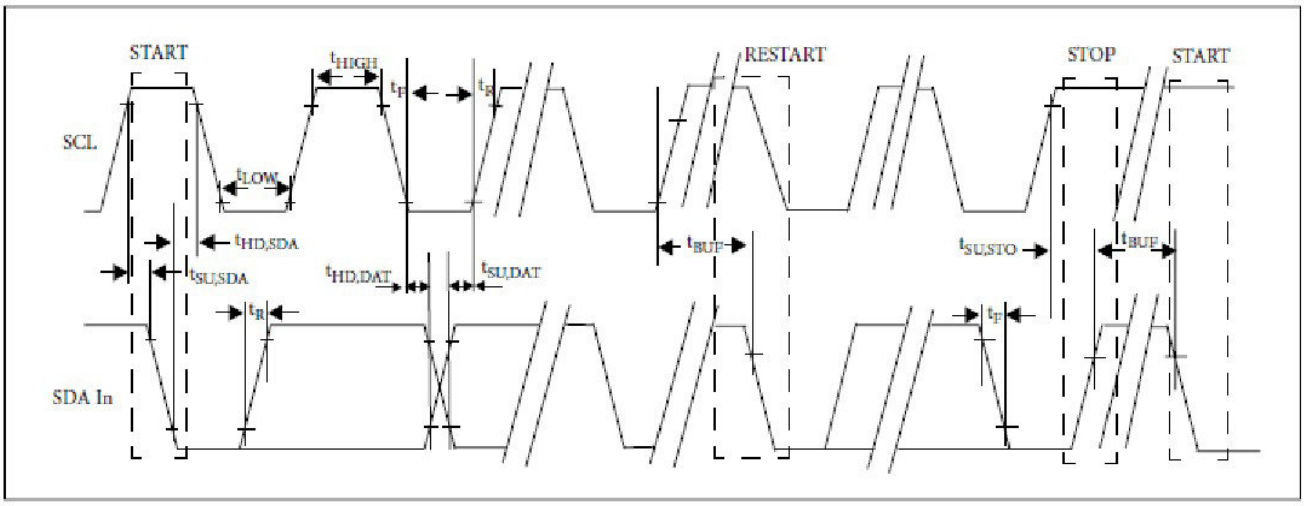


Figure 52: CDFP Timing Diagram

The two-wire serial interface address of the CDFPlower card is (B2h). The two-wire serial interface address of the CDFP upper card is (BAh).

7.2.3 Serial Interface Protocol

The module card asserts LOW for clock stretch on SCL.

7.2.3.1 Management Timing Parameters

The timing parameters for the two-wire interface to the CDFP module are shown in Table 8.

Table 9: Management Interface timing parameters

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	kHz	
Clock Pulse Width Low	tLOW	1.3		us	
Clock Pulse Width High	tHIGH	0.6		us	
Time bus free before new transmission can start	tBUF	20		us	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.SDA	0.6		us	
START Set-up Time	tSU.SDA	0.6		us	
Data In Hold Time	tHD.DAT	0		us	
Data in Set-up Time	tSU.DAT	0.1		us	
Input Rise Time (400kHz)	tR.400		300	ns	From (VIL,MAX-0.15) to (VIH, MIN +0.15)
Input Fall Time (400kHz)	tF.400		300	ns	From (VIH,MIN + 0.15) to (VIL,MAX – 0.15)
STOP Set-up Time	tSU.STO	0.6		us	

7.3 Memory Interaction Specifications

CDFP memory transaction timings are given in Table 9. Single byte writable memory blocks are given in Table 10. Multiple byte writable memory blocks are defined in Table 11.

Table 10: CDFP Memory Specification

Parameter	Symbol	Min	Max	Unit	Conditions
Serial Interface Clock Hold off "Clock Stretching"	T_clock_hold		500	us	Maximum time the CDFP Module card may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	tWR		40	ms	Complete (up to) 4 Byte Write
Endurance (Write Cycles)		50K		cycles	70 ^{0} C

Table 11: Single Byte Writable Memory Block

Address	Volatile or Nonvolatile	Description
86	Volatile	Control register
87	Volatile	Rx Rate select register
88	Volatile	Tx Rate select register
127	Volatile	Page Select Byte

Table 12: Multiple Byte Writable Memory Block

Address	# Bytes	Volatile/NonVolatile	Description
89-92	4	Volatile	Application select per channel
100-106	7	Volatile	Module Mask
119-122	4	Volatile	Password Change Entry Area (Optional)
123-126	4	Volatile	Password Entry Area (Optional)
128-255	128	Non-Volatile	User Writable memory - Page 02h
225-241	16	Volatile	Vendor Specific Channel Controls- Page 03h
242-253	12	Volatile	Channel Monitor Masks - Page 03h

7.3.1 Timing for Soft Control and Status Functions

Timing for CDFP soft control and status functions are described in Table 13.

Table 13: Timing for CDFP soft control and status functions

Parameter	Symbol	Max	Unit	Conditions
Initialization time	t_init	2000	ms	Time from power on[2] , hot plug or rising edge of reset until the module card is fully functional[3] This time does not apply to non-Power level 0 modules in Low Power State
Reset Init Assert Time	t_reset_init	2	us	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[2] until module card responds to data transmission over the two-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on[2] to DataNotReady, (bit 0 of Byte 2), deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the RstL pin until the module card is fully functional[3]
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL	500	us	Time from clear on read[4] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask	100	ms	Time from mask bit set (value=1b)[1] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared (value=0b)[1] until associated IntL operation resumes
Application or Rate Select Change Time	t_ratesel	100	ms	Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification
Power_override or Power_set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set (value = 1b)[1] until module card power consumption reaches Power Level 1
Power_override or Power_set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared (value = 0b)[1] until the module card is fully functional[3]
Note 1. Measured from falling clock edge after stop bit of write transaction				
Note 2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 4				
Note 3. Fully functional is defined as IntL asserted due to DataNotReady bit, bit 0 byte 2, deasserted. The module should also meet optical and electrical specifications.				
Note 4. Measured from falling clock edge after stop bit of read transaction				
Note 5. Does not apply to power level 1 modules				

Squelch and disable timings are defined in Table 14.

Table 14: I/O Timing for Squelch & Disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	80	us	Time from loss of Rx input signal until the squelched output condition is reached. See Subclause 4.1.3.1.
Rx Squelch Deassert Time	toff_Rxsq	80	us	Time from resumption of Rx input signals until normal Rx output condition is reached. See sub clause 4.1.3.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached. See sub clause 4.1.3.2.
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Tx output condition is reached. See sub clause 4.1.3.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled
Note 1: Measured from falling clock edge after stop bit of write transaction				

7.4 Device Addressing and Operation

Serial Clock (SCL): The host supplied SCL input to CDFP Modules is used to positive-edge clock data into each CDFP device and negative-edge clock data out of each device. The SCL line may be pulled low by a CDFP module during clock stretching.

Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven and may be wire-ORed with any number of open-drain or open collector devices.

Master/Slave: CDFP Modules operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Device Address: Each CDFP card is hard wired at the device address B2h for the lower card and BAh for upper card. See Clause 8 for memory structure within each Module for Style 1 and Style 2. See Clause 9 for memory structure with each Module for Style 3.

Multiple Devices per SCL/SDA: CDFP Module cards are compatible with point-to-point SCL/SDA, they cannot share a single SCL/SDA bus through the use of a ModSelL line.

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the CDFP in 8-bit words.Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host shall be acknowledged by CDFP Module card. Read data bytes transmitted by CDFP Module card shall be acknowledged by the host for all but the final byte read, for which the host shall respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the CDFP management interface can be reset. Memory reset is intended only to reset the CDFP Module management interface (to correct a hung bus). No other module functionality is implied.

1) Clock up to 9 cycles.
2) Look for SDA high in each cycle while SCL is high.
3) Create a START condition as SDA is high

Device Addressing: CDFP devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 53. This is common to all CDFP devices.

1	**0**	**1**	**1**	**x**	**0**	**1**	**R/W**
MSB							**LSB**

Figure 53: CDFP Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address the CDFP Module card shall output a zero (ACK) on the SDA line to acknowledge the address.

7.5 Read/Write Functionality

7.5.1 CDFP Memory Address Counter (Read AND Write Operations)

CDFP devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the module card. This address stays valid between operations as long as CDFP power is maintained. The address "roll over" during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

7.5.2 Read Operations

7.5.2.1 Current Address Read

A current address read operation requires only the device address read word (1011X011) be sent, see Figure 54.

		<-- CDFP ADDRESS --->																	
HOST	START	MSB						LSB	READ									NACK	STOP
		1	0	1	1	x	0	1	1	0	x	x	x	x	x	x	x	x	1	
CDFP										ACK	MSB							LSB		
											<---- DATA WORD ----->									

Figure 54: CDFP Current Address Read Operation

Once acknowledged by the CDFP, the current address data word is serially clocked out. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

7.5.2.2 Random Read

A random read operation requires a "dummy" write operation to load in the target byte address as shown in Figure 55. This is accomplished by the following sequence.

		<- CDFP ADDRESS ->									<- MEMORY ADDRESS ->								
HOST	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	1	x	0	1	0	0	x	x	x	x	x	x	x	x	0
CDFP										ACK									ACK
Begin Figure 55																			

	<- CDFP ADDRESS ->																	
START	MSB						LSB	READ									NACK	STOP
	1	0	1	1	x	0	1	1	0	x	x	x	x	x	x	x	x	1	
									ACK	MSB							LSB		
										<---- DATA WORD n---->									
Figure 55 End																			

Figure 55: CDFP Random Read

The target 8-bit data word address is sent following the device address write word (1011X010) and acknowledged by the CDFP. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (1011X011). The CDFP acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledge, but does generate a STOP condition once the data word is read.

7.5.2.3 Sequential Read

Sequential reads are initiated by either a current address read (Figure 56) or a random address read (Figure 57). To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the CDFP receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

		<- CDFP ADDRESS ->																
HOST	START	MSB						LSB	READ									ACK
		1	0	1	1	x	0	1	1	0	x	x	x	x	x	x	x	x	0
CDFP										ACK	MSB							LSB	
											<---- DATA WORD n---->								

Begin Figure 56

								ACK									NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
MSB							LSB		MSB							LSB		
<-- DATA WORD n+1 --->									<-- DATA WORD n+x --->									

Figure 56 End

Figure 56: Sequential Address Read Starting at CDFP Current Address

7.5.2.4 Sequential Read from Random Start Address

		<- CDFP ADDRESS ->									<- MEMORY ADDRESS ->								
HOST	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	1	x	0	1	0	0	x	x	x	x	x	x	x	x	0
CDFP										ACK									ACK
Begin Figure 57																			

	<- CDFP ADDRESS ->																	
START	MSB						LSB	READ										ACK
	1	0	1	1	x	0	1	1	0	x	x	x	x	x	x	x	x	1
									ACK	MSB							LSB	
										<---- DATA WORD n---->								
Figure 57 Middle																		

								ACK									NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
MSB							LSB		MSB							LSB		
<-- DATA WORD n+1 --->									<-- DATA WORD n+x --->									
Figure 57 End																		

Figure 57: Sequential Address Read Starting with Random CDFP Read

7.5.3 Write Operations

7.5.3.1 BYTE Write

A write operation requires an 8-bit data word address following the device address write word (1011X010) and acknowledgement, see Figure 58.

		<- CDFP ADDRESS ->									<- MEMORY ADDRESS ->									<- DATA WORD ->									
HOST	**START**	**MSB**						**LSB**	**WRITE**		**MSB**							**LSB**												**STOP**
		1	**0**	**1**	**1**	**x**	**0**	**1**	**0**	**0**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**0**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**0**	
CDFP										**ACK**									**ACK**	**MSB**							**LSB**	**ACK**	

Figure 58: CDFP Write Byte Operation

Upon receipt of this address, the CDFP shall again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the CDFP shall output a zero (ACK) and the host master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the two-wire interface specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the CDFP enters an internally timed write cycle, tWR, to internal memory. The CDFP disables its management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the write is complete. Note that two-wire interface "Combined Format" using repeated START conditions is not supported on CDFP write commands.

7.5.3.2 Sequential Write

CDFP's shall support up to a 4 sequential byte write without repeatedly sending CDFP address and memory address information as shown in Figure 59.

		<- CDFP ADDRESS ->									<- MEMORY ADDRESS ->								
HOST	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	1	x	0	1	0	0	x	x	x	x	x	x	x	x	0
CDFP										ACK									ACK

Begin Figure 59

<--- DATA WORD 1 --->									<--- DATA WORD 2 ---->								
MSB							LSB		MSB							LSB	
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0
								ACK									ACK

Figure 59 Middle

<--- DATA WORD 3 --->									<--- DATA WORD 4 ---->									
MSB							LSB		MSB							LSB		STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
								ACK									ACK	

Figure 59 End

Figure 59: CDFP Sequential Write Operation

A "sequential" write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the CDFP acknowledges receipt of the first data word, the host can transmit up to three more data words. The CDFP shall send an acknowledge after each data word received. The host must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that two-wire interface "combined format" using repeated START conditions is not supported on CDFP write commands.

7.5.3.3 Acknowledge Polling

Once the CDFP internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the CDFP respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

8 CDFP MSA Management Interface Memory Map-Styles 1 and 2

8.1 Overview

Each end of the CDFP features two module cards, each of which contains a microcontroller, an 8-channel transmitter and an 8-channel receiver. These transmitters and receivers may contain retimers as shown in the example below. The connectivity between these components on each module card is illustrated as follows:

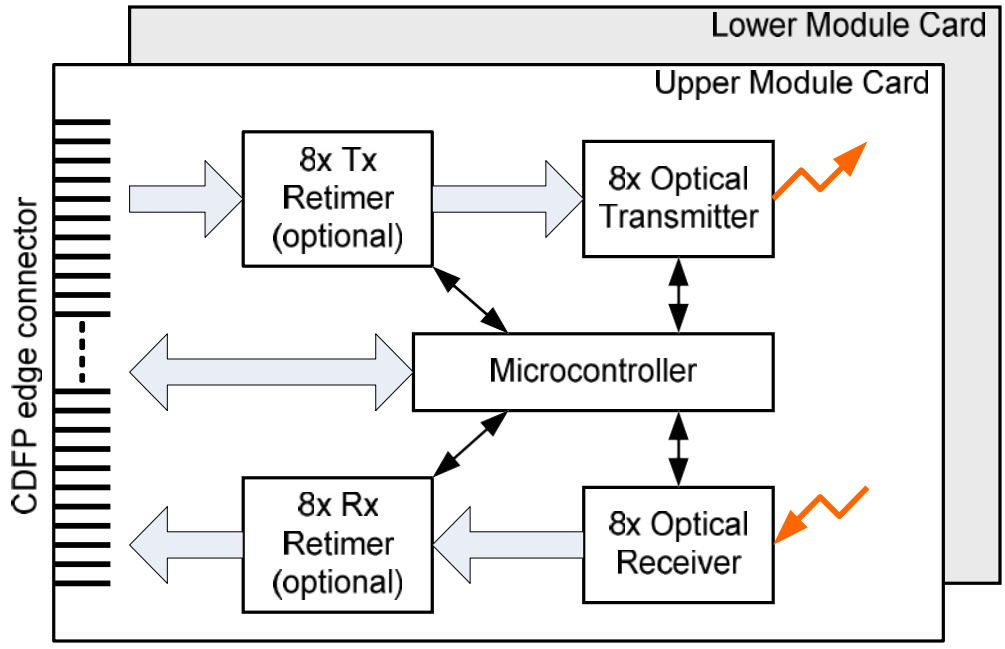


Figure 60: Example CDFP Style 1/Style 2 optical transceiver implementation

The microcontroller manages the operation of both the optical transceivers and the retimers and presents a standard management interface to the host computer system. The management interface provided is the industry standard QSFP specification extended to eight channels. Each circuit board reports its own measurements of temperature, voltage, etc. Similarly, "global" control mechanisms are local to the circuit board being addressed.

The upper module card handles CDFP Tx channels 0 through 7 and Rx channels 8 through 15; the lower module card handles CDFP Tx channels 8 through 15 and Rx channels 0 through 7. The terms Tx and Rx represent the host's viewpoint – the host transmits data through the Tx channels and receives data through the Rx channels.

8.2 Management Interface

At power-on or module insertion into the CDFP connector, the host computer system detects the presence of the module by the change of state of the ModPrsL (Module Present, active Low) signal from the module card. The module card will then initialize itself and signal that it is ready to communicate with the host computer system by asserting a low level on the IntL signal. The host computer system should then interrogate the module card via the two-wire serial interface to determine the module card status.

The two-wire serial interface (SCL and SDA) deviates from the QSFP specification in that the two wire serial address for the lower circuit board is B2h/B3h (1011001x) (for 7 bit addressing it would be 0x59) and the two wire serial address for the upper circuit board is BAh/BBh (1011101x) (for 7 bit addressing it would be 0x5D). The 2 two wire serial interfaces (one on each circuit board) operate independently from each other. Note: The CDFP modules have no Modsel signal input and module selection must be made via alternate means not defined in this document.

Like the QSFP specification, the CDFP provides a memory map with a lower page (addresses 00h to 7Fh) and multiple upper pages (addresses 80h to FFh). The lower page is always accessible and contains critical monitoring information and control fields. The last byte of the lower page, address 7Fh, can be written with a value indicating which upper page is to be accessed using the upper page addresses. The CDFP module card has 3 upper pages.

All pages in the memory map are readable at all times. Some areas in the QSFP-like pages are writable by the host system; these are listed below. To prevent inadvertent changes to other areas in the memory map, some areas are protected by passwords; write access to these areas is enabled by writing the appropriate password into the password field at the top of the lower page (addresses 7Bh to 7Eh).

The structure of the lower page of the memory map is illustrated in the diagram below:

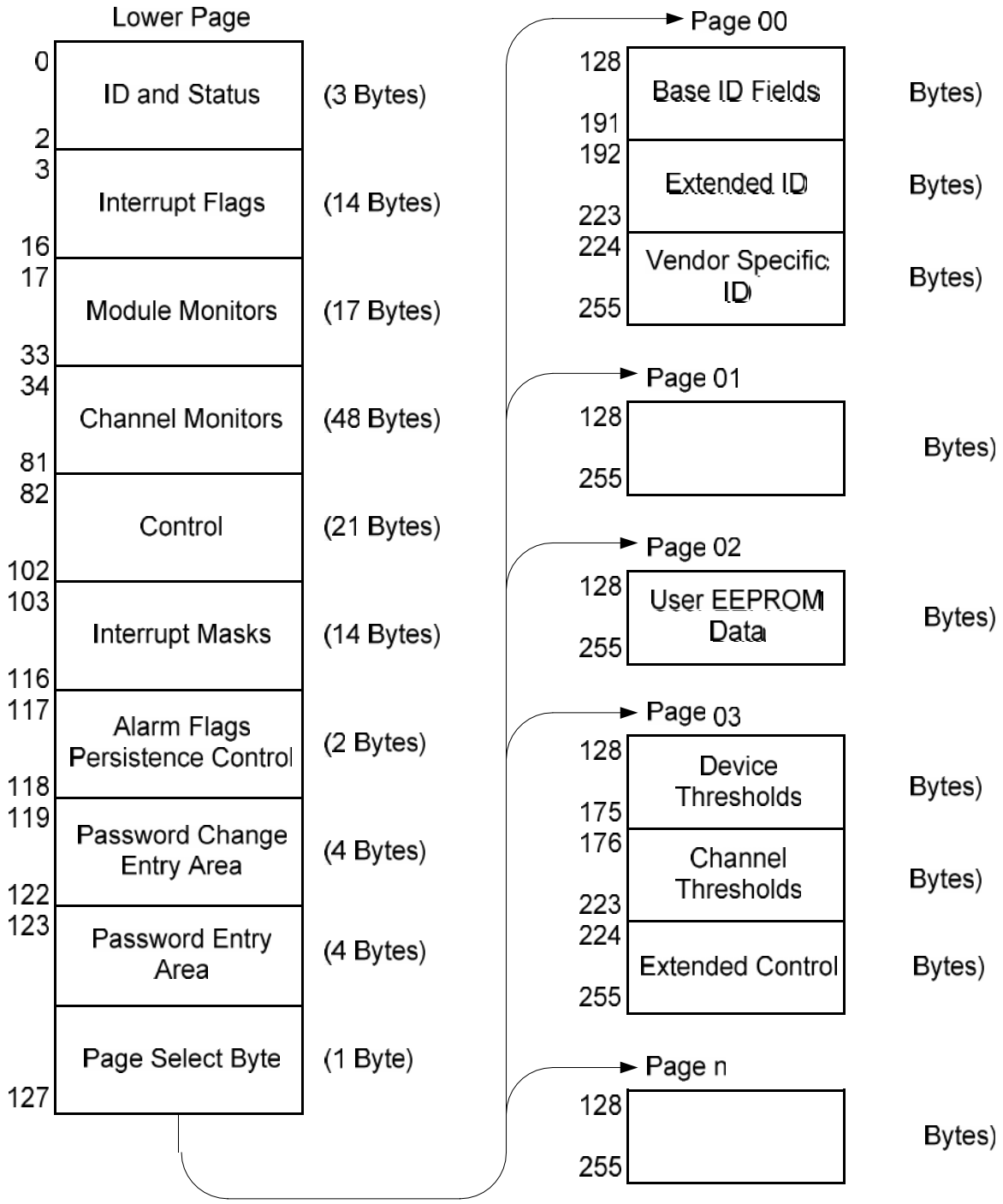


Figure 61: CDFP Style 1/Style 2 Memory Map

8.3 Lower Page 00L

The lower 128 bytes of the two-wire serial bus address space is used to access a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent accesses. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed.

The lower page is subdivided into several areas as illustrated in the following table:

Table 15: Lower Page Overview (Page 0L)

Address	Description	Type
0 – 2	Id and Status (3 bytes)	Read-only
3 – 16	Interrupt Flags (14 bytes)	Read-only
17 – 33	Module card Monitors (17 bytes)	Read-only
34 – 81	Channel Monitors (48 bytes)	Read-only
82 – 102	Control Fields (21 bytes)	Read/Write
103 – 116	Interrupt Flag Masks (14 bytes)	Read/Write
117 – 118	Interrupt Flag Persistence Control (2 bytes)	Read/Write
119 – 122	Password Change Area (4 bytes)	Read/Write
123 – 126	Password Entry Area (4 bytes)	Read/Write
127	Page Select Byte	Read/Write

8.3.1 ID and Status

Table 16: Identifier and Status Summary (Page 0L)

Byte	Bits	Name	Description	Type
0 00h	All	Identifier	Identifier – Type of Serial Module (same value as page 0 byte 128)	RO Rqrd.
1 01h	All	Version Id	Identifier – Version of Serial Module Specification (coded 1, this document)	RO Rqrd.
2 02h	7	Flat_mem	Upper memory flat or paged. 0= paged, 1=Page 00h only	RO Rqrd.
	6	Tx Bias and Tx Power Alarm Summary	Set to 1 whenever any Tx Bias Alarm bit (bytes 11 and 12) or any Tx Power Alarm bit (bytes 13 and 14) is set to 1 and not masked.	
	5	Rx Power Alarm/Warning Summary	Set to 1 whenever any Rx Power Alarm or Warning bit (bytes 8, 9 and 10) is set to 1 and not masked.	
	4	Tx LOS, Tx Fault and Tx LOL Alarm Summary	Set to 1 whenever any Tx LOS Alarm bit (byte 4), Tx Fault Alarm bit (byte 5) or Tx CDR LOL Alarm bit (byte 16) is set to 1 and not masked.	
	3	Rx LOS and Rx LOL Alarm Summary	Set to 1 whenever any Rx LOS Alarm bit (byte 3) or Rx CDR LOL Alarm bit (byte 15) is set to 1 and not masked.	
	2	Temperature and Voltage Alarm/Warning Summary	Set to 1 whenever any Temperature Alarm or Warning bit (byte 6) or Voltage Alarm bit (byte 7) is set to 1 and not masked	
	1	Interrupt	Set to 1 whenever the IntL pin is asserted low	
	0	DataNotReady	Indicates Module card has not yet achieved power up and memory data is not ready. Bit remains high until data is ready to be read at which time the device sets the bit low.	

The identifier value (byte 0) specifies the type of the physical device described by the serial information. The identifier value is the same value as page 0 byte 128.

The DataNotReady bit is high during module power up and prior to a valid suite of monitor readings. Once all monitor readings are valid, the bit is set low until the device is powered down or reset.

All summary bits 2-6 are nonlatched, reflecting real-time values in the specific registers. This is to avoid multiple levels of latching and clearing of faults.

8.3.2 Interrupt Flags

A portion of the memory map (bytes 3 through 16), form a flags field. Within this field, the status of LOS and Tx Fault as well as alarms and warnings for the various monitored items is reported. If a monitor is implemented the associated flags must also be implemented. For normal operation and default state, the bits in this field have the value of 0b. For the defined conditions of LOS, Tx Fault, module and channel alarms and warnings, the appropriate bit or bits are set, value = 1b. Once asserted, the bits remained set (latched) until cleared by a read operation that includes the affected bit or reset by the ResetL pin. After being read and cleared, the bit may be set again if the condition persists and the appropriate persistence control bit is set (see below). The Interrupt Flags are defined in the following table:

Table 17: Alarm Flags (Page 0L)

Byte	Bit	Name	Description	Type
3 03h	7	L-Rx15 LOS	Latched Rx LOS indicator, channel 7	RO Opt.
	6	L-Rx14 LOS	Latched Rx LOS indicator, channel 6	
	5	L-Rx13 LOS	Latched Rx LOS indicator, channel 5	
	4	L-Rx12 LOS	Latched Rx LOS indicator, channel 4	
	3	L-Rx11 LOS	Latched Rx LOS indicator, channel 3	
	2	L-Rx10 LOS	Latched Rx LOS indicator, channel 2	
	1	L-Rx9 LOS	Latched Rx LOS indicator, channel 1	
	0	L-Rx8 LOS	Latched Rx LOS indicator, channel 0	
4 04h	7	L-Tx7 LOS	Latched Tx LOS indicator, channel 7	RO Opt.
	6	L-Tx6 LOS	Latched Tx LOS indicator, channel 6	
	5	L-Tx5 LOS	Latched Tx LOS indicator, channel 5	
	4	L-Tx4 LOS	Latched Tx LOS indicator, channel 4	
	3	L-Tx3 LOS	Latched Tx LOS indicator, channel 3	
	2	L-Tx2 LOS	Latched Tx LOS indicator, channel 2	
	1	L-Tx1 LOS	Latched Tx LOS indicator, channel 1	
	0	L-Tx0 LOS	Latched Tx LOS indicator, channel 0	
5 05h	7	L-Tx7 Fault	Latched Tx fault indicator, channel 7	RO Opt.
	6	L-Tx6 Fault	Latched Tx fault indicator, channel 6	
	5	L-Tx5 Fault	Latched Tx fault indicator, channel 5	
	4	L-Tx4 Fault	Latched Tx fault indicator, channel 4	
	3	L-Tx3 Fault	Latched Tx fault indicator, channel 3	
	2	L-Tx2 Fault	Latched Tx fault indicator, channel 2	
	1	L-Tx1 Fault	Latched Tx fault indicator, channel 1	
	0	L-Tx0 Fault	Latched Tx fault indicator, channel 0	
6 06h	7	L-Temp High Alarm	Latched high temperature alarm	RO Opt.
	6	L-Temp Low Alarm	Latched low temperature alarm	
	5	L-Temp High Warning	Latched high temperature warning	
	4	L-Temp Low Warning	Latched low temperature warning	
	3	L-Temp2 High Alarm	Latched high second temperature alarm	
	2	L-Temp2 Low Alarm	Latched low second temperature alarm	

	1	L-Temp2 High Warning	Latched high second temperature warning	
	0	L-Temp2 Low Warning	Latched low second temperature warning	
7 07h	7	L-Vcc3.3v High Alarm	Latched high 3.3 volts supply voltage alarm	RO Opt.
	6	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm	
	0-5	Reserved		
8 08h	7	L-Rx15 Power Low Warning	Latched low Rx power warning, channel 7	RO Opt.
	6	L-Rx14 Power Low Warning	Latched low Rx power warning, channel 6	
	5	L-Rx13 Power Low Warning	Latched low Rx power warning, channel 5	
	4	L-Rx12 Power Low Warning	Latched low Rx power warning, channel 4	
	3	L-Rx11 Power Low Warning	Latched low Rx power warning, channel 3	
	2	L-Rx10 Power Low Warning	Latched low Rx power warning, channel 2	
	1	L-Rx9 Power Low Warning	Latched low Rx power warning, channel 1	
	0	L-Rx8 Power Low Warning	Latched low Rx power warning, channel 0	
9 09h	7	L-Rx15 Power Low Alarm	Latched low Rx power alarm, channel 7	RO Opt.
	6	L-Rx14 Power Low Alarm	Latched low Rx power alarm, channel 6	
	5	L-Rx13 Power Low Alarm	Latched low Rx power alarm, channel 5	
	4	L-Rx12 Power Low Alarm	Latched low Rx power alarm, channel 4	
	3	L-Rx11 Power Low Alarm	Latched low Rx power alarm, channel 3	
	2	L-Rx10 Power Low Alarm	Latched low Rx power alarm, channel 2	
	1	L-Rx9 Power Low Alarm	Latched low Rx power alarm, channel 1	
	0	L-Rx8 Power Low Alarm	Latched low Rx power alarm, channel 0	
10 0Ah	7	L-Rx15 Power High Alarm	Latched high Rx power alarm, channel 7	RO Opt.
	6	L-Rx14 Power High Alarm	Latched high Rx power alarm, channel 6	
	5	L-Rx13 Power High Alarm	Latched high Rx power alarm, channel 5	
	4	L-Rx12 Power High Alarm	Latched high Rx power alarm, channel 4	
	3	L-Rx11 Power High Alarm	Latched high Rx power alarm, channel 3	
	2	L-Rx10 Power High Alarm	Latched high Rx power alarm, channel 2	
	1	L-Rx9 Power High Alarm	Latched high Rx power alarm, channel 1	
	0	L-Rx8 Power High Alarm	Latched high Rx power alarm, channel 0	
11 0Bh	7	L-Tx7 Bias Low Alarm	Latched low Tx bias alarm, channel 7	RO Opt.
	6	L-Tx6 Bias Low Alarm	Latched low Tx bias alarm, channel 6	
	5	L-Tx5 Bias Low Alarm	Latched low Tx bias alarm, channel 5	
	4	L-Tx4 Bias Low Alarm	Latched low Tx bias alarm, channel 4	
	3	L-Tx3 Bias Low Alarm	Latched low Tx bias alarm, channel 3	
	2	L-Tx2 Bias Low Alarm	Latched low Tx bias alarm, channel 2	
	1	L-Tx1 Bias Low Alarm	Latched low Tx bias alarm, channel 1	
	0	L-Tx0 Bias Low Alarm	Latched low Tx bias alarm, channel 0	
12 0Ch	7	L-Tx7 Bias High Alarm	Latched high Tx bias alarm, channel 7	RO Opt.
	6	L-Tx6 Bias High Alarm	Latched high Tx bias alarm, channel 6	
	5	L-Tx5 Bias High Alarm	Latched high Tx bias alarm, channel 5	
	4	L-Tx4 Bias High Alarm	Latched high Tx bias alarm, channel 4	
	3	L-Tx3 Bias High Alarm	Latched high Tx bias alarm, channel 3	
	2	L-Tx2 Bias High Alarm	Latched high Tx bias alarm, channel 2	
	1	L-Tx1 Bias High Alarm	Latched high Tx bias alarm, channel 1	
	0	L-Tx0 Bias High Alarm	Latched high Tx bias alarm, channel 0	
13 0Dh	7	L-Tx7 Power LowAlarm	Latched low Tx power alarm, channel 7	RO Opt.
	6	L-Tx6 Power LowAlarm	Latched low Tx power alarm, channel 6	
	5	L-Tx5 Power LowAlarm	Latched low Tx power alarm, channel 5	
	4	L-Tx4 Power LowAlarm	Latched low Tx power alarm, channel 4	
	3	L-Tx3 Power LowAlarm	Latched low Tx power alarm, channel 3	
	2	L-Tx2 Power LowAlarm	Latched low Tx power alarm, channel 2	
	1	L-Tx1 Power LowAlarm	Latched low Tx power alarm, channel 1	
	0	L-Tx0 Power LowAlarm	Latched low Tx power alarm, channel 0	
14 0Eh	7	L-Tx7 Power HighAlarm	Latched high Tx power alarm, channel 7	RO Opt.
	6	L-Tx6 Power HighAlarm	Latched high Tx power alarm, channel 6	
	5	L-Tx5 Power HighAlarm	Latched high Tx power alarm, channel 5	

	4	L-Tx4 Power HighAlarm	Latched high Tx power alarm, channel 4	
	3	L-Tx3 Power HighAlarm	Latched high Tx power alarm, channel 3	
	2	L-Tx2 Power HighAlarm	Latched high Tx power alarm, channel 2	
	1	L-Tx1 Power HighAlarm	Latched high Tx power alarm, channel 1	
	0	L-Tx0 Power HighAlarm	Latched high Tx power alarm, channel 0	
15 0Fh	7	L_Rx15 CDR _LOL	Latched Rx CDR LOL indicator, channel 7	RO Opt.
	6	L_Rx14 CDR _LOL	Latched Rx CDR LOL indicator, channel 6	
	5	L_Rx13 CDR _LOL	Latched Rx CDR LOL indicator, channel 5	
	4	L_Rx12 CDR _LOL	Latched Rx CDR LOL indicator, channel 4	
	3	L_Rx11 CDR _LOL	Latched Rx CDR LOL indicator, channel 3	
	2	L_Rx10 CDR _LOL	Latched Rx CDR LOL indicator, channel 2	
	1	L_Rx9 CDR _LOL	Latched Rx CDR LOL indicator, channel 1	
	0	L_Rx8 CDR _LOL	Latched Rx CDR LOL indicator, channel 0	
16 10h	7	L_Tx7 CDR _LOL	Latched Tx CDR LOL indicator, channel 7	RO Opt.
	6	L_Tx6 CDR _LOL	Latched Tx CDR LOL indicator, channel 6	
	5	L_Tx5 CDR _LOL	Latched Tx CDR LOL indicator, channel 5	
	4	L_Tx4 CDR _LOL	Latched Tx CDR LOL indicator, channel 4	
	3	L_Tx3 CDR _LOL	Latched Tx CDR LOL indicator, channel 3	
	2	L_Tx2 CDR _LOL	Latched Tx CDR LOL indicator, channel 2	
	1	L_Tx1 CDR _LOL	Latched Tx CDR LOL indicator, channel 1	
	0	L_Tx0 CDR _LOL	Latched Tx CDR LOL indicator, channel 0	

8.3.3 Module Card Monitors

Optional real time monitoring for the module includes Module Card temperature, supply voltage, supply current and monitoring for each transmit and receive channel. Channel monitoring functions are described in section 3.4 below. Measured parameters are reported in 16-bit data fields, i.e. two concatenated bytes, most-significant byte (MSB) first. To guarantee coherency of the diagnostic monitoring data, the host should retrieve any multi-byte fields from the diagnostic monitoring data structure by the use of a single multi-byte read sequence across the two-wire serial interface.

Internally measured device temperatures are represented as a 16-bit signed twos complement value in increments of 1/256 degrees Celsius, yielding a total range of -128 C to +128 C that is considered valid in the range specified in the device datasheet. Temperature accuracy is vendor specific but must be better than ±3 degrees Celsius over the specified operating temperature and voltage.

Internally measured Module 3.3 volts supply voltage is represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0 - 65535) with LSB equal to 100 uVolt, yielding a total measurement range of 0 to +6.55 Volts. Accuracy is vendor specific but must be better than ±3% of the manufacturer's nominal value over specified operating temperature and voltage.

Internally measured supply current is represented as a 16-bit unsigned integer with the current defined as the full 16-bit value (0 - 65535) with LSB equal to 1 mA, yielding a total measurement range of 0 to 65.5 A. Accuracy is vendor specific but must be better than ±10% of the maximum current of the vendor's specified power class over operating temperature and voltage.

Elapsed operating time is represented as a 16-bit unsigned integer with the time since power-on or reset defined as the full 16-bit value (0 - 65535) with LSB equal to 2 hours, yielding a total measurement range of 0 to +14.96 years.

The Raw LOS, Fault and CDR LOL indicators show the real-time unlatched state of the respective channel monitors. Whereas the latched alarm flags (bytes 3 through 16) show

the onset of a particular condition, the negation of the corresponding raw flag shows the cessation of the condition, implying that the channel may now be used for data transfer.

Table 18: Module Monitors (Page 0L)

Byte	Bit	Name	Description	Type
17 11h	7	Raw -Rx15 LOS	Unlatched Rx LOS indicator, channel 7	RO Opt.
	6	Raw -Rx14 LOS	Unlatched Rx LOS indicator, channel 6	
	5	Raw -Rx13 LOS	Unlatched Rx LOS indicator, channel 5	
	4	Raw -Rx12 LOS	Unlatched Rx LOS indicator, channel 4	
	3	Raw -Rx11 LOS	Unlatched Rx LOS indicator, channel 3	
	2	Raw -Rx10 LOS	Unlatched Rx LOS indicator, channel 2	
	1	Raw -Rx9 LOS	Unlatched Rx LOS indicator, channel 1	
	0	Raw -Rx8 LOS	Unlatched Rx LOS indicator, channel 0	
18 12h	7	Raw -Tx7 LOS	Unlatched Tx LOS indicator, channel 7	RO Opt.
	6	Raw -Tx6 LOS	Unlatched Tx LOS indicator, channel 6	
	5	Raw -Tx5 LOS	Unlatched Tx LOS indicator, channel 5	
	4	Raw -Tx4 LOS	Unlatched Tx LOS indicator, channel 4	
	3	Raw -Tx3 LOS	Unlatched Tx LOS indicator, channel 3	
	2	Raw -Tx2 LOS	Unlatched Tx LOS indicator, channel 2	
	1	Raw -Tx1 LOS	Unlatched Tx LOS indicator, channel 1	
	0	Raw -Tx0 LOS	Unlatched Tx LOS indicator, channel 0	
19 13h	7	Raw -Tx7 Fault	Unlatched Tx fault indicator, channel 7	RO Opt.
	6	Raw -Tx6 Fault	Unlatched Tx fault indicator, channel 6	
	5	Raw -Tx5 Fault	Unlatched Tx fault indicator, channel 5	
	4	Raw -Tx4 Fault	Unlatched Tx fault indicator, channel 4	
	3	Raw -Tx3 Fault	Unlatched Tx fault indicator, channel 3	
	2	Raw -Tx2 Fault	Unlatched Tx fault indicator, channel 2	
	1	Raw -Tx1 Fault	Unlatched Tx fault indicator, channel 1	
	0	Raw -Tx0 Fault	Unlatched Tx fault indicator, channel 0	
20 14h	7	Raw _Rx15 CDR _LOL	Unlatched Rx CDR LOL indicator, channel 7	RO Opt.
	6	Raw _Rx14 CDR _LOL	Unlatched Rx CDR LOL indicator, channel 6	
	5	Raw _Rx13 CDR _LOL	Unlatched Rx CDR LOL indicator, channel 5	
	4	Raw _Rx12 CDR _LOL	Unlatched Rx CDR LOL indicator, channel 4	
	3	Raw _Rx11 CDR _LOL	Unlatched Rx CDR LOL indicator, channel 3	
	2	Raw _Rx10 CDR _LOL	Unlatched Rx CDR LOL indicator, channel 2	
	1	Raw _Rx9 CDR _LOL	Unlatched Rx CDR LOL indicator, channel 1	
	0	Raw _Rx8 CDR _LOL	Unlatched Rx CDR LOL indicator, channel 0	
21 15h	7	Raw _Tx7 CDR _LOL	Unlatched Tx CDR LOLindicator, channel 7	RO Opt.
	6	Raw _Tx6 CDR _LOL	Unlatched Tx CDR LOL indicator, channel 6	
	5	Raw _Tx5 CDR _LOL	Unlatched Tx CDR LOL indicator, channel 5	
	4	Raw _Tx4 CDR _LOL	Unlatched Tx CDR LOL indicator, channel 4	
	3	Raw _Tx3 CDR _LOL	Unlatched Tx CDR LOL indicator, channel 3	
	2	Raw _Tx2 CDR _LOL	Unlatched Tx CDR LOL indicator, channel 2	
	1	Raw _Tx1 CDR _LOL	Unlatched Tx CDR LOL indicator, channel 1	
	0	Raw _Tx0 CDR _LOL	Unlatched Tx CDR LOL indicator, channel 0	
22 16h	All	Temperature1 MSB	First internally measured temperature	RO Rqrd.
23 17h	All	Temperature1 LSB		
24 18h	All	Temperature2 MSB	Second internally measured temperature	RO Opt.
25 19h	All	Temperature2 LSB		
26 1Ah	All	Supply 3.3-volt MSB	Internally measured supply voltage, 3.3 volt input voltage in 100uV units	RO Opt.
27	All	Supply 3.3-volt LSB		

1Bh				
28 1Ch	All	Reserved		RO Opt.
29 1Dh	All	Reserved		
30 1Eh	All	Supply Current MSB	Internally measured supply current in 1 mA units.	RO Opt.
31 1Fh	All	Supply Current LSB		
32 20h	All	Elapsed Operating Time MSB	Elapsed (Power-on) Operating Time: Elapsed time in 2 hour units coded as 16-bit unsigned integer	RO Opt.
33 21h	All	Elapsed Operating Time LSB		

8.3.4 Channel Monitors

Real time channel monitoring is performed for each transmit and receive channel and includes Rx optical input power and Tx bias current. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data.

Measured RX received optical power is in mW and can represent either average received power or OMA depending upon how bit 3 of byte 220 (upper memory page 00h) is set. Represented as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 - 65535) with LSB equal to 0.1 uW, yielding a total measurement range of 0 to 6.5535 mW (approx. -40 to +8.2 dBm).

Measured Tx bias current is in mA and are represented as a 16-bit unsigned integer with the current defined as the full 16-bit value (0 - 65535) with LSB equal to 2 uA, yielding a total measurement range of 0 to 131 mA.

Table 19: Channel Monitors (Page 0L)

Byte	Bit	Name	Description	Type
34, 22h	All	Rx8 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 0	RO Opt.
35, 23h	All	Rx8 Power LSB		
36, 24h	All	Rx9 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 1	RO Opt.
37, 25h	All	Rx9 Power LSB		
38, 26h	All	Rx10 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 2	RO Opt.
39, 27h	All	Rx10 Power LSB		
40, 28h	All	Rx11 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 3	RO Opt.
41, 29h	All	Rx11 Power LSB		
42, 2Ah	All	Rx12 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 44	RO Opt.
43, 2Bh	All	Rx12 Power LSB		
44, 2Ch	All	Rx13 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 5	RO Opt.
45, 2Dh	All	Rx13 Power LSB		
46,	All	Rx14 Power MSB	Rx Light Input Monitor in 0.1µW	RO

2Eh			units, channel 6	Opt.
47, 2Fh	All	Rx14 Power LSB		
48, 30h	All	Rx15 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 7	RO Opt.
49, 31h	All	Rx15 Power LSB		
50, 32h	All	Tx0 Bias MSB	Internally measured Tx bias current, channel 0	RO Opt.
51, 33h	All	Tx0 Bias LSB		
52, 34h	All	Tx1 Bias MSB	Internally measured Tx bias current, channel 1	RO Opt.
53, 35h	All	Tx1 Bias LSB		
54, 36h	All	Tx2 Bias MSB	Internally measured Tx bias current, channel 2	RO Opt.
55, 37h	All	Tx2 Bias LSB		
56, 38h	All	Tx3 Bias MSB	Internally measured Tx bias current, channel 3	RO Opt.
57, 39h	All	Tx3 Bias LSB		
58, 3Ah	All	Tx4 Bias MSB	Internally measured Tx bias current, channel 4	RO Opt.
59, 3Bh	All	Tx4 Bias LSB		
60, 3Ch	All	Tx5 Bias MSB	Internally measured Tx bias current, channel 5	RO Opt.
61, 3Dh	All	Tx5 Bias LSB		
62, 3Eh	All	Tx6 Bias MSB	Internally measured Tx bias current, channel 6	RO Opt.
63, 3Fh	All	Tx6 Bias LSB		
64, 40h	All	Tx7 Bias MSB	Internally measured Tx bias current, channel 7	RO Opt.
65, 41h	All	Tx7 Bias LSB		
66, 42h	All	Tx0 Power MSB	Internally measured Tx power, channel 0	RO Opt.
67, 43h	All	Tx0 Power LSB		
68, 44h	All	Tx1 Power MSB	Internally measured Tx power, channel 1	RO Opt.
69, 45h	All	Tx1 Power LSB		
70, 46h	All	Tx2 Power MSB	Internally measured Tx power, channel 2	RO Opt.
71, 47h	All	Tx2 Power LSB		
72, 48h	All	Tx3 Power MSB	Internally measured Tx power, channel 3	RO Opt.
73, 49h	All	Tx3 Power LSB		
74, 4Ah	All	Tx4 Power MSB	Internally measured Tx power, channel 4	RO Opt.
75,	All	Tx4 Power LSB		

4Bh				
76, 4Ch	All	Tx5 Power MSB	Internally measured Tx power, channel 5	RO Opt.
77, 4Dh	All	Tx5 Power LSB		
78, 4Eh	All	Tx6 Power MSB	Internally measured Tx power, channel 6	RO Opt.
79, 4Fh	All	Tx6 Power LSB		
80, 50h	All	Tx7 Power MSB	Internally measured Tx power, channel 7	RO Opt.
81, 51h	All	Tx7 Power LSB		

8.3.5 Control Fields

The control fields allow the host to dynamically change the behavior of the device. The changeable parameters include Tx input equalization, Rx pre-emphasis and output amplitude in addition to disabling channels or squelching and setting the channel polarities.

Tx Input Equalization Control has a four bit code block (bits 7-4 or 3-0) assigned to each channel. Codes 1xxxb are reserved. Code 0111b calls for the maximum equalization supported. Code 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. The exact Tx Equalization parameters are presented in the device datasheet.

Rx Output Pre-emphasis Control has a four bit code block (bits 7-4 or 3-0) assigned to each channel. Codes 1xxxb are reserved. Code 0111b calls for the maximum output pre-emphasis supported. Code 0000b calls for no output pre-emphasis. Intermediate code values call for intermediate levels of output pre-emphasis. The exact Rx Pre-emphasis parameters are presented in the device datasheet.

Rx Output Amplitude Control has a four bit code block (bits 7-4 or 3-0) assigned to each channel. Codes 1xxxb are reserved. Code 0111b calls for the maximum output amplitude supported. Code 0000b calls for the minimum output amplitude supported. Intermediate code values call for intermediate levels of output amplitude. The exact Rx Amplitude parameters are presented in the device datasheet.

Table 20: Control Fields (Page 0L)

Byte	Bits	Name	Description	Type
82	7-4	Tx1 Equalization	Tx input equalization, channel 1	RW
52h	3-0	Tx0 Equalization	Tx input equalization, channel 0	Opt.
83	7-4	Tx3 Equalization	Tx input equalization, channel 3	RW
53h	3-0	Tx2 Equalization	Tx input equalization, channel 2	Opt.
84	7-4	Tx5 Equalization	Tx input equalization, channel 5	RW
54h	3-0	Tx4 Equalization	Tx input equalization, channel 4	Opt.
85	7-4	Tx7 Equalization	Tx input equalization, channel 7	RW
55h	3-0	Tx6 Equalization	Tx input equalization, channel 6	Opt.
86	7	Tx7 Disable	Tx channel disable, channel 7	RW
56h	6	Tx6 Disable	Tx channel disable, channel 6	Opt.
	5	Tx5 Disable	Tx channel disable, channel 5	
	4	Tx4 Disable	Tx channel disable, channel 4	
	3	Tx3 Disable	Tx channel disable, channel 3	
	2	Tx2 Disable	Tx channel disable, channel 2	
	1	Tx1 Disable	Tx channel disable, channel 1	
	0	Tx0 Disable	Tx channel disable, channel 0	

87	7	Tx7 Squelch Disable	Tx squelch disable, channel 7	RW
57h	6	Tx6 Squelch Disable	Tx squelch disable, channel 6	Opt.
	5	Tx5 Squelch Disable	Tx squelch disable, channel 5	
	4	Tx4 Squelch Disable	Tx squelch disable, channel 4	
	3	Tx3 Squelch Disable	Tx squelch disable, channel 3	
	2	Tx2 Squelch Disable	Tx squelch disable, channel 2	
	1	Tx1 Squelch Disable	Tx squelch disable, channel 1	
	0	Tx0 Squelch Disable	Tx squelch disable, channel 0	
88	7	Tx7 Polarity	Tx polarity flip, channel 7	RW
58h	6	Tx6 Polarity	Tx polarity flip, channel 6	Opt.
	5	Tx5 Polarity	Tx polarity flip, channel 5	
	4	Tx4 Polarity	Tx polarity flip, channel 4	
	3	Tx3 Polarity	Tx polarity flip, channel 3	
	2	Tx2 Polarity	Tx polarity flip, channel 2	
	1	Tx1 Polarity	Tx polarity flip, channel 1	
	0	Tx0 Polarity	Tx polarity flip, channel 0	
89	7-4	Rx9 Pre-emphasis	Rx output equalization, channel 1	RW
59h	3-0	Rx8 Pre-emphasis	Rx output pre-emphasis, channel 0	Opt.
90	7-4	Rx11 Pre-emphasis	Rx output equalization channel 3	RW
5Ah	3-0	Rx10 Pre-emphasis	Rx output equalization, channel 2	Opt.
91	7-4	Rx13 Pre-emphasis	Rx output equalization, channel 5	RW
5Bh	3-0	Rx12 Pre-emphasis	Rx output equalization, channel 4	Opt.
92	7-4	Rx15 Pre-emphasis	Rx output equalization, channel 7	RW
5Ch	3-0	Rx14 Pre-emphasis	Rx output equalization, channel 6	Opt.
93	7-3	Reserved		RW
5Dh				Opt.
	2	Soft Reset	Software reset, same effect as RST pin	RW Rqrd.
	1	Power Set	Power override: codes x0 = no override, code 11 = low power, code 01 = high power	RW
	0	Power Override		Opt.
94	7-4	Rx9 Amplitude	Rx output amplitude, channel 1	RW
5Eh	3-0	Rx8 Amplitude	Rx output amplitude, channel 0	Opt.
95	7-4	Rx11 Amplitude	Rx output amplitude, channel 3	RW
5Fh	3-0	Rx10 Amplitude	Rx output amplitude, channel 2	Opt.
96	7-4	Rx13 Amplitude	Rx output amplitude, channel 5	RW
60h	3-0	Rx12 Amplitude	Rx output amplitude, channel 4	Opt.
97	7-4	Rx15 Amplitude	Rx output amplitude, channel 7	RW
61h	3-0	Rx14 Amplitude	Rx output amplitude, channel 6	Opt.
98	7	Rx15 Output Disable	Rx output disable, channel 7	RW
62h	6	Rx14 Output Disable	Rx output disable, channel 6	Opt.
	5	Rx13 Output Disable	Rx output disable, channel 5	
	4	Rx12 Output Disable	Rx output disable, channel 4	
	3	Rx11 Output Disable	Rx output disable, channel 3	
	2	Rx10 Output Disable	Rx output disable, channel 2	
	1	Rx9 Output Disable	Rx output disable, channel 1	
	0	Rx8 Output Disable	Rx output disable, channel 0	
99	7	Rx15 Squelch Disable	Rx squelch disable, channel 7	RW
63h	6	Rx14 Squelch Disable	Rx squelch disable, channel 6	Opt.
	5	Rx13 Squelch Disable	Rx squelch disable, channel 5	
	4	Rx12 Squelch Disable	Rx squelch disable, channel 4	
	3	Rx11 Squelch Disable	Rx squelch disable, channel 3	
	2	Rx10 Squelch Disable	Rx squelch disable, channel 2	
	1	Rx9 Squelch Disable	Rx squelch disable, channel 1	
	0	Rx8 Squelch Disable	Rx squelch disable, channel 0	
100	7	Rx15 Polarity	Rx polarity flip, channel 7	RW

64h	6	Rx14 Polarity	Rx polarity flip, channel 6	Opt.
	5	Rx13 Polarity	Rx polarity flip, channel 5	
	4	Rx12 Polarity	Rx polarity flip, channel 4	
	3	Rx11 Polarity	Rx polarity flip, channel 3	
	2	Rx10 Polarity	Rx polarity flip, channel 2	
	1	Rx9 Polarity	Rx polarity flip, channel 1	
	0	Rx8 Polarity	Rx polarity flip, channel 0	
101	7	Tx7 CDR Bypass	Tx CDR bypass, channel 7	RW
65h	6	Tx6 CDR Bypass	Tx CDR bypass, channel 6	Opt.
	5	Tx5 CDR Bypass	Tx CDR bypass, channel 5	
	4	Tx4 CDR Bypass	Tx CDR bypass, channel 4	
	3	Tx3 CDR Bypass	Tx CDR bypass, channel 3	
	2	Tx2 CDR Bypass	Tx CDR bypass, channel 2	
	1	Tx1 CDR Bypass	Tx CDR bypass, channel 1	
	0	Tx0 CDR Bypass	Tx CDR bypass, channel 0	
102	7	Rx15 CDR Bypass	Rx CDR bypass, channel 7	RW
66h	6	Rx14 CDR Bypass	Rx CDR bypass, channel 6	Opt.
	5	Rx13 CDR Bypass	Rx CDR bypass, channel 5	
	4	Rx12 CDR Bypass	Rx CDR bypass, channel 4	
	3	Rx11 CDR Bypass	Rx CDR bypass, channel 3	
	2	Rx10 CDR Bypass	Rx CDR bypass, channel 2	
	1	Rx9 CDR Bypass	Rx CDR bypass, channel 1	
	0	Rx8 CDR Bypass	Rx CDR bypass, channel 0	

8.3.6 Interrupt Masks

The host system may control which flags result in an interrupt (IntL) by setting high individual bits from a set of masking bits in bytes 103-116. There is one masking bit per alarm flag. A 1 value in a masking bit prevents the assertion of the hardware IntL pin by the corresponding latched flag bit. Masking bits are volatile and startup with all unmasked (masking bits 0).The mask bits may be used to prevent continued interruption from recurring conditions, which would otherwise continually reassert the hardware IntL pin (such as a monitor value hovering around an alarm threshold value).

The clearing of an interrupt mask bit will cause an interrupt to be generated only if the corresponding alarm flag became set while masked and has not been read (and cleared) by the host computer system. There is a maximum of one interrupt generated per occurrence of an alarm condition.

Table 21: Interrupt Masks (Page 0L)

Byte	Bits	Name	Description	Type
103	7	M-Rx15 LOS	Masking bit for Rx LOS indicator, channel 7	RW
67h	6	M-Rx14 LOS	Masking bit for Rx LOS indicator, channel 6	Opt.
	5	M-Rx13 LOS	Masking bit for Rx LOS indicator, channel 5	
	4	M-Rx12 LOS	Masking bit for Rx LOS indicator, channel 4	
	3	M-Rx11 LOS	Masking bit for Rx LOS indicator, channel 3	
	2	M-Rx10 LOS	Masking bit for Rx LOS indicator, channel 2	
	1	M-Rx9 LOS	Masking bit for Rx LOS indicator, channel 1	
	0	M-Rx8 LOS	Masking bit for Rx LOS indicator, channel 0	
104	7	M-Tx7 LOS	Masking bit for Tx LOS indicator, channel 7	RW
68h	6	M-Tx6 LOS	Masking bit for Tx LOS indicator, channel 6	Opt.
	5	M-Tx5 LOS	Masking bit for Tx LOS indicator, channel 5	
	4	M-Tx4 LOS	Masking bit for Tx LOS indicator, channel 4	
	3	M-Tx3 LOS	Masking bit for Tx LOS indicator, channel 3	
	2	M-Tx2 LOS	Masking bit for Tx LOS indicator, channel 2	

	1	M-Tx1 LOS	Masking bit for Tx LOS indicator, channel 1	
	0	M-Tx0 LOS	Masking bit for Tx LOS indicator, channel 0	
105 69h	7	M-Tx7Fault	Masking bit for TxFault indicator, channel 7	RW Opt.
	6	M-Tx6Fault	Masking bit for TxFault indicator, channel 6	
	5	M-Tx5Fault	Masking bit for TxFault indicator, channel 5	
	4	M-Tx4Fault	Masking bit for TxFault indicator, channel 4	
	3	M-Tx3Fault	Masking bit for TxFault indicator, channel 3	
	2	M-Tx2Fault	Masking bit for TxFault indicator, channel 2	
	1	M-Tx1Fault	Masking bit for TxFault indicator, channel 1	
	0	M-Tx0Fault	Masking bit for TxFault indicator, channel 0	
106 6Ah	7	M-Temp High	Masking bit for first temperature monitor high alarm indicator	RO Rqrd.
	6	M-Temp Low	Masking bit for first temperature monitor low alarm indicator	
	5	M-Temp High Warning	Masking bit for first temperature monitor high warning indicator	
	4	M-Temp Low Warning	Masking bit for first temperature monitor low warning indicator	
	3	M-Temp2 High	Masking bit for second temperature monitor high alarm indicator	
	2	M-Temp2 Low	Masking bit for second temperature monitor low alarm indicator	
	1	M-Temp2 High Warning	Masking bit for second temperature monitor high warning indicator	
	0	M-Temp2 Low Warning	Masking bit for second temperature monitor low warning indicator	
107 6Bh	7	M-Vcc3.3 High	Masking bit for 3.3 volts power supply monitor high alarm	RW Opt.
	6	M-Vcc3.3 Low	Masking bit for 3.3 volts power supply monitor low alarm	
	5-0	Reserved		
108 6Ch	7	M-Rx15 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 7	RW Opt.
	6	M-Rx14 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 6	
	5	M-Rx13 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 5	
	4	M-Rx12 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 4	
	3	M-Rx11 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 3	
	2	M-Rx10 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 2	
	1	M-Rx9 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 1	
	0	M-Rx8 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 0	
109 6Dh	7	M-Rx15 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 7	RW Opt.
	6	M-Rx14 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 6	
	5	M-Rx13 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 5	
	4	M-Rx12 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 4	
	3	M-Rx11Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 3	
	2	M-Rx10Power Low	Masking bit for Rx input power low alarm	

		Alarm	indicator, channel 2	
	1	M-Rx9Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 1	
	0	M-Rx8Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 0	
110 6Eh	7	M-Rx15Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 7	RW Opt.
	6	M-Rx14 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 6	
	5	M-Rx13 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 5	
	4	M-Rx12 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 4	
	3	M-Rx11 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 3	
	2	M-Rx10 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 2	
	1	M-Rx9 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 1	
	0	M-Rx8 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 0	
111 6Fh	7	M-Tx7 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 7	RW Opt.
	6	M-Tx6 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 6	
	5	M-Tx5 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 5	
	4	M-Tx4 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 4	
	3	M-Tx3 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 3	
	2	M-Tx2 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 2	
	1	M-Tx1 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 1	
	0	M-Tx0Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 0	
112 70h	7	M-Tx7Bias High	Masking bit for Tx bias current high alarm indicator, channel 7	RW Opt.
	6	M-Tx6 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 6	
	5	M-Tx5 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 5	
	4	M-Tx4 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 4	
	3	M-Tx3 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 3	
	2	M-Tx2 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 2	
	1	M-Tx1 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 1	
	0	M-Tx0 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 0	
113 71h	7	M-Tx7 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 7	RW Opt.
	6	M-Tx6 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 6	
	5	M-Tx5 Power Low	Masking bit for Tx output power low alarm	

		Alarm	indicator, channel 5	
	4	M-Tx4 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 4	
	3	M-Tx3 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 3	
	2	M-Tx2 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 2	
	1	M-Tx1 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 1	
	0	M-Tx0Power Low	Masking bit for TX output power low alarm indicator, channel 0	
114 72h	7	M-Tx7Power High	Masking bit for TX output power high alarm indicator, channel 7	RW Opt.
	6	M-Tx6 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 6	
	5	M-Tx5 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 5	
	4	M-Tx4 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 4	
	3	M-Tx3 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 3	
	2	M-Tx2 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 2	
	1	M-Tx1 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 1	
	0	M-Tx0 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 0	
115 73h	7	M-Rx15CDR LOL	Masking bit for RxCDR LOL indicator, channel 7	RW Opt.
	6	M-Rx14CDR LOL	Masking bit for RxCDR LOL indicator, channel 6	
	5	M-Rx13CDR LOL	Masking bit for RxCDR LOL indicator, channel 5	
	4	M-Rx12CDR LOL	Masking bit for RxCDR LOL indicator, channel 4	
	3	M-Rx11CDR LOL	Masking bit for RxCDR LOL indicator, channel 3	
	2	M-Rx10CDR LOL	Masking bit for RxCDR LOL indicator, channel 2	
	1	M-Rx9CDR LOL	Masking bit for RxCDR LOL indicator, channel 1	
	0	M-Rx8CDR LOL	Masking bit for RxCDR LOL indicator, channel 0	
116 74h	7	M-Tx7CDR LOL	Masking bit for TxCDR LOL indicator, channel 7	RW Opt.
	6	M-Tx6CDR LOL	Masking bit for TxCDR LOL indicator, channel 6	
	5	M-Tx5CDR LOL	Masking bit for TxCDR LOL indicator, channel 5	
	4	M-Tx4CDR LOL	Masking bit for TxCDR LOL indicator, channel 4	
	3	M-Tx3CDR LOL	Masking bit for TxCDR LOL indicator, channel 3	
	2	M-Tx2CDR LOL	Masking bit for TxCDR LOL indicator, channel 2	
	1	M-Tx1CDR LOL	Masking bit for TxCDR LOL indicator, channel 1	
	0	M-Tx0CDR LOL	Masking bit for TxCDR LOL indicator, channel 0	

8.3.7 Alarm Flags Persistence Control

The Alarm Flags Persistence controls determine the behavior of the Interrupt Flag bits in bytes 3 to 16. Normally, the interrupt flag bytes are cleared when they are read by the host system and not reasserted unless the alarm condition goes away and then comes back again. However, if the persistence control bit appropriate to an alarm flag is set, the bit in the Interrupt Flags field is immediately reasserted after the clear-on-read; note that this reassertion does not cause an interrupt to be generated (implicit masking); there is a maximum of one interrupt generated per occurrence of an alarm condition. The alarm persistence control bytes may be loaded from non-volatile memory at power on or reset.

Table 22: Alarm Persistence Control (Page 0L)

Byte	Bit	Name	Description	Type
117 75h	7-2	Reserved		RW Opt.
	1	Persistent CDR LOL Tx alarm	Writing 1b causes CDR LOL Tx alarms in byte 16 to be reasserted after clear-on-read if the CDR LOL condition persists.	
	0	Persistent CDR LOL Rx alarm	Writing 1b causes CDR LOL Rx alarms in byte 15 to be reasserted after clear-on-read if the CDR LOL condition persists.	
118 76h	7	Persistent LOS Tx alarm	Writing 1b causes Tx LOS alarms in byte 4 to be reasserted after clear-on-read if the LOS condition persists.	RW Opt.
	6	Persistent LOS Rx alarm	Writing 1b causes Rx LOS alarms in byte 3 to be reasserted after clear-on-read if the LOS condition persists.	
	5	Persistent Fault Tx alarm	Writing 1b causes Fault Tx alarms in byte 5 to be reasserted after clear-on-read if the Fault condition persists.	
	4	Persistent Bias Tx alarm	Writing 1b causes Tx Bias alarms in bytes 11 and 12 to be reasserted after clear-on-read if the alarm condition persists.	
	3	Persistent Power Tx alarm	Writing 1b causes Tx Power alarms in bytes 13 and 14 to be reasserted after clear-on-read if the alarm condition persists.	
	2	Persistent Power Rx alarm	Writing 1b causes Rx Power alarms in bytes 9 and 10 to be reasserted after clear-on-read if the alarm condition persists.	
	1	Persistent Temperature Tx alarm	Writing 1b causes Temperature alarms in byte 6 to be reasserted after clear-on-read if the alarm condition persists.	
	0	Persistent Voltage Tx alarm	Writing 1b causes Voltage alarms in byte 7 to be reasserted after clear-on-read if the alarm condition persists.	

8.3.8 Password Entry and Change

Bytes 119-126 are reserved for the password entry function. The Password entry bytes are write only and will be retained until power down, reset, or rewritten by host. This function is used to control write access to vendor specific page 02h (eeprom) and other upper pages. Additionally, module vendors may use this function to implement write protection of Serial ID and other read only information. Note that multiple module manufacturer passwords may be defined to allow selective access to write to various sections of memory as allowed above.

8.3.9 Page Select Byte

The value written to the page select determines which upper page is accessed at addresses 128 to 255 (80h to FFh). Attempting to access non-existent upper pages will cause writes to be ignored and reads to return all zeros, all ones, or some other preset value.

8.4 Upper Page 00h

Upper Page 00h consists of the Serial ID and is used for read only identification information. The Serial ID is divided into the Base ID Fields, Extended ID Fields and Vendor Specific ID Fields.

8.4.1 Base ID

The Base ID area provides basic information about the device.
The format of the Serial ID Memory Map is illustrated as follows:

Table 23: Upper Page 0 Overview (Page 0h)

Serial ID Fields (Page 0h)Address	Size (bytes)	Name	Description
Base ID Fields			
128	1	Identifier	Identifier Type of Module
129	1	Ext. Identifier	Extended Identifier
130	1	Connector	Code for connector type
131-138	8	Specification compliance	Code for electronic compatibility or optical compatibility
139	1	Encoding	Code for serial encoding algorithm
140	1	BR, nominal	Nominal bit rate, units of 100 MBits/s
141	1	Extended rate select compliance	Tags for extended rate select compliance
142-146	5	Link length	Link length / transmission media
147	1	Device tech	Device technology
148-163	16	Vendor name	Vendor name (ASCII)
164	1	Extended Module	Extended Module codes for InfiniBand
165-167	3	Vendor OUI	Vendor IEEE company ID
168-183	16	Vendor PN	Part number provided by vendor (ASCII)
184-185	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
186-187	2	Wavelength or Copper cable Attenuation	Nominal laser wavelength (wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5GHz (Adrs 186) and 5.0GHz (Adrs 187)
188-189	2	Wavelength tolerance	Guaranteed range of laser wavelength(+/- value) from nominal wavelength.(wavelength Tolerance=value/200 in nm)
190	1	Max case temp.	Maximum case temperature in degrees C
191	1	CC_BASE	Check code for base ID fields (addresses 128-190 inclusive)
Extended ID Fields			
192-195	4	Options	Indicates which optional capabilities are implemented in the Module
196-211	16	Vendor S/N	Vendor product serial number
212-219	8	Date Code	Vendor's manufacturing date code
220	1	Diagnostic Monitoring Type	Indicates which types of diagnostic monitoring are implemented in the Module
221-222	2	Enhanced Options	Indicates which optional enhanced features are implemented in the Module.
223	1	CC_EXT	Check code for the Extended ID Fields (addresses 192-222 inclusive)
Vendor Specific ID Fields			

224-255	32	Vendor-Specific	Vendor-specific ID information

8.4.2 Identifier and Extended Identifier

The identifier value specifies the physical device described by the serial information. This field should contain the same value as byte 0 in the lower page. These values are maintained in the Transceiver Management section of SFF-8024.

The extended identifier identifies the power consumption class that the device belongs to and provides additional information such as whether the Module card contains a CDR function. The power classes indicate the power consumed per circuit board.

Table 24: Identifiers (Page 0h)

Byte	Bits	Name	Description	Type
128 80h	All	Identifier	Identifier - Type of Serial Module CDFP style 1 or style 2 = 13h	RO Rqrd.
129 81h	7-5	Module Card Power Class	000: Power class 1 (3.0 W maximum) 001: Power class 2 (4.0 W maximum) 010: Power class 3 (5.0 W maximum) 011: Power class 4 (6.0 W maximum) 100: Power class 5 - maximum specified in byte 145 101-111: reserved	RO Rqrd.
	4	CLEI code presence	Coded 1 if CLEI code present in page 02h, otherwise coded 0	
	3	CDR present in TX	Coded 1 if Tx channels include CDRs	
	2	CDR present in RX	Coded 1 if Rx channels include CDRs	
	1-0	CDR Power Class	00: Less than 50 mW per CDR channel 01: 50 to 100 mW per CDR channel 10: 100 to 200 mW per CDR channel 11: More than 200 mW per CDR channel	

8.4.3 Connector Type (Address 130)

The Connector value indicates the external connector provided on the interface. This value shall be included in the serial data. The defined connector type values are shown in the following table:

Table 25: Connector Types

Value	Description of Connector
00h	Unknown or unspecified
01h	SC (Subscriber Connector)
02h	FC Style 1 copper connector
03h	FC Style 2 copper connector
04h	BNC/TNC
05h	Fibre Channel coax headers
06h	Fiber jack
07h	Dual LC (Lucent Connector)
08h	MT-RJ (Mechanical Transfer-Registered Jack
09h	MU (Multiple Optical)
0Ah	SG

0Bh	Optical Pigtail
0Ch	MPO 1x12 (Multifiber Parallel Optic)
0Dh	MPO 2x16
0E-1Fh	Reserved
20h	HSSDC II (High Speed Serial Data Connector)
21h	Copper pigtail
22h	RJ45 (Registered Jack)
23h	No separable connector
24h	MXC 2x16
25h-7Fh	Reserved
80-FFh	Vendor specific
Note: 01h to 05h are not SFP-compatible, and are included for compatibility with GBIC standards.	

8.4.4 Specification Compliance

The Specification Compliance fields are bit-significant indicators defining the electronic or optical interfaces that are supported by the device. For Fibre Channel support, the Fibre Channel speed, transmission media, transmitter technology, and distance capability shall all be indicated.

Table 26: Specification compliance (Page 0h)

Byte	Bits	Name	Description	Type
131 83h	All		10/40G Ethernet Compliance Code	RO Rqrd.
132 84h	All		SONET Compliance codes	RO Rqrd.
133 85h	All		SAS/SATA compliance codes	RO Rqrd.
134 86h	All		Gigabit Ethernet Compliant codes	RO Rqrd.
135 87h	All		Fibre Channel link length	RO Rqrd.
136 88h	All		Fibre Channel Transmitter Technology	RO Rqrd.
137 89h	All		Fibre Channel transmission media	RO Rqrd.
138 8Ah	All		Fibre Channel Speed	RO Rqrd.

8.4.5 Encoding (Address 139)

The encoding value indicates the serial encoding mechanism that is the nominal design target of the particular device. This value shall be contained in the serial data. The defined encoding values shown in the following table:

Table 27: Encoding values

Code	Description of encoding mechanism
00h	Unspecified
01h	8B10B
02h	4B5B
03h	NRZ
04h	SONET Scrambled
05h	64B66B
06h	Manchester
07h	256B/257B (transcoded FEC-enabled data)
08h-FFh	Reserved

8.4.6 BR, nominal (Address 140)

The nominal bit rate (BR, nominal) is specified in units of 100 Megabits per second, rounded off to the nearest 100 Megabits per second. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of 0 indicates that the bit rate is not specified and must be determined from the device technology. The actual information transfer rate may depend on the encoding of the data, as defined by the encoding value. For BR > 25.4Gb/s, set this to FFh and use Address 222.

8.4.7 Extended Rate Select and Global Options

The Extended RateSelect Compliance field is used to allow a single device the flexibility to comply with single or multiple Extended RateSelect definitions. A supported definition is indicated by presence of a "1" in the specified bit position.

Table 28: Extended rate-select compliance (Page 0h)

Byte	Bits	Name	Description	Type
141 8Dh	7	Global Tx Disable	Coded 1 if any Tx Disable control bit being set disables all Tx channels	RO Rqrd.
	6	Global Tx Squelch Disable	Coded 1 if any Tx Squelch Disable control bit being set disables squelching for all Tx channels	
	5	Global Tx Equalization	Coded 1 if writing to any Tx Equalization control field writes the same value to all Tx Equalization control fields	
	4	Global Rx Output Disable	Coded 1 if any Rx Output Disable control bit being set disables the output on all Rx channels	
	3	Global Rx Squelch Disable	Coded 1 if any Rx Squelch Disable control bit being set disables squelching for all Rx channels	
	2	Global Rx Pre-Emphasis	Coded 1 if writing to any Rx Pre-Emphasis control field writes the same value to all Rx Pre-Emphasis control fields	
	1	Global Rx Output Amplitude	Coded 1 if writing to any Rx Output Amplitude control field writes the same value to all Rx Output Amplitude control fields	
	0	Rate Select Version	Coded 1 if QSFP+ Rate Select Version 1 implemented. This functionalityis different from SFF-8472 and SFF-8431.	

8.4.8 Link Length

The link length fields specify the data link length in various transmission media. In each case, a value of zero means that the device does not support the transmission media or that the length information must be determined from the device technology.

Table 29: Link Length (Page 0h)

Address	Bits	Name	Description	Type
142 8Eh	7	New length format	Indicates 16-bit link length and use of variable cable length scale method	RO Rqrd.
	6-5	Cable length scale	0= length is in meters 1= length is in kilometers 2= length is in multiples of 32 meters 3= length is in multiples of 1/256 meters	RO Rqrd.
	4-0	Transmission Media	1= 62.5/125 um MMF (OM1) 2= 50/125um MMF (OM2) 3= EBW 50/125 um MMF (OM3) 4= EBW 50/125um MMF (OM4) 5= SMF 6= Copper	RO Rqrd.
143 8Fh	All	Link Length MSB	Link length in the units identified by the Cable Length Scale	RO Rqrd.
144 90h	All	Link Length LSB		
145 91h	All	Maximum Power	Module card maximum power in tenth-watt units, rounded to the nearest unit. A byte value of 255 indicates a maximum power greater than 25.4 Watts.	RO Rqrd.
146 92h	All	Reserved		RO Rqrd.

8.4.9 Device Technology (Address 147)

The device technology byte specifies the technology used in the device. Four bits are used to identify the technology type and the remaining four bits are used to indicate options implemented.

Table 30: Device technology

Byte	Bits	Name	Description	Type
147 93h	7-4	Technology	Transmitter technology code	RO Rqrd.
	3	Wavelength control	0: No wavelength control 1: Active wavelength control	
	2	Cooling	0: Uncooled transmitter device 1: Cooled transmitter	
	1	Detector type	0: Pin detector 1: APD detector	
	0	Tunable	0: Transmitter not tunable 1: Transmitter tunable	

Table 31: Technology values

Code	Description of physical device
00h	850 nm VCSEL
01h	1310 nm VCSEL
02h	1550 nm VCSEL
03h	1310 nm FP
04h	1310 nm DFB
05h	1550 nm DFB
06h	1310 nm EML
07h	1550 nm EML
08h	Others
09h	1490 nm DFB
0Ah	Copper cable unequalized
0Bh	Copper cable passive equalized
0Ch	Copper cable, near and far end limiting active equalizers
0Dh	Copper cable, far end limiting active equalizers
0Eh	Copper cable, near end limiting active equalizers
0Fh	Copper cable, linear active equalizers

8.4.10 Vendor Name (Addresses 148-163)

The vendor name is a 16 character field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

8.4.11 Extended Module Code

The Extended Module Code defines the electronic or optical interfaces for InfiniBand that are supported by the device.

Table 32: Extended module code (Page 0h)

Byte	Bits	Name	Description	Type
164	7-5	Reserved		RO
A4h	4	EDR Speed	Coded 1 for EDR Speed support	Rqrd.
	3	FDR Speed	Coded 1 for FDR Speed support	
	2	QDR Speed	Coded 1 for QDR Speed support	
	1	DDR Speed	Coded 1 for DDR Speed support	
	0	SDR Speed	Coded 1 for SDR Speed support	

8.4.12 Vendor Organizationally Unique Identifier (OUI, Address 165-167)

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

8.4.13 Vendor Part Number (Address 168-183)

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part

number or product name. A value of all zero in the 16-byte field indicates that the vendor part number is unspecified.

8.4.14 Vendor Revision Number (Address 184-185)

The vendor revision number (vendor rev) is a 2-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the field indicates that the vendor Rev is unspecified.

8.4.15 Wavelength (Address 186-187)

The wavelength field specifies the nominal transmitter output wavelength at room temperature; this is a16-bit value with byte 186 as the high order byte and byte 187 as the low order byte. The laser wavelength value is equal to the 16-bit integer value of the wavelength in nm divided by 20 (units of 0.05nm). This resolution should be adequate to cover all relevant wavelengths yet provide enough resolution for all expected applications. For accurate representation of controlled wavelength applications, this value should represent the center of the guaranteed wavelength range.

If the cable is identified as a copper cable, these addresses will be used to define the cable attenuation. Address 186 (00-FFh) holds an 8 bit value indicating the copper cable attenuation at 2.5GHz in units of 1 dB. Address 187 (00-FFh) holds an 8 bit value indicating the copper cable attenuation at 5.0GHz in units of 1 dB. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

8.4.16 Wavelength Tolerance (Address 188-189)

The wavelength tolerance is the guaranteed +/- range of the transmitter output wavelength under all normal operating conditions; this is a16-bit value with byte 188 as the high order byte and byte 189 as the low order byte. The laser wavelength tolerance is equal to the 16-bit integer value in nm divided by 200 (units of 0.005nm). Thus, the following two examples:

Example 1:
- 10GBASE-LR Wavelength Range = 1260 to 1355 nm
- Nominal Wavelength in bytes 186 - 187 = 1307.5 nm.
- Represented as INT (1307.5 nm * 20) = 26150 = 6626h
- Wavelength Tolerance in bytes 188 - 189 = 47.5nm.
- Represented as INT (47.5 nm * 200) = 9500 = 251Ch

Example 2:
- ITU-T Grid Wavelength = 1534.25 nm with 0.236 nm Tolerance
- Nominal Wavelength in bytes 186 - 187 = 1534.25 nm.
- Represented as INT (1534.25nm * 20) = 30685 = 77DDh
- Wavelength Tolerance in bytes 188 - 189 = 0.236 nm.
- Represented as INT (0.236 nm * 200) = 47 = 002Fh

8.4.17 Maximum Case Temperature (Address 190)

The maximum case temperature field allows specification of a maximum case temperature other than the standard default of 70C. The maximum case temperature is an 8-bit value in degrees C.

8.4.18 CC-BASE (Address 191)

The check code is a one byte code that can be used to verify that the first 63 bytes of serial information in the device is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 128 to byte 190, inclusive.

8.4.19 Options

The bits in the options field shall specify the options implemented in the Module.

Table 33: Options (Page 0h)

Byte	Bit	Name	Description	Type
192 C0h	All	Extended Ethernet Compliance Codes	00h Unspecified 01h 100G AOC (Active optical cable) 02h 100GBASE-SR4 03h 100GBASE-LR4 04h 100GBASE-ER4 05h 100GBASE-SR10 06h 100G CWDM4 Coarse WDM SMF 07h 100G PSM4 Parallel SMF 08h 40GBASE-ER4 09-FFh Reserved	RO Rqrd.
193 C1h	7	Reserved		RO Rqrd.
	6	Reserved		
	5	Rx polarity flip implemented	Coded 1 if Rx polarity flip control provided	
	4	Tx polarity flip implemented	Coded 1 if Tx polarity flip control provided	
	3	TX input Equalization implemented	Coded 1 if Tx equalization control provided	
	2	Rx Loss of Signal implemented	Coded 1 if Rx LOS alarm flags provided	
	1	Rx preemphasis implemented	Coded 1 if Rx pre-emphasis control provided	
	0	Rx output amplitude implemented	Coded 1 if Rx output amplitude control provided	
194 C2h	7	Tx CDR Bypass implemented	Coded 1 if Tx CDR bypass control provided	RO Rqrd.
	6	Rx CDR Bypass implemented	Coded 1 if Rx CDR bypass control provided	
	5	Tx CDR Loss of Lock (LOL) Flag implemented	Coded 1 if Tx CDR LOL alarm flag provided	
	4	Rx CDR Loss of Lock (LOL) Flag implemented	Coded 1 if Rx CDR LOL alarm flag provided	
	3	Rx Squelch Disable implemented	Coded 1 if Rx Squelch Disable control provided	
	2	Rx Output Disable implemented	Coded 1 if Rx Output Disable control provided	
	1	Tx Squelch Disable implemented	Coded 1 if Tx Squelch Disable control provided	
	0	Tx Squelch present	Coded 1 if Tx Squelch provided	
195 C3h	7	Memory page 02 present	Coded 1 if memory page 02h provided	RO Rqrd.

	6	Memory page 01 present	Coded 1 if memory page 01h provided	
	5	Tx Rate Select implemented	Coded 1 if Tx Rate Select control provided	
	4	Tx Disable implemented	Coded 1 if Tx Disable control provided	
	3	Tx Fault Flag implemented	Coded 1 if Tx Fault supported	
	2	Tx Squelch Pave	Coded 1 if Tx Squelch implemented to reduce Pave; coded 0 if Tx Squelch implemented to reduce OMA	
	1	Tx LOS Flag implemented	Coded 1 if Tx LOS alarm flag provided	
	0	Rx Squelch present	Coded 1 if Rx Squelch provided	

8.4.20 Vendor Serial Number

The vendor serial number (vendor SN) is a 16-character field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the Product. Note that some products may use two or more modules connected by optical fiber; individual module serial numbers are stored in the vendor-specific area. Direct attach cables are defined to have common serial numbers on both sides with -A, -B to identify the different ends. Both CDFP boards in a single module on one side have the same letter. Octopus cables use the additional letters -C,-D etc. A module with a separable connector uses -T (transceiver).

8.4.21 Date Code

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory. The date code shall be in the following format:

```
Bytes 212-213:    ASCII code, two low order digits of year (00=2000)
Bytes 214-215:    ASCII code digits of month (01=Jan through 12=Dec)
Bytes 216-217:    ASCII code day of month (01-31)
Bytes 218-219:    ASCII code, vendor specific lot code, may be blank
```

The date code and vendor serial number fields are the same as specified for QSFP.

8.4.22 Diagnostic Monitoring Type

Diagnostic Monitoring Type is a 1-byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the particular Module. Bit indicators are as follows:

Table 34: Diagnostic Monitoring Type (Page 0h)

Byte	Bit	Name	Description	Type
220 DCh	7	Reserved		RO Rqrd.
	6	Internal Temperature2 Monitor implemented	Coded 1 if Temperature2 provided as an additional internal real-time monitor	
	5	Peak Temperature2 Monitor implemented	Coded 1 if Temperature2 provided as peak of Temperature1 monitor	
	4	Rx Optical Power Monitor implemented	Coded 1 if individual Rx Power Monitors provided	
	3	Rx Optical Power Measurement Type	Rx Power measurement type, 0=OMA, 1=average power	
	2	Tx Optical Power Channel Monitoring implemented	Coded 1 if individual Tx Optical Power Monitors provided	
	1	Tx Bias Monitor implemented	Coded 1 if individual Tx Bias Monitors provided	
	0	Current Monitor Implemented	Coded 1 if module card current monitor provided	

8.4.23 Enhanced Options

The bits in the enhanced options field specify the enhanced options implemented in the Module.

Table 35: Enhanced Options (Page 0h)

Byte	Bit	Name	Description	Type
221 DDh	7	Internal 3.3 volts Monitor implemented	Coded 1 if Internal 3.3 volts Vcc Monitor provided	RO Rqrd.
	6	Reserved		
	5	Elapsed Operating Time implemented	Coded 1 if Elapsed Operating Time provided	
	4	Alarm Persistence Control implemented	Coded 1 if Alarm Flag persistence control provided	
	3	Rx Rate Select implemented	Coded 1 if Rx Rate Select control provided	
	2	Application Select implemented	Coded 1 if Application Select control provided	
	1-0	Extended Bit Rate Scale	00: Extended Bit rate is in multiples of 250 Mb/s rounded to the nearest 250 Mb/s 01: Extended Bit rate is in multiples of 500 Mb/s rounded to the nearest 500 Mb/s 10: Extended Bit rate is in multiples of 1000 Mb/s rounded to the nearest 1000 Mbps 11: Extended Bit rate is in multiples of 2 Gb/s rounded to the nearest 2 Gb/s	
222 DEh	All	Extended Bit Rate	Nominal bit rate per channel in the units specified in the bit rate scale	RO Rqrd.
223	All	CC-EXT	Checksum on Extended IB bytes 192-224	

8.4.24 CC-EXT (Byte 223)

The check code is a one-byte code that can be used to verify that the first 33 bytes of extended serial information in the Module is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 192 to byte 224, inclusive.

8.4.25 Vendor-Specific ID

The vendor-specific ID area may contain vendor specific read-only information.

8.5 Upper Page 03h

The upper memory map page 03h contains module thresholds, channel thresholds, and optional channel controls. Upper page 03h is subdivided into several areas as illustrated in the following table:

Table 36: Upper Page 3 Overview (Page 3h)

Address	Description	Type
128 – 175	Module Thresholds (48 Bytes)	Read-only
176 – 215	Channel Thresholds (40 Bytes)	Read-only
216 – 241	Extended Channel Controls (26 bytes)	Read/Write
242 – 251	Reserved (10 bytes)	Read/Write
252 – 255	Extended ID (4 bytes)	Read-only

8.5.1 Module card Thresholds

Each quantitative module card monitor has a corresponding high alarm and low alarm threshold. Some monitors may also have high warning and low warning thresholds. For each monitor that is implemented, high and low alarm thresholds are required. These factory-preset values allow the user to determine when a particular value is outside of normal limits as determined by the device manufacturer. The values are stored in the same format as the corresponding monitor value reported in lower page 00L. The threshold values are stored in read-only memory in upper memory page 03h as shown below:

Table 37: Module card Thresholds (Page 3h)

Address	Description
128 – 129	High alarm threshold for first temperature monitor
130 – 131	Low alarm threshold for first temperature monitor
132 – 133	High warning threshold for first temperature monitor
134 – 135	Low warning threshold for first temperature monitor
136 – 137	High alarm threshold for second temperature monitor (if any)
138 – 139	Low alarm threshold for second temperature monitor (if any)
140 – 141	High warning threshold for second temperature monitor (if any)
142 – 143	Low warning threshold for second temperature monitor (if any)
144 – 145	High alarm threshold for 3.3 volt power supply monitor
146 – 147	Low alarm threshold for 3.3 volt power supply monitor
148 – 175	Reserved

8.5.2 Channel Thresholds

Each quantitative channel monitor also has a corresponding high alarm and low alarm threshold. Some monitors may also have high warning and low warning thresholds. These threshold values are stored in read-only memory in upper memory page 03h as shown below:

Table 38: Channel Thresholds (Page 3h)

Address	Description
176 – 177	High alarm threshold for Rx optical power monitor
178 – 179	Low alarm threshold for Rx optical power monitor
180 – 181	Reserved
182 – 183	Low warning threshold for Rx optical power monitor
184 – 185	High alarm threshold for Tx bias current monitor
186 – 187	Low alarm threshold for Tx bias current monitor
188 – 189	Reserved
190 – 191	Reserved
192 – 193	High alarm threshold for Tx optical power monitor (if any)
194 – 195	Low alarm threshold for Tx optical power monitor (if any)
196 – 197	Reserved
198 – 199	Reserved
200 – 215	Reserved

8.5.3 Extended Channel Controls

The extended channel control fields allow the host computer system to change the gross behavior of the device. The changeable parameters include data rate and application supported by the channel.

Rate Select is an optional control used to limit the receiver bandwidth for compatibility with multiple data rates and allows the transmitter to be fine-tuned for specific data rates. The Module may:

a) Provide no support for rate selection
b) Rate selection using extended rate select
c) Rate selection with application select tables

The Extended Rate Select Controls have a four bit code block (bits 7-4 or 3-0) assigned to each channel. Codes 1xxxb are reserved. Code 0000b calls for no rate selection. Code 0111b calls for the highest data rate supported. Code 0001b calls for the lowest data rate supported. Intermediate code values call for intermediate data rates if any. The exact Rate Select parameters are presented in the device datasheet.

When the Extended Rate Select bits for a particular channel are all zeros, the Application Select method defined in Page 01h may be used. The host reads the entire Application Select Table (AST) on page 01h to determine the capabilities of the Module card. The host controls each channel separately by writing a Control Mode and Table Select (TS) byte to the Application Select bytes. The two-bit Control Mode value occupies the most-significant bits of the control byte and defines the application control mode. The six-bit Table Select value occupies the least-significant bits of the control byte and selects module card behavior from the Application Select Table among the 63 possibilities described there (values 000000b to 111110b). Note that value 111111b is invalid.

The extended channel controls in upper page 03h are as follows:

Table 39: Extended Channel Controls (Page 3h)

Byte	Bits	Name	Description	Type
216	7-4	Tx1 Rate Select	Tx data rate select, channel 1	RW
D8h	3-0	Tx0 Rate Select	Tx data rate select, channel 0	Opt.
217	7-4	Tx3 Rate Select	Tx data rate select, channel 3	RW
D9h	3-0	Tx2 Rate Select	Tx data rate select, channel 2	Opt.
218	7-4	Tx5 Rate Select	Tx data rate select, channel 5	RW
DAh	3-0	Tx4 Rate Select	Tx data rate select, channel 4	Opt.
219	7-4	Tx7 Rate Select	Tx data rate select, channel 7	RW
DBh	3-0	Tx6 Rate Select	Tx data rate select, channel 6	Opt.
220	7-4	Rx9 Rate Select	Rx data rate select, channel 1	RW
DCh	3-0	Rx8 Rate Select	Rx data rate select, channel 0	Opt.
221	7-4	Rx11 Rate Select	Rx data rate select, channel 3	RW
DDh	3-0	Rx10 Rate Select	Rx data rate select, channel 2	Opt.
222	7-4	Rx13 Rate Select	Rx data rate select, channel 5	RW
DEh	3-0	Rx12 Rate Select	Rx data rate select, channel 4	Opt.
223	7-4	Rx15 Rate Select	Rx data rate select, channel 7	RW
DFh	3-0	Rx14 Rate Select	Rx data rate select, channel 6	Opt.
224	7-6	Tx0 AST Control Mode	Tx application select, channel 0	RW
E0h	5-0	Tx0 AST Select Index		Opt.
225	7-6	Tx1 AST Control Mode	Tx application select, channel 1	RW
E1h	5-0	Tx1 AST Select Index		Opt.
226	7-6	Tx2 AST Control Mode	Tx application select, channel 2	RW
E2h	5-0	Tx2 AST Select Index		Opt.
227	7-6	Tx3 AST Control Mode	Tx application select, channel 3	RW
E3h	5-0	Tx3 AST Select Index		Opt.
228	7-6	Tx4 AST Control Mode	Tx application select, channel 4	RW
E4h	5-0	Tx4 AST Select Index		Opt.
229	7-6	Tx5 AST Control Mode	Tx application select, channel 5	RW
E5h	5-0	Tx5 AST Select Index		Opt.
230	7-6	Tx6 AST Control Mode	Tx application select, channel 6	RW
E6h	5-0	Tx6 AST Select Index		Opt.
231	7-6	Tx7 AST Control Mode	Tx application select, channel 7	RW
E7h	5-0	Tx7 AST Select Index		Opt.
232	7-6	Rx8 AST Control Mode	Rx application select, channel 0	RW
E8h	5-0	Rx8 AST Select Index		Opt.
233	7-6	Rx9 AST Control Mode	Rx application select, channel 1	RW
E9h	5-0	Rx9 AST Select Index		Opt.
234	7-6	Rx10 AST Control Mode	Rx application select, channel 2	RW
EAh	5-0	Rx10 AST Select Index		Opt.
235	7-6	Rx11 AST Control Mode	Rx application select, channel 3	RW
EBh	5-0	Rx11 AST Select Index		Opt.
236	7-6	Rx12 AST Control Mode	Rx application select, channel 4	RW
ECh	5-0	Rx12 AST Select Index		Opt.
237	7-6	Rx13 AST Control Mode	Rx application select, channel 5	RW
EDh	5-0	Rx13 AST Select Index		Opt.
238	7-6	Rx14 AST Control Mode	Rx application select, channel 6	RW
EEh	5-0	Rx14 AST Select Index		Opt.
239	7-6	Rx15 AST Control Mode	Rx application select, channel 7	RW
EFh	5-0	Rx15 AST Select Index		Opt.
240	7	RX15 Channel Fault Squelch	Disable all FAWS reports from RX bit 7	RW
F0h	6	RX14 Channel Fault Squelch	Disable all FAWS reports from RX bit 6	Opt.
	5	RX13 Channel Fault Squelch	Disable all FAWS reports from RX bit 5	
	4	RX12 Channel Fault	Disable all FAWS reports from RX bit 4	

		Squelch		
	3	RX11 Channel Fault Squelch	Disable all FAWS reports from RX bit 3	
	2	RX10 Channel Fault Squelch	Disable all FAWS reports from RX bit 2	
	1	RX9 Channel Fault Squelch	Disable all FAWS reports from RX bit 1	
	0	RX8 Channel Fault Squelch	Disable all FAWS reports from RX bit 0	
241 F1h	7	TX7 Channel Fault Squelch	Disable all FAWS reports from TX bit 7	RW Opt.
	6	TX6 Channel Fault Squelch	Disable all FAWS reports from TX bit 6	
	5	TX5 Channel Fault Squelch	Disable all FAWS reports from TX bit 5	
	4	TX4 Channel Fault Squelch	Disable all FAWS reports from TX bit 4	
	3	TX3 Channel Fault Squelch	Disable all FAWS reports from TX bit 3	
	2	TX2 Channel Fault Squelch	Disable all FAWS reports from TX bit 2	
	1	TX1 Channel Fault Squelch	Disable all FAWS reports from TX bit 1	
	0	TX0 Channel Fault Squelch	Disable all FAWS reports from TX bit 0	

Note: FAWS = Fault, Alarm, Warning, Status

The setting of any bit in upper page 3 byte 240 inhibits the setting of the corresponding bit in lower page bytes 3 (Rx LOS), 8 (Rx Low Power Warning), 9 (Rx Low Power Alarm), 10 (Rx High Power Alarm), 15 (Rx CDR LOL), 17 (Raw Rx LOS) and 20 (Raw Rx CDR LOL).

The setting of any bit in upper page 3 byte 241 inhibits the setting of the corresponding bit in lower page bytes 4 (Tx LOS), 5 (Tx Fault), 11 (Tx Bias Low Alarm), 12 (Tx Bias High Alarm), 13 (Tx Low Power Alarm), 14 (Tx High Power Alarm), 16 (Tx CDR LOL), 18 (Raw Tx LOS), 19 (Raw Tx Fault) and 21 (Raw Tx CDR LOL).

8.5.4 Extended ID

The Extended ID fields provide vendor-specific information about the construction of the module. This information is necessary for determining the suitability of doing embedded firmware upgrades in the field. The extended ID information is as follows:

Table 40: Extended ID Fields (Page 3h)

Byte	Bits	Name	Description	Type
252 FCh	All	H/W rev	Hardware revision number (if any)	RO Opt.
253 FDh	All	H/W type code	Identifier for the hardware platform within the module	RO Opt.
254 FEh	All	F/W major rev	Major revision number of the embedded firmware	RO Opt.
255 FFh	All	F/W minor rev	Minor revision number of the embedded firmware	RO Opt.

8.6 Upper Page 01h

The format of upper page 01h is identical to that specified for QSFP. For the CDFP products upper page 01h is not used.

8.7 Upper Page 02h

Upper Page 02h is optionally provided as user writable EEPROM. The host system may read or write this memory for any purpose.

9 CDFP MSA Management Interface Memory Map–Style 3

9.1 Overview

Each end of the CDFP Style 3 AOC or Style 3 transceiver features two module cards, each of which contains a microcontroller. One of them is a 16-channel transmitter and the other one is a 16-channel receiver. These transmitters and receivers may contain retimers as shown in the example below. The connectivity between these components on each module card is illustrated as follows:

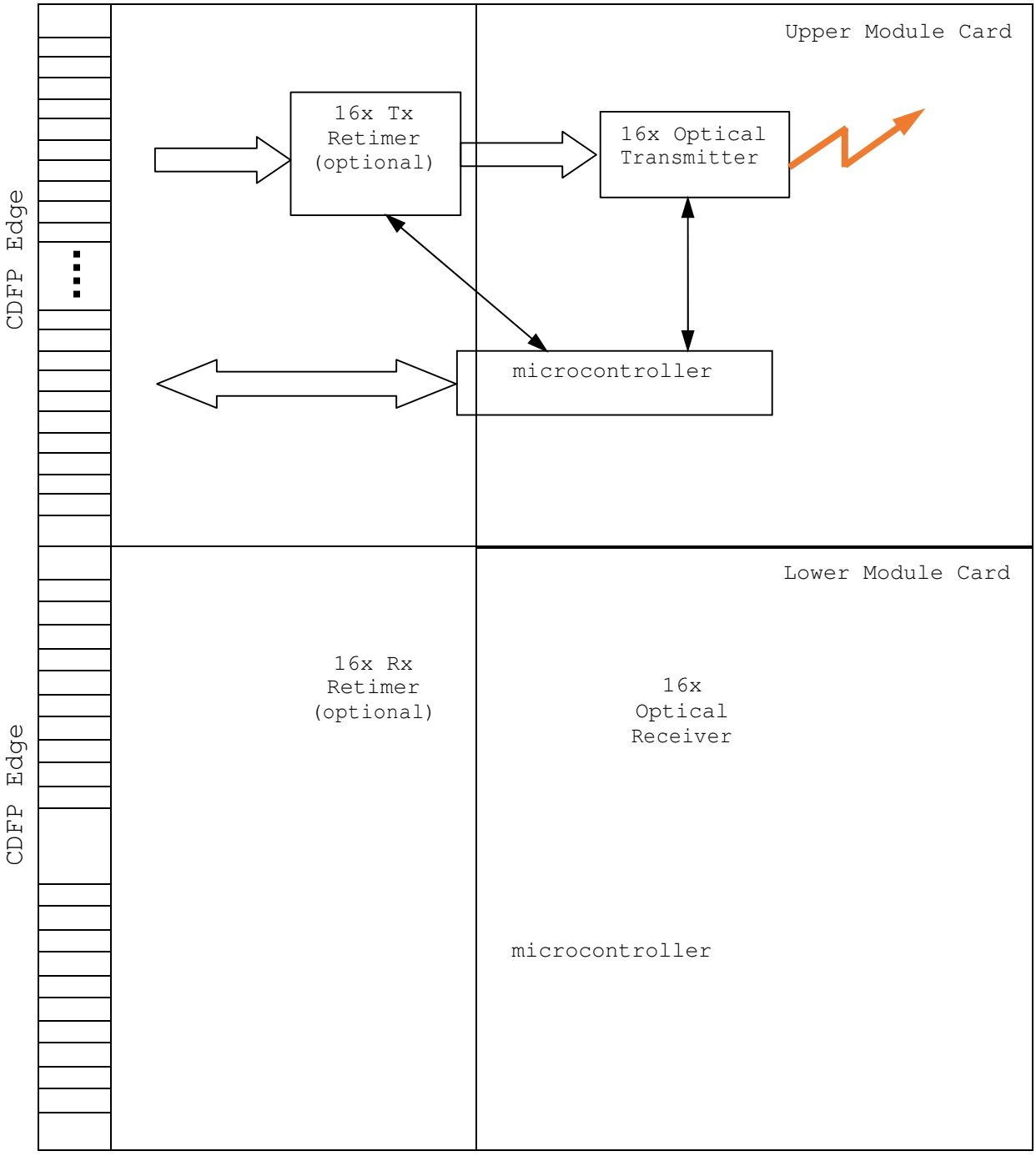


Figure 62: Example CDFP Style 3 optical transceiver implementation

The microcontroller manages the operation of both the optical transmitters/receivers and the retimers and presents a standard management interface to the host computer system. The management interface provided is the industry standard QSFP specification (SFF-8636) extended to sixteen channels. Each circuit board reports its own measurements of temperature, voltage, etc. Similarly, "global" control mechanisms are local to the circuit board being addressed.

The upper module card handles CDFP Tx channels 0 through 15; the lower module card handles CDFP Rx channels 0 through 15. The terms Tx and Rx represent the host's viewpoint – the host transmits data through the Tx channels and receives data through the Rx channels.

9.2 Management Interface

At power-on or module insertion into the CDFP connector, the host computer system detects the presence of the module by the change of state of the ModPrsL (Module Present, active Low) signal from the module card. The module card will then initialize itself and signal that it is ready to communicate with the host computer system by asserting a low level on the IntL signal. The host computer system should then interrogate the module card via the two-wire serial interface to determine the module card status.

The two-wire serial interface (SCL and SDA) deviates from the QSFP specification in that the two-wire serial address for the lower circuit board is B2h/B3h (1011001x) (for 7 bit addressing it would be 0x59) and the two-wire serial address for the upper circuit board is BAh/BBh (1011101x) (for 7 bit addressing it would be 0x5D). The 2 two-wire serial interfaces (one on each circuit board) operate independently from each other. Note: The CDFP modules have no ModSelL signal input and module selection must be made via alternate means not defined in this document.

Like the QSFP specification, the CDFP provides a memory map with a lower page (addresses 00h to 7Fh) and multiple upper pages (addresses 80h to FFh). The lower page is always accessible and contains critical monitoring information and control fields. The last byte of the lower page, address 7Fh, can be written with a value indicating which upper page is to be accessed using the upper page addresses. The CDFP module card has 3 upper pages.

All pages in the memory map are readable at all times. Some areas in the QSFP-like pages are writable by the host system; these are listed below. To prevent inadvertent changes to other areas in the memory map, some areas are protected by passwords; write access to these areas is enabled by writing the appropriate password into the password field at the top of the lower page (addresses 7Bh to 7Eh).

The lower 128 byte of the two-wire serial bus address space is used to access a variety of measurement and diagnostic functions, a set of control functions, and a means to select which of the upper memory map pages are accessed on subsequent accesses. This portion of the address space is always directly addressable and thus, is chosen for monitoring and control functions that may need to be repeatedly accessed.

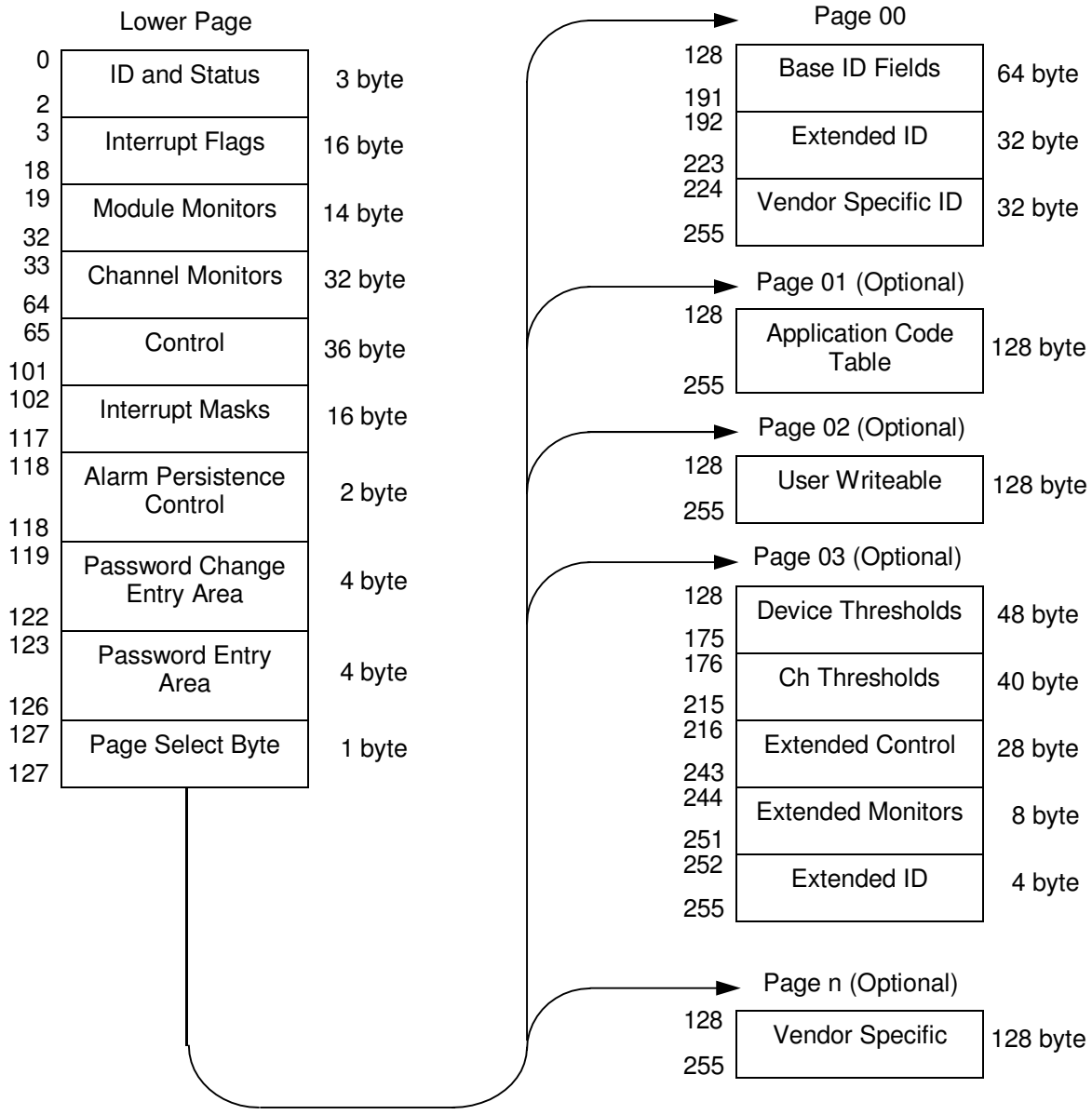


Figure 63: CDFP Style 3 memory map structure

9.3 Lower Page

The lower 128 byte of the two-wire serial bus address space is used to access a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of the various upper memory pages are accessed on subsequent accesses. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed.

9.3.1 ID and Status

The identifier value (byte 0) specifies the type of the physical device described by the serial information. The identifier value is the same value as page 0 byte 128. The DataNotReady bit is high during module power up and prior to a valid suite of monitor readings. Once all monitor readings are valid, the bit is set low until the device is powered down or reset.
All summary bits 2-6 are non-latched, reflecting real-time values in the specific registers. This is to avoid multiple levels of latching and clearing faults.

9.3.2 Interrupt Flags

A portion of the memory map (bytes 3 through 18), form a flags field. Within this field, the status of LOS and Tx Fault as well as alarms and warnings for the various monitored items is reported. If a monitor is implemented the associated flag must also be implemented. For normal operation and default state, the bits in this field have the value of 0b. For the defined conditions of LOS, Fault, module and channel alarms and warnings, the appropriate bit or bits are set, value = 1b. Once asserted, the bits remain set (latched) until cleared by a read operation that includes the affected bit or reset by the ResetL pin. After being read and cleared, the bit may be set again if the condition persists and the appropriate persistence control bit is set (see below).

9.3.3 Module Card Monitors

Optional real time monitoring for the module includes Module Card temperature, supply voltage, supply current and monitoring for each transmit and receive channel. Channel monitoring functions are described in section 0 below. Measured temperature is reported in an 8-bit data field, supply voltage, supply current and elapsed operating time in 16-bit data fields.

Internal measured device temperatures are represented in 8-bit signed values in increments of 1°C, yielding a total range of -128 °C to 127 °C that is considered valid in the range specified in the device datasheet. Temperature accuracy is vendor specific but must be better than ±3 °C over the specified operating temperature and voltage.

Internally measured Module 3.3 V supply voltage is represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0 - 65535) with LSb equal to 100 μV, yielding a total measurement range of 0 to +6.55 Volts. Accuracy is vendor specific but must be better than ±3 % of the manufacturer's nominal value over specified operating temperature and voltage.

Internally measured supply current is represented as a 16-bit unsigned integer with the current defined as the full 16-bit value (0 - 65535) with LSb equal to 1 mA, yielding a total measurement range of 0 to 65.5 A. Accuracy is vendor specific but must be better than ±10 % of the maximum current of the vendor's specified power class over operating temperature and voltage.

Elapsed operating time is represented as a 16-bit unsigned integer with the time since power-on or reset defined as the full 16-bit value (0 - 65535) with LSb equal to 2 hours, yielding a total measurement range of 0 to +14.96 years.

The Raw LOS, Fault and CDR LOL indicators show the real-time unlatched state of the respective channel monitors. Whereas the latched alarm flags (bytes 3 through 16) show the onset of a particular condition, the negation of the corresponding raw flag shows the cessation of the condition, implying that the channel may now be used for data transfer.

9.3.4 Channel Monitors

Real time channel monitoring is performed for each transmit and receive channel and includes Rx optical input power and Tx bias current. Alarm and warning threshold values should be interpreted in the same manner as real time 8-bit data.

Measured Rx received optical power is in mW and can represent either average received power or OMA depending upon how bit 3 of byte 220 (upper memory page 00) is set. Represented as an 8-bit unsigned integer with the power defined as the full 8-bit value (0 - 255), with LSb equal to 20μW, yielding a total measurement range of 0 to 5.1 mW (approx. -17 to +7 dBm).

Measured Tx bias current is in mA and is represented as an 8-bit unsigned integer with the current defined as the full 8-bit value (0 - 255) with LSb equal to 0.1 mA, yielding a total measurement range of 0 to 25.5 mA.

9.3.5 Control Fields

The control fields allow the host to dynamically change the behavior of the device. The changeable parameters include Tx input equalization, Rx pre-emphasis and output amplitude in addition to disabling channels or squelching and setting the channel polarities.

Tx Input Equalization Control has a four bit code block (bits 7-4 or 3-0) assigned to each channel- Codes 1xxxb a reserved. Code 0111b calls for the maximum equalization supported. Code 0000b calls for no equalization. Intermediate code values call for intermediate levels of equalization. The exact Tx Equalization parameters are presented in the device datasheet.

Rx Output Pre-emphasis Control has a four bit code block (bits 7-4 or 3-0) assigned to each channel. Codes 1xxxb are reserved. Code 0111b calls for the maximum output pre-emphasis supported. Code 0000b calls for no output pre-emphasis. Intermediate code values call for intermediate levels of output pre-emphasis. The exact Rx Pre-emphasis parameters are presented in the device datasheet.

Rx Output Amplitude Control has a four bit code block (bits 7-4 or 3-0) assigned to each channel. Codes 1xxxb are reserved. Code 0111b calls for the maximum output amplitude supported. Code 0000b calls for no output amplitude. Intermediate code values call for intermediate levels of output amplitude. The exact Rx Amplitude parameters are presented in the device datasheet.

The setting of any bit in byte 98-99 inhibits the setting of the corresponding bit in lower page bytes 3 (LOS), 8 (Low Power Warning), 9 (Low Power Alarm), 10 (High Power Alarm), 15 (CDR LOL), 17 (Raw LOS) and 20 (Raw CDR LOL).

9.3.6 Interrupt Masks

The host system may control which flags result in an interrupt (IntL) by setting the individual bits from a set of masking bits in bytes 102-117. There is one masking bit per alarm flag. A 1 value in a masking bit prevents the assertion of the hardware IntL pin by the corresponding latched flag bit. Masking bits are volatile and start up with all unmasked (masking bits 0). The mask bits may be used to prevent continued interruption from recurring conditions, which would otherwise continually reassert the hardware IntL pin (such as a monitor value hovering around an alarm threshold value).

The clearing of an interrupt mask bit will cause an interrupt to be generated only if the corresponding alarm flag became set while masked and has not been read (and cleared) by the host computer system. There is a maximum of one interrupt generated per occurrence of an alarm condition.

9.3.7 Alarm Persistence Control

The Alarm Flags Persistence controls determine the behavior of the Interrupt Flag bits in bytes 3 to 18. Normally, the interrupt flag bytes are cleared when they are read by the host system and not reasserted unless the alarm condition goes away and then comes back again. However, if the persistence control bit appropriate to an alarm flag is set, the bit in the Interrupt Flags field is immediately reasserted after the clear-on-read; note that this reassertion does not cause an interrupt to be generated (implicit masking); there is a maximum of one interrupt generated per occurrence of an alarm condition. The alarm persistence control bytes may be loaded from non-volatile memory at power on or reset. Non-volatile persistence control is configured by setting bit 7 in byte 118 to 1.

9.3.8 Password Entry and Change

Bytes 119-126 are served for the password entry function. The password entry bytes are write only and will be retained until power down, reset, or rewritten by host. This function is used to control write access to vendor specific page 02 (EEPROM) and other upper pages. Additionally, module vendors may use this function to implement write protection of Serial ID and other read only information. Note that multiple module manufacturer passwords may be defined to allow selective access to write to various sections of the memory as allowed above.

9.3.9 Page Select Byte

The value written to the page select determines which upper page is accessed at addresses 128 to 255 (80h to FFh). Attempting to access non-existent upper pages will cause writes to be ignored and reads to return all zeroes, all ones, or some other preset value.

9.4 Lower Page Summary

The lower page is subdivided into several areas as illustrated in the following table:

Table 41: Lower Memory Page Summary

Address	Description	Type
0-2	ID and Status	Read-Only
3-18	Status Interrupt Flags (SIF)	Read-Only
19-32	Module Monitors	Read-Only
33-64	Channel Monitors	Read-Only
65-101	Control Fields	Read/Write
102-117	Interrupt Flag Masks	Read/Write
118	Interrupt Flag Persistence Control	Read/Write
119-.122	Password Change Entry Area	Write-Only
123-126	Password Entry Area	Write-Only
127	Page Select byte	Read/Write

9.5 Lower Page Overview

Table 42: Lower Memory Page Overview

Byte	Rx, Lower Card	Tx, Upper Card	Type	Option
0	Identifier	Identifier	RO	Required
1	Version ID	Version ID	RO	Required
2	Summary	Summary	RO	Required
3-4	L-Rx LOS	L-Tx LOS	RO	Optional
5-6	L-Rx CDR LOL	L-Tx CDR LOL	RO	Optional
7-8	Reserved	L-Tx Fault	RO	Optional
9-10	Reserved	Tx High Bias Alarm	RO	Optional
11-12	Rx Low Power Warning	Tx Low High Bias Alarm	RO	Optional
13-14	Rx High Power Alarm	Tx High Power Alarm	RO	Optional
15-16	Rx Low Power Alarm	Tx Low Power Alarm	RO	Optional
17	Temp H/L A/W	Temp H/L A/W	RO	Optional
18	Vcc H/L A/W	Vcc H/L A/W	RO	Optional
19-20	Raw Rx LOS	Raw Tx LOS	RO	Optional
21-22	Raw Rx CDR LOL	Raw Tx CDR LOL	RO	Optional
23-24	Reserved	Raw Tx Fault	RO	Optional
25	Temperature 1	Temperature 1	RO	Optional
26	Temperature 2	Temperature 2	RO	Optional
27-28	Vcc	Vcc	RO	Optional
29-30	Icc	Icc	RO	Optional
31-32	TiO	TiO	RO	Optional
33-48	Rx Optical Power	Tx Optical Power	RO	Optional
49-64	Reserved Channel Mon	Tx Bias Current	RO	Optional
65-66	Rx Disable	Tx Disable	RW	Optional
67-68	Rx Squelch Disable	Tx Squelch Disable	RW	Optional
69-70	Rx Polarity Flip	Tx Polarity Flip	RW	Optional
71-72	Rx CDR Bypass	Tx CDR Bypass	RW	Optional
73-80	Rx OA	Tx Adaptive Equalization Enable	RW	Optional
81-88	Rx PE	Tx Equalization	RW	Optional
89-96	Rx Rate Select	Tx Rate Select	RW	Optional
97-98	Rx Channel FAWS disable	Tx Channel FAWS disable	RW	Optional
99	Rx SIF disable	Tx SIF disable	RW	Optional
100	Reset, Pwr Down, Pwr Override	Reset, Pwr Down, Pwr Override	RW	Optional
101	Reserved	Reserved	RW	Optional
102-117	Mask for 3-18	Mask for 3-18	RW	Optional
118	Alarm Persistence Control	Alarm Persistence Control	RW	Optional
119-122	Password Change Entry Area	Password Change Entry Area	WO	Optional
123-126	Password Entry Area	Password Entry Area	WO	Required
127	Page Select byte	Page Select byte	RW	Required

9.6 Lower Page Rx

Table 43: Lower Memory Page Rx

Byte	Bit	Name	Description	Type	Option
0	All	Identifier	Identifier - Type of Serial Module(same value as page 0 byte 128)	RO	Required
1	All	Version ID	Identifier - Version of Serial Module Specification	RO	Required
2	7	Flat_mem	Upper memory flat or paged. 0= paged, 1= Page 00h only	RO	Required
	6	Reserved			
	5	Rx Power Alarm/Warning Summary	Set, when any bit in #11-16 is set		
	4	Reserved			
	3	Rx LOS and LOL Alarm Summary	Set, when any bit in #3-8 is set		
	2	Temperature and Vcc Alarm Summary	Set, when any bit in #17-18 is set		
	1	Interrupt	Set, when IntL pin is asserted low		
	0	DataNotReady	Set while memory data is not ready		
3	7	L-Rx15 LOS	Latched Rx LOS indicator, channel 15	RO	Optional
	6	L-Rx14 LOS	Latched Rx LOS indicator, channel 14		
	5	L-Rx13 LOS	Latched Rx LOS indicator, channel 13		
	4	L-Rx12 LOS	Latched Rx LOS indicator, channel 12		
	3	L-Rx11 LOS	Latched Rx LOS indicator, channel 11		
	2	L-Rx10 LOS	Latched Rx LOS indicator, channel 10		
	1	L-Rx9 LOS	Latched Rx LOS indicator, channel 9		
	0	L-Rx8 LOS	Latched Rx LOS indicator, channel 8		
4	7	L-Rx7 LOS	Latched Rx LOS indicator, channel 7		
	6	L-Rx6 LOS	Latched Rx LOS indicator, channel 6		
	5	L-Rx5 LOS	Latched Rx LOS indicator, channel 5		
	4	L-Rx4 LOS	Latched Rx LOS indicator, channel 4		
	3	L-Rx3 LOS	Latched Rx LOS indicator, channel 3		
	2	L-Rx2 LOS	Latched Rx LOS indicator, channel 2		
	1	L-Rx1 LOS	Latched Rx LOS indicator, channel 1		
	0	L-Rx0 LOS	Latched Rx LOS indicator, channel 0		
5	7	L-Rx15 CDR LOL	Latched Rx CDR LOL indicator, channel 15	RO	Optional
	6	L-Rx14 CDR LOL	Latched Rx CDR LOL indicator, channel 14		
	5	L-Rx13 CDR LOL	Latched Rx CDR LOL indicator, channel 13		
	4	L-Rx12 CDR LOL	Latched Rx CDR LOL indicator, channel 12		
	3	L-Rx11 CDR LOL	Latched Rx CDR LOL indicator, channel 11		
	2	L-Rx10 CDR LOL	Latched Rx CDR LOL indicator, channel 10		
	1	L-Rx9 CDR LOL	Latched Rx CDR LOL indicator, channel 9		
	0	L-Rx8 CDR LOL	Latched Rx CDR LOL indicator, channel 8		
6	7	L-Rx7 CDR LOL	Latched Rx CDR LOL indicator, channel 7		
	6	L-Rx6 CDR LOL	Latched Rx CDR LOL indicator, channel 6		
	5	L-Rx5 CDR LOL	Latched Rx CDR LOL indicator, channel 5		
	4	L-Rx4 CDR LOL	Latched Rx CDR LOL indicator, channel 4		
	3	L-Rx3 CDR LOL	Latched Rx CDR LOL indicator, channel 3		
	2	L-Rx2 CDR LOL	Latched Rx CDR LOL indicator, channel 2		
	1	L-Rx1 CDR LOL	Latched Rx CDR LOL indicator, channel 1		
	0	L-Rx0 CDR LOL	Latched Rx CDR LOL indicator, channel 0		
7	All	Reserved		RO	
8	All	Reserved		RO	
9	All	Reserved		RO	
10	All	Reserved		RO	

Byte	Bit	Name	Description	Type	Option
11	7	L-Rx15 LPW	Latched Rx Low Power Warning, channel 15	RO	Optional
	6	L-Rx14 LPW	Latched Rx Low Power Warning, channel 14		
	5	L-Rx13 LPW	Latched Rx Low Power Warning, channel 13		
	4	L-Rx12 LPW	Latched Rx Low Power Warning, channel 12		
	3	L-Rx11 LPW	Latched Rx Low Power Warning, channel 11		
	2	L-Rx10 LPW	Latched Rx Low Power Warning, channel 10		
	1	L-Rx9 LPW	Latched Rx Low Power Warning, channel 9		
	0	L-Rx8 LPW	Latched Rx Low Power Warning, channel 8		
12	7	L-Rx7 LPW	Latched Rx Low Power Warning, channel 7		
	6	L-Rx6 LPW	Latched Rx Low Power Warning, channel 6		
	5	L-Rx5 LPW	Latched Rx Low Power Warning, channel 4		
	4	L-Rx4 LPW	Latched Rx Low Power Warning, channel 4		
	3	L-Rx3 LPW	Latched Rx Low Power Warning, channel 3		
	2	L-Rx2 LPW	Latched Rx Low Power Warning, channel 2		
	1	L-Rx1 LPW	Latched Rx Low Power Warning, channel 1		
	0	L-Rx0 LPW	Latched Rx Low Power Warning, channel 0		
13	7	L-Rx15 HPA	Latched Rx High Power Alarm, channel 15	RO	Optional
	6	L-Rx14 HPA	Latched Rx High Power Alarm, channel 14		
	5	L-Rx13 HPA	Latched Rx High Power Alarm, channel 13		
	4	L-Rx12 HPA	Latched Rx High Power Alarm, channel 12		
	3	L-Rx11 HPA	Latched Rx High Power Alarm, channel 11		
	2	L-Rx10 HPA	Latched Rx High Power Alarm, channel 10		
	1	L-Rx9 HPA	Latched Rx High Power Alarm, channel 9		
	0	L-Rx8 HPA	Latched Rx High Power Alarm, channel 8		
14	7	L-Rx7 HPA	Latched Rx High Power Alarm, channel 7		
	6	L-Rx6 HPA	Latched Rx High Power Alarm, channel 6		
	5	L-Rx5 HPA	Latched Rx High Power Alarm, channel 5		
	4	L-Rx4 HPA	Latched Rx High Power Alarm, channel 4		
	3	L-Rx3 HPA	Latched Rx High Power Alarm, channel 3		
	2	L-Rx2 HPA	Latched Rx High Power Alarm, channel 2		
	1	L-Rx1 HPA	Latched Rx High Power Alarm, channel 1		
	0	L-Rx0 HPA	Latched Rx High Power Alarm, channel 0		
15	7	L-Rx15 LPA	Latched Rx Low Power Alarm, channel 15	RO	Optional
	6	L-Rx14 LPA	Latched Rx Low Power Alarm, channel 14		
	5	L-Rx13 LPA	Latched Rx Low Power Alarm, channel 13		
	4	L-Rx12 LPA	Latched Rx Low Power Alarm, channel 12		
	3	L-Rx11 LPA	Latched Rx Low Power Alarm, channel 11		
	2	L-Rx10 LPA	Latched Rx Low Power Alarm, channel 10		
	1	L-Rx9 LPA	Latched Rx Low Power Alarm, channel 9		
	0	L-Rx8 LPA	Latched Rx Low Power Alarm, channel 8		
16	7	L-Rx7 LPA	Latched Rx Low Power Alarm, channel 7		
	6	L-Rx6 LPA	Latched Rx Low Power Alarm, channel 6		
	5	L-Rx5 LPA	Latched Rx Low Power Alarm, channel 5		
	4	L-Rx4 LPA	Latched Rx Low Power Alarm, channel 4		
	3	L-Rx3 LPA	Latched Rx Low Power Alarm, channel 3		
	2	L-Rx2 LPA	Latched Rx Low Power Alarm, channel 2		
	1	L-Rx1 LPA	Latched Rx Low Power Alarm, channel 1		
	0	L-Rx0 LPA	Latched Rx Low Power Alarm, channel 0		
17	7	L-Temp High Alarm	Latched High 1st Temperature Alarm	RO	Optional
	6	L-Temp Low Alarm	Latched Low 1st Temperature Alarm		
	5	L-Temp High Warning	Latched High 1st Temperature Warning		
	4	L-Temp Low Warning	Latched Low 1st Temperature Warning		
	3	L-Temp 2 High Alarm	Latched High 2nd Temperature Alarm		

Byte	Bit	Name	Description	Type	Option
	2	L-Temp 2 Low Alarm	Latched Low 2nd Temperature 2 Alarm		
	1	L-Temp 2 High Warning	Latched High 2nd Temperature Warning		
	0	L-Temp 2 Low Warning	Latched Low 2nd Temperature Warning		
18	7	L-Vcc 3.3V High Alarm	Latched 3.3V Supply High Alarm	RO	Optional
	6	L-Vcc 3.3V Low Alarm	Latched 3.3V Supply Low Alarm		
	5	L-Vcc 3.3V High Warning	Latched 3.3V Supply High Warning		
	4	L-Vcc 3.3V Low Warning	Latched 3.3V Supply Low Warning		
	3-0	Reserved			
19	7	Raw Rx15 LOS State	Unlatched Rx LOS indicator, channel 15	RO	Optional
	6	Raw Rx14 LOS State	Unlatched Rx LOS indicator, channel 14		
	5	Raw Rx13 LOS State	Unlatched Rx LOS indicator, channel 13		
	4	Raw Rx12 LOS State	Unlatched Rx LOS indicator, channel 12		
	3	Raw Rx11 LOS State	Unlatched Rx LOS indicator, channel 11		
	2	Raw Rx10 LOS State	Unlatched Rx LOS indicator, channel 10		
	1	Raw Rx9 LOS State	Unlatched Rx LOS indicator, channel 9		
	0	Raw Rx8 LOS State	Unlatched Rx LOS indicator, channel 8		
20	7	Raw Rx7 LOS State	Unlatched Rx LOS indicator, channel 7		
	6	Raw Rx6 LOS State	Unlatched Rx LOS indicator, channel 6		
	5	Raw Rx5 LOS State	Unlatched Rx LOS indicator, channel 5		
	4	Raw Rx4 LOS State	Unlatched Rx LOS indicator, channel 4		
	3	Raw Rx3 LOS State	Unlatched Rx LOS indicator, channel 3		
	2	Raw Rx2 LOS State	Unlatched Rx LOS indicator, channel 2		
	1	Raw Rx1 LOS State	Unlatched Rx LOS indicator, channel 1		
	0	Raw Rx0 LOS State	Unlatched Rx LOS indicator, channel 0		
21	7	Raw Rx15 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 15	RO	Optional
	6	Raw Rx14 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 14		
	5	Raw Rx13 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 13		
	4	Raw Rx12 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 12		
	3	Raw Rx11 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 11		
	2	Raw Rx10 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 10		
	1	Raw Rx9 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 9		
	0	Raw Rx8 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 8		
22	7	Raw Rx7 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 7		
	6	Raw Rx6 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 6		

Byte	Bit	Name	Description	Type	Option
	5	Raw Rx5 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 5		
	4	Raw Rx4 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 4		
	3	Raw Rx3 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 3		
	2	Raw Rx2 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 2		
	1	Raw Rx1 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 1		
	0	Raw Rx0 CDR LOL State	Unlatched Rx CDR LOL indicator, channel 0		
23	All	Reserved		RO	
24	All	Reserved		RO	
25	All	Temperature 1	1st internally measured temperature [1 °C]	RO	Optional
26	All	Temperature 2	2nd internally measured temperature [1 °C]	RO	Optional
27	All	Vcc 3.3V MSB	Internally measured supply voltage	RO	Optional
28	All	Vcc 3.3V LSB	3.3V [100 µV]		
29	All	Icc MSB	Internally measured supply current [1 mA]	RO	Optional
30	All	Icc LSB			
31	All	TiO MSB	Elapsed Time in Operation [2 h]	RO	Optional
32	All	TiO LSB			
33	All	Rx0 Optical Power	Rx Light Input Monitor, channel 0 [20 µW]	RO	Optional
34	All	Rx1 Optical Power	Rx Light Input Monitor, channel 1 [20 µW]		
35	All	Rx2 Optical Power	Rx Light Input Monitor, channel 2 [20 µW]		
36	All	Rx3 Optical Power	Rx Light Input Monitor, channel 3 [20 µW]		
37	All	Rx4 Optical Power	Rx Light Input Monitor, channel 4 [20 µW]		
38	All	Rx5 Optical Power	Rx Light Input Monitor, channel 5 [20 µW]		
39	All	Rx6 Optical Power	Rx Light Input Monitor, channel 6 [20 µW]		
40	All	Rx7 Optical Power	Rx Light Input Monitor, channel 7 [20 µW]		
41	All	Rx8 Optical Power	Rx Light Input Monitor, channel 8 [20 µW]		
42	All	Rx9 Optical Power	Rx Light Input Monitor, channel 9 [20 µW]		
43	All	Rx10 Optical Power	Rx Light Input Monitor, channel 10 [20 µW]		
44	All	Rx11 Optical Power	Rx Light Input Monitor, channel 11 [20 µW]		
45	All	Rx12 Optical Power	Rx Light Input Monitor, channel 12 [20 µW]		
46	All	Rx13Optical Power	Rx Light Input Monitor, channel 13 [20 µW]		
47	All	Rx14 Optical Power	Rx Light Input Monitor, channel 14 [20 µW]		
48	All	Rx15 Optical Power	Rx Light Input Monitor, channel 15 [20 µW]		
49-64	All	Reserved	Reserved Channel Monitor	RO	
65	7	Rx15 Disable	Rx Output Disable, channel 15	RW	Optional
	6	Rx14 Disable	Rx Output Disable, channel 14		
	5	Rx13 Disable	Rx Output Disable, channel 13		
	4	Rx12 Disable	Rx Output Disable, channel 12		
	3	Rx11 Disable	Rx Output Disable, channel 11		
	2	Rx10 Disable	Rx Output Disable, channel 10		
	1	Rx9 Disable	Rx Output Disable, channel 9		
	0	Rx8 Disable	Rx Output Disable, channel 8		
66	7	Rx7 Disable	Rx Output Disable, channel 7		
	6	Rx6 Disable	Rx Output Disable, channel 6		
	5	Rx5 Disable	Rx Output Disable, channel 5		

Byte	Bit	Name	Description	Type	Option
	4	Rx4 Disable	Rx Output Disable, channel 4		
	3	Rx3 Disable	Rx Output Disable, channel 3		
	2	Rx2 Disable	Rx Output Disable, channel 2		
	1	Rx1 Disable	Rx Output Disable, channel 1		
	0	Rx0 Disable	Rx Output Disable, channel 0		
67	7	Rx15 Squelch Disable	Rx Squelch Disable, channel 15	RW	Optional
	6	Rx14 Squelch Disable	Rx Squelch Disable, channel 14		
	5	Rx13 Squelch Disable	Rx Squelch Disable, channel 13		
	4	Rx12 Squelch Disable	Rx Squelch Disable, channel 12		
	3	Rx11 Squelch Disable	Rx Squelch Disable, channel 11		
	2	Rx10 Squelch Disable	Rx Squelch Disable, channel 10		
	1	Rx9 Squelch Disable	Rx Squelch Disable, channel 9		
	0	Rx8 Squelch Disable	Rx Squelch Disable, channel 8		
68	7	Rx7 Squelch Disable	Rx Squelch Disable, channel 7		
	6	Rx6 Squelch Disable	Rx Squelch Disable, channel 6		
	5	Rx5 Squelch Disable	Rx Squelch Disable, channel 5		
	4	Rx4 Squelch Disable	Rx Squelch Disable, channel 4		
	3	Rx3 Squelch Disable	Rx Squelch Disable, channel 3		
	2	Rx2 Squelch Disable	Rx Squelch Disable, channel 2		
	1	Rx1 Squelch Disable	Rx Squelch Disable, channel 1		
	0	Rx0 Squelch Disable	Rx Squelch Disable, channel 0		
69	7	Rx15 Polarity Flip	Rx Polarity Flip, channel 15	RW	Optional
	6	Rx14 Polarity Flip	Rx Polarity Flip, channel 14		
	5	Rx13 Polarity Flip	Rx Polarity Flip, channel 13		
	4	Rx12 Polarity Flip	Rx Polarity Flip, channel 12		
	3	Rx11 Polarity Flip	Rx Polarity Flip, channel 11		
	2	Rx10 Polarity Flip	Rx Polarity Flip, channel 10		
	1	Rx9 Polarity Flip	Rx Polarity Flip, channel 9		
	0	Rx8 Polarity Flip	Rx Polarity Flip, channel 8		
70	7	Rx7 Polarity Flip	Rx Polarity Flip, channel 7		
	6	Rx6 Polarity Flip	Rx Polarity Flip, channel 6		
	5	Rx5 Polarity Flip	Rx Polarity Flip, channel 5		
	4	Rx4 Polarity Flip	Rx Polarity Flip, channel 4		
	3	Rx3 Polarity Flip	Rx Polarity Flip, channel 3		
	2	Rx2 Polarity Flip	Rx Polarity Flip, channel 2		

Byte	Bit	Name	Description	Type	Option
	1	Rx1 Polarity Flip	Rx Polarity Flip, channel 1		
	0	Rx0 Polarity Flip	Rx Polarity Flip, channel 0		
71	7	Rx15 CDR Bypass	Rx CDR Bypass, channel 15	RW	Optional
	6	Rx14 CDR Bypass	Rx CDR Bypass, channel 14		
	5	Rx13 CDR Bypass	Rx CDR Bypass, channel 13		
	4	Rx12 CDR Bypass	Rx CDR Bypass, channel 12		
	3	Rx11 CDR Bypass	Rx CDR Bypass, channel 11		
	2	Rx10 CDR Bypass	Rx CDR Bypass, channel 10		
	1	Rx9 CDR Bypass	Rx CDR Bypass, channel 9		
	0	Rx8 CDR Bypass	Rx CDR Bypass, channel 8		
72	7	Rx7 CDR Bypass	Rx CDR Bypass, channel 7		
	6	Rx6 CDR Bypass	Rx CDR Bypass, channel 6		
	5	Rx5 CDR Bypass	Rx CDR Bypass, channel 5		
	4	Rx4 CDR Bypass	Rx CDR Bypass, channel 4		
	3	Rx3 CDR Bypass	Rx CDR Bypass, channel 3		
	2	Rx2 CDR Bypass	Rx CDR Bypass, channel 2		
	1	Rx1 CDR Bypass	Rx CDR Bypass, channel 1		
	0	Rx0 CDR Bypass	Rx CDR Bypass, channel 0		
73	7-4	Rx1 OA	Rx Output Amplitude, channel 1	RW	Optional
	3-0	Rx0 OA	Rx Output Amplitude, channel 0		
74	7-4	Rx3 OA	Rx Output Amplitude, channel 3		
	3-0	Rx2 OA	Rx Output Amplitude, channel 2		
75	7-4	Rx5 OA	Rx Output Amplitude, channel 5		
	3-0	Rx4 OA	Rx Output Amplitude, channel 4		
76	7-4	Rx7 OA	Rx Output Amplitude, channel 7		
	3-0	Rx6 OA	Rx Output Amplitude, channel 6		
77	7-4	Rx9 OA	Rx Output Amplitude, channel 9		
	3-0	Rx8 OA	Rx Output Amplitude, channel 8		
78	7-4	Rx11 OA	Rx Output Amplitude, channel 11		
	3-0	Rx10 OA	Rx Output Amplitude, channel 10		
79	7-4	Rx13 OA	Rx Output Amplitude, channel 13		
	3-0	Rx12 OA	Rx Output Amplitude, channel 12		
80	7-4	Rx15 OA	Rx Output Amplitude, channel 15		
	3-0	Rx14 OA	Rx Output Amplitude, channel 14		
81	7-4	Rx1 PE	Rx Pre-Emphasis, channel 1	RW	Optional
	3-0	Rx0 PE	Rx Pre-Emphasis, channel 0		
82	7-4	Rx3 PE	Rx Pre-Emphasis, channel 3		
	3-0	Rx2 PE	Rx Pre-Emphasis, channel 2		
83	7-4	Rx5 PE	Rx Pre-Emphasis, channel 5		
	3-0	Rx4 PE	Rx Pre-Emphasis, channel 4		
84	7-4	Rx7 PE	Rx Pre-Emphasis, channel 7		
	3-0	Rx6 PE	Rx Pre-Emphasis, channel 6		
85	7-4	Rx9 PE	Rx Pre-Emphasis, channel 9		
	3-0	Rx8 PE	Rx Pre-Emphasis, channel 8		
86	7-4	Rx11 PE	Rx Pre-Emphasis, channel 11		
	3-0	Rx10 PE	Rx Pre-Emphasis, channel 10		
87	7-4	Rx13 PE	Rx Pre-Emphasis, channel 13		
	3-0	Rx12 PE	Rx Pre-Emphasis, channel 12		
88	7-4	Rx15 PE	Rx Pre-Emphasis, channel 15		
	3-0	Rx14 PE	Rx Pre-Emphasis, channel 14		
89	7-4	Rx1 PE	Rx Rate Select, channel 1	RW	Optional
	3-0	Rx0 PE	Rx Rate Select, channel 0		
90	7-4	Rx3 PE	Rx Rate Select, channel 3		
	3-0	Rx2 PE	Rx Rate Select, channel 2		
91	7-4	Rx5 PE	Rx Rate Select, channel 5		
	3-0	Rx4 PE	Rx Rate Select, channel 4		

Byte	Bit	Name	Description	Type	Option
92	7-4	Rx7 PE	Rx Rate Select, channel 7		
	3-0	Rx6 PE	Rx Rate Select, channel 6		
93	7-4	Rx9 PE	Rx Rate Select, channel 9		
	3-0	Rx8 PE	Rx Rate Select, channel 8		
94	7-4	Rx11 PE	Rx Rate Select, channel 11		
	3-0	Rx10 PE	Rx Rate Select, channel 10		
95	7-4	Rx13 PE	Rx Rate Select, channel 13		
	3-0	Rx12 PE	Rx Rate Select, channel 12		
96	7-4	Rx15 PE	Rx Rate Select, channel 15		
	3-0	Rx14 PE	Rx Rate Select, channel 14		
97	7	Reserved		RW	Optional
	6	Rx LOS Disable	Rx LOS SIF disable		
	5	Rx CDR LOL Disable	Rx CDR LOL SIF disable		
	4	Reserved			
	3	Reserved			
	2	Rx Power A/W Disable	Rx Power Alarm/Warning SIF disable		
	1	Rx Temp A/W Disable	Rx Temperature Alarm/Warning SIF disable		
	0	Rx Vcc A/W Disable	Rx Vcc Alarm/Warning SIF disable		
98	7	Rx15 Channel Fault Squelch	Disable all FAWS reports from Rx channel 15	RW	Optional
	6	Rx14 Channel Fault Squelch	Disable all FAWS reports from Rx channel 14		
	5	Rx13 Channel Fault Squelch	Disable all FAWS reports from Rx channel 13		
	4	Rx12 Channel Fault Squelch	Disable all FAWS reports from Rx channel 12		
	3	Rx11 Channel Fault Squelch	Disable all FAWS reports from Rx channel 11		
	2	Rx10 Channel Fault Squelch	Disable all FAWS reports from Rx channel 10		
	1	Rx9 Channel Fault Squelch	Disable all FAWS reports from Rx channel 9		
	0	Rx8 Channel Fault Squelch	Disable all FAWS reports from Rx channel 8		
99	7	Rx7 Channel Fault Squelch	Disable all FAWS reports from Rx channel 7		
	6	Rx6 Channel Fault Squelch	Disable all FAWS reports from Rx channel 6		
	5	Rx5 Channel Fault Squelch	Disable all FAWS reports from Rx channel 5		
	4	Rx4 Channel Fault Squelch	Disable all FAWS reports from Rx channel 4		
	3	Rx3 Channel Fault Squelch	Disable all FAWS reports from Rx channel 3		
	2	Rx2 Channel Fault Squelch	Disable all FAWS reports from Rx channel 2		
	1	Rx1 Channel Fault Squelch	Disable all FAWS reports from Rx channel 1		
	0	Rx0 Channel Fault Squelch	Disable all FAWS reports from Rx channel 0		
100	7-3	Reserved		RW	Optional
	2	Rx Power Override			
	1	Rx Power Down			

Byte	Bit	Name	Description	Type	Option
	0	Soft Reset			
101	All	Reserved		RW	Optional
102	7	M-Rx15 LOS	Mask Rx LOS indicator, channel 15	RW	Optional
	6	M-Rx14 LOS	Mask Rx LOS indicator, channel 14		
	5	M-Rx13 LOS	Mask Rx LOS indicator, channel 13		
	4	M-Rx12 LOS	Mask Rx LOS indicator, channel 12		
	3	M-Rx11 LOS	Mask Rx LOS indicator, channel 11		
	2	M-Rx10 LOS	Mask Rx LOS indicator, channel 10		
	1	M-Rx9 LOS	Mask Rx LOS indicator, channel 9		
	0	M-Rx8 LOS	Mask Rx LOS indicator, channel 8		
103	7	M-Rx7 LOS	Mask Rx LOS indicator, channel 7		
	6	M-Rx6 LOS	Mask Rx LOS indicator, channel 6		
	5	M-Rx5 LOS	Mask Rx LOS indicator, channel 5		
	4	M-Rx4 LOS	Mask Rx LOS indicator, channel 4		
	3	M-Rx3 LOS	Mask Rx LOS indicator, channel 3		
	2	M-Rx2 LOS	Mask Rx LOS indicator, channel 2		
	1	M-Rx1 LOS	Mask Rx LOS indicator, channel 1		
	0	M-Rx0 LOS	Mask Rx LOS indicator, channel 0		
104	7	M-Rx15 CDR LOL	Mask Rx CDR LOL indicator, channel 15	RW	Optional
	6	M-Rx14 CDR LOL	Mask Rx CDR LOL indicator, channel 14		
	5	M-Rx13 CDR LOL	Mask Rx CDR LOL indicator, channel 13		
	4	M-Rx12 CDR LOL	Mask Rx CDR LOL indicator, channel 12		
	3	M-Rx11 CDR LOL	Mask Rx CDR LOL indicator, channel 11		
	2	M-Rx10 CDR LOL	Mask Rx CDR LOL indicator, channel 10		
	1	M-Rx9 CDR LOL	Mask Rx CDR LOL indicator, channel 9		
	0	M-Rx8 CDR LOL	Mask Rx CDR LOL indicator, channel 8		
105	7	M-Rx7 CDR LOL	Mask Rx CDR LOL indicator, channel 7		
	6	M-Rx6 CDR LOL	Mask Rx CDR LOL indicator, channel 6		
	5	M-Rx5 CDR LOL	Mask Rx CDR LOL indicator, channel 5		
	4	M-Rx4 CDR LOL	Mask Rx CDR LOL indicator, channel 4		
	3	M-Rx3 CDR LOL	Mask Rx CDR LOL indicator, channel 3		
	2	M-Rx2 CDR LOL	Mask Rx CDR LOL indicator, channel 2		
	1	M-Rx1 CDR LOL	Mask Rx CDR LOL indicator, channel 1		
	0	M-Rx0 CDR LOL	Mask Rx CDR LOL indicator, channel 0		
106	All	Reserved		RW	
107	All	Reserved		RW	
108	All	Reserved		RW	Optional
109	All	Reserved		RW	Optional
110	7	M-Rx15 LPW	Mask Rx Low Power Warning, channel 15	RW	Optional
	6	M-Rx14 LPW	Mask Rx Low Power Warning, channel 14		
	5	M-Rx13 LPW	Mask Rx Low Power Warning, channel 13		
	4	M-Rx12 LPW	Mask Rx Low Power Warning, channel 12		
	3	M-Rx11 LPW	Mask Rx Low Power Warning, channel 11		
	2	M-Rx10 LPW	Mask Rx Low Power Warning, channel 10		
	1	M-Rx9 LPW	Mask Rx Low Power Warning, channel 9		
	0	M-Rx8 LPW	Mask Rx Low Power Warning, channel 8		
111	7	M-Rx7 LPW	Mask Rx Low Power Warning, channel 7		
	6	M-Rx6 LPW	Mask Rx Low Power Warning, channel 6		
	5	M-Rx5 LPW	Mask Rx Low Power Warning, channel 4		
	4	M-Rx4 LPW	Mask Rx Low Power Warning, channel 4		
	3	M-Rx3 LPW	Mask Rx Low Power Warning, channel 3		
	2	M-Rx2 LPW	Mask Rx Low Power Warning, channel 2		
	1	M-Rx1 LPW	Mask Rx Low Power Warning, channel 1		
	0	M-Rx0 LPW	Mask Rx Low Power Warning, channel 0		
112	7	M-Rx15 LPA	Mask Rx Low Power Alarm, channel 15	RW	Optional
	6	M-Rx14 LPA	Mask Rx Low Power Alarm, channel 14		

Byte	Bit	Name	Description	Type	Option
	5	M-Rx13 LPA	Mask Rx Low Power Alarm, channel 13		
	4	M-Rx12 LPA	Mask Rx Low Power Alarm, channel 12		
	3	M-Rx11 LPA	Mask Rx Low Power Alarm, channel 11		
	2	M-Rx10 LPA	Mask Rx Low Power Alarm, channel 10		
	1	M-Rx9 LPA	Mask Rx Low Power Alarm, channel 9		
	0	M-Rx8 LPA	Mask Rx Low Power Alarm, channel 8		
113	7	M-Rx7 LPA	Mask Rx Low Power Alarm, channel 7		
	6	M-Rx6 LPA	Mask Rx Low Power Alarm, channel 6		
	5	M-Rx5 LPA	Mask Rx Low Power Alarm, channel 5		
	4	M-Rx4 LPA	Mask Rx Low Power Alarm, channel 4		
	3	M-Rx3 LPA	Mask Rx Low Power Alarm, channel 3		
	2	M-Rx2 LPA	Mask Rx Low Power Alarm, channel 2		
	1	M-Rx1 LPA	Mask Rx Low Power Alarm, channel 1		
	0	M-Rx0 LPA	Mask Rx Low Power Alarm, channel 0		
114	7	M-Rx15 HPA	Mask Rx High Power Alarm, channel 15	RW	Optional
	6	M-Rx14 HPA	Mask Rx High Power Alarm, channel 14		
	5	M-Rx13 HPA	Mask Rx High Power Alarm, channel 13		
	4	M-Rx12 HPA	Mask Rx High Power Alarm, channel 12		
	3	M-Rx11 HPA	Mask Rx High Power Alarm, channel 11		
	2	M-Rx10 HPA	Mask Rx High Power Alarm, channel 10		
	1	M-Rx9 HPA	Mask Rx High Power Alarm, channel 9		
	0	M-Rx8 HPA	Mask Rx High Power Alarm, channel 8		
115	7	M-Rx7 HPA	Mask Rx High Power Alarm, channel 7		
	6	M-Rx6 HPA	Mask Rx High Power Alarm, channel 6		
	5	M-Rx5 HPA	Mask Rx High Power Alarm, channel 5		
	4	M-Rx4 HPA	Mask Rx High Power Alarm, channel 4		
	3	M-Rx3 HPA	Mask Rx High Power Alarm, channel 3		
	2	M-Rx2 HPA	Mask Rx High Power Alarm, channel 2		
	1	M-Rx1 HPA	Mask Rx High Power Alarm, channel 1		
	0	M-Rx0 HPA	Mask Rx High Power Alarm, channel 0		
116	7	M-Temp High Alarm	Mask High 1st Temperature Alarm	RW	Optional
	6	M-Temp Low Alarm	Mask Low 1st Temperature Alarm		
	5	M-Temp High Warning	Mask High 1st Temperature Warning		
	4	M-Temp Low Warning	Mask Low 1st Temperature Warning		
	3	M-Temp 2 High Alarm	Mask High 2nd Temperature Alarm		
	2	M-Temp 2 Low Alarm	Mask Low 2nd Temperature 2 Alarm		
	1	M-Temp 2 High Warning	Mask High 2nd Temperature Warning		
	0	M-Temp 2 Low Warning	Mask Low 2nd Temperature Warning		
117	7	M-Vcc 3.3V High Alarm	Mask 3.3V Supply High Alarm	RW	Optional
	6	M-Vcc 3.3V Low Alarm	Mask 3.3V Supply Low Alarm		
	5	M-Vcc 3.3V High Warning	Mask 3.3V Supply High Warning		
	4	M-Vcc 3.3V Low Warning	Mask 3.3V Supply Low Warning		
	3-0	Reserved			
118	7	P-Non-Volatile	Persistence treated as non-volatile	RW	Optional
	6	P-Rx LOS Alarm	Persistent Rx LOS Alarm		
	5	P-Rx CDR LOL Alarm	Persistent Rx CDR LOL Alarm		

Byte	Bit	Name	Description	Type	Option
	4	Reserved			
	3	Reserved			
	2	P-Rx Power Alarm	Persistent Rx Power Alarm		
	1	P-Rx Temperature Alarm	Persistent Rx Temperature Alarm		
	0	P-Rx Vcc Alarm	Persistent Rx Vcc Alarm		
119	All	PWCE MSB	Password Change Entry Area	WO	Optional
120	All	PWCE			
121	All	PWCE			
122	All	PWCE LSB			
123	All	PWE MSB	Password Entry Area	WO	Required
124	All	PWE			
120	All	PWE			
126	All	PWE LSB			
127	All	PSB	Page Select byte	RW	Required

1

9.7 Lower Page Tx

Table 44: Lower Memory Page Tx

Byte	Bit	Name	Description	Type	Option
0	All	Identifier	Identifier - Type of Serial Module (same value as page 0 byte 128)	RO	Required
1	All	Version ID	Identifier - Version of Serial Module Specification	RO	Required
2	7	Flat_mem	Upper memory flat or paged. 0= paged, 1= Page 00h only	RO	Required
	6	Tx Bias and Power Alarm Summary	Set, when any bit in #11-16 is set		
	5	Reserved			
	4	Tx LOS, Fault and LOL Alarm Summary	Set, when any bit in #3-8 is set		
	3	Reserved			
	2	Temperature and Vcc Alarm Summary	Set, when any bit in #17-18 is set		
	1	Interrupt	Set, when IntL pin is asserted low		
	0	DataNotReady	Set while memory data is not ready		
3	7	L-Tx15 LOS	Latched Tx LOS indicator, channel 15	RO	Optional
	6	L-Tx14 LOS	Latched Tx LOS indicator, channel 14		
	5	L-Tx13 LOS	Latched Tx LOS indicator, channel 13		
	4	L-Tx12 LOS	Latched Tx LOS indicator, channel 12		
	3	L-Tx11 LOS	Latched Tx LOS indicator, channel 11		
	2	L-Tx10 LOS	Latched Tx LOS indicator, channel 10		
	1	L-Tx9 LOS	Latched Tx LOS indicator, channel 9		
	0	L-Tx8 LOS	Latched Tx LOS indicator, channel 8		
4	7	L-Tx7 LOS	Latched Tx LOS indicator, channel 7		
	6	L-Tx6 LOS	Latched Tx LOS indicator, channel 6		
	5	L-Tx5 LOS	Latched Tx LOS indicator, channel 5		
	4	L-Tx4 LOS	Latched Tx LOS indicator, channel 4		
	3	L-Tx3 LOS	Latched Tx LOS indicator, channel 3		
	2	L-Tx2 LOS	Latched Tx LOS indicator, channel 2		
	1	L-Tx1 LOS	Latched Tx LOS indicator, channel 1		
	0	L-Tx0 LOS	Latched Tx LOS indicator, channel 0		
5	7	L-Tx15 CDR LOL	Latched Tx CDR LOL indicator, channel 15	RO	Optional
	6	L-Tx14 CDR LOL	Latched Tx CDR LOL indicator, channel 14		
	5	L-Tx13 CDR LOL	Latched Tx CDR LOL indicator, channel 13		
	4	L-Tx12 CDR LOL	Latched Tx CDR LOL indicator, channel 12		
	3	L-Tx11 CDR LOL	Latched Tx CDR LOL indicator, channel 11		
	2	L-Tx10 CDR LOL	Latched Tx CDR LOL indicator, channel 10		
	1	L-Tx9 CDR LOL	Latched Tx CDR LOL indicator, channel 9		
	0	L-Tx8 CDR LOL	Latched Tx CDR LOL indicator, channel 8		
6	7	L-Tx7 CDR LOL	Latched Tx CDR LOL indicator, channel 7		
	6	L-Tx6 CDR LOL	Latched Tx CDR LOL indicator, channel 6		
	5	L-Tx5 CDR LOL	Latched Tx CDR LOL indicator, channel 5		
	4	L-Tx4 CDR LOL	Latched Tx CDR LOL indicator, channel 4		
	3	L-Tx3 CDR LOL	Latched Tx CDR LOL indicator, channel 3		
	2	L-Tx2 CDR LOL	Latched Tx CDR LOL indicator, channel 2		
	1	L-Tx1 CDR LOL	Latched Tx CDR LOL indicator, channel 1		
	0	L-Tx0 CDR LOL	Latched Tx CDR LOL indicator, channel 0		
7	7	L-Tx15 Fault	Latched Tx Fault indicator, channel 15	RO	Optional
	6	L-Tx14 Fault	Latched Tx Fault indicator, channel 14		
	5	L-Tx13 Fault	Latched Tx Fault indicator, channel 13		
	4	L-Tx12 Fault	Latched Tx Fault indicator, channel 12		
	3	L-Tx11 Fault	Latched Tx Fault indicator, channel 11		

	2	L-Tx10 Fault	Latched Tx Fault indicator, channel 10		
	1	L-Tx9 Fault	Latched Tx Fault indicator, channel 9		
	0	L-Tx8 Fault	Latched Tx Fault indicator, channel 8		
8	7	L-Tx7 Fault	Latched Tx Fault indicator, channel 7		
	6	L-Tx6 Fault	Latched Tx Fault indicator, channel 6		
	5	L-Tx5 Fault	Latched Tx Fault indicator, channel 5		
	4	L-Tx4 Fault	Latched Tx Fault indicator, channel 4		
	3	L-Tx3 Fault	Latched Tx Fault indicator, channel 3		
	2	L-Tx2 Fault	Latched Tx Fault indicator, channel 2		
	1	L-Tx1 Fault	Latched Tx Fault indicator, channel 1		
	0	L-Tx0 Fault	Latched Tx Fault indicator, channel 0		
9	7	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 15	RO	Optional
	6	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 14		
	5	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 13		
	4	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 12		
	3	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 11		
	2	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 10		
	1	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 9		
	0	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 8		
10	7	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 7		
	6	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 6		
	5	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 5		
	4	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 4		
	3	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 3		
	2	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 2		
	1	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 1		
	0	L-Tx15 HBA	Latched Tx High Bias Alarm, channel 0		
11	7	L-Tx15 LBA	Latched Tx Low Bias Alarm, channel 15	RO	Optional
	6	L-Tx14 LBA	Latched Tx Low Bias Alarm, channel 14		
	5	L-Tx13 LBA	Latched Tx Low Bias Alarm, channel 13		
	4	L-Tx12 LBA	Latched Tx Low Bias Alarm, channel 12		
	3	L-Tx11 LBA	Latched Tx Low Bias Alarm, channel 11		
	2	L-Tx10 LBA	Latched Tx Low Bias Alarm, channel 10		
	1	L-Tx9 LBA	Latched Tx Low Bias Alarm, channel 9		
	0	L-Tx8 LBA	Latched Tx Low Bias Alarm, channel 8		
12	7	L-Tx7 LBA	Latched Tx Low Bias Alarm, channel 7		
	6	L-Tx6 LBA	Latched Tx Low Bias Alarm, channel 6		
	5	L-Tx5 LBA	Latched Tx Low Bias Alarm, channel 4		
	4	L-Tx4 LBA	Latched Tx Low Bias Alarm, channel 4		
	3	L-Tx3 LBA	Latched Tx Low Bias Alarm, channel 3		
	2	L-Tx2 LBA	Latched Tx Low Bias Alarm, channel 2		
	1	L-Tx1 LBA	Latched Tx Low Bias Alarm, channel 1		
	0	L-Tx0 LBA	Latched Tx Low Bias Alarm, channel 0		
13	7	L-Tx15 HPA	Latched Tx High Power Alarm, channel 15	RO	Optional
	6	L-Tx14 HPA	Latched Tx High Power Alarm, channel 14		
	5	L-Tx13 HPA	Latched Tx High Power Alarm, channel 13		
	4	L-Tx12 HPA	Latched Tx High Power Alarm, channel 12		
	3	L-Tx11 HPA	Latched Tx High Power Alarm, channel 11		
	2	L-Tx10 HPA	Latched Tx High Power Alarm, channel 10		
	1	L-Tx9 HPA	Latched Tx High Power Alarm, channel 9		
	0	L-Tx8 HPA	Latched Tx High Power Alarm, channel 8		
14	7	L-Tx7 HPA	Latched Tx High Power Alarm, channel 7		
	6	L-Tx6 HPA	Latched Tx High Power Alarm, channel 6		
	5	L-Tx5 HPA	Latched Tx High Power Alarm, channel 5		
	4	L-Tx4 HPA	Latched Tx High Power Alarm, channel 4		
	3	L-Tx3 HPA	Latched Tx High Power Alarm, channel 3		
	2	L-Tx2 HPA	Latched Tx High Power Alarm, channel 2		

	1	L-Tx1 HPA	Latched Tx High Power Alarm, channel 1		
	0	L-Tx0 HPA	Latched Tx High Power Alarm, channel 0		
15	7	L-Tx15 LPA	Latched Tx Low Power Alarm, channel 15	RO	Optional
	6	L-Tx14 LPA	Latched Tx Low Power Alarm, channel 14		
	5	L-Tx13 LPA	Latched Tx Low Power Alarm, channel 13		
	4	L-Tx12 LPA	Latched Tx Low Power Alarm, channel 12		
	3	L-Tx11 LPA	Latched Tx Low Power Alarm, channel 11		
	2	L-Tx10 LPA	Latched Tx Low Power Alarm, channel 10		
	1	L-Tx9 LPA	Latched Tx Low Power Alarm, channel 9		
	0	L-Tx8 LPA	Latched Tx Low Power Alarm, channel 8		
16	7	L-Tx7 LPA	Latched Tx Low Power Alarm, channel 7		
	6	L-Tx6 LPA	Latched Tx Low Power Alarm, channel 6		
	5	L-Tx5 LPA	Latched Tx Low Power Alarm, channel 5		
	4	L-Tx4 LPA	Latched Tx Low Power Alarm, channel 4		
	3	L-Tx3 LPA	Latched Tx Low Power Alarm, channel 3		
	2	L-Tx2 LPA	Latched Tx Low Power Alarm, channel 2		
	1	L-Tx1 LPA	Latched Tx Low Power Alarm, channel 1		
	0	L-Tx0 LPA	Latched Tx Low Power Alarm, channel 0		
17	7	L-Temp High Alarm	Latched High 1st Temperature Alarm	RO	Optional
	6	L-Temp Low Alarm	Latched Low 1st Temperature Alarm		
	5	L-Temp High Warning	Latched High 1st Temperature Warning		
	4	L-Temp Low Warning	Latched Low 1st Temperature Warning		
	3	L-Temp 2 High Alarm	Latched High 2nd Temperature Alarm		
	2	L-Temp 2 Low Alarm	Latched Low 2nd Temperature 2 Alarm		
	1	L-Temp 2 High Warning	Latched High 2nd Temperature Warning		
	0	L-Temp 2 Low Warning	Latched Low 2nd Temperature Warning		
18	7	L-Vcc 3.3V High Alarm	Latched 3.3V Supply High Alarm	RO	Optional
	6	L-Vcc 3.3V Low Alarm	Latched 3.3V Supply Low Alarm		
	5	L-Vcc 3.3V High Warning	Latched 3.3V Supply High Warning		
	4	L-Vcc 3.3V Low Warning	Latched 3.3V Supply Low Warning		
	3-0	Reserved			
19	7	Raw Tx15 LOS State	Unlatched Tx LOS indicator, channel 15	RO	Optional
	6	Raw Tx14 LOS State	Unlatched Tx LOS indicator, channel 14		
	5	Raw Tx13 LOS State	Unlatched Tx LOS indicator, channel 13		
	4	Raw Tx12 LOS State	Unlatched Tx LOS indicator, channel 12		
	3	Raw Tx11 LOS State	Unlatched Tx LOS indicator, channel 11		
	2	Raw Tx10 LOS State	Unlatched Tx LOS indicator, channel 10		
	1	Raw Tx9 LOS State	Unlatched Tx LOS indicator, channel 9		
	0	Raw Tx8 LOS State	Unlatched Tx LOS indicator, channel 8		
20	7	Raw Tx7 LOS State	Unlatched Tx LOS indicator, channel 7		
	6	Raw Tx6 LOS State	Unlatched Tx LOS indicator, channel 6		
	5	Raw Tx5 LOS State	Unlatched Tx LOS indicator, channel 5		
	4	Raw Tx4 LOS State	Unlatched Tx LOS indicator, channel 4		
	3	Raw Tx3 LOS State	Unlatched Tx LOS indicator, channel 3		
	2	Raw Tx2 LOS State	Unlatched Tx LOS indicator, channel 2		
	1	Raw Tx1 LOS State	Unlatched Tx LOS indicator, channel 1		
	0	Raw Tx0 LOS State	Unlatched Tx LOS indicator, channel 0		
21	7	Raw Tx15 LOL State	Unlatched Tx CDR LOL indicator, channel 15	RO	Optional
	6	Raw Tx14 CDR LOL	Unlatched Tx CDR LOL indicator, channel 14		

		State			
	5	Raw Tx13 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 13		
	4	Raw Tx12 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 12		
	3	Raw Tx11 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 11		
	2	Raw Tx10 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 10		
	1	Raw Tx9 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 9		
	0	Raw Tx8 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 8		
22	7	Raw Tx7 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 7		
	6	Raw Tx6 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 6		
	5	Raw Tx5 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 5		
	4	Raw Tx4 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 4		
	3	Raw Tx3 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 3		
	2	Raw Tx2 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 2		
	1	Raw Tx1 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 1		
	0	Raw Tx0 CDR LOL State	Unlatched Tx CDR LOL indicator, channel 0		
23	7	Raw Tx15 Fault State	Unlatched Tx Fault indicator, channel 15	RO	Optional
	6	Raw Tx14 Fault State	Unlatched Tx Fault indicator, channel 14		
	5	Raw Tx13 Fault State	Unlatched Tx Fault indicator, channel 13		
	4	Raw Tx12 Fault State	Unlatched Tx Fault indicator, channel 12		
	3	Raw Tx11 Fault State	Unlatched Tx Fault indicator, channel 11		
	2	Raw Tx10 Fault State	Unlatched Tx Fault indicator, channel 10		
	1	Raw Tx9 Fault State	Unlatched Tx Fault indicator, channel 9		
	0	Raw Tx8 FaultState	Unlatched Tx Fault indicator, channel 8		
24	7	Raw Tx7 Fault State	Unlatched Tx Fault indicator, channel 7		
	6	Raw Tx6 Fault State	Unlatched Tx Fault indicator, channel 6		
	5	Raw Tx5 Fault State	Unlatched Tx Fault indicator, channel 5		
	4	Raw Tx4 Fault State	Unlatched Tx Fault indicator, channel 4		
	3	Raw Tx3 Fault State	Unlatched Tx Fault indicator, channel 3		
	2	Raw Tx2 Fault State	Unlatched Tx Fault indicator, channel 2		
	1	Raw Tx1 Fault State	Unlatched Tx Fault indicator, channel 1		

	0	Raw Tx0 Fault State	Unlatched Tx Fault indicator, channel 0		
25	All	Temperature 1	1st internally measured temperature [°C]	RW	Optional
26	All	Temperature 2	2nd internally measured temperature [°C]	RW	Optional
27	All	Vcc 3.3V MSB	Internally measured supply voltage 3.3V [100 µV]	RO	Optional
28	All	Vcc 3.3V LSB			
29	All	Icc MSB	Internally measured supply current [1 mA]	RO	Optional
30	All	Icc LSB			
31	All	TiO MSB	Elapsed Time in Operation [2 h]	RO	Optional
32	All	TiO LSB			
33	All	Tx0 Optical Power	Tx Light Output Monitor, channel 0 [20µW]	RO	Optional
34	All	Tx1 Optical Power	Tx Light Output Monitor, channel 1 [20µW]		
35	All	Tx2 Optical Power	Tx Light Output Monitor, channel 2 [20µW]		
36	All	Tx3 Optical Power	Tx Light Output Monitor, channel 3 [20µW]		
37	All	Tx4 Optical Power	Tx Light Output Monitor, channel 4 [20µW]		
38	All	Tx5 Optical Power	Tx Light Output Monitor, channel 5 [20µW]		
39	All	Tx6 Optical Power	Tx Light Output Monitor, channel 6 [20µW]		
40	All	Tx7 Optical Power	Tx Light Output Monitor, channel 7 [20µW]		
41	All	Tx8 Optical Power	Tx Light Output Monitor, channel 8 [20µW]		
42	All	Tx9 Optical Power	Tx Light Output Monitor, channel 9 [20µW]		
43	All	Tx10 Optical Power	Tx Light Output Monitor, channel 10 [20µW]		
44	All	Tx11 Optical Power	Tx Light Output Monitor, channel 11 [20µW]		
45	All	Tx12 Optical Power	Tx Light Output Monitor, channel 12 [20µW]		
46	All	Tx13Optical Power	Tx Light Output Monitor, channel 13 [20µW]		
47	All	Tx14 Optical Power	Tx Light Output Monitor, channel 14 [20µW]		
48	All	Tx15 Optical Power	Tx Light Output Monitor, channel 15 [20µW]		
49	All	Tx0 Bias Current	Tx Bias Current Monitor, channel 0 [0.1 mA]	RO	Optional
50	All	Tx1 Bias Current	Tx Bias Current Monitor, channel 1 [0.1 mA]		
51	All	Tx2 Bias Current	Tx Bias Current Monitor, channel 2 [0.1 mA]		
52	All	Tx3 Bias Current	Tx Bias Current Monitor, channel 3 [0.1 mA]		
53	All	Tx4 Bias Current	Tx Bias Current Monitor, channel 4 [0.1 mA]		
54	All	Tx5 Bias Current	Tx Bias Current Monitor, channel 5 [0.1 mA]		
55	All	Tx6 Bias Current	Tx Bias Current Monitor, channel 6 [0.1 mA]		
56	All	Tx7 Bias Current	Tx Bias Current Monitor, channel 7 [0.1 mA]		
57	All	Tx8 Bias Current	Tx Bias Current Monitor, channel 8 [0.1 mA]		
58	All	Tx9 Bias Current	Tx Bias Current Monitor, channel 9 [0.1 mA]		
59	All	Tx10 Bias Current	Tx Bias Current Monitor, channel 10 [0.1 mA]		
60	All	Tx11 Bias Current	Tx Bias Current Monitor, channel 11 [0.1 mA]		
61	All	Tx12 Bias Current	Tx Bias Current Monitor, channel 12 [0.1 mA]		
62	All	Tx13Bias Current	Tx Bias Current Monitor, channel 13 [0.1 mA]		
63	All	Tx14 Bias Current	Tx Bias Current Monitor, channel 14 [0.1 mA]		
64	All	Tx15 Bias Current	Tx Bias Current Monitor, channel 15 [0.1 mA]		
65	7	Tx15 Disable	Tx Output Disable, channel 15	RW	Optional
	6	Tx14 Disable	Tx Output Disable, channel 14		
	5	Tx13 Disable	Tx Output Disable, channel 13		
	4	Tx12 Disable	Tx Output Disable, channel 12		
	3	Tx11 Disable	Tx Output Disable, channel 11		
	2	Tx10 Disable	Tx Output Disable, channel 10		
	1	Tx9 Disable	Tx Output Disable, channel 9		

	0	Tx8 Disable	Tx Output Disable, channel 8		
66	7	Tx7 Disable	Tx Output Disable, channel 7		
	6	Tx6 Disable	Tx Output Disable, channel 6		
	5	Tx5 Disable	Tx Output Disable, channel 5		
	4	Tx4 Disable	Tx Output Disable, channel 4		
	3	Tx3 Disable	Tx Output Disable, channel 3		
	2	Tx2 Disable	Tx Output Disable, channel 2		
	1	Tx1 Disable	Tx Output Disable, channel 1		
	0	Tx0 Disable	Tx Output Disable, channel 0		
67	7	Tx15 Squelch Disable	Tx Squelch Disable, channel 15	RW	Optional
	6	Tx14 Squelch Disable	Tx Squelch Disable, channel 14		
	5	Tx13 Squelch Disable	Tx Squelch Disable, channel 13		
	4	Tx12 Squelch Disable	Tx Squelch Disable, channel 12		
	3	Tx11 Squelch Disable	Tx Squelch Disable, channel 11		
	2	Tx10 Squelch Disable	Tx Squelch Disable, channel 10		
	1	Tx9 Squelch Disable	Tx Squelch Disable, channel 9		
	0	Tx8 Squelch Disable	Tx Squelch Disable, channel 8		
68	7	Tx7 Squelch Disable	Tx Squelch Disable, channel 7		
	6	Tx6 Squelch Disable	Tx Squelch Disable, channel 6		
	5	Tx5 Squelch Disable	Tx Squelch Disable, channel 5		
	4	Tx4 Squelch Disable	Tx Squelch Disable, channel 4		
	3	Tx3 Squelch Disable	Tx Squelch Disable, channel 3		
	2	Tx2 Squelch Disable	Tx Squelch Disable, channel 2		
	1	Tx1 Squelch Disable	Tx Squelch Disable, channel 1		
	0	Tx0 Squelch Disable	Tx Squelch Disable, channel 0		
69	7	Tx15 Polarity Flip	Tx Polarity Flip, channel 15	RW	Optional
	6	Tx14 Polarity Flip	Tx Polarity Flip, channel 14		
	5	Tx13 Polarity Flip	Tx Polarity Flip, channel 13		
	4	Tx12 Polarity Flip	Tx Polarity Flip, channel 12		
	3	Tx11 Polarity Flip	Tx Polarity Flip, channel 11		
	2	Tx10 Polarity Flip	Tx Polarity Flip, channel 10		
	1	Tx9 Polarity Flip	Tx Polarity Flip, channel 9		
	0	Tx8 Polarity Flip	Tx Polarity Flip, channel 8		
70	7	Tx7 Polarity Flip	Tx Polarity Flip, channel 7		
	6	Tx6 Polarity Flip	Tx Polarity Flip, channel 6		
	5	Tx5 Polarity Flip	Tx Polarity Flip, channel 5		
	4	Tx4 Polarity Flip	Tx Polarity Flip, channel 4		
	3	Tx3 Polarity Flip	Tx Polarity Flip, channel 3		
	2	Tx2 Polarity Flip	Tx Polarity Flip, channel 2		
	1	Tx1 Polarity Flip	Tx Polarity Flip, channel 1		
	0	Tx0 Polarity Flip	Tx Polarity Flip, channel 0		

71	7	Tx15 CDR Bypass	Tx CDR Bypass, channel 15	RW	Optional
	6	Tx14 CDR Bypass	Tx CDR Bypass, channel 14		
	5	Tx13 CDR Bypass	Tx CDR Bypass, channel 13		
	4	Tx12 CDR Bypass	Tx CDR Bypass, channel 12		
	3	Tx11 CDR Bypass	Tx CDR Bypass, channel 11		
	2	Tx10 CDR Bypass	Tx CDR Bypass, channel 10		
	1	Tx9 CDR Bypass	Tx CDR Bypass, channel 9		
	0	Tx8 CDR Bypass	Tx CDR Bypass, channel 8		
72	7	Tx7 CDR Bypass	Tx CDR Bypass, channel 7		
	6	Tx6 CDR Bypass	Tx CDR Bypass, channel 6		
	5	Tx5 CDR Bypass	Tx CDR Bypass, channel 5		
	4	Tx4 CDR Bypass	Tx CDR Bypass, channel 4		
	3	Tx3 CDR Bypass	Tx CDR Bypass, channel 3		
	2	Tx2 CDR Bypass	Tx CDR Bypass, channel 2		
	1	Tx1 CDR Bypass	Tx CDR Bypass, channel 1		
	0	Tx0 CDR Bypass	Tx CDR Bypass, channel 0		
73	7	Tx15 CTLE Mode	Tx Equalization Mode, channel 15[1]	RW	Optional
	6	Tx14 CTLE Mode	Tx Equalization Mode, channel 14[1]		
	5	Tx13 CTLE Mode	Tx Equalization Mode, channel 13[1]		
	4	Tx12 CTLE Mode	Tx Equalization Mode, channel 12[1]		
	3	Tx11 CTLE Mode	Tx Equalization Mode, channel 11[1]		
	2	Tx10 CTLE Mode	Tx Equalization Mode, channel 10[1]		
	1	Tx9 CTLE Mode	Tx Equalization Mode, channel 9[1]		
	0	Tx8 CTLE Mode	Tx Equalization Mode, channel 8[1]		
74	7	Tx7 CTLE Mode	Tx Equalization Mode, channel 7[1]		
	6	Tx6 CTLE Mode	Tx Equalization Mode, channel 6[1]		
	5	Tx5 CTLE Mode	Tx Equalization Mode, channel 5[1]		
	4	Tx4 CTLE Mode	Tx Equalization Mode, channel 4[1]		
	3	Tx3 CTLE Mode	Tx Equalization Mode, channel 3[1]		
	2	Tx2 CTLE Mode	Tx Equalization Mode, channel 2[1]		
	1	Tx1 CTLE Mode	Tx Equalization Mode, channel 1[1]		
	0	Tx0 CTLE Mode	Tx Equalization Mode, channel 0[1]		
75	7	Tx15AEFreeze	Tx Adaptive Equalization Freeze, channel 15[2]		
	6	Tx14AE Freeze	Tx Adaptive Equalization Freeze, channel 14[2]		
	5	Tx13AE Freeze	Tx Adaptive Equalization Freeze, channel 13[2]		
	4	Tx12AE Freeze	Tx Adaptive Equalization Freeze, channel 12[2]		
	3	Tx11AE Freeze	Tx Adaptive Equalization Freeze, channel 11[2]		
	2	Tx10AE Freeze	Tx Adaptive Equalization Freeze, channel 10[2]		
	1	Tx9AE Freeze	Tx Adaptive Equalization Freeze, channel 9[2]		
	0	Tx8AE Freeze	Tx Adaptive Equalization Freeze, channel 8[2]		
76	7	Tx7 AE Freeze	Tx Adaptive Equalization Freeze, channel 7[2]		
	6	Tx6 AE Freeze	Tx Adaptive Equalization Freeze, channel 6[2]		
	5	Tx5 AE Freeze	Tx Adaptive Equalization Freeze, channel 5[2]		
	4	Tx4 AE Freeze	Tx Adaptive Equalization Freeze, channel 4[2]		
	3	Tx3 AE Freeze	Tx Adaptive Equalization Freeze, channel 3[2]		
	2	Tx2 AE Freeze	Tx Adaptive Equalization Freeze, channel 2[2]		
	1	Tx1 AE Freeze	Tx Adaptive Equalization Freeze, channel 1[2]		
	0	Tx0 AE Freeze	Tx Adaptive Equalization Freeze, channel 0[2]		
77		Reserved			
78		Reserved			
79		Reserved			

80		Reserved			
81	7-4	Tx1 EQ	Tx Equalization, channel 1		
81	3-0	Tx0 EQ	Tx Equalization, channel 0	RW	Optional
82	7-4	Tx3 EQ	Tx Equalization, channel 3		
82	3-0	Tx2 EQ	Tx Equalization, channel 2		
83	7-4	Tx5 EQ	Tx Equalization, channel 5		
83	3-0	Tx4 EQ	Tx Equalization, channel 4		
84	7-4	Tx7 EQ	Tx Equalization, channel 7		
84	3-0	Tx6 EQ	Tx Equalization, channel 6		
85	7-4	Tx9 EQ	Tx Equalization, channel 9		
85	3-0	Tx8 EQ	Tx Equalization, channel 8		
86	7-4	Tx11 EQ	Tx Equalization, channel 11		
86	3-0	Tx10 EQ	Tx Equalization, channel 10		
87	7-4	Tx13 EQ	Tx Equalization, channel 13		
87	3-0	Tx12 EQ	Tx Equalization, channel 12		
88	7-4	Tx15 EQ	Tx Equalization, channel 15		
88	3-0	Tx14 EQ	Tx Equalization, channel 14		
89	7-4	Tx1 PE	Tx Rate Select, channel 1		
89	3-0	Tx0 PE	Tx Rate Select, channel 0	RW	Optional
90	7-4	Tx3 PE	Tx Rate Select, channel 3		
90	3-0	Tx2 PE	Tx Rate Select, channel 2		
91	7-4	Tx5 PE	Tx Rate Select, channel 5		
91	3-0	Tx4 PE	Tx Rate Select, channel 4		
92	7-4	Tx7 PE	Tx Rate Select, channel 7		
92	3-0	Tx6 PE	Tx Rate Select, channel 6		
93	7-4	Tx9 PE	Tx Rate Select, channel 9		
93	3-0	Tx8 PE	Tx Rate Select, channel 8		
94	7-4	Tx11 PE	Tx Rate Select, channel 11		
94	3-0	Tx10 PE	Tx Rate Select, channel 10		
95	7-4	Tx13 PE	Tx Rate Select, channel 13		
95	3-0	Tx12 PE	Tx Rate Select, channel 12		
96	7-4	Tx15 PE	Tx Rate Select, channel 15		
96	3-0	Tx14 PE	Tx Rate Select, channel 14		
97	7	Reserved			
97	6	Tx LOS Disable	Tx LOS SIF disable	RW	Optional
	5	Tx CDR LOL Disable	Tx CDR LOL SIF disable		
	4	Tx Fault Disable	Tx Fault SIF disable		
	3	Reserved			
	2	Tx Power A/W Disable	Tx Power Alarm/Warning SIF disable		
	1	Tx Temp A/W Disable	Tx Temperature Alarm/Warning SIF disable		
	0	Tx Vcc A/W Disable	Tx Vcc Alarm/Warning SIF disable		
98	7	Tx15 Channel Fault Squelch	Disable all FAWS reports from Tx channel 15		
98	6	Tx14 Channel Fault Squelch	Disable all FAWS reports from Tx channel 14	RW	Optional
	5	Tx13 Channel Fault Squelch	Disable all FAWS reports from Tx channel 13		
	4	Tx12 Channel Fault Squelch	Disable all FAWS reports from Tx channel 12		
	3	Tx11 Channel Fault Squelch	Disable all FAWS reports from Tx channel 11		
	2	Tx10 Channel Fault Squelch	Disable all FAWS reports from Tx channel 10		
	1	Tx9 Channel Fault Squelch	Disable all FAWS reports from Tx channel 9		

	0	Tx8 Channel Fault Squelch	Disable all FAWS reports from Tx channel 8		
99	7	Tx7 Channel Fault Squelch	Disable all FAWS reports from Tx channel 7		
99	6	Tx6 Channel Fault Squelch	Disable all FAWS reports from Tx channel 6		
	5	Tx5 Channel Fault Squelch	Disable all FAWS reports from Tx channel 5		
	4	Tx4 Channel Fault Squelch	Disable all FAWS reports from Tx channel 4		
	3	Tx3 Channel Fault Squelch	Disable all FAWS reports from Tx channel 3		
	2	Tx2 Channel Fault Squelch	Disable all FAWS reports from Tx channel 2		
	1	Tx1 Channel Fault Squelch	Disable all FAWS reports from Tx channel 1		
	0	Tx0 Channel Fault Squelch	Disable all FAWS reports from Tx channel 0		
100	7-3	Reserved			
100	2	Tx Power Override		RW	Optional
	1	Tx Power Down			
	0	Soft Reset			
101	All	Reserved			
102	7	M-Tx15 LOS	Mask Tx LOS indicator, channel 15	RW	Optional
	6	M-Tx14 LOS	Mask Tx LOS indicator, channel 14		
	5	M-Tx13 LOS	Mask Tx LOS indicator, channel 13		
	4	M-Tx12 LOS	Mask Tx LOS indicator, channel 12		
	3	M-Tx11 LOS	Mask Tx LOS indicator, channel 11		
	2	M-Tx10 LOS	Mask Tx LOS indicator, channel 10		
	1	M-Tx9 LOS	Mask Tx LOS indicator, channel 9		
	0	M-Tx8 LOS	Mask Tx LOS indicator, channel 8		
103	7	M-Tx7 LOS	Mask Tx LOS indicator, channel 7		
	6	M-Tx6 LOS	Mask Tx LOS indicator, channel 6		
	5	M-Tx5 LOS	Mask Tx LOS indicator, channel 5		
	4	M-Tx4 LOS	Mask Tx LOS indicator, channel 4		
	3	M-Tx3 LOS	Mask Tx LOS indicator, channel 3		
	2	M-Tx2 LOS	Mask Tx LOS indicator, channel 2		
	1	M-Tx1 LOS	Mask Tx LOS indicator, channel 1		
	0	M-Tx0 LOS	Mask Tx LOS indicator, channel 0		
104	7	M-Tx15 CDR LOL	Mask Tx CDR LOL indicator, channel 15	RW	Optional
	6	M-Tx14 CDR LOL	Mask Tx CDR LOL indicator, channel 14		
	5	M-Tx13 CDR LOL	Mask Tx CDR LOL indicator, channel 13		
	4	M-Tx12 CDR LOL	Mask Tx CDR LOL indicator, channel 12		
	3	M-Tx11 CDR LOL	Mask Tx CDR LOL indicator, channel 11		
	2	M-Tx10 CDR LOL	Mask Tx CDR LOL indicator, channel 10		
	1	M-Tx9 CDR LOL	Mask Tx CDR LOL indicator, channel 9		
	0	M-Tx8 CDR LOL	Mask Tx CDR LOL indicator, channel 8		
105	7	M-Tx7 CDR LOL	Mask Tx CDR LOL indicator, channel 7		
	6	M-Tx6 CDR LOL	Mask Tx CDR LOL indicator, channel 6		
	5	M-Tx5 CDR LOL	Mask Tx CDR LOL indicator, channel 5		
	4	M-Tx4 CDR LOL	Mask Tx CDR LOL indicator, channel 4		
	3	M-Tx3 CDR LOL	Mask Tx CDR LOL indicator, channel 3		
	2	M-Tx2 CDR LOL	Mask Tx CDR LOL indicator, channel 2		
	1	M-Tx1 CDR LOL	Mask Tx CDR LOL indicator, channel 1		
	0	M-Tx0 CDR LOL	Mask Tx CDR LOL indicator, channel 0		
106	7	M-Tx15 Fault	Mask Tx Fault indicator, channel 15	RW	Optional

	6	M-Tx14 Fault	Mask Tx Fault indicator, channel 14		
	5	M-Tx13 Fault	Mask Tx Fault indicator, channel 13		
	4	M-Tx12 Fault	Mask Tx Fault indicator, channel 12		
	3	M-Tx11 Fault	Mask Tx Fault indicator, channel 11		
	2	M-Tx10 Fault	Mask Tx Fault indicator, channel 10		
	1	M-Tx9 Fault	Mask Tx Fault indicator, channel 9		
	0	M-Tx8 Fault	Mask Tx Fault indicator, channel 8		
107	7	M-Tx7 Fault	Mask Tx Fault indicator, channel 7		
	6	M-Tx6 Fault	Mask Tx Fault indicator, channel 6		
	5	M-Tx5 Fault	Mask Tx Fault indicator, channel 5		
	4	M-Tx4 Fault	Mask Tx Fault indicator, channel 4		
	3	M-Tx3 Fault	Mask Tx Fault indicator, channel 3		
	2	M-Tx2 Fault	Mask Tx Fault indicator, channel 2		
	1	M-Tx1 Fault	Mask Tx Fault indicator, channel 1		
	0	M-Tx0 Fault	Mask Tx Fault indicator, channel 0		
108	All	Reserved		RW	Optional
109	All	Reserved		RW	Optional
110	7	M-Tx15 LPW	Mask Tx Low Power Warning, channel 15	RW	Optional
	6	M-Tx14 LPW	Mask Tx Low Power Warning, channel 14		
	5	M-Tx13 LPW	Mask Tx Low Power Warning, channel 13		
	4	M-Tx12 LPW	Mask Tx Low Power Warning, channel 12		
	3	M-Tx11 LPW	Mask Tx Low Power Warning, channel 11		
	2	M-Tx10 LPW	Mask Tx Low Power Warning, channel 10		
	1	M-Tx9 LPW	Mask Tx Low Power Warning, channel 9		
	0	M-Tx8 LPW	Mask Tx Low Power Warning, channel 8		
111	7	M-Tx7 LPW	Mask Tx Low Power Warning, channel 7		
	6	M-Tx6 LPW	Mask Tx Low Power Warning, channel 6		
	5	M-Tx5 LPW	Mask Tx Low Power Warning, channel 4		
	4	M-Tx4 LPW	Mask Tx Low Power Warning, channel 4		
	3	M-Tx3 LPW	Mask Tx Low Power Warning, channel 3		
	2	M-Tx2 LPW	Mask Tx Low Power Warning, channel 2		
	1	M-Tx1 LPW	Mask Tx Low Power Warning, channel 1		
	0	M-Tx0 LPW	Mask Tx Low Power Warning, channel 0		
112	7	M-Tx15 LPA	Mask Tx Low Power Alarm, channel 15	RW	Optional
	6	M-Tx14 LPA	Mask Tx Low Power Alarm, channel 14		
	5	M-Tx13 LPA	Mask Tx Low Power Alarm, channel 13		
	4	M-Tx12 LPA	Mask Tx Low Power Alarm, channel 12		
	3	M-Tx11 LPA	Mask Tx Low Power Alarm, channel 11		
	2	M-Tx10 LPA	Mask Tx Low Power Alarm, channel 10		
	1	M-Tx9 LPA	Mask Tx Low Power Alarm, channel 9		
	0	M-Tx8 LPA	Mask Tx Low Power Alarm, channel 8		
113	7	M-Tx7 LPA	Mask Tx Low Power Alarm, channel 7		
	6	M-Tx6 LPA	Mask Tx Low Power Alarm, channel 6		
	5	M-Tx5 LPA	Mask Tx Low Power Alarm, channel 5		
	4	M-Tx4 LPA	Mask Tx Low Power Alarm, channel 4		
	3	M-Tx3 LPA	Mask Tx Low Power Alarm, channel 3		
	2	M-Tx2 LPA	Mask Tx Low Power Alarm, channel 2		
	1	M-Tx1 LPA	Mask Tx Low Power Alarm, channel 1		
	0	M-Tx0 LPA	Mask Tx Low Power Alarm, channel 0		
114	7	M-Tx15 HPA	Mask Tx High Power Alarm, channel 15	RW	Optional
	6	M-Tx14 HPA	Mask Tx High Power Alarm, channel 14		
	5	M-Tx13 HPA	Mask Tx High Power Alarm, channel 13		
	4	M-Tx12 HPA	Mask Tx High Power Alarm, channel 12		
	3	M-Tx11 HPA	Mask Tx High Power Alarm, channel 11		
	2	M-Tx10 HPA	Mask Tx High Power Alarm, channel 10		
	1	M-Tx9 HPA	Mask Tx High Power Alarm, channel 9		
	0	M-Tx8 HPA	Mask Tx High Power Alarm, channel 8		

115	7	M-Tx7 HPA	Mask Tx High Power Alarm, channel 7		
	6	M-Tx6 HPA	Mask Tx High Power Alarm, channel 6		
	5	M-Tx5 HPA	Mask Tx High Power Alarm, channel 5		
	4	M-Tx4 HPA	Mask Tx High Power Alarm, channel 4		
	3	M-Tx3 HPA	Mask Tx High Power Alarm, channel 3		
	2	M-Tx2 HPA	Mask Tx High Power Alarm, channel 2		
	1	M-Tx1 HPA	Mask Tx High Power Alarm, channel 1		
	0	M-Tx0 HPA	Mask Tx High Power Alarm, channel 0		
116	7	M-Temp High Alarm	Mask High 1st Temperature Alarm	RW	Optional
	6	M-Temp Low Alarm	Mask Low 1st Temperature Alarm		
	5	M-Temp High Warning	Mask High 1st Temperature Warning		
	4	M-Temp Low Warning	Mask Low 1st Temperature Warning		
	3	M-Temp 2 High Alarm	Mask High 2nd Temperature Alarm		
	2	M-Temp 2 Low Alarm	Mask Low 2nd Temperature 2 Alarm		
	1	M-Temp 2 High Warning	Mask High 2nd Temperature Warning		
	0	M-Temp 2 Low Warning	Mask Low 2nd Temperature Warning		
117	7	M-Vcc 3.3V High Alarm	Mask 3.3V Supply High Alarm	RW	Optional
	6	M-Vcc 3.3V Low Alarm	Mask 3.3V Supply Low Alarm		
	5	M-Vcc 3.3V High Warning	Mask 3.3V Supply High Warning		
	4	M-Vcc 3.3V Low Warning	Mask 3.3V Supply Low Warning		
	3-0	Reserved			
118	7	P-Non-Volatile	Persistence treated as non-volatile	RW	Optional
	6	P-Tx LOS Alarm	Persistent Tx LOS Alarm		
	5	P-Tx CDR LOL Alarm	Persistent Tx CDR LOL Alarm		
	4	P-Tx Fault Alarm	Persistent Tx Fault Alarm		
	3	Reserved			
	2	P-Tx Power Alarm	Persistent Tx Power Alarm		
	1	P-Tx Temperature Alarm	Persistent Tx Temperature Alarm		
	0	P-Tx Vcc Alarm	Persistent Tx Vcc Alarm		
119	All	PWCE MSB	Password Change Entry Area	WO	Optional
120	All	PWCE			
121	All	PWCE			
122	All	PWCE LSB			
123	All	PWE MSB	Password Entry Area	WO	Required
124	All	PWE			
120	All	PWE			
126	All	PWE LSB			
127	All	PSB	Page Select byte	RW	Required
Note 1: 0 = Adaptive equalization mode, 1 = Manual equalization mode (see Bytes 81-88 for manual equalization settings) Note 2: Freeze bit not used in manual equalization mode					

9.8 Upper Page 00

Upper Page 00 consists of the Serial ID and is used for read only identification information. The Serial ID is divided into the Base ID Fields, Extended ID Fields and Vendor Specific ID Fields.

Table 45: P00 Page Summary

Byte	Size	Name	Description	Type	Option
128	1	Identifier	Identifier Type of Module CDFP style 3 = 16h	RO	Required
129	1	Extended Identifier	Extended Identifier	RO	Required
130	1	Connector	Code for connector type	RO	Required
131–138	8	Specification Compliance	Code for electronic or optical compatibility	RO	Required
139	1	Encoding	Code for serial encoding algorithm	RO	Required
140	1	BR, nominal	Nominal bit rate, units of 100 Mbit/s	RO	Required
141	1	Extended Rate Select	Tags for Extended Rate Select Compliance	RO	Required
142–146	5	Link Length	Link length /Transmission media	RO	Required
147	1	Device Tech	Device technology	RO	Required
148–163	16	Vendor name	Vendor name (ASCII)	RO	Required
164	1	Extended Module	Extended module codes for Infiniband	RO	Required
165–167	3	Vendor OUI	Vendor IEEE company ID	RO	Required
168–183	16	Vendor PN	Part number provided by vendor (ASCII)	RO	Required
184–185	2	Vendor Rev	Revision level for part number provided by vendor (ASCII)	RO	Required
186–187	2	Wavelength or Cu Att	Nominal laser wavelength (1/20 nm) or copper cable attenuation in dB at 2.5 GHz (#186) and 5 GHz (#187)	RO	Required
188–189	2	Wavelength Tolerance	Guaranteed range of laser wavelength from nominal wavelength (1/200 nm)	RO	Required
190	1	Max Case Temp	Maximum case temperature in °C	RO	Required
191	1	CC_BASE	Check code for Base ID fields (#128-190)	RO	Required
192–195	4	Options	Indicates which optional capabilities are implemented in the module	RO	Required
196–211	16	Vendor S/N	Vendor product serial number (ASCII)	RO	Required
212–219	8	Date Code	Vendor manufacturing date code (ASCII)	RO	Required
220	1	Diagnostic Monitoring	Indicates which type of diagnostic monitoring are implemented in the module	RO	Required
221–222	2	Enhanced Options	Indicates which optional enhanced features are implemented in the module	RO	Required
223	1	CC_EXT	Check code for Extended ID (#192-222)	RO	Required
224–255	32	Vendor Specific	Vendor-specific ID information	RO	Optional

9.8.1 Identifier and Extended Identifier

See Section 8.4.2

9.8.2 Connector Type

See Section 8.4.3

9.8.3 Specification Compliance

See Section 8.4.4

9.8.4 Encoding

See Section 8.4.5

9.8.5 BR, nominal

See Section 8.4.6

9.8.6 Extended Rate Select and Global Options

See Section 8.4.7

9.8.7 Link Length

See Section 8.4.8

9.8.8 Device technology

See Section 8.4.9

9.8.9 Vendor Name

See Section 8.4.10

9.8.10 Extended Module Code

See Section 8.4.11

9.8.11 Vendor OUI

See Section 8.4.12

9.8.12 Vendor Part Number

See Section 8.4.13

9.8.13 Vendor Revision Number

See Section 8.4.14

9.8.14 Wavelength

See Section 8.4.15

9.8.15 Wavelength Tolerance

See Section 8.4.16

9.8.16 Maximum Case Temperature

See Section 8.4.17

9.8.17 CC_BASE

See Section 8.4.18

9.8.18 Options

See Section 8.4.19

Table 46: Options

Byte	Bit	Name	Description	Type	Option
192	All	Extended Ethernet Compliance Codes	00h Unspecified 01h 100G AOC (Active Optical Cable) 02h 100GBASE-SR4 03h 100GBASE-LR4 04h 100GBASE-ER4 05h 100GBASE-SR10 06h 100G CWDM4 Coarse WDM SMF	RO	Required

			07h 100G PSM4 Parallel SSMF 08h 40GBASE-ER4 09h-FFh Reserved		
193	7	Tx Adaptive Equalization implemented	Coded 1 if Tx Adaptive Equalization provided	RO	Required
	6	Tx Adaptive Equalization Freeze implemented	Coded 1 if Tx Adaptive Equalization Freeze provided		
	5	Rx polarity flip implemented	Coded 1 if Rx polarity flip control provided		
	4	Tx polarity flip implemented	Coded 1 if Tx polarity flip control provided		
	3	Tx input Equalization implemented	Coded 1 if Tx equalization control provided		
	2	Rx LOS implemented	Coded 1 if Rx LOS alarm flags provided		
	1	Rx pre-emphasis implemented	Coded 1 if Rx pre-emphasis control provided		
	0	Rx output amplitude implemented	Coded 1 if Rx output amplitude control provided		
194	7	Tx CDR Bypass implemented	Coded 1 if Tx CDR Bypass control provided	RO	Required
	6	Rx CDR Bypass implemented	Coded 1 if Rx CDR Bypass control provided		
	5	Tx CDR LOL implemented	Coded 1 if Tx CDR LOL alarm flag provided		
	4	Rx CDR LOL implemented	Coded 1 if Rx CDR LOL alarm flag provided		
	3	Rx Squelch Disable implemented	Coded 1 if Rx Squelch Disable control provided		
	2	Rx Output Disable implemented	Coded 1 if Rx Output Disable control provided		
	1	Tx Squelch Disable implemented	Coded 1 if Tx Squelch Disable control provided		
	0	Tx Squelch present	Coded 1 if Tx Squelch provided		
195	7	Memory Page 02 present	Coded 1 if memory page 02 provided	RO	Required
	6	Memory Page 01 present	Coded 1 if memory page 01 provided		
	5	Tx Rate Select implemented	Coded 1 if Tx Rate Select control provided		
	4	Tx Disable implemented	Coded 1 if Tx Disable control provided		
	3	Tx Fault Flag implemented	Coded 1 if Tx Fault supported		
	2	Tx Squelch Pave	Coded 1 if Tx Squelch implemented to reduce Pave; coded 0 if Tx Squelch implemented to reduce OMA		
	1	Tx LOS Flag implemented	Coded 1 if Tx LOS alarm flag provided		
	0	Rx Squelch implemented	Coded 1 if Rx Squelch provided		

9.8.19 Vendor Serial Number

See Section 8.4.20

9.8.20 Date Code

See Section 8.4.21

9.8.21 Diagnostic Monitoring Type

See Section 8.4.22

9.8.22 Enhanced Options

See Section 8.4.23

9.8.23 CC_EXT

See Section 8.4.24

9.8.24 Vendor Specific

See Section 8.4.25

9.9 Upper Page 01

The format of upper page 01 is identical to that specified for QSFP. For CDFP products upper page 01 is not used.

9.10 Upper Page 02

Upper Page 02 is optionally provided as user writable EEPROM. The host system may read or write this memory for any purpose.

9.11 Upper Page 03

The upper memory page 03 contains module thresholds, channel thresholds and optional channel controls.

9.11.1 Module Card Thresholds

Each quantitative module card monitor has a corresponding high alarm and low alarm threshold. Some monitors may also have high warning and low warning thresholds. For each monitor that is implemented, high and low alarm thresholds are required. These factory-preset values allow the user to determine when a particular value is outside of normal limits as determined by the device manufacturer. The values are stored in the same format as the corresponding monitor value reported in the lower page. The threshold values are stored in read-only memory in upper memory page 03.

9.11.2 Channel Thresholds

Each quantitative channel monitor has also a corresponding high alarm and low alarm threshold. Some monitors may also have high warning and low warning thresholds. These threshold values are stored in read-only memory in upper memory page 03.

9.11.3 Extended Channel Controls

The extended channel control fields allow the host computer system to change the gross behavior of the device. The changeable parameters include data rate and application support by the channel.
Rate Select is an optional control used to limit the receiver bandwidth for compatibility with multiple data rates and allows the transmitter to be fine-tuned for specific data rates. The module may:

a) Provide no support for rate selection

b) Rate selection using extended rate select

c) Rater selection with application select tables

The Extended Rae Select Controls have a four bit code block (bits 7-4 or 3-0) assigned to each channel. Codes 1xxxb are reserved. Code 0000b calls for no rate selection. Code 0111b calls for the highest data rate supported. Code 0001b calls for the lowest data rate supported. Intermediate code values call for intermediate data rates if any. The exact Rate Select parameters are presented in the device datasheet. When the Extended Rate Select bits for a particular channel are all zeroes, the Application Select method defined in Page 01 may be used. The host reads the entire

Application Select Table (AST) on page 01 to determine the capabilities of the Module card. The host controls each channel separately by writing a Control Mode and Table Select (TS) byte to the Application Select bytes. The two-bit Control Mode value occupies the most-significant bits of the control byte and defines the application control mode. The six-bit Table Select value occupies the least-significant bits of the control byte and selects the module card behavior from the Application Select table among the 63 possibilities described there (values 000000b to 111110b). Note that the value 111111b is invalid.

9.11.4 Extended ID

The Extended ID fields provide vendor-specific information about the construction of the module. This information is necessary for determining the suitability of the embedded firmware upgrades in the field.

9.12 Upper Page 03 Summary

Upper page 03 is subdivided into several areas as illustrated in the following table:

Table 47: Upper Memory Page 03 Summary

Byte	Name Rx, Lower Card	Type	Option
128-175	Module Thresholds	RO	Optional
176-215	Channel Thresholds	RO	Optional
216-243	Extended Channel Controls	RW	Optional
244-251	Extended Channel Monitors	RO	Optional
252-255	Extended ID	RO	Required

9.13 Upper Page 03 Overview

Table 48: Upper Memory Page 03 Overview

Byte	Name Rx, Lower Card	Name Tx, Upper Card	Type	Option
128-131	Temp 1 H/L A/W Threshold	Temp 1 H/L A/W Threshold	RO	Optional
132-135	Temp 2 H/L A/W Threshold	Temp 2 H/L A/W Threshold	RO	Optional
136-143	Reserved	Reserved	RO	
144-147	Vcc 3.3V H/L A/W Threshold	Vcc 3.3V H/L A/W Threshold	RO	Optional
148-175	Reserved	Reserved	RO	
176	Rx Power HA Threshold	Tx Power HA Threshold	RO	Optional
177	Rx Power LA Threshold	Tx Power LA Threshold	RO	Optional
178	Reserved	Tx Bias HA Threshold	RO	Optional
179	Rx Power LW Threshold	Tx Bias LA Threshold	RO	Optional
180-215	Reserved	Reserved	RO	Optional
216-223	Rx Rate Select	Tx Rate Select	RW	Optional
224-239	Rx Application Select	Tx Application Select	RW	Optional
240-243	Reserved	Reserved	RW	Optional
244-251	Reserved	Tx Current Adaptive Equalization	RO	Optional
252-253	HW Rev	HW Rev	RO	Required
254-255	FW Rev	FW Rev	RO	Required

9.14 Upper Page 03 Rx

Table 49: Upper Memory Page 03 Rx

Byte	Bit	Name	Description
128	All	Temp1 HA Thr	High Alarm threshold for 1st temperature monitor
129	All	Temp1 LA Thr	Low Alarm threshold for 1st temperature monitor
130	All	Temp1 HW Thr	High Warning threshold for 1st temperature monitor

131	All	Temp1 LW Thr	Low Warning threshold for 1st temperature monitor
132	All	Temp2 HA Thr	High Alarm threshold for 2nd temperature monitor
133	All	Temp2 LA Thr	Low Alarm threshold for 2nd temperature monitor
134	All	Temp2 HW Thr	High Warning threshold for 2nd temperature monitor
135	All	Temp2 LW Thr	Low Warning threshold for 2nd temperature monitor
136–143	All	Reserved	
144	All	Vcc 3.3V HA Thr MSB	High Alarm threshold for Vcc 3.3V monitor
145	All	Vcc 3.3V HA Thr LSB	
146	All	Vcc 3.3V LA Thr MSB	Low Alarm threshold for Vcc 3.3V monitor
147	All	Vcc 3.3V LA Thr LSB	
144	All	Vcc 3.3V HW Thr MSB	High Warning threshold for Vcc 3.3V monitor
145	All	Vcc 3.3V HW Thr LSB	
146	All	Vcc 3.3V LW Thr MSB	Low Warning threshold for Vcc 3.3V monitor
147	All	Vcc 3.3V LW Thr LSB	
148–175	All	Reserved	
176	All	Rx Power HA Thr	Rx Power High Alarm Threshold [20μW]
177	All	Rx Power LA Thr	Rx Power Low Alarm Threshold [20μW]
178	All	Reserved	
179	All	Rx Power LW Thr	Rx Power Low Warning Threshold [20μW]
180–215	All	Reserved	
216	7-4	Rx1 Rate Select	Rx data rate select, channel 1
	3-0	Rx0 Rate Select	Rx data rate select, channel 0
217	7-4	Rx3 Rate Select	Rx data rate select, channel 3
	3-0	Rx2 Rate Select	Rx data rate select, channel 2
218	7-4	Rx5 Rate Select	Rx data rate select, channel 5
	3-0	Rx4 Rate Select	Rx data rate select, channel 4
219	7-4	Rx7 Rate Select	Rx data rate select, channel 7
	3-0	Rx6 Rate Select	Rx data rate select, channel 6
220	7-4	Rx9 Rate Select	Rx data rate select, channel 9
	3-0	Rx8 Rate Select	Rx data rate select, channel 8
221	7-4	Rx11 Rate Select	Rx data rate select, channel 11
	3-0	Rx10 Rate Select	Rx data rate select, channel 10
222	7-4	Rx13 Rate Select	Rx data rate select, channel 13
	3-0	Rx12 Rate Select	Rx data rate select, channel 12
223	7-4	Rx15 Rate Select	Rx data rate select, channel 15
	3-0	Rx14 Rate Select	Rx data rate select, channel 14
224	7-6	Rx0 AST Control	Rx application select, channel 0
	5-0	Rx0 AST Select	
220	7-6	Rx1 AST Control	Rx application select, channel 1
	5-0	Rx1 AST Select	
226	7-6	Rx2 AST Control	Rx application select, channel 2
	5-0	Rx2 AST Select	
227	7-6	Rx3 AST Control	Rx application select, channel 3
	5-0	Rx3 AST Select	
228	7-6	Rx4 AST Control	Rx application select, channel 4
	5-0	Rx4 AST Select	

229	7-6	Rx5 AST Control	Rx application select, channel 5
	5-0	Rx5 AST Select	
230	7-6	Rx6 AST Control	Rx application select, channel 6
	5-0	Rx6 AST Select	
231	7-6	Rx7 AST Control	Rx application select, channel 7
	5-0	Rx7 AST Select	
232	7-6	Rx8 AST Control	Rx application select, channel 8
	5-0	Rx8 AST Select	
233	7-6	Rx9 AST Control	Rx application select, channel 9
	5-0	Rx9 AST Select	
234	7-6	Rx10 AST Control	Rx application select, channel 10
	5-0	Rx10 AST Select	
235	7-6	Rx11 AST Control	Rx application select, channel 11
	5-0	Rx11 AST Select	
236	7-6	Rx12 AST Control	Rx application select, channel 12
	5-0	Rx12 AST Select	
237	7-6	Rx13 AST Control	Rx application select, channel 13
	5-0	Rx13 AST Select	
238	7-6	Rx14 AST Control	Rx application select, channel 14
	5-0	Rx14 AST Select	
239	7-6	Rx15 AST Control	Rx application select, channel 15
	5-0	Rx15 AST Select	
240-251	All	Reserved	
252	All	HW Rev	Hardware revision number
253	All	HW Type	Hardware type code
254	All	FW Rev Maj	Firmware major revision number
255	All	FW Rev Min	Firmware minor revision number

9.15 Upper Page 03 Tx

Table 50: Upper memory Page 03 Tx

Byte	Bit	Name	Description
128	All	Temp1 HA Thr	High Alarm threshold for 1st temperature monitor
129	All	Temp1 LA Thr	Low Alarm threshold for 1st temperature monitor
130	All	Temp1 HW Thr	High Warning threshold for 1st temperature monitor
131	All	Temp1 LW Thr	Low Warning threshold for 1st temperature monitor
132	All	Temp2 HA Thr	High Alarm threshold for 2nd temperature monitor
133	All	Temp2 LA Thr	Low Alarm threshold for 2nd temperature monitor
134	All	Temp2 HW Thr	High Warning threshold for 2nd temperature monitor
135	All	Temp2 LW Thr	Low Warning threshold for 2nd temperature monitor
136-143	All	Reserved	
144	All	Vcc 3.3V HA Thr MSB	High Alarm threshold for Vcc 3.3V monitor
145	All	Vcc 3.3V HA Thr LSB	
146	All	Vcc 3.3V LA Thr MSB	Low Alarm threshold for Vcc 3.3V monitor
147	All	Vcc 3.3V LA Thr LSB	
144	All	Vcc 3.3V HW Thr MSB	High Warning threshold for Vcc 3.3V monitor
145	All	Vcc 3.3V HW Thr LSB	
146	All	Vcc 3.3V LW Thr MSB	Low Warning threshold for Vcc 3.3V monitor
147	All	Vcc 3.3V LW Thr	

		LSB	
148–175	All	Reserved	
176	All	Tx Power HA Thr	Tx Power High Alarm Threshold [20μW]
177	All	Tx Power LA Thr	Tx Power Low Alarm Threshold [20μW]
178	All	Tx Bias HA Thr	Tx Bias Current High Alarm Threshold [0.1 mA]
179	All	Tx Bias LA Thr	Tx Bias Current Low Alarm Threshold [0.1 mA]
180–215	All	Reserved	
216	7-4	Tx1 Rate Select	Tx data rate select, channel 1
	3-0	Tx0 Rate Select	Tx data rate select, channel 0
217	7-4	Tx3 Rate Select	Tx data rate select, channel 3
	3-0	Tx2 Rate Select	Tx data rate select, channel 2
218	7-4	Tx5 Rate Select	Tx data rate select, channel 5
	3-0	Tx4 Rate Select	Tx data rate select, channel 4
219	7-4	Tx7 Rate Select	Tx data rate select, channel 7
	3-0	Tx6 Rate Select	Tx data rate select, channel 6
220	7-4	Tx9 Rate Select	Tx data rate select, channel 9
	3-0	Tx8 Rate Select	Tx data rate select, channel 8
221	7-4	Tx11 Rate Select	Tx data rate select, channel 11
	3-0	Tx10 Rate Select	Tx data rate select, channel 10
222	7-4	Tx13 Rate Select	Tx data rate select, channel 13
	3-0	Tx12 Rate Select	Tx data rate select, channel 12
223	7-4	Tx15 Rate Select	Tx data rate select, channel 15
	3-0	Tx14 Rate Select	Tx data rate select, channel 14
224	7-6	Tx0 AST Control	Tx application select, channel 0
	5-0	Tx0 AST Select	
220	7-6	Tx1 AST Control	Tx application select, channel 1
	5-0	Tx1 AST Select	
226	7-6	Tx2 AST Control	Tx application select, channel 2
	5-0	Tx2 AST Select	
227	7-6	Tx3 AST Control	Tx application select, channel 3
	5-0	Tx3 AST Select	
228	7-6	Tx4 AST Control	Tx application select, channel 4
	5-0	Tx4 AST Select	
229	7-6	Tx5 AST Control	Tx application select, channel 5
	5-0	Tx5 AST Select	
230	7-6	Tx6 AST Control	Tx application select, channel 6
	5-0	Tx6 AST Select	
231	7-6	Tx7 AST Control	Tx application select, channel 7
	5-0	Tx7 AST Select	
232	7-6	Tx8 AST Control	Tx application select, channel 8
	5-0	Tx8 AST Select	
233	7-6	Tx9 AST Control	Tx application select, channel 9
	5-0	Tx9 AST Select	
234	7-6	Tx10 AST Control	Tx application select, channel 10
	5-0	Tx10 AST Select	
235	7-6	Tx11 AST Control	Tx application select, channel 11
	5-0	Tx11 AST Select	
236	7-6	Tx12 AST Control	Tx application select, channel 12
	5-0	Tx12 AST Select	
237	7-6	Tx13 AST Control	Tx application select, channel 13
	5-0	Tx13 AST Select	
238	7-6	Tx14 AST Control	Tx application select, channel 14
	5-0	Tx14 AST Select	
239	7-6	Tx15 AST Control	Tx application select, channel 15
	5-0	Tx15 AST Select	

240-243		Reserved	
244	7-4	Tx1 Current AE	Tx Current Adaptive Equalization, channel 1
	3-0	Tx0 Current AE	Tx Current Adaptive Equalization, channel 0
245	7-4	Tx3 Current AE	Tx Current Adaptive Equalization, channel 3
	3-0	Tx2 Current AE	Tx Current Adaptive Equalization, channel 2
246	7-4	Tx5 Current AE	Tx Current Adaptive Equalization, channel 5
	3-0	Tx4 Current AE	Tx Current Adaptive Equalization, channel 4
247	7-4	Tx7 Current AE	Tx Current Adaptive Equalization, channel 7
	3-0	Tx6 Current AE	Tx Current Adaptive Equalization, channel 6
248	7-4	Tx9 Current AE	Tx Current Adaptive Equalization, channel 9
	3-0	Tx8 Current AE	Tx Current Adaptive Equalization, channel 8
249	7-4	Tx11 Current AE	Tx Current Adaptive Equalization, channel 11
	3-0	Tx10 Current AE	Tx Current Adaptive Equalization, channel 10
250	7-4	Tx13 Current AE	Tx Current Adaptive Equalization, channel 13
	3-0	Tx12 Current AE	Tx Current Adaptive Equalization, channel 12
251	7-4	Tx15 Current AE	Tx Current Adaptive Equalization, channel 15
	3-0	Tx14 Current AE	Tx Current Adaptive Equalization, channel 14
252		HW Rev	Hardware revision number
253		HW Type	Hardware type code
254		FW Rev Maj	Firmware major revision number
255		FW Rev Min	Firmware minor revision number

10 CDFP Firmware Upgrade

This section addresses the method of upgrading of firmware in CDFP modules after the modules have been installed in a communications network. The requirements of the method are

1) The upgrade must be done without removing the modules from the system where they are installed,
2) The method should be common across multiple vendors modules,
3) The host system should not have to know the internal details of any particular module, and
4) The firmware data files must be able to be sent over the internet without being corrupted or blocked by corporate firewalls and anti-virus filters.

The first requirement dictates that the host system must communicate with the module over the existing two-wire serial interface; this in turn indicates that the data file should contain a sequence of "packets" to be sent over the two-wire serial interface. The last requirement indicates that the data files should be ASCII text with the binary bytes to be sent over the two-wire serial interface being represented by pairs of hexadecimal digit characters.

The data file has a human-readable header section describing the firmware in the file and a firmware data section containing the packets of data to be sent over the two-wire serial interface. The first part of the data section is a prelude which configures the module for firmware loading.

10.1 Human-readable Header Section

The header section consists of a number of lines which all start with a semicolon to distinguish them from the firmware data section. The first line describes the firmware in human terms and should be ignored by the host system; this line should include the module manufacturer's name. The remaining lines in the header section are all tag/value pairs which can be evaluated by the host system to determine the various parameters of the firmware. Each of the tag/value pairs is described in detail below.

;FMTVer=1.02

This should be the second line of the header. It defines the format of the rest of the file. Format version 1.02 is the format described in this document.

;Version=5.17

This line identifies the version number of the firmware in the data file, a major version number and a minor version number separated by a decimal point. After the firmware has been loaded the host can read the firmware version from the module memory map (P03 #254 FW major and P03 #255 FW minor revision) to determine if the firmware was loaded correctly.

;H/Wcomp=9

This line identifies the type of hardware in the module that the firmware is designed for. The host system should read the module hardware type from the memory map (P03 #252) and check for compatibility before attempting to load the firmware. If the module has a different hardware version number, the host system should not continue with the firmware upgrade for that module.

;F/Wcomp=5.*

This line identifies the firmware version in the module that the firmware in the data file is intended to replace or modify; an asterisk indicates a wildcard which matches any value in the corresponding field.

; CRC16=1234
; CRC32=12345678
; MD5=1234567890123456
; SHA1=12345678901234567890

These lines define the checksum of all the binary bytes to be sent over the two-wire serial interface by the corresponding algorithm. The lines in the header section (including these checksums) are excluded from the checksum calculations.

Additional tag/value pairs may be added to cater for any special requirements of the modules.

10.2 Firmware Data Section

The firmware data section is a list of "packets" to be sent over the two-wire serial interface, one packet per line in the file. If a packet is too large to fit reasonably in a single line, it may be split across multiple lines by putting a backslash character ('\') at the end of each line of the packet except the last; there is no limit to the size of the packet except that the module must be able to receive and process an entire packet. The packet data is represented by a sequence of hexadecimal digit character pairs with no embedded spaces or punctuation other than a possible parameter sentinel (see below). The host system is expected to convert the sequence of hexadecimal digit character pairs into a sequence of binary bytes and then send the binary bytes over the two-wire serial interface along with the appropriate start and stop conditions.

Write packets

Packets of data to be sent to the module start with the two-wire serial address of the module receiver and the read/write bit set to zero to indicate a write. The rest of the packet may contain a buffer address, a wrapper round the data, the data itself, and one

or more checksums so that the module can verify that the packet was transmitted correctly. The host system does no checksum verification - such checking is delegated to the module.

Status Read Packets

Packets requesting data from the module start with the two-wire serial address of the module receiver and the read/write bit set to one to indicate a read. A Status Read requests a single byte from the module. The value read can then be compared with the remaining bytes in the packet - a match with any byte indicates that the previous write packet was received and processed correctly. For modules that provide the status response at a particular register address, the read request must be preceded by a write packet that sets the register address but sends no data.

Parameter Read Packets

Some microcontrollers have a loader built into the hardware; that loader may have a write-protect feature that requires a "password" to be read from the hardware and then re-written to permit firmware upgrade. Packets requesting such data from the module have the device address byte followed by a parameter sentinel, '%', a one-digit parameter number, and the number of bytes to be read. For example, the packet "B3%120" means read hex 20 (32 decimal) bytes from the device at address hex B3 and store them in parameter 1. A subsequent write packet may have one of its data bytes replaced by the parameter sentinel and accompanying digit; the host system is expected to replace the parameter indicator with the contents of the stored parameter before transmitting the packet to the module. At the time of writing, the only requirement identified is for one parameter of length 32 bytes. When calculating the file checksums, the parameter sentinel characters should be replaced by zero characters ('0').

10.3 Implementation Notes

When the host system gets an unexpected response to a status read, it should first read the status byte again to check for transmission errors. If the response is still not one of the expected values, the host system should re-write the last block written to the module card. The allowable number of retries before declaring a failure should be set by the system administrator.

A CDFP module contains two module cards, each with its own two-wire serial address. The host system may have one controller for both module cards or one controller for each card. In the first case the firmware for the two module cards can be combined in a single file, either serially or interleaved depending on the module capabilities. In the second case, the firmware for each module card should be contained in a separate file; the host systems management of multiple files is beyond the scope of this document. The module manufacturers may need to support both types of systems.

After the firmware has been written to the module, the host system can optionally reset the module and later read the firmware version number to verify that the firmware was loaded correctly.

10.4 Example File

This example shows the most complex form of the data file - interleaved data for both module cards. A data file for either module card alone would be the same with the lines for the other module card removed. Similarly, a data file for loading the module cards serially would have all the lines for one module card ahead of all the lines for the other module card. The example shows the human-readable header section followed by a preamble which tells one module card and then the other that a firmware update is about

to commence. A status read to each module card then verifies that both module cards processed the preamble correctly. The remainder of the file consists of the data packets to be sent to the module cards and the status read-backs to verify that the data packets were processed correctly.

```
; XYZcompany CDFP firmware version 0.01
; FMTVer=1.02
; Version=0.01
; H/Wcomp=9
; F/Wcomp=0.*
; CRC16=1234
; CRC32=12345678
; MD5=1234567890123456
; SHA1=12345678901234567890
B2774C6F6164
B27BDEADBEEF
B27F07
B2816996
B280DA
BA774C6F6164
BA7BDEADBEEF
BA7F07
BA816996
BA80DA
B283
B311CC
BA83
BB11CC
B288066019310000C1A100280000D827D8270000D827D8270000D827D8270000D827A822\
0000D827D82700005E23D8270000D827D8270000D8271A260000D827D8270000B3243CC1
BA880770D827D8270000D827D8270000D827542100004E21D82700005822D8270000D827D\
8270000D827D8270000D827D8270000D827D8270000D827D8270000D827D827CD6A5FC0
B283
B33366
B28808800000D827D8270000D827D8270000D827D8270000D827D8270000D827D8270000\
D827D8270000D827D8270000D827D8270000D827D8270000D827D8270000D82769C5F25D
BA83
BB3366
BA880990D8270000D827D8270000D827D8270000D827D8270000D827D8270000D827D82\
70000D827D8270000D827D8270000D827D8270000D827D8270000D827D8270000AD156B04
B283
B33366
B2880AA0D827D8270000D827D8270000D827A00F000000E4A8610000E40C28410000D94\
0003200009C1D5A0B00000032A5A8000055D50AD700005500F1FF00005500F1FFB1416C89
BA83
BB3366
Etc.
```

10.5 Host Upgrade Procedure

The recommended procedure for the host to follow is illustrated in the flowchart below:

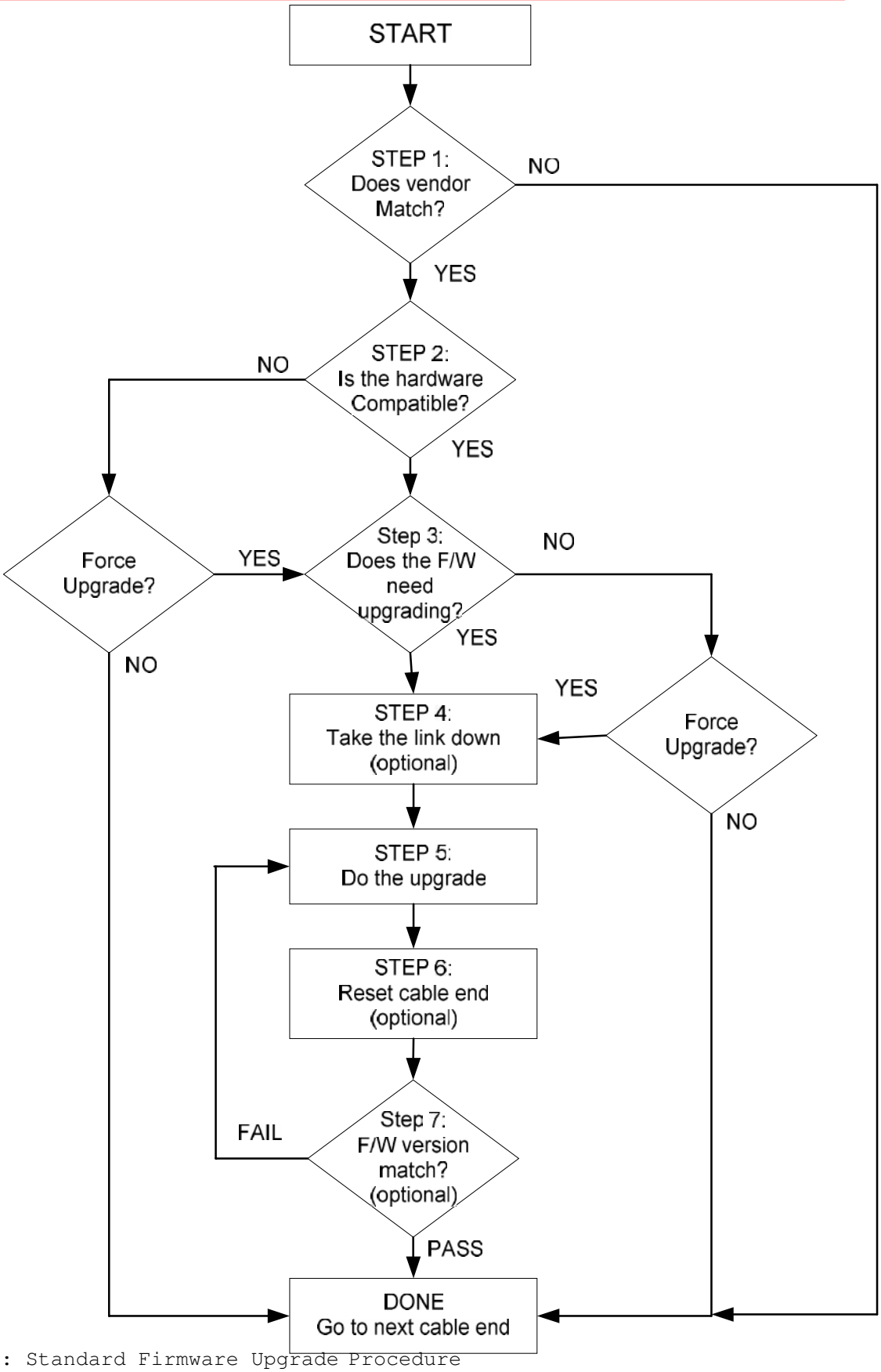


Figure 64: Standard Firmware Upgrade Procedure

STEP 1: Does the vendor match?

The host should verify that the module manufacturer is the same as that given in the data file. Note that reading the part number or vendor name from the module may not be sufficient – private labeling of modules means that the vendor name in the module may not be that of the manufacturer.

For some vendor's modules, there may be a preliminary step as illustrated in the flowchart below.

STEP 2: Is the hardware compatible?

The host should verify that the hardware id specified in the data file matches the value read from the module. This step allows the user to update a system with multiple product types generically, without loading incorrect firmware on cables from different product families.

STEP 3: Does the firmware need upgrading?

If the firmware version number in the data file is the same as the firmware version number in the module there is no need to do the firmware update.

STEP 4: Take the link down (optional)

This is customer specific. The customer needs to manage this step. In theory, the optical engines can keep running while the firmware is being upgraded, but they do so with whatever parameters were set prior to the start of the firmware upgrade.

STEP 5: Do the firmware upgrade

Having decided to do the firmware upgrade, the host performs the two-wire serial transactions listed in the data file(s).

STEP 6: Reset the cable end (optional)

After all lines from the data file have been written to the module, the host can toggle the modules reset pin or cycle its power to activate the new firmware. Note that this will disrupt the flow of high-speed data through the module. For hitless firmware upgrades, this step can be omitted.

STEP 7: Does the new firmware number appear in the module?

If the firmware has been upgraded successfully, the new firmware version number should appear in the memory map. If it doesn't then something went wrong with the upgrade and the operation should be repeated. It is at the customers' discretion to decide how many upgrade failures should result in the attempts being abandoned.

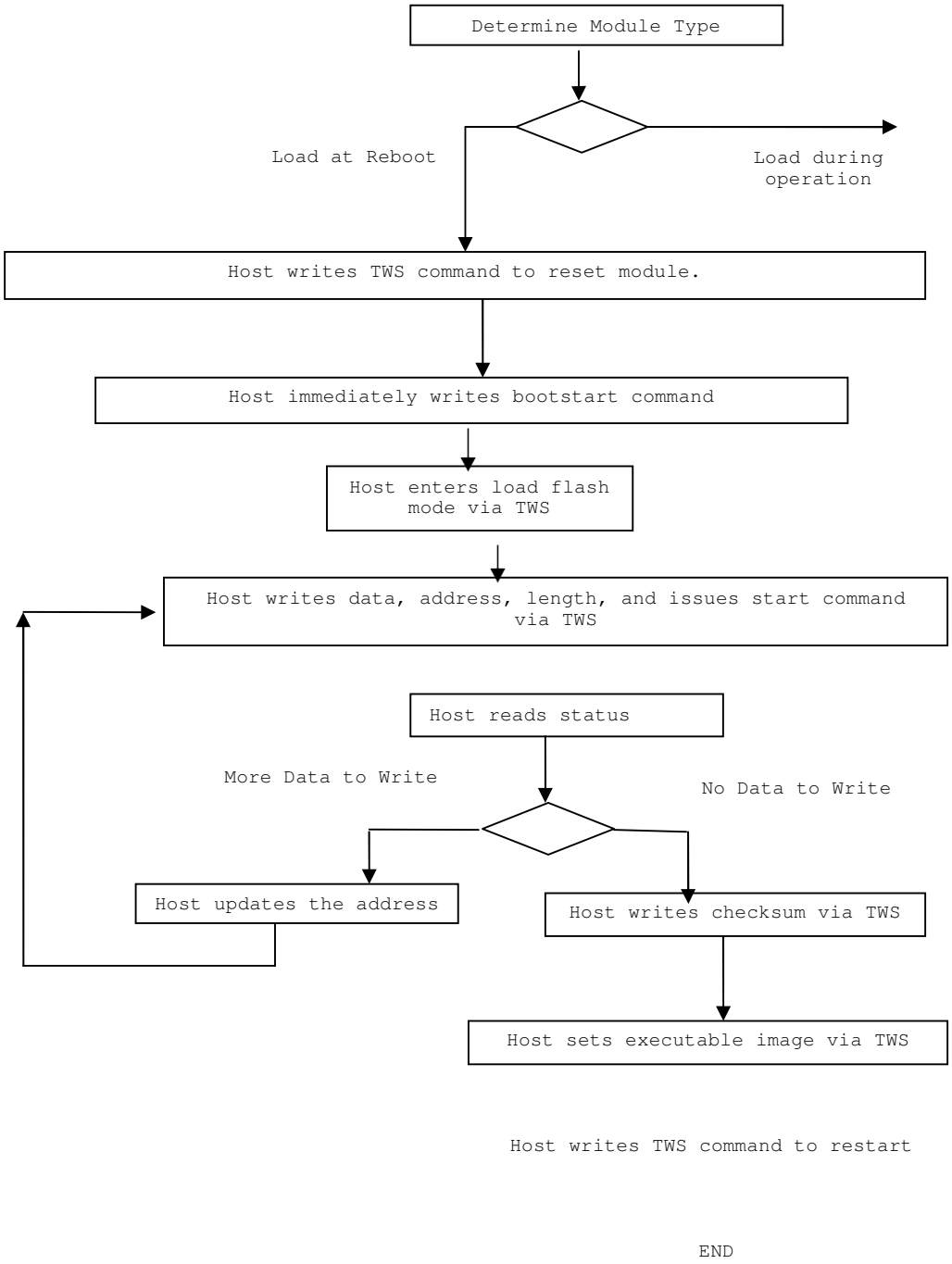


Figure 65: Alternate Firmware Upgrade Procedure