Serial-MII Specification

Change History

Revision	Date	Description
0.1	March 3, 1998	First Draft
0.2	March 10, 1998	Changed the input setup time specification from 2ns to 1ns.
0.3	March 30, 1998	Added high nibble valid bit to inter-frame status
1.0	April 30, 1998	Moved CRS to the end of the receive segment and TX_ER to the end of the transmit segment. Changed the input setup time specification from 1 ns to 1.5 ns.
1.1	May 8, 1998	Moved CRS to the beginning of the receive segment and TX_ER to the beginning of the transmit segment. Changed the receive status encoding from CRS=0 and RX_DV=0 to CRS=X and RX_DV=0.
1.2	June 16, 1998	Clarified the free running nature of SYNC, the signalling of inter-frame status, and where in the system each timing parameter is specified. Added false carrier bit to inter-frame status.
2.0	January 17, 2000	Added source synchronous option.
2.1	February 9, 2000	Reduced minimum output delay from 2 nsec to 1.5 nsec

table 1 Change History

Overview

The Serial Media Independent Interface (SMII) is designed to satisfy the following requirements:

- Convey complete MII information between a 10/100 PHY and MAC with two pins per port.
- Allow a multi-port MAC/PHY communication with one system clock.
- Operate in both half and full duplex.
- Per packet switching between 10MBit and 100MBit data rates.
- Allow direct MAC to MAC communication.
- Optional source synchronous mode

SMII is composed of two signals per port, a global synchronization signal, and a global 125MHz reference clock. All signals are synchronous to the clock.

For applications requiring longer trace delay's (more than 1ns), four optional signals may be added in place of SYNC. RX_CLK and RX_SYNC synchronize RX for one or more ports, similarly TX_CLK and TX_SYNC synchronize TX for one or more ports. RX_CLK and TX_CLK are frequency locked, but not necessarily phase locked to CLOCK. An SMII application that uses these optional signals is referred to as *source synchronous.*

Name	From	To	Use	Notes
RX	PHY	MAC	Receive Data and Control	
TX	MAC	PHY	Transmit Data and Control	
SYNC	MAC	PHY	Synchronization	
CLOCK	System	MAC & PHY	Synchronization	
RX_CLK	PHY	MAC	Synchronization	These signals may be used in place of SYNC in systems requiring trace delay's longer than 1ns.
RX_SYNC	PHY	MAC	Synchronization	
TX_CLK	MAC	PHY	Synchronization	
TX_SYNC	MAC	PHY	Synchronization	

table 2 SMII Signals

The following figure shows a common SMII application.

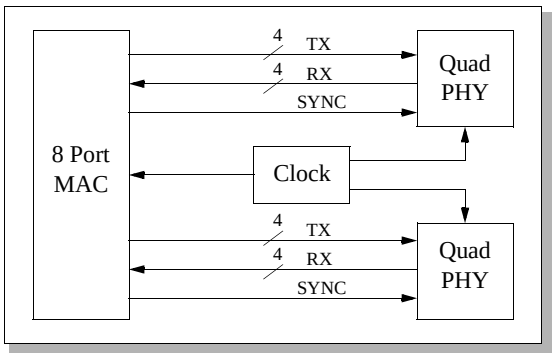

figure 1 Typical SMII System

A sample SMII application requiring long trace delay's is shown in the following figure.

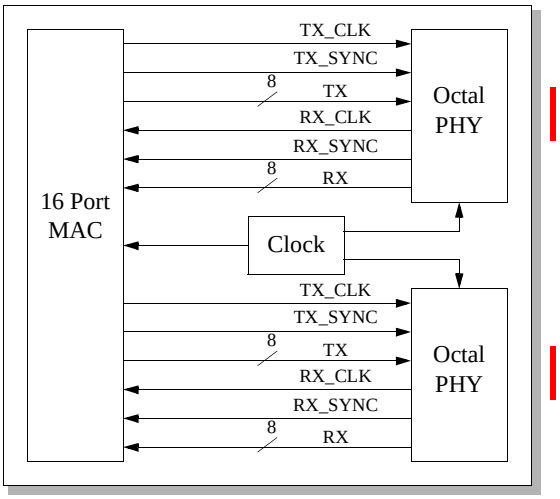

figure 2 Source Synchronous SMII System

Receive Path

Receive data and control information are signalled in ten bit segments. In 100MBit mode, each segment represents a new byte of data. In 10MBit mode, each segment is repeated ten times; therefore, every ten segments represents a new byte of data. The MAC can sample any one of every 10 segments in 10MBit mode.

Segment boundaries are delimited by SYNC. The MAC continuously generates a pulse on SYNC every 10 clocks.

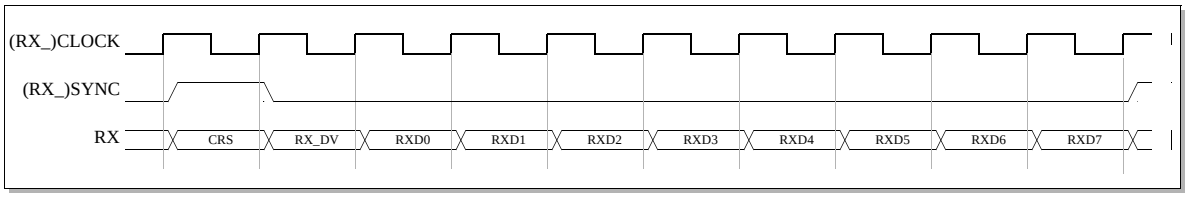

figure 3 Receive Sequence Diagram

RX contains all of the information found on the receive path of the standard MII.

Bit	Purpose
CRS	Carrier Sense - identical to MII, except that it is not an asynchronous signal
RX_DV	Receive Data Valid - identical to MII
RXD7-0	Encoded Data, see Table 4

table 3 RX - Bit Description

RXD7-0 are used to convey packet data, RX_ER, and PHY status. The MAC can infer the meaning of RXD on a segment by segment basis by decoding the two control bits.

CRS	RX_DV	RXD0	RXD1	RXD2	RXD3	RXD4	RXD5	RXD6	RXD7
x	0	RX_ER from previous frame	Speed 0 = 10MBit 1 = 100MBit	Duplex 0 = Half 1 = Full	Link 0 = Down 1 = Up	Jabber 0 = OK 1 = Error	Upper Nibble 0 = invalid 1 = valid	False Carrier Detected	1
x	1	One Data Byte (Two MII Data Nibbles)							

table 4 RXD7-0 Encoding

Inter-frame status bit RXD5 conveys the validity of the upper nibble of the last byte of the previous frame. Inter-frame status bit RXD0 indicates whether or not the PHY detected an error somewhere in the previous frame. Both of these bits should be valid in the segment immediately following a frame, and should stay valid until the first data segment of the next frame begins.

When asserted, inter-frame status bit RXD6 indicates that the PHY has detected a false carrier event.

In order to send receive data to the MAC synchronous to the reference clock, the PHY must pass the data through an elasticity FIFO to handle any difference between the reference clock rate and the clock rate at the packet source. The Ethernet specification calls for packet data to be referenced to a clock with a frequency tolerance of 100ppm (0.01%); however, it is not uncommon to encounter Ethernet stations with clocks that have frequency errors up to 0.1%. Therefore the elasticity FIFO should be at least 27 bits[1] long, filling to the half way point before beginning valid data transfer via RX. RX_ER should be asserted if, during the reception of a frame, this fifo overflows or underflows.

Only RXD and RX_DV should be passed through the elasticity FIFO. CRS should not be passed through the elasticity FIFO. Instead, CRS should be asserted for the time the ‘wire’ is busy receiving a frame.

Transmit Path

Transmit data and control information are signalled in ten bit segments, just like the receive path. In 100MBit mode, each segment represents a new byte of data. In 10MBit mode each segment is repeated ten times; therefore, every ten segments represents a new byte of data. The PHY can sample any one of every 10 segments in 10MBit mode.

Segment boundaries are delimited by SYNC. The MAC continuously generates a pulse on SYNC every 10 clocks.

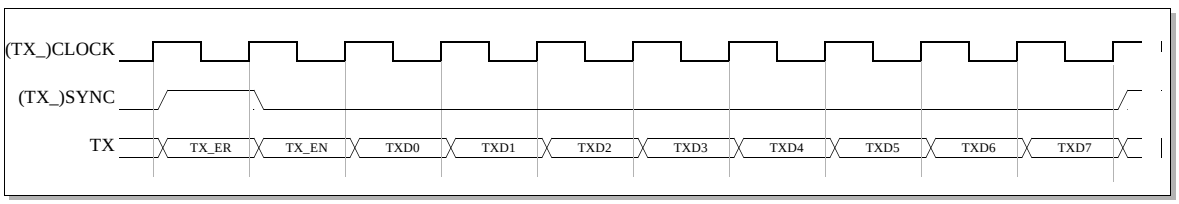

figure 4 Transmit Sequence Diagram

1. # of bits = 2 * (max frame in bits) * (end station error + our error) = 2 * (1518*8) * (0.1% + 0.01%) = 26.7 bits

TX contains all of the information found on the transmit path of the standard MII.

Bit	Purpose
TX_EN	Transmit Enable - identical to MIl
TX_ER	Transmit Error - identical to MII
TXD7-0	Encoded Data - see Table 6

table 5 TX - Bit Description

As far as the PHY is concerned, TXD7-0 are used to convey only packet data. To allow for a direct MAC to MAC connection, the MAC uses TXD7-0 to signal ‘status’ in between frames.

TX_ER	TX_EN	TXD0	TXD1	TXD2	TXD3	TXD4	TXD7-5
x	0	Use to force an error in a direct MAC to MAC connection	1 100MBit	1 Full Duplex	1 Link Up	0 No Jabber	1
x	1	One Data Byte (Two MII Data Nibbles)					

table 6 TXD7-0 Encoding

Collision Detection

Collisions occur when CRS and TX_EN are simultaneously asserted. For this to work, the PHY must ensure that CRS is not affected by its transmit path.

DC Specification

Parameter	Symbol	Min	Max	Units
Input High Voltage	Vih	2.0		volts
Input Low Voltage	Vil		0.8	volts
Input High Current	Iih	-10	10	µA
Input Low Current	Iil	-10	10	µA

table 7 DC Specification

Timing Specification

Traditional Interface

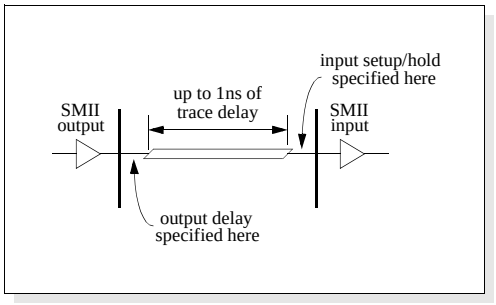

figure 5 SMII System Timing Topology

These parameters are specified with respect to CLOCK.

Parameter	Min	Max	Units
Input Setup	1.5		ns
Input Hold	1		ns
Output Delay	1.5	5	ns

table 8 Timing Specification

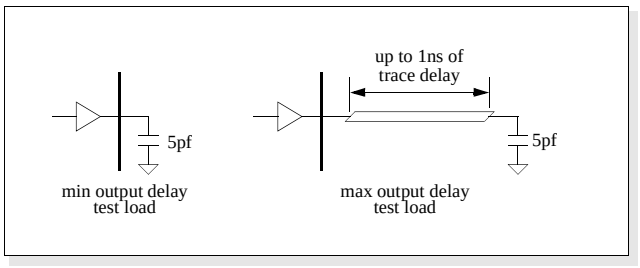

figure 6 Traditional Interface Test Loads

Source Synchronous Interface

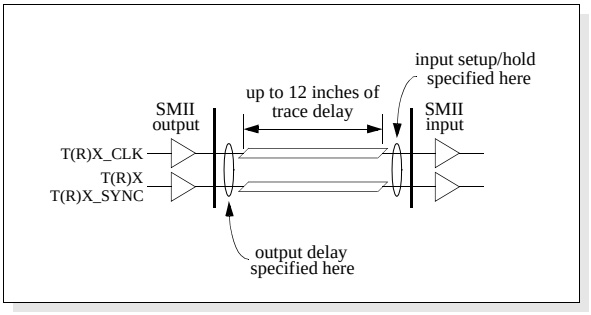

figure 7 Source Synchronous SMII System Timing Topology

These parameters are specified with respect to T(R)X_CLK

Parameter	Min	Max	Units
Input Setup	1.5		ns
Input Hold	1		ns
Output Delay[a]	1.5	5	ns

table 9 Timing Specification

a. Output delays are specified with test load #1 and #2.

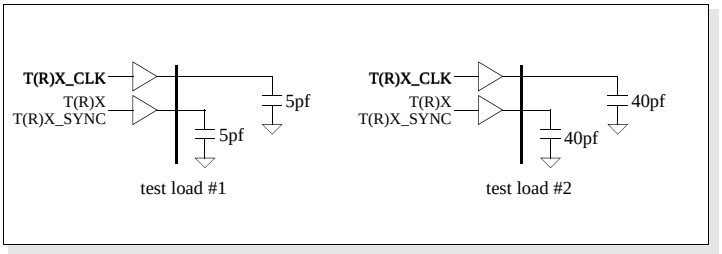

figure 8 Source Synchronous Interface Test Loads