CoreTSN User Guide

Introduction (Ask a Question)

The Microchip FPGA CoreTSN core, compliant with IEEE® 802.1Q standards, is engineered to support Time-Sensitive Networking (TSN) operations over 1 Gbps Ethernet. TSN is a Layer 2 technology, and the IEEE 802.1Q standards operate at OSI Layer 2. It leverages Precision Time Protocol (PTP) hardware timestamps, as per IEEE 1588, to synchronize network clocks. With PTP's hardware timestamps and associated protocol, jitter error can be reduced from microseconds to tens or hundreds of nanoseconds.

A VLAN packet is an Ethernet frame tagged with VLAN information, including a Priority Code Point (PCP) and VLAN ID, which are used for service differentiation. The destination MAC address can also be utilized for service differentiation. A PTP packet is used for time synchronization across the network, which is essential for coordinating time-sensitive operations. The TSN IP core typically has multiple transmission queues, each configured for a different priority level. Based on the stream IDs configured for the queues, the TSN IP places the packet into the corresponding queue. High-priority packets are placed in queues that are serviced more frequently or have a higher bandwidth allocation, ensuring that these packets are transmitted with lower latency.

The PTP protocol time stamping is managed by the Core1588 IP and is not included within the TSN IP. The TSN IP interfaces with the Core1588 IP, which subsequently interfaces with the CoreSGMII IP (also not part of the TSN IP) to provide a complete TSN solution. This core is developed specifically for PolarFire® and PolarFire SoC devices.

Summary

Core Version	This document applies to CoreTSN v3.0.
Supported Device Families	• PolarFire® • PolarFire SoC
Supported Tool Flow	Requires Libero® SoC v12.6 or later releases
Supported Interfaces	**AXI4-Stream**: • AXI4-Stream target interface to receive stream data from the external initiator • AXI4-Stream initiator interface to transmit data to external target **APB Interface**: Dedicated APB target interface for register configuration
Licensing	CoreTSN is license locked and paid. • **Evaluation**: The evaluation version is available with obfuscated and encrypted Verilog/VHDL RTL with self-destruct logic. This version provides approximately eight hours of functionality on silicon. Evaluation version is not license locked and is available for free. • **Obfuscated**: The obfuscated version is available with obfuscated and encrypted Verilog/VHDL RTL. It supports unlimited functionality on silicon. The obfuscated version will be license locked. You must purchase this license separately.
Installation Instructions	CoreTSN must be installed to the IP Catalog of Libero SoC automatically through the update function. Alternatively, CoreTSN could be manually downloaded from the catalog. Once the IP core is installed, it is configured, generated, and instantiated within SmartDesign for inclusion in the project.
Device Utilization and Performance	A summary of utilization and performance information for CoreTSN is listed in the Device Utilization and Performance section.

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1. Features (Ask a Question)

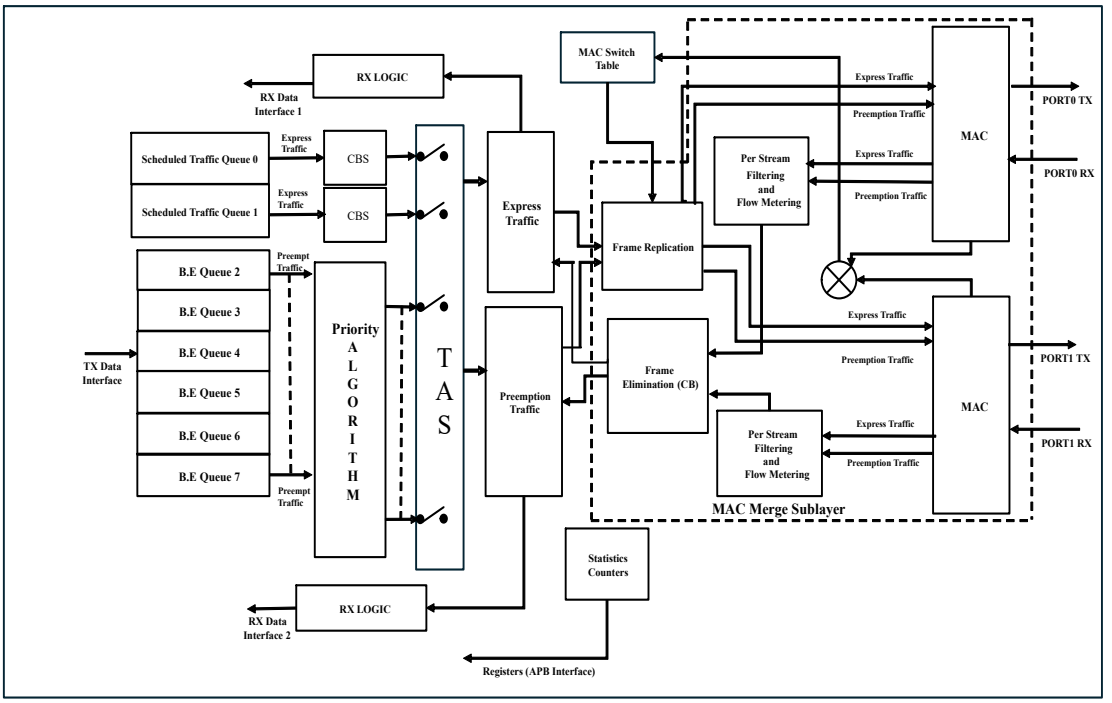
CoreTSN supports the following features:

- Supports AXI4-Stream interface at host side to access Tx, Rx packet interface.
- Gigabit Media-Independent Interface (GMII) support at the line side
- Supports Programmable Priority Queues (max 8), 16 Stream ID's which are distributed as 2 Stream ID's per Queue.
- Frame Scheduling as per IEEE 802.1 Qbv and IEEE 802.1 Qav (credit-based shaper).
- Frame Preemption as per IEEE 802.1Qbu for efficient traffic management
- Frame Replication and Elimination as per IEEE 802.1 CB
- Per-Stream Filtering and Policing as per IEEE 802.1Qci for enhanced traffic control and management
- Supports IEEE 802.1AS Precision Time Protocol (PTP) packet pass through this core.
- Supports Advanced Peripheral Bus (APB) register interface for the register configuration
- Supports Management Data Input/Output (MDIO) interface for the PHY configuration
- Medium Access Control (MAC) support as per IEEE 802.3
- MAC table support with up to 16 entries to route the egress traffic to the corresponding port

2. Functional Description (Ask a Question)

The following figure shows the top-level block diagram of the CoreTSN IP.

Figure 2-1. Functional Block Diagram



CoreTSN module has the following interfaces:

- AXI4-Stream interface
  - TX Data interface
  - RX Data interface1
  - RX Data interface2
- Priority Queues
- Traffic Scheduling
  - Credit-based Shaper
  - Time Aware Scheduler
- MAC Merge Sub-Layer (MMS)
  - Transmission data path
    - Frame Replication
  - Receive data path
    - Per Stream Filtering and Policing
    - Frame Elimination
- Register interface
- Statistics Counter
- MAC Switch table
- MDIO interface

2.1. AXI-Stream Interface (Ask a Question)

The IP supports AXI-Stream interface at the system side and consists of the following interfaces:

- TX Data Interface (AXI Target Interface): The IP has one stream interface on the TX side. The AXI-Stream target interface on the transmit side is controlled by the processor/Fabric. It handles the scheduling of the TSN, PTP, and the best-effort data packets. The preemption feature can be enabled for the best-effort traffic to effectively utilize the available bandwidth.
- RX Data Interface1 (AXI Initiator Interface): On the receive side of the IP, there are two AXI-Stream initiator interfaces. The RX data interface1 outputs the Express packets received on port0 and port 1 of the TSN IP. This output can be routed to the MSS or handled within the fabric.
- RX Data Interface2 (AXI Initiator Interface): The RX data interface2 outputs the preempted traffic received on both RX ports. This interface outputs best-effort traffic to the Fabric/MSS.

The timing diagram for the data expected to be on TX Data interface is specified in Figure 4-6. The timing diagram that the IP provides to the client on AXI-Stream interfaces S0 and S1 is specified in Figure 4-7.

2.2. Priority Queues (Ask a Question)

There are eight priority queues implemented in the TSN IP.

1. Stream IDs are used to classify transmit traffic into these queues. Each Stream ID is defined by a combination of:
   - Destination Address (DA)
   - VLAN Identifier (VID)
   - Priority Code Point (PCP)

   These parameters can be masked using the StreamIDx_Mask register, allowing flexible matching criteria.
2. Stream ID Configuration:
   - Two Stream ID configurations are supported for each queue.
   - Total Stream IDs: 16 (2 per queue × 8 queues)
   - The software can configure these Stream IDs to match specific traffic flows.
3. Packet Classification and Queue Assignment:
   When a packet arrives, following are the conditions to be checked:
   - Its DA, VID, and PCP are compared against the configured Stream IDs for all queues.
   - If a match is found, the packet is placed in the corresponding queue (based on priority).
   - If no match is found, the packet is placed in the lowest priority queue (QUEUE7).
   - PTP packets are assigned to the highest priority queue (QUEUE0).

2.3. Traffic Scheduling (Ask a Question)

When the TAS is not enabled in the TSN IP, packets are processed from the queues sequentially, starting from Queue0 (highest priority) to Queue7 (lowest priority). The traffic in Queue0 and Queue1 is treated as priority traffic and is transmitted as express traffic. This ensures low-latency and high reliability for time-sensitive applications. The traffic from Queue2 through Queue7 is classified as best-effort traffic, suitable for less critical data transfers. If the preemption feature is enabled, best-effort traffic from these queues becomes eligible for fragmentation. This allows express traffic to preempt ongoing transmissions and further guarantees timely delivery for high-priority streams. This mechanism provides a clear separation between critical and non-critical traffic, supporting deterministic communication for time-sensitive networking scenarios.

2.3.1. Credit Based Shaper (Ask a Question)

Credit-Based Shaping (CBS) is applied to traffic from Queue0 and Queue1 in accordance with the IEEE 802.1Qav standard. The CBS mechanism for these queues can be enabled or disabled through configuration settings. The credit-based shaper is implemented as per IEEE 802.1Qav-2009, Section 8.6.8.2.

Each CBS logic instance requires the configuration of four key parameters:

- Credit Increment: This defines the rate at which credit accumulates while frames are waiting in the queue for transmission.
- Credit Decrement: This specifies the rate at which credit decreases when frames are transmitted from the queue.
- Credit Max Value: This specifies the maximum number of credits the queue can hold. The credit value of the queue does not increase beyond the configured maximum value.
- Credit Min Value: This specifies the minimum value to which the credit of the queue can be decremented. If the decremented value falls below or equals the credit minimum, the credit is held at the minimum value.

Note: The value configured for Credit Decrement and Credit Min Value is treated as negative value by the IP. If configured as 8000, it is treated as -8000 by the IP.

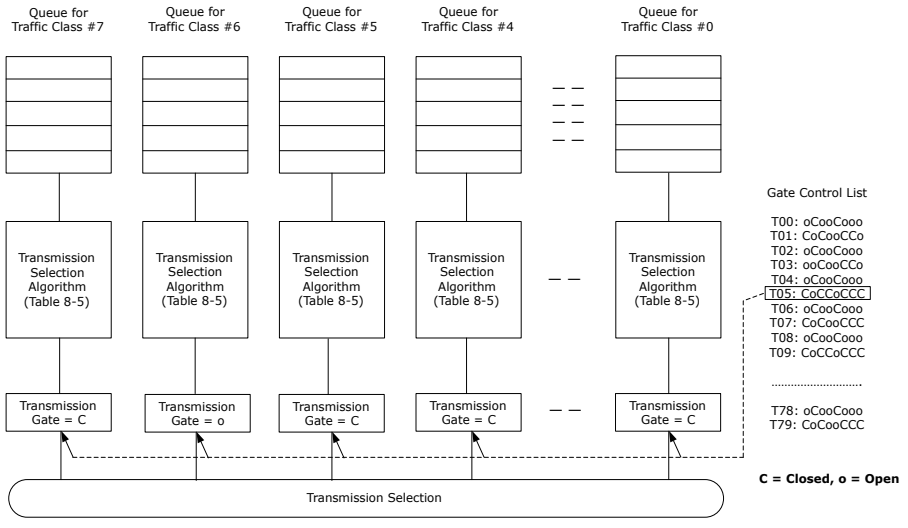
Frames are transmitted from the queue when the credit value is zero or positive, provided transmission is allowed by the Read Control Logic. The credit-based shaper ensures that traffic is regulated according to the configured credit parameters. Annex L of the IEEE 8021Qav-2009 specifies the various operational scenarios for the credit-based shaper.

2.3.2. Time Aware Shaper (Ask a Question)

The Time Aware Scheduler (TAS) is defined in IEEE 802.1Qbv. It divides the transmission into cycles, and these cycles are further divided into phases. The TAS relies on a common time base in all devices, which is provided through PTP, so each node knows when a cycle starts and which phase is active.

A gate control list associated with each port contains an ordered list of gate operations. Each gate operation changes the transmission gate state for the gate associated with each of the port's traffic class queues. The following figure shows the transmission selection using gates.

Figure 2-2. Transmission Selection using Gates

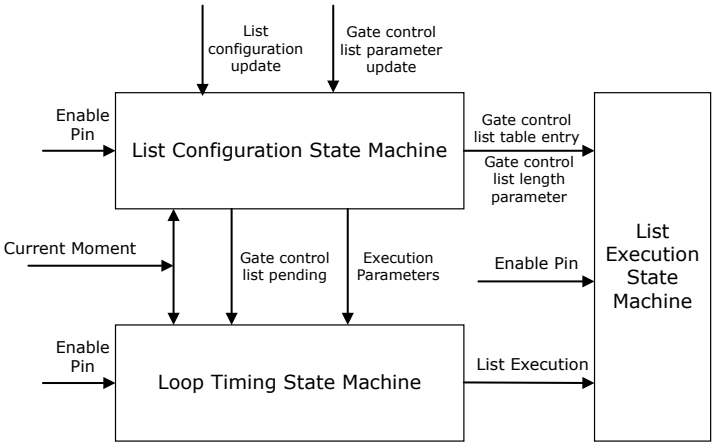


The two states in the transmission are listed as:

- Open: Queued frames are selected for transmission, in accordance with the definition of the transmission selection algorithm associated with the queue.
- Closed: Queued frames are not selected for transmission.

The following figure shows the execution of gate operations using state machine.

Figure 2-3. Traffic Scheduling State Machine



The execution of the gate operations in a ports gate control list is controlled by three state machines as listed:

1. Cycle Timer/Loop Timing state machine: This state machine initiates the execution of the gate control list and ensures that the gating cycle time defined for the Port is maintained and is implemented as per Figure 8-14 of IEEE 802.1Qbv.
   This state machine is responsible for starting the traffic scheduling process at a defined Base Time (configured through Base Time High/Low Register). The start time can be adjusted as per the requirements through the PTP Base time Adjust register. The cycle time is configured in the Scheduler Cycle Time Register. After each cycle time elapses, the state machine re-initiates the execution of the gate control list, maintaining a consistent and deterministic traffic schedule.
2. List Execute state machine: This state machine executes the gate operations in the gate control list, in sequence, and establishes the appropriate time delay between each operation and is implemented as specified by the state diagram in Figure 8-15 of IEEE 802.1Qbv.
   The TSN IP supports up to 32 gate entries. Each entry specifies:
   - Entry Execution Time: The precise time at which the gate operation should be executed.
   - Gate States for Each Queue:
     - A value of '1' indicates the corresponding queue is open (frames can be transmitted).
     - A value of '0' indicates the queue is closed (frames are blocked from transmission).

   The Scheduler Control List Length register holds the count of the valid gate entries for the current configuration.
3. List Config state machine: This state machine manages the process of updating the current active schedule. It interrupts the operation of the other two state machines during the update process. Once the new schedule is installed, it restarts the other state machine and is implemented as specified by the state diagram in Figure 8-16 of IEEE 802.1Qbv.
   To enable a new schedule, pulse the CFG_Val bit in the Gate Control List Register. This action signals the List Config State Machine to start the update process. Ensure the Gate_en signal is set high to activate traffic scheduling. If Gate_en is low, scheduling is disabled regardless of the configuration.

Note: The new configuration is applied only after the current gate control list execution completes, maintaining the integrity and predictability of traffic scheduling.

2.4. MAC Merge Sub Layer (MMS) (Ask a Question)

This section describes about the MMS module transmitter and receiver path. The major blocks of the MAC merge sublayer are Frame replication, Frame elimination, Per stream filtering & flow metering, and MAC functionality.

2.4.1. Transmission Data Path (Ask a Question)

The modules included in the transmission data path are the Frame Replication module and the MAC GMII TX block.

2.4.1.1. Frame Replication (Ask a Question)

In TSN, frame replication is standardized by IEEE 802.1CB. This standard defines how frames are replicated from both the express and preemption traffic blocks, using a predefined set of stream identifiers provided by the register module. Each egress packet is examined to determine its Stream ID. The Stream ID is determined using the Destination Address (DA) and the VLAN identifier.

The input configuration parameters are defined as follows:

- FRER Status – It is an input signal to enable or disable the FRER feature.
  - 0 – FRER block is disabled
  - 1 – FRER block is enabled
- Stream ID – The destination address, VLAN ID, FRER enable indication, and configured through register are considered for the FRER tag insertion.

2.4.1.1.1. Stream Identification (Ask a Question)

The design supports three modes for Stream ID configuration:

- DA only: The Stream ID consists of the destination MAC address.
- VLAN only: The Stream ID consists of the VLAN identifier.
- DA + VLAN: The Stream ID is a combination of the destination MAC address with the VLAN identifier.

Additionally, the system is configured to recognize up to 16 unique Stream IDs.

2.4.1.1.2. Replication Logic (Ask a Question)

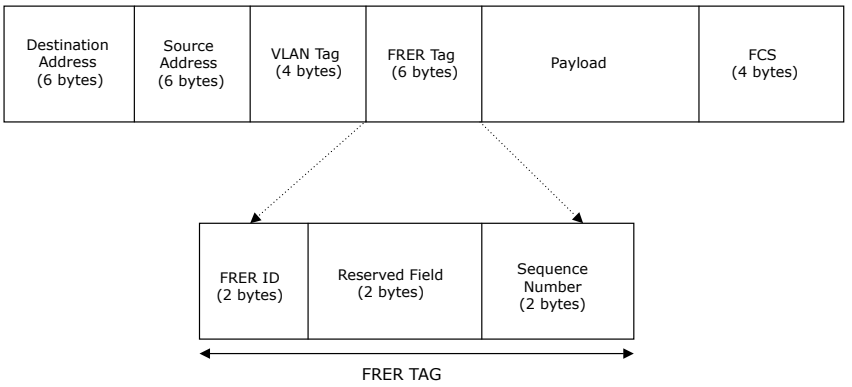
- If the Stream ID of the egress packet matches with one of the pre-configured Stream IDs:
  - The FRER logic appends an RTAG control field and a sequence number to the packet.
  - For each subsequent packet with the same Stream ID, the FRER logic increments the sequence number and appends it to the packet.
  - The packet is then replicated and transmitted through two separate ports.
- If a packet is not replicated, or if the FRER feature is disabled, it is forwarded to a port as specified by the MAC switching table.
- The PTP packets are transmitted through the port on which the PTP messages are received. Replication is not supported for PTP packets.

2.4.1.1.3. FRER Packet Structure (Ask a Question)

FRER packet structure has the following key fields:

- FRER ID: A value of 0xFFC1 in this field indicates that the packet is replicated using FRER (R-TAG).
- Reserved field: This field consists of two reserved bytes.
- Sequence number: The sequence number in the R-TAG field is a unique identifier assigned to each packet. This number helps to identify and discard the duplicate packets when multiple copies are received.

Figure 2-4. FRER Packet Structure



2.4.1.2. MAC-GMII Transmitter Block (Ask a Question)

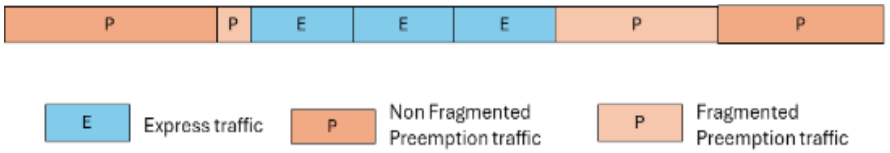
The GMII Transmitter block is a part of the MAC module, which manages egress traffic from both the express data and preemption data modules in accordance with the IEEE Std 802.3br-2016 standard.

The input configuration parameters are defined as follows:

- Preemption: Indicates whether preemption is enabled or disabled. A value of '1' enables preemption, while '0' disables the feature.
- Premp_pkt_size[2:1]: Specifies the minimum packet length that must be transmitted before fragmentation occurs.
- IFG: Defines the number of idle bytes to be inserted at the end of packet transmission.

Messages received from the express data block are transmitted immediately. If preemption traffic is being transmitted and express traffic arrives, the preemption packet is fragmented to allow the express traffic to be sent first. The preemption packet is fragmented into initial, continuation, and final packets to facilitate this process.

Figure 2-5. GMII Transmitter Block

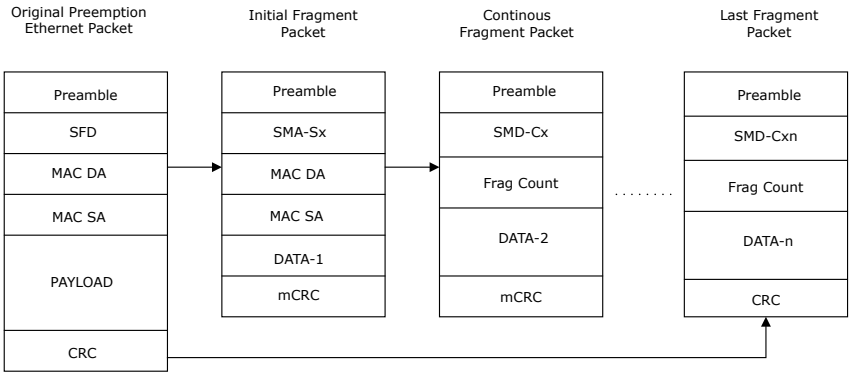


2.4.1.2.1. Frame Preemption (Ask a Question)

When the preemption feature is disabled, all traffic is treated as express traffic, and no fragmentation occurs. The transmitter can handle the following types of packets:

- A complete express packet
- A complete preemptable packet
- An initial fragment of a preemptable packet
- A continuation fragment of a preemptable packet

Figure 2-6. Frame Preemption Process



Note: The Preamble, SFD, and Frag Count values are implemented as per the section 99.3 of the IEEE Std 802.3br-2016 specification.

2.4.2. Receive Data Path (Ask a Question)

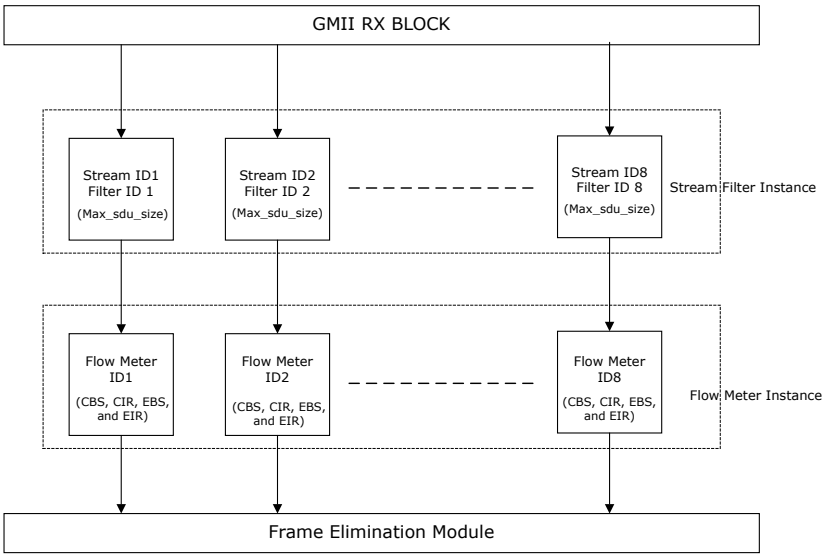
The MAC GMII Receiver block is a component of the MAC module that monitors the GMII interface for ingress Ethernet frames, differentiating between express packets and preemptable packets in accordance with the IEEE Std 802.3br™-2016 standard.

Upon receiving a preempted packet, the receiver uses fragment count and identification information from the packet headers to accurately reassemble the original packet. If the expected subsequent fragments are not received, the stored preemption data packet is discarded. The receiver performs error checking, such as CRC validation, and discards any corrupted packets. Both the received express packets and the reassembled preemption packets are then forwarded to the per-stream filtering block.

2.4.2.1. Per Stream Filtering and Policing (Ask a Question)

The functional block diagram is shown in the following figure.

Figure 2-7. Functional Block Diagram for Per-Stream Filtering and Policing



Per-Stream Filtering and Policing (PSFP) is a mechanism designed to ensure that participant streams in a TSN network adhere to the stream descriptors indicated during admission control. In a PSFP-enabled system, streams that do not adhere to the stream descriptors can be blocked entirely, or have individual violating frames dropped. The PSFP functionality is implemented as per the IEEE 802.1 Qci standard.

PSFP supports up to eight different stream ID's per port (Port0 and Port1) and respective stream filtering and flow meter parameters configurable for each stream ID. The parameters used in PSFP logic are outlined as follows:

- Stream Filtering Instance Parameters:
  - FILTERING_EN_DIS: A 1-bit input used to enable or disable SDU size filtering for the stream.
  - MAX_SDU_SIZE: A 16-bit input that defines the maximum allowed SDU (frame) size for the stream.
  - MAX_SDUSIZE_EXCEEDED: A 1-bit input. When enabled, if a frame exceeds the maximum SDU size, all subsequent frames for that stream will be dropped.
- Flow Meter Instance Parameters:
  - FLOW_METER_EN_DIS: A 1-bit input used to enable or disable flow metering for the stream.
  - Committed Information Rate (CIR): A 32-bit input specifying the guaranteed bandwidth for the stream, measured in Megabits per second (Mbps).
  - Committed Burst Size (CBS): A 11-bit input that defines the maximum burst size allowed for committed traffic, measured in Bytes.
  - Excess Information Rate (EIR): A 32-bit input specifying the additional bandwidth allowed for excess traffic, measured in Mbps.
  - Excess Burst Size (EBS): A 11-bit input that defines the maximum burst size allowed for excess traffic, measured in Bytes.
  - DROP_ON_YELLOW: A 1-bit input. If set, frames marked as yellow (excess) will be dropped rather than forwarded.

These parameters are configured for each stream ID. When the PSFP logic is enabled by setting the PSFP_Block _EN bit, each ingress frame is first identified by the stream filter instance. The identified stream is then assigned to its respective flow meter instance. The stream filtering instance maps ingress streams to one of eight stream IDs per port, based on parameters such as source address and VID value. Frames that do not match any of the stream ID parameters are forwarded to the next module without any checks. Each stream ID applies filtering based on the configured Max_SDU_size parameter. The flow meter then checks whether the frame is in-profile with respect to bandwidth parameters, including CBS, EBS, CIR, and EIR.

The PSFP block integrates two main functions for each stream:

- Per-Stream Filtering (SDU Filtering)
- Per-Stream Policing (Flow Metering)

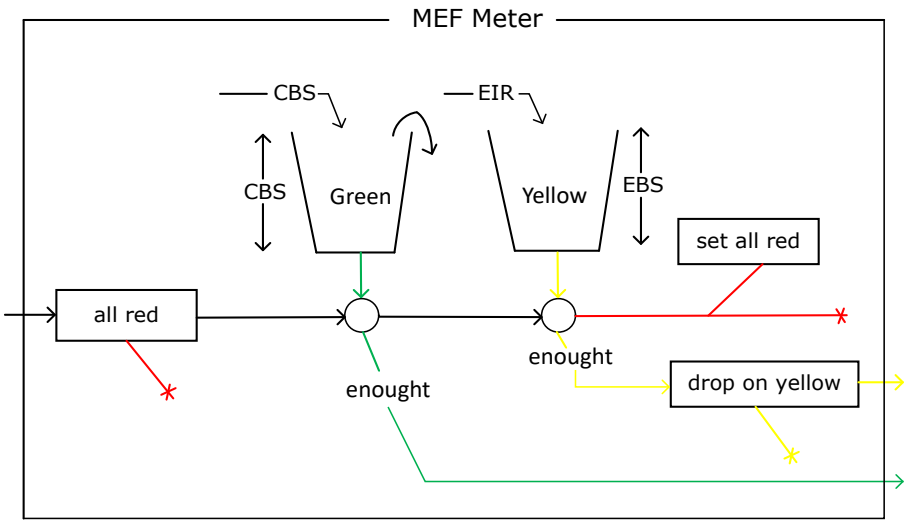
2.4.2.1.1. Per-Stream Filtering (SDU Filtering) (Ask a Question)

The following steps outline the stream filtering process performed for each ingress packet:

- Incoming packets are checked against the configured stream identification parameters (such as Source Address and VLAN ID).
- The packet size is verified to ensure it does not exceed the maximum allowed Service Data Unit (SDU) size for the stream.
- If the MAX_SDUSIZE_EXCEEDED parameter is enabled and an incoming frame exceeds the configured maximum size, then all subsequent frames from that specific stream ID will be dropped.

2.4.2.1.2. Per-Stream Policing (Flow Metering) (Ask a Question)

Figure 2-8. Token-Based Algorithm for Flow Metering



Each frame processed by the flow meter follows the sequence presented in preceding figure. During this process, frames are virtually marked as green, yellow, or red, based on the availability of tokens in the buckets. The green and yellow token buckets are replenished at the rates of CIR and EIR, with maximum capacities defined by the CBS and EBS.

If sufficient tokens are available in the green (committed) bucket, the frame is marked as green. If the green bucket does not have enough tokens, the flow meter checks the yellow (excess) bucket. If sufficient tokens are available there, the frame is marked as yellow. If neither bucket has enough tokens, the frame is marked as red and is dropped. This color classification is used to indicate the frame's compliance with the configured bandwidth parameters only within this meter sub-system and is not visible outside.

Additional flow meter functions include:

- Monitors the rate and burst size of ingress packets for each stream.
- Implements CIR, CBS, EIR, and EBS policing.
- Drops or marks packets that exceed the configured rate or burst limits, supporting color-aware policing (for example., DROP_ON_YELLOW).

Packets that pass these checks are forwarded to the Frame Elimination block for further processing.

Note: The available bandwidth for the user is 1 Gbps, when both ports are active, this bandwidth is shared between the two ports.

2.4.2.2. Frame Elimination (Ask a Question)

The Frame Replication and Elimination for Reliability (FRER) elimination block is implemented as specified in IEEE 802.1CB. It uses sequence numbers, source address, and VLAN information in the frame headers to detect and discard duplicate packets.

2.4.2.2.1. Input Configurable Parameters (Ask a Question)

MAX_STREAMID_RESET_VAL: Specifies the timeout period after which an inactive stream ID entry is cleared/released, making that table entry available for a newly received stream ID.

FRER Elimination Logic Overview:

- The Vector Recovery algorithm, recognized as the most effective FRER elimination method, is implemented in this block.

- The elimination logic captures the stream identifier from each received packet, which is defined as the combination of the Source MAC address and VLAN ID.
- For each unique stream identifier (up to a maximum of eight), the block allocates dedicated internal memory to record the sequence numbers of received packets and maintains an independent sliding window history for each stream. Each stream ID has a 32 window size, which specifies how many recent sequence numbers are tracked for duplicate detection.
- If no further packets are received for a particular stream identifier within a configurable timeout period (default value is 100ms), the associated memory is automatically released, making those resources available for newly detected RTAG-based streams.
- For packets that are not RTAG-based, or when the number of unique stream identifiers exceeds the supported limit of eight and a new stream identifier is detected, elimination is not performed on those packets.
- The elimination logic processes both express and pre-emption packets, routing them to the corresponding system interfaces.
- Before processing non-eliminated RTAG packets, the FRER RTAG header is removed.

2.5. MDIO Interface (Ask a Question)

The PHY communicates control and status information through a two-wire MDIO management interface detailed in *IEEE802.3u Clause 22*.

The MDIO write/read cycles are initiated through the APB target. During a write cycle, the MAC uses the MDIO_PHYID, register address, and 16-bit write data. For a read cycle, the MAC uses the MDIO_PHYID register address and updates the sixteen-bit read data into the MDIO Management STATUS Register, which can be accessed through the APB target.

2.6. Register Interface (Ask a Question)

The core has APB interface to configure the registers of the TSN, and the MAC_CONFIG registers. The details of the each register is provided in the Register Map and Descriptions section.

2.7. Statistics Counter (Ask a Question)

The TSN IP includes a comprehensive set of statistics counters that log and monitor various feature-specific statistics. These counters provide valuable insights into the operation and performance of the TSN features, aiding in diagnostics and monitoring.

For information about specific registers and their detailed descriptions, see register description section. All statistics registers are designed with a clear on read mechanism. When a register is read, its value is returned, and the register is then cleared (reset to zero).

2.8. MAC Switch Table (Ask a Question)

This module is responsible for directing egress packets to the appropriate output ports (port0 and port1) using MAC address learning and forwarding logic. It dynamically learns and makes the forwarding decisions.

This module has two main functions:

- Learning: The switch table supports a total of 16 entries shared between port0 and port1. When a packet arrives at either Rx port (port0 or port1), the module captures the source MAC address and the port number. This data is stored in the table, marking the entry as valid. Each entry remains valid until it times out. The default timeout is 1 second, is configurable through the SWITCH_PORT_TABLE_TIMEOUT register. Once a table entry times out, it becomes available for new entries.
- Packet Forwarding: When a packet is ready for transmission, its destination MAC address is compared with the entries in the switch table. If a match is found, the packet is forwarded to the corresponding port. Packets with an RTAG field are sent to both ports, ensuring redundancy or broadcast as required. If the destination address does not match with any valid table entry, the

packet is transmitted on both ports (flooding), ensuring delivery even if the address is not yet learned.

3. IP Core Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the CoreTSN Configurator settings and I/O signals.

3.1. Configuration Parameters (Ask a Question)

The following table lists the configurable options for CoreTSN. Configure the CoreTSN using the configuration window in the SmartDesign.

Important: The "Name" column in the following table shows the actual parameter names used in RTL. The "Description" column starts with the parameter names as they appear in the CoreTSN configurator.

Table 3-1. Configuration Parameters of CoreTSN

Name	Valid Values	Default	Description
PSFP	0–1	0	This parameter is used to enable/disable the PSFP feature. • 0: Disable • 1: Enable

3.2. Inputs and Outputs Signals (Ask a Question)

The following table lists the input and output signals and their description.

Table 3-2. Input and Output Signals

Port Name	Width	Direction	Clock Domain	Description
Clock Ports				
AXI_S0_CLK	1	Input	—	**AXI-Stream interface1** This clock is used for TX Data interface and Rx Data interface1
AXI_S1_CLK	1	Input	—	**AXI-Stream interface2** This clock is used for RX Data interface 2
PCLK	1	Input	—	**APB Clock**
MAC_TX_CLK	1	Input	—	**MAC Transmit Core Clock** This clock is used for the MAC TX PKT, on the line side.
MAC_RX_CLK	1	Input	—	**MAC Receive Core Clock** This clock is used for the MAC RX PKT, on the line side.
MAC_SYS_CLK	1	Input	—	**System Clock** This clock is used for the system side of the MAC interface
Reset Ports				
AXI_S0_RESETN	1	Input	Asynchronous	Active-Low asynchronous reset for the AXI-Stream interface1

Table 3-2. Input and Output Signals (continued)

Port Name	Width	Direction	Clock Domain	Description
MAC_SYS_CLK_RSTN	1	Input	Asynchronous	Active-Low asynchronous reset for the MAC system side interface
PRESETN	1	Input	Asynchronous	Active-Low asynchronous reset for the APB interface
AXI_S1_RESETN	1	Input	Asynchronous	Active-Low asynchronous reset for the AXI-Stream interface2
RD_RESET_FIFO_N	8	Input	Asynchronous	FIFO read reset
WR_RESET_FIFO_N	8	Input	Asynchronous	FIFO write reset
MAC_RST_N	1	Input	Asynchronous	MAC/MMS reset
APB Interface Ports				
APB_SLAVE_PADDR	32	Input	PCLK	APB address bus
APB_SLAVE_PENABLE	1	Input	PCLK	APB enable
APB_SLAVE_PSEL	1	Input	PCLK	APB target select
APB_SLAVE_PWDATA	32	Input	PCLK	APB write data
APB_SLAVE_PWRITE	1	Input	PCLK	1: APB write 0: APB read
APB_SLAVE_PRDATA	32	Output	PCLK	APB read data
APB_SLAVE_PREADY	1	Output	PCLK	APB ready signal
APB_SLAVE_PSLVERR	1	Output	PCLK	APB error signal to indicate the failure of transfer
AXI4-Stream Interface1				
AXI4-Stream Target Transaction				
AXI4S0_I_AXI4S_TDATA	32	Input	AXI_S0_CLK	AXI4-Stream data is the primary payload that provides the data that is passing across the interface
AXI4S0_I_AXI4S_TKEEP	4	Input	AXI_S0_CLK	AXI4-Stream byte qualifier that indicates whether the content of the associated byte of data is processed as part of the data stream. Associated bytes that have the TKEEP byte qualifier de-asserted are null bytes and are removed from the data stream.
AXI4S0_I_AXI4S_TLAST	1	Input	AXI_S0_CLK	AXI4-Stream last indicates the boundary of a packet
AXI4S0_I_AXI4S_TUSER	1	Input	AXI_S0_CLK	AXI4-Stream target user defined sideband information that are transmitted alongside the data stream. Not used in IP

Table 3-2. Input and Output Signals (continued)

Port Name	Width	Direction	Clock Domain	Description
AXI4S0_I_AXI4S_TVALID	1	Input	AXI_S0_CLK	AXI4-Stream valid indicates that the initiator is driving a valid transfer
AXI4S0_O_AXI4S_TREADY	1	Output	AXI_S0_CLK	AXI4-Stream ready indicates that the target accepts a transfer in the current cycle
AXI4-Stream Initiator Transaction				
AXI4S0_O_AXI4S_TDATA	32	Output	AXI_S0_CLK	AXI4-Stream data is the primary payload that provides the data that is passing across the interface
AXI4S0_O_AXI4S_TKEEP	4	Output	AXI_S0_CLK	AXI4-Stream byte qualifier that indicates whether the content of the associated byte of data is processed as part of the data stream. Associated bytes that have the TKEEP byte qualifier de-asserted are null bytes and are removed from the data stream
AXI4S0_O_AXI4S_TLAST	1	Output	AXI_S0_CLK	AXI4-Stream last indicates the boundary of a packet
AXI4S0_I_AXI4S_TREADY	1	Input	AXI_S0_CLK	AXI4-Stream ready indicates that the target accepts a transfer in the current cycle
AXI4S0_O_AXI4S_TUSER	1	Output	AXI_S0_CLK	AXI4-Stream target user defined sideband information that can be transmitted alongside the data stream Tied to 0
AXI4S0_O_AXI4S_TVALID	1	Output	AXI_S0_CLK	AXI4-Stream valid indicates that the initiator is driving a valid transfer
AXI4-Stream Interface2				
AXI4-Stream Initiator Interface				
AXI4S1_O_AXI4S_TDATA	32	Output	AXI_S1_CLK	AXI4-Stream data is the primary payload that provides the data that is passing across the interface

Table 3-2. Input and Output Signals (continued)

Port Name	Width	Direction	Clock Domain	Description
AXI4S1_O_AXI4S_TKEEP	4	Output	AXI_S1_CLK	AXI4-Stream byte qualifier that indicates whether the content of the associated byte of data is processed as part of the data stream. Associated bytes that have the TKEEP byte qualifier de-asserted are null bytes and are removed from the data stream
AXI4S1_O_AXI4S_TLAST	1	Output	AXI_S1_CLK	AXI4-Stream last indicates the boundary of a packet
AXI4S0_I_AXI4S_TREADY	1	Input	AXI_S1_CLK	AXI4-Stream ready indicates that the target accepts a transfer in the current cycle
AXI4S1_O_AXI4S_TUSER	1	Output	AXI_S1_CLK	AXI4-Stream target user defined sideband information that are transmitted alongside the data stream Tied to 0
AXI4S1_O_AXI4S_TVALID	1	Output	AXI_S1_CLK	AXI4-Stream valid indicates that the initiator is driving a valid transfer
GMII Inputs/Outputs				
Port0				
MII_COL_N_0	1	Input	MAC_RX_CLK	GMII collision detect flag
MII_CRS_IN_0	—	Input	MAC_RX_CLK	GMII carrier sense flag
MII_RXDV_IN_0	1	Input	MAC_RX_CLK	Receive data valid
MII_RXD_IN_0	8	Input	MAC_RX_CLK	Receive data used for GMII 1000 Mbps
MII_RXER_IN_0	1	Input	MAC_RX_CLK	Receive error
MII_TXD_OUT_0	8	Output	MAC_TX_CLK	Transmit data used for GMII 1000 Mbps
MII_TXEN_OUT_0	1	Output	MAC_TX_CLK	Transmit enable
MII_TXER_OUT_0	1	Output	MAC_TX_CLK	Transmit error
Port1				
MII_COL_N_1	1	Input	MAC_RX_CLK	GMII collision detect flag
MII_CRS_IN_1	—	Input	MAC_RX_CLK	GMII carrier sense flag
MII_RXDV_IN_1	1	Input	MAC_RX_CLK	Receive data valid
MII_RXD_IN_1	8	Input	MAC_RX_CLK	Receive data used for GMII 1000 Mbps
MII_RXER_IN_1	1	Input	MAC_RX_CLK	Receive error
MII_TXD_OUT_1	8	Output	MAC_TX_CLK	Transmit data used for GMII 1000 Mbps
MII_TXEN_OUT_1	1	Output	MAC_TX_CLK	Transmit enable

Table 3-2. Input and Output Signals (continued)

Port Name	Width	Direction	Clock Domain	Description
MII_TXER_OUT_1	1	Output	MAC_TX_CLK	Transmit error
MDIO Signals				
MDO	1	Output	MDC	MDIO management data output
MDOEN	1	Output	MDC	MDIO management data output enable
MDI	1	Input	MDC	MDIO management data input from pad
MDC	1	output	MDC	MDIO management data clock
PTP-related Ports				
BASE_TIME_1588	78	Input	Asynchronous	PTP counter value
PTP_PORT	2	Output	MAC_RX_CLK	PTP packets received port • Port1 – 01 • Port0 – 10

4. Timing Diagrams (Ask a Question)

This section discusses various timing diagrams.

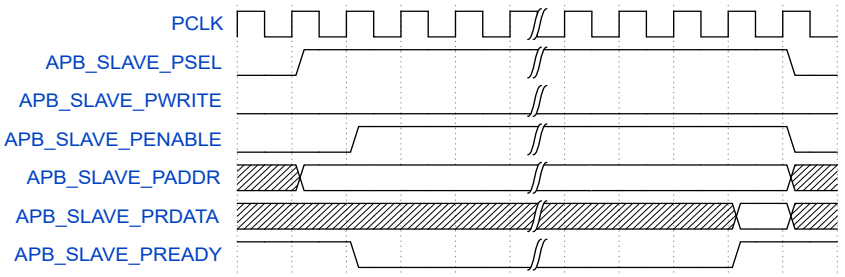
4.1. APB Interface (Ask a Question)

This section describes about the APB Read timing and APB write timing.

4.1.1. APB Read Timing (Ask a Question)

The following figure shows the timing diagram for an APB read access.

Figure 4-1. APB Read Timing Diagram



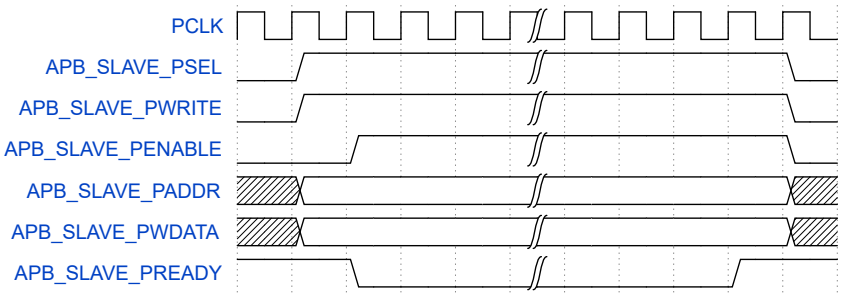
The APB read transfer begins when APB_SLAVE_PADDR, APB_SLAVE_PWRITE, and APB_SLAVE_PSEL change after the rising edge of PCLK. The first clock cycle of the transfer is known as the setup phase. After the subsequent clock edge, APB_SLAVE_PENABLE is asserted, and APB_SLAVE_PREADY is de-asserted, indicating that the access phase is underway. Throughout the access phase, APB_SLAVE_PADDR, APB_SLAVE_PWRITE, APB_SLAVE_PSEL, and APB_SLAVE_PENABLE remain valid. The transfer is completed at the end of the cycle when APB_SLAVE_PREADY is asserted. During this cycle, APB_SLAVE_PRDATA is valid. At the end of the transfer, APB_SLAVE_PENABLE is de-asserted.

Additionally, APB_SLAVE_PSEL goes low unless the transfer is immediately followed by another transfer to the same peripheral.

4.1.2. APB Write Timing (Ask a Question)

The following figure shows the timing diagram for an APB write access.

Figure 4-2. APB Write Timing Diagram



The APB write transfer begins when APB_SLAVE_PADDR, APB_SLAVE_PWDATA,APB_SLAVE_PWRITE, and APB_SLAVE_PSEL change after the rising edge of PCLK. The first clock cycle of the transfer is known as the setup phase. After the subsequent clock edge, the APB_SLAVE_PENABLE is asserted, and APB_SLAVE_PREADY is de-asserted, indicating that the access phase is underway. Throughout the access phase, APB_SLAVE_PADDR, APB_SLAVE_PWDATA, APB_SLAVE_PWRITE, APB_SLAVE_PSEL, and APB_SLAVE_PENABLE all remain valid. The transfer completes at the end of the cycle where APB_SLAVE_PREADY is asserted. PENABLE is de-asserted at the end of the transfer.

Additionally, APB_SLAVE_PSEL goes low unless the transfer is immediately followed by another transfer to the same peripheral.

4.2. Ethernet Frame Structure (Ask a Question)

Figure 4-3. Traditional Ethernet Data Frame

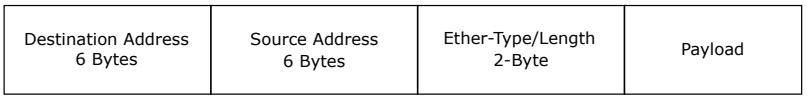
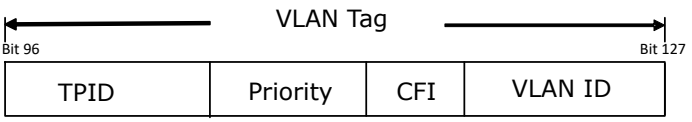


Figure 4-4. VLAN Data Frame

The following are the fields of the data frame:

- **Destination Address**: This field is 6 bytes long. It contains the MAC address of the destination device. MAC address is 48 bits (6 bytes) in length. For convenience, usually, it is written as 12-digit hexadecimal numbers. As we are using 32-bit data bus the first four bytes considering D5 as MSB byte and D0 as LSB byte which are received first are as D2 D3 D4 D5 from MSB to LSB and next four bytes contain the 2 bytes each of Destination address and source address as S4 S5 D0 D1(MSB to LSB).
- **Source Address**: This field is also 6 bytes long. It contains the MAC address of the source device. For 32-bit data bus, first 2 words S4 S5 are received first and next 4 bytes are S0 S1 S2 S3(MSB to LSB).
- **Ether-Type/Length**: In the 802.3 Ethernet header, a Length field specifies the size of the payload in bytes. Meanwhile, the Ethernet II header includes an Ether-Type field, identifying the upper layer protocol such as IP (0x0800) or ARP (0x0806). Each field is two bytes in size.
- **Virtual Local Area Network (VLAN) Tag**:
  The following figure shows the structure of VLAN tag.

  Figure 4-5. VLAN Tag Structure



  The fields of a VLAN tag are as follows:
  - **Tag Protocol Identifier (TPID)**: The 16-bit TPID field indicates whether a frame is VLAN-tagged. By default, the TPID value is 0x8100, which indicates that the frame is VLAN-tagged. Devices vendors can set the TPID to different values. To ensure compatibility with these devices, adjusting the TPID value may be necessary so that frames carry a TPID value that matches a specific vendor's requirements, enabling interoperability. The device determines whether a received frame carries a VLAN tag by checking the TPID value. If the TPID value of a frame matches the configured value or is 0x8100, the frame will be recognized as a VLAN-tagged frame.
  - **Priority**: The 3-bit priority field indicates the 802.1p priority of the frame.

- **Canonical Format Indicator (CFI)**: The CFI field, which is 1-bit in size, signifies the encapsulation format of MAC addresses during packet transmission across various media types. A CFI value of 0 indicates that the MAC addresses are encapsulated using the standard format, while a value of 1 indicates that the encapsulation in a non-standard format. The default CFI value is 0.
- **VLAN ID**: The VLAN ID field, which is 12-bit in length, specify the VLAN to which a frame is associated. The assignable VLAN ID values ranges from 1 to 4094, as the endpoints 0 and 4095 are reserved.

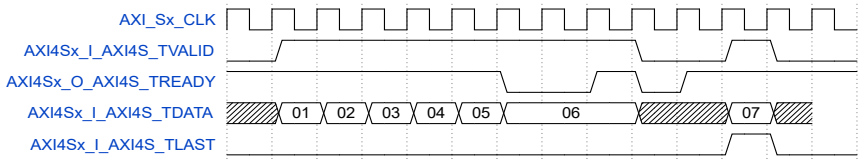
4.3. AXI4-Stream Interface (Ask a Question)

This section describes about the AXI4-Stream target interface and AXI4-Stream initiator interface.

4.3.1. AXI4-Stream Target Transaction (Ask a Question)

The following figure shows the AXI4 stream target transaction timing diagram.

Figure 4-6. AXI4 Stream Target Transaction

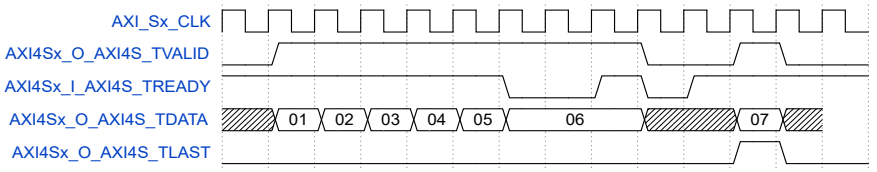


AXISx_I_AXI4S_TVALID represents the valid data on the data bus where x stands for channels if it is high, it means data is valid. AXISx_I_AXI4S_TLAST shows the last four bytes of data and AXISx_O_AXI4S_TREADY is generated from destination. Data transfer occurs only when both AXI*_TVALID and TREADY are high on the same rising clock.

4.3.2. AXI4 Stream Initiator Transaction (Ask a Question)

The following figure shows the AXI4 stream initiator transaction timing diagram.

Figure 4-7. AXI4 Stream Initiator Transaction



AXISx_O_AXI4S_TVALID represents the valid data on the data bus where x stands for channels if it is high, it means data is valid. AXISx_O_AXI4S_TLAST shows the last four bytes of data and AXI4Sx_I_AXI4S_TREADY is generated from destination.

For traditional Ethernet frame, following are the configurations listed:

- 01: Destination address higher 4 bytes (D2, D3, D4, D5)
- 02: Destination address lower 2 bytes and Source address higher 2 bytes (S4, S5, D0, D1)
- 03: Source address lower 4 bytes (S0, S1, S2, S3)
- 04: Combination of Ether-type/length and payload, where the lower 16 bits represent Ether-type/length and the higher bytes represent payload
- 05 and onwards: Payload data

For VLAN tagged Ethernet frames, following are the configurations listed:

- 01: Destination address higher 4 bytes (D2, D3, D4, D5)

- 02: Destination address lower 2 bytes and Source address higher 2 bytes (S4, S5, D0, D1)
- 03: Source address lower 4 bytes (S0, S1, S2, S3)
- 04: VLAN tag field consisting of TPID (lower 16 bits of field), priority value (next 3 bits ranging from 0 to 7), CFI, and VLAN ID (1 and 12 bit)
- 05: Combination of Ether-type/ length and payload, where lower 16 bits represents Ether-type/ length and higher bytes representing payload
- 06 and onwards: Payload data

5. Implementation of CoreTSN in Libero Design Suite (Ask a Question)

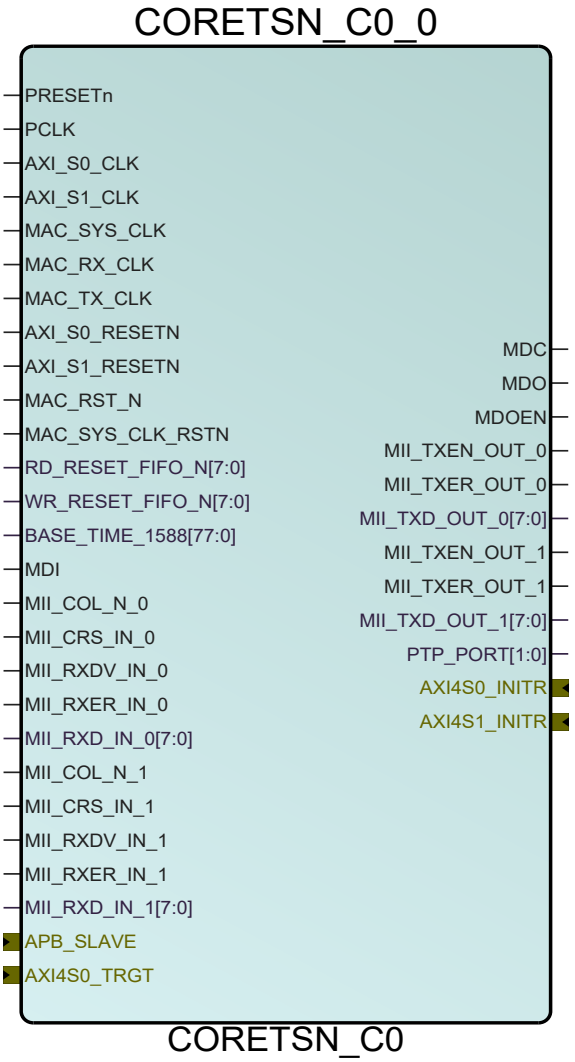
This section describes the implementation of CoreTSN in the Libero® Design Suite.

5.1. SmartDesign (Ask a Question)

CoreTSN is available for download to the SmartDesign IP Catalog through the Libero® SoC web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, see the Libero SOC online help.

The following figure shows an example of an instantiated view of CoreTSN on the SmartDesign.

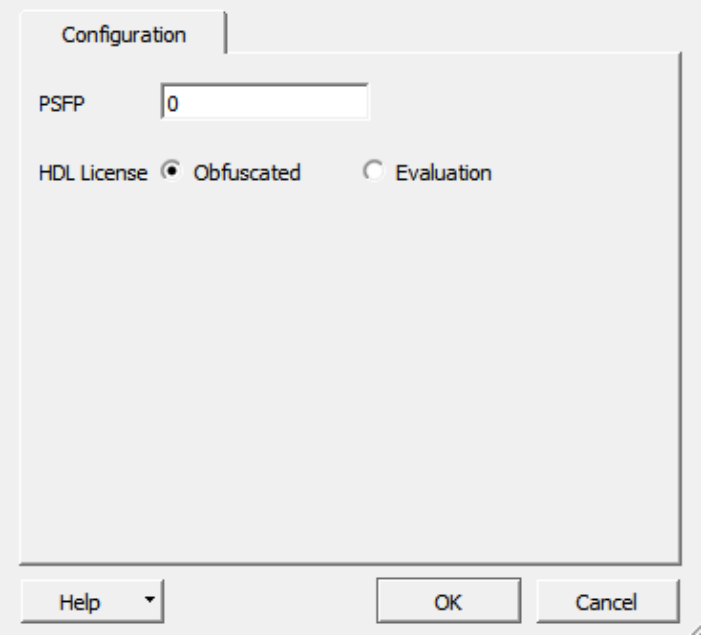
Figure 5-1. Instantiation of CoreTSN on SmartDesign for Libero SoC



5.1.1. Configuring the CoreTSN (Ask a Question)

The core is configured using the configuration GUI within SmartDesign, as shown in the following figure.

Figure 5-2. Configuration GUI



The configuration options displayed in the configuration GUI correspond with the configuration parameters listed in the Table 3-1.

5.1.2. Synthesis in Libero SoC (Ask a Question)

To run synthesis, perform the following steps:

1. Set the design root appropriately.
2. Under **Implement Design**, on the **Design Flow** tab, right-click **Synthesize** and click **Run**.

5.1.3. Place-and-Route in Libero SoC (Ask a Question)

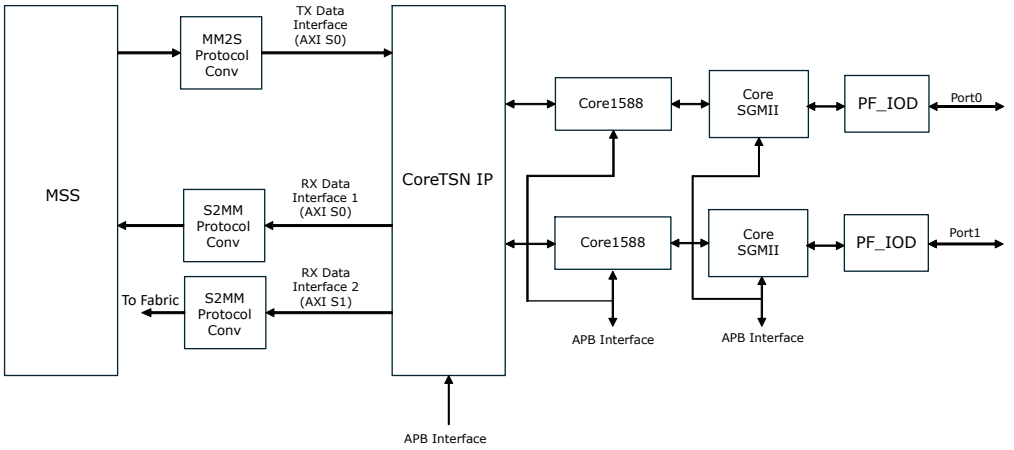
To run the place and route, perform the following steps:

Under **Implement Design**, on the **Design Flow** tab, right-click **Place and Route** and click **Run**.

5.1.4. System Integration (Ask a Question)

The following block diagram shows the integration of CoreTSN IP in the system for the 1Gbps end point application.

Figure 5-3. System Integration of CoreTSN

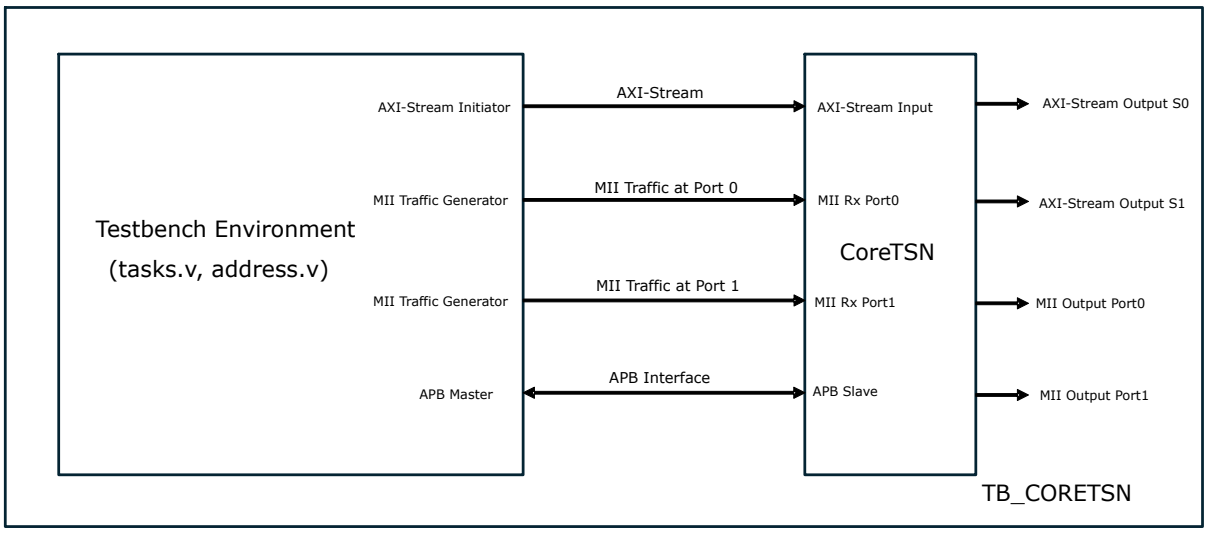


The preceding diagram shows the SGMII interface towards the line side. The GMII to SGMII conversion is performed by the CoreSGMII IP. The CoreSGMII IP is responsible for the auto negotiation with the link partner at the line side. The time synchronization needed for the TSN application is carried out by the Core1588 IP.

5.2. Verification (Ask a Question)

As a unit-level test bench is not included in this release, the following setup explains how the user can build his test bench to verify the CoreTSN IP (DUT). The environment should comprise of traffic stimulus, DUT configuration/control and observation/checking to validate correct behavior under various traffic profiles and configuration conditions. CoreTSN supports AXI-Stream at the system side and MII interface at the line side. The registers of the DUT are configured using the APB interfaces.

Figure 5-4. Verification Setup



The verification setup consists of two primary modules:

- Testbench Environment: Responsible for stimulus and control generation
- CoreTSN (Device Under Test (DUT))

All stimulus signals are generated by the Testbench Environment and sent to the CoreTSN. The outputs produced by the CoreTSN are subsequently checked or logged by the testbench.

5.2.1. AXI-Stream Initiator (Ask a Question)

The AXI-Stream Initiator generates AXI4-Stream packets to simulate traffic for CoreTSN. It drives the AXI-Stream interface with standard handshake and framing semantics (TVALID/TREADY, TDATA, TKEEP, and TLAST) to validate correct packet transfer, packet boundary handling, and frame integrity through the CoreTSN Datapath. The tasks of transmitting and receiving packets involve applying framed traffic to the AXI-Stream input and capturing and reconstructing the packets on the AXI-Stream outputs for integrity verification.

5.2.2. MII Traffic Generators (Port0 and Port1) (Ask a Question)

The MII/GMII Traffic Generators simulate Ethernet PHY behavior to inject frames into the DUT and validate ingress processing on Rx0/Rx1 and egress behavior on the corresponding output ports. The environment can generate representative Ethernet traffic types (such as, standard Ethernet, VLAN-tagged traffic, and time-synchronization profiles like PTP/gPTP). These traffic types are used to test TSN functions that depend on stream identification, priority, and filtering/policing behaviors.

To support these scenarios, the verification environment uses generalized frame construction and transmit tasks. These tasks generate complete Ethernet frames (including optional VLAN tagging fields and RTAG headers where applicable) and drive them on the GMII/MII interfaces with appropriate framing and spacing.

5.2.3. APB Master Interface (Ask a Question)

The APB Master interface acts as the configuration master for CoreTSN. It performs register reads/writes to initialize the DUT, enable/disable TSN features, and read status/statistics required for functional confirmation.

6. Register Map and Descriptions (Ask a Question)

The TSN IP has two sets of registers. Registers pertaining to MDIO interface, MAC configuration are available in the third-party IP and are described in the following CONFIG_MAC section. All the registers related to TSN operation are listed in TSN Registers.

The bits of the PADDR to select the operation for MAC registers or TSN registers are listed as follows:

- PADDR[13:12] = 2'b0 configures the TSN registers.
- PADDR[13:12] = 2'b1 configures the MAC registers.
- The lower bits, PADDR[9:0], represent the offset of the registers to be configured.
- The PADDR[11:10] are treated as xx.

Table 6-1. Abbreviations and Meanings for Register Maps

Abbreviation	Meaning
R	Read Only
R/W	Read Write
R/Wc	Read Write, Self-clearing
Rc	Clear on Read
W	Write Only

6.1. TSNREG Register Summary (Ask a Question)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	prempt_cntrl	7:0						ADDR_FLAG_SIZE[1:0]		PRE-EMPTION ENABLE / DISABLE
		15:8								
		23:16								
		31:24								
0x04 ... 0x23	Reserved									
0x24	Gate Control	7:0					GATE_EN	CFG_VAL		
		15:8								
		23:16								
		31:24								
0x28 ... 0x5F	Reserved									
0x60	Scheduler Cycle Time	7:0	SCHEDULER CYCLE TIME[7:0]							
		15:8	SCHEDULER CYCLE TIME[15:8]							
		23:16	SCHEDULER CYCLE TIME[23:16]							
		31:24	SCHEDULER CYCLE TIME[31:24]							
0x64 ... 0x6F	Reserved									
0x70	Base Time Low Register	7:0	BASE_TIME_NS[7:0]							
		15:8	BASE_TIME_NS[15:8]							
		23:16	BASE_TIME_NS[23:16]							
		31:24			BASE_TIME_NS[29:24]					
0x74	Base Time High Register0	7:0	BASE_TIME_S0[7:0]							
		15:8	BASE_TIME_S0[15:8]							
		23:16	BASE_TIME_S0[23:16]							
		31:24	BASE_TIME_S0[31:24]							
0x78	Base Time High Register1	7:0	BASE_TIME_S1[7:0]							
		15:8	BASE_TIME_S1[15:8]							
		23:16								
		31:24								
0x7C ... 0x7F	Reserved									
0x80	Gate State Control	7:0	GATE STATE Q7	GATE STATE Q6	GATE STATE Q5	GATE STATE Q4	GATE STATE Q3	GATE STATE Q2	GATE STATE Q1	GATE STATE Q0
		15:8								
		23:16								
		31:24								
0x84	Scheduler Control List Length	7:0				CTRL_LIST_LENGTH[4:0]				
		15:8								
		23:16								
		31:24								
0x88 ... 0x8B	Reserved									
0x8C	Gate Control List0 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0x90	Gate Control List1 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x94	Gate Control List2 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0x98	Gate Control List3 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0x9C	Gate Control List4 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xA0	Gate Control List5 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xA4	Gate Control List6 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xA8	Gate Control List7 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xAC	Gate Control List8 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xB0	Gate Control List9 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xB4	Gate Control List10 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xB8	Gate Control List11 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xBC	Gate Control List12 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xC0	Gate Control List13 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xC4	Gate Control List14 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xC8	Gate Control List15 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xCC	Gate Control List16 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xD0	Gate Control List17 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xD4	Gate Control List18 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xD8	Gate Control List19 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xDC	Gate Control List20 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xE0	Gate Control List21 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xE4	Gate Control List22 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xE8	Gate Control List23 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xEC	Gate Control List24 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xF0	Gate Control List25 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xF4	Gate Control List26 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xF8	Gate Control List27 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0xFC	Gate Control List28 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0x0100	Gate Control List29 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0x0104	Gate Control List30 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
0x0108	Gate Control List31 Register	7:0	TIME_INTERVAL[7:0]							
		15:8	TIME_INTERVAL[15:8]							
		23:16	TIME_INTERVAL[23:16]							
		31:24	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x010C ... 0x0117	Reserved									
0x0118	Base Time Adjust	7:0				BASE_TIME_ADJUST[4:0]				
		15:8								
		23:16								
		31:24								
0x011C	Version Register	7:0								
		15:8								
		23:16	MINOR VERSION[7:0]							
		31:24	MAJOR VERSION[7:0]							
0x0120 ... 0x015F	Reserved									
0x0160	FRER_PSFP Control	7:0							PSFP_EN	FRER_EN
		15:8								
		23:16								
		31:24								
0x0164	SID1_0_Q0	7:0	SD1_Q0_DA_LSB[7:0]							
		15:8	SD1_Q0_DA_LSB[15:8]							
		23:16	SD1_Q0_DA_LSB[23:16]							
		31:24	SD1_Q0_DA_LSB[31:24]							
0x0168	SID1_1_Q0	7:0	SD1_Q0_DA_MSB[7:0]							
		15:8	SD1_Q0_DA_MSB[15:8]							
		23:16	SD1_Q0_VID[7:0]							
		31:24	SD1_Q0_FRER_EN	SD1_Q0_PCP[2:0]			SD1_Q0_VID[11:8]			
0x016C	SID1_Mask_Q0	7:0						SD1_Q0_PCP_EN	SD1_Q0_VID_EN	SD1_Q0_DA_EN
		15:8								
		23:16								
		31:24								
0x0170	SID2_0_Q0	7:0	SD2_Q0_DA_LSB[7:0]							
		15:8	SD2_Q0_DA_LSB[15:8]							
		23:16	SD2_Q0_DA_LSB[23:16]							
		31:24	SD2_Q0_DA_LSB[31:24]							
0x0174	SID2_1_Q0	7:0	SD2_Q0_DA_MSB[7:0]							
		15:8	SD2_Q0_DA_MSB[15:8]							
		23:16	SD2_Q0_VID[7:0]							
		31:24	SD2_Q0_FRER_EN	SD2_Q0_PCP[2:0]			SD2_Q0_VID[11:8]			
0x0178	SID2_Mask_Q0	7:0						SD2_Q0_PCP_EN	SD2_Q0_VID_EN	SD2_Q0_DA_EN
		15:8								
		23:16								
		31:24								
0x017C	SID1_0_Q1	7:0	SD1_Q1_DA_LSB[7:0]							
		15:8	SD1_Q1_DA_LSB[15:8]							
		23:16	SD1_Q1_DA_LSB[23:16]							
		31:24	SD1_Q1_DA_LSB[31:24]							
0x0180	SID1_1_Q1	7:0	SD1_Q1_DA_MSB[7:0]							
		15:8	SD1_Q1_DA_MSB[15:8]							
		23:16	SD1_Q1_VID[7:0]							
		31:24	SD1_Q1_FRER_EN	SD1_Q1_PCP[2:0]			SD1_Q1_VID[11:8]			
0x0184	SID1_Mask_Q1	7:0						SD1_Q1_PCP_EN	SD1_Q1_VID_EN	SD1_Q1_DA_EN
		15:8								
		23:16								
		31:24								

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0188	SID2_0_Q1	7:0	SD2_Q1_DA_LSB[7:0]							
		15:8	SD2_Q1_DA_LSB[15:8]							
		23:16	SD2_Q1_DA_LSB[23:16]							
		31:24	SD2_Q1_DA_LSB[31:24]							
0x018C	SID2_1_Q1	7:0	SD2_Q1_DA_MSB[7:0]							
		15:8	SD2_Q1_DA_MSB[15:8]							
		23:16	SD2_Q1_VID[7:0]							
		31:24	SD2_Q1_FRER_EN	SD2_Q1_PCP[2:0]			SD2_Q1_VID[11:8]			
0x0190	SID2_Mask_Q1	7:0						SD2_Q1_PCP_EN	SD2_Q1_VID_EN	SD2_Q1_DA_EN
		15:8								
		23:16								
		31:24								
0x0194	SID1_0_Q2	7:0	SD1_Q2_DA_LSB[7:0]							
		15:8	SD1_Q2_DA_LSB[15:8]							
		23:16	SD1_Q2_DA_LSB[23:16]							
		31:24	SD1_Q2_DA_LSB[31:24]							
0x0198	SID1_1_Q2	7:0	SD1_Q2_DA_MSB[7:0]							
		15:8	SD1_Q2_DA_MSB[15:8]							
		23:16	SD1_Q2_VID[7:0]							
		31:24	SD1_Q2_FRER_EN	SD1_Q2_PCP[2:0]			SD1_Q2_VID[11:8]			
0x019C	SID1_Mask_Q2	7:0						SD1_Q2_PCP_EN	SD1_Q2_VID_EN	SD1_Q2_DA_EN
		15:8								
		23:16								
		31:24								
0x01A0	SID2_0_Q2	7:0	SD2_Q2_DA_LSB[7:0]							
		15:8	SD2_Q2_DA_LSB[15:8]							
		23:16	SD2_Q2_DA_LSB[23:16]							
		31:24	SD2_Q2_DA_LSB[31:24]							
0x01A4	SID2_1_Q2	7:0	SD2_Q2_DA_MSB[7:0]							
		15:8	SD2_Q2_DA_MSB[15:8]							
		23:16	SD2_Q2_VID[7:0]							
		31:24	SD2_Q2_FRER_EN	SD2_Q2_PCP[2:0]			SD2_Q2_VID[11:8]			
0x01A8	SID2_Mask_Q2	7:0						SD2_Q2_PCP_EN	SD2_Q2_VID_EN	SD2_Q2_DA_EN
		15:8								
		23:16								
		31:24								
0x01AC	SID1_0_Q3	7:0	SD1_Q3_DA_LSB[7:0]							
		15:8	SD1_Q3_DA_LSB[15:8]							
		23:16	SD1_Q3_DA_LSB[23:16]							
		31:24	SD1_Q3_DA_LSB[31:24]							
0x01B0	SID1_1_Q3	7:0	SD1_Q3_DA_MSB[7:0]							
		15:8	SD1_Q3_DA_MSB[15:8]							
		23:16	SD1_Q3_VID[7:0]							
		31:24	SD1_Q3_FRER_EN	SD1_Q3_PCP[2:0]			SD1_Q3_VID[11:8]			
0x01B4	SID1_Mask_Q3	7:0						SD1_Q3_PCP_EN	SD1_Q3_VID_EN	SD1_Q3_DA_EN
		15:8								
		23:16								
		31:24								
0x01B8	SID2_0_Q3	7:0	SD2_Q3_DA_LSB[7:0]							
		15:8	SD2_Q3_DA_LSB[15:8]							
		23:16	SD2_Q3_DA_LSB[23:16]							
		31:24	SD2_Q3_DA_LSB[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x01BC	SID2_1_Q3	7:0	SD2_Q3_DA_MSB[7:0]							
		15:8	SD2_Q3_DA_MSB[15:8]							
		23:16	SD2_Q3_VID[7:0]							
		31:24	SD2_Q3_FRER_EN	SD2_Q3_PCP[2:0]			SD2_Q3_VID[11:8]			
0x01C0	SID2_Mask_Q3	7:0						SD2_Q3_PCP_EN	SD2_Q3_VID_EN	SD2_Q3_DA_EN
		15:8								
		23:16								
		31:24								
0x01C4	SID1_0_Q4	7:0	SD1_Q4_DA_LSB[7:0]							
		15:8	SD1_Q4_DA_LSB[15:8]							
		23:16	SD1_Q4_DA_LSB[23:16]							
		31:24	SD1_Q4_DA_LSB[31:24]							
0x01C8	SID1_1_Q4	7:0	SD1_Q4_DA_MSB[7:0]							
		15:8	SD1_Q4_DA_MSB[15:8]							
		23:16	SD1_Q4_VID[7:0]							
		31:24	SD1_Q4_FRER_EN	SD1_Q4_PCP[2:0]			SD1_Q4_VID[11:8]			
0x01CC	SID1_Mask_Q4	7:0						SD1_Q4_PCP_EN	SD1_Q4_VID_EN	SD1_Q4_DA_EN
		15:8								
		23:16								
		31:24								
0x01D0	SID2_0_Q4	7:0	SD2_Q4_DA_LSB[7:0]							
		15:8	SD2_Q4_DA_LSB[15:8]							
		23:16	SD2_Q4_DA_LSB[23:16]							
		31:24	SD2_Q4_DA_LSB[31:24]							
0x01D4	SID2_1_Q4	7:0	SD2_Q4_DA_MSB[7:0]							
		15:8	SD2_Q4_DA_MSB[15:8]							
		23:16	SD2_Q4_VID[7:0]							
		31:24	SD2_Q4_FRER_EN	SD2_Q4_PCP[2:0]			SD2_Q4_VID[11:8]			
0x01D8	SID2_Mask_Q4	7:0						SD2_Q4_PCP_EN	SD2_Q4_VID_EN	SD2_Q4_DA_EN
		15:8								
		23:16								
		31:24								
0x01DC	SID1_0_Q5	7:0	SD1_Q5_DA_LSB[7:0]							
		15:8	SD1_Q5_DA_LSB[15:8]							
		23:16	SD1_Q5_DA_LSB[23:16]							
		31:24	SD1_Q5_DA_LSB[31:24]							
0x01E0	SID1_1_Q5	7:0	SD1_Q5_DA_MSB[7:0]							
		15:8	SD1_Q5_DA_MSB[15:8]							
		23:16	SD1_Q5_VID[7:0]							
		31:24	SD1_Q5_FRER_EN	SD1_Q5_PCP[2:0]			SD1_Q5_VID[11:8]			
0x01E4	SID1_Mask_Q5	7:0						SD1_Q5_PCP_EN	SD1_Q5_VID_EN	SD1_Q5_DA_EN
		15:8								
		23:16								
		31:24								
0x01E8	SID2_0_Q5	7:0	SD2_Q5_DA_LSB[7:0]							
		15:8	SD2_Q5_DA_LSB[15:8]							
		23:16	SD2_Q5_DA_LSB[23:16]							
		31:24	SD2_Q5_DA_LSB[31:24]							
0x01EC	SID2_1_Q5	7:0	SD2_Q5_DA_MSB[7:0]							
		15:8	SD2_Q5_DA_MSB[15:8]							
		23:16	SD2_Q5_VID[7:0]							
		31:24	SD2_Q5_FRER_EN	SD2_Q5_PCP[2:0]			SD2_Q5_VID[11:8]			

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x01F0	SID2_Mask_Q5	7:0						SD2_Q5_PCP_EN	SD2_Q5_VID_EN	SD2_Q5_DA_EN
		15:8								
		23:16								
		31:24								
0x01F4	SID1_0_Q6	7:0	SD1_Q6_DA_LSB[7:0]							
		15:8	SD1_Q6_DA_LSB[15:8]							
		23:16	SD1_Q6_DA_LSB[23:16]							
		31:24	SD1_Q6_DA_LSB[31:24]							
0x01F8	SID1_1_Q6	7:0	SD1_Q6_DA_MSB[7:0]							
		15:8	SD1_Q6_DA_MSB[15:8]							
		23:16	SD1_Q6_VID[7:0]							
		31:24	SD1_Q6_FRER_EN	SD1_Q6_PCP[2:0]			SD1_Q6_VID[11:8]			
0x01FC	SID1_Mask_Q6	7:0						SD1_Q6_PCP_EN	SD1_Q6_VID_EN	SD1_Q6_DA_EN
		15:8								
		23:16								
		31:24								
0x0200	SID2_0_Q6	7:0	SD2_Q6_DA_LSB[7:0]							
		15:8	SD2_Q6_DA_LSB[15:8]							
		23:16	SD2_Q6_DA_LSB[23:16]							
		31:24	SD2_Q6_DA_LSB[31:24]							
0x0204	SID2_1_Q6	7:0	SD2_Q6_DA_MSB[7:0]							
		15:8	SD2_Q6_DA_MSB[15:8]							
		23:16	SD2_Q6_VID[7:0]							
		31:24	SD2_Q6_FRER_EN	SD2_Q6_PCP[2:0]			SD2_Q6_VID[11:8]			
0x0208	SID2_Mask_Q6	7:0						SD2_Q6_PCP_EN	SD2_Q6_VID_EN	SD2_Q6_DA_EN
		15:8								
		23:16								
		31:24								
0x020C	SID1_0_Q7	7:0	SD1_Q7_DA_LSB[7:0]							
		15:8	SD1_Q7_DA_LSB[15:8]							
		23:16	SD1_Q7_DA_LSB[23:16]							
		31:24	SD1_Q7_DA_LSB[31:24]							
0x0210	SID1_1_Q7	7:0	SD1_Q7_DA_MSB[7:0]							
		15:8	SD1_Q7_DA_MSB[15:8]							
		23:16	SD1_Q7_VID[7:0]							
		31:24	SD1_Q7_FRER_EN	SD1_Q7_PCP[2:0]			SD1_Q7_VID[11:8]			
0x0214	SID1_Mask_Q7	7:0						SD1_Q7_PCP_EN	SD1_Q7_VID_EN	SD1_Q7_DA_EN
		15:8								
		23:16								
		31:24								
0x0218	SID2_0_Q7	7:0	SD2_Q7_DA_LSB[7:0]							
		15:8	SD2_Q7_DA_LSB[15:8]							
		23:16	SD2_Q7_DA_LSB[23:16]							
		31:24	SD2_Q7_DA_LSB[31:24]							
0x021C	SID2_1_Q7	7:0	SD2_Q7_DA_MSB[7:0]							
		15:8	SD2_Q7_DA_MSB[15:8]							
		23:16	SD2_Q7_VID[7:0]							
		31:24	SD2_Q7_FRER_EN	SD2_Q7_PCP[2:0]			SD2_Q7_VID[11:8]			
0x0220	SID2_Mask_Q7	7:0						SD2_Q7_PCP_EN	SD2_Q7_VID_EN	SD2_Q7_DA_EN
		15:8								
		23:16								
		31:24								

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0224	CBS_CTRL	7:0							CBS_EN_Q1	CBS_EN_Q0
		15:8								
		23:16								
		31:24								
0x0228	CBS_Q0	7:0	CREDIT_INCR_Q0[7:0]							
		15:8	CREDIT_INCR_Q0[15:8]							
		23:16	CREDIT_DECR_Q0[7:0]							
		31:24	CREDIT_DECR_Q0[15:8]							
0x022C	CBS_Q1	7:0	CREDIT_INCR_Q1[7:0]							
		15:8		CREDIT_INCR_Q1[14:8]						
		23:16	CREDIT_DECR_Q1[7:0]							
		31:24	CREDIT_DECR_Q1[15:8]							
0x0230	CBS_Min_Q0	7:0	CREDIT_MIN_Q0[7:0]							
		15:8	CREDIT_MIN_Q0[15:8]							
		23:16	CREDIT_MIN_Q0[23:16]							
		31:24		CREDIT_MIN_Q0[30:24]						
0x0234	CBS_Max_Q0	7:0	CREDIT_MAX_Q0[7:0]							
		15:8	CREDIT_MAX_Q0[15:8]							
		23:16	CREDIT_MAX_Q0[23:16]							
		31:24		CREDIT_MAX_Q0[30:24]						
0x0238	CBS_Min_Q1	7:0	CREDIT_MIN_Q1[7:0]							
		15:8	CREDIT_MIN_Q1[15:8]							
		23:16	CREDIT_MIN_Q1[23:16]							
		31:24		CREDIT_MIN_Q1[30:24]						
0x023C	CBS_Max_Q1	7:0	CREDIT_MAX_Q1[7:0]							
		15:8	CREDIT_MAX_Q1[15:8]							
		23:16	CREDIT_MAX_Q1[23:16]							
		31:24		CREDIT_MAX_Q1[30:24]						
0x0240	RX_SID_RST_TIMER	7:0	RX_STREMID_RST_TIMER[7:0]							
		15:8	RX_STREMID_RST_TIMER[15:8]							
		23:16	RX_STREMID_RST_TIMER[23:16]							
		31:24	RX_STREMID_RST_TIMER[31:24]							
0x0244 ... 0x028B	Reserved									
0x028C	PRIORITY_QUEUE_STATUS	7:0	QUEUE7_FULL	QUEUE6_FULL	QUEUE5_FULL	QUEUE4_FULL	QUEUE3_FULL	QUEUE2_FULL	QUEUE1_FULL	QUEUE0_FULL
		15:8	QUEUE7_EMPTY	QUEUE6_EMPTY	QUEUE5_EMPTY	QUEUE4_EMPTY	QUEUE3_EMPTY	QUEUE2_EMPTY	QUEUE1_EMPTY	QUEUE0_EMPTY
		23:16								
		31:24								
0x0290 ... 0x02FF	Reserved									
0x0300	PSFP_SID1_P0_0	7:0	PSFP_SID1_P0_SA_LSB[7:0]							
		15:8	PSFP_SID1_P0_SA_LSB[15:8]							
		23:16	PSFP_SID1_P0_SA_LSB[23:16]							
		31:24	PSFP_SID1_P0_SA_LSB[31:24]							
0x0304	PSFP_SID1_P0_1	7:0	PSFP_SID1_P0_SA_MSB[7:0]							
		15:8	PSFP_SID1_P0_SA_MSB[15:8]							
		23:16	PSFP_SID1_P0_VID[7:0]							
		31:24					PSFP_SID1_P0_VID[11:8]			
0x0308	PSFP_SID1_P0_CTRL	7:0							PSFP_SID1_P0_VID_EN	PSFP_SID1_P0_SA_EN
		15:8								
		23:16								
		31:24								
0x030C	PSFP_SID1_P0_MAX	7:0	PSFP_SID1_P0_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID1_P0_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0310	PSFP_SID1_P0_FM	7:0	PSFP_SID1_P0_CBS_LSB[7:0]							
		15:8	PSFP_SID1_P0_CBS_LSB[15:8]							
		23:16	PSFP_SID1_P0_EBS_LSB[7:0]							
		31:24	PSFP_SID1_P0_EBS_LSB[15:8]							
0x0314	PSFP_SID1_P0_FM_1	7:0	PSFP_SID1_P0_CIR[7:0]							
		15:8	PSFP_SID1_P0_CIR[15:8]							
		23:16	PSFP_SID1_P0_CIR[23:16]							
		31:24	PSFP_SID1_P0_CIR[31:24]							
0x0318	PSFP_SID1_P0_FM_2	7:0	PSFP_SID1_P0_EIR[7:0]							
		15:8	PSFP_SID1_P0_EIR[15:8]							
		23:16	PSFP_SID1_P0_EIR[23:16]							
		31:24	PSFP_SID1_P0_EIR[31:24]							
0x031C	PSFP_SID1_P0_FM_CTRL	7:0				PSFP_SID1_P0_CFG_UPD	PSFP_SID1_P0_DRP_MAX_EXCD	PSFP_SID1_P0_DRP_YELLOW	PSFP_SID1_P0_FM_EN	PSFP_SID1_P0_FIL_EN
		15:8								
		23:16								
		31:24								
0x0320	PSFP_SID2_P0_0	7:0	PSFP_SID2_P0_SA_LSB[7:0]							
		15:8	PSFP_SID2_P0_SA_LSB[15:8]							
		23:16	PSFP_SID2_P0_SA_LSB[23:16]							
		31:24	PSFP_SID2_P0_SA_LSB[31:24]							
0x0324	PSFP_SID2_P0_1	7:0	PSFP_SID2_P0_SA_MSB[7:0]							
		15:8	PSFP_SID2_P0_SA_MSB[15:8]							
		23:16	PSFP_SID2_P0_VID[7:0]							
		31:24					PSFP_SID2_P0_VID[11:8]			
0x0328	PSFP_SID2_P0_CTRL	7:0							PSFP_SID2_P0_VID_EN	PSFP_SID2_P0_SA_EN
		15:8								
		23:16								
		31:24								
0x032C	PSFP_SID2_P0_MAX	7:0	PSFP_SID2_P0_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID2_P0_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x0330	PSFP_SID2_P0_FM	7:0	PSFP_SID2_P0_CBS_LSB[7:0]							
		15:8	PSFP_SID2_P0_CBS_LSB[15:8]							
		23:16	PSFP_SID2_P0_EBS_LSB[7:0]							
		31:24	PSFP_SID2_P0_EBS_LSB[15:8]							
0x0334	PSFP_SID2_P0_FM_1	7:0	PSFP_SID2_P0_CIR[7:0]							
		15:8	PSFP_SID2_P0_CIR[15:8]							
		23:16	PSFP_SID2_P0_CIR[23:16]							
		31:24	PSFP_SID2_P0_CIR[31:24]							
0x0338	PSFP_SID2_P0_FM_2	7:0	PSFP_SID2_P0_EIR[7:0]							
		15:8	PSFP_SID2_P0_EIR[15:8]							
		23:16	PSFP_SID2_P0_EIR[23:16]							
		31:24	PSFP_SID2_P0_EIR[31:24]							
0x033C	PSFP_SID2_P0_FM_CTRL	7:0				PSFP_SID2_P0_CFG_UPD	PSFP_SID2_P0_DRP_MAX_EXCD	PSFP_SID2_P0_DRP_YELLOW	PSFP_SID2_P0_FM_EN	PSFP_SID2_P0_FIL_EN
		15:8								
		23:16								
		31:24								
0x0340	PSFP_SID3_P0_0	7:0	PSFP_SID3_P0_SA_LSB[7:0]							
		15:8	PSFP_SID3_P0_SA_LSB[15:8]							
		23:16	PSFP_SID3_P0_SA_LSB[23:16]							
		31:24	PSFP_SID3_P0_SA_LSB[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0344	PSFP_SID3_P0_1	7:0	PSFP_SID3_P0_SA_MSB[7:0]							
		15:8	PSFP_SID3_P0_SA_MSB[15:8]							
		23:16	PSFP_SID3_P0_VID[7:0]							
		31:24					PSFP_SID3_P0_VID[11:8]			
0x0348	PSFP_SID3_P0_CTRL	7:0							PSFP_SID3_P0_VID_EN	PSFP_SID3_P0_SA_EN
		15:8								
		23:16								
		31:24								
0x034C	PSFP_SID3_P0_MAX	7:0	PSFP_SID3_P0_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID3_P0_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x0350	PSFP_SID3_P0_FM	7:0	PSFP_SID3_P0_CBS_LSB[7:0]							
		15:8	PSFP_SID3_P0_CBS_LSB[15:8]							
		23:16	PSFP_SID3_P0_EBS_LSB[7:0]							
		31:24	PSFP_SID3_P0_EBS_LSB[15:8]							
0x0354	PSFP_SID3_P0_FM_1	7:0	PSFP_SID3_P0_CIR[7:0]							
		15:8	PSFP_SID3_P0_CIR[15:8]							
		23:16	PSFP_SID3_P0_CIR[23:16]							
		31:24	PSFP_SID3_P0_CIR[31:24]							
0x0358	PSFP_SID3_P0_FM_2	7:0	PSFP_SID3_P0_EIR[7:0]							
		15:8	PSFP_SID3_P0_EIR[15:8]							
		23:16	PSFP_SID3_P0_EIR[23:16]							
		31:24	PSFP_SID3_P0_EIR[31:24]							
0x035C	PSFP_SID3_P0_FM_CTRL	7:0				PSFP_SID3_P0_CFG_UPD	PSFP_SID3_P0_DRP_MAX_EXCD	PSFP_SID3_P0_DRP_YELLOW	PSFP_SID3_P0_FM_EN	PSFP_SID3_P0_FIL_EN
		15:8								
		23:16								
		31:24								
0x0360	PSFP_SID4_P0_0	7:0	PSFP_SID4_P0_SA_LSB[7:0]							
		15:8	PSFP_SID4_P0_SA_LSB[15:8]							
		23:16	PSFP_SID4_P0_SA_LSB[23:16]							
		31:24	PSFP_SID4_P0_SA_LSB[31:24]							
0x0364	PSFP_SID4_P0_1	7:0	PSFP_SID4_P0_SA_MSB[7:0]							
		15:8	PSFP_SID4_P0_SA_MSB[15:8]							
		23:16	PSFP_SID4_P0_VID[7:0]							
		31:24					PSFP_SID4_P0_VID[11:8]			
0x0368	PSFP_SID4_P0_CTRL	7:0							PSFP_SID4_P0_VID_EN	PSFP_SID4_P0_SA_EN
		15:8								
		23:16								
		31:24								
0x036C	PSFP_SID4_P0_MAX	7:0	PSFP_SID4_P0_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID4_P0_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x0370	PSFP_SID4_P0_FM	7:0	PSFP_SID4_P0_CBS_LSB[7:0]							
		15:8	PSFP_SID4_P0_CBS_LSB[15:8]							
		23:16	PSFP_SID4_P0_EBS_LSB[7:0]							
		31:24	PSFP_SID4_P0_EBS_LSB[15:8]							
0x0374	PSFP_SID4_P0_FM_1	7:0	PSFP_SID4_P0_CIR[7:0]							
		15:8	PSFP_SID4_P0_CIR[15:8]							
		23:16	PSFP_SID4_P0_CIR[23:16]							
		31:24	PSFP_SID4_P0_CIR[31:24]							
0x0378	PSFP_SID4_P0_FM_2	7:0	PSFP_SID4_P0_EIR[7:0]							
		15:8	PSFP_SID4_P0_EIR[15:8]							
		23:16	PSFP_SID4_P0_EIR[23:16]							
		31:24	PSFP_SID4_P0_EIR[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x037C	PSFP_SID4_P0_FM_CTRL	7:0				PSFP_SID4_P0_CFG_UPD	PSFP_SID4_P0_DRP_MAX_EXCD	PSFP_SID4_P0_DRP_YELLOW	PSFP_SID4_P0_FM_EN	PSFP_SID4_P0_FIL_EN
		15:8								
		23:16								
		31:24								
0x0380	PSFP_SID5_P0_0	7:0	PSFP_SID5_P0_SA_LSB[7:0]							
		15:8	PSFP_SID5_P0_SA_LSB[15:8]							
		23:16	PSFP_SID5_P0_SA_LSB[23:16]							
		31:24	PSFP_SID5_P0_SA_LSB[31:24]							
0x0384	PSFP_SID5_P0_1	7:0	PSFP_SID5_P0_SA_MSB[7:0]							
		15:8	PSFP_SID5_P0_SA_MSB[15:8]							
		23:16	PSFP_SID5_P0_VID[7:0]							
		31:24					PSFP_SID5_P0_VID[11:8]			
0x0388	PSFP_SID5_P0_CTRL	7:0							PSFP_SID5_P0_VID_EN	PSFP_SID5_P0_SA_EN
		15:8								
		23:16								
		31:24								
0x038C	PSFP_SID5_P0_MAX	7:0	PSFP_SID5_P0_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID5_P0_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x0390	PSFP_SID5_P0_FM	7:0	PSFP_SID5_P0_CBS_LSB[7:0]							
		15:8	PSFP_SID5_P0_CBS_LSB[15:8]							
		23:16	PSFP_SID5_P0_EBS_LSB[7:0]							
		31:24	PSFP_SID5_P0_EBS_LSB[15:8]							
0x0394	PSFP_SID5_P0_FM_1	7:0	PSFP_SID5_P0_CIR[7:0]							
		15:8	PSFP_SID5_P0_CIR[15:8]							
		23:16	PSFP_SID5_P0_CIR[23:16]							
		31:24	PSFP_SID5_P0_CIR[31:24]							
0x0398	PSFP_SID5_P0_FM_2	7:0	PSFP_SID5_P0_EIR[7:0]							
		15:8	PSFP_SID5_P0_EIR[15:8]							
		23:16	PSFP_SID5_P0_EIR[23:16]							
		31:24	PSFP_SID5_P0_EIR[31:24]							
0x039C	PSFP_SID5_P0_FM_CTRL	7:0				PSFP_SID5_P0_CFG_UPD	PSFP_SID5_P0_DRP_MAX_EXCD	PSFP_SID5_P0_DRP_YELLOW	PSFP_SID5_P0_FM_EN	PSFP_SID5_P0_FIL_EN
		15:8								
		23:16								
		31:24								
0x03A0	PSFP_SID6_P0_0	7:0	PSFP_SID6_P0_SA_LSB[7:0]							
		15:8	PSFP_SID6_P0_SA_LSB[15:8]							
		23:16	PSFP_SID6_P0_SA_LSB[23:16]							
		31:24	PSFP_SID6_P0_SA_LSB[31:24]							
0x03A4	PSFP_SID6_P0_1	7:0	PSFP_SID6_P0_SA_MSB[7:0]							
		15:8	PSFP_SID6_P0_SA_MSB[15:8]							
		23:16	PSFP_SID6_P0_VID[7:0]							
		31:24					PSFP_SID6_P0_VID[11:8]			
0x03A8	PSFP_SID6_P0_CTRL	7:0							PSFP_SID6_P0_VID_EN	PSFP_SID6_P0_SA_EN
		15:8								
		23:16								
		31:24								
0x03AC	PSFP_SID6_P0_MAX	7:0	PSFP_SID6_P0_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID6_P0_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x03B0	PSFP_SID6_P0_FM	7:0	PSFP_SID6_P0_CBS_LSB[7:0]							
		15:8	PSFP_SID6_P0_CBS_LSB[15:8]							
		23:16	PSFP_SID6_P0_EBS_LSB[7:0]							
		31:24	PSFP_SID6_P0_EBS_LSB[15:8]							
0x03B4	PSFP_SID6_P0_FM_1	7:0	PSFP_SID6_P0_CIR[7:0]							
		15:8	PSFP_SID6_P0_CIR[15:8]							
		23:16	PSFP_SID6_P0_CIR[23:16]							
		31:24	PSFP_SID6_P0_CIR[31:24]							
0x03B8	PSFP_SID6_P0_FM_2	7:0	PSFP_SID6_P0_EIR[7:0]							
		15:8	PSFP_SID6_P0_EIR[15:8]							
		23:16	PSFP_SID6_P0_EIR[23:16]							
		31:24	PSFP_SID6_P0_EIR[31:24]							
0x03BC	PSFP_SID6_P0_FM_CTRL	7:0				PSFP_SID6_P0_CFG_UPD	PSFP_SID6_P0_DRP_MAX_EXCD	PSFP_SID6_P0_DRP_YELLOW	PSFP_SID6_P0_FM_EN	PSFP_SID6_P0_FIL_EN
		15:8								
		23:16								
		31:24								
0x03C0	PSFP_SID7_P0_0	7:0	PSFP_SID7_P0_SA_LSB[7:0]							
		15:8	PSFP_SID7_P0_SA_LSB[15:8]							
		23:16	PSFP_SID7_P0_SA_LSB[23:16]							
		31:24	PSFP_SID7_P0_SA_LSB[31:24]							
0x03C4	PSFP_SID7_P0_1	7:0	PSFP_SID7_P0_SA_MSB[7:0]							
		15:8	PSFP_SID7_P0_SA_MSB[15:8]							
		23:16	PSFP_SID7_P0_VID[7:0]							
		31:24					PSFP_SID7_P0_VID[11:8]			
0x03C8	PSFP_SID7_P0_CTRL	7:0							PSFP_SID7_P0_VID_EN	PSFP_SID7_P0_SA_EN
		15:8								
		23:16								
		31:24								
0x03CC	PSFP_SID7_P0_MAX	7:0	PSFP_SID7_P0_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID7_P0_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x03D0	PSFP_SID7_P0_FM	7:0	PSFP_SID7_P0_CBS_LSB[7:0]							
		15:8	PSFP_SID7_P0_CBS_LSB[15:8]							
		23:16	PSFP_SID7_P0_EBS_LSB[7:0]							
		31:24	PSFP_SID7_P0_EBS_LSB[15:8]							
0x03D4	PSFP_SID7_P0_FM_1	7:0	PSFP_SID7_P0_CIR[7:0]							
		15:8	PSFP_SID7_P0_CIR[15:8]							
		23:16	PSFP_SID7_P0_CIR[23:16]							
		31:24	PSFP_SID7_P0_CIR[31:24]							
0x03D8	PSFP_SID7_P0_FM_2	7:0	PSFP_SID7_P0_EIR[7:0]							
		15:8	PSFP_SID7_P0_EIR[15:8]							
		23:16	PSFP_SID7_P0_EIR[23:16]							
		31:24	PSFP_SID7_P0_EIR[31:24]							
0x03DC	PSFP_SID7_P0_FM_CTRL	7:0				PSFP_SID7_P0_CFG_UPD	PSFP_SID7_P0_DRP_MAX_EXCD	PSFP_SID7_P0_DRP_YELLOW	PSFP_SID7_P0_FM_EN	PSFP_SID7_P0_FIL_EN
		15:8								
		23:16								
		31:24								
0x03E0	PSFP_SID8_P0_0	7:0	PSFP_SID8_P0_SA_LSB[7:0]							
		15:8	PSFP_SID8_P0_SA_LSB[15:8]							
		23:16	PSFP_SID8_P0_SA_LSB[23:16]							
		31:24	PSFP_SID8_P0_SA_LSB[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x03E4	PSFP_SID8_P0_1	7:0	PSFP_SID8_P0_SA_MSB[7:0]							
		15:8	PSFP_SID8_P0_SA_MSB[15:8]							
		23:16	PSFP_SID8_P0_VID[7:0]							
		31:24					PSFP_SID8_P0_VID[11:8]			
0x03E8	PSFP_SID8_P0_CTRL	7:0							PSFP_SID8_P0_VID_EN	PSFP_SID8_P0_SA_EN
		15:8								
		23:16								
		31:24								
0x03EC	PSFP_SID8_P0_MAX	7:0	PSFP_SID8_P0_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID8_P0_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x03F0	PSFP_SID8_P0_FM	7:0	PSFP_SID8_P0_CBS_LSB[7:0]							
		15:8	PSFP_SID8_P0_CBS_LSB[15:8]							
		23:16	PSFP_SID8_P0_EBS_LSB[7:0]							
		31:24	PSFP_SID8_P0_EBS_LSB[15:8]							
0x03F4	PSFP_SID8_P0_FM_1	7:0	PSFP_SID8_P0_CIR[7:0]							
		15:8	PSFP_SID8_P0_CIR[15:8]							
		23:16	PSFP_SID8_P0_CIR[23:16]							
		31:24	PSFP_SID8_P0_CIR[31:24]							
0x03F8	PSFP_SID8_P0_FM_2	7:0	PSFP_SID8_P0_EIR[7:0]							
		15:8	PSFP_SID8_P0_EIR[15:8]							
		23:16	PSFP_SID8_P0_EIR[23:16]							
		31:24	PSFP_SID8_P0_EIR[31:24]							
0x03FC	PSFP_SID8_P0_FM_CTRL	7:0				PSFP_SID8_P0_CFG_UPD	PSFP_SID8_P0_DRP_MAX_EXCD	PSFP_SID8_P0_DRP_YELLOW	PSFP_SID8_P0_FM_EN	PSFP_SID8_P0_FIL_EN
		15:8								
		23:16								
		31:24								
0x0400	PSFP_SID1_P1_0	7:0	PSFP_SID1_P1_SA_LSB[7:0]							
		15:8	PSFP_SID1_P1_SA_LSB[15:8]							
		23:16	PSFP_SID1_P1_SA_LSB[23:16]							
		31:24	PSFP_SID1_P1_SA_LSB[31:24]							
0x0404	PSFP_SID1_P1_1	7:0	PSFP_SID1_P1_SA_MSB[7:0]							
		15:8	PSFP_SID1_P1_SA_MSB[15:8]							
		23:16	PSFP_SID1_P1_VID[7:0]							
		31:24					PSFP_SID1_P1_VID[11:8]			
0x0408	PSFP_SID1_P1_CTRL	7:0							PSFP_SID1_P1_VID_EN	PSFP_SID1_P1_SA_EN
		15:8								
		23:16								
		31:24								
0x040C	PSFP_SID1_P1_MAX	7:0	PSFP_SID1_P1_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID1_P1_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x0410	PSFP_SID1_P1_FM	7:0	PSFP_SID1_P1_CBS_LSB[7:0]							
		15:8	PSFP_SID1_P1_CBS_LSB[15:8]							
		23:16	PSFP_SID1_P1_EBS_LSB[7:0]							
		31:24	PSFP_SID1_P1_EBS_LSB[15:8]							
0x0414	PSFP_SID1_P1_FM_1	7:0	PSFP_SID1_P1_CIR[7:0]							
		15:8	PSFP_SID1_P1_CIR[15:8]							
		23:16	PSFP_SID1_P1_CIR[23:16]							
		31:24	PSFP_SID1_P1_CIR[31:24]							
0x0418	PSFP_SID1_P1_FM_2	7:0	PSFP_SID1_P1_EIR[7:0]							
		15:8	PSFP_SID1_P1_EIR[15:8]							
		23:16	PSFP_SID1_P1_EIR[23:16]							
		31:24	PSFP_SID1_P1_EIR[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x041C	PSFP_SID1_P1_FM_CTRL	7:0				PSFP_SID1_P1_CFG_UPD	PSFP_SID1_P1_DRP_MAX_EXCD	PSFP_SID1_P1_DRP_YELLOW	PSFP_SID1_P1_FM_EN	PSFP_SID1_P1_FIL_EN
		15:8								
		23:16								
		31:24								
0x0420	PSFP_SID2_P1_0	7:0	PSFP_SID2_P1_SA_LSB[7:0]							
		15:8	PSFP_SID2_P1_SA_LSB[15:8]							
		23:16	PSFP_SID2_P1_SA_LSB[23:16]							
		31:24	PSFP_SID2_P1_SA_LSB[31:24]							
0x0424	PSFP_SID2_P1_1	7:0	PSFP_SID2_P1_SA_MSB[7:0]							
		15:8	PSFP_SID2_P1_SA_MSB[15:8]							
		23:16	PSFP_SID2_P1_VID[7:0]							
		31:24					PSFP_SID2_P1_VID[11:8]			
0x0428	PSFP_SID2_P1_CTRL	7:0							PSFP_SID2_P1_VID_EN	PSFP_SID2_P1_SA_EN
		15:8								
		23:16								
		31:24								
0x042C	PSFP_SID2_P1_MAX	7:0	PSFP_SID2_P1_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID2_P1_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x0430	PSFP_SID2_P1_FM	7:0	PSFP_SID2_P1_CBS_LSB[7:0]							
		15:8	PSFP_SID2_P1_CBS_LSB[15:8]							
		23:16	PSFP_SID2_P1_EBS_LSB[7:0]							
		31:24	PSFP_SID2_P1_EBS_LSB[15:8]							
0x0434	PSFP_SID2_P1_FM_1	7:0	PSFP_SID2_P1_CIR[7:0]							
		15:8	PSFP_SID2_P1_CIR[15:8]							
		23:16	PSFP_SID2_P1_CIR[23:16]							
		31:24	PSFP_SID2_P1_CIR[31:24]							
0x0438	PSFP_SID2_P1_FM_2	7:0	PSFP_SID2_P1_EIR[7:0]							
		15:8	PSFP_SID2_P1_EIR[15:8]							
		23:16	PSFP_SID2_P1_EIR[23:16]							
		31:24	PSFP_SID2_P1_EIR[31:24]							
0x043C	PSFP_SID2_P1_FM_CTRL	7:0				PSFP_SID2_P1_CFG_UPD	PSFP_SID2_P1_DRP_MAX_EXCD	PSFP_SID2_P1_DRP_YELLOW	PSFP_SID2_P1_FM_EN	PSFP_SID2_P1_FIL_EN
		15:8								
		23:16								
		31:24								
0x0440	PSFP_SID3_P1_0	7:0	PSFP_SID3_P1_SA_LSB[7:0]							
		15:8	PSFP_SID3_P1_SA_LSB[15:8]							
		23:16	PSFP_SID3_P1_SA_LSB[23:16]							
		31:24	PSFP_SID3_P1_SA_LSB[31:24]							
0x0444	PSFP_SID3_P1_1	7:0	PSFP_SID3_P1_SA_MSB[7:0]							
		15:8	PSFP_SID3_P1_SA_MSB[15:8]							
		23:16	PSFP_SID3_P1_VID[7:0]							
		31:24					PSFP_SID3_P1_VID[11:8]			
0x0448	PSFP_SID3_P1_CTRL	7:0							PSFP_SID3_P1_VID_EN	PSFP_SID3_P1_SA_EN
		15:8								
		23:16								
		31:24								
0x044C	PSFP_SID3_P1_MAX	7:0	PSFP_SID3_P1_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID3_P1_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0450	PSFP_SID3_P1_FM	7:0	PSFP_SID3_P1_CBS_LSB[7:0]							
		15:8	PSFP_SID3_P1_CBS_LSB[15:8]							
		23:16	PSFP_SID3_P1_EBS_LSB[7:0]							
		31:24	PSFP_SID3_P1_EBS_LSB[15:8]							
0x0454	PSFP_SID3_P1_FM_1	7:0	PSFP_SID3_P1_CIR[7:0]							
		15:8	PSFP_SID3_P1_CIR[15:8]							
		23:16	PSFP_SID3_P1_CIR[23:16]							
		31:24	PSFP_SID3_P1_CIR[31:24]							
0x0458	PSFP_SID3_P1_FM_2	7:0	PSFP_SID3_P1_EIR[7:0]							
		15:8	PSFP_SID3_P1_EIR[15:8]							
		23:16	PSFP_SID3_P1_EIR[23:16]							
		31:24	PSFP_SID3_P1_EIR[31:24]							
0x045C	PSFP_SID3_P1_FM_CTRL	7:0				PSFP_SID3_P1_CFG_UPD	PSFP_SID3_P1_DRP_MAX_EXCD	PSFP_SID3_P1_DRP_YELLOW	PSFP_SID3_P1_FM_EN	PSFP_SID3_P1_FIL_EN
		15:8								
		23:16								
		31:24								
0x0460	PSFP_SID4_P1_0	7:0	PSFP_SID4_P1_SA_LSB[7:0]							
		15:8	PSFP_SID4_P1_SA_LSB[15:8]							
		23:16	PSFP_SID4_P1_SA_LSB[23:16]							
		31:24	PSFP_SID4_P1_SA_LSB[31:24]							
0x0464	PSFP_SID4_P1_1	7:0	PSFP_SID4_P1_SA_MSB[7:0]							
		15:8	PSFP_SID4_P1_SA_MSB[15:8]							
		23:16	PSFP_SID4_P1_VID[7:0]							
		31:24					PSFP_SID4_P1_VID[11:8]			
0x0468	PSFP_SID4_P1_CTRL	7:0							PSFP_SID4_P1_VID_EN	PSFP_SID4_P1_SA_EN
		15:8								
		23:16								
		31:24								
0x046C	PSFP_SID4_P1_MAX	7:0	PSFP_SID4_P1_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID4_P1_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x0470	PSFP_SID4_P1_FM	7:0	PSFP_SID4_P1_CBS_LSB[7:0]							
		15:8	PSFP_SID4_P1_CBS_LSB[15:8]							
		23:16	PSFP_SID4_P1_EBS_LSB[7:0]							
		31:24	PSFP_SID4_P1_EBS_LSB[15:8]							
0x0474	PSFP_SID4_P1_FM_1	7:0	PSFP_SID4_P1_CIR[7:0]							
		15:8	PSFP_SID4_P1_CIR[15:8]							
		23:16	PSFP_SID4_P1_CIR[23:16]							
		31:24	PSFP_SID4_P1_CIR[31:24]							
0x0478	PSFP_SID4_P1_FM_2	7:0	PSFP_SID4_P1_EIR[7:0]							
		15:8	PSFP_SID4_P1_EIR[15:8]							
		23:16	PSFP_SID4_P1_EIR[23:16]							
		31:24	PSFP_SID4_P1_EIR[31:24]							
0x047C	PSFP_SID4_P1_FM_CTRL	7:0				PSFP_SID4_P1_CFG_UPD	PSFP_SID4_P1_DRP_MAX_EXCD	PSFP_SID4_P1_DRP_YELLOW	PSFP_SID4_P1_FM_EN	PSFP_SID4_P1_FIL_EN
		15:8								
		23:16								
		31:24								
0x0480	PSFP_SID5_P1_0	7:0	PSFP_SID5_P1_SA_LSB[7:0]							
		15:8	PSFP_SID5_P1_SA_LSB[15:8]							
		23:16	PSFP_SID5_P1_SA_LSB[23:16]							
		31:24	PSFP_SID5_P1_SA_LSB[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0484	PSFP_SID5_P1_1	7:0	PSFP_SID5_P1_SA_MSB[7:0]							
		15:8	PSFP_SID5_P1_SA_MSB[15:8]							
		23:16	PSFP_SID5_P1_VID[7:0]							
		31:24					PSFP_SID5_P1_VID[11:8]			
0x0488	PSFP_SID5_P1_CTRL	7:0							PSFP_SID5_P1_VID_EN	PSFP_SID5_P1_SA_EN
		15:8								
		23:16								
		31:24								
0x048C	PSFP_SID5_P1_MAX	7:0	PSFP_SID5_P1_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID5_P1_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x0490	PSFP_SID5_P1_FM	7:0	PSFP_SID5_P1_CBS_LSB[7:0]							
		15:8	PSFP_SID5_P1_CBS_LSB[15:8]							
		23:16	PSFP_SID5_P1_EBS_LSB[7:0]							
		31:24	PSFP_SID5_P1_EBS_LSB[15:8]							
0x0494	PSFP_SID5_P1_FM_1	7:0	PSFP_SID5_P1_CIR[7:0]							
		15:8	PSFP_SID5_P1_CIR[15:8]							
		23:16	PSFP_SID5_P1_CIR[23:16]							
		31:24	PSFP_SID5_P1_CIR[31:24]							
0x0498	PSFP_SID5_P1_FM_2	7:0	PSFP_SID5_P1_EIR[7:0]							
		15:8	PSFP_SID5_P1_EIR[15:8]							
		23:16	PSFP_SID5_P1_EIR[23:16]							
		31:24	PSFP_SID5_P1_EIR[31:24]							
0x049C	PSFP_SID5_P1_FM_CTRL	7:0				PSFP_SID5_P1_CFG_UPD	PSFP_SID5_P1_DRP_MAX_EXCD	PSFP_SID5_P1_DRP_YELLOW	PSFP_SID5_P1_FM_EN	PSFP_SID5_P1_FIL_EN
		15:8								
		23:16								
		31:24								
0x04A0	PSFP_SID6_P1_0	7:0	PSFP_SID6_P1_SA_LSB[7:0]							
		15:8	PSFP_SID6_P1_SA_LSB[15:8]							
		23:16	PSFP_SID6_P1_SA_LSB[23:16]							
		31:24	PSFP_SID6_P1_SA_LSB[31:24]							
0x04A4	PSFP_SID6_P1_1	7:0	PSFP_SID6_P1_SA_MSB[7:0]							
		15:8	PSFP_SID6_P1_SA_MSB[15:8]							
		23:16	PSFP_SID6_P1_VID[7:0]							
		31:24					PSFP_SID6_P1_VID[11:8]			
0x04A8	PSFP_SID6_P1_CTRL	7:0							PSFP_SID6_P1_VID_EN	PSFP_SID6_P1_SA_EN
		15:8								
		23:16								
		31:24								
0x04AC	PSFP_SID6_P1_MAX	7:0	PSFP_SID6_P1_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID6_P1_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x04B0	PSFP_SID6_P1_FM	7:0	PSFP_SID6_P1_CBS_LSB[7:0]							
		15:8	PSFP_SID6_P1_CBS_LSB[15:8]							
		23:16	PSFP_SID6_P1_EBS_LSB[7:0]							
		31:24	PSFP_SID6_P1_EBS_LSB[15:8]							
0x04B4	PSFP_SID6_P1_FM_1	7:0	PSFP_SID6_P1_CIR[7:0]							
		15:8	PSFP_SID6_P1_CIR[15:8]							
		23:16	PSFP_SID6_P1_CIR[23:16]							
		31:24	PSFP_SID6_P1_CIR[31:24]							
0x04B8	PSFP_SID6_P1_FM_2	7:0	PSFP_SID6_P1_EIR[7:0]							
		15:8	PSFP_SID6_P1_EIR[15:8]							
		23:16	PSFP_SID6_P1_EIR[23:16]							
		31:24	PSFP_SID6_P1_EIR[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x04BC	PSFP_SID6_P1_FM_CTRL	7:0				PSFP_SID6_P1_CFG_UPD	PSFP_SID6_P1_DRP_MAX_EXCD	PSFP_SID6_P1_DRP_YELLOW	PSFP_SID6_P1_FM_EN	PSFP_SID6_P1_FIL_EN
		15:8								
		23:16								
		31:24								
0x04C0	PSFP_SID7_P1_0	7:0	PSFP_SID7_P1_SA_LSB[7:0]							
		15:8	PSFP_SID7_P1_SA_LSB[15:8]							
		23:16	PSFP_SID7_P1_SA_LSB[23:16]							
		31:24	PSFP_SID7_P1_SA_LSB[31:24]							
0x04C4	PSFP_SID7_P1_1	7:0	PSFP_SID7_P1_SA_MSB[7:0]							
		15:8	PSFP_SID7_P1_SA_MSB[15:8]							
		23:16	PSFP_SID7_P1_VID[7:0]							
		31:24					PSFP_SID7_P1_VID[11:8]			
0x04C8	PSFP_SID7_P1_CTRL	7:0							PSFP_SID7_P1_VID_EN	PSFP_SID7_P1_SA_EN
		15:8								
		23:16								
		31:24								
0x04CC	PSFP_SID7_P1_MAX	7:0	PSFP_SID7_P1_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID7_P1_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								
0x04D0	PSFP_SID7_P1_FM	7:0	PSFP_SID7_P1_CBS_LSB[7:0]							
		15:8	PSFP_SID7_P1_CBS_LSB[15:8]							
		23:16	PSFP_SID7_P1_EBS_LSB[7:0]							
		31:24	PSFP_SID7_P1_EBS_LSB[15:8]							
0x04D4	PSFP_SID7_P1_FM_1	7:0	PSFP_SID7_P1_CIR[7:0]							
		15:8	PSFP_SID7_P1_CIR[15:8]							
		23:16	PSFP_SID7_P1_CIR[23:16]							
		31:24	PSFP_SID7_P1_CIR[31:24]							
0x04D8	PSFP_SID7_P1_FM_2	7:0	PSFP_SID7_P1_EIR[7:0]							
		15:8	PSFP_SID7_P1_EIR[15:8]							
		23:16	PSFP_SID7_P1_EIR[23:16]							
		31:24	PSFP_SID7_P1_EIR[31:24]							
0x04DC	PSFP_SID7_P1_FM_CTRL	7:0				PSFP_SID7_P1_CFG_UPD	PSFP_SID7_P1_DRP_MAX_EXCD	PSFP_SID7_P1_DRP_YELLOW	PSFP_SID7_P1_FM_EN	PSFP_SID7_P1_FIL_EN
		15:8								
		23:16								
		31:24								
0x04E0	PSFP_SID8_P1_0	7:0	PSFP_SID8_P1_SA_LSB[7:0]							
		15:8	PSFP_SID8_P1_SA_LSB[15:8]							
		23:16	PSFP_SID8_P1_SA_LSB[23:16]							
		31:24	PSFP_SID8_P1_SA_LSB[31:24]							
0x04E4	PSFP_SID8_P1_1	7:0	PSFP_SID8_P1_SA_MSB[7:0]							
		15:8	PSFP_SID8_P1_SA_MSB[15:8]							
		23:16	PSFP_SID8_P1_VID[7:0]							
		31:24					PSFP_SID8_P1_VID[11:8]			
0x04E8	PSFP_SID8_P1_CTRL	7:0							PSFP_SID8_P1_VID_EN	PSFP_SID8_P1_SA_EN
		15:8								
		23:16								
		31:24								
0x04EC	PSFP_SID8_P1_MAX	7:0	PSFP_SID8_P1_MAX_PKT_SIZE[7:0]							
		15:8	PSFP_SID8_P1_MAX_PKT_SIZE[15:8]							
		23:16								
		31:24								

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x04F0	PSFP_SID8_P1_FM	7:0	PSFP_SID8_P1_CBS_LSB[7:0]							
		15:8	PSFP_SID8_P1_CBS_LSB[15:8]							
		23:16	PSFP_SID8_P1_EBS_LSB[7:0]							
		31:24	PSFP_SID8_P1_EBS_LSB[15:8]							
0x04F4	PSFP_SID8_P1_FM_1	7:0	PSFP_SID8_P1_CIR[7:0]							
		15:8	PSFP_SID8_P1_CIR[15:8]							
		23:16	PSFP_SID8_P1_CIR[23:16]							
		31:24	PSFP_SID8_P1_CIR[31:24]							
0x04F8	PSFP_SID8_P1_FM_2	7:0	PSFP_SID8_P1_EIR[7:0]							
		15:8	PSFP_SID8_P1_EIR[15:8]							
		23:16	PSFP_SID8_P1_EIR[23:16]							
		31:24	PSFP_SID8_P1_EIR[31:24]							
0x04FC	PSFP_SID8_P1_FM_CTRL	7:0				PSFP_SID8_P1_CFG_UPD	PSFP_SID8_P1_DRP_MAX_EXCD	PSFP_SID8_P1_DRP_YELLOW	PSFP_SID8_P1_FM_EN	PSFP_SID8_P1_FIL_EN
		15:8								
		23:16								
		31:24								
0x0500	PSFP_SID1_P0_FM_3	7:0	PSFP_SID1_P0_CBS_MSB[7:0]							
		15:8	PSFP_SID1_P0_CBS_MSB[15:8]							
		23:16	PSFP_SID1_P0_EBS_MSB[7:0]							
		31:24	PSFP_SID1_P0_EBS_MSB[15:8]							
0x0504	PSFP_SID2_P0_FM_3	7:0	PSFP_SID2_P0_CBS_MSB[7:0]							
		15:8	PSFP_SID2_P0_CBS_MSB[15:8]							
		23:16	PSFP_SID2_P0_EBS_MSB[7:0]							
		31:24	PSFP_SID2_P0_EBS_MSB[15:8]							
0x0508	PSFP_SID3_P0_FM_3	7:0	PSFP_SID3_P0_CBS_MSB[7:0]							
		15:8	PSFP_SID3_P0_CBS_MSB[15:8]							
		23:16	PSFP_SID3_P0_EBS_MSB[7:0]							
		31:24	PSFP_SID3_P0_EBS_MSB[15:8]							
0x050C	PSFP_SID4_P0_FM_3	7:0	PSFP_SID4_P0_CBS_MSB[7:0]							
		15:8	PSFP_SID4_P0_CBS_MSB[15:8]							
		23:16	PSFP_SID4_P0_EBS_MSB[7:0]							
		31:24	PSFP_SID4_P0_EBS_MSB[15:8]							
0x0510	PSFP_SID5_P0_FM_3	7:0	PSFP_SID5_P0_CBS_MSB[7:0]							
		15:8	PSFP_SID5_P0_CBS_MSB[15:8]							
		23:16	PSFP_SID5_P0_EBS_MSB[7:0]							
		31:24	PSFP_SID5_P0_EBS_MSB[15:8]							
0x0514	PSFP_SID6_P0_FM_3	7:0	PSFP_SID6_P0_CBS_MSB[7:0]							
		15:8	PSFP_SID6_P0_CBS_MSB[15:8]							
		23:16	PSFP_SID6_P0_EBS_MSB[7:0]							
		31:24	PSFP_SID6_P0_EBS_MSB[15:8]							
0x0518	PSFP_SID7_P0_FM_3	7:0	PSFP_SID7_P0_CBS_MSB[7:0]							
		15:8	PSFP_SID7_P0_CBS_MSB[15:8]							
		23:16	PSFP_SID7_P0_EBS_MSB[7:0]							
		31:24	PSFP_SID7_P0_EBS_MSB[15:8]							
0x051C	PSFP_SID8_P0_FM_3	7:0	PSFP_SID8_P0_CBS_MSB[7:0]							
		15:8	PSFP_SID8_P0_CBS_MSB[15:8]							
		23:16	PSFP_SID8_P0_EBS_MSB[7:0]							
		31:24	PSFP_SID8_P0_EBS_MSB[15:8]							
0x0520	PSFP_SID1_P1_FM_3	7:0	PSFP_SID1_P1_CBS_MSB[7:0]							
		15:8	PSFP_SID1_P1_CBS_MSB[15:8]							
		23:16	PSFP_SID1_P1_EBS_MSB[7:0]							
		31:24	PSFP_SID1_P1_EBS_MSB[15:8]							
0x0524	PSFP_SID2_P1_FM_3	7:0	PSFP_SID2_P1_CBS_MSB[7:0]							
		15:8	PSFP_SID2_P1_CBS_MSB[15:8]							
		23:16	PSFP_SID2_P1_EBS_MSB[7:0]							
		31:24	PSFP_SID2_P1_EBS_MSB[15:8]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0528	PSFP_SID3_P1_FM_3	7:0	PSFP_SID3_P1_CBS_MSB[7:0]							
		15:8	PSFP_SID3_P1_CBS_MSB[15:8]							
		23:16	PSFP_SID3_P1_EBS_MSB[7:0]							
		31:24	PSFP_SID3_P1_EBS_MSB[15:8]							
0x052C	PSFP_SID4_P1_FM_3	7:0	PSFP_SID4_P1_CBS_MSB[7:0]							
		15:8	PSFP_SID4_P1_CBS_MSB[15:8]							
		23:16	PSFP_SID4_P1_EBS_MSB[7:0]							
		31:24	PSFP_SID4_P1_EBS_MSB[15:8]							
0x0530	PSFP_SID5_P1_FM_3	7:0	PSFP_SID5_P1_CBS_MSB[7:0]							
		15:8	PSFP_SID5_P1_CBS_MSB[15:8]							
		23:16	PSFP_SID5_P1_EBS_MSB[7:0]							
		31:24	PSFP_SID5_P1_EBS_MSB[15:8]							
0x0534	PSFP_SID6_P1_FM_3	7:0	PSFP_SID6_P1_CBS_MSB[7:0]							
		15:8	PSFP_SID6_P1_CBS_MSB[15:8]							
		23:16	PSFP_SID6_P1_EBS_MSB[7:0]							
		31:24	PSFP_SID6_P1_EBS_MSB[15:8]							
0x0538	PSFP_SID7_P1_FM_3	7:0	PSFP_SID7_P1_CBS_MSB[7:0]							
		15:8	PSFP_SID7_P1_CBS_MSB[15:8]							
		23:16	PSFP_SID7_P1_EBS_MSB[7:0]							
		31:24	PSFP_SID7_P1_EBS_MSB[15:8]							
0x053C	PSFP_SID8_P1_FM_3	7:0	PSFP_SID8_P1_CBS_MSB[7:0]							
		15:8	PSFP_SID8_P1_CBS_MSB[15:8]							
		23:16	PSFP_SID8_P1_EBS_MSB[7:0]							
		31:24	PSFP_SID8_P1_EBS_MSB[15:8]							
0x0540	GUARD_BAND_GCL0_GCL1	7:0	GCL0_GUARD_BAND[7:0]							
		15:8	GCL0_GUARD_BAND[15:8]							
		23:16	GCL1_GUARD_BAND[7:0]							
		31:24	GCL1_GUARD_BAND[15:8]							
0x0544	GUARD_BAND_GCL2_GCL3	7:0	GCL2_GUARD_BAND[7:0]							
		15:8	GCL2_GUARD_BAND[15:8]							
		23:16	GCL3_GUARD_BAND[7:0]							
		31:24	GCL3_GUARD_BAND[15:8]							
0x0548	GUARD_BAND_GCL4_GCL5	7:0	GCL4_GUARD_BAND[7:0]							
		15:8	GCL4_GUARD_BAND[15:8]							
		23:16	GCL5_GUARD_BAND[7:0]							
		31:24	GCL5_GUARD_BAND[15:8]							
0x054C	GUARD_BAND_GCL6_GCL7	7:0	GCL6_GUARD_BAND[7:0]							
		15:8	GCL6_GUARD_BAND[15:8]							
		23:16	GCL7_GUARD_BAND[7:0]							
		31:24	GCL7_GUARD_BAND[15:8]							
0x0550	GUARD_BAND_GCL8_GCL9	7:0	GCL8_GUARD_BAND[7:0]							
		15:8	GCL8_GUARD_BAND[15:8]							
		23:16	GCL9_GUARD_BAND[7:0]							
		31:24	GCL9_GUARD_BAND[15:8]							
0x0554	GUARD_BAND_GCL10_GCL11	7:0	GCL10_GUARD_BAND[7:0]							
		15:8	GCL10_GUARD_BAND[15:8]							
		23:16	GCL11_GUARD_BAND[7:0]							
		31:24	GCL11_GUARD_BAND[15:8]							
0x0558	GUARD_BAND_GCL12_GCL13	7:0	GCL12_GUARD_BAND[7:0]							
		15:8	GCL12_GUARD_BAND[15:8]							
		23:16	GCL13_GUARD_BAND[7:0]							
		31:24	GCL13_GUARD_BAND[15:8]							
0x055C	GUARD_BAND_GCL14_GCL15	7:0	GCL14_GUARD_BAND[7:0]							
		15:8	GCL14_GUARD_BAND[15:8]							
		23:16	GCL15_GUARD_BAND[7:0]							
		31:24	GCL15_GUARD_BAND[15:8]							
0x0560	GUARD_BAND_GCL16_GCL17	7:0	GCL16_GUARD_BAND[7:0]							
		15:8	GCL16_GUARD_BAND[15:8]							
		23:16	GCL17_GUARD_BAND[7:0]							
		31:24	GCL17_GUARD_BAND[15:8]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0564	GUARD_BAND_GCL18_GCL19	7:0	GCL18_GUARD_BAND[7:0]							
		15:8	GCL18_GUARD_BAND[15:8]							
		23:16	GCL19_GUARD_BAND[7:0]							
		31:24	GCL19_GUARD_BAND[15:8]							
0x0568	GUARD_BAND_GCL20_GCL21	7:0	GCL20_GUARD_BAND[7:0]							
		15:8	GCL20_GUARD_BAND[15:8]							
		23:16	GCL21_GUARD_BAND[7:0]							
		31:24	GCL21_GUARD_BAND[15:8]							
0x056C	GUARD_BAND_GCL22_GCL23	7:0	GCL22_GUARD_BAND[7:0]							
		15:8	GCL22_GUARD_BAND[15:8]							
		23:16	GCL23_GUARD_BAND[7:0]							
		31:24	GCL23_GUARD_BAND[15:8]							
0x0570	GUARD_BAND_GCL24_GCL25	7:0	GCL24_GUARD_BAND[7:0]							
		15:8	GCL24_GUARD_BAND[15:8]							
		23:16	GCL25_GUARD_BAND[7:0]							
		31:24	GCL25_GUARD_BAND[15:8]							
0x0574	GUARD_BAND_GCL26_GCL27	7:0	GCL26_GUARD_BAND[7:0]							
		15:8	GCL26_GUARD_BAND[15:8]							
		23:16	GCL27_GUARD_BAND[7:0]							
		31:24	GCL27_GUARD_BAND[15:8]							
0x0578	GUARD_BAND_GCL28_GCL29	7:0	GCL28_GUARD_BAND[7:0]							
		15:8	GCL28_GUARD_BAND[15:8]							
		23:16	GCL29_GUARD_BAND[7:0]							
		31:24	GCL29_GUARD_BAND[15:8]							
0x057C	GUARD_BAND_GCL30_GCL31	7:0	GCL30_GUARD_BAND[7:0]							
		15:8	GCL30_GUARD_BAND[15:8]							
		23:16	GCL31_GUARD_BAND[7:0]							
		31:24	GCL31_GUARD_BAND[15:8]							
0x0580 ... 0x05FF	Reserved									
0x0600	SID1_Q0_PKT_DRP	7:0	SID1_Q0_PKT_DRP_CNT[7:0]							
		15:8	SID1_Q0_PKT_DRP_CNT[15:8]							
		23:16	SID1_Q0_PKT_DRP_CNT[23:16]							
		31:24	SID1_Q0_PKT_DRP_CNT[31:24]							
0x0604	SID2_Q0_PKT_DRP	7:0	SID2_Q0_PKT_DRP_CNT[7:0]							
		15:8	SID2_Q0_PKT_DRP_CNT[15:8]							
		23:16	SID2_Q0_PKT_DRP_CNT[23:16]							
		31:24	SID2_Q0_PKT_DRP_CNT[31:24]							
0x0608	SID1_Q1_PKT_DRP	7:0	SID1_Q1_PKT_DRP_CNT[7:0]							
		15:8	SID1_Q1_PKT_DRP_CNT[15:8]							
		23:16	SID1_Q1_PKT_DRP_CNT[23:16]							
		31:24	SID1_Q1_PKT_DRP_CNT[31:24]							
0x060C	SID2_Q1_PKT_DRP	7:0	SID2_Q1_PKT_DRP_CNT[7:0]							
		15:8	SID2_Q1_PKT_DRP_CNT[15:8]							
		23:16	SID2_Q1_PKT_DRP_CNT[23:16]							
		31:24	SID2_Q1_PKT_DRP_CNT[31:24]							
0x0610	SID1_Q2_PKT_DRP	7:0	SID1_Q2_PKT_DRP_CNT[7:0]							
		15:8	SID1_Q2_PKT_DRP_CNT[15:8]							
		23:16	SID1_Q2_PKT_DRP_CNT[23:16]							
		31:24	SID1_Q2_PKT_DRP_CNT[31:24]							
0x0614	SID2_Q2_PKT_DRP	7:0	SID2_Q2_PKT_DRP_CNT[7:0]							
		15:8	SID2_Q2_PKT_DRP_CNT[15:8]							
		23:16	SID2_Q2_PKT_DRP_CNT[23:16]							
		31:24	SID2_Q2_PKT_DRP_CNT[31:24]							
0x0618	SID1_Q3_PKT_DRP	7:0	SID1_Q3_PKT_DRP_CNT[7:0]							
		15:8	SID1_Q3_PKT_DRP_CNT[15:8]							
		23:16	SID1_Q3_PKT_DRP_CNT[23:16]							
		31:24	SID1_Q3_PKT_DRP_CNT[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x061C	SID2_Q3_PKT_DRP	7:0	SID2_Q3_PKT_DRP_CNT[7:0]							
		15:8	SID2_Q3_PKT_DRP_CNT[15:8]							
		23:16	SID2_Q3_PKT_DRP_CNT[23:16]							
		31:24	SID2_Q3_PKT_DRP_CNT[31:24]							
0x0620	SID1_Q4_PKT_DRP	7:0	SID1_Q4_PKT_DRP_CNT[7:0]							
		15:8	SID1_Q4_PKT_DRP_CNT[15:8]							
		23:16	SID1_Q4_PKT_DRP_CNT[23:16]							
		31:24	SID1_Q4_PKT_DRP_CNT[31:24]							
0x0624	SID2_Q4_PKT_DRP	7:0	SID2_Q4_PKT_DRP_CNT[7:0]							
		15:8	SID2_Q4_PKT_DRP_CNT[15:8]							
		23:16	SID2_Q4_PKT_DRP_CNT[23:16]							
		31:24	SID2_Q4_PKT_DRP_CNT[31:24]							
0x0628	SID1_Q5_PKT_DRP	7:0	SID1_Q5_PKT_DRP_CNT[7:0]							
		15:8	SID1_Q5_PKT_DRP_CNT[15:8]							
		23:16	SID1_Q5_PKT_DRP_CNT[23:16]							
		31:24	SID1_Q5_PKT_DRP_CNT[31:24]							
0x062C	SID2_Q5_PKT_DRP	7:0	SID2_Q5_PKT_DRP_CNT[7:0]							
		15:8	SID2_Q5_PKT_DRP_CNT[15:8]							
		23:16	SID2_Q5_PKT_DRP_CNT[23:16]							
		31:24	SID2_Q5_PKT_DRP_CNT[31:24]							
0x0630	SID1_Q6_PKT_DRP	7:0	SID1_Q6_PKT_DRP_CNT[7:0]							
		15:8	SID1_Q6_PKT_DRP_CNT[15:8]							
		23:16	SID1_Q6_PKT_DRP_CNT[23:16]							
		31:24	SID1_Q6_PKT_DRP_CNT[31:24]							
0x0634	SID2_Q6_PKT_DRP	7:0	SID2_Q6_PKT_DRP_CNT[7:0]							
		15:8	SID2_Q6_PKT_DRP_CNT[15:8]							
		23:16	SID2_Q6_PKT_DRP_CNT[23:16]							
		31:24	SID2_Q6_PKT_DRP_CNT[31:24]							
0x0638	SID1_Q7_PKT_DRP	7:0	SID1_Q7_PKT_DRP_CNT[7:0]							
		15:8	SID1_Q7_PKT_DRP_CNT[15:8]							
		23:16	SID1_Q7_PKT_DRP_CNT[23:16]							
		31:24	SID1_Q7_PKT_DRP_CNT[31:24]							
0x063C	SID2_Q7_PKT_DRP	7:0	SID2_Q7_PKT_DRP_CNT[7:0]							
		15:8	SID2_Q7_PKT_DRP_CNT[15:8]							
		23:16	SID2_Q7_PKT_DRP_CNT[23:16]							
		31:24	SID2_Q7_PKT_DRP_CNT[31:24]							
0x0640	SID1_Q0_PKT_SENT	7:0	SID1_Q0_PKT_SENT_CNT[7:0]							
		15:8	SID1_Q0_PKT_SENT_CNT[15:8]							
		23:16	SID1_Q0_PKT_SENT_CNT[23:16]							
		31:24	SID1_Q0_PKT_SENT_CNT[31:24]							
0x0644	SID2_Q0_PKT_SENT	7:0	SID2_Q0_PKT_SENT_CNT[7:0]							
		15:8	SID2_Q0_PKT_SENT_CNT[15:8]							
		23:16	SID2_Q0_PKT_SENT_CNT[23:16]							
		31:24	SID2_Q0_PKT_SENT_CNT[31:24]							
0x0648	SID1_Q1_PKT_SENT	7:0	SID1_Q1_PKT_SENT_CNT[7:0]							
		15:8	SID1_Q1_PKT_SENT_CNT[15:8]							
		23:16	SID1_Q1_PKT_SENT_CNT[23:16]							
		31:24	SID1_Q1_PKT_SENT_CNT[31:24]							
0x064C	SID2_Q1_PKT_SENT	7:0	SID2_Q1_PKT_SENT_CNT[7:0]							
		15:8	SID2_Q1_PKT_SENT_CNT[15:8]							
		23:16	SID2_Q1_PKT_SENT_CNT[23:16]							
		31:24	SID2_Q1_PKT_SENT_CNT[31:24]							
0x0650	SID1_Q2_PKT_SENT	7:0	SID1_Q2_PKT_SENT_CNT[7:0]							
		15:8	SID1_Q2_PKT_SENT_CNT[15:8]							
		23:16	SID1_Q2_PKT_SENT_CNT[23:16]							
		31:24	SID1_Q2_PKT_SENT_CNT[31:24]							
0x0654	SID2_Q2_PKT_SENT	7:0	SID2_Q2_PKT_SENT_CNT[7:0]							
		15:8	SID2_Q2_PKT_SENT_CNT[15:8]							
		23:16	SID2_Q2_PKT_SENT_CNT[23:16]							
		31:24	SID2_Q2_PKT_SENT_CNT[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0658	SID1_Q3_PKT_SENT	7:0	SID1_Q3_PKT_SENT_CNT[7:0]							
		15:8	SID1_Q3_PKT_SENT_CNT[15:8]							
		23:16	SID1_Q3_PKT_SENT_CNT[23:16]							
		31:24	SID1_Q3_PKT_SENT_CNT[31:24]							
0x065C	SID2_Q3_PKT_SENT	7:0	SID2_Q3_PKT_SENT_CNT[7:0]							
		15:8	SID2_Q3_PKT_SENT_CNT[15:8]							
		23:16	SID2_Q3_PKT_SENT_CNT[23:16]							
		31:24	SID2_Q3_PKT_SENT_CNT[31:24]							
0x0660	SID1_Q4_PKT_SENT	7:0	SID1_Q4_PKT_SENT_CNT[7:0]							
		15:8	SID1_Q4_PKT_SENT_CNT[15:8]							
		23:16	SID1_Q4_PKT_SENT_CNT[23:16]							
		31:24	SID1_Q4_PKT_SENT_CNT[31:24]							
0x0664	SID2_Q4_PKT_SENT	7:0	SID2_Q4_PKT_SENT_CNT[7:0]							
		15:8	SID2_Q4_PKT_SENT_CNT[15:8]							
		23:16	SID2_Q4_PKT_SENT_CNT[23:16]							
		31:24	SID2_Q4_PKT_SENT_CNT[31:24]							
0x0668	SID1_Q5_PKT_SENT	7:0	SID1_Q5_PKT_SENT_CNT[7:0]							
		15:8	SID1_Q5_PKT_SENT_CNT[15:8]							
		23:16	SID1_Q5_PKT_SENT_CNT[23:16]							
		31:24	SID1_Q5_PKT_SENT_CNT[31:24]							
0x066C	SID2_Q5_PKT_SENT	7:0	SID2_Q5_PKT_SENT_CNT[7:0]							
		15:8	SID2_Q5_PKT_SENT_CNT[15:8]							
		23:16	SID2_Q5_PKT_SENT_CNT[23:16]							
		31:24	SID2_Q5_PKT_SENT_CNT[31:24]							
0x0670	SID1_Q6_PKT_SENT	7:0	SID1_Q6_PKT_SENT_CNT[7:0]							
		15:8	SID1_Q6_PKT_SENT_CNT[15:8]							
		23:16	SID1_Q6_PKT_SENT_CNT[23:16]							
		31:24	SID1_Q6_PKT_SENT_CNT[31:24]							
0x0674	SID2_Q6_PKT_SENT	7:0	SID2_Q6_PKT_SENT_CNT[7:0]							
		15:8	SID2_Q6_PKT_SENT_CNT[15:8]							
		23:16	SID2_Q6_PKT_SENT_CNT[23:16]							
		31:24	SID2_Q6_PKT_SENT_CNT[31:24]							
0x0678	SID1_Q7_PKT_SENT	7:0	SID1_Q7_PKT_SENT_CNT[7:0]							
		15:8	SID1_Q7_PKT_SENT_CNT[15:8]							
		23:16	SID1_Q7_PKT_SENT_CNT[23:16]							
		31:24	SID1_Q7_PKT_SENT_CNT[31:24]							
0x067C	SID2_Q7_PKT_SENT	7:0	SID2_Q7_PKT_SENT_CNT[7:0]							
		15:8	SID2_Q7_PKT_SENT_CNT[15:8]							
		23:16	SID2_Q7_PKT_SENT_CNT[23:16]							
		31:24	SID2_Q7_PKT_SENT_CNT[31:24]							
0x0680	RX_PORT0_DUP_PRMPT_PKTS_DROP	7:0	RX_PORT0_REP_PRMPT_PKTS_DROP[7:0]							
		15:8	RX_PORT0_REP_PRMPT_PKTS_DROP[15:8]							
		23:16	RX_PORT0_REP_PRMPT_PKTS_DROP[23:16]							
		31:24	RX_PORT0_REP_PRMPT_PKTS_DROP[31:24]							
0x0684	RX_PORT0_PRMPT_PKTS_RECEIVED	7:0	RX_PORT0_PRMPT_PKTS_RECEIVED[7:0]							
		15:8	RX_PORT0_PRMPT_PKTS_RECEIVED[15:8]							
		23:16	RX_PORT0_PRMPT_PKTS_RECEIVED[23:16]							
		31:24	RX_PORT0_PRMPT_PKTS_RECEIVED[31:24]							
0x0688	RX_PORT0_EXP_PKTS_DROP	7:0	RX_PORT0_REP_EXP_PKTS_DROP[7:0]							
		15:8	RX_PORT0_REP_EXP_PKTS_DROP[15:8]							
		23:16	RX_PORT0_REP_EXP_PKTS_DROP[23:16]							
		31:24	RX_PORT0_REP_EXP_PKTS_DROP[31:24]							
0x068C	RX_PORT0_EXP_PKTS_RECEIVED	7:0	RX_PORT0_EXP_PKTS_RECEIVED [7:0]							
		15:8	RX_PORT0_EXP_PKTS_RECEIVED [15:8]							
		23:16	RX_PORT0_EXP_PKTS_RECEIVED [23:16]							
		31:24	RX_PORT0_EXP_PKTS_RECEIVED [31:24]							
0x0690	RX_PORT1_DUP_PRMPT_PKTS_DROP	7:0	RX_PORT1_REP_PRMPT_PKTS_DROP[7:0]							
		15:8	RX_PORT1_REP_PRMPT_PKTS_DROP[15:8]							
		23:16	RX_PORT1_REP_PRMPT_PKTS_DROP[23:16]							
		31:24	RX_PORT1_REP_PRMPT_PKTS_DROP[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0694	RX_PORT1_PRMPT_PKTS_RECEIVED	7:0	RX_PORT1_PRMPT_PKTS_RECEIVED[7:0]							
		15:8	RX_PORT1_PRMPT_PKTS_RECEIVED[15:8]							
		23:16	RX_PORT1_PRMPT_PKTS_RECEIVED[23:16]							
		31:24	RX_PORT1_PRMPT_PKTS_RECEIVED[31:24]							
0x0698	RX_PORT1_EXP_PKTS_DROP	7:0	RX_PORT1_REP_EXP_PKTS_DROP[7:0]							
		15:8	RX_PORT1_REP_EXP_PKTS_DROP[15:8]							
		23:16	RX_PORT1_REP_EXP_PKTS_DROP[23:16]							
		31:24	RX_PORT1_REP_EXP_PKTS_DROP[31:24]							
0x069C	RX_PORT1_EXP_PKTS_RECEIVED	7:0	RX_PORT1_EXP_PKTS_RECEIVED [7:0]							
		15:8	RX_PORT1_EXP_PKTS_RECEIVED [15:8]							
		23:16	RX_PORT1_EXP_PKTS_RECEIVED [23:16]							
		31:24	RX_PORT1_EXP_PKTS_RECEIVED [31:24]							
0x06A0	RX_PSFP_PORT0_STRM1_PKT_COUNT	7:0	RX_PSFP_PORT0_STRM1_PKT_RCV[7:0]							
		15:8	RX_PSFP_PORT0_STRM1_PKT_RCV[15:8]							
		23:16	RX_PSFP_PORT0_STRM1_PKT_RCV[23:16]							
		31:24	RX_PSFP_PORT0_STRM1_PKT_RCV[31:24]							
0x06A4	RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP	7:0	RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP [7:0]							
		15:8	RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP [15:8]							
		23:16	RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP [23:16]							
		31:24	RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP [31:24]							
0x06A8	RX_PSFP_PORT0_STRM2_PKT_COUNT	7:0	RX_PSFP_PORT0_STRM2_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT0_STRM2_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT0_STRM2_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT0_STRM2_PKT_RCV [31:24]							
0x06AC	RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP	7:0	RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP [7:0]							
		15:8	RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP [15:8]							
		23:16	RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP [23:16]							
		31:24	RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP [31:24]							
0x06B0	RX_PSFP_PORT0_STRM3_PKT_COUNT	7:0	RX_PSFP_PORT0_STRM3_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT0_STRM3_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT0_STRM3_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT0_STRM3_PKT_RCV [31:24]							
0x06B4	RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP	7:0	RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP[31:24]							
0x06B8	RX_PSFP_PORT0_STRM4_PKT_COUNT	7:0	RX_PSFP_PORT0_STRM4_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT0_STRM4_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT0_STRM4_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT0_STRM4_PKT_RCV [31:24]							
0x06BC	RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP	7:0	RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP [7:0]							
		15:8	RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP [15:8]							
		23:16	RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP [23:16]							
		31:24	RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP [31:24]							
0x06C0	RX_PSFP_PORT0_STRM5_PKT_COUNT	7:0	RX_PSFP_PORT0_STRM5_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT0_STRM5_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT0_STRM5_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT0_STRM5_PKT_RCV [31:24]							
0x06C4	RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP	7:0	RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP [7:0]							
		15:8	RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP [15:8]							
		23:16	RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP [23:16]							
		31:24	RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP [31:24]							
0x06C8	RX_PSFP_PORT0_STRM6_PKT_COUNT	7:0	RX_PSFP_PORT0_STRM6_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT0_STRM6_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT0_STRM6_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT0_STRM6_PKT_RCV [31:24]							
0x06CC	RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP	7:0	RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP [7:0]							
		15:8	RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP [15:8]							
		23:16	RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP [23:16]							
		31:24	RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP [31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x06D0	RX_PSFP_PORT0_STRM7_PKT_COUNT	7:0	RX_PSFP_PORT0_STRM7_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT0_STRM7_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT0_STRM7_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT0_STRM7_PKT_RCV [31:24]							
0x06D4	RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP	7:0	RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP[31:24]							
0x06D8	RX_PSFP_PORT0_STRM8_PKT_COUNT	7:0	RX_PSFP_PORT0_STRM8_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT0_STRM8_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT0_STRM8_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT0_STRM8_PKT_RCV [31:24]							
0x06DC	RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP	7:0	RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP[31:24]							
0x06E0	RX_PSFP_PORT1_STRM1_PKT_COUNT	7:0	RX_PSFP_PORT1_STRM1_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT1_STRM1_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT1_STRM1_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT1_STRM1_PKT_RCV [31:24]							
0x06E4	RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP	7:0	RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP[31:24]							
0x06E8	RX_PSFP_PORT1_STRM2_PKT_COUNT	7:0	RX_PSFP_PORT1_STRM2_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT1_STRM2_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT1_STRM2_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT1_STRM2_PKT_RCV [31:24]							
0x06EC	RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP	7:0	RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP[31:24]							
0x06F0	RX_PSFP_PORT1_STRM3_PKT_COUNT	7:0	RX_PSFP_PORT1_STRM3_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT1_STRM3_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT1_STRM3_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT1_STRM3_PKT_RCV [31:24]							
0x06F4	RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP	7:0	RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP[31:24]							
0x06F8	RX_PSFP_PORT1_STRM4_PKT_COUNT	7:0	RX_PSFP_PORT1_STRM4_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT1_STRM4_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT1_STRM4_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT1_STRM4_PKT_RCV [31:24]							
0x06FC	RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP	7:0	RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP[31:24]							
0x0700	RX_PSFP_PORT1_STRM5_PKT_COUNT	7:0	RX_PSFP_PORT1_STRM5_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT1_STRM5_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT1_STRM5_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT1_STRM5_PKT_RCV [31:24]							
0x0704	RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP	7:0	RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP[31:24]							
0x0708	RX_PSFP_PORT1_STRM6_PKT_COUNT	7:0	RX_PSFP_PORT1_STRM6_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT1_STRM6_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT1_STRM6_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT1_STRM6_PKT_RCV [31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x070C	RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP	7:0	RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP[31:24]							
0x0710	RX_PSFP_PORT1_STRM7_PKT_COUNT	7:0	RX_PSFP_PORT1_STRM7_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT1_STRM7_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT1_STRM7_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT1_STRM7_PKT_RCV [31:24]							
0x0714	RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP	7:0	RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP[31:24]							
0x0718	RX_PSFP_PORT1_STRM8_PKT_COUNT	7:0	RX_PSFP_PORT1_STRM8_PKT_RCV [7:0]							
		15:8	RX_PSFP_PORT1_STRM8_PKT_RCV [15:8]							
		23:16	RX_PSFP_PORT1_STRM8_PKT_RCV [23:16]							
		31:24	RX_PSFP_PORT1_STRM8_PKT_RCV [31:24]							
0x071C	RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP	7:0	RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP[7:0]							
		15:8	RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP[15:8]							
		23:16	RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP[23:16]							
		31:24	RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP[31:24]							
0x0720	TX_PORT0_EXP_CNT	7:0	TX_PORT0_EXP_PKT_SENT[7:0]							
		15:8	TX_PORT0_EXP_PKT_SENT[15:8]							
		23:16	TX_PORT0_EXP_PKT_SENT[23:16]							
		31:24	TX_PORT0_EXP_PKT_SENT[31:24]							
0x0724	TX_PORT0_PREMPT_CNT	7:0	TX_PORT0_PREMPT_PKT_SENT[7:0]							
		15:8	TX_PORT0_PREMPT_PKT_SENT[15:8]							
		23:16	TX_PORT0_PREMPT_PKT_SENT[23:16]							
		31:24	TX_PORT0_PREMPT_PKT_SENT[31:24]							
0x0728	TX_PORT1_EXP_CNT	7:0	TX_PORT1_EXP_PKT_SENT[7:0]							
		15:8	TX_PORT1_EXP_PKT_SENT[15:8]							
		23:16	TX_PORT1_EXP_PKT_SENT[23:16]							
		31:24	TX_PORT1_EXP_PKT_SENT[31:24]							
0x072C	TX_PORT1_PREMPT_CNT	7:0	TX_PORT1_PREMPT_PKT_SENT [7:0]							
		15:8	TX_PORT1_PREMPT_PKT_SENT [15:8]							
		23:16	TX_PORT1_PREMPT_PKT_SENT [23:16]							
		31:24	TX_PORT1_PREMPT_PKT_SENT [31:24]							
0x0730	RX_PORT0_PRMPT_ERROR	7:0	RX_PORT0_PRMPT_ERR_PKTS[7:0]							
		15:8	RX_PORT0_PRMPT_ERR_PKTS[15:8]							
		23:16	RX_PORT0_PRMPT_ERR_PKTS[23:16]							
		31:24	RX_PORT0_PRMPT_ERR_PKTS[31:24]							
0x0734	RX_PORT1_PRMPT_ERROR	7:0	RX_PORT1_PRMPT_ERR_PKTS[7:0]							
		15:8	RX_PORT1_PRMPT_ERR_PKTS[15:8]							
		23:16	RX_PORT1_PRMPT_ERR_PKTS[23:16]							
		31:24	RX_PORT1_PRMPT_ERR_PKTS[31:24]							
0x0738	RX_PORT0_EXP_ERROR	7:0	RX_PORT0_EXP_ERR_PKTS[7:0]							
		15:8	RX_PORT0_EXP_ERR_PKTS[15:8]							
		23:16	RX_PORT0_EXP_ERR_PKTS[23:16]							
		31:24	RX_PORT0_EXP_ERR_PKTS[31:24]							
0x073C	RX_PORT1_EXP_ERROR	7:0	RX_PORT1_EXP_ERR_PKTS[7:0]							
		15:8	RX_PORT1_EXP_ERR_PKTS[15:8]							
		23:16	RX_PORT1_EXP_ERR_PKTS[23:16]							
		31:24	RX_PORT1_EXP_ERR_PKTS[31:24]							
0x0740	RX_PSFP_FM_PORT0_STRM1_PKT_DROP	7:0	RX_PSFP_FM_PORT0_STRM1_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT0_STRM1_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT0_STRM1_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT0_STRM1_PKT_DROP[31:24]							
0x0744	RX_PSFP_FM_PORT0_STRM2_PKT_DROP	7:0	RX_PSFP_FM_PORT0_STRM2_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT0_STRM2_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT0_STRM2_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT0_STRM2_PKT_DROP[31:24]							

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0748	RX_PSFP_FM_PORT0_STRM3_PKT_DROP	7:0	RX_PSFP_FM_PORT0_STRM3_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT0_STRM3_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT0_STRM3_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT0_STRM3_PKT_DROP[31:24]							
0x074C	RX_PSFP_FM_PORT0_STRM4_PKT_DROP	7:0	RX_PSFP_FM_PORT0_STRM4_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT0_STRM4_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT0_STRM4_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT0_STRM4_PKT_DROP[31:24]							
0x0750	RX_PSFP_FM_PORT0_STRM5_PKT_DROP	7:0	RX_PSFP_FM_PORT0_STRM5_PKT_DROP [7:0]							
		15:8	RX_PSFP_FM_PORT0_STRM5_PKT_DROP [15:8]							
		23:16	RX_PSFP_FM_PORT0_STRM5_PKT_DROP [23:16]							
		31:24	RX_PSFP_FM_PORT0_STRM5_PKT_DROP [31:24]							
0x0754	RX_PSFP_FM_PORT0_STRM6_PKT_DROP	7:0	RX_PSFP_FM_PORT0_STRM6_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT0_STRM6_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT0_STRM6_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT0_STRM6_PKT_DROP[31:24]							
0x0758	RX_PSFP_FM_PORT0_STRM7_PKT_DROP	7:0	RX_PSFP_FM_PORT0_STRM7_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT0_STRM7_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT0_STRM7_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT0_STRM7_PKT_DROP[31:24]							
0x075C	RX_PSFP_FM_PORT0_STRM8_PKT_DROP	7:0	RX_PSFP_FM_PORT0_STRM8_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT0_STRM8_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT0_STRM8_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT0_STRM8_PKT_DROP[31:24]							
0x0760	RX_PSFP_FM_PORT1_STRM1_PKT_DROP	7:0	RX_PSFP_FM_PORT1_STRM1_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT1_STRM1_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT1_STRM1_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT1_STRM1_PKT_DROP[31:24]							
0x0764	RX_PSFP_FM_PORT1_STRM2_PKT_DROP	7:0	RX_PSFP_FM_PORT1_STRM2_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT1_STRM2_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT1_STRM2_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT1_STRM2_PKT_DROP[31:24]							
0x0768	RX_PSFP_FM_PORT1_STRM3_PKT_DROP	7:0	RX_PSFP_FM_PORT1_STRM3_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT1_STRM3_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT1_STRM3_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT1_STRM3_PKT_DROP[31:24]							
0x076C	RX_PSFP_FM_PORT1_STRM4_PKT_DROP	7:0	RX_PSFP_FM_PORT1_STRM4_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT1_STRM4_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT1_STRM4_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT1_STRM4_PKT_DROP[31:24]							
0x0770	RX_PSFP_FM_PORT1_STRM5_PKT_DROP	7:0	RX_PSFP_FM_PORT1_STRM5_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT1_STRM5_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT1_STRM5_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT1_STRM5_PKT_DROP[31:24]							
0x0774	RX_PSFP_FM_PORT1_STRM6_PKT_DROP	7:0	RX_PSFP_FM_PORT1_STRM6_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT1_STRM6_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT1_STRM6_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT1_STRM6_PKT_DROP[31:24]							
0x0778	RX_PSFP_FM_PORT1_STRM7_PKT_DROP	7:0	RX_PSFP_FM_PORT1_STRM7_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT1_STRM7_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT1_STRM7_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT1_STRM7_PKT_DROP[31:24]							
0x077C	RX_PSFP_FM_PORT1_STRM8_PKT_DROP	7:0	RX_PSFP_FM_PORT1_STRM8_PKT_DROP[7:0]							
		15:8	RX_PSFP_FM_PORT1_STRM8_PKT_DROP[15:8]							
		23:16	RX_PSFP_FM_PORT1_STRM8_PKT_DROP[23:16]							
		31:24	RX_PSFP_FM_PORT1_STRM8_PKT_DROP[31:24]							
0x0780 ... 0x07FF	Reserved									

TSNREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0800	MAC_TABLE_TIMEOUT	7:0	MAC_ENTRY_TIMEOUT[7:0]							
		15:8	MAC_ENTRY_TIMEOUT[15:8]							
		23:16	MAC_ENTRY_TIMEOUT[23:16]							
		31:24	MAC_ENTRY_TIMEOUT[31:24]							
0x0804	MAX_PKT_SIZE_SUPPORT	7:0	MAX_PKT_SIZE[7:0]							
		15:8	MAX_PKT_SIZE[15:8]							
		23:16	MAX_PKT_SIZE[23:16]							
		31:24	MAX_PKT_SIZE[31:24]							

6.1.1. Version Register (Ask a Question)

Name: Version Register
Offset: 0x11C
Property: Read-only

Version Control Register

Bit	31	30	29	28	27	26	25	24
	MAJOR VERSION[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	MINOR VERSION[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 31:24 – MAJOR VERSION[7:0] Major Version of the IP

Bits 23:16 – MINOR VERSION[7:0] Minor Version of the IP

6.1.2. TX_PORT1_PREMPT_CNT (Ask a Question)

Name: TX_PORT1_PREMPT_CNT
Offset: 0x72C
Reset: 0x0
Property: Clear on Read

Transmitted Preempted Packet Count Register,Port1

Bit	31	30	29	28	27	26	25	24
	TX_PORT1_PREMPT_PKT_SENT [31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TX_PORT1_PREMPT_PKT_SENT [23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TX_PORT1_PREMPT_PKT_SENT [15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TX_PORT1_PREMPT_PKT_SENT [7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TX_PORT1_PREMPT_PKT_SENT [31:0] Preempt packets transmitted on Port1

6.1.3. TX_PORT1_EXP_CNT (Ask a Question)

Name: TX_PORT1_EXP_CNT
Offset: 0x728
Reset: 0x0
Property: Clear on Read

Transmitted Express Packet Count Register,Port1

Bit	31	30	29	28	27	26	25	24
	TX_PORT1_EXP_PKT_SENT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TX_PORT1_EXP_PKT_SENT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TX_PORT1_EXP_PKT_SENT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TX_PORT1_EXP_PKT_SENT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TX_PORT1_EXP_PKT_SENT[31:0] Express packets transmitted on Port1

6.1.4. TX_PORT0_PREMPT_CNT (Ask a Question)

Name: TX_PORT0_PREMPT_CNT
Offset: 0x724
Reset: 0x0
Property: Clear on Read

Transmitted Preempted Packet Count Register,Port0

Bit	31	30	29	28	27	26	25	24
	TX_PORT0_PREMPT_PKT_SENT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TX_PORT0_PREMPT_PKT_SENT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TX_PORT0_PREMPT_PKT_SENT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TX_PORT0_PREMPT_PKT_SENT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TX_PORT0_PREMPT_PKT_SENT[31:0] Preempt packets transmitted on Port0

6.1.5. TX_PORT0_EXP_CNT (Ask a Question)

Name: TX_PORT0_EXP_CNT
Offset: 0x720
Reset: 0x0
Property: Clear on Read

Transmitted Express Packet Count Register,Port0

Bit	31	30	29	28	27	26	25	24
	TX_PORT0_EXP_PKT_SENT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TX_PORT0_EXP_PKT_SENT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TX_PORT0_EXP_PKT_SENT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TX_PORT0_EXP_PKT_SENT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TX_PORT0_EXP_PKT_SENT[31:0] Express packets transmitted on Port0

6.1.6. SID2_Q7_PKT_SENT (Ask a Question)

Name: SID2_Q7_PKT_SENT
Offset: 0x67C
Reset: 0x0
Property: Clear on Read

STREAMID2 Q7 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q7_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q7_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q7_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q7_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q7_PKT_SENT_CNT[31:0] STREAMID2 packet Sent count for Q7

6.1.7. SID2_Q7_PKT_DRP (Ask a Question)

Name: SID2_Q7_PKT_DRP
Offset: 0x63C
Reset: 0x0
Property: Clear on Read

STREAMID2 Q7 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q7_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q7_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q7_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q7_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q7_PKT_DRP_CNT[31:0] STREAMID2 packet drop count for Q7 (Drop when Queue7 is full)

6.1.8. SID2_Q6_PKT_SENT (Ask a Question)

Name: SID2_Q6_PKT_SENT
Offset: 0x674
Reset: 0x0
Property: Clear on Read

STREAMID2 Q6 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q6_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q6_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q6_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q6_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q6_PKT_SENT_CNT[31:0] STREAMID2 packet Sent count for Q6

6.1.9. SID2_Q6_PKT_DRP (Ask a Question)

Name: SID2_Q6_PKT_DRP
Offset: 0x634
Reset: 0x0
Property: Clear on Read

STREAMID2 Q6 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q6_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q6_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q6_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q6_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q6_PKT_DRP_CNT[31:0] STREAMID2 packet drop count for Q6 (Drop when Queue6 is full)

6.1.10. SID2_Q5_PKT_SENT (Ask a Question)

Name: SID2_Q5_PKT_SENT
Offset: 0x66C
Reset: 0x0
Property: Clear on Read

STREAMID2 Q5 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q5_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q5_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q5_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q5_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q5_PKT_SENT_CNT[31:0] STREAMID2 packet Sent count for Q5

6.1.11. SID2_Q5_PKT_DRP (Ask a Question)

Name: SID2_Q5_PKT_DRP
Offset: 0x62C
Reset: 0x0
Property: Clear on Read

STREAMID2 Q5 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q5_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q5_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q5_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q5_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q5_PKT_DRP_CNT[31:0] STREAMID2 packet drop count for Q5 (Drop when Queue5 is full)

6.1.12. SID2_Q4_PKT_SENT (Ask a Question)

Name: SID2_Q4_PKT_SENT
Offset: 0x664
Reset: 0x0
Property: Clear on Read

STREAMID2 Q4 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q4_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q4_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q4_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q4_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q4_PKT_SENT_CNT[31:0] STREAMID2 packet Sent count for Q4

6.1.13. SID2_Q4_PKT_DRP (Ask a Question)

Name: SID2_Q4_PKT_DRP
Offset: 0x624
Reset: 0x0
Property: Clear on Read

STREAMID2 Q4 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q4_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q4_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q4_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q4_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q4_PKT_DRP_CNT[31:0] STREAMID2 packet drop count for Q4 (Drop when Queue4 is full)

6.1.14. SID2_Q3_PKT_SENT (Ask a Question)

Name: SID2_Q3_PKT_SENT
Offset: 0x65C
Reset: 0x0
Property: Clear on Read

STREAMID2 Q3 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q3_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q3_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q3_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q3_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q3_PKT_SENT_CNT[31:0] STREAMID2 packet Sent count for Q3

6.1.15. SID2_Q3_PKT_DRP (Ask a Question)

Name: SID2_Q3_PKT_DRP
Offset: 0x61C
Reset: 0x0
Property: Clear on Read

STREAMID2 Q3 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q3_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q3_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q3_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q3_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q3_PKT_DRP_CNT[31:0] STREAMID2 packet drop count for Q3(Drop when Queue3 is full)

6.1.16. SID2_Q2_PKT_SENT (Ask a Question)

Name: SID2_Q2_PKT_SENT
Offset: 0x654
Reset: 0x0
Property: Clear on Read

STREAMID2 Q2 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q2_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q2_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q2_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q2_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q2_PKT_SENT_CNT[31:0] STREAMID2 packet Sent count for Q2

6.1.17. SID2_Q2_PKT_DRP (Ask a Question)

Name: SID2_Q2_PKT_DRP
Offset: 0x614
Reset: 0x0
Property: Clear on Read

STREAMID2 Q2 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q2_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q2_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q2_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q2_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q2_PKT_DRP_CNT[31:0] STREAMID2 packet drop count for Q2 (Drop when Queue2 is full)

6.1.18. SID2_Q1_PKT_DRP (Ask a Question)

Name: SID2_Q1_PKT_DRP
Offset: 0x60C
Reset: 0x0
Property: Clear on Read

STREAMID2 Q1 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q1_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q1_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q1_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q1_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q1_PKT_DRP_CNT[31:0] STREAMID2 packet drop count for Q1 (Drop when Queue1 is full)

6.1.19. SID2_Q1_PKT_SENT (Ask a Question)

Name: SID2_Q1_PKT_SENT
Offset: 0x64C
Reset: 0x0
Property: Clear on Read

STREAMID2 Q1 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q1_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q1_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q1_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q1_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q1_PKT_SENT_CNT[31:0] STREAMID2 packet Sent count for Q1

6.1.20. SID2_Q0_PKT_SENT (Ask a Question)

Name: SID2_Q0_PKT_SENT
Offset: 0x644
Reset: 0x0
Property: Clear on Read

STREAMID2 Q0 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q0_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q0_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q0_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q0_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q0_PKT_SENT_CNT[31:0] STREAMID2 packet Sent count for Q0

6.1.21. SID2_Q0_PKT_DRP (Ask a Question)

Name: SID2_Q0_PKT_DRP
Offset: 0x604
Reset: 0x0
Property: Clear on Read

STREAMID2 Q0 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID2_Q0_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID2_Q0_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID2_Q0_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID2_Q0_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID2_Q0_PKT_DRP_CNT[31:0] STREAMID2 packet drop count for Q0(Drop when Queue0 is full)

6.1.22. SID2_Mask_Q7 (Ask a Question)

Name: SID2_Mask_Q7
Offset: 0x220
Reset: 0x0
Property: Read/Write

Stream ID2 Queue7 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD2_Q7_PCP_EN	SD2_Q7_VID_EN	SD2_Q7_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD2_Q7_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID2, Q7
[0]	PCP Check Disabled for SID2, Q7

Bit 1 – SD2_Q7_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID2, Q7
[0]	VLAN ID Check Disabled for SID2, Q7

Bit 0 – SD2_Q7_DA_EN

Value	Description
[1]	DA Check Enabled for SID2, Q7
[0]	DA Check Disabled for SID2, Q7

6.1.23. SID2_Mask_Q6 (Ask a Question)

Name: SID2_Mask_Q6
Offset: 0x208
Reset: 0x0
Property: Read/Write

Stream ID2 Queue6 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD2_Q6_PCP_EN	SD2_Q6_VID_EN	SD2_Q6_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD2_Q6_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID2, Q6
[0]	PCP Check Disabled for SID2, Q6

Bit 1 – SD2_Q6_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID2, Q6
[0]	VLAN ID Check Disabled for SID2, Q6

Bit 0 – SD2_Q6_DA_EN

Value	Description
[1]	DA Check Enabled for SID2, Q6
[0]	DA Check Disabled for SID2, Q6

6.1.24. SID2_Mask_Q5 (Ask a Question)

Name: SID2_Mask_Q5
Offset: 0x1F0
Reset: 0x0
Property: Read/Write

Stream ID2 Queue5 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD2_Q5_PCP_EN	SD2_Q5_VID_EN	SD2_Q5_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD2_Q5_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID2, Q5
[0]	PCP Check Disabled for SID2, Q5

Bit 1 – SD2_Q5_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID2, Q5
[0]	VLAN ID Check Disabled for SID2, Q5

Bit 0 – SD2_Q5_DA_EN

Value	Description
[1]	DA Check Enabled for SID2, Q5
[0]	DA Check Disabled for SID2, Q5

6.1.25. SID2_Mask_Q4 (Ask a Question)

Name: SID2_Mask_Q4
Offset: 0x1D8
Reset: 0x0
Property: Read/Write

Stream ID2 Queue4 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD2_Q4_PCP_EN	SD2_Q4_VID_EN	SD2_Q4_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD2_Q4_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID2, Q4
[0]	PCP Check Disabled for SID2, Q4

Bit 1 – SD2_Q4_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID2, Q4
[0]	VLAN ID Check Disabled for SID2, Q4

Bit 0 – SD2_Q4_DA_EN

Value	Description
[1]	DA Check Enabled for SID2, Q4
[0]	DA Check Disabled for SID2, Q4

6.1.26. SID2_Mask_Q3 (Ask a Question)

Name: SID2_Mask_Q3
Offset: 0x1C0
Reset: 0x0
Property: Read/Write

Stream ID2 Queue3 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD2_Q3_PCP_EN	SD2_Q3_VID_EN	SD2_Q3_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD2_Q3_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID2, Q3
[0]	PCP Check Disabled for SID2, Q3

Bit 1 – SD2_Q3_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID2, Q3
[0]	VLAN ID Check Disabled for SID2, Q3

Bit 0 – SD2_Q3_DA_EN

Value	Description
[1]	DA Check Enabled for SID2, Q3
[0]	DA Check Disabled for SID2, Q3

6.1.27. SID2_Mask_Q2 (Ask a Question)

Name: SID2_Mask_Q2
Offset: 0x1A8
Reset: 0x0
Property: Read/Write

Stream ID2 Queue2 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD2_Q2_PCP_EN	SD2_Q2_VID_EN	SD2_Q2_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD2_Q2_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID2, Q2
[0]	PCP Check Disabled for SID2, Q2

Bit 1 – SD2_Q2_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID2, Q2
[0]	VLAN ID Check Disabled for SID2, Q2

Bit 0 – SD2_Q2_DA_EN

Value	Description
[1]	DA Check Enabled for SID2, Q2
[0]	DA Check Disabled for SID2, Q2

6.1.28. SID2_Mask_Q1 (Ask a Question)

Name: SID2_Mask_Q1
Offset: 0x190
Reset: 0x0
Property: Read/Write

Stream ID2 Queue1 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD2_Q1_PCP_EN	SD2_Q1_VID_EN	SD2_Q1_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD2_Q1_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID2, Q1
[0]	PCP Check Disabled for SID2, Q1

Bit 1 – SD2_Q1_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID2, Q1
[0]	VLAN ID Check Disabled for SID2, Q1

Bit 0 – SD2_Q1_DA_EN

Value	Description
[1]	DA Check Enabled for SID2, Q1
[0]	DA Check Disabled for SID2, Q1

6.1.29. SID2_Mask_Q0 (Ask a Question)

Name: SID2_Mask_Q0
Offset: 0x178
Reset: 0x0
Property: Read/Write

Stream ID2 Queue0 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD2_Q0_PCP_EN	SD2_Q0_VID_EN	SD2_Q0_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD2_Q0_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID2, Q0
[0]	PCP Check Disabled for SID2, Q0

Bit 1 – SD2_Q0_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID2, Q0
[0]	VLAN ID Check Disabled for SID2, Q0

Bit 0 – SD2_Q0_DA_EN

Value	Description
[1]	DA Check Enabled for SID2, Q0
[0]	DA Check Disabled for SID2, Q0

6.1.30. SID2_1_Q6 (Ask a Question)

Name: SID2_1_Q6
Offset: 0x204
Reset: 0x0
Property: Read/Write

Stream ID2_1 Queue6

Bit	31	30	29	28	27	26	25	24
	SD2_Q6_FRER_EN	SD2_Q6_PCP[2:0]			SD2_Q6_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q6_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q6_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q6_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD2_Q6_FRER_EN Replication Enabled for Stream ID2,Queue6(valid combinations are DA or DA+VID)

Bits 30:28 – SD2_Q6_PCP[2:0] PCP of Stream ID2 parameter for Queue6

Bits 27:16 – SD2_Q6_VID[11:0] VLAN Identifier of Stream ID2 parameter for Queue6

Bits 15:0 – SD2_Q6_DA_MSB[15:0] Destination address bits [48:32] of Stream ID2 parameter for Queue6

6.1.31. SID2_1_Q7 (Ask a Question)

Name: SID2_1_Q7
Offset: 0x21C
Reset: 0x0
Property: Read/Write

Stream ID2_1 Queue7

Bit	31	30	29	28	27	26	25	24
	SD2_Q7_FRER_EN	SD2_Q7_PCP[2:0]			SD2_Q7_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q7_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q7_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q7_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD2_Q7_FRER_EN Replication Enabled for Stream ID2,Queue7(valid combinations are DA or DA+VID)

Bits 30:28 – SD2_Q7_PCP[2:0] PCP of Stream ID2 parameter for Queue7

Bits 27:16 – SD2_Q7_VID[11:0] VLAN Identifier of Stream ID2 parameter for Queue7

Bits 15:0 – SD2_Q7_DA_MSB[15:0] Destination address bits [48:32] of Stream ID2 parameter for Queue7

6.1.32. SID2_1_Q5 (Ask a Question)

Name: SID2_1_Q5
Offset: 0x1EC
Reset: 0x0
Property: Read/Write

Stream ID2_1 Queue5

Bit	31	30	29	28	27	26	25	24
	SD2_Q5_FRER_EN	SD2_Q5_PCP[2:0]			SD2_Q5_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q5_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q5_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q5_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD2_Q5_FRER_EN Replication Enabled for Stream ID2,Queue5(valid combinations are DA or DA+VID)

Bits 30:28 – SD2_Q5_PCP[2:0] PCP of Stream ID2 parameter for Queue5

Bits 27:16 – SD2_Q5_VID[11:0] VLAN Identifier of Stream ID2 parameter for Queue5

Bits 15:0 – SD2_Q5_DA_MSB[15:0] Destination address bits [48:32] of Stream ID2 parameter for Queue5

6.1.33. SID2_1_Q4 (Ask a Question)

Name: SID2_1_Q4
Offset: 0x1D4
Reset: 0x0
Property: Read/Write

Stream ID2_1 Queue4

Bit	31	30	29	28	27	26	25	24
	SD2_Q4_FRER_EN	SD2_Q4_PCP[2:0]			SD2_Q4_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q4_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q4_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q4_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD2_Q4_FRER_EN Replication Enabled for Stream ID2,Queue4(valid combinations are DA or DA+VID)

Bits 30:28 – SD2_Q4_PCP[2:0] PCP of Stream ID2 parameter for Queue4

Bits 27:16 – SD2_Q4_VID[11:0] VLAN Identifier of Stream ID2 parameter for Queue4

Bits 15:0 – SD2_Q4_DA_MSB[15:0] Destination address bits [48:32] of Stream ID2 parameter for Queue4

6.1.34. SID2_1_Q3 (Ask a Question)

Name: SID2_1_Q3
Offset: 0x1BC
Reset: 0x0
Property: Read/Write

Stream ID2_1 Queue3

Bit	31	30	29	28	27	26	25	24
	SD2_Q3_FRER_EN	SD2_Q3_PCP[2:0]			SD2_Q3_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q3_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q3_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q3_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD2_Q3_FRER_EN Replication Enabled for Stream ID2,Queue3(valid combinations are DA or DA+VID)

Bits 30:28 – SD2_Q3_PCP[2:0] PCP of Stream ID2 parameter for Queue3

Bits 27:16 – SD2_Q3_VID[11:0] VLAN Identifier of Stream ID2 parameter for Queue3

Bits 15:0 – SD2_Q3_DA_MSB[15:0] Destination address bits [48:32] of Stream ID2 parameter for Queue3

6.1.35. SID2_1_Q2 (Ask a Question)

Name: SID2_1_Q2
Offset: 0x1A4
Reset: 0x0
Property: Read/Write

Stream ID2_1 Queue2

Bit	31	30	29	28	27	26	25	24
	SD2_Q2_FRER_EN	SD2_Q2_PCP[2:0]			SD2_Q2_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q2_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q2_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q2_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD2_Q2_FRER_EN Replication Enabled for Stream ID2,Queue2(valid combinations are DA or DA+VID)

Bits 30:28 – SD2_Q2_PCP[2:0] PCP of Stream ID2 parameter for Queue2

Bits 27:16 – SD2_Q2_VID[11:0] VLAN Identifier of Stream ID2 parameter for Queue2

Bits 15:0 – SD2_Q2_DA_MSB[15:0] Destination address bits [48:32] of Stream ID2 parameter for Queue2

6.1.36. SID2_1_Q1 (Ask a Question)

Name: SID2_1_Q1
Offset: 0x18C
Reset: 0x0
Property: Read/Write

Stream ID2_1 Queue1

Bit	31	30	29	28	27	26	25	24
	SD2_Q1_FRER_EN	SD2_Q1_PCP[2:0]			SD2_Q1_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q1_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q1_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q1_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD2_Q1_FRER_EN Replication Enabled for Stream ID2,Queue1(valid combinations are DA or DA+VID)

Bits 30:28 – SD2_Q1_PCP[2:0] PCP of Stream ID2 parameter for Queue1

Bits 27:16 – SD2_Q1_VID[11:0] VLAN Identifier of Stream ID2 parameter for Queue1

Bits 15:0 – SD2_Q1_DA_MSB[15:0] Destination address bits [48:32] of Stream ID2 parameter for Queue1

6.1.37. SID2_1_Q0 (Ask a Question)

Name: SID2_1_Q0
Offset: 0x174
Reset: 0x0
Property: Read/Write

Stream ID2_1 Queue0

Bit	31	30	29	28	27	26	25	24
	SD2_Q0_FRER_EN	SD2_Q0_PCP[2:0]			SD2_Q0_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q0_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q0_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q0_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD2_Q0_FRER_EN Replication Enabled for Stream ID2,Queue0(valid combinations are DA or DA+VID)

Bits 30:28 – SD2_Q0_PCP[2:0] PCP of Stream ID2 parameter for Queue0

Bits 27:16 – SD2_Q0_VID[11:0] VLAN Identifier of Stream ID2 parameter for Queue0

Bits 15:0 – SD2_Q0_DA_MSB[15:0] Destination address bits [48:32] of Stream ID2 parameter for Queue0

6.1.38. SID2_0_Q7 (Ask a Question)

Name: SID2_0_Q7
Offset: 0x218
Reset: 0x0
Property: Read/Write

Stream ID2_0 Queue7

Bit	31	30	29	28	27	26	25	24
	SD2_Q7_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q7_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q7_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q7_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD2_Q7_DA_LSB[31:0] Destination address bits [31:0] of Stream ID2 parameter for Queue7

6.1.39. SID2_0_Q6 (Ask a Question)

Name: SID2_0_Q6
Offset: 0x200
Reset: 0x0
Property: Read/Write

Stream ID2_0 Queue6

Bit	31	30	29	28	27	26	25	24
	SD2_Q6_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q6_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q6_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q6_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD2_Q6_DA_LSB[31:0] Destination address bits [31:0] of Stream ID2 parameter for Queue6

6.1.40. SID2_0_Q5 (Ask a Question)

Name: SID2_0_Q5
Offset: 0x1E8
Reset: 0x0
Property: Read/Write

Stream ID2_0 Queue5

Bit	31	30	29	28	27	26	25	24
	SD2_Q5_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q5_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q5_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q5_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD2_Q5_DA_LSB[31:0] Destination address bits [31:0] of Stream ID2 parameter for Queue5

6.1.41. SID2_0_Q4 (Ask a Question)

Name: SID2_0_Q4
Offset: 0x1D0
Reset: 0x0
Property: Read/Write

Stream ID2_0 Queue4

Bit	31	30	29	28	27	26	25	24
	SD2_Q4_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q4_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q4_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q4_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD2_Q4_DA_LSB[31:0] Destination address bits [31:0] of Stream ID2 parameter for Queue4

6.1.42. SID2_0_Q3 (Ask a Question)

Name: SID2_0_Q3
Offset: 0x1B8
Reset: 0x0
Property: Read/Write

Stream ID2_0 Queue3

Bit	31	30	29	28	27	26	25	24
	SD2_Q3_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q3_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q3_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q3_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD2_Q3_DA_LSB[31:0] Destination address bits [31:0] of Stream ID2 parameter for Queue3

6.1.43. SID2_0_Q2 (Ask a Question)

Name: SID2_0_Q2
Offset: 0x1A0
Reset: 0x0
Property: Read/Write

Stream ID2_0 Queue2

Bit	31	30	29	28	27	26	25	24
	SD2_Q2_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q2_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q2_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q2_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD2_Q2_DA_LSB[31:0] Destination address bits [31:0] of Stream ID2 parameter for Queue2

6.1.44. SID2_0_Q1 (Ask a Question)

Name: SID2_0_Q1
Offset: 0x188
Reset: 0x0
Property: Read/Write

Stream ID2_0 Queue1

Bit	31	30	29	28	27	26	25	24
	SD2_Q1_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q1_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q1_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q1_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD2_Q1_DA_LSB[31:0] Destination address bits [31:0] of Stream ID2 parameter for Queue1

6.1.45. SID2_0_Q0 (Ask a Question)

Name: SID2_0_Q0
Offset: 0x170
Reset: 0x0
Property: Read/Write

Stream ID2_0 Queue0

Bit	31	30	29	28	27	26	25	24
	SD2_Q0_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2_Q0_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD2_Q0_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD2_Q0_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD2_Q0_DA_LSB[31:0] Destination address bits [31:0] of Stream ID2 parameter for Queue0

6.1.46. SID1_Q7_PKT_SENT (Ask a Question)

Name: SID1_Q7_PKT_SENT
Offset: 0x678
Reset: 0x0
Property: Clear on Read

STREAMID1 Q7 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q7_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q7_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q7_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q7_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q7_PKT_SENT_CNT[31:0] STREAMID1 packet Sent count for Q7

6.1.47. SID1_Q7_PKT_DRP (Ask a Question)

Name: SID1_Q7_PKT_DRP
Offset: 0x638
Reset: 0x0
Property: Clear on Read

STREAMID1 Q7 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q7_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q7_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q7_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q7_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q7_PKT_DRP_CNT[31:0] STREAMID1 packet drop count for Q7 (Drop when Queue7 is full)

6.1.48. SID1_Q6_PKT_SENT (Ask a Question)

Name: SID1_Q6_PKT_SENT
Offset: 0x670
Reset: 0x0
Property: Clear on Read

STREAMID1 Q6 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q6_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q6_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q6_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q6_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q6_PKT_SENT_CNT[31:0] STREAMID1 packet Sent count for Q6

6.1.49. SID1_Q6_PKT_DRP (Ask a Question)

Name: SID1_Q6_PKT_DRP
Offset: 0x630
Reset: 0x0
Property: Clear on Read

STREAMID1 Q6 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q6_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q6_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q6_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q6_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q6_PKT_DRP_CNT[31:0] STREAMID1 packet drop count for Q6 (Drop when Queue6 is full)

6.1.50. SID1_Q5_PKT_SENT (Ask a Question)

Name: SID1_Q5_PKT_SENT
Offset: 0x668
Reset: 0x0
Property: Clear on Read

STREAMID1 Q5 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q5_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q5_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q5_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q5_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q5_PKT_SENT_CNT[31:0] STREAMID1 packet Sent count for Q5

6.1.51. SID1_Q5_PKT_DRP (Ask a Question)

Name: SID1_Q5_PKT_DRP
Offset: 0x628
Reset: 0x0
Property: Clear on Read

STREAMID1 Q5 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q5_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q5_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q5_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q5_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q5_PKT_DRP_CNT[31:0] STREAMID1 packet drop count for Q5 (Drop when Queue5 is full)

6.1.52. SID1_Q4_PKT_SENT (Ask a Question)

Name: SID1_Q4_PKT_SENT
Offset: 0x660
Reset: 0x0
Property: Clear on Read

STREAMID1 Q4 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q4_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q4_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q4_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q4_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q4_PKT_SENT_CNT[31:0] STREAMID1 packet Sent count for Q4

6.1.53. SID1_Q4_PKT_DRP (Ask a Question)

Name: SID1_Q4_PKT_DRP
Offset: 0x620
Reset: 0x0
Property: Clear on Read

STREAMID1 Q4 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q4_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q4_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q4_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q4_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q4_PKT_DRP_CNT[31:0] STREAMID1 packet drop count for Q4 (Drop when Queue4 is full)

6.1.54. SID1_Q3_PKT_SENT (Ask a Question)

Name: SID1_Q3_PKT_SENT
Offset: 0x658
Reset: 0x0
Property: Clear on Read

STREAMID1 Q3 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q3_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q3_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q3_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q3_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q3_PKT_SENT_CNT[31:0] STREAMID1 packet Sent count for Q3

6.1.55. SID1_Q3_PKT_DRP (Ask a Question)

Name: SID1_Q3_PKT_DRP
Offset: 0x618
Reset: 0x0
Property: Clear on Read

STREAMID1 Q3 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q3_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q3_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q3_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q3_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q3_PKT_DRP_CNT[31:0] STREAMID1 packet drop count for Q3(Drop when Queue3 is full)

6.1.56. SID1_Q2_PKT_SENT (Ask a Question)

Name: SID1_Q2_PKT_SENT
Offset: 0x650
Reset: 0x0
Property: Clear on Read

STREAMID1 Q2 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q2_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q2_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q2_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q2_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q2_PKT_SENT_CNT[31:0] STREAMID1 packet Sent count for Q2

6.1.57. SID1_Q2_PKT_DRP (Ask a Question)

Name: SID1_Q2_PKT_DRP
Offset: 0x610
Reset: 0x0
Property: Clear on Read

STREAMID1 Q2 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q2_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q2_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q2_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q2_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q2_PKT_DRP_CNT[31:0] STREAMID1 packet drop count for Q2(Drop when Queue2 is full)

6.1.58. SID1_Q1_PKT_SENT (Ask a Question)

Name: SID1_Q1_PKT_SENT
Offset: 0x648
Reset: 0x0
Property: Clear on Read

STREAMID1 Q1 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q1_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q1_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q1_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q1_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q1_PKT_SENT_CNT[31:0] STREAMID1 packet Sent count for Q1

6.1.59. SID1_Q1_PKT_DRP (Ask a Question)

Name: SID1_Q1_PKT_DRP
Offset: 0x608
Reset: 0x0
Property: Clear on Read

STREAMID1 Q1 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q1_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q1_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q1_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q1_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q1_PKT_DRP_CNT[31:0] STREAMID1 packet drop count for Q1(Drop when Queue1 is full)

6.1.60. SID1_Q0_PKT_SENT (Ask a Question)

Name: SID1_Q0_PKT_SENT
Offset: 0x640
Reset: 0x0
Property: Clear on Read

STREAMID1 Q0 Packets Sent Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q0_PKT_SENT_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q0_PKT_SENT_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q0_PKT_SENT_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q0_PKT_SENT_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q0_PKT_SENT_CNT[31:0] STREAMID1 packet Sent count for Q0

6.1.61. SID1_Q0_PKT_DRP (Ask a Question)

Name: SID1_Q0_PKT_DRP
Offset: 0x600
Reset: 0x0
Property: Clear on Read

STREAMID1 Q0 Packets Drop Count Register

Bit	31	30	29	28	27	26	25	24
	SID1_Q0_PKT_DRP_CNT[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SID1_Q0_PKT_DRP_CNT[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SID1_Q0_PKT_DRP_CNT[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SID1_Q0_PKT_DRP_CNT[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SID1_Q0_PKT_DRP_CNT[31:0] STREAMID1 packet drop count for Q0(Drop when Queue0 is full)

6.1.62. SID1_Mask_Q7 (Ask a Question)

Name: SID1_Mask_Q7
Offset: 0x214
Reset: 0x0
Property: Read/Write

Stream ID1 Queue7 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD1_Q7_PCP_EN	SD1_Q7_VID_EN	SD1_Q7_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD1_Q7_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID1, Q7
[0]	PCP Check Disabled for SID1, Q7

Bit 1 – SD1_Q7_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID1, Q7
[0]	VLAN ID Check Disabled for SID1, Q7

Bit 0 – SD1_Q7_DA_EN

Value	Description
[1]	DA Check Enabled for SID1, Q7
[0]	DA Check Disabled for SID1, Q7

6.1.63. SID1_Mask_Q6 (Ask a Question)

Name: SID1_Mask_Q6
Offset: 0x1FC
Reset: 0x0
Property: Read/Write

Stream ID1 Queue6 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD1_Q6_PCP_EN	SD1_Q6_VID_EN	SD1_Q6_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD1_Q6_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID1, Q6
[0]	PCP Check Disabled for SID1, Q6

Bit 1 – SD1_Q6_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID1, Q6
[0]	VLAN ID Check Disabled for SID1, Q6

Bit 0 – SD1_Q6_DA_EN

Value	Description
[1]	DA Check Enabled for SID1, Q6
[0]	DA Check Disabled for SID1, Q6

6.1.64. SID1_Mask_Q5 (Ask a Question)

Name: SID1_Mask_Q5
Offset: 0x1E4
Reset: 0x0
Property: Read/Write

Stream ID1 Queue5 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD1_Q5_PCP_EN	SD1_Q5_VID_EN	SD1_Q5_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD1_Q5_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID1, Q5
[0]	PCP Check Disabled for SID1, Q5

Bit 1 – SD1_Q5_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID1, Q5
[0]	VLAN ID Check Disabled for SID1, Q5

Bit 0 – SD1_Q5_DA_EN

Value	Description
[1]	DA Check Enabled for SID1, Q5
[0]	DA Check Disabled for SID1, Q5

6.1.65. SID1_Mask_Q4 (Ask a Question)

Name: SID1_Mask_Q4
Offset: 0x1CC
Reset: 0x0
Property: Read/Write

Stream ID1 Queue4 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD1_Q4_PCP_EN	SD1_Q4_VID_EN	SD1_Q4_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD1_Q4_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID1, Q4
[0]	PCP Check Disabled for SID1, Q4

Bit 1 – SD1_Q4_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID1, Q4
[0]	VLAN ID Check Disabled for SID1, Q4

Bit 0 – SD1_Q4_DA_EN

Value	Description
[1]	DA Check Enabled for SID1, Q4
[0]	DA Check Disabled for SID1, Q4

6.1.66. SID1_Mask_Q3 (Ask a Question)

Name: SID1_Mask_Q3
Offset: 0x1B4
Reset: 0x0
Property: Read/Write

Stream ID1 Queue3 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD1_Q3_PCP_EN	SD1_Q3_VID_EN	SD1_Q3_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD1_Q3_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID1, Q3
[0]	PCP Check Disabled for SID1, Q3

Bit 1 – SD1_Q3_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID1, Q3
[0]	VLAN ID Check Disabled for SID1, Q3

Bit 0 – SD1_Q3_DA_EN

Value	Description
[1]	DA Check Enabled for SID1, Q3
[0]	DA Check Disabled for SID1, Q3

6.1.67. SID1_Mask_Q2 (Ask a Question)

Name: SID1_Mask_Q2
Offset: 0x19C
Reset: 0x0
Property: Read/Write

Stream ID1 Queue2 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD1_Q2_PCP_EN	SD1_Q2_VID_EN	SD1_Q2_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD1_Q2_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID1, Q2
[0]	PCP Check Disabled for SID1, Q2

Bit 1 – SD1_Q2_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID1, Q2
[0]	VLAN ID Check Disabled for SID1, Q2

Bit 0 – SD1_Q2_DA_EN

Value	Description
[1]	DA Check Enabled for SID1, Q2
[0]	DA Check Disabled for SID1, Q2

6.1.68. SID1_Mask_Q1 (Ask a Question)

Name: SID1_Mask_Q1
Offset: 0x184
Reset: 0x0
Property: Read/Write

Stream ID1 Queue1 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD1_Q1_PCP_EN	SD1_Q1_VID_EN	SD1_Q1_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD1_Q1_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID1, Q1
[0]	PCP Check Disabled for SID1, Q1

Bit 1 – SD1_Q1_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID1, Q1
[0]	VLAN ID Check Disabled for SID1, Q1

Bit 0 – SD1_Q1_DA_EN

Value	Description
[1]	DA Check Enabled for SID1, Q1
[0]	DA Check Disabled for SID1, Q1

6.1.69. SID1_Mask_Q0 (Ask a Question)

Name: SID1_Mask_Q0
Offset: 0x16C
Reset: 0x0
Property: Read/Write

Stream ID1 Queue0 Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						SD1_Q0_PCP_EN	SD1_Q0_VID_EN	SD1_Q0_DA_EN
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SD1_Q0_PCP_EN

Value	Description
[1]	PCP Check Enabled for SID1, Q0
[0]	PCP Check Disabled for SID1, Q0

Bit 1 – SD1_Q0_VID_EN

Value	Description
[1]	VLAN ID Check Enabled for SID1, Q0
[0]	VLAN ID Check Disabled for SID1, Q0

Bit 0 – SD1_Q0_DA_EN

Value	Description
[1]	DA Check Enabled for SID1, Q0
[0]	DA Check Disabled for SID1, Q0

6.1.70. SID1_1_Q7 (Ask a Question)

Name: SID1_1_Q7
Offset: 0x210
Reset: 0x0
Property: Read/Write

Stream ID1_1 Queue7

Bit	31	30	29	28	27	26	25	24
	SD1_Q7_FRER_EN	SD1_Q7_PCP[2:0]			SD1_Q7_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q7_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q7_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q7_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD1_Q7_FRER_EN Replication Enabled for Stream ID1,Queue7(valid combinations are DA or DA+VID)

Bits 30:28 – SD1_Q7_PCP[2:0] PCP of Stream ID1 parameter for Queue7

Bits 27:16 – SD1_Q7_VID[11:0] VLAN Identifier of Stream ID1 parameter for Queue7

Bits 15:0 – SD1_Q7_DA_MSB[15:0] Destination address bits [48:32] of Stream ID1 parameter for Queue7

6.1.71. SID1_1_Q6 (Ask a Question)

Name: SID1_1_Q6
Offset: 0x1F8
Reset: 0x0
Property: Read/Write

Stream ID1_1 Queue6

Bit	31	30	29	28	27	26	25	24
	SD1_Q6_FRER_EN	SD1_Q6_PCP[2:0]			SD1_Q6_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q6_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q6_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q6_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD1_Q6_FRER_EN Replication Enabled for Stream ID1,Queue6(valid combinations are DA or DA+VID)

Bits 30:28 – SD1_Q6_PCP[2:0] PCP of Stream ID1 parameter for Queue6

Bits 27:16 – SD1_Q6_VID[11:0] VLAN Identifier of Stream ID1 parameter for Queue6

Bits 15:0 – SD1_Q6_DA_MSB[15:0] Destination address bits [48:32] of Stream ID1 parameter for Queue6

6.1.72. SID1_1_Q5 (Ask a Question)

Name: SID1_1_Q5
Offset: 0x1E0
Reset: 0x0
Property: Read/Write

Stream ID1_1 Queue5

Bit	31	30	29	28	27	26	25	24
	SD1_Q5_FRER_EN	SD1_Q5_PCP[2:0]			SD1_Q5_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q5_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q5_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q5_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD1_Q5_FRER_EN Replication Enabled for Stream ID1,Queue5(valid combinations are DA or DA+VID)

Bits 30:28 – SD1_Q5_PCP[2:0] PCP of Stream ID1 parameter for Queue5

Bits 27:16 – SD1_Q5_VID[11:0] VLAN Identifier of Stream ID1 parameter for Queue5

Bits 15:0 – SD1_Q5_DA_MSB[15:0] Destination address bits [48:32] of Stream ID1 parameter for Queue5

6.1.73. SID1_1_Q4 (Ask a Question)

Name: SID1_1_Q4
Offset: 0x1C8
Reset: 0x0
Property: Read/Write

Stream ID1_1 Queue4

Bit	31	30	29	28	27	26	25	24
	SD1_Q4_FRER_EN	SD1_Q4_PCP[2:0]			SD1_Q4_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q4_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q4_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q4_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD1_Q4_FRER_EN Replication Enabled for Stream ID1,Queue4(valid combinations are DA or DA+VID)

Bits 30:28 – SD1_Q4_PCP[2:0] PCP of Stream ID1 parameter for Queue4

Bits 27:16 – SD1_Q4_VID[11:0] VLAN Identifier of Stream ID1 parameter for Queue4

Bits 15:0 – SD1_Q4_DA_MSB[15:0] Destination address bits [48:32] of Stream ID1 parameter for Queue4

6.1.74. SID1_1_Q3 (Ask a Question)

Name: SID1_1_Q3
Offset: 0x1B0
Reset: 0x0
Property: Read/Write

Stream ID1_1 Queue3

Bit	31	30	29	28	27	26	25	24
	SD1_Q3_FRER_EN	SD1_Q3_PCP[2:0]			SD1_Q3_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q3_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q3_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q3_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD1_Q3_FRER_EN Replication Enabled for Stream ID1,Queue3(valid combinations are DA or DA+VID)

Bits 30:28 – SD1_Q3_PCP[2:0] PCP of Stream ID1 parameter for Queue3

Bits 27:16 – SD1_Q3_VID[11:0] VLAN Identifier of Stream ID1 parameter for Queue3

Bits 15:0 – SD1_Q3_DA_MSB[15:0] Destination address bits [48:32] of Stream ID1 parameter for Queue3

6.1.75. SID1_1_Q2 (Ask a Question)

Name: SID1_1_Q2
Offset: 0x198
Reset: 0x0
Property: Read/Write

Stream ID1_1 Queue2

Bit	31	30	29	28	27	26	25	24
	SD1_Q2_FRER_EN	SD1_Q2_PCP[2:0]			SD1_Q2_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q2_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q2_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q2_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD1_Q2_FRER_EN Replication Enabled for Stream ID1,Queue2(valid combinations are DA or DA+VID)

Bits 30:28 – SD1_Q2_PCP[2:0] PCP of Stream ID1 parameter for Queue2

Bits 27:16 – SD1_Q2_VID[11:0] VLAN Identifier of Stream ID1 parameter for Queue2

Bits 15:0 – SD1_Q2_DA_MSB[15:0] Destination address bits [48:32] of Stream ID1 parameter for Queue2

6.1.76. SID1_1_Q1 (Ask a Question)

Name: SID1_1_Q1
Offset: 0x180
Reset: 0x0
Property: Read/Write

Stream ID1_1 Queue1

Bit	31	30	29	28	27	26	25	24
	SD1_Q1_FRER_EN	SD1_Q1_PCP[2:0]			SD1_Q1_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q1_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q1_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q1_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD1_Q1_FRER_EN Replication Enabled for Stream ID1,Queue1(valid combinations are DA or DA+VID)

Bits 30:28 – SD1_Q1_PCP[2:0] PCP of Stream ID1 parameter for Queue1

Bits 27:16 – SD1_Q1_VID[11:0] VLAN Identifier of Stream ID1 parameter for Queue1

Bits 15:0 – SD1_Q1_DA_MSB[15:0] Destination address bits [48:32] of Stream ID1 parameter for Queue1

6.1.77. SID1_1_Q0 (Ask a Question)

Name: SID1_1_Q0
Offset: 0x168
Reset: 0x0
Property: Read/Write

Stream ID1_1 Queue0

Bit	31	30	29	28	27	26	25	24
	SD1_Q0_FRER_EN	SD1_Q0_PCP[2:0]			SD1_Q0_VID[11:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q0_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q0_DA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q0_DA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – SD1_Q0_FRER_EN Replication Enabled for Stream ID1,Queue0(valid combinations are DA or DA+VID)

Bits 30:28 – SD1_Q0_PCP[2:0] PCP of Stream ID1 parameter for Queue0

Bits 27:16 – SD1_Q0_VID[11:0] VLAN Identifier of Stream ID1 parameter for Queue0

Bits 15:0 – SD1_Q0_DA_MSB[15:0] Destination address bits [48:32] of Stream ID1 parameter for Queue0

6.1.78. SID1_0_Q7 (Ask a Question)

Name: SID1_0_Q7
Offset: 0x20C
Reset: 0x0
Property: Read/Write

Stream ID1_0 Queue7

Bit	31	30	29	28	27	26	25	24
	SD1_Q7_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q7_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q7_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q7_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD1_Q7_DA_LSB[31:0] Destination address bits [31:0] of Stream ID1 parameter for Queue7

6.1.79. SID1_0_Q6 (Ask a Question)

Name: SID1_0_Q6
Offset: 0x1F4
Reset: 0x0
Property: Read/Write

Stream ID1_0 Queue6

Bit	31	30	29	28	27	26	25	24
	SD1_Q6_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q6_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q6_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q6_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD1_Q6_DA_LSB[31:0] Destination address bits [31:0] of Stream ID1 parameter for Queue6

6.1.80. SID1_0_Q5 (Ask a Question)

Name: SID1_0_Q5
Offset: 0x1DC
Reset: 0x0
Property: Read/Write

Stream ID1_0 Queue5

Bit	31	30	29	28	27	26	25	24
	SD1_Q5_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q5_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q5_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q5_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD1_Q5_DA_LSB[31:0] Destination address bits [31:0] of Stream ID1 parameter for Queue5

6.1.81. SID1_0_Q4 (Ask a Question)

Name: SID1_0_Q4
Offset: 0x1C4
Reset: 0x0
Property: Read/Write

Stream ID1_0 Queue4

Bit	31	30	29	28	27	26	25	24
	SD1_Q4_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q4_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q4_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q4_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD1_Q4_DA_LSB[31:0] Destination address bits [31:0] of Stream ID1 parameter for Queue4

6.1.82. SID1_0_Q3 (Ask a Question)

Name: SID1_0_Q3
Offset: 0x1AC
Reset: 0x0
Property: Read/Write

Stream ID1_0 Queue3

Bit	31	30	29	28	27	26	25	24
	SD1_Q3_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q3_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q3_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q3_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD1_Q3_DA_LSB[31:0] Destination address bits [31:0] of Stream ID1 parameter for Queue3

6.1.83. SID1_0_Q2 (Ask a Question)

Name: SID1_0_Q2
Offset: 0x194
Reset: 0x0
Property: Read/Write

Stream ID1_0 Queue2

Bit	31	30	29	28	27	26	25	24
	SD1_Q2_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q2_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q2_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q2_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD1_Q2_DA_LSB[31:0] Destination address bits [31:0] of Stream ID1 parameter for Queue2

6.1.84. SID1_0_Q1 (Ask a Question)

Name: SID1_0_Q1
Offset: 0x17C
Reset: 0x0
Property: Read/Write

Stream ID1_0 Queue1

Bit	31	30	29	28	27	26	25	24
	SD1_Q1_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q1_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q1_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q1_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD1_Q1_DA_LSB[31:0] Destination address bits [31:0] of Stream ID1 parameter for Queue1

6.1.85. SID1_0_Q0 (Ask a Question)

Name: SID1_0_Q0
Offset: 0x164
Reset: 0x0
Property: Read/Write

Stream ID1_0 Queue0

Bit	31	30	29	28	27	26	25	24
	SD1_Q0_DA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD1_Q0_DA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1_Q0_DA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD1_Q0_DA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SD1_Q0_DA_LSB[31:0] Destination address bits [31:0] of Stream ID1 parameter for Queue0

6.1.86. Scheduler Cycle Time (Ask a Question)

Name: Scheduler Cycle Time
Offset: 0x060
Reset: 0x0
Property: Read/Write

Scheduler Cycle Time Register

Bit	31	30	29	28	27	26	25	24
	SCHEDULER CYCLE TIME[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SCHEDULER CYCLE TIME[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SCHEDULER CYCLE TIME[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SCHEDULER CYCLE TIME[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SCHEDULER CYCLE TIME[31:0] Configured number of clock cycles are counted. The Cycle is repeated after the cycle time, until gate control is disabled.

6.1.87. Scheduler Control List Length (Ask a Question)

Name: Scheduler Control List Length
Offset: 0x084
Reset: 0x0
Property: Read/Write

Scheduler Control List Length Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				CTRL_LIST_LENGTH[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CTRL_LIST_LENGTH[4:0] Number of entries that will be valid in the control list. Range 0-31

6.1.88. RX_SID_RST_TIMER (Ask a Question)

Name: RX_SID_RST_TIMER
Offset: 0x240
Reset: 0xbebc1f
Property: Read/Write

Receiver Stream ID Reset Timer Register

Bit	31	30	29	28	27	26	25	24
	RX_STREMID_RST_TIMER[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_STREMID_RST_TIMER[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	1	1	1	1	1	0

Bit	15	14	13	12	11	10	9	8
	RX_STREMID_RST_TIMER[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	1	1	1	1	0	0

Bit	7	6	5	4	3	2	1	0
	RX_STREMID_RST_TIMER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	1

Bits 31:0 – RX_STREMID_RST_TIMER[31:0] Receiver Stream ID Reset timer, clear the Receive Stream ID entry in the table after the timeout period specified, if no frames pertaining to that streamID are received

6.1.89. RX_PSFP_PORT1_STRM8_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT1_STRM8_PKT_COUNT
Offset: 0x718
Reset: 0x0
Property: Read/Write

Filtering/Policing SID8 Count Register (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT1_STRM8_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT1_STRM8_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT1_STRM8_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT1_STRM8_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT1_STRM8_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID8, Port1

6.1.90. RX_PSFP_PORT1_STRM7_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT1_STRM7_PKT_COUNT
Offset: 0x710
Reset: 0x0
Property: Read/Write

Filtering/Policing SID7 Count Register (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT1_STRM7_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT1_STRM7_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT1_STRM7_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT1_STRM7_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT1_STRM7_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID7, Port1

6.1.91. RX_PSFP_PORT1_STRM6_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT1_STRM6_PKT_COUNT
Offset: 0x708
Reset: 0x0
Property: Read/Write

Filtering/Policing SID6 Count Register (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT1_STRM6_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT1_STRM6_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT1_STRM6_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT1_STRM6_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT1_STRM6_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID6, Port1

6.1.92. RX_PSFP_PORT1_STRM5_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT1_STRM5_PKT_COUNT
Offset: 0x700
Reset: 0x0
Property: Read/Write

Filtering/Policing SID5 Count Register (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT1_STRM5_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT1_STRM5_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT1_STRM5_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT1_STRM5_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT1_STRM5_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID5, Port1

6.1.93. RX_PSFP_PORT1_STRM4_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT1_STRM4_PKT_COUNT
Offset: 0x6F8
Reset: 0x0
Property: Read/Write

Filtering/Policing SID4 Count Register (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT1_STRM4_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT1_STRM4_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT1_STRM4_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT1_STRM4_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT1_STRM4_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID4, Port1

6.1.94. RX_PSFP_PORT1_STRM3_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT1_STRM3_PKT_COUNT
Offset: 0x6F0
Reset: 0x0
Property: Read/Write

Filtering/Policing SID3 Count Register (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT1_STRM3_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT1_STRM3_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT1_STRM3_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT1_STRM3_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT1_STRM3_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID3, Port1

6.1.95. RX_PSFP_PORT1_STRM2_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT1_STRM2_PKT_COUNT
Offset: 0x6E8
Reset: 0x0
Property: Read/Write

Filtering/Policing SID2 Count Register (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT1_STRM2_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT1_STRM2_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT1_STRM2_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT1_STRM2_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT1_STRM2_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID2, Port1

6.1.96. RX_PSFP_PORT1_STRM1_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT1_STRM1_PKT_COUNT
Offset: 0x6E0
Reset: 0x0
Property: Read/Write

Filtering/Policing SID1 Count Register (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT1_STRM1_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT1_STRM1_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT1_STRM1_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT1_STRM1_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT1_STRM1_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID1, Port1

6.1.97. RX_PSFP_PORT0_STRM8_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT0_STRM8_PKT_COUNT
Offset: 0x6D8
Reset: 0x0
Property: Read/Write

Filtering/Policing SID8 Count Register (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT0_STRM8_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT0_STRM8_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT0_STRM8_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT0_STRM8_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT0_STRM8_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID8, Port0

6.1.98. RX_PSFP_PORT0_STRM7_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT0_STRM7_PKT_COUNT
Offset: 0x6D0
Reset: 0x0
Property: Read/Write

Filtering/Policing SID7 Count Register (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT0_STRM7_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT0_STRM7_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT0_STRM7_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT0_STRM7_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT0_STRM7_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID7, Port0

6.1.99. RX_PSFP_PORT0_STRM6_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT0_STRM6_PKT_COUNT
Offset: 0x6C8
Reset: 0x0
Property: Read/Write

Filtering/Policing SID6 Count Register (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT0_STRM6_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT0_STRM6_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT0_STRM6_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT0_STRM6_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT0_STRM6_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID6, Port0

6.1.100. RX_PSFP_PORT0_STRM5_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT0_STRM5_PKT_COUNT
Offset: 0x6C0
Reset: 0x0
Property: Read/Write

Filtering/Policing SID5 Count Register (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT0_STRM5_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT0_STRM5_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT0_STRM5_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT0_STRM5_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT0_STRM5_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID5, Port0

6.1.101. RX_PSFP_PORT0_STRM4_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT0_STRM4_PKT_COUNT
Offset: 0x6B8
Reset: 0x0
Property: Read/Write

Filtering/Policing SID4 Count Register (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT0_STRM4_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT0_STRM4_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT0_STRM4_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT0_STRM4_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT0_STRM4_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID4, Port0

6.1.102. RX_PSFP_PORT0_STRM3_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT0_STRM3_PKT_COUNT
Offset: 0x6B0
Reset: 0x0
Property: Read/Write

Filtering/Policing SID3 Count Register (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT0_STRM3_PKT_RCV [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT0_STRM3_PKT_RCV [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT0_STRM3_PKT_RCV [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT0_STRM3_PKT_RCV [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT0_STRM3_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID3, Port0

6.1.103. RX_PSFP_PORT0_STRM2_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT0_STRM2_PKT_COUNT
Offset: 0x6A8
Reset: 0x0
Property: Clear on Read

Filtering/Policing SID2 Count Register (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT0_STRM2_PKT_RCV [31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT0_STRM2_PKT_RCV [23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT0_STRM2_PKT_RCV [15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT0_STRM2_PKT_RCV [7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT0_STRM2_PKT_RCV [31:0] Gives the count of the packets received by the PSFP Block for STREAMID2, Port0

6.1.104. RX_PSFP_PORT0_STRM1_PKT_COUNT (Ask a Question)

Name: RX_PSFP_PORT0_STRM1_PKT_COUNT
Offset: 0x6A0
Reset: 0x0
Property: Clear on Read

Filtering/Policing SID1 Count Register (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_PORT0_STRM1_PKT_RCV[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_PORT0_STRM1_PKT_RCV[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_PORT0_STRM1_PKT_RCV[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_PORT0_STRM1_PKT_RCV[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_PORT0_STRM1_PKT_RCV[31:0] Gives the count of the packets received by the PSFP Block for STREAMID1, Port0

6.1.105. RX_PSFP_FM_PORT1_STRM8_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT1_STRM8_PKT_DROP
Offset: 0x77C
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID8 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT1_STRM8_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT1_STRM8_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT1_STRM8_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT1_STRM8_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT1_STRM8_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID8, Port1

6.1.106. RX_PSFP_FM_PORT1_STRM7_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT1_STRM7_PKT_DROP
Offset: 0x778
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID7 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT1_STRM7_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT1_STRM7_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT1_STRM7_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT1_STRM7_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT1_STRM7_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID7, Port1

6.1.107. RX_PSFP_FM_PORT1_STRM6_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT1_STRM6_PKT_DROP
Offset: 0x774
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID6 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT1_STRM6_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT1_STRM6_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT1_STRM6_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT1_STRM6_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT1_STRM6_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID6, Port1

6.1.108. RX_PSFP_FM_PORT1_STRM5_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT1_STRM5_PKT_DROP
Offset: 0x770
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID5 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT1_STRM5_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT1_STRM5_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT1_STRM5_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT1_STRM5_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT1_STRM5_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID5, Port1

6.1.109. RX_PSFP_FM_PORT1_STRM4_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT1_STRM4_PKT_DROP
Offset: 0x76C
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID4 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT1_STRM4_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT1_STRM4_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT1_STRM4_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT1_STRM4_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT1_STRM4_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID4, Port1

6.1.110. RX_PSFP_FM_PORT1_STRM3_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT1_STRM3_PKT_DROP
Offset: 0x768
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID3 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT1_STRM3_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT1_STRM3_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT1_STRM3_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT1_STRM3_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT1_STRM3_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID3, Port1

6.1.111. RX_PSFP_FM_PORT1_STRM2_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT1_STRM2_PKT_DROP
Offset: 0x764
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID2 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT1_STRM2_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT1_STRM2_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT1_STRM2_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT1_STRM2_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT1_STRM2_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID2, Port1

6.1.112. RX_PSFP_FM_PORT1_STRM1_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT1_STRM1_PKT_DROP
Offset: 0x760
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID1 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT1_STRM1_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT1_STRM1_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT1_STRM1_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT1_STRM1_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT1_STRM1_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID1, Port1

6.1.113. RX_PSFP_FM_PORT0_STRM8_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT0_STRM8_PKT_DROP
Offset: 0x75C
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID8 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT0_STRM8_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT0_STRM8_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT0_STRM8_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT0_STRM8_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT0_STRM8_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID8, Port0

6.1.114. RX_PSFP_FM_PORT0_STRM7_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT0_STRM7_PKT_DROP
Offset: 0x758
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID7 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT0_STRM7_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT0_STRM7_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT0_STRM7_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT0_STRM7_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT0_STRM7_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID7, Port0

6.1.115. RX_PSFP_FM_PORT0_STRM6_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT0_STRM6_PKT_DROP
Offset: 0x754
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID6 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT0_STRM6_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT0_STRM6_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT0_STRM6_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT0_STRM6_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT0_STRM6_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID6, Port0

6.1.116. RX_PSFP_FM_PORT0_STRM5_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT0_STRM5_PKT_DROP
Offset: 0x750
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID5 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT0_STRM5_PKT_DROP [31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT0_STRM5_PKT_DROP [23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT0_STRM5_PKT_DROP [15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT0_STRM5_PKT_DROP [7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT0_STRM5_PKT_DROP [31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID5, Port0

6.1.117. RX_PSFP_FM_PORT0_STRM4_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT0_STRM4_PKT_DROP
Offset: 0x74C
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID4 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT0_STRM4_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT0_STRM4_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT0_STRM4_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT0_STRM4_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT0_STRM4_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID4, Port0

6.1.118. RX_PSFP_FM_PORT0_STRM3_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT0_STRM3_PKT_DROP
Offset: 0x748
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID3 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT0_STRM3_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT0_STRM3_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT0_STRM3_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT0_STRM3_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT0_STRM3_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID3, Port0

6.1.119. RX_PSFP_FM_PORT0_STRM2_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT0_STRM2_PKT_DROP
Offset: 0x744
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID2 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT0_STRM2_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT0_STRM2_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT0_STRM2_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT0_STRM2_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT0_STRM2_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID2, Port0

6.1.120. RX_PSFP_FM_PORT0_STRM1_PKT_DROP (Ask a Question)

Name: RX_PSFP_FM_PORT0_STRM1_PKT_DROP
Offset: 0x740
Reset: 0x0
Property: Clear on Read

Policing Drop Count Register SID1 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FM_PORT0_STRM1_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FM_PORT0_STRM1_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FM_PORT0_STRM1_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FM_PORT0_STRM1_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FM_PORT0_STRM1_PKT_DROP[31:0] Gives the count of the packets Dropped by the Policing Block for STREAMID1, Port0

6.1.121. RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP
Offset: 0x71C
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID8 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT1_STRM8_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID8, Port1

6.1.122. RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP
Offset: 0x714
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID7 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT1_STRM7_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID7, Port1

6.1.123. RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP
Offset: 0x70C
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID6 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT1_STRM6_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID6, Port1

6.1.124. RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP
Offset: 0x704
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID5 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT1_STRM5_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID5, Port1

6.1.125. RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP
Offset: 0x6FC
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID4 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT1_STRM4_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID4, Port1

6.1.126. RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP
Offset: 0x6F4
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID3 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT1_STRM3_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID3, Port1

6.1.127. RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP
Offset: 0x6EC
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID2 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT1_STRM2_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID2, Port1

6.1.128. RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP
Offset: 0x6E4
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID1 (Port1)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT1_STRM1_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID1, Port1

6.1.129. RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP
Offset: 0x6DC
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID8 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT0_STRM8_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID8, Port0

6.1.130. RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP
Offset: 0x6D4
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID7 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT0_STRM7_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID7, Port0

6.1.131. RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP
Offset: 0x6CC
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID6 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP [31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP [23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP [15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP [7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT0_STRM6_PKT_DROP [31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID6, Port0

6.1.132. RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP
Offset: 0x6C4
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID5 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP [31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP [23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP [15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP [7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT0_STRM5_PKT_DROP [31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID5, Port0

6.1.133. RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP
Offset: 0x6BC
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID4 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP [31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP [23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP [15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP [7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT0_STRM4_PKT_DROP [31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID4, Port0

6.1.134. RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP
Offset: 0x6B4
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID3 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT0_STRM3_PKT_DROP[31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID3, Port0

6.1.135. RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP
Offset: 0x6AC
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID2 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP [31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP [23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP [15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP [7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT0_STRM2_PKT_DROP [31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID2, Port0

6.1.136. RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP (Ask a Question)

Name: RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP
Offset: 0x6A4
Reset: 0x0
Property: Clear on Read

Filtering Drop Count Register SID1 (Port0)

Bit	31	30	29	28	27	26	25	24
	RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP [31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP [23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP [15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP [7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PSFP_FILTER_PORT0_STRM1_PKT_DROP [31:0] Gives the count of the packets Dropped by the Filtering Block for STREAMID1, Port0

6.1.137. RX_PORT1_PRMPT_PKTS_RECEIVED (Ask a Question)

Name: RX_PORT1_PRMPT_PKTS_RECEIVED
Offset: 0x694
Reset: 0x0
Property: Clear on Read

Preempt Packet Receive count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT1_PRMPT_PKTS_RECEIVED[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT1_PRMPT_PKTS_RECEIVED[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT1_PRMPT_PKTS_RECEIVED[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT1_PRMPT_PKTS_RECEIVED[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT1_PRMPT_PKTS_RECEIVED[31:0] Gives the count of valid reassembled Preempted packets Received at PORT1

6.1.138. RX_PORT1_PRMPT_ERROR (Ask a Question)

Name: RX_PORT1_PRMPT_ERROR
Offset: 0x734
Reset: 0x0
Property: Read/Write

RX Port1 Preempt Error Count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT1_PRMPT_ERR_PKTS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT1_PRMPT_ERR_PKTS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT1_PRMPT_ERR_PKTS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT1_PRMPT_ERR_PKTS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT1_PRMPT_ERR_PKTS[31:0] Count of the Preempted Packets Discarded at Receive Port1.Packets are dropped when ingress Frame has ¢ CRC error ¢ Invalid fragment of preemption ¢ Short length packet (less than 64 bytes) ¢ Packets greater than configured Frame Length ¢ Packets received when input FIFO is full ¢

6.1.139. RX_PORT1_EXP_PKTS_RECEIVED (Ask a Question)

Name: RX_PORT1_EXP_PKTS_RECEIVED
Offset: 0x69C
Reset: 0x0
Property: Clear on Read

Express Packet Receive count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT1_EXP_PKTS_RECEIVED [31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT1_EXP_PKTS_RECEIVED [23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT1_EXP_PKTS_RECEIVED [15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT1_EXP_PKTS_RECEIVED [7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT1_EXP_PKTS_RECEIVED [31:0] Gives the count of valid reassembled Express packets Received at PORT1

6.1.140. RX_PORT1_EXP_PKTS_DROP (Ask a Question)

Name: RX_PORT1_EXP_PKTS_DROP
Offset: 0x698
Reset: 0x0
Property: Clear on Read

Replicated Express Packet count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT1_REP_EXP_PKTS_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT1_REP_EXP_PKTS_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT1_REP_EXP_PKTS_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT1_REP_EXP_PKTS_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT1_REP_EXP_PKTS_DROP[31:0] Gives the count of the dropped Express Packets received at PORT1, due to Replication.

6.1.141. RX_PORT1_EXP_ERROR (Ask a Question)

Name: RX_PORT1_EXP_ERROR
Offset: 0x73C
Reset: 0x0
Property: Read/Write

RX Port1 Express Error Count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT1_EXP_ERR_PKTS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT1_EXP_ERR_PKTS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT1_EXP_ERR_PKTS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT1_EXP_ERR_PKTS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT1_EXP_ERR_PKTS[31:0] Count of the Preempted Packets Discarded at Receive Port1.Packets are dropped when ingress Frame has - CRC error Invalid fragment of preemption - Short length packet (less than 64 bytes) - Packets greater than configured Frame Length - Packets received when input FIFO is full.

6.1.142. RX_PORT1_DUP_PRMPT_PKTS_DROP (Ask a Question)

Name: RX_PORT1_DUP_PRMPT_PKTS_DROP
Offset: 0x690
Reset: 0x0
Property: Clear on Read

Replicated Preempt Packet count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT1_REP_PRMPT_PKTS_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT1_REP_PRMPT_PKTS_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT1_REP_PRMPT_PKTS_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT1_REP_PRMPT_PKTS_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT1_REP_PRMPT_PKTS_DROP[31:0] Gives the count of the dropped Preempted Packets received at PORT1, due to Replication.

6.1.143. RX_PORT0_PRMPT_PKTS_RECEIVED (Ask a Question)

Name: RX_PORT0_PRMPT_PKTS_RECEIVED
Offset: 0x684
Reset: 0x0
Property: Clear on Read

Preempt Packet Receive count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT0_PRMPT_PKTS_RECEIVED[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT0_PRMPT_PKTS_RECEIVED[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT0_PRMPT_PKTS_RECEIVED[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT0_PRMPT_PKTS_RECEIVED[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT0_PRMPT_PKTS_RECEIVED[31:0] Gives the count of valid reassembled Preempted packets Received at Port0

6.1.144. RX_PORT0_PRMPT_ERROR (Ask a Question)

Name: RX_PORT0_PRMPT_ERROR
Offset: 0x730
Reset: 0x0
Property: Read/Write

RX Port0 Preempt Error Count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT0_PRMPT_ERR_PKTS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT0_PRMPT_ERR_PKTS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT0_PRMPT_ERR_PKTS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT0_PRMPT_ERR_PKTS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT0_PRMPT_ERR_PKTS[31:0] Count of the Preempted Packets Discarded at Receive Port0.Packets are dropped when ingress Frame has - CRC error ¢ Invalid fragment of preemption - Short length packet (less than 64 bytes) - Packets greater than configured Frame Length - Packets received when input FIFO is full.

6.1.145. RX_PORT0_EXP_PKTS_RECEIVED (Ask a Question)

Name: RX_PORT0_EXP_PKTS_RECEIVED
Offset: 0x68C
Reset: 0x0
Property: Clear on Read

Express Packet Receive count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT0_EXP_PKTS_RECEIVED [31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT0_EXP_PKTS_RECEIVED [23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT0_EXP_PKTS_RECEIVED [15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT0_EXP_PKTS_RECEIVED [7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT0_EXP_PKTS_RECEIVED [31:0] Gives the count of valid reassembled Express packets Received at Port0

6.1.146. RX_PORT0_EXP_PKTS_DROP (Ask a Question)

Name: RX_PORT0_EXP_PKTS_DROP
Offset: 0x688
Reset: 0x0
Property: Clear on Read

Replicated Express Packet count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT0_REP_EXP_PKTS_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT0_REP_EXP_PKTS_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT0_REP_EXP_PKTS_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT0_REP_EXP_PKTS_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT0_REP_EXP_PKTS_DROP[31:0] Gives the count of the dropped Express Packets received at port0, due to Replication.

6.1.147. RX_PORT0_EXP_ERROR (Ask a Question)

Name: RX_PORT0_EXP_ERROR
Offset: 0x738
Reset: 0x0
Property: Read/Write

RX Port0 Express Error Count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT0_EXP_ERR_PKTS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT0_EXP_ERR_PKTS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT0_EXP_ERR_PKTS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT0_EXP_ERR_PKTS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT0_EXP_ERR_PKTS[31:0] Count of the Preempted Packets Discarded at Receive Port0.Packets are dropped when ingress Frame has - CRC error ¢ Invalid fragment of preemption - Short length packet (less than 64 bytes) - Packets greater than configured Frame Length - Packets received when input FIFO is full.

6.1.148. RX_PORT0_DUP_PRMPT_PKTS_DROP (Ask a Question)

Name: RX_PORT0_DUP_PRMPT_PKTS_DROP
Offset: 0x680
Reset: 0x0
Property: Clear on Read

Preempt Packet drop count Register

Bit	31	30	29	28	27	26	25	24
	RX_PORT0_REP_PRMPT_PKTS_DROP[31:24]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_PORT0_REP_PRMPT_PKTS_DROP[23:16]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_PORT0_REP_PRMPT_PKTS_DROP[15:8]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_PORT0_REP_PRMPT_PKTS_DROP[7:0]							
Access	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_PORT0_REP_PRMPT_PKTS_DROP[31:0] Gives the count of the dropped Preempted Packets received at port0, due to Replication

6.1.149. PSFP_SID8_P1_MAX (Ask a Question)

Name: PSFP_SID8_P1_MAX
Offset: 0x4EC
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID8 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P1_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P1_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID8_P1_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID8 on RX Port1

6.1.150. PSFP_SID8_P1_FM_CTRL (Ask a Question)

Name: PSFP_SID8_P1_FM_CTRL
Offset: 0x4FC
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID8 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID8_P1_CFG_UPD	PSFP_SID8_P1_DRP_MAX_EXCD	PSFP_SID8_P1_DRP_YELLOW	PSFP_SID8_P1_FM_EN	PSFP_SID8_P1_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID8_P1_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID8_P1_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID8
[0]	If Disabled only frames greater than Max packet size are dropped, SID8

Bit 2 – PSFP_SID8_P1_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID8 are dropped
[0]	If Disabled Yellow frames are passed of SID8

Bit 1 – PSFP_SID8_P1_FM_EN

Value	Description
[1]	Policing Enabled for SID8 , RX Port1
[0]	Policing Disabled for SID8 , RX Port1

Bit 0 – PSFP_SID8_P1_FIL_EN

Value	Description
[1]	Filtering Enabled for SID8 , RX Port1
[0]	Filtering Disabled for SID8 , RX Port1

6.1.151. PSFP_SID8_P1_FM_3 (Ask a Question)

Name: PSFP_SID8_P1_FM_3
Offset: 0x53C
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID8 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID8_P1_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P1_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P1_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P1_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID8_P1_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID8 RX Port1

Bits 15:0 – PSFP_SID8_P1_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID8 RX Port1

6.1.152. PSFP_SID8_P1_FM_2 (Ask a Question)

Name: PSFP_SID8_P1_FM_2
Offset: 0x4F8
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID8 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID8_P1_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P1_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P1_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P1_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID8_P1_EIR[31:0] Excess Information Rate allowed for STREAMID8, RX Port1, given in bits per second

6.1.153. PSFP_SID8_P1_FM_1 (Ask a Question)

Name: PSFP_SID8_P1_FM_1
Offset: 0x4F4
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID8 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID8_P1_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P1_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P1_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P1_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID8_P1_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID8, RX Port1, given in bits per second

6.1.154. PSFP_SID8_P1_FM (Ask a Question)

Name: PSFP_SID8_P1_FM
Offset: 0x4F0
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID8 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID8_P1_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P1_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P1_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P1_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID8_P1_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID8 RX Port1

Bits 15:0 – PSFP_SID8_P1_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID8, RX Port1,given in Bytes

6.1.155. PSFP_SID8_P1_CTRL (Ask a Question)

Name: PSFP_SID8_P1_CTRL
Offset: 0x4E8
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID8_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID8_P1_VID_EN	PSFP_SID8_P1_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID8_P1_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID8 , RX Port1
[0]	VLAN ID check Disabled for SID8 , RX Port1

Bit 0 – PSFP_SID8_P1_SA_EN

Value	Description
[1]	Source address check Enabled for SID8 , RX Port1
[0]	Source address check Disabled for SID8 , RX Port1

6.1.156. PSFP_SID8_P1_1 (Ask a Question)

Name: PSFP_SID8_P1_1
Offset: 0x4E4
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID8_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID8_P1_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P1_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P1_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P1_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID8_P1_VID[11:0] VLAN Identifier of STREAMID8 for Filtering on Rx port1

Bits 15:0 – PSFP_SID8_P1_SA_MSB[15:0] Source address bits[48:32] of STREAMID8 for Filtering on Rx port1

6.1.157. PSFP_SID8_P1_0 (Ask a Question)

Name: PSFP_SID8_P1_0
Offset: 0x4E0
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID8_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID8_P1_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P1_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P1_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P1_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID8_P1_SA_LSB[31:0] Source address bits[31:0] of STREAMID8 for Filtering on Rx port1

6.1.158. PSFP_SID8_P0_MAX (Ask a Question)

Name: PSFP_SID8_P0_MAX
Offset: 0x3EC
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID8 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P0_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P0_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID8_P0_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID8 on RX Port0

6.1.159. PSFP_SID8_P0_FM_CTRL (Ask a Question)

Name: PSFP_SID8_P0_FM_CTRL
Offset: 0x3FC
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID8 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID8_P0_CFG_UPD	PSFP_SID8_P0_DRP_MAX_EXCD	PSFP_SID8_P0_DRP_YELLOW	PSFP_SID8_P0_FM_EN	PSFP_SID8_P0_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID8_P0_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID8_P0_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID8
[0]	If Disabled only frames greater than Max packet size are dropped, SID8

Bit 2 – PSFP_SID8_P0_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID8 are dropped
[0]	If Disabled Yellow frames are passed of SID8

Bit 1 – PSFP_SID8_P0_FM_EN

Value	Description
[1]	Policing Enabled for SID8 , RX Port0
[0]	Policing Disabled for SID8 , RX Port0

Bit 0 – PSFP_SID8_P0_FIL_EN

Value	Description
[1]	Filtering Enabled for SID8 , RX Port0
[0]	Filtering Disabled for SID8 , RX Port0

6.1.160. PSFP_SID8_P0_FM_3 (Ask a Question)

Name: PSFP_SID8_P0_FM_3
Offset: 0x51C
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID8 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID8_P0_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P0_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P0_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P0_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID8_P0_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID8 RX Port0

Bits 15:0 – PSFP_SID8_P0_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID8 RX Port0

6.1.161. PSFP_SID8_P0_FM_2 (Ask a Question)

Name: PSFP_SID8_P0_FM_2
Offset: 0x3F8
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID8 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID8_P0_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P0_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P0_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P0_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID8_P0_EIR[31:0] Excess Information Rate allowed for STREAMID8, RX Port0, given in bits per second

6.1.162. PSFP_SID8_P0_FM_1 (Ask a Question)

Name: PSFP_SID8_P0_FM_1
Offset: 0x3F4
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID8 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID8_P0_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P0_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P0_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P0_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID8_P0_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID8, RX Port0, given in bits per second

6.1.163. PSFP_SID8_P0_FM (Ask a Question)

Name: PSFP_SID8_P0_FM
Offset: 0x3F0
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID8 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID8_P0_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P0_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P0_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P0_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID8_P0_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID8 RX Port0

Bits 15:0 – PSFP_SID8_P0_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID8, RX Port0,given in Bytes

6.1.164. PSFP_SID8_P0_CTRL (Ask a Question)

Name: PSFP_SID8_P0_CTRL
Offset: 0x3E8
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID8_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID8_P0_VID_EN	PSFP_SID8_P0_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID8_P0_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID8 , RX Port0
[0]	VLAN ID check Disabled for SID8 , RX Port0

Bit 0 – PSFP_SID8_P0_SA_EN

Value	Description
[1]	Source address check Enabled for SID8 , RX Port0
[0]	Source address check Disabled for SID8 , RX Port0

6.1.165. PSFP_SID8_P0_1 (Ask a Question)

Name: PSFP_SID8_P0_1
Offset: 0x3E4
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID8_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID8_P0_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P0_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P0_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P0_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID8_P0_VID[11:0] VLAN Identifier of STREAMID8 for Filtering on Rx port0

Bits 15:0 – PSFP_SID8_P0_SA_MSB[15:0] Source address bits[48:32] of STREAMID8 for Filtering on Rx port0

6.1.166. PSFP_SID8_P0_0 (Ask a Question)

Name: PSFP_SID8_P0_0
Offset: 0x3E0
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID8_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID8_P0_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID8_P0_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID8_P0_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID8_P0_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID8_P0_SA_LSB[31:0] Source address bits[31:0] of STREAMID8 for Filtering on Rx port0

6.1.167. PSFP_SID7_P1_MAX (Ask a Question)

Name: PSFP_SID7_P1_MAX
Offset: 0x4CC
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID7 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P1_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P1_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID7_P1_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID7 on RX Port1

6.1.168. PSFP_SID7_P1_FM_CTRL (Ask a Question)

Name: PSFP_SID7_P1_FM_CTRL
Offset: 0x4DC
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID7 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID7_P1_CFG_UPD	PSFP_SID7_P1_DRP_MAX_EXCD	PSFP_SID7_P1_DRP_YELLOW	PSFP_SID7_P1_FM_EN	PSFP_SID7_P1_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID7_P1_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID7_P1_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID7
[0]	If Disabled only frames greater than Max packet size are dropped, SID7

Bit 2 – PSFP_SID7_P1_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID7 are dropped
[0]	If Disabled Yellow frames are passed of SID7

Bit 1 – PSFP_SID7_P1_FM_EN

Value	Description
[1]	Policing Enabled for SID7 , RX Port1
[0]	Policing Disabled for SID7 , RX Port1

Bit 0 – PSFP_SID7_P1_FIL_EN

Value	Description
[1]	Filtering Enabled for SID7 , RX Port1
[0]	Filtering Disabled for SID7 , RX Port1

6.1.169. PSFP_SID7_P1_FM_3 (Ask a Question)

Name: PSFP_SID7_P1_FM_3
Offset: 0x538
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID7 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID7_P1_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P1_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P1_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P1_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID7_P1_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID7 RX Port1

Bits 15:0 – PSFP_SID7_P1_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID7 RX Port1

6.1.170. PSFP_SID7_P1_FM_2 (Ask a Question)

Name: PSFP_SID7_P1_FM_2
Offset: 0x4D8
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID7 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID7_P1_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P1_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P1_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P1_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID7_P1_EIR[31:0] Excess Information Rate allowed for STREAMID7, RX Port1, given in bits per second

6.1.171. PSFP_SID7_P1_FM_1 (Ask a Question)

Name: PSFP_SID7_P1_FM_1
Offset: 0x4D4
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID7 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID7_P1_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P1_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P1_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P1_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID7_P1_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID7, RX Port1, given in bits per second

6.1.172. PSFP_SID7_P1_FM (Ask a Question)

Name: PSFP_SID7_P1_FM
Offset: 0x4D0
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID7 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID7_P1_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P1_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P1_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P1_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID7_P1_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID7 RX Port1

Bits 15:0 – PSFP_SID7_P1_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID7, RX Port1,given in Bytes

6.1.173. PSFP_SID7_P1_CTRL (Ask a Question)

Name: PSFP_SID7_P1_CTRL
Offset: 0x4C8
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID7_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID7_P1_VID_EN	PSFP_SID7_P1_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID7_P1_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID7 , RX Port1
[0]	VLAN ID check Disabled for SID7 , RX Port1

Bit 0 – PSFP_SID7_P1_SA_EN

Value	Description
[1]	Source address check Enabled for SID7 , RX Port1
[0]	Source address check Disabled for SID7 , RX Port1

6.1.174. PSFP_SID7_P1_1 (Ask a Question)

Name: PSFP_SID7_P1_1
Offset: 0x4C4
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID7_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID7_P1_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P1_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P1_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P1_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID7_P1_VID[11:0] VLAN Identifier of STREAMID7 for Filtering on Rx port1

Bits 15:0 – PSFP_SID7_P1_SA_MSB[15:0] Source address bits[48:32] of STREAMID7 for Filtering on Rx port1

6.1.175. PSFP_SID7_P1_0 (Ask a Question)

Name: PSFP_SID7_P1_0
Offset: 0x4C0
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID7_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID7_P1_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P1_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P1_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P1_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID7_P1_SA_LSB[31:0] Source address bits[31:0] of STREAMID7 for Filtering on Rx port1

6.1.176. PSFP_SID7_P0_MAX (Ask a Question)

Name: PSFP_SID7_P0_MAX
Offset: 0x3CC
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID7 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P0_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P0_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID7_P0_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID7 on RX Port0

6.1.177. PSFP_SID7_P0_FM_CTRL (Ask a Question)

Name: PSFP_SID7_P0_FM_CTRL
Offset: 0x3DC
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID7 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID7_P0_CFG_UPD	PSFP_SID7_P0_DRP_MAX_EXCD	PSFP_SID7_P0_DRP_YELLOW	PSFP_SID7_P0_FM_EN	PSFP_SID7_P0_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID7_P0_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID7_P0_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID7
[0]	If Disabled only frames greater than Max packet size are dropped, SID7

Bit 2 – PSFP_SID7_P0_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID7 are dropped
[0]	If Disabled Yellow frames are passed of SID7

Bit 1 – PSFP_SID7_P0_FM_EN

Value	Description
[1]	Policing Enabled for SID7 , RX Port0
[0]	Policing Disabled for SID7 , RX Port0

Bit 0 – PSFP_SID7_P0_FIL_EN

Value	Description
[1]	Filtering Enabled for SID7 , RX Port0
[0]	Filtering Disabled for SID7 , RX Port0

6.1.178. PSFP_SID7_P0_FM_3 (Ask a Question)

Name: PSFP_SID7_P0_FM_3
Offset: 0x518
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID7 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID7_P0_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P0_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P0_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P0_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID7_P0_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID7 RX Port0

Bits 15:0 – PSFP_SID7_P0_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID7 RX Port0

6.1.179. PSFP_SID7_P0_FM_2 (Ask a Question)

Name: PSFP_SID7_P0_FM_2
Offset: 0x3D8
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID7 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID7_P0_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P0_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P0_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P0_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID7_P0_EIR[31:0] Excess Information Rate allowed for STREAMID7, RX Port0, given in bits per second

6.1.180. PSFP_SID7_P0_FM_1 (Ask a Question)

Name: PSFP_SID7_P0_FM_1
Offset: 0x3D4
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID7 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID7_P0_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P0_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P0_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P0_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID7_P0_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID7, RX Port0, given in bits per second

6.1.181. PSFP_SID7_P0_FM (Ask a Question)

Name: PSFP_SID7_P0_FM
Offset: 0x3D0
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID7 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID7_P0_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P0_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P0_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P0_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID7_P0_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID7 RX Port0

Bits 15:0 – PSFP_SID7_P0_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID7, RX Port0,given in Bytes

6.1.182. PSFP_SID7_P0_CTRL (Ask a Question)

Name: PSFP_SID7_P0_CTRL
Offset: 0x3C8
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID7_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID7_P0_VID_EN	PSFP_SID7_P0_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID7_P0_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID7 , RX Port0
[0]	VLAN ID check Disabled for SID7 , RX Port0

Bit 0 – PSFP_SID7_P0_SA_EN

Value	Description
[1]	Source address check Enabled for SID7 , RX Port0
[0]	Source address check Disabled for SID7 , RX Port0

6.1.183. PSFP_SID7_P0_1 (Ask a Question)

Name: PSFP_SID7_P0_1
Offset: 0x3C4
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID7_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID7_P0_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P0_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P0_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P0_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID7_P0_VID[11:0] VLAN Identifier of STREAMID7 for Filtering on Rx port0

Bits 15:0 – PSFP_SID7_P0_SA_MSB[15:0] Source address bits[48:32] of STREAMID7 for Filtering on Rx port0

6.1.184. PSFP_SID7_P0_0 (Ask a Question)

Name: PSFP_SID7_P0_0
Offset: 0x3C0
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID7_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID7_P0_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID7_P0_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID7_P0_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID7_P0_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID7_P0_SA_LSB[31:0] Source address bits[31:0] of STREAMID7 for Filtering on Rx port0

6.1.185. PSFP_SID6_P1_MAX (Ask a Question)

Name: PSFP_SID6_P1_MAX
Offset: 0x4AC
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID6 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P1_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P1_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID6_P1_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID6 on RX Port1

6.1.186. PSFP_SID6_P1_FM_CTRL (Ask a Question)

Name: PSFP_SID6_P1_FM_CTRL
Offset: 0x4BC
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID6 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID6_P1_CFG_UPD	PSFP_SID6_P1_DRP_MAX_EXCD	PSFP_SID6_P1_DRP_YELLOW	PSFP_SID6_P1_FM_EN	PSFP_SID6_P1_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID6_P1_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID6_P1_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID6
[0]	If Disabled only frames greater than Max packet size are dropped, SID6

Bit 2 – PSFP_SID6_P1_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID6 are dropped
[0]	If Disabled Yellow frames are passed of SID6

Bit 1 – PSFP_SID6_P1_FM_EN

Value	Description
[1]	Policing Enabled for SID6 , RX Port1
[0]	Policing Disabled for SID6 , RX Port1

Bit 0 – PSFP_SID6_P1_FIL_EN

Value	Description
[1]	Filtering Enabled for SID6 , RX Port1
[0]	Filtering Disabled for SID6 , RX Port1

6.1.187. PSFP_SID6_P1_FM_3 (Ask a Question)

Name: PSFP_SID6_P1_FM_3
Offset: 0x534
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID6 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID6_P1_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P1_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P1_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P1_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID6_P1_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID6 RX Port1

Bits 15:0 – PSFP_SID6_P1_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID6 RX Port1

6.1.188. PSFP_SID6_P1_FM_2 (Ask a Question)

Name: PSFP_SID6_P1_FM_2
Offset: 0x4B8
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID6 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID6_P1_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P1_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P1_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P1_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID6_P1_EIR[31:0] Excess Information Rate allowed for STREAMID6, RX Port1, given in bits per second

6.1.189. PSFP_SID6_P1_FM_1 (Ask a Question)

Name: PSFP_SID6_P1_FM_1
Offset: 0x4B4
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID6 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID6_P1_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P1_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P1_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P1_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID6_P1_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID6, RX Port1, given in bits per second

6.1.190. PSFP_SID6_P1_FM (Ask a Question)

Name: PSFP_SID6_P1_FM
Offset: 0x4B0
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID6 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID6_P1_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P1_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P1_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P1_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID6_P1_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID6 RX Port1

Bits 15:0 – PSFP_SID6_P1_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID6, RX Port1,given in Bytes

6.1.191. PSFP_SID6_P1_CTRL (Ask a Question)

Name: PSFP_SID6_P1_CTRL
Offset: 0x4A8
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID6_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID6_P1_VID_EN	PSFP_SID6_P1_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID6_P1_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID6 , RX Port1
[0]	VLAN ID check Disabled for SID6 , RX Port1

Bit 0 – PSFP_SID6_P1_SA_EN

Value	Description
[1]	Source address check Enabled for SID6 , RX Port1
[0]	Source address check Disabled for SID6 , RX Port1

6.1.192. PSFP_SID6_P1_1 (Ask a Question)

Name: PSFP_SID6_P1_1
Offset: 0x4A4
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID6_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID6_P1_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P1_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P1_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P1_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID6_P1_VID[11:0] VLAN Identifier of STREAMID6 for Filtering on Rx port1

Bits 15:0 – PSFP_SID6_P1_SA_MSB[15:0] Source address bits[48:32] of STREAMID6 for Filtering on Rx port1

6.1.193. PSFP_SID6_P1_0 (Ask a Question)

Name: PSFP_SID6_P1_0
Offset: 0x4A0
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID6_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID6_P1_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P1_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P1_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P1_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID6_P1_SA_LSB[31:0] Source address bits[31:0] of STREAMID6 for Filtering on Rx port1

6.1.194. PSFP_SID6_P0_MAX (Ask a Question)

Name: PSFP_SID6_P0_MAX
Offset: 0x3AC
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID6 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P0_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P0_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID6_P0_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID6 on RX Port0

6.1.195. PSFP_SID6_P0_FM_CTRL (Ask a Question)

Name: PSFP_SID6_P0_FM_CTRL
Offset: 0x3BC
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID6 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID6_P0_CFG_UPD	PSFP_SID6_P0_DRP_MAX_EXCD	PSFP_SID6_P0_DRP_YELLOW	PSFP_SID6_P0_FM_EN	PSFP_SID6_P0_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID6_P0_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID6_P0_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID6
[0]	If Disabled only frames greater than Max packet size are dropped, SID6

Bit 2 – PSFP_SID6_P0_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID6 are dropped
[0]	If Disabled Yellow frames are passed of SID6

Bit 1 – PSFP_SID6_P0_FM_EN

Value	Description
[1]	Policing Enabled for SID6 , RX Port0
[0]	Policing Disabled for SID6 , RX Port0

Bit 0 – PSFP_SID6_P0_FIL_EN

Value	Description
[1]	Filtering Enabled for SID6 , RX Port0
[0]	Filtering Disabled for SID6 , RX Port0

6.1.196. PSFP_SID6_P0_FM_3 (Ask a Question)

Name: PSFP_SID6_P0_FM_3
Offset: 0x514
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID6 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID6_P0_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P0_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P0_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P0_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID6_P0_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID6 RX Port0

Bits 15:0 – PSFP_SID6_P0_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID6 RX Port0

6.1.197. PSFP_SID6_P0_FM_2 (Ask a Question)

Name: PSFP_SID6_P0_FM_2
Offset: 0x3B8
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID6 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID6_P0_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P0_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P0_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P0_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID6_P0_EIR[31:0] Excess Information Rate allowed for STREAMID6, RX Port0, given in bits per second

6.1.198. PSFP_SID6_P0_FM_1 (Ask a Question)

Name: PSFP_SID6_P0_FM_1
Offset: 0x3B4
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID6 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID6_P0_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P0_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P0_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P0_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID6_P0_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID6, RX Port0, given in bits per second

6.1.199. PSFP_SID6_P0_FM (Ask a Question)

Name: PSFP_SID6_P0_FM
Offset: 0x3B0
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID6 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID6_P0_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P0_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P0_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P0_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID6_P0_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID6 RX Port0

Bits 15:0 – PSFP_SID6_P0_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID6, RX Port0,given in Bytes

6.1.200. PSFP_SID6_P0_CTRL (Ask a Question)

Name: PSFP_SID6_P0_CTRL
Offset: 0x3A8
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID6_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID6_P0_VID_EN	PSFP_SID6_P0_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID6_P0_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID6 , RX Port0
[0]	VLAN ID check Disabled for SID6 , RX Port0

Bit 0 – PSFP_SID6_P0_SA_EN

Value	Description
[1]	Source address check Enabled for SID6 , RX Port0
[0]	Source address check Disabled for SID6 , RX Port0

6.1.201. PSFP_SID6_P0_1 (Ask a Question)

Name: PSFP_SID6_P0_1
Offset: 0x3A4
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID6_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID6_P0_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P0_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P0_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P0_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID6_P0_VID[11:0] VLAN Identifier of STREAMID6 for Filtering on Rx port0

Bits 15:0 – PSFP_SID6_P0_SA_MSB[15:0] Source address bits[48:32] of STREAMID6 for Filtering on Rx port0

6.1.202. PSFP_SID6_P0_0 (Ask a Question)

Name: PSFP_SID6_P0_0
Offset: 0x3A0
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID6_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID6_P0_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID6_P0_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID6_P0_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID6_P0_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID6_P0_SA_LSB[31:0] Source address bits[31:0] of STREAMID6 for Filtering on Rx port0

6.1.203. PSFP_SID5_P1_MAX (Ask a Question)

Name: PSFP_SID5_P1_MAX
Offset: 0x48C
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID5 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P1_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P1_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID5_P1_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID5 on RX Port1

6.1.204. PSFP_SID5_P1_FM_CTRL (Ask a Question)

Name: PSFP_SID5_P1_FM_CTRL
Offset: 0x49C
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID5 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID5_P1_CFG_UPD	PSFP_SID5_P1_DRP_MAX_EXCD	PSFP_SID5_P1_DRP_YELLOW	PSFP_SID5_P1_FM_EN	PSFP_SID5_P1_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID5_P1_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID5_P1_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID5
[0]	If Disabled only frames greater than Max packet size are dropped, SID5

Bit 2 – PSFP_SID5_P1_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID5 are dropped
[0]	If Disabled Yellow frames are passed of SID5

Bit 1 – PSFP_SID5_P1_FM_EN

Value	Description
[1]	Policing Enabled for SID5 , RX Port1
[0]	Policing Disabled for SID5 , RX Port1

Bit 0 – PSFP_SID5_P1_FIL_EN

Value	Description
[1]	Filtering Enabled for SID5 , RX Port1
[0]	Filtering Disabled for SID5 , RX Port1

6.1.205. PSFP_SID5_P1_FM_3 (Ask a Question)

Name: PSFP_SID5_P1_FM_3
Offset: 0x530
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID5 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID5_P1_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P1_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P1_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P1_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID5_P1_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID5 RX Port1

Bits 15:0 – PSFP_SID5_P1_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID5 RX Port1

6.1.206. PSFP_SID5_P1_FM_2 (Ask a Question)

Name: PSFP_SID5_P1_FM_2
Offset: 0x498
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID5 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID5_P1_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P1_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P1_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P1_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID5_P1_EIR[31:0] Excess Information Rate allowed for STREAMID5, RX Port1, given in bits per second

6.1.207. PSFP_SID5_P1_FM_1 (Ask a Question)

Name: PSFP_SID5_P1_FM_1
Offset: 0x494
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID5 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID5_P1_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P1_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P1_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P1_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID5_P1_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID5, RX Port1, given in bits per second

6.1.208. PSFP_SID5_P1_FM (Ask a Question)

Name: PSFP_SID5_P1_FM
Offset: 0x490
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID5 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID5_P1_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P1_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P1_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P1_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID5_P1_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID5 RX Port1

Bits 15:0 – PSFP_SID5_P1_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID5, RX Port1,given in Bytes

6.1.209. PSFP_SID5_P1_CTRL (Ask a Question)

Name: PSFP_SID5_P1_CTRL
Offset: 0x488
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID5_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID5_P1_VID_EN	PSFP_SID5_P1_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID5_P1_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID5 , RX Port1
[0]	VLAN ID check Disabled for SID5 , RX Port1

Bit 0 – PSFP_SID5_P1_SA_EN

Value	Description
[1]	Source address check Enabled for SID5 , RX Port1
[0]	Source address check Disabled for SID5 , RX Port1

6.1.210. PSFP_SID5_P1_1 (Ask a Question)

Name: PSFP_SID5_P1_1
Offset: 0x484
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID5_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID5_P1_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P1_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P1_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P1_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID5_P1_VID[11:0] VLAN Identifier of STREAMID5 for Filtering on Rx port1

Bits 15:0 – PSFP_SID5_P1_SA_MSB[15:0] Source address bits[48:32] of STREAMID5 for Filtering on Rx port1

6.1.211. PSFP_SID5_P1_0 (Ask a Question)

Name: PSFP_SID5_P1_0
Offset: 0x480
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID5_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID5_P1_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P1_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P1_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P1_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID5_P1_SA_LSB[31:0] Source address bits[31:0] of STREAMID5 for Filtering on Rx port1

6.1.212. PSFP_SID5_P0_MAX (Ask a Question)

Name: PSFP_SID5_P0_MAX
Offset: 0x38C
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID5 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P0_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P0_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID5_P0_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID5 on RX Port0

6.1.213. PSFP_SID5_P0_FM_CTRL (Ask a Question)

Name: PSFP_SID5_P0_FM_CTRL
Offset: 0x39C
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID5 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID5_P0_CFG_UPD	PSFP_SID5_P0_DRP_MAX_EXCD	PSFP_SID5_P0_DRP_YELLOW	PSFP_SID5_P0_FM_EN	PSFP_SID5_P0_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID5_P0_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID5_P0_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID5
[0]	If Disabled only frames greater than Max packet size are dropped, SID5

Bit 2 – PSFP_SID5_P0_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID5 are dropped
[0]	If Disabled Yellow frames are passed of SID5

Bit 1 – PSFP_SID5_P0_FM_EN

Value	Description
[1]	Policing Enabled for SID5 , RX Port0
[0]	Policing Disabled for SID5 , RX Port0

Bit 0 – PSFP_SID5_P0_FIL_EN

Value	Description
[1]	Filtering Enabled for SID5 , RX Port0
[0]	Filtering Disabled for SID5 , RX Port0

6.1.214. PSFP_SID5_P0_FM_3 (Ask a Question)

Name: PSFP_SID5_P0_FM_3
Offset: 0x510
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID5 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID5_P0_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P0_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P0_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P0_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID5_P0_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID5 RX Port0

Bits 15:0 – PSFP_SID5_P0_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID5 RX Port0

6.1.215. PSFP_SID5_P0_FM_2 (Ask a Question)

Name: PSFP_SID5_P0_FM_2
Offset: 0x398
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID5 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID5_P0_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P0_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P0_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P0_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID5_P0_EIR[31:0] Excess Information Rate allowed for STREAMID5, RX Port0, given in bits per second

6.1.216. PSFP_SID5_P0_FM_1 (Ask a Question)

Name: PSFP_SID5_P0_FM_1
Offset: 0x394
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID5 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID5_P0_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P0_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P0_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P0_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID5_P0_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID5, RX Port0, given in bits per second

6.1.217. PSFP_SID5_P0_FM (Ask a Question)

Name: PSFP_SID5_P0_FM
Offset: 0x390
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID5 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID5_P0_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P0_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P0_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P0_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID5_P0_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID5 RX Port0

Bits 15:0 – PSFP_SID5_P0_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID5, RX Port0,given in Bytes

6.1.218. PSFP_SID5_P0_CTRL (Ask a Question)

Name: PSFP_SID5_P0_CTRL
Offset: 0x388
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID5_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID5_P0_VID_EN	PSFP_SID5_P0_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID5_P0_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID5 , RX Port0
[0]	VLAN ID check Disabled for SID5 , RX Port0

Bit 0 – PSFP_SID5_P0_SA_EN

Value	Description
[1]	Source address check Enabled for SID5 , RX Port0
[0]	Source address check Disabled for SID5 , RX Port0

6.1.219. PSFP_SID5_P0_1 (Ask a Question)

Name: PSFP_SID5_P0_1
Offset: 0x384
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID5_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID5_P0_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P0_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P0_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P0_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID5_P0_VID[11:0] VLAN Identifier of STREAMID5 for Filtering on Rx port0

Bits 15:0 – PSFP_SID5_P0_SA_MSB[15:0] Source address bits[48:32] of STREAMID5 for Filtering on Rx port0

6.1.220. PSFP_SID5_P0_0 (Ask a Question)

Name: PSFP_SID5_P0_0
Offset: 0x380
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID5_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID5_P0_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID5_P0_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID5_P0_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID5_P0_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID5_P0_SA_LSB[31:0] Source address bits[31:0] of STREAMID5 for Filtering on Rx port0

6.1.221. PSFP_SID4_P1_MAX (Ask a Question)

Name: PSFP_SID4_P1_MAX
Offset: 0x46C
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID4 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P1_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P1_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID4_P1_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID4 on RX Port1

6.1.222. PSFP_SID4_P1_FM_CTRL (Ask a Question)

Name: PSFP_SID4_P1_FM_CTRL
Offset: 0x47C
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID4 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID4_P1_CFG_UPD	PSFP_SID4_P1_DRP_MAX_EXCD	PSFP_SID4_P1_DRP_YELLOW	PSFP_SID4_P1_FM_EN	PSFP_SID4_P1_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID4_P1_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID4_P1_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID4
[0]	If Disabled only frames greater than Max packet size are dropped, SID4

Bit 2 – PSFP_SID4_P1_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID4 are dropped
[0]	If Disabled Yellow frames are passed of SID4

Bit 1 – PSFP_SID4_P1_FM_EN

Value	Description
[1]	Policing Enabled for SID4 , RX Port1
[0]	Policing Disabled for SID4 , RX Port1

Bit 0 – PSFP_SID4_P1_FIL_EN

Value	Description
[1]	Filtering Enabled for SID4 , RX Port1
[0]	Filtering Disabled for SID4 , RX Port1

6.1.223. PSFP_SID4_P1_FM_3 (Ask a Question)

Name: PSFP_SID4_P1_FM_3
Offset: 0x52C
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID4 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID4_P1_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P1_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P1_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P1_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID4_P1_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID4 RX Port1

Bits 15:0 – PSFP_SID4_P1_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID4 RX Port1

6.1.224. PSFP_SID4_P1_FM_2 (Ask a Question)

Name: PSFP_SID4_P1_FM_2
Offset: 0x478
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID4 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID4_P1_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P1_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P1_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P1_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID4_P1_EIR[31:0] Excess Information Rate allowed for STREAMID4, RX Port1, given in bits per second

6.1.225. PSFP_SID4_P1_FM_1 (Ask a Question)

Name: PSFP_SID4_P1_FM_1
Offset: 0x474
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID4 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID4_P1_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P1_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P1_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P1_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID4_P1_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID4, RX Port1, given in bits per second

6.1.226. PSFP_SID4_P1_FM (Ask a Question)

Name: PSFP_SID4_P1_FM
Offset: 0x470
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID4 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID4_P1_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P1_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P1_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P1_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID4_P1_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID4 RX Port1

Bits 15:0 – PSFP_SID4_P1_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID4, RX Port1,given in Bytes

6.1.227. PSFP_SID4_P1_CTRL (Ask a Question)

Name: PSFP_SID4_P1_CTRL
Offset: 0x468
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID4_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID4_P1_VID_EN	PSFP_SID4_P1_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID4_P1_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID4 , RX Port1
[0]	VLAN ID check Disabled for SID4 , RX Port1

Bit 0 – PSFP_SID4_P1_SA_EN

Value	Description
[1]	Source address check Enabled for SID4 , RX Port1
[0]	Source address check Disabled for SID4 , RX Port1

6.1.228. PSFP_SID4_P1_1 (Ask a Question)

Name: PSFP_SID4_P1_1
Offset: 0x464
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID4_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID4_P1_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P1_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P1_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P1_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID4_P1_VID[11:0] VLAN Identifier of STREAMID4 for Filtering on Rx port1

Bits 15:0 – PSFP_SID4_P1_SA_MSB[15:0] Source address bits[48:32] of STREAMID4 for Filtering on Rx port1

6.1.229. PSFP_SID4_P1_0 (Ask a Question)

Name: PSFP_SID4_P1_0
Offset: 0x460
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID4_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID4_P1_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P1_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P1_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P1_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID4_P1_SA_LSB[31:0] Source address bits[31:0] of STREAMID4 for Filtering on Rx port1

6.1.230. PSFP_SID4_P0_MAX (Ask a Question)

Name: PSFP_SID4_P0_MAX
Offset: 0x36C
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID4 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P0_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P0_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID4_P0_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID4 on RX Port0

6.1.231. PSFP_SID4_P0_FM_CTRL (Ask a Question)

Name: PSFP_SID4_P0_FM_CTRL
Offset: 0x37C
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID4 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID4_P0_CFG_UPD	PSFP_SID4_P0_DRP_MAX_EXCD	PSFP_SID4_P0_DRP_YELLOW	PSFP_SID4_P0_FM_EN	PSFP_SID4_P0_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID4_P0_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID4_P0_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID4
[0]	If Disabled only frames greater than Max packet size are dropped, SID4

Bit 2 – PSFP_SID4_P0_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID4 are dropped
[0]	If Disabled Yellow frames are passed of SID4

Bit 1 – PSFP_SID4_P0_FM_EN

Value	Description
[1]	Policing Enabled for SID4 , RX Port0
[0]	Policing Disabled for SID4 , RX Port0

Bit 0 – PSFP_SID4_P0_FIL_EN

Value	Description
[1]	Filtering Enabled for SID4 , RX Port0
[0]	Filtering Disabled for SID4 , RX Port0

6.1.232. PSFP_SID4_P0_FM_3 (Ask a Question)

Name: PSFP_SID4_P0_FM_3
Offset: 0x50C
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID4 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID4_P0_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P0_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P0_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P0_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID4_P0_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID4 RX Port0

Bits 15:0 – PSFP_SID4_P0_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID4 RX Port0

6.1.233. PSFP_SID4_P0_FM_2 (Ask a Question)

Name: PSFP_SID4_P0_FM_2
Offset: 0x378
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID4 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID4_P0_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P0_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P0_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P0_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID4_P0_EIR[31:0] Excess Information Rate allowed for STREAMID4, RX Port0, given in bits per second

6.1.234. PSFP_SID4_P0_FM_1 (Ask a Question)

Name: PSFP_SID4_P0_FM_1
Offset: 0x374
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID4 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID4_P0_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P0_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P0_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P0_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID4_P0_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID4, RX Port0, given in bits per second

6.1.235. PSFP_SID4_P0_FM (Ask a Question)

Name: PSFP_SID4_P0_FM
Offset: 0x370
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID4 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID4_P0_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P0_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P0_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P0_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID4_P0_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID4 RX Port0

Bits 15:0 – PSFP_SID4_P0_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID4, RX Port0,given in Bytes

6.1.236. PSFP_SID4_P0_CTRL (Ask a Question)

Name: PSFP_SID4_P0_CTRL
Offset: 0x368
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID4_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID4_P0_VID_EN	PSFP_SID4_P0_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID4_P0_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID4 , RX Port0
[0]	VLAN ID check Disabled for SID4 , RX Port0

Bit 0 – PSFP_SID4_P0_SA_EN

Value	Description
[1]	Source address check Enabled for SID4 , RX Port0
[0]	Source address check Disabled for SID4 , RX Port0

6.1.237. PSFP_SID4_P0_1 (Ask a Question)

Name: PSFP_SID4_P0_1
Offset: 0x364
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID4_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID4_P0_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P0_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P0_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P0_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID4_P0_VID[11:0] VLAN Identifier of STREAMID4 for Filtering on Rx port0

Bits 15:0 – PSFP_SID4_P0_SA_MSB[15:0] Source address bits[48:32] of STREAMID4 for Filtering on Rx port0

6.1.238. PSFP_SID4_P0_0 (Ask a Question)

Name: PSFP_SID4_P0_0
Offset: 0x360
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID4_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID4_P0_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID4_P0_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID4_P0_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID4_P0_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID4_P0_SA_LSB[31:0] Source address bits[31:0] of STREAMID4 for Filtering on Rx port0

6.1.239. PSFP_SID3_P1_MAX (Ask a Question)

Name: PSFP_SID3_P1_MAX
Offset: 0x44C
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID3 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P1_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P1_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID3_P1_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID3 on RX Port1

6.1.240. PSFP_SID3_P1_FM_CTRL (Ask a Question)

Name: PSFP_SID3_P1_FM_CTRL
Offset: 0x45C
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID3 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID3_P1_CFG_UPD	PSFP_SID3_P1_DRP_MAX_EXCD	PSFP_SID3_P1_DRP_YELLOW	PSFP_SID3_P1_FM_EN	PSFP_SID3_P1_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID3_P1_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID3_P1_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID3
[0]	If Disabled only frames greater than Max packet size are dropped, SID3

Bit 2 – PSFP_SID3_P1_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID3 are dropped
[0]	If Disabled Yellow frames are passed of SID3

Bit 1 – PSFP_SID3_P1_FM_EN

Value	Description
[1]	Policing Enabled for SID3 , RX Port1
[0]	Policing Disabled for SID3 , RX Port1

Bit 0 – PSFP_SID3_P1_FIL_EN

Value	Description
[1]	Filtering Enabled for SID3 , RX Port1
[0]	Filtering Disabled for SID3 , RX Port1

6.1.241. PSFP_SID3_P1_FM_3 (Ask a Question)

Name: PSFP_SID3_P1_FM_3
Offset: 0x528
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID3 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID3_P1_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P1_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P1_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P1_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID3_P1_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID3 RX Port1

Bits 15:0 – PSFP_SID3_P1_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID3 RX Port1

6.1.242. PSFP_SID3_P1_FM_2 (Ask a Question)

Name: PSFP_SID3_P1_FM_2
Offset: 0x458
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID3 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID3_P1_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P1_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P1_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P1_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID3_P1_EIR[31:0] Excess Information Rate allowed for STREAMID3, RX Port1, given in bits per second

6.1.243. PSFP_SID3_P1_FM_1 (Ask a Question)

Name: PSFP_SID3_P1_FM_1
Offset: 0x454
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID3 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID3_P1_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P1_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P1_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P1_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID3_P1_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID3, RX Port1, given in bits per second

6.1.244. PSFP_SID3_P1_FM (Ask a Question)

Name: PSFP_SID3_P1_FM
Offset: 0x450
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID3 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID3_P1_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P1_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P1_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P1_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID3_P1_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID3 RX Port1

Bits 15:0 – PSFP_SID3_P1_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID3, RX Port1,given in Bytes

6.1.245. PSFP_SID3_P1_CTRL (Ask a Question)

Name: PSFP_SID3_P1_CTRL
Offset: 0x448
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID3_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID3_P1_VID_EN	PSFP_SID3_P1_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID3_P1_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID3 , RX Port1
[0]	VLAN ID check Disabled for SID3 , RX Port1

Bit 0 – PSFP_SID3_P1_SA_EN

Value	Description
[1]	Source address check Enabled for SID3 , RX Port1
[0]	Source address check Disabled for SID3 , RX Port1

6.1.246. PSFP_SID3_P1_1 (Ask a Question)

Name: PSFP_SID3_P1_1
Offset: 0x444
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID3_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID3_P1_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P1_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P1_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P1_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID3_P1_VID[11:0] VLAN Identifier of STREAMID3 for Filtering on Rx port1

Bits 15:0 – PSFP_SID3_P1_SA_MSB[15:0] Source address bits[48:32] of STREAMID3 for Filtering on Rx port1

6.1.247. PSFP_SID3_P1_0 (Ask a Question)

Name: PSFP_SID3_P1_0
Offset: 0x440
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID3_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID3_P1_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P1_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P1_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P1_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID3_P1_SA_LSB[31:0] Source address bits[31:0] of STREAMID3 for Filtering on Rx port1

6.1.248. PSFP_SID3_P0_MAX (Ask a Question)

Name: PSFP_SID3_P0_MAX
Offset: 0x34C
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID3 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P0_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P0_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID3_P0_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID3 on RX Port0

6.1.249. PSFP_SID3_P0_FM_CTRL (Ask a Question)

Name: PSFP_SID3_P0_FM_CTRL
Offset: 0x35C
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID3 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID3_P0_CFG_UPD	PSFP_SID3_P0_DRP_MAX_EXCD	PSFP_SID3_P0_DRP_YELLOW	PSFP_SID3_P0_FM_EN	PSFP_SID3_P0_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID3_P0_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID3_P0_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID3
[0]	If Disabled only frames greater than Max packet size are dropped, SID3

Bit 2 – PSFP_SID3_P0_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID3 are dropped
[0]	If Disabled Yellow frames are passed of SID3

Bit 1 – PSFP_SID3_P0_FM_EN

Value	Description
[1]	Policing Enabled for SID3 , RX Port0
[0]	Policing Disabled for SID3 , RX Port0

Bit 0 – PSFP_SID3_P0_FIL_EN

Value	Description
[1]	Filtering Enabled for SID3 , RX Port0
[0]	Filtering Disabled for SID3 , RX Port0

6.1.250. PSFP_SID3_P0_FM_3 (Ask a Question)

Name: PSFP_SID3_P0_FM_3
Offset: 0x508
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID3 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID3_P0_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P0_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P0_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P0_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID3_P0_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID3 RX Port0

Bits 15:0 – PSFP_SID3_P0_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID3 RX Port0

6.1.251. PSFP_SID3_P0_FM_2 (Ask a Question)

Name: PSFP_SID3_P0_FM_2
Offset: 0x358
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID3 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID3_P0_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P0_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P0_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P0_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID3_P0_EIR[31:0] Excess Information Rate allowed for STREAMID3, RX Port0, given in bits per second

6.1.252. PSFP_SID3_P0_FM_1 (Ask a Question)

Name: PSFP_SID3_P0_FM_1
Offset: 0x354
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID3 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID3_P0_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P0_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P0_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P0_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID3_P0_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID3, RX Port0, given in bits per second

6.1.253. PSFP_SID3_P0_FM (Ask a Question)

Name: PSFP_SID3_P0_FM
Offset: 0x350
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID3 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID3_P0_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P0_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P0_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P0_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID3_P0_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID3 RX Port0

Bits 15:0 – PSFP_SID3_P0_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID3, RX Port0,given in Bytes

6.1.254. PSFP_SID3_P0_CTRL (Ask a Question)

Name: PSFP_SID3_P0_CTRL
Offset: 0x348
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID3_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID3_P0_VID_EN	PSFP_SID3_P0_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID3_P0_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID3 , RX Port0
[0]	VLAN ID check Disabled for SID3 , RX Port0

Bit 0 – PSFP_SID3_P0_SA_EN

Value	Description
[1]	Source address check Enabled for SID3 , RX Port0
[0]	Source address check Disabled for SID3 , RX Port0

6.1.255. PSFP_SID3_P0_1 (Ask a Question)

Name: PSFP_SID3_P0_1
Offset: 0x344
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID3_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID3_P0_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P0_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P0_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P0_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID3_P0_VID[11:0] VLAN Identifier of STREAMID3 for Filtering on Rx port0

Bits 15:0 – PSFP_SID3_P0_SA_MSB[15:0] Source address bits[48:32] of STREAMID3 for Filtering on Rx port0

6.1.256. PSFP_SID3_P0_0 (Ask a Question)

Name: PSFP_SID3_P0_0
Offset: 0x340
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID3_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID3_P0_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID3_P0_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID3_P0_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID3_P0_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID3_P0_SA_LSB[31:0] Source address bits[31:0] of STREAMID3 for Filtering on Rx port0

6.1.257. PSFP_SID2_P1_MAX (Ask a Question)

Name: PSFP_SID2_P1_MAX
Offset: 0x42C
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID2 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P1_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P1_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID2_P1_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID2 on RX Port1

6.1.258. PSFP_SID2_P1_FM_CTRL (Ask a Question)

Name: PSFP_SID2_P1_FM_CTRL
Offset: 0x43C
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID2 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID2_P1_CFG_UPD	PSFP_SID2_P1_DRP_MAX_EXCD	PSFP_SID2_P1_DRP_YELLOW	PSFP_SID2_P1_FM_EN	PSFP_SID2_P1_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID2_P1_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID2_P1_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID2
[0]	If Disabled only frames greater than Max packet size are dropped, SID2

Bit 2 – PSFP_SID2_P1_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID2 are dropped
[0]	If Disabled Yellow frames are passed of SID2

Bit 1 – PSFP_SID2_P1_FM_EN

Value	Description
[1]	Policing Enabled for SID2 , RX Port1
[0]	Policing Disabled for SID2 , RX Port1

Bit 0 – PSFP_SID2_P1_FIL_EN

Value	Description
[1]	Filtering Enabled for SID2 , RX Port1
[0]	Filtering Disabled for SID2 , RX Port1

6.1.259. PSFP_SID2_P1_FM_3 (Ask a Question)

Name: PSFP_SID2_P1_FM_3
Offset: 0x524
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID2 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID2_P1_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P1_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P1_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P1_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID2_P1_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID2 RX Port1

Bits 15:0 – PSFP_SID2_P1_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID2 RX Port1

6.1.260. PSFP_SID2_P1_FM_2 (Ask a Question)

Name: PSFP_SID2_P1_FM_2
Offset: 0x438
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID2 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID2_P1_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P1_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P1_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P1_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID2_P1_EIR[31:0] Excess Information Rate allowed for STREAMID2, RX Port1, given in bits per second

6.1.261. PSFP_SID2_P1_FM_1 (Ask a Question)

Name: PSFP_SID2_P1_FM_1
Offset: 0x434
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID2 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID2_P1_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P1_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P1_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P1_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID2_P1_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID2, RX Port1, given in bits per second

6.1.262. PSFP_SID2_P1_FM (Ask a Question)

Name: PSFP_SID2_P1_FM
Offset: 0x430
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID2 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID2_P1_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P1_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P1_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P1_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID2_P1_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,STREAMID2 RX Port1

Bits 15:0 – PSFP_SID2_P1_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID2, RX Port1,given in Bytes

6.1.263. PSFP_SID2_P1_CTRL (Ask a Question)

Name: PSFP_SID2_P1_CTRL
Offset: 0x428
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID2_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID2_P1_VID_EN	PSFP_SID2_P1_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID2_P1_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID2 , RX Port1
[0]	VLAN ID check Disabled for SID2 , RX Port1

Bit 0 – PSFP_SID2_P1_SA_EN

Value	Description
[1]	Source address check Enabled for SID2 , RX Port1
[0]	Source address check Disabled for SID2 , RX Port1

6.1.264. PSFP_SID2_P1_1 (Ask a Question)

Name: PSFP_SID2_P1_1
Offset: 0x424
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID2_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID2_P1_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P1_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P1_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P1_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID2_P1_VID[11:0] VLAN Identifier of StreamID2 for Filtering on Rx port1

Bits 15:0 – PSFP_SID2_P1_SA_MSB[15:0] Source address bits[48:32] of StreamID2 for Filtering on Rx port1

6.1.265. PSFP_SID2_P1_0 (Ask a Question)

Name: PSFP_SID2_P1_0
Offset: 0x420
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID2_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID2_P1_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P1_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P1_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P1_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID2_P1_SA_LSB[31:0] Source address bits[31:0] of StreamID2 for Filtering on Rx port1

6.1.266. PSFP_SID2_P0_MAX (Ask a Question)

Name: PSFP_SID2_P0_MAX
Offset: 0x32C
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID2 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P0_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P0_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID2_P0_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with STREAMID2 on RX Port0

6.1.267. PSFP_SID2_P0_FM_CTRL (Ask a Question)

Name: PSFP_SID2_P0_FM_CTRL
Offset: 0x33C
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID2 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID2_P0_CFG_UPD	PSFP_SID2_P0_DRP_MAX_EXCD	PSFP_SID2_P0_DRP_YELLOW	PSFP_SID2_P0_FM_EN	PSFP_SID2_P0_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID2_P0_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID2_P0_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID2
[0]	If Disabled only frames greater than Max packet size are dropped, SID2

Bit 2 – PSFP_SID2_P0_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID2 are dropped
[0]	If Disabled Yellow frames are passed of SID2

Bit 1 – PSFP_SID2_P0_FM_EN

Value	Description
[1]	Policing Enabled for SID2 , RX Port0
[0]	Policing Disabled for SID2 , RX Port0

Bit 0 – PSFP_SID2_P0_FIL_EN

Value	Description
[1]	Filtering Enabled for SID2 , RX Port0
[0]	Filtering Disabled for SID2 , RX Port0

6.1.268. PSFP_SID2_P0_FM_3 (Ask a Question)

Name: PSFP_SID2_P0_FM_3
Offset: 0x504
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID2 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID2_P0_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P0_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P0_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P0_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID2_P0_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID2 RX Port0

Bits 15:0 – PSFP_SID2_P0_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID2 RX Port0

6.1.269. PSFP_SID2_P0_FM_2 (Ask a Question)

Name: PSFP_SID2_P0_FM_2
Offset: 0x338
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID2 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID2_P0_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P0_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P0_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P0_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID2_P0_EIR[31:0] Excess Information Rate allowed for STREAMID2, RX Port0, given in bits per second

6.1.270. PSFP_SID2_P0_FM_1 (Ask a Question)

Name: PSFP_SID2_P0_FM_1
Offset: 0x334
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID2 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID2_P0_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P0_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P0_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P0_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID2_P0_CIR[31:0] Comitted Information Rate (avg allowed rate) for STREAMID2, RX Port0, given in bits per second

6.1.271. PSFP_SID2_P0_FM (Ask a Question)

Name: PSFP_SID2_P0_FM
Offset: 0x330
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID2 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID2_P0_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P0_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P0_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P0_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID2_P0_EBS_LSB[15:0] Bits[15:0] of Excess Burst size supported on top of CBS, STREAMID2, RX Port0

Bits 15:0 – PSFP_SID2_P0_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID2, RX Port0, given in Bytes

6.1.272. PSFP_SID2_P0_CTRL (Ask a Question)

Name: PSFP_SID2_P0_CTRL
Offset: 0x328
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID2_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID2_P0_VID_EN	PSFP_SID2_P0_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID2_P0_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID2 , RX Port0
[0]	VLAN ID check Disabled for SID2 , RX Port0

Bit 0 – PSFP_SID2_P0_SA_EN

Value	Description
[1]	Source address check Enabled for SID2 , RX Port0
[0]	Source address check Disabled for SID2 , RX Port0

6.1.273. PSFP_SID2_P0_1 (Ask a Question)

Name: PSFP_SID2_P0_1
Offset: 0x324
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID2_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID2_P0_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P0_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P0_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P0_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID2_P0_VID[11:0] VLAN Identifier of StreamID2 for Filtering on Rx port0

Bits 15:0 – PSFP_SID2_P0_SA_MSB[15:0] Source address bits[48:32] of StreamID2 for Filtering on Rx port0

6.1.274. PSFP_SID2_P0_0 (Ask a Question)

Name: PSFP_SID2_P0_0
Offset: 0x320
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID2_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID2_P0_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID2_P0_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID2_P0_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID2_P0_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID2_P0_SA_LSB[31:0] Source address bits[31:0] of StreamID2 for Filtering on Rx port0

6.1.275. PSFP_SID1_P1_MAX (Ask a Question)

Name: PSFP_SID1_P1_MAX
Offset: 0x40C
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID1 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P1_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P1_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID1_P1_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with StreamID1 on RX Port1

6.1.276. PSFP_SID1_P1_FM_CTRL (Ask a Question)

Name: PSFP_SID1_P1_FM_CTRL
Offset: 0x41C
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID1 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID1_P1_CFG_UPD	PSFP_SID1_P1_DRP_MAX_EXCD	PSFP_SID1_P1_DRP_YELLOW	PSFP_SID1_P1_FM_EN	PSFP_SID1_P1_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID1_P1_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID1_P1_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID1
[0]	If Disabled only frames greater than Max packet size are dropped, SID1

Bit 2 – PSFP_SID1_P1_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID1 are dropped
[0]	If Disabled Yellow frames are passed of SID1

Bit 1 – PSFP_SID1_P1_FM_EN

Value	Description
[1]	Policing Enabled for SID1 , RX Port1
[0]	Policing Disabled for SID1 , RX Port1

Bit 0 – PSFP_SID1_P1_FIL_EN

Value	Description
[1]	Filtering Enabled for SID1 , RX Port1
[0]	Filtering Disabled for SID1 , RX Port1

6.1.277. PSFP_SID1_P1_FM_3 (Ask a Question)

Name: PSFP_SID1_P1_FM_3
Offset: 0x520
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID1 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID1_P1_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P1_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P1_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P1_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID1_P1_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID1 RX PORT1

Bits 15:0 – PSFP_SID1_P1_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID1 RX PORT1

6.1.278. PSFP_SID1_P1_FM_2 (Ask a Question)

Name: PSFP_SID1_P1_FM_2
Offset: 0x418
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID1 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID1_P1_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P1_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P1_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P1_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID1_P1_EIR[31:0] Excess Information Rate allowed for StreamID1, RX Port1, given in bits per second

6.1.279. PSFP_SID1_P1_FM_1 (Ask a Question)

Name: PSFP_SID1_P1_FM_1
Offset: 0x414
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID1 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID1_P1_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P1_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P1_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P1_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID1_P1_CIR[31:0] Comitted Information Rate (avg allowed rate) for StreamID1, RX Port1, given in bits per second

6.1.280. PSFP_SID1_P1_FM (Ask a Question)

Name: PSFP_SID1_P1_FM
Offset: 0x410
Reset: 0x0
Property: Read/Write

RX PORT1 STREAMID1 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID1_P1_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P1_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P1_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P1_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID1_P1_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,StreamID1 RX Port1

Bits 15:0 – PSFP_SID1_P1_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID1, RX Port1,given in Bytes

6.1.281. PSFP_SID1_P1_CTRL (Ask a Question)

Name: PSFP_SID1_P1_CTRL
Offset: 0x408
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID1_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID1_P1_VID_EN	PSFP_SID1_P1_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID1_P1_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID1 , RX Port1
[0]	VLAN ID check Disabled for SID1 , RX Port1

Bit 0 – PSFP_SID1_P1_SA_EN

Value	Description
[1]	Source address check Enabled for SID1 , RX Port1
[0]	Source address check Disabled for SID1 , RX Port1

6.1.282. PSFP_SID1_P1_1 (Ask a Question)

Name: PSFP_SID1_P1_1
Offset: 0x404
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID1_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID1_P1_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P1_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P1_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P1_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID1_P1_VID[11:0] VLAN Identifier of StreamID1 for Filtering on Rx port1

Bits 15:0 – PSFP_SID1_P1_SA_MSB[15:0] Source address bits[48:32] of StreamID1 for Filtering on Rx port1

6.1.283. PSFP_SID1_P1_0 (Ask a Question)

Name: PSFP_SID1_P1_0
Offset: 0x400
Reset: 0x0
Property: Read/Write

PSFP_PORT1_STREAMID1_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID1_P1_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P1_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P1_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P1_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID1_P1_SA_LSB[31:0] Source address bits[31:0] of StreamID1 for Filtering on Rx port1

6.1.284. PSFP_SID1_P0_MAX (Ask a Question)

Name: PSFP_SID1_P0_MAX
Offset: 0x30C
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID1 Max Packet Size Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P0_MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P0_MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PSFP_SID1_P0_MAX_PKT_SIZE[15:0] Max Packet size including headers supported for packets with StreamID1 on RX Port0

6.1.285. PSFP_SID1_P0_FM_CTRL (Ask a Question)

Name: PSFP_SID1_P0_FM_CTRL
Offset: 0x31C
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID1 Flow metering/Policing Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				PSFP_SID1_P0_CFG_UPD	PSFP_SID1_P0_DRP_MAX_EXCD	PSFP_SID1_P0_DRP_YELLOW	PSFP_SID1_P0_FM_EN	PSFP_SID1_P0_FIL_EN
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – PSFP_SID1_P0_CFG_UPD The current PSFP configuration is loaded on the rising edge of this bit. Software should write '0' and then '1' to this bit to create the rising edge

Bit 3 – PSFP_SID1_P0_DRP_MAX_EXCD

Value	Description
[1]	If Enabled all the subsequent frames will be dropped if frame exceeds the max packet size even once, SID1
[0]	If Disabled only frames greater than Max packet size are dropped, SID1

Bit 2 – PSFP_SID1_P0_DRP_YELLOW

Value	Description
[1]	If Enabled Yellow frames (excess frames) of SID1 are dropped
[0]	If Disabled Yellow frames are passed of SID1

Bit 1 – PSFP_SID1_P0_FM_EN

Value	Description
[1]	Policing Enabled for SID1 , RX Port0
[0]	Policing Disabled for SID1 , RX Port0

Bit 0 – PSFP_SID1_P0_FIL_EN

Value	Description
[1]	Filtering Enabled for SID1 , RX Port0
[0]	Filtering Disabled for SID1 , RX Port0

6.1.286. PSFP_SID1_P0_FM_3 (Ask a Question)

Name: PSFP_SID1_P0_FM_3
Offset: 0x500
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID1 Flow metering/Policing Register1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID1_P0_EBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P0_EBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P0_CBS_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P0_CBS_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID1_P0_EBS_MSB[15:0] Bits [31:16] of Excess Burst size supported on top of CBS,STREAMID1 RX Port0

Bits 15:0 – PSFP_SID1_P0_CBS_MSB[15:0] Bits [31:16] of the CBS Value,STREAMID1 RX Port0

6.1.287. PSFP_SID1_P0_FM_2 (Ask a Question)

Name: PSFP_SID1_P0_FM_2
Offset: 0x318
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID1 Flow metering/Policing Register 2

Bit	31	30	29	28	27	26	25	24
	PSFP_SID1_P0_EIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P0_EIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P0_EIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P0_EIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID1_P0_EIR[31:0] Excess Information Rate allowed for StreamID1, RX Port0, given in bits per second

6.1.288. PSFP_SID1_P0_FM_1 (Ask a Question)

Name: PSFP_SID1_P0_FM_1
Offset: 0x314
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID1 Flow metering/Policing Register 1

Bit	31	30	29	28	27	26	25	24
	PSFP_SID1_P0_CIR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P0_CIR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P0_CIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P0_CIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID1_P0_CIR[31:0] Comitted Information Rate (avg allowed rate) for StreamID1, RX Port0, given in bits per second

6.1.289. PSFP_SID1_P0_FM (Ask a Question)

Name: PSFP_SID1_P0_FM
Offset: 0x310
Reset: 0x0
Property: Read/Write

RX PORT0 STREAMID1 Flow metering/Policing Register

Bit	31	30	29	28	27	26	25	24
	PSFP_SID1_P0_EBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P0_EBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P0_CBS_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P0_CBS_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PSFP_SID1_P0_EBS_LSB[15:0] Bits[15:0]of Excess Burst size supported on top of CBS,StreamID1 RX Port0

Bits 15:0 – PSFP_SID1_P0_CBS_LSB[15:0] Bits[15:0] of Comitted Burst size(Data allowed in burst without being dropped) STREAMID1, RX Port0,given in Bytes

6.1.290. PSFP_SID1_P0_CTRL (Ask a Question)

Name: PSFP_SID1_P0_CTRL
Offset: 0x308
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID1_CTRL Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_SID1_P0_VID_EN	PSFP_SID1_P0_SA_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_SID1_P0_VID_EN

Value	Description
[1]	VLAN ID check Enabled for SID1 , RX Port0
[0]	VLAN ID check Disabled for SID1 , RX Port0

Bit 0 – PSFP_SID1_P0_SA_EN

Value	Description
[1]	Source address check Enabled for SID1 , RX Port0
[0]	Source address check Disabled for SID1 , RX Port0

6.1.291. PSFP_SID1_P0_1 (Ask a Question)

Name: PSFP_SID1_P0_1
Offset: 0x304
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID1_1

Bit	31	30	29	28	27	26	25	24
					PSFP_SID1_P0_VID[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P0_VID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P0_SA_MSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P0_SA_MSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 27:16 – PSFP_SID1_P0_VID[11:0] VLAN Identifier of StreamID1 for Filtering on Rx port0

Bits 15:0 – PSFP_SID1_P0_SA_MSB[15:0] Source address bits[48:32] of StreamID1 for Filtering on Rx port0

6.1.292. PSFP_SID1_P0_0 (Ask a Question)

Name: PSFP_SID1_P0_0
Offset: 0x300
Reset: 0x0
Property: Read/Write

PSFP_PORT0_STREAMID1_0

Bit	31	30	29	28	27	26	25	24
	PSFP_SID1_P0_SA_LSB[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PSFP_SID1_P0_SA_LSB[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PSFP_SID1_P0_SA_LSB[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PSFP_SID1_P0_SA_LSB[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PSFP_SID1_P0_SA_LSB[31:0] Source address bits[31:0] of StreamID1 for Filtering on Rx port0

6.1.293. PRIORITY_QUEUE_STATUS (Ask a Question)

Name: PRIORITY_QUEUE_STATUS
Offset: 0x28C
Reset: 0x0
Property: Read-only

Priority Queue Status Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	QUEUE7_EMPTY	QUEUE6_EMPTY	QUEUE5_EMPTY	QUEUE4_EMPTY	QUEUE3_EMPTY	QUEUE2_EMPTY	QUEUE1_EMPTY	QUEUE0_EMPTY
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	QUEUE7_FULL	QUEUE6_FULL	QUEUE5_FULL	QUEUE4_FULL	QUEUE3_FULL	QUEUE2_FULL	QUEUE1_FULL	QUEUE0_FULL
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 15 – QUEUE7_EMPTY Queue7 Empty status

Bit 14 – QUEUE6_EMPTY Queue6 Empty status

Bit 13 – QUEUE5_EMPTY Queue5 Empty status

Bit 12 – QUEUE4_EMPTY Queue4 Empty status

Bit 11 – QUEUE3_EMPTY Queue3 Empty status

Bit 10 – QUEUE2_EMPTY Queue2 Empty status

Bit 9 – QUEUE1_EMPTY Queue1 Empty status

Bit 8 – QUEUE0_EMPTY Queue0 Empty status

Bit 7 – QUEUE7_FULL Queue7 Full status

Bit 6 – QUEUE6_FULL Queue6 Full status

Bit 5 – QUEUE5_FULL Queue5 Full status

Bit 4 – QUEUE4_FULL Queue4 Full status

Bit 3 – QUEUE3_FULL Queue3 Full status

Bit 2 – QUEUE2_FULL Queue2 Full status

Bit 1 – QUEUE1_FULL Queue1 Full status

Bit 0 – QUEUE0_FULL Queue0 Full status

6.1.294. prempt_cntrl (Ask a Question)

Name: prempt_cntrl
Offset: 0x000
Reset: 0x0
Property: Read/Write

Pre-emption Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						ADDR_FLAG_SIZE[1:0]		PRE-EMPTION ENABLE / DISABLE
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:1 – ADDR_FLAG_SIZE[1:0]

Value	Description
[11]	252 Bytes
[10]	188 Bytes
[01]	124 Bytes
[00]	60 Bytes

Bit 0 – PRE-EMPTION ENABLE / DISABLE

Value	Description
[1]	Enable
[0]	Disable

6.1.295. MAX_PKT_SIZE_SUPPORT (Ask a Question)

Name: MAX_PKT_SIZE_SUPPORT
Offset: 0x804
Reset: 0x5f2
Property: Read/Write

Max Rx Packet size Register

Bit	31	30	29	28	27	26	25	24
	MAX_PKT_SIZE[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	MAX_PKT_SIZE[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MAX_PKT_SIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	1

Bit	7	6	5	4	3	2	1	0
	MAX_PKT_SIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	0	1	0

Bits 31:0 – MAX_PKT_SIZE[31:0] Maximum packet size at Rx port 0/1, packets greater than this size will be dropped

6.1.296. MAC_TABLE_TIMEOUT (Ask a Question)

Name: MAC_TABLE_TIMEOUT
Offset: 0x800
Reset: 0x7735940
Property: Read/Write

MAC Table Timeout Register

Bit	31	30	29	28	27	26	25	24
	MAC_ENTRY_TIMEOUT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	1

Bit	23	22	21	20	19	18	17	16
	MAC_ENTRY_TIMEOUT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	0	0	1	1

Bit	15	14	13	12	11	10	9	8
	MAC_ENTRY_TIMEOUT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	1	0	0	1

Bit	7	6	5	4	3	2	1	0
	MAC_ENTRY_TIMEOUT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

Bits 31:0 – MAC_ENTRY_TIMEOUT[31:0] Gives the Max timeout for each Entry in the MAC Table, the time for which each entry in the table is held before it is occupied by the new entry

6.1.297. GUARD_BAND_GCL8_GCL9 (Ask a Question)

Name: GUARD_BAND_GCL8_GCL9
Offset: 0x550
Reset: 0x0
Property: Read/Write

Guard Band Register GCL8_GCL9

Bit	31	30	29	28	27	26	25	24
	GCL9_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL9_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL8_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL8_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL9_GUARD_BAND[15:0] Guard Band Value for GCL[9] Entry specified as number of clock cycles

Bits 15:0 – GCL8_GUARD_BAND[15:0] Guard Band Value for GCL[8] Entry specified as number of clock cycles

6.1.298. GUARD_BAND_GCL6_GCL7 (Ask a Question)

Name: GUARD_BAND_GCL6_GCL7
Offset: 0x54C
Reset: 0x0
Property: Read/Write

Guard Band Register GCL6_GCL7

Bit	31	30	29	28	27	26	25	24
	GCL7_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL7_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL6_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL6_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL7_GUARD_BAND[15:0] Guard Band Value for GCL[7] Entry specified as number of clock cycles

Bits 15:0 – GCL6_GUARD_BAND[15:0] Guard Band Value for GCL[6] Entry specified as number of clock cycles

6.1.299. GUARD_BAND_GCL4_GCL5 (Ask a Question)

Name: GUARD_BAND_GCL4_GCL5
Offset: 0x548
Reset: 0x0
Property: Read/Write

Guard Band Register GCL4_GCL5

Bit	31	30	29	28	27	26	25	24
	GCL5_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL5_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL4_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL4_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL5_GUARD_BAND[15:0] Guard Band Value for GCL[5] Entry specified as number of clock cycles

Bits 15:0 – GCL4_GUARD_BAND[15:0] Guard Band Value for GCL[4] Entry specified as number of clock cycles

6.1.300. GUARD_BAND_GCL30_GCL31 (Ask a Question)

Name: GUARD_BAND_GCL30_GCL31
Offset: 0x57C
Reset: 0x0
Property: Read/Write

Guard Band Register GCL30_GCL31

Bit	31	30	29	28	27	26	25	24
	GCL31_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL31_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL30_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL30_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL31_GUARD_BAND[15:0] Guard Band Value for GCL[31] Entry specified as number of clock cycles

Bits 15:0 – GCL30_GUARD_BAND[15:0] Guard Band Value for GCL[30] Entry specified as number of clock cycles

6.1.301. GUARD_BAND_GCL28_GCL29 (Ask a Question)

Name: GUARD_BAND_GCL28_GCL29
Offset: 0x578
Reset: 0x0
Property: Read/Write

Guard Band Register GCL28_GCL29

Bit	31	30	29	28	27	26	25	24
	GCL29_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL29_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL28_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL28_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL29_GUARD_BAND[15:0] Guard Band Value for GCL[29] Entry specified as number of clock cycles

Bits 15:0 – GCL28_GUARD_BAND[15:0] Guard Band Value for GCL[28] Entry specified as number of clock cycles

6.1.302. GUARD_BAND_GCL2_GCL3 (Ask a Question)

Name: GUARD_BAND_GCL2_GCL3
Offset: 0x544
Reset: 0x0
Property: Read/Write

Guard Band Register GCL2_GCL3

Bit	31	30	29	28	27	26	25	24
	GCL3_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL3_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL2_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL2_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL3_GUARD_BAND[15:0] Guard Band Value for GCL[3] Entry specified as number of clock cycles

Bits 15:0 – GCL2_GUARD_BAND[15:0] Guard Band Value for GCL[2] Entry specified as number of clock cycles

6.1.303. GUARD_BAND_GCL26_GCL27 (Ask a Question)

Name: GUARD_BAND_GCL26_GCL27
Offset: 0x574
Reset: 0x0
Property: Read/Write

Guard Band Register GCL26_GCL27

Bit	31	30	29	28	27	26	25	24
	GCL27_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL27_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL26_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL26_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL27_GUARD_BAND[15:0] Guard Band Value for GCL[27] Entry specified as number of clock cycles

Bits 15:0 – GCL26_GUARD_BAND[15:0] Guard Band Value for GCL[26] Entry specified as number of clock cycles

6.1.304. GUARD_BAND_GCL24_GCL25 (Ask a Question)

Name: GUARD_BAND_GCL24_GCL25
Offset: 0x570
Reset: 0x0
Property: Read/Write

Guard Band Register GCL24_GCL25

Bit	31	30	29	28	27	26	25	24
	GCL25_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL25_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL24_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL24_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL25_GUARD_BAND[15:0] Guard Band Value for GCL[25] Entry specified as number of clock cycles

Bits 15:0 – GCL24_GUARD_BAND[15:0] Guard Band Value for GCL[24] Entry specified as number of clock cycles

6.1.305. GUARD_BAND_GCL22_GCL23 (Ask a Question)

Name: GUARD_BAND_GCL22_GCL23
Offset: 0x56C
Reset: 0x0
Property: Read/Write

Guard Band Register GCL22_GCL23

Bit	31	30	29	28	27	26	25	24
	GCL23_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL23_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL22_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL22_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL23_GUARD_BAND[15:0] Guard Band Value for GCL[23] Entry specified as number of clock cycles

Bits 15:0 – GCL22_GUARD_BAND[15:0] Guard Band Value for GCL[22] Entry specified as number of clock cycles

6.1.306. GUARD_BAND_GCL20_GCL21 (Ask a Question)

Name: GUARD_BAND_GCL20_GCL21
Offset: 0x568
Reset: 0x0
Property: Read/Write

Guard Band Register GCL20_GCL21

Bit	31	30	29	28	27	26	25	24
	GCL21_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL21_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL20_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL20_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL21_GUARD_BAND[15:0] Guard Band Value for GCL[21] Entry specified as number of clock cycles

Bits 15:0 – GCL20_GUARD_BAND[15:0] Guard Band Value for GCL[20] Entry specified as number of clock cycles

6.1.307. GUARD_BAND_GCL18_GCL19 (Ask a Question)

Name: GUARD_BAND_GCL18_GCL19
Offset: 0x564
Reset: 0x0
Property: Read/Write

Guard Band Register GCL18_GCL19

Bit	31	30	29	28	27	26	25	24
	GCL19_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL19_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL18_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL18_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL19_GUARD_BAND[15:0] Guard Band Value for GCL[19] Entry specified as number of clock cycles

Bits 15:0 – GCL18_GUARD_BAND[15:0] Guard Band Value for GCL[18] Entry specified as number of clock cycles

6.1.308. GUARD_BAND_GCL16_GCL17 (Ask a Question)

Name: GUARD_BAND_GCL16_GCL17
Offset: 0x560
Reset: 0x0
Property: Read/Write

Guard Band Register GCL16_GCL17

Bit	31	30	29	28	27	26	25	24
	GCL17_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL17_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL16_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL16_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL17_GUARD_BAND[15:0] Guard Band Value for GCL[17] Entry specified as number of clock cycles

Bits 15:0 – GCL16_GUARD_BAND[15:0] Guard Band Value for GCL[16] Entry specified as number of clock cycles

6.1.309. GUARD_BAND_GCL14_GCL15 (Ask a Question)

Name: GUARD_BAND_GCL14_GCL15
Offset: 0x55C
Reset: 0x0
Property: Read/Write

Guard Band Register GCL14_GCL15

Bit	31	30	29	28	27	26	25	24
	GCL15_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL15_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL14_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL14_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL15_GUARD_BAND[15:0] Guard Band Value for GCL[15] Entry specified as number of clock cycles

Bits 15:0 – GCL14_GUARD_BAND[15:0] Guard Band Value for GCL[14] Entry specified as number of clock cycles

6.1.310. GUARD_BAND_GCL12_GCL13 (Ask a Question)

Name: GUARD_BAND_GCL12_GCL13
Offset: 0x558
Reset: 0x0
Property: Read/Write

Guard Band Register GCL12_GCL13

Bit	31	30	29	28	27	26	25	24
	GCL13_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL13_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL12_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL12_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL13_GUARD_BAND[15:0] Guard Band Value for GCL[13] Entry specified as number of clock cycles

Bits 15:0 – GCL12_GUARD_BAND[15:0] Guard Band Value for GCL[12] Entry specified as number of clock cycles

6.1.311. GUARD_BAND_GCL10_GCL11 (Ask a Question)

Name: GUARD_BAND_GCL10_GCL11
Offset: 0x554
Reset: 0x0
Property: Read/Write

Guard Band Register GCL10_GCL11

Bit	31	30	29	28	27	26	25	24
	GCL11_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL11_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL10_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL10_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL11_GUARD_BAND[15:0] Guard Band Value for GCL[11] Entry specified as number of clock cycles

Bits 15:0 – GCL10_GUARD_BAND[15:0] Guard Band Value for GCL[10] Entry specified as number of clock cycles

6.1.312. GUARD_BAND_GCL0_GCL1 (Ask a Question)

Name: GUARD_BAND_GCL0_GCL1
Offset: 0x540
Reset: 0x0
Property: Read/Write

Guard Band Register GCL0_GCL1

Bit	31	30	29	28	27	26	25	24
	GCL1_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	GCL1_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GCL0_GUARD_BAND[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GCL0_GUARD_BAND[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – GCL1_GUARD_BAND[15:0] Guard Band Value for GCL[1] Entry specified as number of clock cycles

Bits 15:0 – GCL0_GUARD_BAND[15:0] Guard Band Value for GCL[0] Entry specified as number of clock cycles

6.1.313. Gate State Control (Ask a Question)

Name: Gate State Control
Offset: 0x080
Reset: 0xff
Property: Read/Write

Gate State Register when scheduler is not enabled

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	GATE STATE Q7	GATE STATE Q6	GATE STATE Q5	GATE STATE Q4	GATE STATE Q3	GATE STATE Q2	GATE STATE Q1	GATE STATE Q0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 7 – GATE STATE Q7

Value	Description
[1]	Open
[0]	Closed

Bit 6 – GATE STATE Q6

Value	Description
[1]	Open
[0]	Closed

Bit 5 – GATE STATE Q5

Value	Description
[1]	Open
[0]	Closed

Bit 4 – GATE STATE Q4

Value	Description
[1]	Open
[0]	Closed

Bit 3 – GATE STATE Q3

Value	Description
[1]	Open
[0]	Closed

Bit 2 – GATE STATE Q2

Value	Description
[1]	Open
[0]	Closed

Bit 1 – GATE STATE Q1

Value	Description
[1]	Open
[0]	Closed

Bit 0 – GATE STATE Q0

Value	Description
[1]	Open
[0]	Closed

6.1.314. Gate Control List9 Register (Ask a Question)

Name: Gate Control List9 Register
Offset: 0x0B0
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[9] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[9].

6.1.315. Gate Control (Ask a Question)

Name: Gate Control
Offset: 0x024
Reset: 0x0
Property: Read/Write

Gate Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					GATE_EN	CFG_VAL		
Access					R/W	R/W		
Reset					0	0		

Bit 3 – GATE_EN

Value	Description
[1]	Enable
[0]	Disable

Bit 2 – CFG_VAL GCL configuration is valid.GCL configuration is considered valid on the rising edge of this bit. The s/w needs to write 0 and then 1 for every new configuration uploaded.

6.1.316. Gate Control List8 Register (Ask a Question)

Name: Gate Control List8 Register
Offset: 0x0AC
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[8] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[8].

6.1.317. Gate Control List7 Register (Ask a Question)

Name: Gate Control List7 Register
Offset: 0x0A8
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[7] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL LIST[7].

6.1.318. Gate Control List6 Register (Ask a Question)

Name: Gate Control List6 Register
Offset: 0x0A4
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[6] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL LIST[6].

6.1.319. Gate Control List5 Register (Ask a Question)

Name: Gate Control List5 Register
Offset: 0x0A0
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[5] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL LIST[5].

6.1.320. Gate Control List4 Register (Ask a Question)

Name: Gate Control List4 Register
Offset: 0x09C
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[4] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL LIST[4].

6.1.321. Gate Control List31 Register (Ask a Question)

Name: Gate Control List31 Register
Offset: 0x108
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[31] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[31].

6.1.322. Gate Control List30 Register (Ask a Question)

Name: Gate Control List30 Register
Offset: 0x104
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[30] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[30].

6.1.323. Gate Control List3 Register (Ask a Question)

Name: Gate Control List3 Register
Offset: 0x098
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[3] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL LIST[3].

6.1.324. Gate Control List29 Register (Ask a Question)

Name: Gate Control List29 Register
Offset: 0x100
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[29] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[29].

6.1.325. Gate Control List28 Register (Ask a Question)

Name: Gate Control List28 Register
Offset: 0x0FC
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[28] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[28].

6.1.326. Gate Control List27 Register (Ask a Question)

Name: Gate Control List27 Register
Offset: 0x0F8
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[27] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[27].

6.1.327. Gate Control List26 Register (Ask a Question)

Name: Gate Control List26 Register
Offset: 0x0F4
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[26] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[26].

6.1.328. Gate Control List25 Register (Ask a Question)

Name: Gate Control List25 Register
Offset: 0x0F0
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[25] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[25].

6.1.329. Gate Control List24 Register (Ask a Question)

Name: Gate Control List24 Register
Offset: 0x0EC
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[24] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[24].

6.1.330. Gate Control List23 Register (Ask a Question)

Name: Gate Control List23 Register
Offset: 0x0E8
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[23] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[23].

6.1.331. Gate Control List22 Register (Ask a Question)

Name: Gate Control List22 Register
Offset: 0x0E4
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[22] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[22].

6.1.332. Gate Control List21 Register (Ask a Question)

Name: Gate Control List21 Register
Offset: 0x0E0
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[21] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[21].

6.1.333. Gate Control List20 Register (Ask a Question)

Name: Gate Control List20 Register
Offset: 0x0DC
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[20] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[20].

6.1.334. Gate Control List2 Register (Ask a Question)

Name: Gate Control List2 Register
Offset: 0x094
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[2] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL LIST[2].

6.1.335. Gate Control List19 Register (Ask a Question)

Name: Gate Control List19 Register
Offset: 0x0D8
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[19] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[19].

6.1.336. Gate Control List18 Register (Ask a Question)

Name: Gate Control List18 Register
Offset: 0x0D4
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[18] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[18].

6.1.337. Gate Control List17 Register (Ask a Question)

Name: Gate Control List17 Register
Offset: 0x0D0
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[17] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[17].

6.1.338. Gate Control List16 Register (Ask a Question)

Name: Gate Control List16 Register
Offset: 0x0CC
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[16] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[16].

6.1.339. Gate Control List15 Register (Ask a Question)

Name: Gate Control List15 Register
Offset: 0x0C8
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[14] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[15].

6.1.340. Gate Control List14 Register (Ask a Question)

Name: Gate Control List14 Register
Offset: 0x0C4
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[14] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[14].

6.1.341. Gate Control List13 Register (Ask a Question)

Name: Gate Control List13 Register
Offset: 0x0C0
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[13] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[13].

6.1.342. Gate Control List12 Register (Ask a Question)

Name: Gate Control List12 Register
Offset: 0x0BC
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[12] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[12].

6.1.343. Gate Control List11 Register (Ask a Question)

Name: Gate Control List11 Register
Offset: 0x0B8
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[11] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[11].

6.1.344. Gate Control List10 Register (Ask a Question)

Name: Gate Control List10 Register
Offset: 0x0B4
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[10] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL List[10].

6.1.345. Gate Control List1 Register (Ask a Question)

Name: Gate Control List1 Register
Offset: 0x090
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[1] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL LIST[1].

6.1.346. Gate Control List0 Register (Ask a Question)

Name: Gate Control List0 Register
Offset: 0x08C
Reset: 0xFF000000
Property: Read/Write

Scheduler Gate Control List[0] Entry Register

Bit	31	30	29	28	27	26	25	24
	GATE7_STATE	GATE6_STATE	GATE5_STATE	GATE4_STATE	GATE3_STATE	GATE2_STATE	GATE1_STATE	GATE0_STATE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TIME_INTERVAL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIME_INTERVAL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIME_INTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – GATE7_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 30 – GATE6_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 29 – GATE5_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 28 – GATE4_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 27 – GATE3_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 26 – GATE2_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 25 – GATE1_STATE

Value	Description
[1]	Open
[0]	Closed

Bit 24 – GATE0_STATE

Value	Description
[1]	Open
[0]	Closed

Bits 23:0 – TIME_INTERVAL[23:0] Time Interval of GCL LIST[0].

6.1.347. FRER_PSFP Control (Ask a Question)

Name: FRER_PSFP Control
Offset: 0x160
Reset: 0x0
Property: Read/Write

FRER PSFP Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							PSFP_EN	FRER_EN
Access							R/W	R/W
Reset							0	0

Bit 1 – PSFP_EN

Value	Description
[1]	PSFP Block is Enabled
[0]	PSFP Block is Disabled

Bit 0 – FRER_EN

Value	Description
[1]	FRER Block is Enabled
[0]	FRER Block is Disabled

6.1.348. CBS_Q1 (Ask a Question)

Name: CBS_Q1
Offset: 0x22C
Reset: 0x0
Property: Read/Write

CBS Register Q1

Bit	31	30	29	28	27	26	25	24
	CREDIT_DECR_Q1[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREDIT_DECR_Q1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
		CREDIT_INCR_Q1[14:8]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREDIT_INCR_Q1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – CREDIT_DECR_Q1[15:0] CBS Credit Decrement for Queue1,positive value to be written treated as negative inside the Core

Bits 14:0 – CREDIT_INCR_Q1[14:0] CBS Credit increment for Queue1

6.1.349. CBS_Min_Q1 (Ask a Question)

Name: CBS_Min_Q1
Offset: 0x238
Reset: 0x0
Property: Read/Write

CBS Minimum value Register Q1

Bit	31	30	29	28	27	26	25	24
		CREDIT_MIN_Q1[30:24]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREDIT_MIN_Q1[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREDIT_MIN_Q1[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREDIT_MIN_Q1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 30:0 – CREDIT_MIN_Q1[30:0] Credit Minimum value for Queue1,positive value to be written treated as neagative inside the core

6.1.350. CBS_Q0 (Ask a Question)

Name: CBS_Q0
Offset: 0x228
Reset: 0x0
Property: Read/Write

CBS Register Q0

Bit	31	30	29	28	27	26	25	24
	CREDIT_DECR_Q0[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREDIT_DECR_Q0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREDIT_INCR_Q0[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREDIT_INCR_Q0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – CREDIT_DECR_Q0[15:0] CBS Credit Decrement for Queue0,positive value to be written treated as negative inside the Core

Bits 15:0 – CREDIT_INCR_Q0[15:0] CBS Credit increment for Queue0

6.1.351. CBS_Min_Q0 (Ask a Question)

Name: CBS_Min_Q0
Offset: 0x230
Reset: 0x0
Property: Read/Write

CBS Minimum value Register Q0

Bit	31	30	29	28	27	26	25	24
		CREDIT_MIN_Q0[30:24]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREDIT_MIN_Q0[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREDIT_MIN_Q0[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREDIT_MIN_Q0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 30:0 – CREDIT_MIN_Q0[30:0] Credit Minimum value for Queue0,positive value to be written treated as neagative inside the core

6.1.352. CBS_Max_Q1 (Ask a Question)

Name: CBS_Max_Q1
Offset: 0x23C
Reset: 0x0
Property: Read/Write

CBS Maximum value Register Q1

Bit	31	30	29	28	27	26	25	24
		CREDIT_MAX_Q1[30:24]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREDIT_MAX_Q1[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREDIT_MAX_Q1[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREDIT_MAX_Q1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 30:0 – CREDIT_MAX_Q1[30:0] Credit Maximum value for Queue1

6.1.353. CBS_Max_Q0 (Ask a Question)

Name: CBS_Max_Q0
Offset: 0x234
Reset: 0x0
Property: Read/Write

CBS Maximum value Register Q0

Bit	31	30	29	28	27	26	25	24
		CREDIT_MAX_Q0[30:24]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CREDIT_MAX_Q0[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CREDIT_MAX_Q0[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREDIT_MAX_Q0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 30:0 – CREDIT_MAX_Q0[30:0] Credit Maximum value for Queue0

6.1.354. CBS_CTRL (Ask a Question)

Name: CBS_CTRL
Offset: 0x224
Reset: 0x0
Property: Read/Write

CBS Control Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							CBS_EN_Q1	CBS_EN_Q0
Access							R/W	R/W
Reset							0	0

Bit 1 – CBS_EN_Q1

Value	Description
[1]	CBS Enabled, Q1
[0]	CBS Disabled, Q1

Bit 0 – CBS_EN_Q0

Value	Description
[1]	CBS Enabled, Q0
[0]	CBS Disabled, Q0

6.1.355. Base Time High Register1 (Ask a Question)

Name: Base Time High Register1
Offset: 0x078
Reset: 0x0
Property: Read/Write

Base Time Seconds Register1

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	BASE_TIME_S1[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BASE_TIME_S1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BASE_TIME_S1[15:0] Base Time Seconds (MSB) is specified in this register.

6.1.356. Base Time High Register0 (Ask a Question)

Name: Base Time High Register0
Offset: 0x074
Reset: 0x0
Property: Read/Write

Base Time Seconds Register0

Bit	31	30	29	28	27	26	25	24
	BASE_TIME_S0[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BASE_TIME_S0[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BASE_TIME_S0[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BASE_TIME_S0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – BASE_TIME_S0[31:0] Base Time Seconds(LSB) is specified in this register.

6.1.357. Base Time Low Register (Ask a Question)

Name: Base Time Low Register
Offset: 0x070
Reset: 0x0
Property: Read/Write

Base Time Nano seconds

Bit	31	30	29	28	27	26	25	24
			BASE_TIME_NS[29:24]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BASE_TIME_NS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BASE_TIME_NS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BASE_TIME_NS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 29:0 – BASE_TIME_NS[29:0] Base Time nano seconds is specified in this register.

6.1.358. Base Time Adjust (Ask a Question)

Name: Base Time Adjust
Offset: 0x118
Reset: 0x0
Property: Read/Write

Scheduler Base Time Adjust Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				BASE_TIME_ADJUST[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – BASE_TIME_ADJUST[4:0]

Value	Description
[00001]	Base Time Low Register bit 0 is ignored for the comparision of the Scheduler start time. If none of the bits are set,[2:0] are ignored.
[00010]	Base Time Low Register [1:0] are ignored for the comparision of the Scheduler start time.
[00100]	Base Time Low Register [2:0] are ignored for the comparision of the Scheduler start time.
[01000]	Base Time Low Register [3:0] are ignored for the comparision of the Scheduler start time.
[10000]	Base Time Low Register [4:0] are ignored for the comparision of the Scheduler start time.

6.2. MACREG Register Summary (Ask a Question)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	MACConfiguration1	7:0					SYNCHRONIZED RECEIVE ENABLE	RECEIVE ENABLE	SYNCHRONIZED TRANSMIT ENABLE	TRANSMIT ENABLE
		15:8								
		23:16								
		31:24	SOFT RESET							
0x04	MACConfiguration2	7:0			HUGE FRAME ENABLE	LENGTH FIELD CHECKING		PAD/CRC ENABLE	CRC ENABLE	FULL-DUPLEX
		15:8	PREAMBLE LENGTH[3:0]						INTERFACE MODE[1:0]	
		23:16								
		31:24								
0x08	IPG	7:0		BACK_TO_BACK INTER_PACKET_GAP[6:0]						
		15:8	MINIMUM IFG ENFORCEMENT[7:0]							
		23:16	NON_BACK_TO_BACK INTER_PACKET_GAP[7:0]							
		31:24								
0x0C ... 0x0F	Reserved									
0x10	Maximum_Frame_Length	7:0	MAXIMUM FRAME LENGTH[7:0]							
		15:8	MAXIMUM FRAME LENGTH[15:8]							
		23:16								
		31:24								
0x14 ... 0x1F	Reserved									
0x20	MIIMgmt_Configuration	7:0			SCAN AUTO INCREMENT	PREAMBLE SUPPRESSION		MGMT CLOCK SELECT[2:0]		
		15:8								
		23:16								
		31:24	RESET MDIO MGMT							
0x24	MIIMgmt_Command	7:0							SCAN CYCLE	READ CYCLE
		15:8								
		23:16								
		31:24								
0x28	MIIMgmt_Address	7:0				REGISTER ADDRESS[4:0]				
		15:8				PHY ADDRESS[4:0]				
		23:16								
		31:24								
0x2C	MIIMgmt_Control	7:0	MDIO MGMT CONTROL (PHY CONTROL)[7:0]							
		15:8	MDIO MGMT CONTROL (PHY CONTROL)[15:8]							
		23:16								
		31:24								
0x30	MIIMgmt_Status	7:0	MDIO MGMT STATUS (PHY STATUS)[7:0]							
		15:8	MDIO MGMT STATUS (PHY STATUS)[15:8]							
		23:16								
		31:24								
0x34	MIIMgmt_Indicators	7:0						NOT VALID	SCANNING	BUSY
		15:8								
		23:16								
		31:24								

MACREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x38	Interface_Control	7:0				STATS COUNTERS : AUTO CLEAR COUNTERS ON READ	STATS COUNTERS : CLEAR ALL COUNTERS	STATS COUNTERS : MODULE ENABLE		
		15:8								
		23:16								
		31:24								
0x3C	Interface_Status	7:0					LINK FAIL			
		15:8							EXCESS DEFER	
		23:16								
		31:24								
0x40 ... 0x7F	Reserved									
0x80	TR64	7:0	TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [17:16]	
		31:24								
0x84	TR127	7:0	TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [17:16]	
		31:24								
0x88	TR255	7:0	TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [17:16]	
		31:24								
0x8C	TR511	7:0	TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [17:16]	
		31:24								
0x90	TR1K	7:0	TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [17:16]	
		31:24								
0x94	TRMAX	7:0	TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [17:16]	
		31:24								
0x98	TRMGV	7:0	TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [17:16]	
		31:24								

MACREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x9C	RBYT	7:0	RECEIVE BYTE COUNTER [7:0]							
		15:8	RECEIVE BYTE COUNTER [15:8]							
		23:16							RECEIVE BYTE COUNTER [17:16]	
		31:24								
0xA0	RPKT	7:0	RECEIVE PACKET COUNTER [7:0]							
		15:8	RECEIVE PACKET COUNTER [15:8]							
		23:16							RECEIVE PACKET COUNTER [17:16]	
		31:24								
0xA4	RFCS	7:0	RECEIVE FCS ERROR COUNTER [7:0]							
		15:8	RECEIVE FCS ERROR COUNTER [15:8]							
		23:16							RECEIVE FCS ERROR COUNTER [17:16]	
		31:24								
0xA8	RMCA	7:0	RECEIVE MULTICAST PACKET COUNTER [7:0]							
		15:8	RECEIVE MULTICAST PACKET COUNTER [15:8]							
		23:16							RECEIVE MULTICAST PACKET COUNTER [17:16]	
		31:24								
0xAC	RBCA	7:0	RECEIVE BROADCAST PACKET COUNTER [7:0]							
		15:8	RECEIVE BROADCAST PACKET COUNTER [15:8]							
		23:16							RECEIVE BROADCAST PACKET COUNTER [17:16]	
		31:24								
0xB0	RXCF	7:0	RECEIVE CONTROL FRAME PACKET COUNTER [7:0]							
		15:8	RECEIVE CONTROL FRAME PACKET COUNTER [15:8]							
		23:16							RECEIVE CONTROL FRAME PACKET COUNTER [17:16]	
		31:24								
0xB4 ... 0xBB	Reserved									
0xBC	RALN	7:0	RECEIVE ALIGNMENT ERROR COUNTER [7:0]							
		15:8					RECEIVE ALIGNMENT ERROR COUNTER [11:8]			
		23:16								
		31:24								
0xC0	RFLR	7:0	RECEIVE FRAME LENGTH ERROR COUNTER [7:0]							
		15:8	RECEIVE FRAME LENGTH ERROR COUNTER [15:8]							
		23:16								
		31:24								
0xC4 ... 0xCB	Reserved									
0xCC	RUND	7:0	RECEIVE UNDERSIZE PACKET COUNTER [7:0]							
		15:8					RECEIVE UNDERSIZE PACKET COUNTER [11:8]			
		23:16								
		31:24								
0xD0	ROVR	7:0	RECEIVE OVERSIZE PACKET COUNTER [7:0]							
		15:8					RECEIVE OVERSIZE PACKET COUNTER [11:8]			
		23:16								
		31:24								
0xD4	RFRG	7:0	RECEIVE FRAGMENTS COUNTER [7:0]							
		15:8					RECEIVE FRAGMENTS COUNTER [11:8]			
		23:16								
		31:24								
0xD8	RJBR	7:0	RECEIVE JABBER COUNTER [7:0]							
		15:8					RECEIVE JABBER COUNTER [11:8]			
		23:16								
		31:24								

MACREG Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xDC ... 0xDF	Reserved									
0xE0	TBYT	7:0	TRANSMIT BYTE COUNTER [7:0]							
		15:8	TRANSMIT BYTE COUNTER [15:8]							
		23:16	TRANSMIT BYTE COUNTER [23:16]							
		31:24								
0xE4	TPKT	7:0	TRANSMIT PACKET COUNTER [7:0]							
		15:8	TRANSMIT PACKET COUNTER [15:8]							
		23:16							TRANSMIT PACKET COUNTER [17:16]	
		31:24								
0xE8	TMCA	7:0	TRANSMIT MULTICAST PACKET COUNTER [7:0]							
		15:8	TRANSMIT MULTICAST PACKET COUNTER [15:8]							
		23:16							TRANSMIT MULTICAST PACKET COUNTER [17:16]	
		31:24								
0xEC	TBCA	7:0	TRANSMIT BROADCAST PACKET COUNTER [7:0]							
		15:8	TRANSMIT BROADCAST PACKET COUNTER [15:8]							
		23:16							TRANSMIT BROADCAST PACKET COUNTER [17:16]	
		31:24								
0xF0 ... 0x0117	Reserved									
0x0118	TJBR	7:0	TRANSMIT JABBER FRAME COUNTER [7:0]							
		15:8					TRANSMIT JABBER FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x011C	TFCS	7:0	TRANSMIT FCS ERROR COUNTER [7:0]							
		15:8					TRANSMIT FCS ERROR COUNTER [11:8]			
		23:16								
		31:24								
0x0120	TXCF	7:0	TRANSMIT CONTROL FRAME COUNTER [7:0]							
		15:8					TRANSMIT CONTROL FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x0124	TOVR	7:0	TRANSMIT OVERSIZE FRAME COUNTER [7:0]							
		15:8					TRANSMIT OVERSIZE FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x0128	TUND	7:0	TRANSMIT UNDER SIZE FRAME COUNTER [7:0]							
		15:8					TRANSMIT UNDER SIZE FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x012C	TFRG	7:0	TRANSMIT FRAGMENTS FRAME COUNTER [7:0]							
		15:8					TRANSMIT FRAGMENTS FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x0130 ... 0x01BF	Reserved									
0x01C0	Framefiltercontrols	7:0			FRAME FILTER CONTROLS[5:0]					
		15:8								
		23:16								
		31:24								

6.2.1. TXCF (Ask a Question)

Name: TXCF
Offset: 0x120
Reset: 0x0
Property: Read-only

TXCF- Transmit Control Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT CONTROL FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT CONTROL FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT CONTROL FRAME COUNTER [11:0] Incremented for every valid size frame with a Type Field signifying a Control frame.

6.2.2. TUND (Ask a Question)

Name: TUND
Offset: 0x128
Reset: 0x0
Property: Read-only

TUND- Transmit Under size Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT UNDER SIZE FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT UNDER SIZE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT UNDER SIZE FRAME COUNTER [11:0] Incremented for every frame less than 64 bytes, with a correct FCS value

6.2.3. TRMGV (Ask a Question)

Name: TRMGV
Offset: 0x098
Reset: 0x0
Property: Read-only

TRMGV-Transmit & Receive 1519 to 1522 Byte VLAN Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [17:0] Incremented for each good or bad VLAN frame transmitted and received which is 1519 to 1522 bytes in length inclusive (excluding framing bits) but including FCS bytes.

6.2.4. TRMAX (Ask a Question)

Name: TRMAX
Offset: 0x094
Reset: 0x0
Property: Read-only

TRMAX - Transmit & Receive 1024 to 1518 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 1024 to 1518 bytes in length inclusive (excluding framing bits) but including FCS bytes.

6.2.5. TR64 (Ask a Question)

Name: TR64
Offset: 0x080
Reset: 0x0
Property: Read-only

TR64 - Transmit & Receive 64 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing bits) but including FCS bytes.

6.2.6. TR511 (Ask a Question)

Name: TR511
Offset: 0x08C
Reset: 0x0
Property: Read-only

TR511 - Transmit & Receive 256 to 511 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 256 to 511 bytes in length inclusive (excluding framing bits) but including FCS bytes.

6.2.7. TR255 (Ask a Question)

Name: TR255
Offset: 0x088
Reset: 0x0
Property: Read-only

TR255 - Transmit & Receive 128 to 255 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 128 to 255 bytes in length inclusive (excluding framing bits) but including FCS bytes.

6.2.8. TR1K (Ask a Question)

Name: TR1K
Offset: 0x090
Reset: 0x0
Property: Read-only

TR1K - Transmit & Receive 512 to 1023 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 512 to 1023 bytes in length inclusive (excluding framing bits) but including FCS bytes.

6.2.9. TR127 (Ask a Question)

Name: TR127
Offset: 0x084
Reset: 0x0
Property: Read-only

TR127 - Transmit & Receive 65 to 127 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 65 to 127 bytes in length inclusive (excluding framing bits) but including FCS bytes.

6.2.10. TPKT (Ask a Question)

Name: TPKT
Offset: 0x0E4
Reset: 0x0
Property: Read-only

TPKT- Transmit Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT PACKET COUNTER [17:0] Incremented for each transmitted packet (including bad packets, excessive deferred packets, all Unicast, Broadcast, and Multicast packets).

6.2.11. TOVR (Ask a Question)

Name: TOVR
Offset: 0x124
Reset: 0x0
Property: Read-only

TOVR- Transmit Oversize Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT OVERSIZE FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT OVERSIZE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT OVERSIZE FRAME COUNTER [11:0] Incremented for each oversized transmitted frame with a correct FCS value.

6.2.12. TMCA (Ask a Question)

Name: TMCA
Offset: 0x0E8
Reset: 0x0
Property: Read-only

TMCA- Transmit Multicast Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT MULTICAST PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT MULTICAST PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT MULTICAST PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT MULTICAST PACKET COUNTER [17:0] Incremented for each Multicast valid frame transmitted (excluding Broadcast frames).

6.2.13. TJBR (Ask a Question)

Name: TJBR
Offset: 0x118
Reset: 0x0
Property: Read-only

TJBR-TransmitJabberFrameCounter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT JABBER FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT JABBER FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT JABBER FRAME COUNTER [11:0] Incremented for each oversized transmitted frame with an incorrect FCS value

6.2.14. TFRG (Ask a Question)

Name: TFRG
Offset: 0x12C
Reset: 0x0
Property: Read-only

TFRG- Transmit Fragments Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT FRAGMENTS FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT FRAGMENTS FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT FRAGMENTS FRAME COUNTER [11:0] Incremented for every frame less than 64 bytes, with an incorrect FCS value

6.2.15. TFCS (Ask a Question)

Name: TFCS
Offset: 0x11C
Reset: 0x0
Property: Read-only

TFCS- Transmit FCS Error Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT FCS ERROR COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT FCS ERROR COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT FCS ERROR COUNTER [11:0] Incremented for every valid sized packet with an incorrect FCS value.

6.2.16. TBYT (Ask a Question)

Name: TBYT
Offset: 0x0E0
Reset: 0x0
Property: Read-only

TBYT- Transmit Byte Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	TRANSMIT BYTE COUNTER [23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT BYTE COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT BYTE COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – TRANSMIT BYTE COUNTER [23:0] Incremented by the number of bytes that were put on the wire. This count does not include preamble/SFD.

6.2.17. TBCA (Ask a Question)

Name: TBCA
Offset: 0x0EC
Reset: 0x0
Property: Read-only

TBCA- Transmit Broadcast Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT BROADCAST PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT BROADCAST PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT BROADCAST PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT BROADCAST PACKET COUNTER [17:0] Incremented for each Broadcast frame transmitted (excluding Multicast frames).

6.2.18. RXCF (Ask a Question)

Name: RXCF
Offset: 0x0B0
Reset: 0x0
Property: Read-only

RXCF - Receive Control Frame Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RECEIVE CONTROL FRAME PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	RECEIVE CONTROL FRAME PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE CONTROL FRAME PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – RECEIVE CONTROL FRAME PACKET COUNTER [17:0] Incremented for each MAC Control frame received (PAUSE and Unsupported).

6.2.19. RUND (Ask a Question)

Name: RUND
Offset: 0x0CC
Reset: 0x0
Property: Read-only

RUND - Receive Undersize Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE UNDERSIZE PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE UNDERSIZE PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE UNDERSIZE PACKET COUNTER [11:0] Incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors.

6.2.20. RPKT (Ask a Question)

Name: RPKT
Offset: 0x0A0
Reset: 0x0
Property: Read-only

RPKT- Receive Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RECEIVE PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	RECEIVE PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – RECEIVE PACKET COUNTER [17:0] Incremented for each frame received packet (including bad packets, all Unicast, Broadcast, and Multicast packets).

6.2.21. ROVR (Ask a Question)

Name: ROVR
Offset: 0x0D0
Reset: 0x0
Property: Read-only

ROVR - Receive Oversize Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE OVERSIZE PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE OVERSIZE PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE OVERSIZE PACKET COUNTER [11:0] Incremented each time a frame is received which exceeded 1518 (non VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors.

6.2.22. RMCA (Ask a Question)

Name: RMCA
Offset: 0x0A8
Reset: 0x0
Property: Read-only

RMCA - Receive Multicast Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RECEIVE MULTICAST PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	RECEIVE MULTICAST PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE MULTICAST PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – RECEIVE MULTICAST PACKET COUNTER [17:0] Incremented for each Multicast good frame of lengths smaller than 1518 (non VLAN) or 1522 (VLAN) excluding Broadcast frames. This does not look at range/length errors.

6.2.23. RJBR (Ask a Question)

Name: RJBR
Offset: 0x0D8
Reset: 0x0
Property: Read-only

RJBR - Receive Jabber Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE JABBER COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE JABBER COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE JABBER COUNTER [11:0] Incremented for frames received which exceed 1518 (non VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, includes alignment errors.

6.2.24. RFRG (Ask a Question)

Name: RFRG
Offset: 0x0D4
Reset: 0x0
Property: Read-only

RFRG -Receive Fragments Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE FRAGMENTS COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE FRAGMENTS COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE FRAGMENTS COUNTER [11:0] Incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS.

6.2.25. RFLR (Ask a Question)

Name: RFLR
Offset: 0x0C0
Reset: 0x0
Property: Read-only

RFLR - Receive Frame Length Error Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RECEIVE FRAME LENGTH ERROR COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE FRAME LENGTH ERROR COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RECEIVE FRAME LENGTH ERROR COUNTER [15:0] Incremented for each frame received in which the 802.3 length field did not match the number of data bytes actually received (46-1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value.

6.2.26. RFCS (Ask a Question)

Name: RFCS
Offset: 0x0A4
Reset: 0x0
Property: Read-only

RFCS - Receive FCS Error Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RECEIVE FCS ERROR COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	RECEIVE FCS ERROR COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE FCS ERROR COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – RECEIVE FCS ERROR COUNTER [17:0] Incremented for each frame received that has an integral 64 to 1518 length and contains a Frame Check Sequence error.

6.2.27. RBYT (Ask a Question)

Name: RBYT
Offset: 0x09C
Reset: 0x0
Property: Read-only

RBYT - Receive Byte Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RECEIVE BYTE COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	RECEIVE BYTE COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE BYTE COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – RECEIVE BYTE COUNTER [17:0] The Statistic Counter register is incremented by the byte count of all frames received, including those in bad packets, excluding framing bits but including FCS bytes.

6.2.28. RBCA (Ask a Question)

Name: RBCA
Offset: 0x0AC
Reset: 0x0
Property: Read-only

RBCA - Receive Broadcast Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RECEIVE BROADCAST PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	RECEIVE BROADCAST PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE BROADCAST PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – RECEIVE BROADCAST PACKET COUNTER [17:0] Incremented for each Broadcast good frame of lengths smaller than 1518 (non VLAN) or 1522 (VLAN) excluding Multicast frames. This does not look at range/length errors.

6.2.29. RALN (Ask a Question)

Name: RALN
Offset: 0x0BC
Reset: 0x0
Property: Read-only

RALN - Receive Alignment Error Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE ALIGNMENT ERROR COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE ALIGNMENT ERROR COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE ALIGNMENT ERROR COUNTER [11:0] Incremented for each received frame from 64 to 1518 which contains an invalid FCS and is not an integral number of bytes.

6.2.30. MIIMgmt_Status (Ask a Question)

Name: MIIMgmt_Status
Offset: 0x030
Reset: 0x0
Property: Read-only

MDIO Mgmt: Status

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	MDIO MGMT STATUS (PHY STATUS)[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MDIO MGMT STATUS (PHY STATUS)[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – MDIO MGMT STATUS (PHY STATUS)[15:0] Following an MDIO Mgmt Read Cycle, the 16 bit data can be read from this location.

6.2.31. MIIMgmt_Indicators (Ask a Question)

Name: MIIMgmt_Indicators
Offset: 0x034
Reset: 0x0
Property: Read-only

MDIO Mgmt: Indicators

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						NOT VALID	SCANNING	BUSY
Access						R	R	R
Reset						0	0	0

Bit 2 – NOT VALID When 1 is returned indicates MDIO Mgmt Read cycle has not completed and the Read Data is not yet valid.

Bit 1 – SCANNING When 1 is returned-indicates a scan operation (continuous MDIO Mgmt Read cycles) is in progress.

Bit 0 – BUSY When 1 is returned-indicates MDIO Mgmt block is currently performing an MDIO Mgmt Read or Write cycle.

6.2.32. MIIMgmt_Control (Ask a Question)

Name: MIIMgmt_Control
Offset: 0x02C
Reset: 0x0
Property: Write-only

MDIO Mgmt: Control

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	MDIO MGMT CONTROL (PHY CONTROL)[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MDIO MGMT CONTROL (PHY CONTROL)[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – MDIO MGMT CONTROL (PHY CONTROL)[15:0] When written, an MDIO Mgmt write cycle is performed using the 16-bit data and the preconfigured PHY and Register addresses from the MDIO Mgmt Address Register.

6.2.33. MIIMgmt_Configuration (Ask a Question)

Name: MIIMgmt_Configuration
Offset: 0x020
Reset: 0x0
Property: Read/Write

MDIO Mgmt: Configuration

Bit	31	30	29	28	27	26	25	24
	RESET MDIO MGMT							
Access	R/W							
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			SCAN AUTO INCREMENT	PREAMBLE SUPPRESSION		MGMT CLOCK SELECT[2:0]		
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bit 31 – RESET MDIO MGMT Setting this bit resets MDIO Mgmt. Clearing this bit allows MDIO Mgmt to perform Mgmt read or write cycles as requested via the APB target interface.

Bit 5 – SCAN AUTO INCREMENT Setting this bit causes MDIO Mgmt to continually read from a set of PHYs of contiguous address space. The starting address of the PHY is specified by the content of the PHY address field recorded in the MDIO Mgmt Address register. The next PHY to be read is PHY address + 1. The last PHY to be queried in this read sequence is the one residing at address 0x31, after which the read sequence returns to the PHY specified by the PHY address field.

Bit 4 – PREAMBLE SUPPRESSION Setting this bit causes MDIO Mgmt to suppress preamble generation and reduce the Mgmt cycle from 64 clocks to 32 clocks. This is in accordance with IEEE 802.3/22.2.4.4.2. Clearing this bit causes MDIO Mgmt to perform Mgmt read/write cycles with the 64 clocks of preamble.

Bits 2:0 – MGMT CLOCK SELECT[2:0]

Value	Description
3b000/3b001	Source clock divided by 4
3b010	Source clock divided by 6
3b011	Source clock divided by 8
3b100	Source clock divided by 10
3b101	Source clock divided by 14
3b110	Source clock divided by 20
3b111	Source clock divided by 28

6.2.34. MIIMgmt_Command (Ask a Question)

Name: MIIMgmt_Command
Offset: 0x024
Reset: 0x0
Property: Read/Write

MDIO Mgmt: Command

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							SCAN CYCLE	READ CYCLE
Access							R/W	R/W
Reset							0	0

Bit 1 – SCAN CYCLE This bit causes MDIO Mgmt to perform Read cycles continuously. This is useful for monitoring Link Fail.

Bit 0 – READ CYCLE This bit causes MDIO Mgmt to perform a single Read cycle. The Read data is returned in MDIO Mgmt STATUS Register.

6.2.35. MIIMgmt_Address (Ask a Question)

Name: MIIMgmt_Address
Offset: 0x028
Reset: 0x0
Property: Read/Write

MDIO Mgmt: Address

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				PHY ADDRESS[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				REGISTER ADDRESS[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – PHY ADDRESS[4:0] This field represents the 5 bit PHY Address field used in Mgmt cycles. Up to 31 PHYs can be addressed.

Bits 4:0 – REGISTER ADDRESS[4:0] This field represents the 5 bit Register Address field of Mgmt cycles.

6.2.36. Maximum_Frame_Length (Ask a Question)

Name: Maximum_Frame_Length
Offset: 0x010
Reset: 0x7d0
Property: Read/Write

Maximum Frame Length

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	MAXIMUM FRAME LENGTH[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	MAXIMUM FRAME LENGTH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	0	1	0	0	0	0

Bits 15:0 – MAXIMUM FRAME LENGTH[15:0] This programmable field sets the maximum frame size in both the transmit and receive directions.

6.2.37. MACConfiguration1 (Ask a Question)

Name: MACConfiguration1
Offset: 0x000
Reset: 0x80000000
Property: NEEDS_CLEANUP

MAC Configuration # 1

Bit	31	30	29	28	27	26	25	24
	SOFT RESET							
Access	R/W							
Reset	1							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					SYNCHRONIZED RECEIVE ENABLE	RECEIVE ENABLE	SYNCHRONIZED TRANSMIT ENABLE	TRANSMIT ENABLE
Access					R	R/W	R	R/W
Reset					0	0	0	0

Bit 31 – SOFT RESET Setting this bit puts all modules within the MAC in reset except the APB target interface.

Bit 3 – SYNCHRONIZED RECEIVE ENABLE Receive Enable synchronized to the receive stream.

Bit 2 – RECEIVE ENABLE Setting this bit allows the MAC to receive frames from the PHY. Clearing this bit prevents the reception of frames.

Bit 1 – SYNCHRONIZED TRANSMIT ENABLE Transmit Enable synchronized to the transmit stream.

Bit 0 – TRANSMIT ENABLE Setting this bit allows the MAC to transmit frames from the system. Clearing this bit prevents the transmission of frames.

6.2.38. MACConfiguration2 (Ask a Question)

Name: MACConfiguration2
Offset: 0x004
Reset: 0x7200
Property: Read/Write

MAC Configuration # 2

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PREAMBLE LENGTH[3:0]						INTERFACE MODE[1:0]	
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	1	1	1			1	0

Bit	7	6	5	4	3	2	1	0
			HUGE FRAME ENABLE	LENGTH FIELD CHECKING		PAD/CRC ENABLE	CRC ENABLE	FULL-DUPLEX
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 15:12 – PREAMBLE LENGTH[3:0] This field determines the length of the preamble field of the packet, in bytes. Minimum value supported for this field is 0x3.

Bits 9:8 – INTERFACE MODE[1:0]

Value	Description
2b00	Reserved.
2b01	Reserved.
2b10	MAC Tx/Rx represents GMII 1000Mbps interface (Byte Mode).
2b11	Reserved.

Bit 5 – HUGE FRAME ENABLE Setting this bit allows frames longer than the MAXIMUM FRAME LENGTH to be transmitted and received. Clear this bit to have the MAC limit the length of frames at the MAXIMUM FRAMELENGTH value. (Maximum Frame Length is set in separate Maximum Frame Length register.)

Bit 4 – LENGTH FIELD CHECKING Setting this bit causes the MAC to check the frame length field to ensure it matches the actual data field length. Clear this bit if no length field checking is desired.

Bit 2 – PAD/CRC ENABLE Set this bit to have the MAC pad all short frames and append a CRC to every frame whether or not padding was required. Clear this bit if frames presented to the MAC have a valid length and contain a CRC.

Bit 1 – CRC ENABLE Set this bit to have the MAC append a CRC to all frames. Clear this bit if frames presented to the MAC have a valid length and contain a valid CRC. If the PAD/CRC ENABLE Configuration bit or the per packet PAD/CRC ENABLE is set, CRC ENABLE is ignored.

Bit 0 – FULL-DUPLEX Setting this bit configures the MAC to operate in full duplex mode. Clearing this bit configures the MAC to operate in half duplex mode only.

6.2.39. IPG (Ask a Question)

Name: IPG
Offset: 0x008
Reset: 0x6005060
Property: Read/Write

IPG / IFG

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	NON_BACK_TO_BACK INTER_PACKET_GAP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MINIMUM IFG ENFORCEMENT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		BACK_TO_BACK INTER_PACKET_GAP[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	0	0	0	0	0

Bits 23:16 – NON_BACK_TO_BACK INTER_PACKET_GAP[7:0] This programmable field represents the Non-Back-to-Back Inter-Packet-Gap in bit times. Default is 0x60 (96d), which represents the minimum IPG of 96 bits

Bits 15:8 – MINIMUM IFG ENFORCEMENT[7:0] Default 0x50. This programmable field represents the minimum size of IFG to enforce between frames(expressed in bit times). A frame whose IFG is less than that programmed is dropped. The default setting of 0x50 (80d) represents half of the nominal minimum IFG which is 160 bits.

Bits 6:0 – BACK_TO_BACK INTER_PACKET_GAP[6:0] Default 0x60. This programmable field represents the IPG between Back-to-Back packets (expressed in bit times). This is the IPG parameter used exclusively in full-duplex mode when two transmit packets are sent back-to-back. Set this field to the desired number of bits. The default setting of 0x60 (96d) represents the minimum IPG of 96 bits. Minimum value supported for this field is 0x28 (40d).

6.2.40. Interface_Status (Ask a Question)

Name: Interface_Status
Offset: 0x03C
Reset: 0x0
Property: Read-only

Interface Status

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							EXCESS DEFER	
Access							R	
Reset							0	

Bit	7	6	5	4	3	2	1	0
					LINK FAIL			
Access					R			
Reset					0			

Bit 9 – EXCESS DEFER This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high. Excessive Deferred is a condition when the MAC has deferred sending a packet for a time longer than the length of two maximum length frames.

Bit 3 – LINK FAIL When read as a 1, the MDIO management module has read the PHY link fail register to be 1. When read as a 0, the MDIO management module has read the PHY link fail register to be 0. Note that for asynchronous host accesses, this bit must be read at least once every scan read cycle of the PHY.

6.2.41. Interface_Control (Ask a Question)

Name: Interface_Control
Offset: 0x038
Reset: 0x0
Property: Read/Write

Interface Control

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				STATS COUNTERS : AUTO CLEAR COUNTERS ON READ	STATS COUNTERS : CLEAR ALL COUNTERS	STATS COUNTERS : MODULE ENABLE		
Access				R/W	R/W	R/W		
Reset				0	0	0		

Bit 4 – STATS COUNTERS : AUTO CLEAR COUNTERS ON READ Setting this bit enables auto-clear-on-read feature for all the counters.

Bit 3 – STATS COUNTERS : CLEAR ALL COUNTERS Setting this bit clears all the statistics counters.

Bit 2 – STATS COUNTERS : MODULE ENABLE Setting this bit enables statistics counter module.

6.2.42. Framefiltercontrols (Ask a Question)

Name: Framefiltercontrols
Offset: 0x1C0
Reset: 0x3f
Property: Read/Write

Frame filter controls

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			FRAME FILTER CONTROLS[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 5:0 – FRAME FILTER CONTROLS[5:0]

Value	Description
[5]	Reserved
[4]	Reserved
[3]	Promiscuous mode, allow all the frames to pass
[2]	Reserved
[1]	Pass all multicast frames
[0]	Pass all broadcast frames

7. Firmware Support (Ask a Question)

The TSN IP exposes configuration registers and must be configured through register R/W to support the following TSN specifications:

- 802.1Qbv – Time Aware Shaper
- 802.1Qav – Credit Based Shaper
- 802.1CB – Frame Replication and Elimination
- 802.1Qbu – Frame Preemption
- 802.1Qci – Per Stream Filtering and Policing

7.1. Configuring 802.1Qbv (Time Aware Shaper) (Ask a Question)

The TAS allows for precise control of time-based transmission gating on the transmit (Tx) side, as specified by IEEE 802.1Qbv. It divides time into fixed gate control lists, opening or closing queues to ensure low-latency traffic meets deadlines while protecting against interference. This feature supports scheduled traffic in TSN, which is essential for applications requiring microsecond-level determinism.

The following are the configurations for the TAS:

- Base time (reference time for TAS)
- Eight queues, where each queue has two Stream IDs
- Cycle time (one Iteration time for Shaping)
- Gate Control list (open or close to control traffic flow from respective Queue)
- Stream ID configuration: For each Stream ID, configure Dst MAC, VLAN-ID, and PCP.

Queue and Stream Configuration: The system supports eight queues (Queue 0–7), which are typically mapped to different priority levels. Each queue contains two Stream IDs (Stream ID 0 and Stream ID 1), resulting in a total of 16 configurable streams. The following table lists the required parameters for each Stream ID.

Table 7-1. Parameters for Stream ID

Parameter	Description	Example Value	Size
Dst MAC	Destination MAC address filter	00:11:22:33:44:55	6 bytes
VLAN-ID	802.1Q VLAN tag identifier	100	12 bits (0-4095)
PCP	Priority Code Point (VLAN priority)	5	3 bits (0-7)

Software disables the gate control and priority queues with a falling edge to the Config Valid bit. Once disabled, enable all or a few priority queues. Configure a gate control list of maximum 32 entries which controls the scheduling of priority queues. It is mandatory to set the cycle time to the sum of the time intervals for all gate control list entries. After setting these configurations, enable the priority queues and gates, followed by a rising edge on the Config Valid bit.

The following table lists the configuration and registers for configuring 802.1Qbv.

Table 7-2. Configuration and Registers

SNO	Configuration	Registers
1	Base Time	• Base Time Low Register • Base Time High Register 0 • Base Time High Register 1 **Note:** For more information related to Base Time Registers, see Base Time Low Register, Base Time High Register0, and Base Time High Register1 sections.

Table 7-2. Configuration and Registers (continued)

SNO	Configuration	Registers
2	Cycle Time	Scheduler Cycle Time Register **Note:** For more information, see Scheduler Cycle Time section.
3	Gate Control List	• Gate Control List Register • Scheduler Gate States Register • Scheduler Control List Length Register • Scheduler Control List [x] Entry Register (x: 0 to 32) **Note:** For more information related to Gate Control List Registers and Scheduler Control List Registers, see Gate State Control, Scheduler Control List Length, and Gate Control List0 Register sections.
4	Stream ID	• STREAM ID1_0 Queue 0 **Note:** For more information, see SID1_0_Q0 section. • STREAM ID1_1 Queue 0 **Note:** For more information related, see SID1_1_Q0 section.

7.2. Configuring 802.1Qav (Credit-Based Shaper) (Ask a Question)

The CBS manages bursty traffic on the Tx side, as specified by IEEE 802.1Qav, also known as Forwarding and Queuing for Time-Sensitive Streams (FQTSS). CBS assigns credits to queues, allowing proportional bandwidth allocation. Idle credits accumulate to allow bursts, while excess credits are reduced at a specific rate to prevent lower-priority traffic from being starved. In TSN, it complements TAS for bandwidth efficiency in mixed traffic scenarios.

Table 7-3. CBS Registers per Queue

Queue	Enable/Disable Register	Increment Value	Decrement Value	Min Credit	Max Credit
Queue 0	Enable bit for CBS Queue 0 **Note:** For more information related to CBS Control Register, see CBS_CTRL section.	Increment counted when the frame has to wait for the Queue 0 **Note:** For more information related to Credit Register Queue 0, see CBS_Q0 section.	Decrement counted when the frame is in sending phase for Queue 0 **Note:** For more information related to Credit Register Queue 0, see CBS_Q0 section.	Credit Minimum value for Queue 0 **Note:** For more information related to Credit Minimum Register Queue 0, see CBS_Min_Q0 section.	Credit Maximum value for Queue 0 **Note:** For more information related to Credit Maximum Register Queue 0, see CBS_Max_Q0 section.
Queue 1	Enable bit for CBS Queue **Note:** For more information related to CBS Control Register, see CBS_CTRL section.	Increment counted when the frame has to wait for the Queue 1 **Note:** For more information related to Credit Register Queue 1, see CBS_Q1 section.	Decrement counted when the frame is in sending phase for Queue 1 **Note:** For more information related to Credit Register Queue 1, see CBS_Q1 section.	Credit Minimum value for Queue 1 **Note:** For more information related to Credit Minimum Register Queue 1, see CBS_Min_Q1 section.	Credit Maximum value for Queue 1 **Note:** For more information related to Credit Maximum Register Queue 1, see CBS_Max_Q1 section.

Note: Decrement and Min credit are considered as negative by the CoreTSN IP. So, the user has to write the positive value. For example, value written 30 is considered as -30.

7.3. Configuring 802.1CB (Frame Replication and Elimination for Reliability) (Ask a Question)

Frame Replication and Elimination for Reliability (FRER), as specified by IEEE 802.1CB, ensures zero-downtime redundancy for both Tx and Rx paths. During transmission, frames are replicated across multiple paths. During reception, duplicates are eliminated using sequence numbers and Stream IDs, ensuring delivery despite link failures. TSN extends this for seamless reliability in converged networks. The software must configure the FRER enable/disable setting using the FRER control register. Additionally, frame replication can be enabled or disabled for each Stream ID individually.

Notes:

- For more information related to FRER Control/Status Register, see the FRER_PSFP Control section.
- For more information related to FRER Status Register for STREAM ID1_1 Queue 0, see the SID1_1_Q0 section on egress traffic replication.

7.4. Configuring 802.1Qbu (Frame Preemption) (Ask a Question)

Frame Preemption (IEEE 802.1Qbu/802.3br) allows high-priority frames to interrupt (express) and resume low-priority (preemptable) frames on Tx or Rx. This minimizes latency blocking without full scheduling, using hold or release mechanisms. In TSN, it integrates with shaping for hybrid urgency handling in real-time systems.

The software must configure the fragmentation size. There are four supported fragmentation sizes: 60 bytes, 124 bytes, 188 bytes, and 252 bytes. These are configured in the Preemption Control Register. Preemption can be enabled or disabled.

These values must be configured accordingly, where the range from 0 to 3 represents the minimum frame size for preemption: 0–60 bytes (default), 1–124 bytes, 2–188 bytes, and 3–252 bytes.
Note: For more information related to Pre-emption Control Register, see prempt_cntrl section.

7.5. Configuring 802.1Qci (Per Stream Filtering and Policing) (Ask a Question)

Per-Stream Filtering and Policing (PSFP) on Rx path, as specified by IEEE 802.1Qci, enforces stream-specific rules such as rate limiting (CIR/EIR), maximum frame sizes, and cumulative intervals.

The software needs configure the source MAC address and VLAN ID with independent enable/disable control through a mask register per stream ID. For information related to Mask Register (PSFP_PORT0_STREAMID1_CTRL), see PSFP_SID1_P0_CTRL section and for information related to Vlan ID and Source MAC Address, see PSFP_SID1_P0_0 section.

The filtering feature can be enabled or disabled using a control register. For more information related to RX PORT0 STREAMID1 Flow metering/Policing Control Register, see PSFP_SID1_P0_FM_CTRL section.

The maximum SDU size can be configured per stream ID. For more information related to SDU size, see the PSFP_PORT0_STREAMID1 Max Packet Size Register in PSFP_SID1_P0_MAX section.

Additionally, if enabled through a control register, all subsequent frames will be dropped if any frame exceeds the configured maximum SDU size once. The flow metering feature can be enabled or disabled using a control register. For more information related to RX PORT0 STREAMID1 Flow metering/Policing Control Register, see PSFP_SID1_P0_FM_CTRL section.

The software must configure the following flow metering parameters:

- Committed Burst Size (CBS): The burst allowance (in bytes or octets) for committed traffic. For more information related RX PORT0 STREAMID1 Flow metering/Policing Register, see PSFP_SID1_P0_FM section.
- Committed Information Rate (CIR): The maximum rate (in bits per second) for committed traffic. For more information related RX PORT0 STREAMID1 Flow metering/Policing Register 1, see PSFP_SID1_P0_FM_1 section. For example, 7000000 is configured in the CIR register for the rate of 7 Mpbs.
- Excess Burst Size (EBS): The burst allowance (in bytes or octets) for excess traffic. For more information related RX RX PORT0 STREAMID1 Flow metering/Policing Register, see PSFP_SID1_P0_FM section.
- Excess Information Rate (EIR): The maximum rate (in bits per second) for excess traffic beyond the CIR. For more information related RX PORT0 STREAMID1 Flow metering/Policing Register 2, see PSFP_SID1_P0_FM_2 section.

Additionally, the Dropping Yellow Frames feature can be enabled or disabled using a control register. For more information about RX PORT0 STREAMID1 Flow metering/Policing Control Register, see PSFP_SID1_P0_FM_CTRL section.

7.6. Statistics (Generic: Tx/PSFP: Rx) (Ask a Question)

The statistics collection mechanism tracks various performance metrics:

- Generic Tx stats include frame counts, errors, and rates across queues.
- PSFP Rx stats (IEEE 802.1Qci) monitor per-stream filtering results, such as dropped packets and policed traffic rates.

These counters help with diagnostics, QoS verification, and troubleshooting in TSN deployments.

Software can read the statistics registers to collect and display these metrics. For information about dropped packets, see STREAMID1 Q0 Packets Drop Count Register in the SID1_Q0_PKT_DRP section. For information about packets sent through Stream ID queues, see STREAMID1 Q0 Packets Sent Count Register register in the SID1_Q0_PKT_SENT section.

Preemption and Express Frame Statistics:

- For the number of preempted frames (packets) discarded at Port0, see Preempt Packet drop count Register.
- For the number of preempted frames (packets) received at Port0, see Preempt Packet Receive count Register.
- For the number of express frames (packets) discarded at Port0, see Replicated Express Packet count Register.
- For the number of express frames (packets) received at Port0, see Express Packet Receive count Register.
- For the number of preempted frames (packets) discarded at Port1, see Replicated Preempt Packet count Register.
- For the number of preempted frames (packets) received at Port1, see Preempt Packet Receive count Register.
- For the number of express frames (packets) discarded at Port1, see Replicated Express Packet count Register.
- For the number of express frames (packets) received at Port1, see Express Packet Receive count Register.

PSFP Stream Statistics:

- For the number of RX Port0 PSFP packet received for STREAMID1, see Filtering/Policing SID1 Count Register (Port0).
- For the number of RX Port0 PSFP packet drop for STREAMID1, see Filtering Drop Count Register SID1 (Port0).

8. Testing of CoreTSN (Ask a Question)

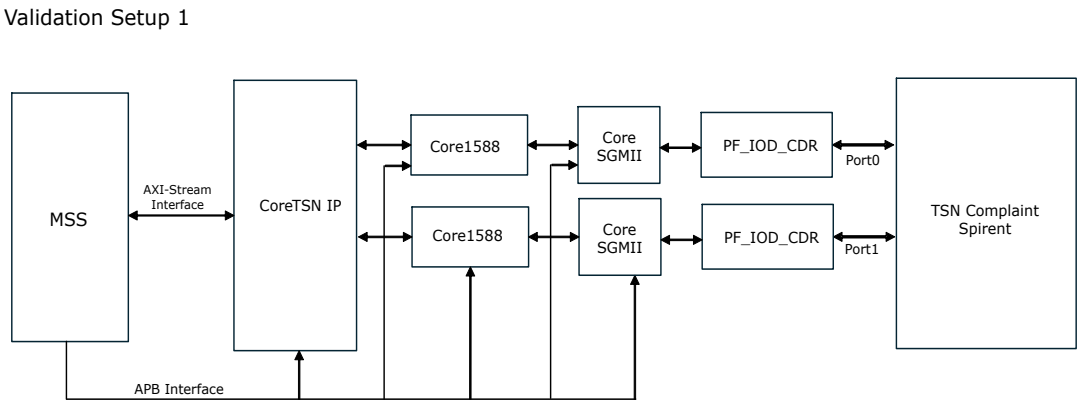
The CoreTSN IP is validated for its features using the Spirent Model N12U. Spirent can generate and analyze express, fragmented preemption, and replicated RTAG frames, enabling effective evaluation and validation of TSN features. Validation setup 1 is used for testing Time Aware Shaper, Credit-based Shaper, and Frame preemption. Validation setup 2 is used for testing FRER and PSFP features.

Validation Setup 1

The following is a step-by-step explanation of validation setup 1:

- PF_IOD_CDR is used for parallel-to-serial and serial-to-parallel data conversion at a rate of 1250 Mbps, with a data width of 10 bits at 125 MHz. The data and clock recovery block is integrated within the PF_IOD_CDR module.
- The Core1588 captures the PTP timestamp value.
- The CoreSGMII converts 8-bit to 10-bit parallel data, and its output is fed to the PF_IOD_CDR module.
- Spirent ports are connected to the 1G RJ45 ports on the TSN Daughter card.
- The MSS serves as the primary processor for configuring all integrated IP blocks, TSN specific registers, and setting GCL configuration registers for real-time modifications. It also generates both express and preemption traffic.
- The CoreTSN IP transmits the traffic as per the configuration, which is analyzed at the Spirent. The Spirent Test Center IQ wizard is used for analyzing preempted and express traffic received.

Figure 8-1. Validation Setup 1



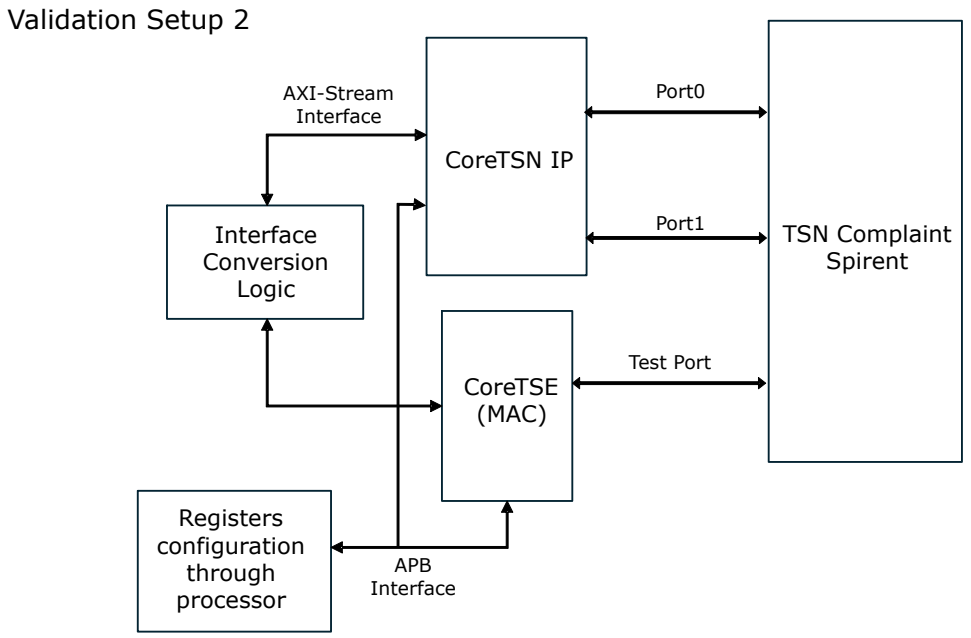
Validation Setup 2

The following is a step-by-step explanation of validation setup 2:

- A multiport test setup is used for Frame Replication and Elimination (FRER) and PSFP feature validation. An additional port is used as the test port and connects to a Spirent test system.
- For FRER elimination, the Spirent sends the replicated packets on the design ports (port0 and port1). The CoreTSN IP eliminates the duplicate packets, removes the RTAG header, and provides the resultant packet on the system side interface (AXI-Stream). These packets are routed to the test port and are analyzed at the Spirent with respect to the sent traffic.
- For FRER replication, Spirent sends traffic on the test port and expects the replicated (RTAG) packets on the design ports. The CoreTSN IP inserts the RTAG header for the received packets from the test port, duplicates the packets, and transmits on port0 and port1. These frames are analyzed at the Spirent with respect to the frames sent on the test port.
- For the various PSFP configurations, the data is generated by the Spirent. The CoreTSN IP performs the filtering and policing on the incoming data streams according to the configured

data rate and drops the packets exceeding the bandwidth allowed. The processed packets are sent through the test port and are analyzed at the Spirent.

Figure 8-2. Validation Setup 2



9. Additional References (Ask a Question)

This section provides a list for additional information. For updates and additional information about the software, devices, and hardware, visit the **Intellectual Property** pages on the Microchip FPGA Intellectual Property Cores.

The reference documents (Third-party documents) mentioned in this document are listed as follows:

- IEEE 802.1Qbv (Time Aware Shaper): IEEE Xplore (search “802.1Qbv”)
  ieeexplore.ieee.org/ (search: 802.1Qbv)
- IEEE 802.1Qbu (Frame Preemption): IEEE Xplore (search “802.1Qbu”)
  ieeexplore.ieee.org/ (search 802.1Qbu)
- IEEE 802.1Qci (Per-Stream Filtering and Policing): IEEE Xplore (search “802.1Qci”)
  ieeexplore.ieee.org/ (search: 802.1Qci)
- IEEE 802.3 (Ethernet includes clauses/sections; your “section2/section3” are typically parts/clauses of 802.3): IEEE Xplore (search “IEEE Std 802.3-2012”)
  ieeexplore.ieee.org/ (search: 802.3-2012)
- AMBA® AXI4-Stream Protocol Specification (AXI-Stream): Arm® developer documentation (AMBA specifications page)
  developer.arm.com/documentation/ (search: AMBA AXI4-Stream protocol specification)
  Alternate landing page often used: developer.arm.com/Architectures/AMBA

Important: For more information about the following documents, contact Microchip Technical support team.

9.1. Known Issues and Workarounds (Ask a Question)

There are no known issues and workarounds for CoreTSN.

9.2. Ordering Codes (Ask a Question)

Order CoreTSN through your local Microchip Sales representative. Use the following number scheme: CoreTSN-XX, where XX corresponds to the options listed in the following table.

Table 9-1. Ordering Codes

XX	Description
OM	Obfuscated RTL Node Locked License
OMFL	Obfuscated RTL Floating License

10. Glossary (Ask a Question)

Following are the list of terms and definitions used in the document.

Table 10-1. Terms and Definitions

Term	Definition
APB	AMBA® Peripheral Bus
AXI	Advanced eXtensible Interface
CBS	Credit Based Shaper
CDC	Clock Domain Crossing
EMAC	Express MAC
FCS	Frame Check Sequence
FIFO	First In First Out
FRER	Frame Replication and Elimination for Reliability
GCL	Gate Control List
GMII	Gigabit Media Independent Interface
I/F	Interface
MAC	Media Access Control
MDIO	Management Data Input/Output
MMS	Mac Merge SubLayer
PCP	Priority Code Point
PKT	Packet
PMAC	Preemption MAC
PSFP	Per Stream Filtering and Policing
PTP	Precision Time Protocol
RX	Receive
TX	Transmit
TAS	Time Aware Shaper
TSN	Time Sensitive Network
VLAN	Virtual Local Area Network

11. Device Utilization and Performance (Ask a Question)

Device utilization and performance data is provided for the supported device families. The AXI_S0_CLK, AXI_S1_CLK, PCLK, MAC_TX_CLK, MAC_RX_CLK, and MAC_SYS_CLK performance is above 125 MHz. The information presented in the table is only indicative. The overall device utilization and core performance are dependent on the system.

Table 11-1. Device Utilization

Family	Device	Utilization			Performance (MHz)			
		DFF	LUT	LSRAM (20K)	AXI_S0_CLK	AXI_S1_CLK	MAC_TX_CLK	MAC_RX_CLK
PolarFire®	MPF300T	38887	54223	5040	128	127	127	127
PolarFire SoC	MPFS250TS	38887	54223	5040	127	127	127	127

Important:

- The data in the preceding are achieved using Libero SoC v2025.2.
- The data in the preceding table is achieved using default synthesis and layout settings.

12. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Table 12-1. Revision History

Revision	Date	Description
D	06/2026	The following is the list of changes in revision C of the document: • Added Table 3-1 in the Configuration Parameters section. • Added Configuring the CoreTSN section.
C	04/2026	The following is the list of changes in revision C of the document: • Updated information related to CoreTSN in the Introduction section. • Updated Figure 2-1 in the Functional Description section • Updated Figure 5-3 in the System Integration section. • Updated Figure 5-4 in the Verification section. • Added Table 7-1 and updated register references in Table 7-2 in the Configuring 802.1Qbv (Time Aware Shaper) section. • Added Configuring 802.1Qav (Credit-Based Shaper), Configuring 802.1CB (Frame Replication and Elimination for Reliability), and Statistics (Generic: Tx/PSFP: Rx) sections. • Updated the Configuring 802.1Qbu (Frame Preemption) section • Updated the Testing of CoreTSN section with validation setup information. • Added weblinks in the Additional References section.
B	07/2024	Updated PADDR bit address and MACConfiguration1 in Register Map and Descriptions section
A	07/2024	Initial release

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