Introduction (Ask a Question)

The CoreTSE provides 10/100/1000 Mbps Ethernet Media Access Controller (MAC) with a Gigabit Media Independent Interface (G/MII) or Serial Gigabit Media Independent Interface (SGMII) Ten Bit Interface (TBI) to support 1000BASE-T and 1000BASE-X.

The CoreTSE has the following major interfaces:

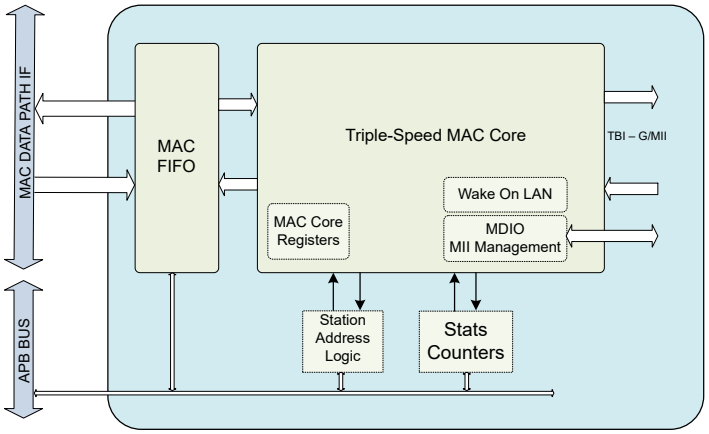
- G/MII or SGMII TBI physical layer (PHY) interface connects to Ethernet PHY
- Management Data Input or Output (MDIO) interface to communicate with the MDIO Manageable Device (MMD) in the PHY
- MAC data path interface
- Advanced Peripheral Bus (APB) - Target interface for MAC configuration registers and status counters access

A triple speed MAC core is responsible for the main functionalities of CoreTSE which are listed as follows:

- Statistics gathering - Statistics information is gathered from the data transmitted and received over the Ethernet link.
- Station address functions - Station address (SAL) feature provides address filtering capability.

The following figure shows the block diagram of CoreTSE.

Figure 1. CoreTSE Block Diagram



Summary

Table 1. CoreTSE Characteristics

Core Version	This document applies to CoreTSE version 4.0

Supported Device Families	• PolarFire® SoC • PolarFire • RTG4™ • IGLOO® 2 • SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v11.7 or later releases
Licensing	CoreTSE is available in the following license versions: Evaluation, Obfuscated and RTL • **Evaluation**: Evaluation version is available for free and supports user testbench simulations and four hours of the functionality on silicon. • **Obfuscated**: Obfuscated version is license locked and supports user testbench simulations and unlimited functionality on silicon. • **RTL**: Complete encrypted RTL source code is provided for the core.
Installation Instructions	CoreTSE must be installed to the **IP Catalog** of Libero SoC automatically through the IP Catalog update function. Alternatively, CoreTSE could be manually downloaded from the catalog. Once the IP core is installed, it is configured, generated, and instantiated SmartDesign within for inclusion in the project.
Device Utilization and Performance	A summary of utilization and performance information for CoreTSE is listed in Device Utilization and Performance.

Table of Contents

1. Features (Ask a Question)

CoreTSE has the following features:

- 10/100/1000 Mbps Operation
- Full-duplex Support at 10/100/1000 Mbps
- Half-duplex Support at 10/100 Mbps
- Standard G/MII Interface
- MDIO Interface for PHY Register access
- SGMII Ten Bit Interface (TBI)
- Wake on LAN (WoL) with Magic Packet Detection
- Frame Statistics Counters
- Destination Address-Based Filtering

2. Functional Description (Ask a Question)

This section describes the functionality of the CoreTSE.

2.1. Triple Speed MAC (Ask a Question)

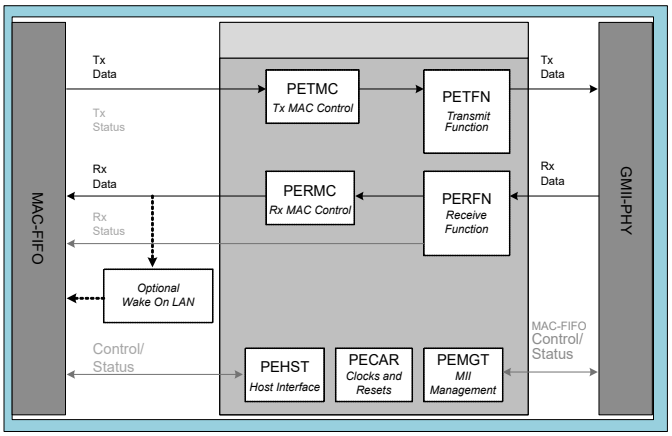
This core is a full-featured 10/100/1000 Mbps MAC with standard G/MII. The MAC has built in G/MII to TBI converter, which supports 1000 Mbps with TBI. The core is capable of full-duplex operation at 10, 100, or 1000 Mbps and of half duplex operation at 10 and 100 Mbps.

In half-duplex mode, the MAC adheres to the Carrier Sense Multiple Access/Collision Detect Access method as defined in IEEE® 802.3 and its several supplements including IEEE 802.3u. In full-duplex mode, the MAC follows IEEE 802.3x, which ignores both carrier and collisions. Following each packet transmission or abortion, a transmit statistics vector is used for statistics collection.

The external PHY device presents packets to the MAC. The MAC scans the preamble searching for the Start Frame Delimiter (SFD). When the SFD is found, the preamble and SFD are stripped and the frame is passed to the system. Following each frame reception, a Receive Statistics Vector (RSV) is used for frame filtering and statistics collection.

CoreTSE supports PAUSE control frames. This core also includes optional support for Wake-on-LAN (WoL) module. The WoL module detects both IEEE 802.3-compliant unicast frames with a destination address that matches the station address and packets that use AMD's Magic Packet™ Detection technology. The detection functionality can be enabled or disabled.

Figure 2-1. Triple Speed MAC Functional Block Diagram



2.2. PAUSE Flow Control (Ask a Question)

MAC transmit logic (MACTL) provides native support for PAUSE flow control frames. PAUSE frames are control frames (frames with 0x8808 as the Ether Type) with a particular DA (01-80-c2-00-00-01) and the Opcode 0x0001. The FIFO-logic automatically Request-to-Send a PAUSE frame by pulsing transmit-control-request (TCRQ) and provides the pause time value available on control-frame-register (CFPT [15:0]). Pause frame payload contains CFPT and Control Frame Extended Parameter (CFEP). Once a frame is received and detected as a control frame, MAC checks for the DA and the Opcode fields. If the DA is either the reserved multicast address used by PAUSE (01-80-c2-00-00-01) or the station's unique address, and the Opcode is 0x0001, then the control frame is considered to be a PAUSE Control frame.

When a PAUSE control frame is received:

- The MAC receive logic (MACRL) module indicates the MACTL to pause the stream of data frames and allows control frames transmission to the link partner. When either a PAUSE frame with a

zero-value pause time is received or the MACRL pause timer expires, MACTL is considered to be unpaused and normal data frames gets resumed.

- The pause time value is loaded into the PERMC pause timer. This pause timer is a 16-bit down counter that decrements every pause quanta (a speed-independent constant of 64 byte-times). Whenever the pause time counter is nonzero, the MAC is considered to be paused and no data frames are sent.

2.2.1. MAC Register Configuration for Pause Frames (Ask a Question)

To send the pause frames, the following registers must be configured:

Table 2-1. MAC Register Configuration for Pause Frames

Action	Configuration Setting	Description
Enable Pause Frame Transmission	MAC Configuration #1 (0x000)	Set Bit[4] to 1 to enable the MAC to generate and send Pause frames whenever necessary
Configure Pause Quanta	MAC-FIFO Configuration Register 1 (0x04C)	Program the bits [15:0] as per the required pause quanta value.
Configure FIFO Thresholds	MAC-FIFO Configuration Register 2 (0x050)	Set the required high and low watermark levels for the Receive FIFO.
Configure Full-duplex/Half-Duplex mode	MAC-FIFO Configuration Register 5 (0x05C)	Set bit [22] to '0' to operate in full-duplex mode (By default its set to 0).
Configure Pause Timer Value	Control Frame Parameter (0x018)	Program the bit[15:0] with the desired Pause timer value.
Configure Source Address (SA)	Program the below two registers to configure the Source Address: • Station Address Lower Register (0x040) • Station Address Higher Register (0x044)	Program these two registers with the Source Address

2.3. Jumbo Frame Support (Ask a Question)

The CoreTSE supports jumbo frames, which are frames that exceed the 1500-byte maximum of standard Ethernet frames. CoreTSE transmitter/receiver are configured in either store and forward or cut through mode. In the store and forward mode, transmitter/receiver buffer will not be read until the entire packet is stored into the buffer. In the cut through mode, transmitter/receiver buffer will be read as soon as the number of bytes threshold configured in "**MAC-FIFO Configuration Register 1 (0x04C)"** and "**MAC-FIFO Configuration Register 3 (0x054)"** are available in the receiver and transmitter buffer respectively. The following parameter/register configurations are recommended.

Parameter Configuration

CoreTSE transmitter/receiver buffers can be used in either store and forward mode or cut through mode. Packet Size parameter shall be configured to more than or equal to two times maximum jumbo frame size for the store and forward mode. For example, if maximum jumbo frame size is 9K bytes, then Packet Size should be selected to 32K bytes in the CoreTSE GUI configurator. Packet Size parameter can be configured to any value for cut through mode.

Registers Configuration

Following registers configuration is recommended when jumbo frame size is greater than 1500 bytes.

When CoreTSE transmitter/receiver buffer used in store and forward mode:

1. To configure CoreTSE receiver buffer in store and forward mode, **system receive for cut through threshold** of the**"MAC-FIFO Configuration Register 1 (0x04C)"** shall be programmed to maximum jumbo frame size.

2. To configure CoreTSE transmitter buffer in store and forward mode, **fabric transmit cut through threshold** of the "**MAC-FIFO Configuration Register 3 (0x054)"** shall beprogrammed to maximum jumbo frame size
3. To enable huge frame, **HUGE FRAME ENABLE** of the **"MAC Configuration #2 Register (0x004)"** shall be programmed to 1

When CoreTSE transmitter/receiver buffer used in cut through mode:

1. To configure CoreTSE receiver buffer in cut through mode, **system receive for cut through threshold** of the**"MAC-FIFO Configuration Register 1 (0x04C)"** shall be programmed to more than 4 and less than Packet Size parameter. It is recommended to program to 64 bytes.
2. To configure CoreTSE transmitter buffer in cut through mode, **fabric transmit cut through threshold** of the "**MAC-FIFO Configuration Register 3 (0x054)"** shall be programmed to more than 4 and less than half of the Packet Size parameter. It is recommended to program to 64 bytes.
3. To enable huge frame, **HUGE FRAME ENABLE** of the **"MAC Configuration #2 Register (0x004)"** shall be programmed to 1.

2.4. Inter-Frame-Gap (Ask a Question)

MACRL provides the capability to filter frames that have less than a certain inter-frame-gap. The standard states that the inter-frame-gap should be 160 bit-times. This includes 96 bits of inter packet gap (IPG), 56 bits of preamble and 8 bits of start frame delimiter (SFD). To protect downstream logic from over-running, MACRL can be programmed with a minimum inter frame gap (IFG) parameter. The second of two back-to-back frames to violate the minimum IFG is dropped.

2.5. Address Detect (Ask a Question)

MACRL scans the frame and determine its address type. The 48-bit programmed station address is compared to each receive frame's DA. When they match, the unicast address detect (UCAD) is asserted. If the broadcast address is detected, MACRL asserts broadcast address detect (BCAD). If a multicast address is detected, the MAC asserts multicast address detect (MCAD).

2.6. Hash Table Support (Ask a Question)

MACRL supports hash table with up to 128 entries. Seven bits of the Cyclic Redundancy Check (CRC) of the DA are used as the Hash Value (HASHV [6:0]).

2.7. Length Checking and Maximum Length Enforcement (Ask a Question)

MACRL can optionally compare the length field with the actual length of the data field portion of the frame. This is enabled through the MAC Configuration #2 register. MACRL first determines if the length/type field is a valid length. If so, it is compared with the data field length and any mismatches are updated to the receive statistics.

MACRL can limit the length of receive frames passed to the system. The maximum length is programmed through the Maximum Frame Length register. Frames which exceed this maximum are truncated.

2.8. Internal Loopback at G/MII (Ask a Question)

Asserting the internal loopback enable bit in MAC Configuration #1 register, enables MAC transmit output's looped back to the MAC receive inputs at G/MII interface.

2.9. WoL (Ask a Question)

The MAC-WoL is based on AMD's Magic Packet Detection technology.

The first step of the detection procedure is to scan the first twelve bytes of the frame, which contain Destination and Station addresses. Magic Packet detection is only carried out when the incoming frame's destination address matches the MAC's station address, or if the frame's destination address is a multicast or broadcast address.

After the first twelve bytes of the frame have matched, core searches for the Magic Packet technology's defined preamble of six continuous aligned bytes with all bits asserted (0xFFh). Following a valid Magic Packet preamble, core immediately expects 16 back-to-back repetitions of the six-byte MAC station address. Failure to achieve this exact pattern by a single byte at any time during the frame resets the circuitry back to the preamble search state.

After successful recognition of the Magic Packet payload or a successful compare of the MAC's station address with the incoming frame's destination address, the Interface STATUS Register (bit field Wake on Lane Detected) is asserted and status bit can only be cleared through assertion of the Wake on Lane Detected Clear bit field of Interface Control register.

2.10. MDIO Management (Ask a Question)

Control and status is provided to and from the PHY through the two-wire MDIO management interface described in IEEE802.3u Clause22.

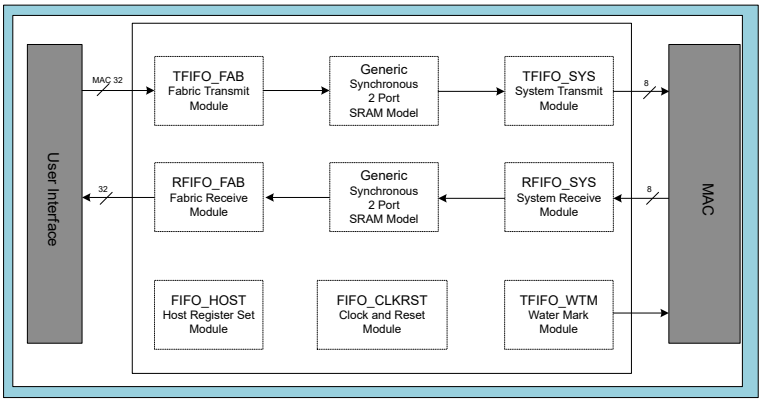
The MDIO write/read cycles are requested through the APB target. MAC performs a write cycle using the MDIO_PHYID, register address and 16-bit write data. MAC performs a read cycle using the MDIO_PHYID register address and updates the sixteen-bit read data into the MDIO Management STATUS Register, which can be read through APB target.

2.11. MAC FIFO (Ask a Question)

This core provides data queuing for increased throughput and sits between back-end, user-interface logic, and MAC core. The core provides clock-domain crossing, automatic pause frame handshaking, and graceful frame dropping.

The data is buffered between the system-interface and the MAC core by transmit and receive FIFOs. The FIFO size can be configured with PACKET_SIZE parameter.

Figure 2-2. MAC-FIFO Functional Block Diagram



Each RAM has additional associated control bits, which are additional to maximum frame data size.

Table 2-2. MAC-FIFO RAM Configurations

PACKET_SIZE Parameter (Bytes)	Transmit RAM		Receive RAM	
	RAM Size in Bits	Number of Address bits (TABITS)	RAM Size in Bits	Number of Address bits (RABITS)
256	64 x 39	6	128 x 36	7
512	128 x 39	7	256 x 36	8
1K	256 x 39	8	512 x 36	9
2K	512 x 39	9	1K x 36	10
4K	1K x 39	10	2K x 36	11
8K	2K x 39	11	4K x 36	12

Table 2-2. MAC-FIFO RAM Configurations (continued)

PACKET_SIZE Parameter (Bytes)	Transmit RAM		Receive RAM	
	RAM Size in Bits	Number of Address bits (TABITS)	RAM Size in Bits	Number of Address bits (RABITS)
16K	4K x 39	12	8K x 36	13
32K	8K x 39	13	16K x 36	14

2.12. Frame Filtering (Ask a Question)

Frame filtering allows the MAC to drop or accept frames using hash table based DA matching and additional register-based controls.

2.12.1. Station Address Logic for Frame Filtering (Ask a Question)

This module provides a mechanism to statistically filter frames not intended for this node.

The MAC core performs DA comparison on all the received frames and provides three information signals: UCAD (Perfect DA match), MCAD, and BCAD along with seven most significant bits of the resulting CRC of DA. This information is used to perform a hashing algorithm, compare the result to a programmable hash table and then communicate to the FIFO logic to either delete or store the frame.

The programmability allows the user to assert any bits in a 128 bit hash table that corresponds to the desired Ethernet MAC DA. If the corresponding bit in the table is set, the frame is accepted. In addition, hashing can selectively be performed on unicast addresses or multicast addresses.

2.12.2. Frame Filtering Using MAC Registers (Ask a Question)

Configure the MAC registers to enable selective frame filtering for efficient packet handling.

2.12.2.1. Registers that need to be Configured for Unicast Frame Filtering (Ask a Question)

To enable filtering of **Unicast frames** based on the MAC's **Destination Address (DA)**, the following registers must be configured:

Station Address Registers (0x040 and 0x044)

These registers store the Station Address (the expected Destination Address).

- 0x040 – Station Address Lower Register
- 0x044 – Station Address Upper Register

Example: If the required DA is **01-80-C2-00-00-01**, the registers are programmed as follows:

0x040 : Station Address Lower Register

Bit [31:24] - 8'h01 (D0)

Bit [23:16] - 8'h00 (D1)

Bit [15:8] - 8'h00 (D2)

Bit [7:0] - 8'hC2 (D3)

0x044 : Station Address Upper Register

Bit [31:24] - 8'h80 (D4)

Bit [23:16] - 8'h01 (D5)

Bit [15:0] - 16'h0000 (reserved)

Important: Bit[17] of register **0x058** (MAC-FIFO Configuration Register 4) and Bit[2] of register **0x1C0** (Frame Filter Controls) are mutually exclusive. So, only one of the below two configurations can be used at a time.

Configuration 1: Configure the two registers 0x05C and 0x058 as shown below

MAC-FIFO Configuration Register 4 (0x058)

- **Bit[17] – Host filter frames**
  - Setting this bit drops the frames where DA does not match the programmed Station Address.
  - Clearing this bit passes all frames even when DA does not match the programmed Station Address (no filtering).

MAC-FIFO Configuration Register 5 (0x05C)

- **Bit[17] – Mask bit for unicast filtering control**
  - Default is 1 which means the Bit[17] of 0x058 is masked (filtering disabled).
  - Set this bit to 0 to make the Bit[17] of 0x058 effective for the unicast filtering.

Configuration 2:

Note: This configuration will be effective only when the “Include Station address filtering logic” is enabled in the Configurator

Frame filter controls (0x1c0)

- Bit[3] should be set to 0 (By default, this bit is set to 1)
- Bit[2] of the register should be 1. (By default, this bit is set to 1).

2.12.2.2. Registers that need to be Configured for Multicast and Broadcast Frame Filtering (Ask a Question)

To enable filtering of **Multicast & Broadcast frames**, the following registers must be configured:

Important: Bit[9:8] of register **0x058** (MAC-FIFO Configuration Register 4) and Bit[1:0] of register **0x1C0** (Frame Filter Controls) are mutually exclusive. So, only one of the below two configurations can be used at a time.

Configuration 1: Configure the two registers 0x05C and 0x058 as shown below

MAC-FIFO Configuration Register 4 (0x058)

- **Bit[9:8] – Host filter frames**
  - Bit[9] : Setting this bit drops the frames that contain broadcast address.
  - Bit[8] : Setting this bit drops the frames that contain multicast address.
  - Clearing these two bits passes all the broadcast and multicast frames without filtering.

MAC-FIFO Configuration Register 5 (0x05C)

- **Bit[9:8] – Mask bits for Multicast and Broadcast filtering control**
  - Default is 2’b11 which means the Bit[9:8] of 0x058 is masked (Broadcast and Multicast filtering is disabled).
  - Set these bits to 2’b00 to make the Bit[9:8] of 0x058 effective for the Broadcast and Multicast filtering respectively.

Configuration 2:

Important: This configuration will be effective only when the “Include Station address filtering logic” is enabled in the Configurator.

Frame filter controls (0x1c0)

- Bit[3] should be set to 0 (By default, this bit is set to 1)
- Bit[1] of the register should be 1 to enable Multicast frame filtering (By default, this bit is set to 1).
- Bit[0] of the register should be 1 to enable Broadcast frame filtering (By default, this bit is set to 1).

2.12.2.3. Registers that need to be Configured for Different Types of Error Frames Filtering (Ask a Question)

To enable filtering of any error frames received, the following registers must be configured:

In addition to Unicast, Multicast, and Broadcast filtering, **bits [17:0] of registers 0x05C and 0x058** can also be used to filter different types of error frames.

- To **enable filtering** for a specific frame type, set the corresponding bit in **register 0x058**.
- To make this setting effective, clear the matching bit in **register 0x05C** (since 0x05C acts as the mask for 0x058).

2.13. Statistics Counters Logic (Ask a Question)

This module has separate counters, which simply counts or accumulate conditions that occur upon packets transmitted and received. These counters support Remote Network Monitoring (RMON) Management Information Base (MIB) group 1, RMON MIB group 2, RMON MIB group 3, RMON MIB group 9, RMON MIB 2, and the dot 3 Ethernet MIB.

2.14. SGMII/Ten-Bit Interface (Ask a Question)

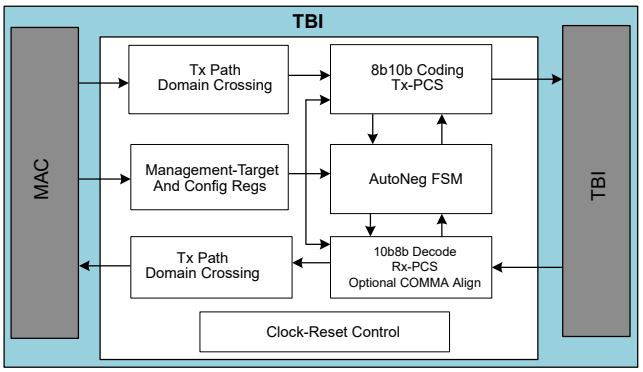
This module takes the transmit G/MII data stream, encodes it into 10-bit symbols and presents 10-bit interface data to Transceiver. Packet data replication is used to match data rates for the different modes of the MII to the transmit clock. In the receive direction de-serialized 10-bit symbols are decoded and converted into the receive G/MII signal set. Packet data under sampling is used to match data rates for the different modes of the MII to the TBI receive clock.

The design uses transmit, receive, and synchronization state machines as specified in Clause 36 of IEEE 802.3z. Also included auto-negotiation (AN) for 1000BASE-X, which is used to exchange information between the link partners. This module is managed and monitored through the MDIO management interface. The extended set of management registers is provided.

Both the transmit and receive paths leverage the physical coding sub layer and the Auto-negotiation sub-layers of the IEEE 802.3z specification, as contained in Clauses 36 and 37. For complete clock domain isolation of the TBI from the MAC, both transmit and receive elasticity FIFOs are used.

The control information exchanged differs from the IEEE specification. Instead of using the ability advertisement, the PHY sends the control information through its Tx_config_Reg [15:0], as listed in following table. Upon receiving control information, the MAC acknowledges the update of the control information by asserting bit 14 of its Tx_config_Reg [15:0].

Figure 2-3. SGMII/TBI Functional Block Diagram



To maintain a constant clock frequency at the PHY interface for all MAC speeds, the MII bus data must be replicated internally to the TBI. Nibble packet data transmitted by a 100 Mbps MAC must be aligned, concatenated, and replicated 10 times. Nibble packet data transmitted by a 10 Mbps MAC must be aligned, concatenated, and replicated 100 times.

Table 2-3. SGMII/TBI Auto-Negotiation Control Information Sent/Received

Bit	Tx_config from PHY to MAC	Tx_config from MAC to PHY
15	Link: • 1: Link up • 0: link down	0: Reserved
14	Reserved for AN ACK.	1
13	0: Reserved	0: Reserved
12	Duplex mode: • 1: Full • 0: Half	0: Reserved
[11:10]	Speed: • 00:10 Mbps • 01:100 Mbps • 10:1000 Mbps • 11: Reserved	0: Reserved
[9:1]	0: Reserved	0: Reserved
0	1	1

Packet data received by the TBI through the PHY must be under sampled by a factor of 10 before being sent to a 100 Mbps MAC. Packet data received by the TBI through the PHY must be under sampled by a factor of 100 before being sent to a 10 Mbps MAC. For half-duplex functionality, carrier sense is inferred from RXDV, and collision is derived from the simultaneous assertion of TXEN and RXDV.

2.15. COMMA Alignment Logic (Ask a Question)

The PHY layer includes COMMA alignment logic in the receive path. This logic detects COMMA data and aligns the 10-bit data to the proper word boundary before passing the data to the receive path.

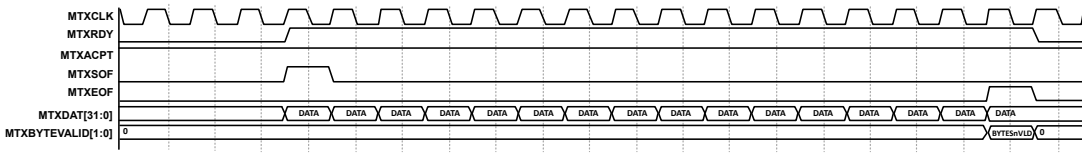
3. Functional Overview (Ask a Question)

This section has all the information regarding utilization of the core.

The MAC Data interface module is interfaced with MAC transmit FIFO for transmit data and MAC receive FIFO for receive data operations. The transmit and receive operations are described as the following respectively.

3.1. Transmit Operation (Ask a Question)

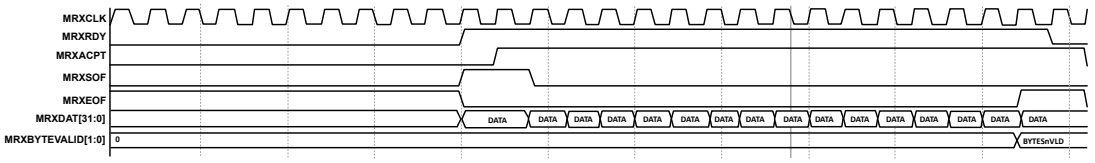
Figure 3-1. Transmit Operation



The MTXDAT (transmit data) word is recorded into MAC transmit FIFO on rising edge of MTXCLK upon the assertion of MTXRDY and MTXACPT and the MTXSOF should be asserted for the first word transfer of the frame. Transmit data stored into MAC transmit FIFO until MTXEOF (end of frame date). MTXBYTEVALID indicates the byte enables of the MTXDAT last word. MTXACPT is asserted when CoreTSE is capable of receiving at least one word from the MAC data path transmit interface. MTXACPT should be monitored for every transmission.

3.2. Receive Operation (Ask a Question)

Figure 3-2. Receive Operation



The core asserts the MRXRDY along with MRXSOF and MRXDAT (receive data) and waits for the MRXACPT. MRXDAT word is available on rising edge of MRXCLK from the MAC receive FIFO until MRXEOF (end of frame date). MRXBYTEVALID indicates the byte enables of the MRXDAT last word.

4. CoreTSE Parameters and Interface Signals (Ask a Question)

This section describes the parameters in the CoreTSE GUI Configurator and Input and Output signals.

4.1. Configuration Settings (Ask a Question)

The register transfer level (RTL) code for CoreTSE has parameters for configuring the core. While working with the core in the SmartDesign tool, a configuration GUI is used to set the values of these parameters. CoreTSE parameters are described in the following table.

Table 4-1. CoreTSE Configuration Parameters

Parameter Name	Valid Values	Default	Description
GMII_TBI	0: G/MII 1: TBI	TBI	This Parameter is used to Select the Interface **Select Interface:** GMII – G/MII interface is enabled TBI (Ten Bit Interface) is enabled.
PACKET_SIZE	6: 256 Bytes 7: 512 Bytes 8: 1K Bytes 9: 2K Bytes 10: 4K Bytes 11: 8K Bytes 12: 16K Bytes 13: 32K Bytes	8K Bytes	This Parameter is used to configure TX/RX FIFO Depth **MAC TX/RX FIFO Depth** PACKET_SIZE parameter is used in the design to define transmit & Receive FIFO address width. The supported PACKET_SIZE choices are: 256 Bytes 512 Bytes 1 K Bytes 2 K Bytes 4 K Bytes 8 K Bytes 16 K Bytes 32 K Bytes
SAL	0-1	1	**Include Station Address filtering logic :** 0 - Do not include SAL 1 - Include SAL
WoL	0-1	1	**Include Wake on LAN logic :** 0 - Do not include WoL 1 - Include WoL **Note:** Supports WoL using AMD's Magic Packet™ Detection Technology
STATS	0-1	1	**Include Statistics Counter logic :** 0 - Do not include statistics counter logic 1 - Include statistics counter logic
MDIO_PHYID	0-31	18	**MDIO Physical Address:** **Note:** This parameter is valid only when parameter GMII_TBI = 1.
SLIP_ENABLE	0-1	0	**Include receive slip logic:** 0 - Do not include receive slip logic 1 - Include receive slip logic **Note:** Applicable for PolarFire and PolarFire SoC device families only when GMII_TBI parameter = 1. **Note:** SLIP_ENABLE must be configured according to Transceiver's SLIP configuration.

Table 4-1. CoreTSE Configuration Parameters (continued)

Parameter Name	Valid Values	Default	Description
ECC_ENABLE	0-1	0	**ECC Enable** 0 – ECC is disabled for embedded memories used in transmit and receive packet FIFO 1 - ECC is enabled for embedded memories used in transmit and receive packet FIFO **Note:** When this parameter is disabled, Interrupts related to ECC in the interrupt ports will be '0' always
TXRX_INTR_ENABLE	0-1	1	**Enable Separate Tx and Rx Interrupt ports** 0 – Enables common Interrupt port TSM_INTR for both Tx and Rx interrupts. 1 – Enables separate Interrupt ports TSM_TX_INTR for Tx and TSM_RX_INTR for Rx interrupts
HOST_INTERFACE	0: Native 1: AXI4Stream	Native	**Host interface** Native: Native interface is enabled AXI4Stream: AXI4Stream interface is enabled

Important:

1. Supports Wake on LAN using AMD's Magic Packet™ Detection technology.
2. This parameter is available for configuration only when GMII_TBI parameter is set to 1 (TBI mode).
3. This parameter is available for configuration only in PolarFire® and PolarFire SoC device families and when GMII_TBI parameter is set to 1 (TBI mode).
4. This parameter should be enabled only if CDR Bit-Slip port is enabled in Transceiver.

4.2. Inputs and Outputs Signals (Ask a Question)

The port signals for CoreTSE are described in the following table.

Clock Ports

CoreTSE has following clock ports.

Table 4-2. Core Clock Signals

Port Name	Width	Direction	Description
MTXCLK	1	Input	MAC Transmit Clock **Note:** This port is exposed to the user only when Native interface is selected.
MRXCLK	1	Input	MAC Receive Clock **Note:** This port is exposed to the user only when Native interface is selected.
AXI4S_ICLK	1	Input	AXI4Stream initiator channel clock signal. **Note:** This port is exposed to the user only when AXI4Stream interface is selected.
AXI4S _TCLK	1	Input	AXI4Stream target channel clock signal. **Note:** This port is exposed to the user only when AXI4Stream interface is selected.
TXCLK	1	Input	2.5/25/125 MHz transmit clock generated from transmit clock of Transceiver according to 10/100/1000 Mbps support
RXCLK	1	Input	2.5/25/125 MHz receive clock generated from receive clock of according to 10/100/1000 Mbps support.
TBI_TX_CLK	1	Input	125 MHz TBI from transmit clock of Transceiver
TBI_RX_CLK	1	Input	125 MHz TBI from receive clock of Transceiver
PCLK	1	Input	APB System Clock: reference clock for all internal logic

Table 4-2. Core Clock Signals (continued)

Port Name	Width	Direction	Description
MDC	1	Output	MDIO management Data Clock. This clock is generated from the PCLK MII Management Data Clock, generated from PCLK.

Reset Ports

Table 4-3. Reset Ports

Port Name	Width	Direction	Clock Domain	Description
PRESETN	1	Input	PCLK	APB system Reset. Active-Low. This active low reset will reset the core to its initial state. This IP core has internal reset synchronizers per clock domain. For RTG4 family devices, PRESETN is used as a synchronous reset and to guarantee successful synchronization this signal should be asserted for a minimum of three clock cycles of slowest clock frequency. For other than RTG4 family devices, PRESETN is used as an asynchronous reset and it is synchronized in all the clock domain such that synchronized reset will be asserted asynchronously and de-assert synchronously.

I/O Signals

All input and output ports are mentioned in following table.

Table 4-4. Input and Output Ports

Port Name	Width	Direction	Clock Domain	Description
MAC Data Path Transmit Interface Signals Note: Below ports will be enabled only when selected Host Interface is "Native"				
MTXRDY	1	Input	MTXCLK	MAC Transmit Ready
MTXACPT	1	Output	MTXCLK	MAC Transmit Accept
MTXSOF	1	Input	MTXCLK	MAC Transmit Start of Frame
MTXEOF	1	Input	MTXCLK	MAC Transmit End of Frame
MTXDAT	32	Input	MTXCLK	MAC Transmit Frame Data
MTXBYTEVALID	2	Input	MTXCLK	MAC Transmit data bytes valid indicator, applicable only for the last word of the frame. 0 - Indicates all bytes in the word are valid. 1 - Indicates the LSB 3 bytes are valid (23:0 bits) 2 - Indicates the LSB 2 bytes are valid (15:0 bits) 3 - Indicates the LSB 1 bytes are valid (7:0 bits)
AXI4Stream target Interface Signals **Note:** Below ports will be enabled only when the Host Interface is "AXI4Stream"				
AXI4S_TTVALID	1	Input		AXI4Stream data valid input
AXI4S_TTREADY	1	Output	AXI4S_TCLK	AXI4Stream data ready to be accepted by the target
AXI4S_TDATA	32	Input	AXI4S_TCLK	AXI4Stream data
AXI4S_TKEEP	4	Input	AXI4S_TCLK	AXI4-Stream byte qualifier that indicates whether the content of the associated byte of the AXI4_TDATA is processed as part of the data or it is a null byte. Valid only at the end of frame. 4'hF - Indicates all bytes in the word are valid. 4'h7 - Indicates the LSB 3 bytes are valid (23:0 bits) 4'h3 - Indicates the LSB 2 bytes are valid (15:0 bits) 4'h1 - Indicates the LSB 1 bytes are valid (7:0 bits)
AXI4S_TTLAST	1	Input	AXI4S_TCLK	AXI4-Stream last transfer indicator, act as a boundary of the packet.

Table 4-4. Input and Output Ports (continued)

Port Name	Width	Direction	Clock Domain	Description
Note: The below port "MTXHWM" will be enabled for both "native" and "AXI4Stream" interfaces.				
MTXHWM	1	Output	MTXCLK	MAC Transmit High Watermark. Asserted whenever the amount of word locations used in the MAC Transmit Data RAM exceeds the configured FIFO register value
MAC Data Path Receive Interface Signals **Note:** Below ports will be enabled only when selected Host Interface is "Native"				
MRXCLK	1	Input	MRXCLK	MAC Receive Clock
MRXRDY	1	Output	MRXCLK	MAC Receive ready
MRXACPT	1	Input	MRXCLK	MAC Receive Accept
MRXSOF	1	Output	MRXCLK	MAC Receive Start of Frame
MRXEOF	1	Output	MRXCLK	MAC Receive End of Frame
MRXDAT	32	Output	MRXCLK	MAC Receive Frame Data
MRXBYTEVALID	2	Output	MRXCLK	MAC Receive data bytes valid indicator, applicable only for the last word of the frame 0 - Indicates all bytes in the word are valid. 1 - Indicates the LSB 3 bytes are valid (23:0 bits) 2 - Indicates the LSB 2 bytes are valid (15:0 bits) 3 - Indicates the LSB 1 bytes are valid (7:0 bits)
AXI4Stream Initiator Interface Signals **Note:** Below ports will be enabled only when selected Host Interface is "AXI4Stream"				
AXI4S_ITVALID	1	Output	AXI4S_ICLK	AXI4Stream data valid output
AXI4S_ITREADY	1	Input	AXI4S_ICLK	AXI4Stream data ready to be accepted by the initiator
AXI4S_IDATA	32	Output	AXI4S_ICLK	AXI4Stream data
AXI4S_IKEEP	4	Output	AXI4S_ICLK	AXI4Stream byte qualifier that indicates whether the content of the associated byte of the AXI4_IDATA is processed as part of the data, or it is a null byte. Valid only at the end of frame. 4'hF - Indicates all bytes in the word are valid. 4'h7 - Indicates the LSB 3 bytes are valid (23:0 bits) 4'h3 - Indicates the LSB 2 bytes are valid (15:0 bits) 4'h1 - Indicates the LSB 1 bytes are valid (7:0 bits)
AXI4S_IUSER	8	Output	AXI4S_ICLK	AXI4Stream side-band information, that can be transmitted alongside the data stream. Bit[7:5] – Reserved Bit[4] – TX_ECC_SEC Bit[3] – TX_ECC_DED Bit[2] – RX_ECC_SEC Bit[1] – RX_ECC_DED Bit[0] – RCG_ERROR
G/MII PHY Signals **Note:** This interface is available when GMII_TBI parameter is 0.				
TXEN	1	Output	TXCLK	Transmit Enable
TXD	8	Output	TXCLK	Transmit Data
TXER	1	Output	TXCLK	Transmit Error
RXDV	1	Input	RXCLK	Receive Data Valid
RXD	8	Input	RXCLK	Receive Data
RXER	1	Input	RXCLK	Receive Error

Table 4-4. Input and Output Ports (continued)

Port Name	Width	Direction	Clock Domain	Description
CRS	1	Input	Asynchronous	G/MII carrier sense flag
COL	1	Input	Asynchronous	G/MII collision detect flag
TBI PHY Signals **Note:** This interface is available when GMII_TBI parameter is 1.				
TCG	10	Output	TBI_TX_CLK	Transmit code group to the Transceiver.
RCG	10	Input	TBI_RX_CLK	Receive code group from the Transceiver.
TBI_TX_VALID	1	Output	TBI_TX_CLK	TCG valid, recommended to connect with Transceiver transmit valid. **Note:** This signal is visible to the user when SmartFusion2/ IGLOO2/RTG4 families are used
TBI_RX_VALID	1	Input	TBI_RX_CLK	Available for PolarFire / PolarFire SoC and PolarFire 2, recommended connecting to Transceiver receive valid. **Note:** This signal is available for PolarFire, PolarFire SoC and PolarFire 2 device families only when SLIP_ENABLE parameter is 1.
TBI_RX_READY	1	Input	TBI_RX_CLK	RCG valid recommended connecting with Transceiver Ready. **Note:** This signal is available for PolarFire and PolarFireSoC device families only when SLIP_ENABLE parameter is 1. **Note:** This signal is available always for other device families.
SIGNAL_DETECT	1	Input	Asynchronous	This signal is typically provided from the optical module to indicate when an optical signal is valid otherwise it should be driven 1.
RX_SLIP	1	Output	TBI_RX_CLK	Recommended to connect to receive slip signal of Transceiver. **Note:** 1. This signal is available for PolarFire and PolarFireSoC device families only when Include receive slip logic (SLIP_ENABLE)is enabled in the GUI configurator. 2. This signal is not available for other device families.
SYNC	1	Output	TBI_RX_CLK	Receive link sync status.
ANX_STATE	10	Output	TBI_TX_CLK	Auto negotiation status information. Bit [0] - DISABLE_LINK_OK state Bit [1] - AN_ENABLE state Bit [2] - AN_RESTART state Bit [3] - ABILITY_DETECT state Bit [4] - ACKNOWLEDGE_DETECT state Bit [5] - NEXT_PAGE_WAIT state Bit [6] - COMPLETE_ACKNOWLEDGE state Bit [7] - IDLE_DETECT state Bit [8] - LINK_OK state Bit [9] - Received configuration frame data
RCG_ERROR	1	Output	TBI_RX_CLK	Indicates the receive code group error.
Management interface Signals				
MDI	1	Input	PCLK	MII Management Data Input.
MDO	1	Output	PCLK	MII Management Data Output.
MDOEN	1	Output	PCLK	MII Management Data Output Enable.
APB Target Interface Signals				
PADDR	32	Input	PCLK	APB Address Bus.
PSEL	1	Input	PCLK	APB Target Select.

Table 4-4. Input and Output Ports (continued)

Port Name	Width	Direction	Clock Domain	Description
PENABLE	1	Input	PCLK	APB Enable
PWRITE	1	Input	PCLK	APB Write.
PWDATA	32	Input	PCLK	APB Write Data Bus.
PREADY	1	Output	PCLK	APB Target Ready.
PRDATA	32	Output	PCLK	APB Read Data Bus.
PSLVERR	1	Output	PCLK	APB Target Error, indicates the failure of the transfer.
Miscellaneous Signals				
TSM_INTR	4	Output	PCLK	This port will be enabled only when "TXRX_INTR_ENABLE" parameter value is '0'. **Note:** If ECC_ENABLE parameter is '0', then the interrupt bits Bit [3] & Bit [2] will be always "0" and can be ignored Interrupt signals. Providing this individual interrupt at top allows user to connect required interrupts to host-processor based on application requirement. Bit [3] – Tx/Rx_ECC_SEC interrupt • This interrupt is asserted when "sb_correct" flag asserts from transmitter or receiver ram and deasserted when read request comes for the respective counters (TSBECC/ RSBECC) Bit [2] – Tx/Rx_ECC_DED interrupt. • This interrupt is asserted when "db_detect" flag asserts from transmitter or receiver ram and deasserted when read request comes for the respective counters (TDBEDC/ RDBEDC) Bit [1] - Wake On LAN detected interrupt Bit [0] - Statistics counter carry interrupt • Statistics counter carry interrupt is generated whenever there is a carry produced in any of the implemented counters. • This will be de-asserted whenever the user clears the generated carry bits in the CAR1 and CAR2 registers.
TSM_TX_INTR	4	Output	PCLK	**Transmitter Interrupt port** This port is enabled only when the parameter "**Enable Separate Tx and Rx Interrupt ports**" value is '1'. This port will have all the interrupt signals related to transmitter. **Note:** If ECC_ENABLE parameter is '0', then the interrupt bits Bit [3] & Bit [2] will be always "0" and can be ignored Bit [3] - Tx_ECC_SEC interrupt • This interrupt is asserted when "sb_correct" flag asserts from transmitter embedded RAM and de - asserted when read request comes for the respective register (TSBECC) Bit [2] – Tx_ECC_DED interrupt • This interrupt is asserted when "db_detect" flag asserts from transmitter embedded RAM and de - asserted when read request comes for the respective register (TDBEDC) Bit [1] – Reserved (Default value '0') Bit [0] – Tx Statistics counter carry interrupt • Transmitter Statistics counter carry interrupt is generated whenever there is a carry produced in any of the implemented counters related to transmitter. • It will be de-asserted whenever the user clears the generated carry bits in the CAR2 register

Table 4-4. Input and Output Ports (continued)

Port Name	Width	Direction	Clock Domain	Description
TSM_RX_INTR	4	Output	PCLK	**Receiver Interrupt port** This port is enabled only when the parameter "**Enable Separate Tx and Rx Interrupt ports**" value is '1'. This port will have all the interrupt signals related to receiver. **Note:** If ECC_ENABLE parameter is '0', then the interrupt bits Bit [3] & Bit [2] will be always "0" and can be ignored Bit [3] - Rx_ECC_SEC interrupt • This interrupt is asserted when "sb_correct" flag asserts from receiver embedded RAM and deasserted when read request comes for the respective register (RSBECC) Bit [2] – Rx_ECC_DED interrupt • This interrupt is asserted when "db_detect" flag asserts from receiver embedded RAM and deasserted when read request comes for the respective register (RDBEDC) Bit [1] – Wake On LAN detected interrupt Bit [0] – Rx Statistics counter carry interrupt • Receiver Statistics counter carry interrupt is generated whenever there is a carry produced in any of the implemented counters related to receiver. • It will be de-asserted whenever the user clears the generated carry bits in the CAR1 register.
TSM_CONTROL	32	Output	PCLK	32bit GPIO output signals mapped to system miscellaneous control register (0x1D4).
TX_ECC_SEC	1	Output	TXCLK	ECC flag for single bit error correction in transmitter buffer **Note:** This flag will be asserted whenever a single bit error is detected/corrected in the transmitter buffer during packet transfer and will be de-asserted after the "sb_correct" flag from transmitter buffer is de-asserted
TX_ECC_DED	1	Output	TXCLK	ECC flag for double bit error detection in transmitter buffer **Note:** This flag will be asserted whenever a double bit error is detected in the transmitter buffer during packet transfer and will be de-asserted after the "db_detect" flag from transmitter buffer is de-asserted
RX_ECC_SEC	1	Output	MRXCLK	ECC flag for single bit error correction in receiver buffer **Note:** This flag will be asserted whenever a single bit error is detected/corrected in the receiver buffer during packet transfer and will be de-asserted only on the occurrence of "End of Frame (**MRXEOF**)" signal.
RX_ECC_DED	1	Output	MRXCLK	ECC flag for double bit error detection in receiver buffer **Note:** This flag will be asserted whenever a double bit error is detected in the receiver buffer during packet transfer and will be de-asserted only on the occurrence of "End of Frame (**MRXEOF**)" signal.

5. Implementation of CoreTSE in Libero Design Suite (Ask a Question)

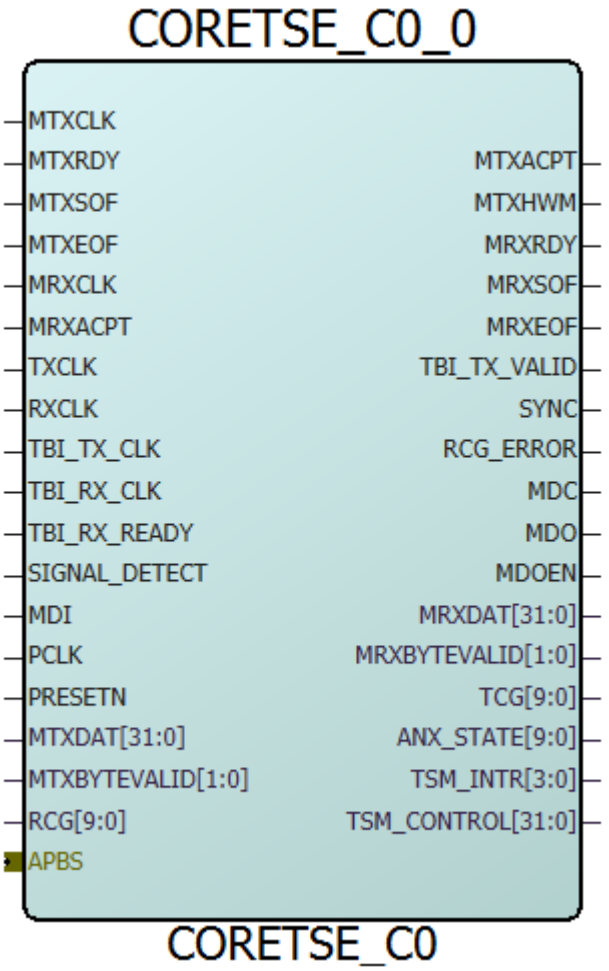
This section describes the implementation of the CoreTSE in Libero Design Suite.

5.1. SmartDesign (Ask a Question)

Once installed in the Libero software, the core is instantiated, configured, connected, and generated using the SmartDesign tool.

The following figure shows an example of instantiated view.

Figure 5-1. SmartDesign CoreTSE Instance View



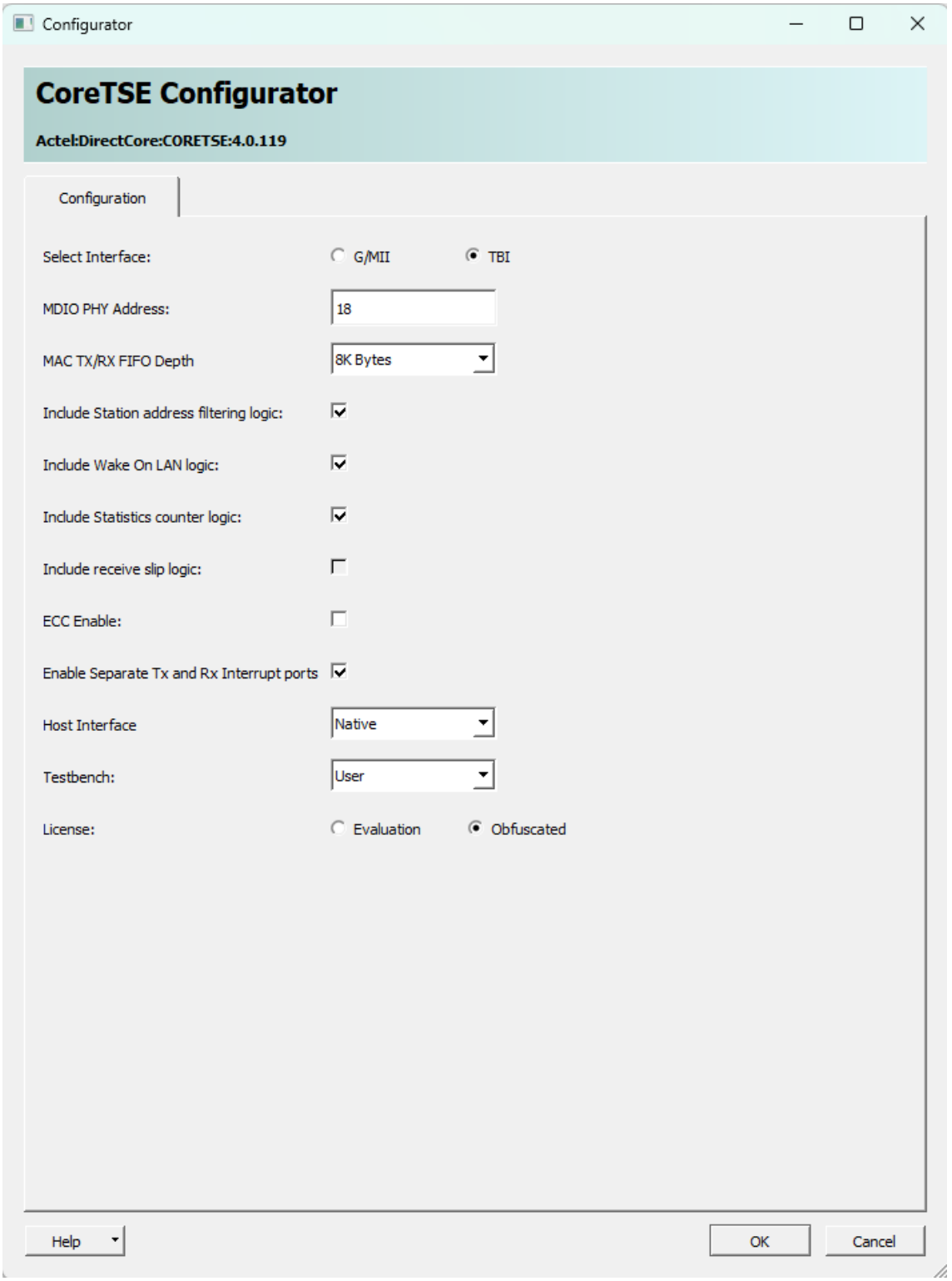
For more information on using SmartDesign to instantiate and generate cores, see, SmartDesign User Guide.

5.1.1. Configuring CoreTSE in SmartDesign (Ask a Question)

The CoreTSE configuration GUI takes up a large amount of screen area when it is sized to show all configuration options.

An example of the GUI for the RTG4™ family is shown in the following figure.

Figure 5-2. CoreTSE Configuration GUI



5.1.2. Simulation Flows (Ask a Question)

To simulate the core using the testbench, after configuring the CoreTSE as per the requirement, perform the following steps:

1. Set the design root to the CoreTSE instantiation in the Libero® SoC Design Hierarchy pane, and then click **Build Hierarchy**.
2. Click **Stimulus Hierarchy** tab, and then click **Build Hierarchy**.
3. Right-click **testbench**.
4. Under **Simulate Pre-Synthesis Design**, select **Open Interactively**.
5. For complete visibility of CoreTSE input and output ports, add an additional vsim command. To add command, perform the following steps:
   - Navigate to **Project Project Settings Simulation Options Vsim Commands**.
   - Under **Additional options**, enter "-voptargs=+acc".
   - Click **Save Changes**.

QuestaSim opens with the testbench file and automatically runs the simulation.

Important: If the simulation is interrupted due to the runtime limit specified in the .do file, use the `run -all` command to complete the simulation.

5.1.3. Synthesis (Ask a Question)

To run synthesis, perform the following steps:

1. With the configuration selected in the configuration GUI, set the design root appropriately.
2. Under **Implement Design**, on the **Design Flow** tab, right-click **Synthesize** and click **Run**.

5.1.4. Place-and-Route (Ask a Question)

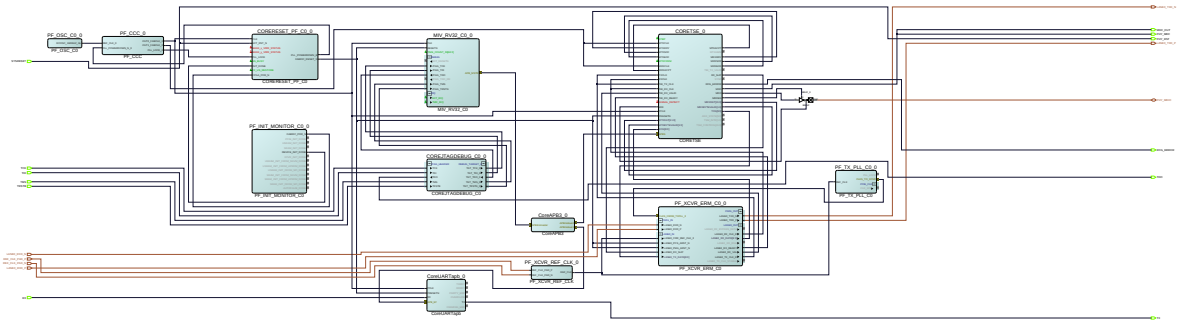
To run the place and route, perform the following steps:

1. With the configuration selected in the configuration GUI, set the design root appropriately.
2. Under Implement Design, on the **Design Flow** tab, right-click Place and Route and click **Run**.

5.1.5. System Integration (Ask a Question)

This section provides the details to ease the integration of CoreTSE.

Figure 5-3. CoreTSE System Integration



- FABRIC_RESET_N of CORE_RESET_PF_C0 is used as reset for all modules
- CoreTSE_0 has PCLK, MTXCLK, MRXCLK, TXCLK, RXCLK, TBI_TX_CLK, TBI_RX_CLK, and MDC clocks.
- PCLK is 50 MHz clock generated from PF_CCC_0

- MTXCLK and MRXCLK are 125 MHz clocks generated from PF_CCC_0
- TBI_TX_CLK and TXCLK are connected to 125 MHz LANE0_TX_CLK_R of PF_XCVR_0
- TBI_RX_CLK and RXCLK are connected to 125 MHz LANE0_RX_CLK_R of PF_XCVR_0
- 2.5 MHz MDC is generated by CoreTSE_0 from PCLK

Run the Libero flow with enabling the timing driven and high effort place and route option. The example design can be obtained from the Microchip technical support team.

5.2. Verification (Ask a Question)

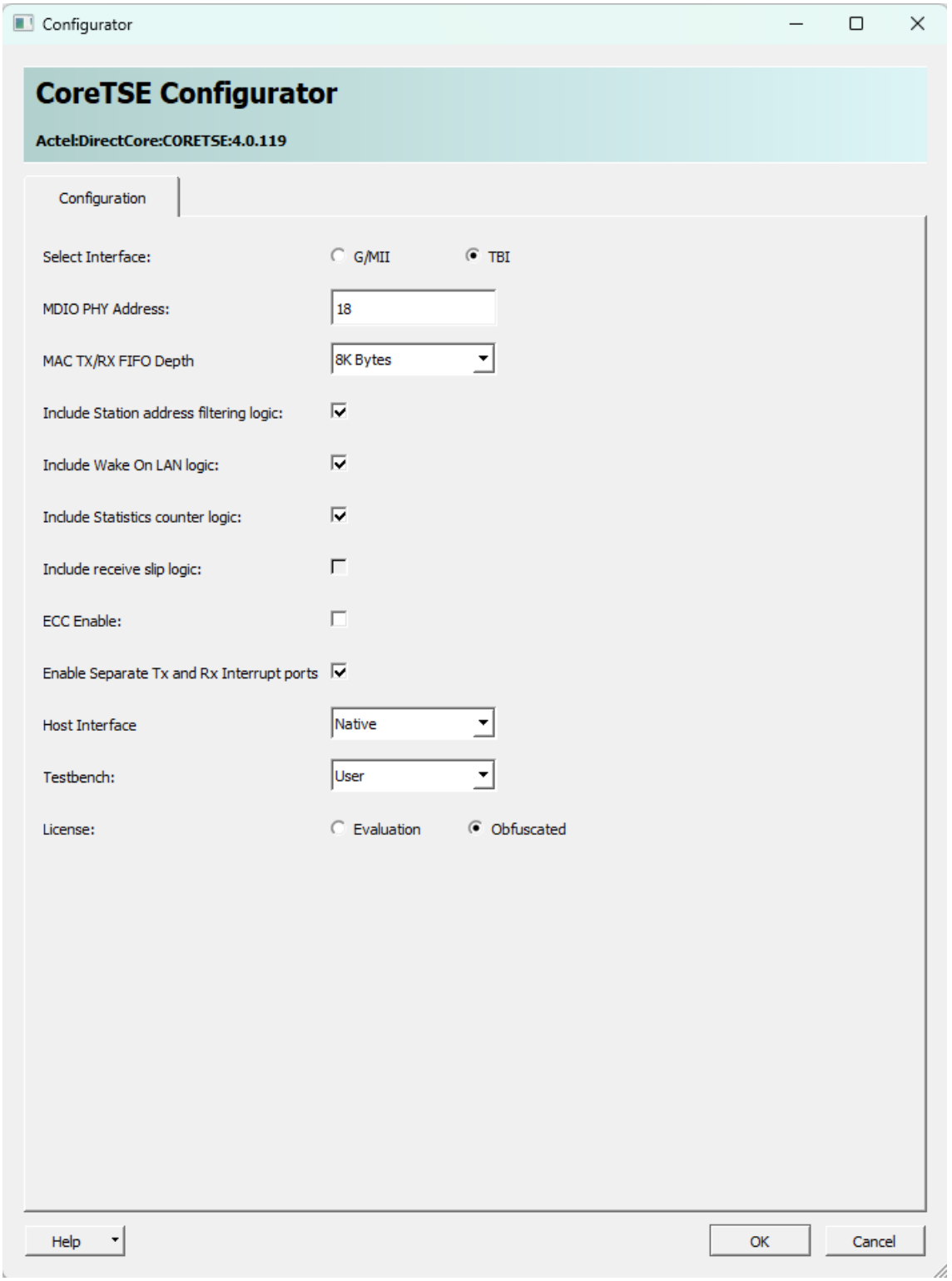
This section describes verification of the CoreTSE.

5.2.1. Testbench (Ask a Question)

A unified testbench is used to verify and test CoreTSE called as user testbench.

Simulation with "user testbench" passes only with default configuration, as shown in the following figure:

Figure 5-4. Default configuration



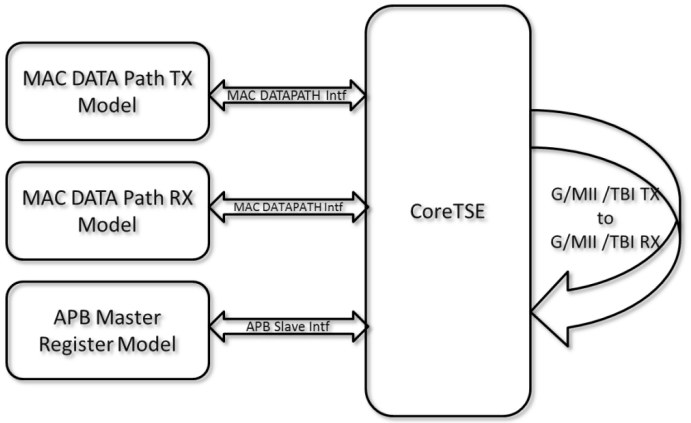
The Select Interface supports switching between G/MII and TBI.

5.2.1.1. User Testbench (Ask a Question)

A simplified block diagram of the user testbench is shown in the following figure. The user testbench instantiates the CoreTSE with near end loopback at TBI/G/MII interface. Testbench

provides behavioral, non-synthesizable MAC data path interface models for descriptors and MAC configurations.

Figure 5-5. CoreTSE User Testbench



Testbench has task based library models for MAC data interface, MAC data transmit, MAC data receive, MAC link transmit, MAC link receive, and generic testbench to check and report errors.

5.2.1.1.1. TBI Mode (Ask a Question)

In TBI mode, the following test case is available:

1. Auto negotiation test case
   - Configure MDIO registers using APB Target register interface for Auto negotiation restart & enable.
   - Waits for auto negotiation completion.
   - Verifies the Auto negation status in MDIO registers and ANX_STATE port status.
2. TBI near end loopback test case
   - Configures MAC registers for full duplex and specific speed mode of operation
   - Test case waits few clocks for CoreTSE to transmit and looped back at TBI interface
   - MAC Data path RX Target model receives the looped back packet and testbench checks for data integrity.
   - Above steps are repeated for 10/100/1000 speed modes with for loop of few iterations.

5.2.1.1.2. G/MII Mode (Ask a Question)

In G/MII mode, the following test cases are available:

1. G/MII near end loopback test case
   - Configures MAC registers for full duplex and specific speed mode of operation.
   - Test case waits few clocks for CoreTSE to transmit and looped back at G/MII interface.
   - MAC Data path RX Target model receives the looped back packet and testbench checks for data integrity.
   - Above steps are repeated for 10/100/1000 speed modes with for loop of few iterations.

6. Clocks and Reset (Ask a Question)

This section describes the clocks and reset of the CoreTSE.

6.1. Clocks (Ask a Question)

The IP core uses the following clocks:

- **PCLK** – Clock input for APB interface.
- **MTXCLK** – Clock input for MAC data path transmit interface (when select interface is "NATIVE").
- **AXI4S_TCLK** – Clock input for MAC data path transmit interface (when select interface is "AXI4Stream").
- **MRXCLK** – Clock input for MAC data path receive interface (when select interface is "NATIVE").
- **AXI4S_ICLK** – Clock input for MAC data path receive interface (when select interface is "AXI4Stream").
- **TBI_TX_CLK** – 125 MHz clock input for TBI transmit interface. This clock is connected to the Transmit clock from the Transceiver. This clock is available only in TBI mode.
- **TXCLK** – 125/25/2.5 MHz clock input for G/MII interface/MAC operations in 1000/100/10 Mbps data-rate respectively. In TBI mode, this clock is generated from TBI_TX_CLK. In G/MII mode, this clock is connected to the Transmit clock from the G/MII PHY.
- **TBI_RX_CLK** – 125 MHz clock input for TBI receive interface. This clock is connected to the Receive clock from the Transceiver. This clock is available only in TBI mode.
- **RXCLK** – 125/25/2.5 MHz clock input for G/MII interface/MAC operations in 1000/100/10 Mbps data-rate respectively. In TBI mode, this clock is generated from TBI_RX_CLK. In G/MII mode, this clock is connected to the Receive clock from the G/MII PHY.
- **MDC** – Management clock output for MDIO interface. This clock is generated by the IP core. PCLK is the source clock. The MGMT CLOCK SELECT field of MDIO Mgmt: Configuration register (address 0x020) determines the frequency of this clock.

6.2. Reset (Ask a Question)

Following reset is used in the IP core:

PRESETN

Active-Low reset input. This reset is asserted asynchronously, but de-asserted synchronous to PCLK.

For all clock domains except PCLK clock domain, PRESETN reset input is synchronized to the respective clock domain and used within that clock domain.

In SmartFusion2, IGLOO2, PolarFire, and PolarFire SoC device families, reset is used as asynchronous reset. In RTG4 device family, reset is used as synchronous reset.

In RTG4 device family, all the clock inputs shall be available and stable before reset assertion. And the reset shall be asserted for atleast three clock cycles of the slowest clock used in this IP.

7. Design Constraints (Ask a Question)

This section describes the design constraints of the CoreTSE.

7.1. Timing Constraints (Ask a Question)

This section provides the information on the timing constraints required for CoreTSE.

Important: In all the timing constraints provided in the reference sdc file, `CORETSE_C0_0` is the instance name of CoreTSE IP in the Libero SoC. You can replace the instance name when using this timing constraint in your design.

To meet the CoreTSE timing requirement, it is important to provide timing constraint.

MDC: Management clock output for MDIO interface. This clock is generated internally by the IP Core. PCLK is the source clock.

It is recommended to use the generated clock constraints for the management clock. The MGMT CLOCK SELECT field of the MDIO Mgmt: Configuration register (address 0x020) determines the frequency of this clock. An example is given in the reference sdc file for generated clock constraint for division factor 8 (MGMT CLOCK SELECT = 3'b011).

It is recommended to provide set clock group timing constraint to set false path between asynchronous clocks.

CoreTSE uses the following clocks when the **select interface** is set to **TBI**:

- MTXCLK / AXI4S _TCLK (Depends on the "Host Interface" selection)
- MRXCLK / AXI4S _ICLK (Depends on the "Host Interface" selection)
- TXCLK (Synchronous to TBI_TX_CLK)
- RXCLK (Synchronous to TBI_RX_CLK)
- TBI_TX_CLK
- TBI_RX_CLK
- MDC (Synchronous to PCLK)

CoreTSE uses the following clocks when the **select interface** is set to **GMII**:

- PCLK
- TXCLK
- RXCLK
- MTXCLK / AXI4S _TCLK (Depends on the "Host Interface" selection)
- MRXCLK / AXI4S _ICLK (Depends on the "Host Interface" selection)

The source clock name used in the reference sdc file is for reference only. The source name might be different in your design, and you must change the clock name in the constraint accordingly.

You can find reference sdc timing constraint file from the following path:

```
<project_directory/component/Actel/DirectCore/CoreTSE/(example 4.0.xxx)/
constraints/CoreTSE.sdc>
```

Important: Additionally, the generated clock (mdc) clock constraint are found in the `CoreTSE_mdc.sdc` file, which is situated in the previously specified directory.

It is important to ensure that the **Synthesis** option is unchecked in the **Constraints Manager** when utilizing the `CoreTSE_mdc.sdc` file.

8. Register Map and Descriptions (Ask a Question)

This section provides the register map descriptions for MAC and MDIO.

8.1. MAC (Ask a Question)

This section provides the MAC register descriptions of the CoreTSE.

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	MACConfiguration1	7:0			RECEIVE FLOW CONTROL ENABLE	TRANSMIT FLOW CONTROL ENABLE	SYNCHRONIZED RECEIVE ENABLE	RECEIVE ENABLE	SYNCHRONIZED TRANSMIT ENABLE	TRANSMIT ENABLE
		15:8								LOOP BACK
		23:16								
		31:24	SOFT RESET							
0x04	MACConfiguration2	7:0		RX CRC DISABLE	HUGE FRAME ENABLE	LENGTH FIELD CHECKING		PAD/CRC ENABLE	CRC ENABLE	FULL-DUPLEX
		15:8	PREAMBLE LENGTH[3:0]						INTERFACE MODE[1:0]	
		23:16								
		31:24								
0x08	IPG	7:0		BACK_TO_BACK INTER_PACKET_GAP[6:0]						
		15:8	MINIMUM IFG ENFORCEMENT[7:0]							
		23:16		NON_BACK_TO_BACK INTER_PACKET_GAP PART2 (IPGR2)[6:0]						
		31:24		NON_BACK_TO_BACK INTER_PACKET_GAP PART1 (IPGR1)[6:0]						
0x0C	Half-Duplex	7:0	COLLISION WINDOW[7:0]							
		15:8	RETRANSMISSION MAXIMUM[3:0]						COLLISION WINDOW[9:8]	
		23:16	ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION[3:0]				ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE	BACKPRESSURE NO BACKOFF	NO BACKOFF	EXCESSIVE DEFER
		31:24								
0x10	Maximum_Frame_Length	7:0	MAXIMUM FRAME LENGTH[7:0]							
		15:8	MAXIMUM FRAME LENGTH[15:8]							
		23:16								
		31:24								
0x14	Control_Frame_extended_parameter	7:0	CFEP[7:0]							
		15:8	CFEP[15:8]							
		23:16								
		31:24								
0x18	Control_Frame_parameter	7:0	CFPT[7:0]							
		15:8	CFPT[15:8]							
		23:16								
		31:24								
0x1C	Test_Register	7:0					MAXIMUM BACKOFF	REGISTERED TRANSMIT FLOW ENABL	TEST PAUSE	SHORTCUT SLOT TIME
		15:8								
		23:16								
		31:24								
0x20	MIIMgmt_Configuration	7:0			SCAN AUTO INCREMENT	PREAMBLE SUPPRESSION		MGMT CLOCK SELECT[2:0]		
		15:8								
		23:16								
		31:24	RESET MDIO MGMT							
0x24	MIIMgmt_Command	7:0							SCAN CYCLE	READ CYCLE
		15:8								
		23:16								
		31:24								
0x28	MIIMgmt_Address	7:0				REGISTER ADDRESS[4:0]				
		15:8				PHY ADDRESS[4:0]				
		23:16								
		31:24								

MAC (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x2C	MIIMgmt_Control	7:0	MDIO MGMT CONTROL (PHY CONTROL)[7:0]							
		15:8	MDIO MGMT CONTROL (PHY CONTROL)[15:8]							
		23:16								
		31:24								
0x30	MIIMgmt_Status	7:0	MDIO MGMT STATUS (PHY STATUS)[7:0]							
		15:8	MDIO MGMT STATUS (PHY STATUS)[15:8]							
		23:16								
		31:24								
0x34	MIIMgmt_Indicators	7:0						NOT VALID	SCANNING	BUSY
		15:8								
		23:16								
		31:24								
0x38	Interface_Control	7:0	WOL: UNICAST MATCH ENABLE	WOL: MAGIC PACKET DETECTION ENABLE	WOL: WAKE ON LANE DETECTED CLEAR STATUS CLEAR	STATS COUNTERS : AUTO CLEAR COUNTERS ON READ	STATS COUNTERS : CLEAR ALL COUNTERS	STATS COUNTERS : MODULE ENABLE		
		15:8								
		23:16								
		31:24								
0x3C	Interface_Status	7:0					LINK FAIL			
		15:8						WAKE ON LANE DETECTED	EXCESS DEFER	
		23:16								
		31:24								
0x40	Station_Address_Lower_Register	7:0	FOURTH OCTET OF THE DA IN THE FRAME[7:0]							
		15:8	THIRD OCTET OF THE DA IN THE FRAME[7:0]							
		23:16	SECOND OCTET OF THE DA IN THE FRAME[7:0]							
		31:24	FIRST OCTET OF THE DA IN THE FRAME[7:0]							
0x44	Station_Address_Higher_Register	7:0								
		15:8								
		23:16	SIXTH OCTET OF THE DA IN THE FRAME[7:0]							
		31:24	FIFTH OCTET OF THE DA IN THE FRAME[7:0]							
0x48	A-MCXFIF0	7:0				HOST FABRIC TRANSMIT MODULE RESET (HSTRSTFT)	HOST MAC TRANSMIT MODULE RESET (HSTRSTST)	HOST FABRIC RECEIVE MODULE RESET (HSTRSTFR)	HOST MAC RECEIVE MODULE RESET (HSTRSTSR)	HOST TRANSMIT WATERMARK MODULE RESET (HSTRSTWT)
		15:8				FABRIC TRANSMIT MODULE ENABLE REQUEST(FTFENREQ)	SYSTEM TRANSMIT MODULE ENABLE REQUEST (STFENREQ)	FABRIC RECEIVE MODULE ENABLE REQUEST(FRFENREQ)	SYSTEM RECEIVE MODULE ENABLE REQUEST(SRFENREQ)	WATER MARK MODULE ENABLE REQUEST(WTMENREQ)
		23:16				FABRIC TRANSMIT MODULE ENABLE STATUS (FTFENRPLY)	SYSTEM TRANSMIT MODULE ENABLE STATUS (STFENRPLY)	FABRIC RECEIVE MODULE ENABLE STATUS (FRFENRPLY)	SYSTEM RECEIVE MODULE ENABLE STATUS (SRFENRPLY)	WATER MARK MODULE ENABLE STATUS(WTMENRPLY)
		31:24								
0x4C	A-MCXFIF1	7:0	NUMBER OF PAUSE QUANTAS BEFORE XOFF RETRANSMISSION (CFGXOFFRTX) [7:0]							
		15:8	NUMBER OF PAUSE QUANTAS BEFORE XOFF RETRANSMISSION (CFGXOFFRTX) [15:8]							
		23:16	SYSTEM RECEIVE FOR CUT THROUGH THRESHOLD (CFGSRTH) [7:0]							
		31:24					SYSTEM RECEIVE FOR CUT THROUGH THRESHOLD (CFGSRTH) [11:8]			

MAC (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x50	A-MCXFIF2	7:0	MIN WORDS IN RECEIVE FIFO BEFORE (CFGLWM) [7:0]							
		15:8				MIN WORDS IN RECEIVE FIFO BEFORE (CFGLWM) [12:8]				
		23:16	MAX WORDS IN RECEIVE FIFO (CFGHWM) [7:0]							
		31:24				MAX WORDS IN RECEIVE FIFO (CFGHWM) [12:8]				
0x54	A-MCXFIF3	7:0	FABRIC TRANSMIT CUT THROUGH THRESHOLD (CFGFTTH) [7:0]							
		15:8				FABRIC TRANSMIT CUT THROUGH THRESHOLD (CFGFTTH) [12:8]				
		23:16	MIN WORDS IN RECEIVE FIFO BEFORE (CFGLWM) [7:0]							
		31:24				MIN WORDS IN RECEIVE FIFO BEFORE (CFGLWM) [12:8]				
0x58	A-MCXFIF4	7:0	HOST FILTER FRAMES (HSTFLTRFRM) [7:0]							
		15:8	HOST FILTER FRAMES (HSTFLTRFRM) [15:8]							
		23:16							HOST FILTER FRAMES (HSTFLTRFRM) [17:16]	
		31:24								
0x5C	A-MCXFIF5	7:0	HOST DONT CARE FOR FILTERING OF FRMES (HSTFLTRFRMDC) [7:0]							
		15:8	HOST DONT CARE FOR FILTERING OF FRMES (HSTFLTRFRMDC) [15:8]							
		23:16		HALF DUPLEX INDICATOR (CFGHDPLX)	SYSTEM RECEIVE FIFO FULL (SRFULL)	HOST CLEAR SYSTEM RECEIVE FIFO FULL (HSTSRFULLCLR)	ONE BYTE TRANSFER PER SYSTEM CLOCK (CFGBYTMODE)	HOST DROP FRAMES LESS THAN 64 BYTES (HSTDRPLT64)	HOST DONT CARE FOR FILTERING OF FRMES (HSTFLTRFRMDC) [17:16]	
		31:24								
0x60	A-MCXFIFRAMAccess0	7:0	HOST TRANSMIT RAM WRITE ADDRESS (HSTTRAMWADX [12:0])							
		15:8				HOST TRANSMIT RAM WRITE ADDRESS (HSTTRAMWADX [12:0])				
		23:16	HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[39:32])							
		31:24	HOST TRANSMIT RAM WRITE REQUEST (HSTTRAMWREQ)	HOST TRANSMIT RAM WRITE ACKNOWLEDGE (HSTTRAMWACK)						
0x64	A-MCXFIFRAMAccess1	7:0	HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[31:0])							
		15:8	HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[31:0])							
		23:16	HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[31:0])							
		31:24	HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[31:0])							
0x68	A-MCXFIFRAMAccess2	7:0	HOST TRANSMIT RAM READ ADDRESS (HSTTRAMRADX[12:0])							
		15:8				HOST TRANSMIT RAM READ ADDRESS (HSTTRAMRADX[12:0])				
		23:16	HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[39:32])							
		31:24	HOST TRANSMIT RAM READ REQUEST. (HSTTRAMRREQ)	HOST TRANSMIT RAM READ ACKNOWLEDGE (HSTTRAMRACK)						
0x6C	A-MCXFIFRAMAccess3	7:0	HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[31:0])							
		15:8	HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[31:0])							
		23:16	HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[31:0])							
		31:24	HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[31:0])							
0x70	A-MCXFIFRAMAccess4	7:0	HOST RECEIVE RAM WRITE ADDRESS (HSTTRAMWADX[(RABITS+2):0])							
		15:8		HOST RECEIVE RAM WRITE ADDRESS (HSTTRAMWADX[(RABITS+2):0])						
		23:16	HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT[39:32])							
		31:24	HOST RECEIVE RAM WRITE REQUEST (HSTRRAMWREQ)	HOST RECEIVE RAM WRITE ACKNOWLEDGE (HSTRRAMWACK)						

MAC (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x74	A-MCXFIFRAMAccess5	7:0	HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT [31:0])							
		15:8	HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT [31:0])							
		23:16	HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT [31:0])							
		31:24	HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT [31:0])							
0x78	A-MCXFIFRAMAccess6	7:0	HOST RECEIVE RAM READ ADDRESS (HSTRRAMRADX[31:0])							
		15:8			HOST RECEIVE RAM READ ADDRESS (HSTRRAMRADX[31:0])					
		23:16	HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[39:32])							
		31:24	HOST RECEIVE RAM READ REQUEST (HSTRRAMRREQ)	HOST RECEIVE RAM READ ACKNOWLEDGE (HSTRRAMRACK)						
0x7C	A-MCXFIFRAMAccess7	7:0	HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[31:0])							
		15:8	HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[31:0])							
		23:16	HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[31:0])							
		31:24	HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[31:0])							
0x80	TR64	7:0	TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [17:16]	
		31:24								
0x84	TR127	7:0	TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [17:16]	
		31:24								
0x88	TR255	7:0	TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [17:16]	
		31:24								
0x8C	TR511	7:0	TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [17:16]	
		31:24								
0x90	TR1K	7:0	TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [17:16]	
		31:24								
0x94	TRMAX	7:0	TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [17:16]	
		31:24								
0x98	TRMGV	7:0	TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [7:0]							
		15:8	TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [15:8]							
		23:16							TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [17:16]	
		31:24								

MAC (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x9C	RBYT	7:0	RECEIVE BYTE COUNTER [7:0]							
		15:8	RECEIVE BYTE COUNTER [15:8]							
		23:16	RECEIVE BYTE COUNTER [23:16]							
		31:24								
0xA0	RPKT	7:0	RECEIVE PACKET COUNTER [7:0]							
		15:8	RECEIVE PACKET COUNTER [15:8]							
		23:16							RECEIVE PACKET COUNTER [17:16]	
		31:24								
0xA4	RFCS	7:0	RECEIVE FCS ERROR COUNTER [7:0]							
		15:8					RECEIVE FCS ERROR COUNTER [11:8]			
		23:16								
		31:24								
0xA8	RMCA	7:0	RECEIVE MULTICAST PACKET COUNTER [7:0]							
		15:8	RECEIVE MULTICAST PACKET COUNTER [15:8]							
		23:16							RECEIVE MULTICAST PACKET COUNTER [17:16]	
		31:24								
0xAC	RBCA	7:0	RECEIVE BROADCAST PACKET COUNTER [7:0]							
		15:8	RECEIVE BROADCAST PACKET COUNTER [15:8]							
		23:16							RECEIVE BROADCAST PACKET COUNTER [17:16]	
		31:24								
0xB0	RXCF	7:0	RECEIVE CONTROL FRAME PACKET COUNTER [7:0]							
		15:8					RECEIVE CONTROL FRAME PACKET COUNTER [11:8]			
		23:16								
		31:24								
0xB4	RXPF	7:0	RECEIVE PAUSE CONTROL FRAME COUNTER [7:0]							
		15:8					RECEIVE PAUSE CONTROL FRAME COUNTER [11:8]			
		23:16								
		31:24								
0xB8	RXUO	7:0	RECEIVE UNKNOWN OPCODE PACKET COUNTER [7:0]							
		15:8					RECEIVE UNKNOWN OPCODE PACKET COUNTER [11:8]			
		23:16								
		31:24								
0xBC	RALN	7:0	RECEIVE ALIGNMENT ERROR COUNTER [7:0]							
		15:8					RECEIVE ALIGNMENT ERROR COUNTER [11:8]			
		23:16								
		31:24								
0xC0	RFLR	7:0	RECEIVE FRAME LENGTH ERROR COUNTER [7:0]							
		15:8					RECEIVE FRAME LENGTH ERROR COUNTER [11:8]			
		23:16								
		31:24								
0xC4	RCDE	7:0	RECEIVE CODE ERROR COUNTER [7:0]							
		15:8					RECEIVE CODE ERROR COUNTER [11:8]			
		23:16								
		31:24								
0xC8	RCSE	7:0	RECEIVE CARRIER SENSE ERROR COUNTER [7:0]							
		15:8					RECEIVE CARRIER SENSE ERROR COUNTER [11:8]			
		23:16								
		31:24								
0xCC	RUND	7:0	RECEIVE UNDERSIZE PACKET COUNTER [7:0]							
		15:8					RECEIVE UNDERSIZE PACKET COUNTER [11:8]			
		23:16								
		31:24								
0xD0	ROVR	7:0	RECEIVE OVERSIZE PACKET COUNTER [7:0]							
		15:8					RECEIVE OVERSIZE PACKET COUNTER [11:8]			
		23:16								
		31:24								

MAC (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xD4	RFRG	7:0	RECEIVE FRAGMENTS COUNTER [7:0]							
		15:8	RECEIVE FRAGMENTS COUNTER [11:8]							
		23:16								
		31:24								
0xD8	RJBR	7:0	RECEIVE JABBER COUNTER [7:0]							
		15:8	RECEIVE JABBER COUNTER [11:8]							
		23:16								
		31:24								
0xDC	RDRP	7:0	RECEIVE DROP [7:0]							
		15:8	RECEIVE DROP [11:8]							
		23:16								
		31:24								
0xE0	TBYT	7:0	TRANSMIT BYTE COUNTER [7:0]							
		15:8	TRANSMIT BYTE COUNTER [15:8]							
		23:16	TRANSMIT BYTE COUNTER [23:16]							
		31:24								
0xE4	TPKT	7:0	TRANSMIT PACKET COUNTER [7:0]							
		15:8	TRANSMIT PACKET COUNTER [15:8]							
		23:16							TRANSMIT PACKET COUNTER [17:16]	
		31:24								
0xE8	TMCA	7:0	TRANSMIT MULTICAST PACKET COUNTER [7:0]							
		15:8	TRANSMIT MULTICAST PACKET COUNTER [15:8]							
		23:16							TRANSMIT MULTICAST PACKET COUNTER [17:16]	
		31:24								
0xEC	TBCA	7:0	TRANSMIT BROADCAST PACKET COUNTER [7:0]							
		15:8	TRANSMIT BROADCAST PACKET COUNTER [15:8]							
		23:16							TRANSMIT BROADCAST PACKET COUNTER [17:16]	
		31:24								
0xF0	TXPF	7:0	TRANSMIT PAUSE CONTROL FRAME COUNTER [7:0]							
		15:8	TRANSMIT PAUSE CONTROL FRAME COUNTER [11:8]							
		23:16								
		31:24								
0xF4	TDFR	7:0	TRANSMIT DEFERRAL PACKET COUNTER [7:0]							
		15:8	TRANSMIT DEFERRAL PACKET COUNTER [11:8]							
		23:16								
		31:24								
0xF8	TEDF	7:0	TRANSMIT EXCESSIVE DEFERRAL PACKET COUNTER [7:0]							
		15:8	TRANSMIT EXCESSIVE DEFERRAL PACKET COUNTER [11:8]							
		23:16								
		31:24								
0xFC	TSCL	7:0	TRANSMIT SINGLE COLLISION PACKET COUNTER [7:0]							
		15:8	TRANSMIT SINGLE COLLISION PACKET COUNTER [11:8]							
		23:16								
		31:24								
0x0100	TMCL	7:0	TRANSMIT MULTIPLE COLLISION PACKET COUNTER [7:0]							
		15:8	TRANSMIT MULTIPLE COLLISION PACKET COUNTER [11:8]							
		23:16								
		31:24								
0x0104	TLCL	7:0	TRANSMIT LATE COLLISION PACKET COUNTER [7:0]							
		15:8	TRANSMIT LATE COLLISION PACKET COUNTER [11:8]							
		23:16								
		31:24								

MAC (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0108	TXCL	7:0	TRANSMIT EXCESSIVE COLLISION PACKET COUNTER [7:0]							
		15:8					TRANSMIT EXCESSIVE COLLISION PACKET COUNTER [11:8]			
		23:16								
		31:24								
0x010C	TNCL	7:0	TRANSMIT TOTAL COLLISION COUNTER [7:0]							
		15:8					TRANSMIT TOTAL COLLISION COUNTER [11:8]			
		23:16								
		31:24								
0x0110 ... 0x0113	Reserved									
0x0114	TDRP	7:0	TRANSMIT DROP FRAME COUNTER [7:0]							
		15:8					TRANSMIT DROP FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x0118	TJBR	7:0	TRANSMIT JABBER FRAME COUNTER [7:0]							
		15:8					TRANSMIT JABBER FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x011C	TFCS	7:0	TRANSMIT FCS ERROR COUNTER [7:0]							
		15:8					TRANSMIT FCS ERROR COUNTER [11:8]			
		23:16								
		31:24								
0x0120	TXCF	7:0	TRANSMIT CONTROL FRAME COUNTER [7:0]							
		15:8					TRANSMIT CONTROL FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x0124	TOVR	7:0	TRANSMIT OVERSIZE FRAME COUNTER [7:0]							
		15:8					TRANSMIT OVERSIZE FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x0128	TUND	7:0	TRANSMIT UNDER SIZE FRAME COUNTER [7:0]							
		15:8					TRANSMIT UNDER SIZE FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x012C	TFRG	7:0	TRANSMIT FRAGMENTS FRAME COUNTER [7:0]							
		15:8					TRANSMIT FRAGMENTS FRAME COUNTER [11:8]			
		23:16								
		31:24								
0x0130	CAR1	7:0	CARRY REGISTER 1 RFLR COUNTER CARRY BIT	CARRY REGISTER 1 RCDE COUNTER CARRY BIT	CARRY REGISTER 1 RCSE COUNTER CARRY BIT	CARRY REGISTER 1 RUND COUNTER CARRY BIT	CARRY REGISTER 1 ROVR COUNTER CARRY BIT	CARRY REGISTER 1 RFRG COUNTER CARRY BIT	CARRY REGISTER 1 RJBR COUNTER CARRY BIT	CARRY REGISTER 1 RDRP COUNTER CARRY BIT
		15:8	CARRY REGISTER 1 RPKT COUNTER CARRY BIT	CARRY REGISTER 1 RFCS COUNTER CARRY BIT	CARRY REGISTER 1 RMCA COUNTER CARRY BIT	CARRY REGISTER 1 RBCA COUNTER CARRY BIT	CARRY REGISTER 1 RXCF COUNTER CARRY BIT	CARRY REGISTER 1 RXPF COUNTER CARRY BIT	CARRY REGISTER 1 RXUO COUNTER CARRY BIT	CARRY REGISTER 1 RALN COUNTER CARRY BIT
		23:16						CARRY REGISTER 1 RSBECC COUNTER CARRY BIT	CARRY REGISTER 1 RDBEDC COUNTER CARRY BIT	CARRY REGISTER 1 RBYT COUNTER CARRY BIT
		31:24	CARRY REGISTER 1 TR64 COUNTER CARRY BIT	CARRY REGISTER 1 TR127 COUNTER CARRY BIT	CARRY REGISTER 1 TR255 COUNTER CARRY BIT	CARRY REGISTER 1 TR511 COUNTER CARRY BIT	CARRY REGISTER 1 TR1K COUNTER CARRY BIT	CARRY REGISTER 1 TRMAX COUNTER CARRY BIT	CARRY REGISTER 1 TRMGV COUNTER CARRY BIT	

MAC (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0134	CAR2	7:0	CARRY REGISTER 2 TEDF COUNTER CARRY BIT	CARRY REGISTER 2 TSCL COUNTER CARRY BIT	CARRY REGISTER 2 TMCL COUNTER CARRY BIT	CARRY REGISTER 2 TLCL COUNTER CARRY BIT	CARRY REGISTER 2 TXCL COUNTER CARRY BIT	CARRY REGISTER 2 TNCL COUNTER CARRY BIT	CARRY REGISTER 2 TPFH COUNTER CARRY BIT	CARRY REGISTER 2 TDRP COUNTER CARRY BIT
		15:8	CARRY REGISTER 2 TUND COUNTER CARRY BIT	CARRY REGISTER 2 TFRG COUNTER CARRY BIT	CARRY REGISTER 2 TBYT COUNTER CARRY BIT	CARRY REGISTER 2 TPKT COUNTER CARRY BIT	CARRY REGISTER 2 TMCA COUNTER CARRY BIT	CARRY REGISTER 2 TBCA COUNTER CARRY BIT	CARRY REGISTER 2 TXPF COUNTER CARRY BIT	CARRY REGISTER 2 TDFR COUNTER CARRY BIT
		23:16			CARRY REGISTER 2 TSBECC COUNTER CARRY BIT	CARRY REGISTER 2 TDBEDC COUNTER CARRY BIT	CARRY REGISTER 2 TJBR COUNTER CARRY BIT	CARRY REGISTER 2 TXFC COUNTER CARRY BIT	CARRY REGISTER 2 TXCF COUNTER CARRY BIT	CARRY REGISTER 2 TOVR COUNTER CARRY BIT
		31:24								
0x0138	CAM1	7:0	MASK REGISTER 1 RFLR COUNTER CARRY BIT	MASK REGISTER 1 RCDE COUNTER CARRY BIT	MASK REGISTER 1 RCSE COUNTER CARRY BIT	MASK REGISTER 1 RUND COUNTER CARRY BIT	MASK REGISTER 1 ROVR COUNTER CARRY BIT	MASK REGISTER 1 RFRG COUNTER CARRY BIT	MASK REGISTER 1 RJBR COUNTER CARRY BIT	MASK REGISTER 1 RDRP COUNTER CARRY BIT
		15:8	MASK REGISTER 1 RPKT COUNTER CARRY BIT	MASK REGISTER 1 RFCS COUNTER CARRY BIT	MASK REGISTER 1 RMCA COUNTER CARRY BIT	MASK REGISTER 1 RBCA COUNTER CARRY BIT	MASK REGISTER 1 RXCF COUNTER CARRY BIT	MASK REGISTER 1 RXPF COUNTER CARRY BIT	MASK REGISTER 1 RXUO COUNTER CARRY BIT	MASK REGISTER 1 RALN COUNTER CARRY BIT
		23:16						MASK REGISTER 1 RSBECC COUNTER CARRY BIT	MASK REGISTER 1 RDBEDC COUNTER CARRY BIT	MASK REGISTER 1 RBYT COUNTER CARRY BIT
		31:24	MASK REGISTER 1 TR64 COUNTER CARRY BIT	MASK REGISTER 1 TR127 COUNTER CARRY BIT	MASK REGISTER 1 TR255 COUNTER CARRY BIT	MASK REGISTER 1 TR511 COUNTER CARRY BIT	MASK REGISTER 1 TR1K COUNTER CARRY BIT	MASK REGISTER 1 TRMAX COUNTER CARRY BIT	MASK REGISTER 1 TRMGV COUNTER CARRY BIT	
0x013C	CAM2	7:0	MASK REGISTER 2 TEDF COUNTER CARRY BIT	MASK REGISTER 2 TSCL COUNTER CARRY BIT	MASK REGISTER 2 TMCL COUNTER CARRY BIT	MASK REGISTER 2 TLCL COUNTER CARRY BIT	MASK REGISTER 2 TXCL COUNTER CARRY BIT	MASK REGISTER 2 TNCL COUNTER CARRY BIT	MASK REGISTER 2 TPFH COUNTER CARRY BIT	MASK REGISTER 2 TDRP COUNTER CARRY BIT
		15:8	MASK REGISTER 2 TUND COUNTER CARRY BIT	MASK REGISTER 2 TFRG COUNTER CARRY BIT	MASK REGISTER 2 TBYT COUNTER CARRY BIT	MASK REGISTER 2 TPKT COUNTER CARRY BIT	MASK REGISTER 2 TMCA COUNTER CARRY BIT	MASK REGISTER 2 TBCA COUNTER CARRY BIT	MASK REGISTER 2 TXPF COUNTER CARRY BIT	MASK REGISTER 2 TDFR COUNTER CARRY BIT
		23:16			MASK REGISTER 2 TSBECC COUNTER CARRY BIT	MASK REGISTER 2 TDBEDC COUNTER CARRY BIT	MASK REGISTER 2 TJBR COUNTER CARRY BIT	MASK REGISTER 2 TXFC COUNTER CARRY BIT	MASK REGISTER 2 TXCF COUNTER CARRY BIT	MASK REGISTER 2 TOVR COUNTER CARRY BIT
		31:24								
0x0140	TSBECC	7:0	TRANSMIT ECC SEC COUNTER [7:0]							
		15:8	TRANSMIT ECC SEC COUNTER [15:8]							
		23:16								
		31:24								
0x0144	TDBEDC	7:0	TRANSMIT ECC DED COUNTER [7:0]							
		15:8	TRANSMIT ECC DED COUNTER [15:8]							
		23:16								
		31:24								

MAC (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0148	RSBECC	7:0	RECEIVER ECC SEC COUNTER [7:0]							
		15:8	RECEIVER ECC SEC COUNTER [15:8]							
		23:16								
		31:24								
0x014C	RDBEDC	7:0	RECEIVER ECC DED COUNTER [7:0]							
		15:8	RECEIVER ECC DED COUNTER [15:8]							
		23:16								
		31:24								
0x0150 ... 0x01BF	Reserved									
0x01C0	Framefiltercontrols	7:0			FRAME FILTER CONTROLS[5:0]					
		15:8								
		23:16								
		31:24								
0x01C4	Hash_Table_Register0	7:0	HASH TABLE REGISTER0 [7:0]							
		15:8	HASH TABLE REGISTER0 [15:8]							
		23:16	HASH TABLE REGISTER0 [23:16]							
		31:24	HASH TABLE REGISTER0 [31:24]							
0x01C8	Hash_Table_Register1	7:0	HASH TABLE REGISTER1 [7:0]							
		15:8	HASH TABLE REGISTER1 [15:8]							
		23:16	HASH TABLE REGISTER1 [23:16]							
		31:24	HASH TABLE REGISTER1 [31:24]							
0x01CC	Hash_Table_Register2	7:0	HASH TABLE REGISTER2 [7:0]							
		15:8	HASH TABLE REGISTER2 [15:8]							
		23:16	HASH TABLE REGISTER2 [23:16]							
		31:24	HASH TABLE REGISTER2 [31:24]							
0x01D0	Hash_Table_Register3	7:0	HASH TABLE REGISTER3 [7:0]							
		15:8	HASH TABLE REGISTER3 [15:8]							
		23:16	HASH TABLE REGISTER3 [23:16]							
		31:24	HASH TABLE REGISTER3 [31:24]							
0x01D4	Misc_Control_register	7:0								
		15:8								
		23:16								
		31:24								
0x01D8	Misc_Status_register	7:0								
		15:8								
		23:16								
		31:24								

8.1.1. TXPF (Ask a Question)

Name: TXPF
Offset: 0x0F0
Reset: 0x0
Property: Read-only

TXPF- Transmit PAUSE Control Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT PAUSE CONTROL FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT PAUSE CONTROL FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT PAUSE CONTROL FRAME COUNTER [11:0] Incremented each time a valid PAUSE MAC Control frame is transmitted.

8.1.2. TXCL (Ask a Question)

Name: TXCL
Offset: 0x108
Reset: 0x0
Property: Read-only

TXCL- Transmit Excessive Collision Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT EXCESSIVE COLLISION PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT EXCESSIVE COLLISION PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT EXCESSIVE COLLISION PACKET COUNTER [11:0] Incremented for each frame that experienced 16 collisions during transmission and was aborted.

8.1.3. TXCF (Ask a Question)

Name: TXCF
Offset: 0x120
Reset: 0x0
Property: Read-only

TXCF- Transmit Control Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT CONTROL FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT CONTROL FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT CONTROL FRAME COUNTER [11:0] Incremented for every valid size frame with a Type Field signifying a Control frame.

8.1.4. TUND (Ask a Question)

Name: TUND
Offset: 0x128
Reset: 0x0
Property: Read-only

TUND- Transmit Under size Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT UNDER SIZE FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT UNDER SIZE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT UNDER SIZE FRAME COUNTER [11:0] Incremented for every frame less than 64 bytes, with a correct FCS value

8.1.5. TSCL (Ask a Question)

Name: TSCL
Offset: 0x0FC
Reset: 0x0
Property: Read-only

TSCL- Transmit Single Collision Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT SINGLE COLLISION PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT SINGLE COLLISION PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT SINGLE COLLISION PACKET COUNTER [11:0] Incremented for each frame transmitted which experienced exactly one collision during transmission.

8.1.6. TSBECC (Ask a Question)

Name: TSBECC
Offset: 0x140
Reset: 0x0
Property: Read-only

TSBECC Transmit ECC SEC Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TRANSMIT ECC SEC COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT ECC SEC COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TRANSMIT ECC SEC COUNTER [15:0] Incremented this counter whenever single bit error correct (SB_CORRECT) flag of transmit buffer memory is asserted.

8.1.7. TRMGV (Ask a Question)

Name: TRMGV
Offset: 0x098
Reset: 0x0
Property: Read-only

TRMGV-Transmit & Receive 1519 to 1522 Byte VLAN Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 1519 TO 1522 BYTE VLAN FRAME COUNTER [17:0] Incremented for each good VLAN frame transmitted and received which is 1519 to 1522 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.1.8. TRMAX (Ask a Question)

Name: TRMAX
Offset: 0x094
Reset: 0x0
Property: Read-only

TRMAX - Transmit & Receive 1024 to 1518 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 1024 TO 1518 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 1024 to 1518 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.1.9. TR64 (Ask a Question)

Name: TR64
Offset: 0x080
Reset: 0x0
Property: Read-only

TR64 - Transmit & Receive 64 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 64 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 64 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.1.10. TR511 (Ask a Question)

Name: TR511
Offset: 0x08C
Reset: 0x0
Property: Read-only

TR511 - Transmit & Receive 256 to 511 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 256 TO 511 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 256 to 511 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.1.11. TR255 (Ask a Question)

Name: TR255
Offset: 0x088
Reset: 0x0
Property: Read-only

TR255 - Transmit & Receive 128 to 255 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 128 TO 255 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 128 to 255 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.1.12. TR1K (Ask a Question)

Name: TR1K
Offset: 0x090
Reset: 0x0
Property: Read-only

TR1K - Transmit & Receive 512 to 1023 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 512 TO 1023 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 512 to 1023 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.1.13. TR127 (Ask a Question)

Name: TR127
Offset: 0x084
Reset: 0x0
Property: Read-only

TR127 - Transmit & Receive 65 to 127 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT AND RECEIVE 65 TO 127 BYTE FRAME COUNTER [17:0] Incremented for each good or bad frame transmitted and received which is 65 to 127 bytes in length inclusive (excluding framing bits but including FCS bytes).

8.1.14. TPKT (Ask a Question)

Name: TPKT
Offset: 0x0E4
Reset: 0x0
Property: Read-only

TPKT- Transmit Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT PACKET COUNTER [17:0] Incremented for each transmitted packet (including bad packets, excessive deferred packets, excessive collision packets, late collision packets, all Unicast, Broadcast, and Multicast packets).

8.1.15. TOVR (Ask a Question)

Name: TOVR
Offset: 0x124
Reset: 0x0
Property: Read-only

TOVR- Transmit Oversize Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT OVERSIZE FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT OVERSIZE FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT OVERSIZE FRAME COUNTER [11:0] Incremented for each oversized transmitted frame with a correct FCS value.

8.1.16. TNCL (Ask a Question)

Name: TNCL
Offset: 0x10C
Reset: 0x0
Property: Read-only

TNCL- Transmit Total Collision Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT TOTAL COLLISION COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT TOTAL COLLISION COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT TOTAL COLLISION COUNTER [11:0] Incremented by the number of collisions experienced during the transmission of a frame as defined as the simultaneous presence of signals on the DO and RD circuits (that is transmitting and receiving at the same time).

8.1.17. TMCL (Ask a Question)

Name: TMCL
Offset: 0x100
Reset: 0x0
Property: Read-only

TMCL- Transmit Multiple Collision Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT MULTIPLE COLLISION PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT MULTIPLE COLLISION PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT MULTIPLE COLLISION PACKET COUNTER [11:0] Incremented for each frame transmitted which experienced 2-15 collisions (including any late collisions.

8.1.18. TMCA (Ask a Question)

Name: TMCA
Offset: 0x0E8
Reset: 0x0
Property: Read-only

TMCA- Transmit Multicast Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT MULTICAST PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT MULTICAST PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT MULTICAST PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT MULTICAST PACKET COUNTER [17:0] Incremented for each Multicast valid frame transmitted (excluding Broadcast frames).

8.1.19. TLCL (Ask a Question)

Name: TLCL
Offset: 0x104
Reset: 0x0
Property: Read-only

TLCL- Transmit Late Collision Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT LATE COLLISION PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT LATE COLLISION PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT LATE COLLISION PACKET COUNTER [11:0] Incremented for each frame transmitted which experienced a late collision during a transmission attempt.

8.1.20. TJBR (Ask a Question)

Name: TJBR
Offset: 0x118
Reset: 0x0
Property: Read-only

TJBR-TransmitJabberFrameCounter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT JABBER FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT JABBER FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT JABBER FRAME COUNTER [11:0] Incremented for each oversized transmitted frame with an incorrect FCS value

8.1.21. TFRG (Ask a Question)

Name: TFRG
Offset: 0x12C
Reset: 0x0
Property: Read-only

TFRG- Transmit Fragments Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT FRAGMENTS FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT FRAGMENTS FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT FRAGMENTS FRAME COUNTER [11:0] Incremented for every frame less than 64 bytes, with an incorrect FCS value

8.1.22. TFCS (Ask a Question)

Name: TFCS
Offset: 0x11C
Reset: 0x0
Property: Read-only

TFCS- Transmit FCS Error Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT FCS ERROR COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT FCS ERROR COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT FCS ERROR COUNTER [11:0] Incremented for every valid sized packet with an incorrect FCS value.

8.1.23. Test_Register (Ask a Question)

Name: Test_Register
Offset: 0x01C
Reset: 0x0
Property: Read/Write

Test Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					MAXIMUM BACKOFF	REGISTERED TRANSMIT FLOW ENABL	TEST PAUSE	SHORTCUT SLOT TIME
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – MAXIMUM BACKOFF Setting this bit causes the MAC to back off for the maximum possible length of time. This test bit is used to predict back off times in Half_Duplex mode.

Bit 2 – REGISTERED TRANSMIT FLOW ENABL Transmit half_duplex Flow Enable.

Bit 1 – TEST PAUSE Setting this bit allows the MAC to be paused through the APB target interface for testing purposes

Bit 0 – SHORTCUT SLOT TIME Setting this bit allows the slot time counter to expire regardless of the current count. This bit is for testing purposes only. Upon PAUSE condition frame transmission gets paused until slot time counter reached h7e for 1G and h3e non 1G modes and it can be overcome by writing 1 to this bit.

8.1.24. TEDF (Ask a Question)

Name: TEDF
Offset: 0x0F8
Reset: 0x0
Property: Read-only

TEDF- Transmit Excessive Deferral Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT EXCESSIVE DEFERRAL PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT EXCESSIVE DEFERRAL PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT EXCESSIVE DEFERRAL PACKET COUNTER [11:0] Incremented for frames aborted which were deferred for an excessive period of time (3036 byte times).

8.1.25. TDRP (Ask a Question)

Name: TDRP
Offset: 0x114
Reset: 0x0
Property: Read-only

TDRP- Transmit Drop Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT DROP FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT DROP FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT DROP FRAME COUNTER [11:0] Incremented each time input PFH is asserted.

8.1.26. TDFR (Ask a Question)

Name: TDFR
Offset: 0x0F4
Reset: 0x0
Property: Read-only

TDFR- Transmit Deferral Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TRANSMIT DEFERRAL PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT DEFERRAL PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – TRANSMIT DEFERRAL PACKET COUNTER [11:0] Incremented for each frame, which was deferred on its first transmission attempt. Does not include frames involved in collisions.

8.1.27. TDBEDC (Ask a Question)

Name: TDBEDC
Offset: 0x144
Reset: 0x0
Property: Read-only

TDBEDC Transmit ECC DED Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TRANSMIT ECC DED COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT ECC DED COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TRANSMIT ECC DED COUNTER [15:0] Incremented this counter whenever double bit error detect (DB_DETECT) flag of transmit buffer memory is asserted.

8.1.28. TBYT (Ask a Question)

Name: TBYT
Offset: 0x0E0
Reset: 0x0
Property: Read-only

TBYT- Transmit Byte Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	TRANSMIT BYTE COUNTER [23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT BYTE COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT BYTE COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – TRANSMIT BYTE COUNTER [23:0] Incremented by the number of bytes that were put on the wire including fragments of frames that were involved with collisions. This count does not include preamble/SFD or jam bytes.

8.1.29. Station_Address_Lower_Register (Ask a Question)

Name: Station_Address_Lower_Register
Offset: 0x040
Reset: 0x0
Property: Read/Write

Station Address Lower Register

Bit	31	30	29	28	27	26	25	24
	FIRST OCTET OF THE DA IN THE FRAME[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SECOND OCTET OF THE DA IN THE FRAME[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	THIRD OCTET OF THE DA IN THE FRAME[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FOURTH OCTET OF THE DA IN THE FRAME[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:24 – FIRST OCTET OF THE DA IN THE FRAME[7:0]

Bits 23:16 – SECOND OCTET OF THE DA IN THE FRAME[7:0]

Bits 15:8 – THIRD OCTET OF THE DA IN THE FRAME[7:0]

Bits 7:0 – FOURTH OCTET OF THE DA IN THE FRAME[7:0]

8.1.30. TBCA (Ask a Question)

Name: TBCA
Offset: 0x0EC
Reset: 0x0
Property: Read-only

TBCA- Transmit Broadcast Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							TRANSMIT BROADCAST PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	TRANSMIT BROADCAST PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRANSMIT BROADCAST PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – TRANSMIT BROADCAST PACKET COUNTER [17:0] Incremented for each Broadcast frame transmitted (excluding Multicast frames).

8.1.31. Station_Address_Higher_Register (Ask a Question)

Name: Station_Address_Higher_Register
Offset: 0x044
Reset: 0x0
Property: Read/Write

Station Address Higher Register

Bit	31	30	29	28	27	26	25	24
	FIFTH OCTET OF THE DA IN THE FRAME[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SIXTH OCTET OF THE DA IN THE FRAME[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 31:24 – FIFTH OCTET OF THE DA IN THE FRAME[7:0]

Bits 23:16 – SIXTH OCTET OF THE DA IN THE FRAME[7:0]

8.1.32. RXUO (Ask a Question)

Name: RXUO
Offset: 0x0B8
Reset: 0x0
Property: Read-only

RXUO - Receive Unknown OPCode Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE UNKNOWN OPCODE PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE UNKNOWN OPCODE PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE UNKNOWN OPCODE PACKET COUNTER [11:0] Incremented each time a MAC Control Frame is received which contains an opcode other than a PAUSE.

8.1.33. RXPF (Ask a Question)

Name: RXPF
Offset: 0x0B4
Reset: 0x0
Property: Read-only

RXPF - Receive PAUSE Control Frame Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE PAUSE CONTROL FRAME COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE PAUSE CONTROL FRAME COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE PAUSE CONTROL FRAME COUNTER [11:0] Incremented each time a valid PAUSE MAC Control frame is received.

8.1.34. RXCF (Ask a Question)

Name: RXCF
Offset: 0x0B0
Reset: 0x0
Property: Read-only

RXCF - Receive Control Frame Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE CONTROL FRAME PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE CONTROL FRAME PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE CONTROL FRAME PACKET COUNTER [11:0] Incremented for each MAC Control frame received (PAUSE and Unsupported).

8.1.35. RUND (Ask a Question)

Name: RUND
Offset: 0x0CC
Reset: 0x0
Property: Read-only

RUND - Receive Undersize Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE UNDERSIZE PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE UNDERSIZE PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE UNDERSIZE PACKET COUNTER [11:0] Incremented each time a frame is received which is less than 64 bytes in length and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors.

8.1.36. RSBECC (Ask a Question)

Name: RSBECC
Offset: 0x148
Reset: 0x0
Property: Read-only

RSBECC Receiver ECC SEC Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RECEIVER ECC SEC COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVER ECC SEC COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RECEIVER ECC SEC COUNTER [15:0] Incremented this counter whenever single bit error correct (SB_CORRECT) flag of receiver buffer memory is asserted.

8.1.37. RPKT (Ask a Question)

Name: RPKT
Offset: 0x0A0
Reset: 0x0
Property: Read-only

RPKT- Receive Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RECEIVE PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	RECEIVE PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – RECEIVE PACKET COUNTER [17:0] Incremented for each frame received packet (including bad packets, all Unicast, Broadcast, and Multicast packets).

8.1.38. ROVR (Ask a Question)

Name: ROVR
Offset: 0x0D0
Reset: 0x0
Property: Read-only

ROVR - Receive Oversize Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE OVERSIZE PACKET COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE OVERSIZE PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE OVERSIZE PACKET COUNTER [11:0] Incremented each time a frame is received which exceeded 1518 (non VLAN) or 1522 (VLAN) and contains a valid FCS and were otherwise well formed. This does not look at Range Length errors.

8.1.39. RMCA (Ask a Question)

Name: RMCA
Offset: 0x0A8
Reset: 0x0
Property: Read-only

RMCA - Receive Multicast Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RECEIVE MULTICAST PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	RECEIVE MULTICAST PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE MULTICAST PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – RECEIVE MULTICAST PACKET COUNTER [17:0] Incremented for each Multicast good frame of lengths smaller than 1518 (non VLAN) or 1522 (VLAN) excluding Broadcast frames. This does not look at range/length errors.

8.1.40. RJBR (Ask a Question)

Name: RJBR
Offset: 0x0D8
Reset: 0x0
Property: Read-only

RJBR - Receive Jabber Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE JABBER COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE JABBER COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE JABBER COUNTER [11:0] Incremented for frames received which exceed 1518 (non VLAN) or 1522 (VLAN) bytes and contains an invalid FCS, includes alignment errors.

8.1.41. RFRG (Ask a Question)

Name: RFRG
Offset: 0x0D4
Reset: 0x0
Property: Read-only

RFRG -Receive Fragments Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE FRAGMENTS COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE FRAGMENTS COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE FRAGMENTS COUNTER [11:0] Incremented for each frame received which is less than 64 bytes in length and contains an invalid FCS, includes integral and non-integral lengths.

8.1.42. RFLR (Ask a Question)

Name: RFLR
Offset: 0x0C0
Reset: 0x0
Property: Read-only

RFLR - Receive Frame Length Error Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE FRAME LENGTH ERROR COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE FRAME LENGTH ERROR COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE FRAME LENGTH ERROR COUNTER [11:0] Incremented for each frame received in which the 802.3 length field did not match the number of data bytes actually received (46-1500 bytes). The counter is not incremented if the length field is not a valid 802.3 length, such as an EtherType value.

8.1.43. RFCS (Ask a Question)

Name: RFCS
Offset: 0x0A4
Reset: 0x0
Property: Read-only

RFCS - Receive FCS Error Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE FCS ERROR COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE FCS ERROR COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE FCS ERROR COUNTER [11:0] Incremented for each frame received that has an integral 64 to 1518 length and contains a Frame Check Sequence error.

8.1.44. RDRP (Ask a Question)

Name: RDRP
Offset: 0x0DC
Reset: 0x0
Property: Read-only

RDRP - Receive Drop

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE DROP [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE DROP [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE DROP [11:0] Incremented for frames received which are streamed to system but are later dropped due to lack of system resources.

8.1.45. RDBEDC (Ask a Question)

Name: RDBEDC
Offset: 0x14C
Reset: 0x0
Property: Read-only

RDBEDC Receiver ECC DED counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RECEIVER ECC DED COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVER ECC DED COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RECEIVER ECC DED COUNTER [15:0] Incremented this counter whenever double bit error detect (DB_DETECT) flag of receiver buffer memory is asserted.

8.1.46. RCSE (Ask a Question)

Name: RCSE
Offset: 0x0C8
Reset: 0x0
Property: Read-only

RCSE - Receive Carrier Sense Error Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE CARRIER SENSE ERROR COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE CARRIER SENSE ERROR COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE CARRIER SENSE ERROR COUNTER [11:0] Incremented each time a false carrier is detected during idle, as defined by a 1 on RXER and an 0xE on RXD. The event is reported along with the statistics generated on the next received frame. Only one false carrier condition can be detected and logged between frames

8.1.47. RCDE (Ask a Question)

Name: RCDE
Offset: 0x0C4
Reset: 0x0
Property: Read-only

RCDE- Receive Code Error Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE CODE ERROR COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE CODE ERROR COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE CODE ERROR COUNTER [11:0] Incremented each time a valid carrier was present and at least one invalid data symbol was detected.

8.1.48. RBYT (Ask a Question)

Name: RBYT
Offset: 0x09C
Reset: 0x0
Property: Read-only

RBYT - Receive Byte Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	RECEIVE BYTE COUNTER [23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RECEIVE BYTE COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE BYTE COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – RECEIVE BYTE COUNTER [23:0] The Statistic Counter register is incremented by the byte count of all frames received, including those in bad packets, excluding framing bits but including FCS bytes.

8.1.49. RBCA (Ask a Question)

Name: RBCA
Offset: 0x0AC
Reset: 0x0
Property: Read-only

RBCA - Receive Broadcast Packet Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RECEIVE BROADCAST PACKET COUNTER [17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	RECEIVE BROADCAST PACKET COUNTER [15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE BROADCAST PACKET COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – RECEIVE BROADCAST PACKET COUNTER [17:0] Incremented for each Broadcast good frame of lengths smaller than 1518 (non VLAN) or 1522 (VLAN) excluding Multicast frames. This does not look at range/length errors.

8.1.50. RALN (Ask a Question)

Name: RALN
Offset: 0x0BC
Reset: 0x0
Property: Read-only

RALN - Receive Alignment Error Counter

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RECEIVE ALIGNMENT ERROR COUNTER [11:8]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RECEIVE ALIGNMENT ERROR COUNTER [7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – RECEIVE ALIGNMENT ERROR COUNTER [11:0] Incremented for each received frame from 64 to 1518 which contains an invalid FCS and is not an integral number of bytes.

8.1.51. Misc_Status_register (Ask a Question)

Name: Misc_Status_register
Offset: 0x1D8
Reset: 0x0
Property: Read/Write

Misc Status register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

8.1.52. Misc_Control_register (Ask a Question)

Name: Misc_Control_register
Offset: 0x1D4
Reset: 0x0
Property: Read/Write

Misc Control register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

8.1.53. MIIMgmt_Status (Ask a Question)

Name: MIIMgmt_Status
Offset: 0x030
Reset: 0x0
Property: Read-only

MII Mgmt: Status

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	MDIO MGMT STATUS (PHY STATUS)[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MDIO MGMT STATUS (PHY STATUS)[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – MDIO MGMT STATUS (PHY STATUS)[15:0] Following an MDIO Mgmt Read Cycle, the 16 bit data can be read from this location.

8.1.54. MIIMgmt_Indicators (Ask a Question)

Name: MIIMgmt_Indicators
Offset: 0x034
Reset: 0x0
Property: Read-only

MII Mgmt: Indicators

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						NOT VALID	SCANNING	BUSY
Access						R	R	R
Reset						0	0	0

Bit 2 – NOT VALID When 1 is returned indicates MDIO Mgmt Read cycle has not completed and the Read Data is not yet valid.

Bit 1 – SCANNING When 1 is returned-indicates a scan operation (continuous MDIO Mgmt Read cycles) is in progress.

Bit 0 – BUSY When 1 is returned-indicates MDIO Mgmt block is currently performing an MDIO Mgmt Read or Write cycle.

8.1.55. MIIMgmt_Control (Ask a Question)

Name: MIIMgmt_Control
Offset: 0x02C
Reset: 0x0
Property: Write-only

MII Mgmt: Control

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	MDIO MGMT CONTROL (PHY CONTROL)[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MDIO MGMT CONTROL (PHY CONTROL)[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – MDIO MGMT CONTROL (PHY CONTROL)[15:0] When written, an MDIO Mgmt write cycle is performed using the 16-bit data and the preconfigured PHY and Register addresses from the MDIO Mgmt Address Register.

8.1.56. MIIMgmt_Configuration (Ask a Question)

Name: MIIMgmt_Configuration
Offset: 0x020
Reset: 0x0
Property: Read/Write

MII Mgmt: Configuration

Bit	31	30	29	28	27	26	25	24
	RESET MDIO MGMT							
Access	R/W							
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			SCAN AUTO INCREMENT	PREAMBLE SUPPRESSION		MGMT CLOCK SELECT[2:0]		
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bit 31 – RESET MDIO MGMT Setting this bit resets MDIO Mgmt. Clearing this bit allows MDIO Mgmt to perform Mgmt read or write cycles as requested via the APB target interface.

Bit 5 – SCAN AUTO INCREMENT Setting this bit causes MDIO Mgmt to continually read from a set of PHYs of contiguous address space. The starting address of the PHY is specified by the content of the PHY address field recorded in the MDIO Mgmt Address register. The next PHY to be read is PHY address + 1. The last PHY to be queried in this read sequence is the one residing at address 0x31, after which the read sequence returns to the PHY specified by the PHY address field.

Bit 4 – PREAMBLE SUPPRESSION Setting this bit causes MDIO Mgmt to suppress preamble generation and reduce the Mgmt cycle from 64 clocks to 32 clocks. This is in accordance with IEEE 802.3/22.2.4.4.2. Clearing this bit causes MDIO Mgmt to perform Mgmt read/write cycles with the 64 clocks of preamble.

Bits 2:0 – MGMT CLOCK SELECT[2:0]

Value	Description
3b000/3b001	Source clock divided by 4
3b010	Source clock divided by 6
3b011	Source clock divided by 8
3b100	Source clock divided by 10
3b101	Source clock divided by 14
3b110	Source clock divided by 20
3b111	Source clock divided by 28

8.1.57. MIIMgmt_Command (Ask a Question)

Name: MIIMgmt_Command
Offset: 0x024
Reset: 0x0
Property: Read/Write

MII Mgmt: Command

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							SCAN CYCLE	READ CYCLE
Access							R/W	R/W
Reset							0	0

Bit 1 – SCAN CYCLE This bit causes MDIO Mgmt to perform Read cycles continuously. This is useful for monitoring Link Fail.

Bit 0 – READ CYCLE This bit causes MDIO Mgmt to perform a single Read cycle. The Read data is returned in MDIO Mgmt STATUS Register.

8.1.58. MIIMgmt_Address (Ask a Question)

Name: MIIMgmt_Address
Offset: 0x028
Reset: 0x0
Property: Read/Write

MII Mgmt: Address

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				PHY ADDRESS[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				REGISTER ADDRESS[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 12:8 – PHY ADDRESS[4:0] This field represents the 5 bit PHY Address field used in Mgmt cycles. Up to 31 PHYs can be addressed.

Bits 4:0 – REGISTER ADDRESS[4:0] This field represents the 5 bit Register Address field of Mgmt cycles.

8.1.59. Maximum_Frame_Length (Ask a Question)

Name: Maximum_Frame_Length
Offset: 0x010
Reset: 0x7d0
Property: Read/Write

Maximum Frame Length

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	MAXIMUM FRAME LENGTH[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	MAXIMUM FRAME LENGTH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	0	1	0	0	0	0

Bits 15:0 – MAXIMUM FRAME LENGTH[15:0] This programmable field sets the maximum frame size in both the transmit and receive directions.The frame size includes the entire Layer 2 (L2) Ethernet frame, starting from the Destination MAC Address and ending with the Frame Check Sequence (FCS).

8.1.60. MACConfiguration2 (Ask a Question)

Name: MACConfiguration2
Offset: 0x004
Reset: 0x7200
Property: Read/Write

MAC Configuration # 2

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PREAMBLE LENGTH[3:0]						INTERFACE MODE[1:0]	
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	1	1	1			1	0

Bit	7	6	5	4	3	2	1	0
		RX CRC DISABLE	HUGE FRAME ENABLE	LENGTH FIELD CHECKING		PAD/CRC ENABLE	CRC ENABLE	FULL-DUPLEX
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bits 15:12 – PREAMBLE LENGTH[3:0] This field determines the length of the preamble field of the packet, in bytes. Minimum value supported for this field is 0x3.

Bits 9:8 – INTERFACE MODE[1:0]

Value	Description
2b00	MAC transmitter/receiver represents MII 10Mbps interface (Nibble Mode).
2b01	MAC transmitter/receiver represents MII 100Mbps interface (Nibble Mode).
2b10	MAC transmitter/receiver represents GMII 1000Mbps interface (Byte Mode).
2b11	Reserved.

Bit 6 – RX CRC DISABLE Setting this bit enables the removal of CRC bytes from all received frames at the MAC RX interface. Clearing this bit retains the CRC bytes at the end of each frame.

Bit 5 – HUGE FRAME ENABLE Setting this bit allows frames longer than the MAXIMUM FRAME LENGTH to be transmitted and received. Clear this bit to have the MAC limit the length of frames at the MAXIMUM FRAMELENGTH value. (Maximum Frame Length is set in separate Maximum Frame Length register.)

Bit 4 – LENGTH FIELD CHECKING Setting this bit causes the MAC to check the frame length field to ensure it matches the actual data field length. Clear this bit if no length field checking is desired.

Bit 2 – PAD/CRC ENABLE Set this bit to have the MAC pad all short frames and append a CRC to every frame whether or not padding was required. Clear this bit if frames presented to the MAC have a valid length and contain a CRC.

Bit 1 – CRC ENABLE Set this bit to have the MAC append a CRC to all frames. Clear this bit if frames presented to the MAC have a valid length and contain a valid CRC. If the PAD/CRC ENABLE Configuration bit or the per packet PAD/CRC ENABLE is set, CRC ENABLE is ignored.

Bit 0 – FULL-DUPLEX Setting this bit configures the MAC to operate in full duplex mode. Clearing this bit configures the MAC to operate in half duplex mode only.

8.1.61. MACConfiguration1 (Ask a Question)

Name: MACConfiguration1
Offset: 0x000
Reset: 0x80000000
Property: Read/Write

MAC Configuration # 1

Bit	31	30	29	28	27	26	25	24
	SOFT RESET							
Access	R/W							
Reset	1							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
								LOOP BACK
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
			RECEIVE FLOW CONTROL ENABLE	TRANSMIT FLOW CONTROL ENABLE	SYNCHRONIZED RECEIVE ENABLE	RECEIVE ENABLE	SYNCHRONIZED TRANSMIT ENABLE	TRANSMIT ENABLE
Access			R/W	R/W	R	R/W	R	R/W
Reset			0	0	0	0	0	0

Bit 31 – SOFT RESET Setting this bit puts all modules within the MAC in reset except the APB target interface.

Bit 8 – LOOP BACK Setting this bit causes the PETFN (Transmit Function) MAC Transmit outputs to be looped back to the MAC Receive inputs. Clearing this bit results in normal operation.

Bit 5 – RECEIVE FLOW CONTROL ENABLE Setting this bit causes the PERFN (Receive Function) Receive MAC Control to detect and act on PAUSE Flow Control frames. Clearing this bit causes the Receive MAC Control to ignore PAUSE Flow Control frames.

Bit 4 – TRANSMIT FLOW CONTROL ENABLE Setting this bit allows the PETMC Transmit MAC Control to send PAUSE Flow Control frames when requested by the system. Clearing this bit prevents the Transmit MAC Control from sending Flow Control frames.

Bit 3 – SYNCHRONIZED RECEIVE ENABLE Receive Enable synchronized to the receive stream.

Bit 2 – RECEIVE ENABLE Setting this bit allows the MAC to receive frames from the PHY. Clearing this bit prevents the reception of frames.

Bit 1 – SYNCHRONIZED TRANSMIT ENABLE Transmit Enable synchronized to the transmit stream.

Bit 0 – TRANSMIT ENABLE Setting this bit allows the MAC to transmit frames from the system. Clearing this bit prevents the transmission of frames.

8.1.62. IPG (Ask a Question)

Name: IPG
Offset: 0x08
Reset: 0x40605060
Property: Read/Write

IPG / IFG

Bit	31	30	29	28	27	26	25	24
		NON_BACK_TO_BACK INTER_PACKET_GAP PART1 (IPGR1)[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		NON_BACK_TO_BACK INTER_PACKET_GAP PART2 (IPGR2)[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MINIMUM IFG ENFORCEMENT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		BACK_TO_BACK INTER_PACKET_GAP[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	0	0	0	0	0

Bits 30:24 – NON_BACK_TO_BACK INTER_PACKET_GAP PART1 (IPGR1)[6:0] This programmable field represents the optional carrier sense window referenced in IEEE 802.3/4.2.3.2.1 Carrier Deference. If a carrier is detected during the timing of IPGR1, the MAC defers to the carrier. If, however, the carrier becomes active after IPGR1, the MAC continues timing IPGR2 and transmits, knowingly causing a collision. This ensures fair access to the medium. The permitted range of values is 0x0 to IPGR2. Default is 0x40 (64d) which follows the two-thirds/one-thirds guideline.

Bits 22:16 – NON_BACK_TO_BACK INTER_PACKET_GAP PART2 (IPGR2)[6:0] This programmable field represents the Non-Back-to-Back Inter-Packet-Gap in bit times. Default is 0x60 (96d), which represents the minimum IPG of 96 bits

Bits 15:8 – MINIMUM IFG ENFORCEMENT[7:0] Default 0x50. This programmable field represents the minimum size of IFG to enforce between frames(expressed in bit times). A frame whose IFG is less than that programmed is dropped. The default setting of 0x50 (80d) represents half of the nominal minimum IFG which is 160 bits.

Bits 6:0 – BACK_TO_BACK INTER_PACKET_GAP[6:0] Default 0x60. This programmable field represents the IPG between Back-to-Back packets (expressed in bit times). This is the IPG parameter used exclusively in full-duplex mode when two transmit packets are sent back-to-back. Set this field to the desired number of bits. The default setting of 0x60 (96d) represents the minimum IPG of 96 bits. Minimum value supported for this field is 0x28 (40d).

8.1.63. Interface_Status (Ask a Question)

Name: Interface_Status
Offset: 0x03C
Reset: 0x0
Property: Read-only

Interface Status

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						WAKE ON LANE DETECTED	EXCESS DEFER	
Access						R	R	
Reset						0	0	

Bit	7	6	5	4	3	2	1	0
					LINK FAIL			
Access					R			
Reset					0			

Bit 10 – WAKE ON LANE DETECTED This bit is only used when the optional WoL module is integrated It is set when the MAC detects a Magic Packet and stays high until it is cleared by the assertion of Wake On Lane Detected Clear. Its reset value is low.

Bit 9 – EXCESS DEFER This bit sets when the MAC excessively defers a transmission. It clears when read. This bit latches high. Excessive Deferred is a condition when the MAC has deferred sending a packet for a time longer than the length of two maximum length frames.

Bit 3 – LINK FAIL When read as a 1, the MDIO management module has read the PHY link fail register to be 1. When read as a 0, the MDIO management module has read the PHY link fail register to be 0. Note that for asynchronous host accesses, this bit must be read at least once every scan read cycle of the PHY.

8.1.64. Interface_Control (Ask a Question)

Name: Interface_Control
Offset: 0x038
Reset: 0x0
Property: Read/Write

Interface Control

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	WOL: UNICAST MATCH ENABLE	WOL: MAGIC PACKET DETECTION ENABLE	WOL: WAKE ON LANE DETECTED CLEAR STATUS CLEAR	STATS COUNTERS : AUTO CLEAR COUNTERS ON READ	STATS COUNTERS : CLEAR ALL COUNTERS	STATS COUNTERS : MODULE ENABLE		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit 7 – WOL: UNICAST MATCH ENABLE Setting this bit configures WoL module to enable Wake On Lane Detected assertion based on Unicast match.

Bit 6 – WOL: MAGIC PACKET DETECTION ENABLE Setting this bit configures WoL module to enable Wake On Lane Detected assertion based on magic packet detection.

Bit 5 – WOL: WAKE ON LANE DETECTED CLEAR STATUS CLEAR When this bit is asserted, Wake On Lane Detected status is held low. When this bit is cleared, Wake On Lane Detected may become asserted appropriately.

Bit 4 – STATS COUNTERS : AUTO CLEAR COUNTERS ON READ Setting this bit enables auto-clear-on-read feature for all the counters.

Bit 3 – STATS COUNTERS : CLEAR ALL COUNTERS Setting this bit clears all the statistics counters.

Bit 2 – STATS COUNTERS : MODULE ENABLE Setting this bit enables statistics counter module.

8.1.65. Hash_Table_Register3 (Ask a Question)

Name: Hash_Table_Register3
Offset: 0x1D0
Reset: 0x0
Property: Read/Write

Hash Table Register3

Bit	31	30	29	28	27	26	25	24
	HASH TABLE REGISTER3 [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	HASH TABLE REGISTER3 [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HASH TABLE REGISTER3 [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HASH TABLE REGISTER3 [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – HASH TABLE REGISTER3 [31:0] Hash Entries-[127:96]. Refer the Station Address Logic for Frame Filtering section of handbook for hash table utilization.

8.1.66. Hash_Table_Register2 (Ask a Question)

Name: Hash_Table_Register2
Offset: 0x1CC
Reset: 0x0
Property: Read/Write

Hash Table Register2

Bit	31	30	29	28	27	26	25	24
	HASH TABLE REGISTER2 [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	HASH TABLE REGISTER2 [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HASH TABLE REGISTER2 [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HASH TABLE REGISTER2 [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – HASH TABLE REGISTER2 [31:0] Hash Entries-[95:64]

8.1.67. Hash_Table_Register1 (Ask a Question)

Name: Hash_Table_Register1
Offset: 0x1C8
Reset: 0x0
Property: Read/Write

Hash Table Register1

Bit	31	30	29	28	27	26	25	24
	HASH TABLE REGISTER1 [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	HASH TABLE REGISTER1 [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HASH TABLE REGISTER1 [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HASH TABLE REGISTER1 [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – HASH TABLE REGISTER1 [31:0] Hash Entries-[63:32]

8.1.68. Hash_Table_Register0 (Ask a Question)

Name: Hash_Table_Register0
Offset: 0x1C4
Reset: 0x0
Property: Read/Write

Hash Table Register0

Bit	31	30	29	28	27	26	25	24
	HASH TABLE REGISTER0 [31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	HASH TABLE REGISTER0 [23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HASH TABLE REGISTER0 [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HASH TABLE REGISTER0 [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – HASH TABLE REGISTER0 [31:0] Hash Entries-[31:0]

8.1.69. Half-Duplex (Ask a Question)

Name: Half-Duplex
Offset: 0x00C
Reset: 0xa1f037
Property: Read/Write

Half-Duplex

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION[3:0]				ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE	BACKPRESSURE NO BACKOFF	NO BACKOFF	EXCESSIVE DEFER
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	1	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8
	RETRANSMISSION MAXIMUM[3:0]						COLLISION WINDOW[9:8]	
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	1	1	1	1			0	0

Bit	7	6	5	4	3	2	1	0
	COLLISION WINDOW[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	0	1	1	1

Bits 23:20 – ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION[3:0] This field is used when ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE is set. The value programmed is substituted for the Ethernet standard value of ten.

Bit 19 – ALTERNATE BINARY EXPONENTIAL BACKOFF ENABLE Setting this bit configures the transmitter MAC to use the ALTERNATE BINARY EXPONENTIAL BACKOFF TRUNCATION setting instead of the 802.3 standard tenth collisions. The Standard specifies that any collision after the tenth uses 210-1 as the maximum backoff time. Clearing this bit causes the transmitter MAC to follow the standard binary exponential backoff rule.

Bit 18 – BACKPRESSURE NO BACKOFF Setting this bit configures the transmitter MAC to immediately re-transmit following a collision during back pressure operation. Clearing this bit causes the transmitter MAC to follow the binary exponential back off rule.

Bit 17 – NO BACKOFF Setting this bit configures the transmitter MAC to immediately re-transmit following a collision. Clearing this bit causes the transmitter MAC to follow the binary exponential back off rule.

Bit 16 – EXCESSIVE DEFER Setting this bit configures the transmitter MAC to allow the transmission of a packet that has been excessively deferred. Clearing this bit causes the transmitter MAC to abort the transmission of a packet that has been excessively deferred.

Bits 15:12 – RETRANSMISSION MAXIMUM[3:0] This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the maximum number of attempts to be 0xF (15d).

Bits 9:0 – COLLISION WINDOW[9:0] This programmable field represents the slot time or collision window during which collisions might occur in a properly configured network. Since the collision window starts at the beginning of transmission, the preamble and SFD are included. The default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.

8.1.70. Framefiltercontrols (Ask a Question)

Name: Framefiltercontrols
Offset: 0x1C0
Reset: 0x0000003F
Property: Read/Write

Frame filter controls

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			FRAME FILTER CONTROLS[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 5:0 – FRAME FILTER CONTROLS[5:0]

Value	Description
[5]	Pass the frame if the hash table entry matches for Multicast-DA
[4]	Pass the frame if the hash table entry matches for Unicast-DA
[3]	Promiscuous mode, allow all the frames to pass
[2]	Pass the frame if its Unicast-DA matches the configured-DA
[1]	Pass all multicast frames
[0]	Pass all broadcast frames

8.1.71. Control_Frame_parameter (Ask a Question)

Name: Control_Frame_parameter
Offset: 0x018
Reset: 0xffff
Property: Read/Write

Control Frame parameter (Used for pause Value)

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	CFPT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	CFPT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – CFPT[15:0] This register bits are append as Pause frame payload.

8.1.72. Control_Frame_extended_parameter (Ask a Question)

Name: Control_Frame_extended_parameter
Offset: 0x014
Reset: 0x0
Property: Read/Write

Control Frame extended parameter (Used for pause frame)

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	CFEP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CFEP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CFEP[15:0] This register bits are append as Pause frame payload.

8.1.73. CAR2 (Ask a Question)

Name: CAR2
Offset: 0x134
Reset: 0x0
Property: Read/Write-1-to Clear

CAR2 - Carry Register Two Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			CARRY REGISTER 2 TSBECC COUNTER CARRY BIT	CARRY REGISTER 2 TDBEDC COUNTER CARRY BIT	CARRY REGISTER 2 TJBR COUNTER CARRY BIT	CARRY REGISTER 2 TXFC COUNTER CARRY BIT	CARRY REGISTER 2 TXCF COUNTER CARRY BIT	CARRY REGISTER 2 TOVR COUNTER CARRY BIT
Access			R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CARRY REGISTER 2 TUND COUNTER CARRY BIT	CARRY REGISTER 2 TFRG COUNTER CARRY BIT	CARRY REGISTER 2 TBYT COUNTER CARRY BIT	CARRY REGISTER 2 TPKT COUNTER CARRY BIT	CARRY REGISTER 2 TMCA COUNTER CARRY BIT	CARRY REGISTER 2 TBCA COUNTER CARRY BIT	CARRY REGISTER 2 TXPF COUNTER CARRY BIT	CARRY REGISTER 2 TDFR COUNTER CARRY BIT
Access	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CARRY REGISTER 2 TEDF COUNTER CARRY BIT	CARRY REGISTER 2 TSCL COUNTER CARRY BIT	CARRY REGISTER 2 TMCL COUNTER CARRY BIT	CARRY REGISTER 2 TLCL COUNTER CARRY BIT	CARRY REGISTER 2 TXCL COUNTER CARRY BIT	CARRY REGISTER 2 TNCL COUNTER CARRY BIT	CARRY REGISTER 2 TPFH COUNTER CARRY BIT	CARRY REGISTER 2 TDRP COUNTER CARRY BIT
Access	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0

Bit 21 – CARRY REGISTER 2 TSBECC COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Single Bit Error Correct Counter

Bit 20 – CARRY REGISTER 2 TDBEDC COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Double Bit Error Detect counter

Bit 19 – CARRY REGISTER 2 TJBR COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Jabber Frame Counter

Bit 18 – CARRY REGISTER 2 TXFC COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit FCS Error Counter

Bit 17 – CARRY REGISTER 2 TXCF COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Control Frame Counter

Bit 16 – CARRY REGISTER 2 TOVR COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Oversize Frame Counter

Bit 15 – CARRY REGISTER 2 TUND COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Under size Frame Counter

Bit 14 – CARRY REGISTER 2 TFRG COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Fragments Frame Counter

Bit 13 – CARRY REGISTER 2 TBYT COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Byte Counter

Bit 12 – CARRY REGISTER 2 TPKT COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Packet Counter

Bit 11 – CARRY REGISTER 2 TMCA COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Multicast Packet Counter

Bit 10 – CARRY REGISTER 2 TBCA COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Broadcast Packet Counter

Bit 9 – CARRY REGISTER 2 TXPF COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit PAUSE Control Frame Counter

Bit 8 – CARRY REGISTER 2 TDFR COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Deferral Packet Counter

Bit 7 – CARRY REGISTER 2 TEDF COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Excessive Deferral Packet Counter

Bit 6 – CARRY REGISTER 2 TSCL COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Single Collision Packet Counter

Bit 5 – CARRY REGISTER 2 TMCL COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Multiple Collision Packet Counter

Bit 4 – CARRY REGISTER 2 TLCL COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Late Collision Packet Counter

Bit 3 – CARRY REGISTER 2 TXCL COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Excessive Collision Packet Counter

Bit 2 – CARRY REGISTER 2 TNCL COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Total Collision Counter

Bit 1 – CARRY REGISTER 2 TPFH COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Pause Frames Honored Counter

Bit 0 – CARRY REGISTER 2 TDRP COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit Drop Frame Counter

8.1.74. CAR1 (Ask a Question)

Name: CAR1
Offset: 0x130
Reset: 0x0
Property: Read/Write-1-to Clear

CAR1 - Carry Register One

Bit	31	30	29	28	27	26	25	24
	CARRY REGISTER 1 TR64 COUNTER CARRY BIT	CARRY REGISTER 1 TR127 COUNTER CARRY BIT	CARRY REGISTER 1 TR255 COUNTER CARRY BIT	CARRY REGISTER 1 TR511 COUNTER CARRY BIT	CARRY REGISTER 1 TR1K COUNTER CARRY BIT	CARRY REGISTER 1 TRMAX COUNTER CARRY BIT	CARRY REGISTER 1 TRMGV COUNTER CARRY BIT	
Access	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	
Reset	0	0	0	0	0	0	0	

Bit	23	22	21	20	19	18	17	16
						CARRY REGISTER 1 RSBECC COUNTER CARRY BIT	CARRY REGISTER 1 RDBEDC COUNTER CARRY BIT	CARRY REGISTER 1 RBYT COUNTER CARRY BIT
Access						R/W1C	R/W1C	R/W1C
Reset						0	0	0

Bit	15	14	13	12	11	10	9	8
	CARRY REGISTER 1 RPKT COUNTER CARRY BIT	CARRY REGISTER 1 RFCS COUNTER CARRY BIT	CARRY REGISTER 1 RMCA COUNTER CARRY BIT	CARRY REGISTER 1 RBCA COUNTER CARRY BIT	CARRY REGISTER 1 RXCF COUNTER CARRY BIT	CARRY REGISTER 1 RXPF COUNTER CARRY BIT	CARRY REGISTER 1 RXUO COUNTER CARRY BIT	CARRY REGISTER 1 RALN COUNTER CARRY BIT
Access	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CARRY REGISTER 1 RFLR COUNTER CARRY BIT	CARRY REGISTER 1 RCDE COUNTER CARRY BIT	CARRY REGISTER 1 RCSE COUNTER CARRY BIT	CARRY REGISTER 1 RUND COUNTER CARRY BIT	CARRY REGISTER 1 ROVR COUNTER CARRY BIT	CARRY REGISTER 1 RFRG COUNTER CARRY BIT	CARRY REGISTER 1 RJBR COUNTER CARRY BIT	CARRY REGISTER 1 RDRP COUNTER CARRY BIT
Access	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0

Bit 31 – CARRY REGISTER 1 TR64 COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit and Receive 64 Byte Frame Counter

Bit 30 – CARRY REGISTER 1 TR127 COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit and Receive 65 to 127 Byte Frame Counter

Bit 29 – CARRY REGISTER 1 TR255 COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit and Receive 128 to 255 Byte Frame Counter

Bit 28 – CARRY REGISTER 1 TR511 COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit and Receive 256 to 511 Byte Frame Counter

Bit 27 – CARRY REGISTER 1 TR1K COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit and Receive 512 to 1023 Byte Frame Counter

Bit 26 – CARRY REGISTER 1 TRMAX COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit and Receive 1024 to 1518 Byte Frame Counter

Bit 25 – CARRY REGISTER 1 TRMGV COUNTER CARRY BIT Indicates the status of the Carry bit of Transmit and Receive 1519 to 1522 Byte VLAN Frame Counter

Bit 18 – CARRY REGISTER 1 RSBECC COUNTER CARRY BIT Indicates the status of the Carry bit of Receiver Single Bit Error Correct Counter

Bit 17 – CARRY REGISTER 1 RDBEDC COUNTER CARRY BIT Indicates the status of the Carry bit of Receiver Double Bit Error Detect Counter

Bit 16 – CARRY REGISTER 1 RBYT COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Byte Counter

Bit 15 – CARRY REGISTER 1 RPKT COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Packet Counter

Bit 14 – CARRY REGISTER 1 RFCS COUNTER CARRY BIT Indicates the status of the Carry bit of Receive FCS Error Counter

Bit 13 – CARRY REGISTER 1 RMCA COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Multicast Packet Counter

Bit 12 – CARRY REGISTER 1 RBCA COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Broadcast Packet Counter

Bit 11 – CARRY REGISTER 1 RXCF COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Control Frame Packet Counter

Bit 10 – CARRY REGISTER 1 RXPF COUNTER CARRY BIT Indicates the status of the Carry bit of Receive PAUSE Control Frame Counter

Bit 9 – CARRY REGISTER 1 RXUO COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Unknown OP code Packet Counter

Bit 8 – CARRY REGISTER 1 RALN COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Alignment Error Counter

Bit 7 – CARRY REGISTER 1 RFLR COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Frame Length Error Counter

Bit 6 – CARRY REGISTER 1 RCDE COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Code Error Counter

Bit 5 – CARRY REGISTER 1 RCSE COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Carrier Sense Error Counter

Bit 4 – CARRY REGISTER 1 RUND COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Undersize Packet Counter

Bit 3 – CARRY REGISTER 1 ROVR COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Oversize Packet Counter

Bit 2 – CARRY REGISTER 1 RFRG COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Fragments Counter

Bit 1 – CARRY REGISTER 1 RJBR COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Jabber Counter Receive Jabber Counter

Bit 0 – CARRY REGISTER 1 RDRP COUNTER CARRY BIT Indicates the status of the Carry bit of Receive Drop Counter

8.1.75. CAM2 (Ask a Question)

Name: CAM2
Offset: 0x13C
Reset: 0x3fffff
Property: Read/Write

CAM2 - Carry Register Two Mask Register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			MASK REGISTER 2 TSBECC COUNTER CARRY BIT	MASK REGISTER 2 TDBEDC COUNTER CARRY BIT	MASK REGISTER 2 TJBR COUNTER CARRY BIT	MASK REGISTER 2 TXFC COUNTER CARRY BIT	MASK REGISTER 2 TXCF COUNTER CARRY BIT	MASK REGISTER 2 TOVR COUNTER CARRY BIT
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	MASK REGISTER 2 TUND COUNTER CARRY BIT	MASK REGISTER 2 TFRG COUNTER CARRY BIT	MASK REGISTER 2 TBYT COUNTER CARRY BIT	MASK REGISTER 2 TPKT COUNTER CARRY BIT	MASK REGISTER 2 TMCA COUNTER CARRY BIT	MASK REGISTER 2 TBCA COUNTER CARRY BIT	MASK REGISTER 2 TXPF COUNTER CARRY BIT	MASK REGISTER 2 TDFR COUNTER CARRY BIT
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	MASK REGISTER 2 TEDF COUNTER CARRY BIT	MASK REGISTER 2 TSCL COUNTER CARRY BIT	MASK REGISTER 2 TMCL COUNTER CARRY BIT	MASK REGISTER 2 TLCL COUNTER CARRY BIT	MASK REGISTER 2 TXCL COUNTER CARRY BIT	MASK REGISTER 2 TNCL COUNTER CARRY BIT	MASK REGISTER 2 TPFH COUNTER CARRY BIT	MASK REGISTER 2 TDRP COUNTER CARRY BIT
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 21 – MASK REGISTER 2 TSBECC COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Single Bit Error Correct Counter.

Value	Description
0	Unmask the counter carry bit
1	Mask the counter carry bit.

Bit 20 – MASK REGISTER 2 TDBEDC COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Double Bit Error Detect counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 19 – MASK REGISTER 2 TJBR COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Jabber Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 18 – MASK REGISTER 2 TXFC COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit FCS Error Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 17 – MASK REGISTER 2 TXCF COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Control Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 16 – MASK REGISTER 2 TOVR COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Oversize Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 15 – MASK REGISTER 2 TUND COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Under size Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 14 – MASK REGISTER 2 TFRG COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Fragments Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 13 – MASK REGISTER 2 TBYT COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Byte Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 12 – MASK REGISTER 2 TPKT COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 11 – MASK REGISTER 2 TMCA COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Multicast Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 10 – MASK REGISTER 2 TBCA COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Broadcast Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 9 – MASK REGISTER 2 TXPF COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit PAUSE Control Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 8 – MASK REGISTER 2 TDFR COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Deferral Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 7 – MASK REGISTER 2 TEDF COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Excessive Deferral Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 6 – MASK REGISTER 2 TSCL COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Single Collision Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 5 – MASK REGISTER 2 TMCL COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Multiple Collision Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 4 – MASK REGISTER 2 TLCL COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Late Collision Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 3 – MASK REGISTER 2 TXCL COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Excessive Collision Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 2 – MASK REGISTER 2 TNCL COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Total Collision Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 1 – MASK REGISTER 2 TPFH COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Pause Frames Honored Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 0 – MASK REGISTER 2 TDRP COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit Drop Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

8.1.76. CAM1 (Ask a Question)

Name: CAM1
Offset: 0x138
Reset: 0xFE07FFFF
Property: Read/Write

CAM1 - Carry Register One Mask Register

Bit	31	30	29	28	27	26	25	24
	MASK REGISTER 1 TR64 COUNTER CARRY BIT	MASK REGISTER 1 TR127 COUNTER CARRY BIT	MASK REGISTER 1 TR255 COUNTER CARRY BIT	MASK REGISTER 1 TR511 COUNTER CARRY BIT	MASK REGISTER 1 TR1K COUNTER CARRY BIT	MASK REGISTER 1 TRMAX COUNTER CARRY BIT	MASK REGISTER 1 TRMGV COUNTER CARRY BIT	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	1	1	1	1	1	1	1	

Bit	23	22	21	20	19	18	17	16
						MASK REGISTER 1 RSBECC COUNTER CARRY BIT	MASK REGISTER 1 RDBEDC COUNTER CARRY BIT	MASK REGISTER 1 RBYT COUNTER CARRY BIT
Access						R/W	R/W	R/W
Reset						1	1	1

Bit	15	14	13	12	11	10	9	8
	MASK REGISTER 1 RPKT COUNTER CARRY BIT	MASK REGISTER 1 RFCS COUNTER CARRY BIT	MASK REGISTER 1 RMCA COUNTER CARRY BIT	MASK REGISTER 1 RBCA COUNTER CARRY BIT	MASK REGISTER 1 RXCF COUNTER CARRY BIT	MASK REGISTER 1 RXPF COUNTER CARRY BIT	MASK REGISTER 1 RXUO COUNTER CARRY BIT	MASK REGISTER 1 RALN COUNTER CARRY BIT
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	MASK REGISTER 1 RFLR COUNTER CARRY BIT	MASK REGISTER 1 RCDE COUNTER CARRY BIT	MASK REGISTER 1 RCSE COUNTER CARRY BIT	MASK REGISTER 1 RUND COUNTER CARRY BIT	MASK REGISTER 1 ROVR COUNTER CARRY BIT	MASK REGISTER 1 RFRG COUNTER CARRY BIT	MASK REGISTER 1 RJBR COUNTER CARRY BIT	MASK REGISTER 1 RDRP COUNTER CARRY BIT
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 31 – MASK REGISTER 1 TR64 COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit and Receive 64 Byte Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 30 – MASK REGISTER 1 TR127 COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit and Receive 65 to 127 Byte Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 29 – MASK REGISTER 1 TR255 COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit and Receive 128 to 255 Byte Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 28 – MASK REGISTER 1 TR511 COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit and Receive 256 to 511 Byte Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 27 – MASK REGISTER 1 TR1K COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit and Receive 512 to 1023 Byte Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 26 – MASK REGISTER 1 TRMAX COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit and Receive 1024 to 1518 Byte Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 25 – MASK REGISTER 1 TRMGV COUNTER CARRY BIT Mask or Unmask the carry bit of Transmit and Receive 1519 to 1522 Byte VLAN Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 18 – MASK REGISTER 1 RSBECC COUNTER CARRY BIT Mask or Unmask the carry bit of Receiver Single Bit Error Correct Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 17 – MASK REGISTER 1 RDBEDC COUNTER CARRY BIT Mask or Unmask the carry bit of Receiver Double Bit Error Detect counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 16 – MASK REGISTER 1 RBYT COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Byte Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 15 – MASK REGISTER 1 RPKT COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 14 – MASK REGISTER 1 RFCS COUNTER CARRY BIT Mask or Unmask the carry bit of Receive FCS Error Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 13 – MASK REGISTER 1 RMCA COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Multicast Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 12 – MASK REGISTER 1 RBCA COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Broadcast Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 11 – MASK REGISTER 1 RXCF COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Control Frame Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 10 – MASK REGISTER 1 RXPF COUNTER CARRY BIT Mask or Unmask the carry bit of Receive PAUSE Control Frame Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 9 – MASK REGISTER 1 RXUO COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Unknown OP code Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 8 – MASK REGISTER 1 RALN COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Alignment Error Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 7 – MASK REGISTER 1 RFLR COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Frame Length Error Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 6 – MASK REGISTER 1 RCDE COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Code Error Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 5 – MASK REGISTER 1 RCSE COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Carrier Sense Error Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 4 – MASK REGISTER 1 RUND COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Undersize Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 3 – MASK REGISTER 1 ROVR COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Oversize Packet Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 2 – MASK REGISTER 1 RFRG COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Fragments Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 1 – MASK REGISTER 1 RJBR COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Jabber Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

Bit 0 – MASK REGISTER 1 RDRP COUNTER CARRY BIT Mask or Unmask the carry bit of Receive Drop Counter.

Value	Description
0	Unmask the counter carry bit.
1	Mask the counter carry bit.

8.1.77. A-MCXFIFRAMAccess7 (Ask a Question)

Name: A-MCXFIFRAMAccess7
Offset: 0x07C
Reset: 0x0
Property: Read-only

A-MCXFIF FIFO RAM Access* Register 7

Bit	31	30	29	28	27	26	25	24
	HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[31:0])							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[31:0])							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[31:0])							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[31:0])							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[31:0]) Host receive RAM read data. This is the lower 4 bytes of receive FIFO RAM data that is read at the address of hstrramradx[RABITS:0] if hstrramradx[RABITS+2] is negated and hstrramreq is asserted. This is a read-only field. Writes specifically to this field have no effects.

8.1.78. A-MCXFIFRAMAccess6 (Ask a Question)

Name: A-MCXFIFRAMAccess6
Offset: 0x078
Reset: 0x0
Property: Read/Write

A-MCXFIF FIFO RAM Access* Register 6

Bit	31	30	29	28	27	26	25	24
	HOST RECEIVE RAM READ REQUEST (HSTRRAMRREQ)	HOST RECEIVE RAM READ ACKNOWLEDGE (HSTRRAMRACK)						
Access	R/W	R/W						
Reset	0	0						

Bit	23	22	21	20	19	18	17	16
	HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[39:32])							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			HOST RECEIVE RAM READ ADDRESS (HSTRRAMRADX[31:0])					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOST RECEIVE RAM READ ADDRESS (HSTRRAMRADX[31:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – HOST RECEIVE RAM READ REQUEST (HSTRRAMRREQ) Host receive RAM read request. Requests the handshake of hstrramradx values to the receive FIFO RAM and hstrramrdat from the receive FIFO RAM. Should only be asserted while hstrramrack is negated and while the receive data path isdisabled from receiving data and is in a steady state. It should only be negated after receiving an asserted hstrramrack.

Bit 30 – HOST RECEIVE RAM READ ACKNOWLEDGE (HSTRRAMRACK) Host receive RAM read acknowledge. Signifies the acceptance of hstrramradx values to the receive FIFO RAM and reception of hstrramrdat from the receive FIFO RAM location addressed. Will only be asserted or negated following assertion or negation of hstrramrreq. This is a readonly bit. Writes specifically to this bit have no effects.

Bits 23:16 – HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[39:32]) Host receive RAM read data. This is the upper byte of receive FIFO RAM data that was read at the address of hstrramwadx[RABITS:0] if hstrramwadx[RABITS+2] is negated and hstrramwreq is asserted. This part of the receive FIFO RAM contains control information for the frame as follows:

Value	Description
hstrramwdat [39:36]	unused.
hstrramwdat [35]	System receive start of frame.
hstrramwdat [34]	System receive end of frame.

HOST RECEIVE RAM READ DATA (HSTRRAMRDAT[39:32]) (continued)	
Value	**Description**
hstrramwdat [33:32]	Data valid byte enable and applicable only for the last word of the frame.
hstrramwdat [33:32] = 0	Indicates all bytes in the word are valid.
hstrramwdat [33:32] = 1	Indicates the LSB 3 bytes are valid [23:0] bits.
hstrramwdat [33:32] = 2	Indicates the LSB 2 bytes are valid [15:0] bits.
hstrramwdat [33:32] = 3	Indicates the LSB 1 bytes are valid [7:0] bits.

Bits 13:0 – HOST RECEIVE RAM READ ADDRESS (HSTRRAMRADX[31:0]) Host receive RAM read address. If hstrramradx[RABITS+2] is written low, hstrramradx[11:0] is the receive FIFO RAM address which hstrramrdat is read from. If hstrramradx[RABITS+2] is written high, hstrramradx[12:0] contains the pointer value read from abric receive module

8.1.79. A-MCXFIFRAMAccess5 (Ask a Question)

Name: A-MCXFIFRAMAccess5
Offset: 0x074
Reset: 0x0
Property: Read/Write

A-MCXFIF FIFO RAM Access* Register 5

Bit	31	30	29	28	27	26	25	24
	HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT [31:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT [31:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT [31:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT [31:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT [31:0]) Host receive RAM write data. This is the lower 4 bytes of receive FIFO RAM data that writes at the address of hstrramwadx[RABITS:0] if hsttramwadx[RABITS+2] is negated and hstrramwreq is asserted.

8.1.80. A-MCXFIFRAMAccess4 (Ask a Question)

Name: A-MCXFIFRAMAccess4
Offset: 0x070
Reset: 0x0
Property: Read/Write

A-MCXFIF FIFO RAM Access* Register 4

Bit	31	30	29	28	27	26	25	24
	HOST RECEIVE RAM WRITE REQUEST (HSTRRAMWREQ)	HOST RECEIVE RAM WRITE ACKNOWLEDGE (HSTRRAMWACK)						
Access	R/W	R						
Reset	0	0						

Bit	23	22	21	20	19	18	17	16
	HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT[39:32])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
		HOST RECEIVE RAM WRITE ADDRESS (HSTTRAMWADX[(RABITS+2):0])						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOST RECEIVE RAM WRITE ADDRESS (HSTTRAMWADX[(RABITS+2):0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – HOST RECEIVE RAM WRITE REQUEST (HSTRRAMWREQ) Host receive RAM write request. Requests the handshake of hstrramwdat and hstrramwadx values to the receive FIFO RAM. Only be asserted while hstrramwack is negated and while the receive data path is disabled from receiving data in a steady state.

Bit 30 – HOST RECEIVE RAM WRITE ACKNOWLEDGE (HSTRRAMWACK) Host receive RAM write acknowledge. Signifies the acceptance of hstrramwdat and hstrramwadx values to the receive FIFO RAM or System receive module. Will only be asserted or negated following assertion or negation of hstrramwreq. This is a read-only bit. Writes specifically to this bit no effects.

Bits 23:16 – HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT[39:32]) Host receive RAM write data. This is the upper byte of receive FIFO RAM data that is written at the address of hstrramwadx[RABITS:0] if hstrramwadx[RABITS+2] is negated and hstrramwreq is asserted. This part of the receive FIFO RAM contains control information for the frame as follows:

Value	Description
hstrramwdat [39:36]	unused
hstrramwdat [35]	System receive start of frame.
hstrramwdat [34]	System receive end of frame.
hstrramwdat [33:32]	data valid Byte enable and applicable only for the last word of the frame.

HOST RECEIVE RAM WRITE DATA (HSTRRAMWDAT[39:32]) (continued)	
Value	**Description**
hstrramwdat [33:32] = 0	Indicates all bytes in the word are valid.
hstrramwdat [33:32] = 1	Indicates the LSB 3 bytes are valid [23:0] bits.
hstrramwdat [33:32] = 2	Indicates the LSB 2 bytes are valid [15:0] bits.
hstrramwdat [33:32] = 3	Indicates the LSB 1 bytes are valid [7:0] bits.

Bits 14:0 – HOST RECEIVE RAM WRITE ADDRESS (HSTTRAMWADX[(RABITS+2):0]) Host receive RAM write address. This field has different functionality based on the value of hstrramwadx[RABITS+1] and whether it is being written to or read from. When read from, hstrramwadx[12:0] field contains the actual write pointer value of the System receieve module. When written to the hstrramwadx register is loaded. If hstrramwadx[RABITS+1] is low, hstrramwadx[11:0] receives FIFO RAM address which hstrramwdat is written to. If hstrramwadx[RABITS+2] is high, hstrramwadx[RABITS+1:0] contains the pointer value that is written to System receieve module.

8.1.81. A-MCXFIFRAMAccess3 (Ask a Question)

Name: A-MCXFIFRAMAccess3
Offset: 0x06C
Reset: 0x0
Property: Read-only

A-MCXFIF FIFO RAM Access* Register 3

Bit	31	30	29	28	27	26	25	24
	HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[31:0])							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[31:0])							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[31:0])							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[31:0])							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[31:0]) Host transmit RAM read data. This is the lower 4 bytes of transmit FIFO RAM data that is read at the address of hsttramradx[(TABITS-1):0] if hsttramradx[(TABITS+1)] is negated and hsttramrreq is asserted.This is a read-only field. Writes specifically to this field have no effects.

8.1.82. A-MCXFIFRAMAccess2 (Ask a Question)

Name: A-MCXFIFRAMAccess2
Offset: 0x068
Reset: 0x0
Property: Read/Write

A-MCXFIF FIFO RAM Access* Register 2

Bit	31	30	29	28	27	26	25	24
	HOST TRANSMIT RAM READ REQUEST. (HSTTRAMRREQ)	HOST TRANSMIT RAM READ ACKNOWLEDGE (HSTTRAMRACK)						
Access	R/W	R						
Reset	0	0						

Bit	23	22	21	20	19	18	17	16
	HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[39:32])							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				HOST TRANSMIT RAM READ ADDRESS (HSTTRAMRADX[12:0])				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOST TRANSMIT RAM READ ADDRESS (HSTTRAMRADX[12:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – HOST TRANSMIT RAM READ REQUEST. (HSTTRAMRREQ) Host transmit RAM read request. Requests the handshake of hsttramradx values to the transmit FIFO RAM and hsttramrdat from the transmit FIFO RAM. Should only be asserted while hsttramrack is negated and while the transmit data path is disabled from receiving data and is in a steady state. It should only be negated after receiving an asserted hsttramrack.

Bit 30 – HOST TRANSMIT RAM READ ACKNOWLEDGE (HSTTRAMRACK) Host transmit RAM read acknowledge. Signifies the acceptance of hsttramradx values to the transmit FIFO RAM and reception of hsttramrdat from the transmit FIFO RAM location addressed. Will only be asserted or negated following assertion or negation of hsttramrreq. This is a read-only bit. Writes specifically to this bit have no effects.

Bits 23:16 – HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[39:32]) Host transmit RAM read data. This is the upper byte of transmit FIFO RAM data that was read at the address of hsttramwadx[(TABITS-1):0] if hsttramwadx[(TABITS+1)] is negated and hsttramwreq is asserted. This part of the transmit FIFO RAM contains control information for the frame as follows:

Value	Description
hsttramrdat[39]	1/0 - Control Frame/ non control frame.
hsttramrdat[38:37]	FIFO receive Per-Packet PAD Mode.
hsttramrdat[38:37]	FIFO receive Per-Packet PAD Mode.

HOST TRANSMIT RAM READ DATA (HSTTRAMRDAT[39:32]) (continued)	
Value	**Description**
hsttramrdat[35]	FIFO receive Per-Packet Generate FCS.
hsttramrdat[34]	FIFO receive end of frame.
hsttramrdat[33:32]	Valid byte enables and applicable only for the last word of the frame.
hsttramrdat[33:32] = 0	Indicates all bytes in the word are valid.
hsttramrdat[33:32] = 1	Indicates the LSB 3 bytes are valid [23:0] bits.
hsttramrdat[33:32] = 2	Indicates the LSB 2 bytes are valid [15:0] bits.
hsttramrdat[33:32] = 3	Indicates the LSB 1 bytes are valid [7:0] bits.

Bits 12:0 – HOST TRANSMIT RAM READ ADDRESS (HSTTRAMRADX[12:0]) Host transmit RAM read address. If hsttramradx[TABITS+1] is written low, hsttramradx[(TABITS-1):0] is the transmit FIFO RAM address which hsttramrdat is read from. If hsttramradx[TABITS+1] is written high, hsttramradx[TABITS:0] contains the pointer value read from system transmit module.

8.1.83. A-MCXFIFRAMAccess1 (Ask a Question)

Name: A-MCXFIFRAMAccess1
Offset: 0x064
Reset: 0x0
Property: Read/Write

A-MCXFIF FIFO RAM Access* Register 1

Bit	31	30	29	28	27	26	25	24
	HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[31:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[31:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[31:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[31:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[31:0]) Host transmit RAM write data. This is the lower 4 bytes of transmit FIFO RAM data that is written at the address of hsttramwadx[(TABITS-1):0] if hsttramwadx[(TABITS+1)] is negated and hsttramwreq is asserted.

8.1.84. A-MCXFIFRAMAccess0 (Ask a Question)

Name: A-MCXFIFRAMAccess0
Offset: 0x060
Reset: 0x0
Property: Read/Write

A-MCXFIF FIFO RAM Access* Register 0

Bit	31	30	29	28	27	26	25	24
	HOST TRANSMIT RAM WRITE REQUEST (HSTTRAMWREQ)	HOST TRANSMIT RAM WRITE ACKNOWLEDGE (HSTTRAMWACK)						
Access	R/W	R						
Reset	0	0						

Bit	23	22	21	20	19	18	17	16
	HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[39:32])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				HOST TRANSMIT RAM WRITE ADDRESS (HSTTRAMWADX [12:0])				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOST TRANSMIT RAM WRITE ADDRESS (HSTTRAMWADX [12:0])							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – HOST TRANSMIT RAM WRITE REQUEST (HSTTRAMWREQ) Host transmit RAM write request. Requests the handshake of hsttramwdat and hsttramwadx values to the transmit FIFO RAM. Should only be asserted while hsttramwack is negated and while the transmit data path is disabled from receiving data and is in a steady state. It should only be negated after receiving an asserted hsttramwack.

Bit 30 – HOST TRANSMIT RAM WRITE ACKNOWLEDGE (HSTTRAMWACK) Host transmit RAM write acknowledge. Signifies the acceptance of hsttramwdat and hsttramwadx values to the transmit FIFO RAM or FIFO Transmit module. Will only be asserted or negated following assertion or negation of hsttramwreq. This is a read-only bit. Writes specifically to this bit have no effects.

Bits 23:16 – HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[39:32]) Host transmit RAM write data. This is the upper byte of transmit FIFO RAM data that is written at the address of hsttramwadx [(TABITS-1):0] if hsttramwadx [TABITS+1] is negated and hsttramwreq is asserted. This part of the transmit FIFO RAM contains control information for the frame as follows:

Value	Description
hsttramwdat[39]	FIFO Transmit Control Frame (1b1 for control frame).
hsttramwdat[38]	Reserved
hsttramwdat[37]	FIFO Transmit Per-Packet PAD Mode.
hsttramwdat[36]	FIFO Transmit Per-Packet enable.

HOST TRANSMIT RAM WRITE DATA (HSTTRAMWDAT[39:32]) (continued)	
Value	**Description**
hsttramwdat[35]	FIFO Transmit Per-Packet Generate FCS.
hsttramwdat[34]	FIFO Transmit end of packet.
hsttramwdat[33:32]	FIFO Transmit data valid, applicable only for the last word of the frame.
hsttramwdat[33:32] = 0	Indicates all bytes in the word are valid.
hsttramwdat[33:32] = 1	Indicates the LSB 3 bytes are valid [23:0] bits.
hsttramwdat[33:32] = 2	Indicates the LSB 2 bytes are valid [15:0] bits.
hsttramwdat[33:32] = 3	Indicates the LSB 1 bytes are valid [7:0] bits.

Bits 12:0 – HOST TRANSMIT RAM WRITE ADDRESS (HSTTRAMWADX [12:0]) Host transmit RAM write address. This field has different functionality based on the value of hsttramwadx [(TABITS+1)] and whether it is being written to or read from. When read from, hsttramwadx [TABITS:0] field contains the actual write pointer value of the FIFO Transmit module. When written to the hsttramwadx register is loaded. If hsttramwadx[TABITS+1] is low, hsttramwadx [(TABITS-1):0] transmits the RAM address which hsttramwdat is written to. If hsttramwadx [TABITS+1] is high, hsttramwadx [TABITS:0] contains the pointer value that is written to FIFO Transmit module.

8.1.85. A-MCXFIF5 (Ask a Question)

Name: A-MCXFIF5
Offset: 0x05C
Reset: 0xbfff7
Property: Read/Write

A-MCXFIF Configuration Register 5

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		HALF DUPLEX INDICATOR (CFGHDPLX)	SYSTEM RECEIVE FIFO FULL (SRFULL)	HOST CLEAR SYSTEM RECEIVE FIFO FULL (HSTSRFULLCLR)	ONE BYTE TRANSFER PER SYSTEM CLOCK (CFGBYTMODE)	HOST DROP FRAMES LESS THAN 64 BYTES (HSTDRPLT64)	HOST DONT CARE FOR FILTERING OF FRMES (HSTFLTRFRMDC) [17:16]	
Access		R/W	R	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	1	0	1	1

Bit	15	14	13	12	11	10	9	8
	HOST DONT CARE FOR FILTERING OF FRMES (HSTFLTRFRMDC) [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	HOST DONT CARE FOR FILTERING OF FRMES (HSTFLTRFRMDC) [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	1	1	1

Bit 22 – HALF DUPLEX INDICATOR (CFGHDPLX) Assertion of this bit configures the MAC-FIFO to enable half-duplex back pressure as a flow control mechanism. De-assertion of this bit configures the MAC-FIFO to enable pause frames as a flow control mechanism.

Bit 21 – SYSTEM RECEIVE FIFO FULL (SRFULL) Assertion of this read-only bit indicates that the maximum capacity of the receive FIFO storage has been met or exceeded.

Bit 20 – HOST CLEAR SYSTEM RECEIVE FIFO FULL (HSTSRFULLCLR) This bit should be written asserted when it is desired to clear the srfull indicator bit. After hstfullclr assertion, srfull should be read until it becomes unasserted. Hstfullclr should then be written unasserted for the indicator to become operational again.

Bit 19 – ONE BYTE TRANSFER PER SYSTEM CLOCK (CFGBYTMODE) This bit should be asserted when data is transferred at the tpd and rpd bus at a rate of one byte per qualified clock. This bit should be negated when data is transferred at the tpd and rpd bus at a rate of one nibble per qualified clock. This bit should therefore be asserted when the MAC is configured for GMII mode.

Bit 18 – HOST DROP FRAMES LESS THAN 64 BYTES (HSTDRPLT64) Setting this bit causes the frame to be dropped if a receive frame is less than 64 bytes in length

Bits 17:0 – HOST DONT CARE FOR FILTERING OF FRMES (HSTFLTRFRMDC) [17:0] The hstfltrfrmdc [17:0] configuration bits indicate which Receive Statistics Vectors are dont cares for MAC-FIFO frame drop circuitry. Setting of an hstfltrfrmdc bit, indicates a dont care for that hstfltrfrm bits. Clearing the bit looks for a matching level on the corresponding hstfltrfrm bit. If a match is made then the frame is dropped.

8.1.86. A-MCXFIF4 (Ask a Question)

Name: A-MCXFIF4
Offset: 0x058
Reset: 0x8
Property: Read/Write

A-MCXFIF Configuration Register 4

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							HOST FILTER FRAMES (HSTFLTRFRM) [17:16]	
Access							R/W	R/W
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	HOST FILTER FRAMES (HSTFLTRFRM) [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOST FILTER FRAMES (HSTFLTRFRM) [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	0	0	0

Bits 17:0 – HOST FILTER FRAMES (HSTFLTRFRM) [17:0]

Value	Description
17	Unicast frame detected but did not match configured station address.
16	Receive Frame Truncated.
15	Receive Long Event.
14	Receive VLAN Tag Detected: Frames length/type field contained 0x8100 which is the VLAN Protocol Identifier.
13	Receive Unsupported Op-code: Current Frame was recognized as a Control frame by the PEMCS, but it contains an unknown Op-code.
12	Receive PAUSE Control Frame: Current frame was recognized as a Control frame containing a valid PAUSE Frame Op-code and a valid address.
11	Receive Control Frame: Current Frame was recognized as a Control frame for having a valid Type-Length designation.
10	Receive Dribble Nibble: Indicates that after the end of the packet an additional 1 to 7 bits were received. A single nibble, called the dribble nibble, is formed but not sent to the system (10/100 Mbps only).
9	Receive Broadcast: Packets destination address contained the broadcast address.
8	Receive Multicast: Packets destination address contained a multicast address.
7	Receive OK. Frame contained a valid CRC and did not have a code error.

HOST FILTER FRAMES (HSTFLTRFRM) (continued)	
Value	**Description**
6	Receive Length Out of Range: Indicates that frames length was larger than 1,518 bytes but smaller than the hosts maximum frame length value (type field).
5	Receive Length Check Error: Indicates that frame length field value in the packet does not match the actual data byte length and is not a type field.
4	Receive CRC Error: Packets CRC did not match the internally generated CRC.
3	Receive Code Error: One or more nibbles were signaled as errors during the reception of the packet.
2	Receive False Carrier: Indicates that at some time since the last receive statistics vector, a false carrier was detected, noted, and reported with this the next receive statistics. The false carrier is not associated with this packet. False carrier is an activity on the receive channel that does not result in a packet receive attempt being made. Defined to be RXER = 1, RXDV = 0, RXD[3:0] = 0xE (RXD[7:0] = 0x0E).
1	Receive RXDV Event: Indicates that the last receive event seen was not long enough to be a valid packet.
0	Receive Previous Packet Dropped as IFG is small.

8.1.87. A-MCXFIF3 (Ask a Question)

Name: A-MCXFIF3
Offset: 0x054
Reset: 0xfff0fff
Property: Read/Write

A-MCXFIF Configuration Register 3

Bit	31	30	29	28	27	26	25	24
				MIN WORDS IN RECEIVE FIFO BEFORE (CFGLWM) [12:8]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	MIN WORDS IN RECEIVE FIFO BEFORE (CFGLWM) [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
				FABRIC TRANSMIT CUT THROUGH THRESHOLD (CFGFTTH) [12:8]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	FABRIC TRANSMIT CUT THROUGH THRESHOLD (CFGFTTH) [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 28:16 – MIN WORDS IN RECEIVE FIFO BEFORE (CFGLWM) [12:0] This hex value represents the maximum number of 4 byte locations that simultaneously stores in the transmit RAM before MTXHWM asserts. Note that MTXHWM has two MTXCLK clock periods of latency before assertion or negation. This should be considered when calculating any headroom required for maximum size packets. The register length is shown for a transmit RAM with 11 address bits (8KB). The register length varies with the configured transmit RAM size.

Bits 12:0 – FABRIC TRANSMIT CUT THROUGH THRESHOLD (CFGFTTH) [12:0] Once the transmit FIFO reaches the cut through threshold (cfgftth), MAC core informs to start frame transmission. Each hex value represents 4 byte locations that simultaneously stores in the transmit RAM.

8.1.88. A-MCXFIF1 (Ask a Question)

Name: A-MCXFIF1
Offset: 0x04C
Reset: 0xffffffff
Property: Read/Write

A-MCXFIF Configuration Register 1

Bit	31	30	29	28	27	26	25	24
					SYSTEM RECEIVE FOR CUT THROUGH THRESHOLD (CFGSRTH) [11:8]			
Access					R/W	R/W	R/W	R/W
Reset					1	1	1	1

Bit	23	22	21	20	19	18	17	16
	SYSTEM RECEIVE FOR CUT THROUGH THRESHOLD (CFGSRTH) [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	NUMBER OF PAUSE QUANTAS BEFORE XOFF RETRANSMISSION (CFGXOFFRTX) [15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	NUMBER OF PAUSE QUANTAS BEFORE XOFF RETRANSMISSION (CFGXOFFRTX) [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 27:16 – SYSTEM RECEIVE FOR CUT THROUGH THRESHOLD (CFGSRTH) [11:0] This hex value represents the minimum number of 4 byte locations that simultaneously stores in the receive RAM, relative to the beginning of the frame being input, before fabric-receive-ready signal (frrdy) may be asserted. Note that frrdy latents a certain amount of time due to fabric transmit clock to system transmit clock time domain crossing, and conditional on fabric-receiveaccept signal (fracpt) assertion. When set to maximum value, frrdy may be asserted only after the completion of the input frame. The value of this register must be greater than 18d when hstdrplt64 is asserted. The register length is shown for a receive RAM with 12 address bits (16KB).

Bits 15:0 – NUMBER OF PAUSE QUANTAS BEFORE XOFF RETRANSMISSION (CFGXOFFRTX) [15:0] This hex value represents the number of pause quanta (64 bit times) after an XOFF pause frame has been acknowledged until the MAC-FIFO re-asserts Transmit-Control Frame-Request (tcrq) if the MAC-FIFO receive storage level has remained higher than the low watermark.

8.1.89. A-MCXFIF2 (Ask a Question)

Name: A-MCXFIF2
Offset: 0x050
Reset: 0x1fff1fff
Property: Read/Write

A-MCXFIF Configuration Register 2

Bit	31	30	29	28	27	26	25	24
				MAX WORDS IN RECEIVE FIFO (CFGHWM) [12:8]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	MAX WORDS IN RECEIVE FIFO (CFGHWM) [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
				MIN WORDS IN RECEIVE FIFO BEFORE (CFGLWM) [12:8]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	MIN WORDS IN RECEIVE FIFO BEFORE (CFGLWM) [7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 28:16 – MAX WORDS IN RECEIVE FIFO (CFGHWM) [12:0] Once the receive FIFO reach the configured water mark level (cfghwm) MAC-FIFO sends XOFF pause control frame. Each hex value represents 4 byte locations that simultaneously stores in the receive RAM.

Bits 12:0 – MIN WORDS IN RECEIVE FIFO BEFORE (CFGLWM) [12:0] Once the receive RAM reaches the cfglwm, XON (transmit ON) pause control frame transmits in response to a previously transmitted XOFF pause control frame. Each hex value represents 4 byte locations that simultaneously stores in the receive RAM.

8.1.90. A-MCXFIF0 (Ask a Question)

Name: A-MCXFIF0
Offset: 0x048
Reset: 0x1f
Property: Read/Write

A-MCXFIF Configuration Register 0

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
				FABRIC TRANSMIT MODULE ENABLE STATUS (FTFENRPLY)	SYSTEM TRANSMIT MODULE ENABLE STATUS (STFENRPLY)	FABRIC RECEIVE MODULE ENABLE STATUS (FRFENRPLY)	SYSTEM RECEIVE MODULE ENABLE STATUS (SRFENRPLY)	WATER MARK MODULE ENABLE STATUS(WTMENRPLY)
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				FABRIC TRANSMIT MODULE ENABLE REQUEST(FTFENREQ)	SYSTEM TRANSMIT MODULE ENABLE REQUEST (STFENREQ)	FABRIC RECEIVE MODULE ENABLE REQUEST(FRFENREQ)	SYSTEM RECEIVE MODULE ENABLE REQUEST(SRFENREQ)	WATER MARK MODULE ENABLE REQUEST(WTMENREQ)
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				HOST FABRIC TRANSMIT MODULE RESET (HSTRSTFT)	HOST MAC TRANSMIT MODULE RESET (HSTRSTST)	HOST FABRIC RECEIVE MODULE RESET (HSTRSTFR)	HOST MAC RECEIVE MODULE RESET (HSTRSTSR)	HOST TRANSMIT WATERMARK MODULE RESET (HSTRSTWT)
Access				R/W	R/W	R/W	R/W	R/W
Reset				1	1	1	1	1

Bit 20 – FABRIC TRANSMIT MODULE ENABLE STATUS (FTFENRPLY) When asserted, the Fabric transmit module is enabled. When negated, the Fabric transmit module is disabled. The bit should be polled until it reaches the expected value.

Bit 19 – SYSTEM TRANSMIT MODULE ENABLE STATUS (STFENRPLY) When asserted, the System transmit module is enabled. When negated, the System transmit module is disabled. The bit should be polled until it reaches the expected value.

Bit 18 – FABRIC RECEIVE MODULE ENABLE STATUS (FRFENRPLY) When asserted, the Fabric receive module is enabled. When negated, the Fabric receive module is disabled. The bit should be polled until it reaches the expected value.

Bit 17 – SYSTEM RECEIVE MODULE ENABLE STATUS (SRFENRPLY) When asserted, the System receive module is enabled and start of packet has been received. When negated, the System receive module is disabled and end-of-frame signal is received.

Bit 16 – WATER MARK MODULE ENABLE STATUS(WTMENRPLY) When asserted, the Water mark module is enabled. When negated, the Water mark module is disabled. The bit should be polled until it reaches the expected value.

Bit 12 – FABRIC TRANSMIT MODULE ENABLE REQUEST(FTFENREQ) When asserted, requests enabling of the Fabric transmit module. When negated, requests disabling of the Fabric transmit module.

Bit 11 – SYSTEM TRANSMIT MODULE ENABLE REQUEST (STFENREQ) When asserted, requests enabling of the System transmit module.

Bit 10 – FABRIC RECEIVE MODULE ENABLE REQUEST(FRFENREQ) When asserted, requests enabling of the Fabric receive module.

Bit 9 – SYSTEM RECEIVE MODULE ENABLE REQUEST(SRFENREQ) When asserted, requests enabling of the System receive module. When negated, requests disabling of the System receive module.

Bit 8 – WATER MARK MODULE ENABLE REQUEST(WTMENREQ) When asserted, requests enabling of the Water mark module. When negated, requests disabling of tark module.

Bit 4 – HOST FABRIC TRANSMIT MODULE RESET (HSTRSTFT) When asserted this bit places fabric transmit module in reset.

Bit 3 – HOST MAC TRANSMIT MODULE RESET (HSTRSTST) When asserted this bit places the System transmit module in reset.

Bit 2 – HOST FABRIC RECEIVE MODULE RESET (HSTRSTFR) When asserted this bit places the fabric receive module in reset.

Bit 1 – HOST MAC RECEIVE MODULE RESET (HSTRSTSR) When asserted this bit places the System receive module in reset.

Bit 0 – HOST TRANSMIT WATERMARK MODULE RESET (HSTRSTWT) When asserted this bit places the transmit watermark module in reset.

8.2. MDIO (Ask a Question)

This section provides the MDIO register descriptions of the CoreTSE.

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	Control	7:0								
		15:8	PHY RESET	LOOP BACK		AUTO-NEGOTIATION ENABLE			RESTART AUTO-NEGOTIATION	
0x01	Status	7:0		MF PREMABLE SUPPRESSION ENABLE	AUTO-NEGOTIATION COMPLETE	REMOTE FAULT	AUTO-NEGOTIATION ABILITY	LINK STATUS		EXTENDED CAPABILITY
		15:8								EXTENDED STATUS
0x03	Reserved									
0x04	AN_Advertisement(1000BASE-T)	7:0	THESE BITS MUST ALWAYS BE WRITTEN 0000000001 FOR TBI OPERATION.[7:0]							
		15:8	LINK UP	ACK		FULL-DUPLEX	LINK SPEED[1:0]		THESE BITS MUST ALWAYS BE WRITTEN 0000000001 FOR TBI OPERATION.[9:8]	
0x05	AN_Link_Partner_Base_Page_Ability(1000BASE-T)	7:0	THESE BITS MUST ALWAYS BE WRITTEN 0000000001 FOR TBI OPERATION[7:0]							
		15:8	LINK UP	AUTO-NEGOTIATION ACK AS SPECIFIED IN 802.3Z		FULL-DUPLEX	LINK SPEED[1:0]		THESE BITS MUST ALWAYS BE WRITTEN 0000000001 FOR TBI OPERATION[9:8]	
0x06	AN_Expansion(1000BASE-T)	7:0						NEXT PAGE ABLE	PAGE RECEIVED	
		15:8								
0x07	AN_Next_Page_Transmit(1000BASE-X)	7:0	MESSAGE/UNFORMATTED CODE FIELD[7:0]							
		15:8	NEXT PAGE		MESSAGE PAGE	ACKNOWLEDGE 2	TOGGLE	MESSAGE/UNFORMATTED CODE FIELD[10:8]		
0x08	AN_Link_Partner_Ability_Next_Page(1000BASE-X)	7:0	MESSAGE OR UNFORMATTED CODE FIELD[7:0]							
		15:8	NEXT PAGE		MESSAGE PAGE	ACKNOWLEDGE 2	TOGGLE	MESSAGE OR UNFORMATTED CODE FIELD[10:8]		
0x0A ... 0x0E	Reserved									
0x0F	Extended_Status	7:0								
		15:8	1000BASE-X FULL-DUPLEX	1000BASE-X HALF-DUPLEX	1000BASE-T FULL-DUPLEX	1000BASE-T HALF-DUPLEX				
0x10	Jitter_Diagnostics	7:0	CUSTOM JITTER PATTERN[7:0]							
		15:8	JITTER DIAGNOSTIC ENABLE	JITTER PATTERN SELECT[2:0]					CUSTOM JITTER PATTERN[9:8]	
0x11	SGMII Ten_Bit_Interface_Control	7:0								
		15:8	SOFT RESET	SHORTCUT LINK TIMER	DISABLE RECEIVE RUNNING DISPARITY	DISABLE TRANSMIT RUNNING DISPARITY	GO LINK TIMER VALUE CONTROL			AUTO-NEGOTIATION SENSE

8.2.1. Status (Ask a Question)

Name: Status
Offset: 0x001
Reset: 0x149
Property: Read-only

Status

Bit	15	14	13	12	11	10	9	8
								EXTENDED STATUS
Access								R
Reset								1

Bit	7	6	5	4	3	2	1	0
		MF PREMABLE SUPPRESSION ENABLE	AUTO-NEGOTIATION COMPLETE	REMOTE FAULT	AUTO-NEGOTIATION ABILITY	LINK STATUS		EXTENDED CAPABILITY
Access		R	R	R	R	R		R
Reset		1	0	0	1	0		1

Bit 8 – EXTENDED STATUS This bit indicates that PHY status information is also contained in Register 0x0F:EXTENDED STATUS.

Bit 6 – MF PREMABLE SUPPRESSION ENABLE This bit indicates whether the PHY is capable of handling MDIO management Frames without the 32-bit preamble field. Returns 1 indicating support for suppressed preamble MDIO management Frames

Bit 5 – AUTO-NEGOTIATION COMPLETE When 1, this bit indicates that the Auto-negotiation process has completed. This bit returns 0 when either the Auto-negotiation process is underway or when the Auto-negotiation function is disabled.

Bit 4 – REMOTE FAULT When 1, a remote Fault condition has been detected between the TBI and the PHY.

Bit 3 – AUTO-NEGOTIATION ABILITY When 1, this bit indicates that the TBI has the ability to perform Auto-negotiation.

Bit 2 – LINK STATUS When 1, this bit indicates that a valid link has been established between the TBI and the PHY. When 0, no valid link has been established.

Bit 0 – EXTENDED CAPABILITY This bit indicates that the TBI contains the extended set of registers.

8.2.2. SGMII Ten_Bit_Interface_Control (Ask a Question)

Name: SGMII Ten_Bit_Interface_Control
Offset: 0x011
Reset: 0x0
Property: Read/Write

SGMII/Ten Bit Interface Control

Bit	15	14	13	12	11	10	9	8
	SOFT RESET	SHORTCUT LINK TIMER	DISABLE RECEIVE RUNNING DISPARITY	DISABLE TRANSMIT RUNNING DISPARITY	GO LINK TIMER VALUE CONTROL			AUTO-NEGOTIATION SENSE
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	0	0	0	0	0			0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – SOFT RESET This bit resets the functional modules in the TBI. Clear it for normal operation.

Bit 14 – SHORTCUT LINK TIMER Set this bit 1 to reduce the value of Go Link Timer and Sync. Status Fail Timer to 64 clock pulse. Ultimately this reduces the amount of simulation time needed to time the 1.6ms Link Timer. Clear it for normal operation. In normal operation the value of Go Link Timer is 200000 clock pulses and the value of the Sync. Status Fail Timer is 1250000 clock pulses.

Bit 13 – DISABLE RECEIVE RUNNING DISPARITY Set this bit to disable the running disparity calculation and checking in the receive direction. This bit must be 0 for TBI operation

Bit 12 – DISABLE TRANSMIT RUNNING DISPARITY Set this bit to disable the running disparity calculation and checking in the transmit direction. This bit must be 0 for TBI operation.

Bit 11 – GO LINK TIMER VALUE CONTROL When 0 the Go Link Timer Value=1.6 ms. When set to 1 the Go Link Timer Value=10 ms

Bit 8 – AUTO-NEGOTIATION SENSE Set this bit to allow the Auto-Negotiation function to sense either a MAC in Auto-Negotiation bypass mode or an older MAC without Auto-Negotiation capability. When sensed, AutoNegotiation Complete becomes true; however Page Received is low, indicating no page was exchanged. Management can then act accordingly. Clear this bit when IEEE 802.3z Clause 37 behaviour is desired, which results in the link not coming up.

8.2.3. Jitter_Diagnostics (Ask a Question)

Name: Jitter_Diagnostics
Offset: 0x010
Reset: 0x0
Property: Read/Write

Jitter Diagnostics

Bit	15	14	13	12	11	10	9	8
	JITTER DIAGNOSTIC ENABLE	JITTER PATTERN SELECT[2:0]					CUSTOM JITTER PATTERN[9:8]	
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0

Bit	7	6	5	4	3	2	1	0
	CUSTOM JITTER PATTERN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – JITTER DIAGNOSTIC ENABLE Set this bit to enable the TBI to transmit the jitter test patterns defined in IEEE 802.3z 36A. Clear this bit to enable normal transmit-operation.

Bits 14:12 – JITTER PATTERN SELECT[2:0] For more information refer to Table 14. Selects the jitter pattern to be transmitted in diagnostics mode

Bits 9:0 – CUSTOM JITTER PATTERN[9:0] Used in conjunction with JITTER PATTERN SELECT and JITTER DIAGNOSTIC ENABLE. Set this field to the desired custom pattern, which transmits continuously.

8.2.4. Extended_Status (Ask a Question)

Name: Extended_Status
Offset: 0x00F
Reset: 0xa000
Property: Read-only

Extended Status

Bit	15	14	13	12	11	10	9	8
	1000BASE-X FULL-DUPLEX	1000BASE-X HALF-DUPLEX	1000BASE-T FULL-DUPLEX	1000BASE-T HALF-DUPLEX				
Access	R	R	R	R				
Reset	1	0	1	0				

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – 1000BASE-X FULL-DUPLEX When 1, indicates PHY can operate in 1000BASE-X Full-Duplex mode. When 0, indicates PHY cannot operate in this mode.

Bit 14 – 1000BASE-X HALF-DUPLEX When 1, indicates PHY can operate in 1000BASE-X Half-Duplex mode. When 0, indicates PHY cannot operate in this mode.

Bit 13 – 1000BASE-T FULL-DUPLEX

Bit 12 – 1000BASE-T HALF-DUPLEX When 1, indicates PHY can operate in 1000BASE-T Half-Duplex mode. When 0, indicates PHY cannot operate in this mode.

8.2.5. Control (Ask a Question)

Name: Control
Offset: 0x000
Reset: 0x0
Property: Read/Write

Control

Bit	15	14	13	12	11	10	9	8
	PHY RESET	LOOP BACK		AUTO-NEGOTIATION ENABLE			RESTART AUTO-NEGOTIATION	
Access	R/W	R/W		R/W			R/W	
Reset	0	0		0			0	

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – PHY RESET Setting this bit causes the transmitter, receiver, and AutoNegX sub-modules in the TBI core to be reset. This bit is self-clearing.

Bit 14 – LOOP BACK Setting this bit causes the 10-bit transmit outputs of the TBI to be connected to the receive 10-bit inputs. Clearing this bit results in normal operation. This bit does not affect the clock signals, which for loopback must be handled external to the core.

Bit 12 – AUTO-NEGOTIATION ENABLE Setting this bit enables the Auto-negotiation process. If cleared, then the values programmed determines the operating condition of the link.

Bit 9 – RESTART AUTO-NEGOTIATION Setting this bit causes the Auto-negotiation process to restart. This action is only available when Auto-Negotiation has been enabled

8.2.6. AN_Next_Page_Transmit(1000BASE-X) (Ask a Question)

Name: AN_Next_Page_Transmit(1000BASE-X)
Offset: 0x007
Reset: 0x0
Property: Read/Write

AN Next Page Transmit (1000BASE-X)

Bit	15	14	13	12	11	10	9	8
	NEXT PAGE		MESSAGE PAGE	ACKNOWLEDGE 2	TOGGLE	MESSAGE/UNFORMATTED CODE FIELD[10:8]		
Access	R/W		R/W	R/W	R	R	R	R
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MESSAGE/UNFORMATTED CODE FIELD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 15 – NEXT PAGE Assert this bit to indicate additional Next Pages to follow. Bit is cleared to indicate last page.

Bit 13 – MESSAGE PAGE Assert bit to indicate Message Page. Clear bit to indicate unformatted page.

Bit 12 – ACKNOWLEDGE 2 Used by Next Page function to indicate device has ability to comply with the message. Assert bit if local device complies with message. Clear bit if local device cannot comply with message.

Bit 11 – TOGGLE Used to ensure synchronization with the Link Partner during Next Page exchange. This bit always takes opposite value of the Toggle bit of the previously exchanged Link Code Word. The initial value in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word.

Bits 10:0 – MESSAGE/UNFORMATTED CODE FIELD[10:0] Message pages are formatted pages that carry a predefined Message Code, which is enumerated in IEEE 802.3u/Annex 28C. Unformatted Code Fields take on an arbitrary value.

8.2.7. AN_Link_Partner_Base_Page_Ability(1000BASE-T) (Ask a Question)

Name: AN_Link_Partner_Base_Page_Ability(1000BASE-T)
Offset: 0x005
Reset: 0x0
Property: Read/Write

AN Link Partner Base Page Ability (1000BASE-T)

Bit	15	14	13	12	11	10	9	8
	LINK UP	AUTO-NEGOTIATION ACK AS SPECIFIED IN 802.3Z		FULL-DUPLEX	LINK SPEED[1:0]		THESE BITS MUST ALWAYS BE WRITTEN 0000000001 FOR TBI OPERATION[9:8]	
Access	R	R		R	R	R	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	THESE BITS MUST ALWAYS BE WRITTEN 0000000001 FOR TBI OPERATION[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – LINK UP Assertion of this bit indicates that the link is up

Bit 14 – AUTO-NEGOTIATION ACK AS SPECIFIED IN 802.3Z

Bit 12 – FULL-DUPLEX Assertion of this bit indicates that the link is transferring data in Full-Duplex mode.

Bits 11:10 – LINK SPEED[1:0] Assertion of these 2 bits indicates the speed that the link is transferring data.

Value	Description
2b00	10Mbps
2b01	100Mbps
2b10	1000Mbps
2b11	Reserve

Bits 9:0 – THESE BITS MUST ALWAYS BE WRITTEN 0000000001 FOR TBI OPERATION[9:0]

8.2.8. AN_Link_Partner_Ability_Next_Page(1000BASE-X) (Ask a Question)

Name: AN_Link_Partner_Ability_Next_Page(1000BASE-X)
Offset: 0x008
Reset: 0x0
Property: Read-only

AN Link Partner Ability Next Page (1000BASE-X)

Bit	15	14	13	12	11	10	9	8
	NEXT PAGE		MESSAGE PAGE	ACKNOWLEDGE 2	TOGGLE	MESSAGE OR UNFORMATTED CODE FIELD[10:8]		
Access	R		R	R	R	R	R	R
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MESSAGE OR UNFORMATTED CODE FIELD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 15 – NEXT PAGE The Link Partner asserts this bit to indicate additional Next Pages to follow. When 0, indicates last Next Page from link partner.

Bit 13 – MESSAGE PAGE When 1, indicates Message Page. When 0, indicates Unformatted Page.

Bit 12 – ACKNOWLEDGE 2 Indicates Link Partners ability to comply with the message. When 1, Link Partner complies with message. When 0, Link Partner cannot comply with message

Bit 11 – TOGGLE Used to ensure synchronization with the Link Partner during Next Page exchange. This bit always takes opposite value of the Toggle bit of the previously exchanged Link Code Word. The initial value in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word.

Bits 10:0 – MESSAGE OR UNFORMATTED CODE FIELD[10:0] Message pages are formatted pages that carry a predefined Message Code, which is enumerated in IEEE 802.3u/Annex 28C. Unformatted Code Fields take on an arbitrary value.

8.2.9. AN_Expansion(1000BASE-T) (Ask a Question)

Name: AN_Expansion(1000BASE-T)
Offset: 0x006
Reset: 0x4
Property: Read-only

AN Expansion (1000BASE-T)

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						NEXT PAGE ABLE	PAGE RECEIVED	
Access						R	R	
Reset						1	0	

Bit 2 – NEXT PAGE ABLE When 1, indicates that the local device supports the Next Page function.

Bit 1 – PAGE RECEIVED When 1, indicates that a new page has been received and stored in the applicable AN LINK PARTNER ABILITY or AN NEXT PAGE

8.2.10. AN_Advertisement(1000BASE-T) (Ask a Question)

Name: AN_Advertisement(1000BASE-T)
Offset: 0x004
Reset: 0x0
Property: Read/Write

AN Advertisement (1000BASE-T)

Bit	15	14	13	12	11	10	9	8
	LINK UP	ACK		FULL-DUPLEX	LINK SPEED[1:0]		THESE BITS MUST ALWAYS BE WRITTEN 0000000001 FOR TBI OPERATION.[9:8]	
Access	R/W	R		R/W	R/W	R/W	R	R
Reset	0	0		0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	THESE BITS MUST ALWAYS BE WRITTEN 0000000001 FOR TBI OPERATION.[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 15 – LINK UP This bit must be written 0 for TBI operation

Bit 14 – ACK Reserved. Ignore on read

Bit 12 – FULL-DUPLEX This bit must be written 0 for TBI operation.

Bits 11:10 – LINK SPEED[1:0] These bits must be written 00 for TBI operation

Bits 9:0 – THESE BITS MUST ALWAYS BE WRITTEN 0000000001 FOR TBI OPERATION.[9:0]

9. References (Ask a Question)

This section provides additional references and information related to CoreTSE. For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microchip FPGAs and PLDs website.

9.1. Known Issues and Workarounds (Ask a Question)

There are no known limitations and workarounds for CoreTSE v4.0.

9.2. Discontinued Features and Devices (Ask a Question)

There are no discontinued features and devices for CoreTSE v4.0.

9.3. Ordering Codes (Ask a Question)

CoreTSE v3.2 can be ordered through Microchip® local Sales Representative. It should be ordered using the following number scheme: CoreTSE-XX, where XX is listed in the following table.

Table 9-1. Ordering Codes

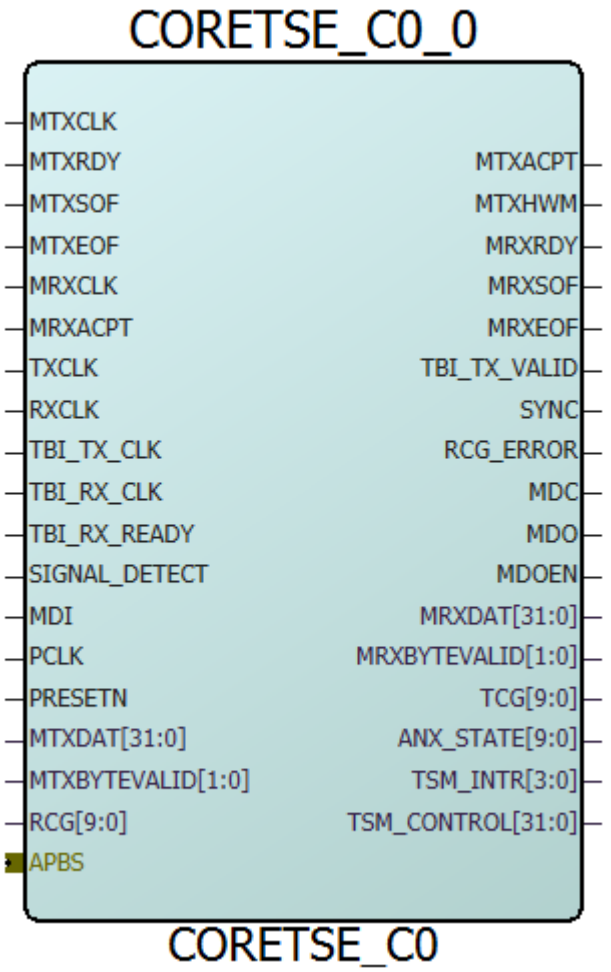
XX	Description
OM	RTL for obfuscated RTL source — multiple-use license

9.4. Migration (Ask a Question)

The following changes occur when migrating IP from legacy to updated release:

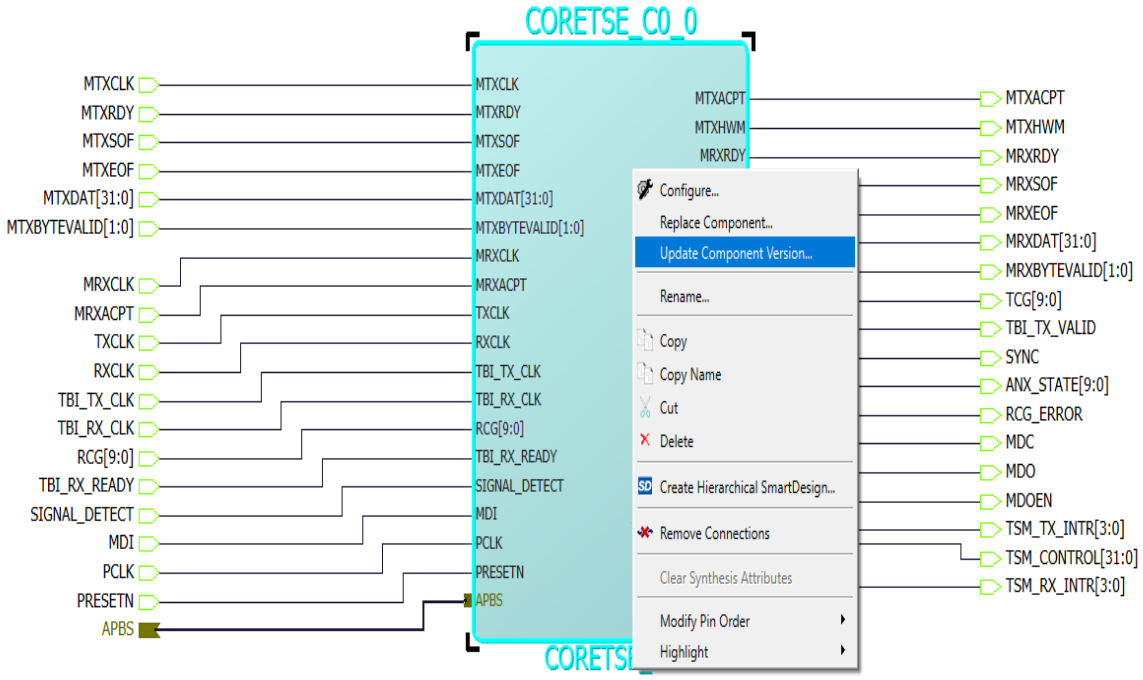
- **STBP signal** is removed from the RTL, as it is always tied to zero.
- **MTXCFRM signal** is removed from the RTL, since it is not used anywhere.
- **TSM_INTR interrupt port** is updated to 4 bits wide instead of 2 bits wide:
  - **Bit [3]** provides the interrupt for any SEC events in the transmitter and receiver path.
  - **Bit [2]** provides the interrupt for any DED events in the transmitter and receiver path.
  - **Bits [1:0]** retains the existing interrupt functionality as follows:
    - **Bit [1]** Wake On LAN detected interrupt.
    - **Bit [0]** Statistics counter carry interrupt.
- **PACKET_SIZE** is modified to **MAC transmitter/receiver FIFO Depth** in the configurator GUI. The following figure shows the expected SmartDesign view when migrating to CoreTSE v4.0 or later.

Figure 9-1. Expected SmartDesign View When Migrating to CoreTSE v4.0 or Later



The following figure shows the updating SmartDesign to CoreTSE v4.0 or later using **Update Component Version** option.

Figure 9-2. Updating SmartDesign to CoreTSE v4.0 or Later Using **Update Component Version** Option



Important: The Info or Error in the following figure might appear during the migration. You can safely ignore them as these are reported due to the newly added parameters `ECC_ENABLE, TXRX_INTR_ENABLE, Host_Interface` ports.

Figure 9-3. Migration Errors

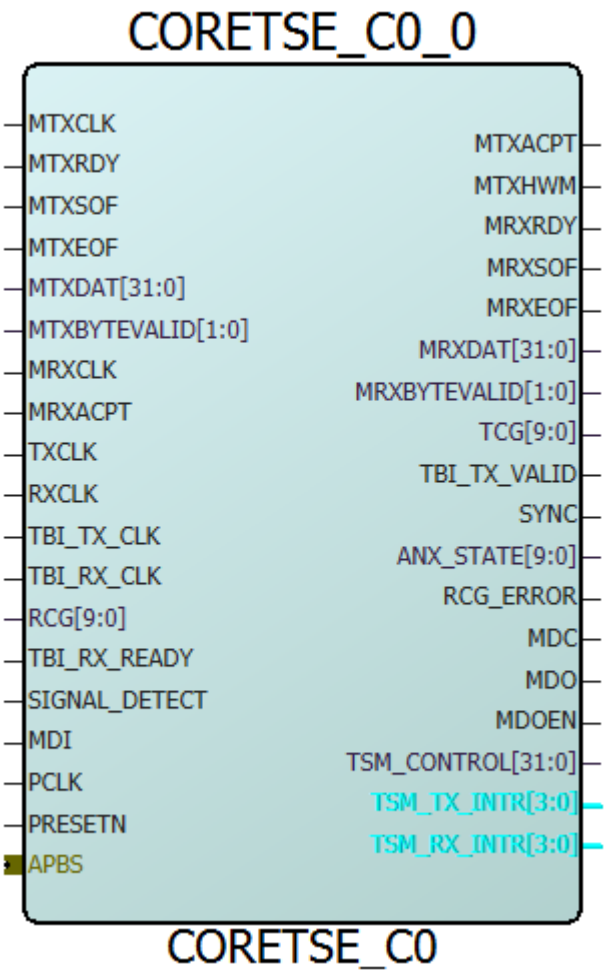
```
Info: Successfully configured component 'CORETSE_C0'.
Error: Parameter 'ECC_ENABLE' not found in the spirit definition of instance 'CORETSE_C0_0'.
Error: Parameter 'HOST_INTERFACE' not found in the spirit definition of instance 'CORETSE_C0_0'.
Error: Parameter 'TXRX_INTR_ENABLE' not found in the spirit definition of instance 'CORETSE_C0_0'.
Info: Disconnecting pin 'TSM_INTR' from net 'TSM_INTR' because it is no longer a valid connection.
Info: 'CORETSE_C0' was successfully generated.
Info: 'CORETSE_C0' manifest file 'C:/Prasanna/Libero/RTG4/CoreTSE/CoreTSE_Latest_tag/component/work/CORETSE_C0/CORETSE_C0_manifest.txt' was successfully generated.

Info: Component 'CORETSE_C0' was successfully updated to 'CORETSE' core version '3.2.119'.
```

- New Configurator option to enable separate interrupt ports for transmitter and receiver.

  The separate interrupt ports, `TSM_TX_INTR` and `TSM_RX_INTR` are enabled by default, as shown in the following figure. You can always revert to the common interrupt port that is, `TSM_INTR`.

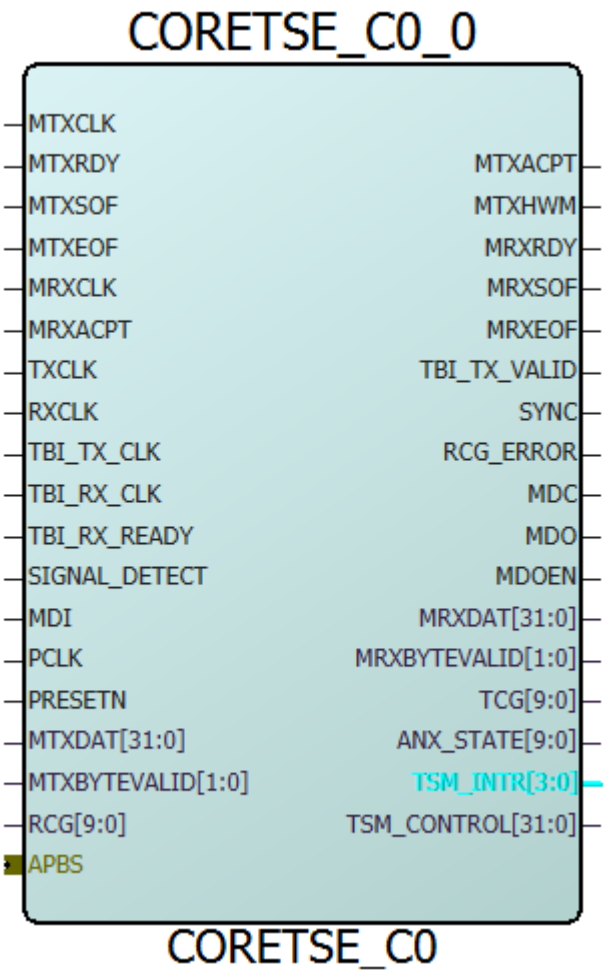
  To revert `TSM_INTR`, in the **Configurator** window, uncheck the `Enable Separate Tx and Rx interrupt ports` option.

Figure 9-4. Separate Interrupt Ports



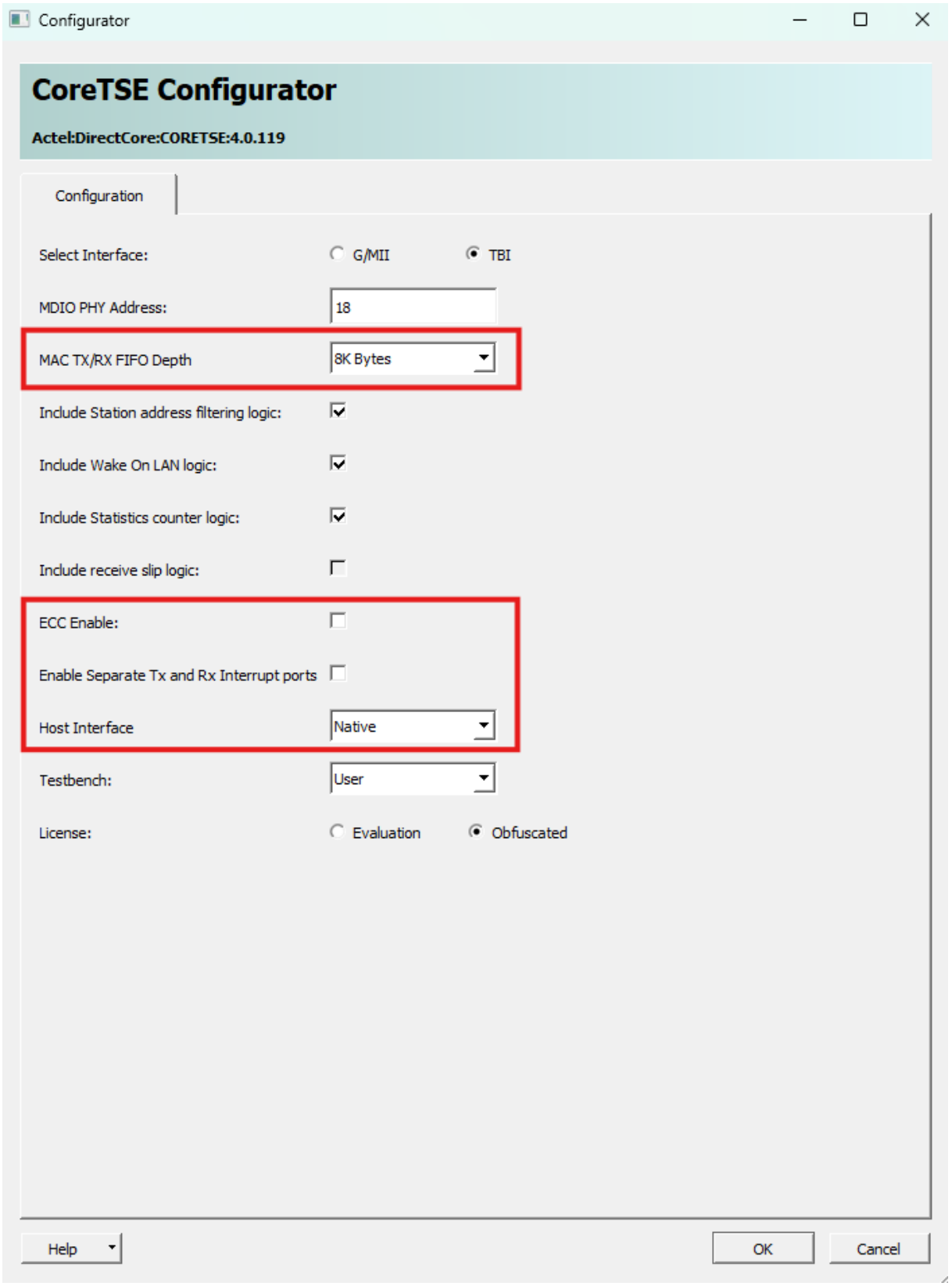
The following figure shows the common interrupt port.

Figure 9-5. Common Interrupt Port



The following figure shows the new **Configurator** window.

Figure 9-6. Updated Configurator Window



10. Glossary (Ask a Question)

Following are the list of terms and definitions used in the document.

Table 10-1. Terms and Definitions

Term	Definition
DED	Double-bit Error Detection
G/MII	Gigabit Media Independent Interface
MAC	Media Access Controller
MDIO	Management Data Input or Output
MIB	Management Information Base
MMD	MDIO Manageable Device
RMON	Remote Network Monitoring
RX	Receiver
SEC	Single-bit Error Correction
SFD	Start Frame Delimiter
SGMII	Serial Gigabit Media Independent Interface
TBI	Ten Bit Interface
TSE	Triple Speed Ethernet
TX	Transmitter
WoL	Wake on LAN

11. Device Utilization and Performance (Ask a Question)

Device utilization and performance data is provided in following tables for the supported device families. The TXCLK, RXCLK, TBI_TX_CLK, and TBI_RX_CLK performance is above 125 MHz. The data in the following table is achieved using typical synthesis and layout settings. The data described in the table is only indicative. The overall device utilization and performance of the core is system dependent.

Important: To meet the timing, use the following instructions.

- **High Effort Layout** must be enabled in the Configure options section of Place and Route for all families before performing PnR.
- Additionally, for RTG4 family devices:
  - Device speed grade must be –1.
  - Enable Single Event Transient Mitigation option must be enabled in the Project > Project Settings > Device settings.
  - MAC TX/RX FIFO Depth must be below 8 KB.

The following table describes the CoreTSE device utilization applicable with default configuration.

Device Details		Resources			Performance	RAMs
Family	Device	4LUT	DFF	Logic Elements		LSRAM
RTG4™	RT4G150-1FCG1657M	8532	4851	9292	MRXCLK – 90.843 MHz MTXCLK – 141.884 MHz PCLK - 111.049 MHz TXCLK - 141.183 MHz RXCLK - 131.062 MHz TBI_TX_CLK – 150.625 MHz TBI_RX_CLK – 150.625 MHz	7
PolarFire®	MPF300TL-FCG1152I	8447	5058	9145	MRXCLK – 149.410 MHz MTXCLK – 235.128 MHz PCLK - 203.791 MHz TXCLK - 255.102 MHz RXCLK - 218.388 MHz TBI_TX_CLK – 284.252 MHz TBI_RX_CLK – 231.054 MHz	12
SmartFusion® 2	M2S050TS-FG896	8480	5121	9366	MRXCLK – 102.564 MHz MTXCLK – 150.898 MHz PCLK - 118.864 MHz TXCLK - 148.082 MHz RXCLK - 128.123 MHz TBI_TX_CLK – 201.248 MHz TBI_RX_CLK – 130.412 MHz	14
IGLOO® 2	M2GL010-1FG484I	8678	5123	9407	MRXCLK – 135.483 MHz MTXCLK – 191.791MHz PCLK - 131.527 MHz TXCLK - 170.213 MHz RXCLK - 168.152MHz TBI_TX_CLK – 235.516 MHz TBI_RX_CLK – 172.771 MHz	14

CoreTSE Device Utilization

The following table describes the CoreTSE device utilization applicable for these (G/MII, PACKET_SIZE = 256 Bytes, SAL-OFF, WoL-OFF, and STATS-OFF) parameters.

Table 11-1. CoreTSE Device Utilization

Family (Device)	Utilization				Performance (MHz)		
	Sequential (DFF)	Combinational (LUT)	Total	%	PCLK	MTXCLK	MRXCLK
SmartFusion® 2 (M2S050)	2347	3211	5558	9.87	190	220	197
IGLOO® 2 (M2GL050)	2347	3211	5558	9.87	190	220	197
RTG4™ (RT4G150)	2323	3313	5635	3.71	156	186	152
PolarFire® (MPF300T)	2287	3143	5430	1.81	297	304	266
PolarFire SoC (MPFS250T)	2287	3143	5430	2.14	292	340	292

CoreTSE Device Utilization

The following table describes the CoreTSE device utilization applicable for these (G/MII, PACKET_SIZE = 32 KB, SAL-ON, WoL-ON, and STATS-ON) parameters.

Table 11-2. CoreTSE Device Utilization

Family (Device)	Utilization				Performance (MHz)		
	Sequential (DFF)	Combinational (LUT)	Total	%	PCLK	MTXCLK	MRXCLK
SmartFusion® 2 (M2S050)	5564	8267	13831	24.55	140	186	124
IGLOO® 2 (M2GL050)	5564	8267	13831	24.55	140	186	124
RTG4™ (RT4G150)	5579	8662	14241	9.38	115	146	91
PolarFire® (MPF300T)	5299	8568	13867	4.63	220	248	187
PolarFire SoC (MPFS250T)	5299	8568	13867	5.46	203	256	174

CoreTSE Device Utilization

The following table describes the CoreTSE device utilization applicable for these (TBI, PACKET_SIZE = 256 Bytes, SAL-OFF, WoL-OFF, and STATS-OFF) parameters.

Table 11-3. CoreTSE Device Utilization

Family (Device)	Utilization				Performance (MHz)		
	Sequential (DFF)	Combinational (LUT)	Total	%	PCLK	MTXCLK	MRXCLK
SmartFusion® 2 (M2S050)	3408	5271	8679	15.40	177	221	184
IGLOO® 2 (M2GL050)	3408	5271	8679	15.40	177	221	184
RTG4™ (RT4G150)	3374	5324	8698	5.73	162	163	154
PolarFire® (MPF300T)	3329	5113	8442	2.82	288	358	301
PolarFire SoC (MPFS250T)	3329	5113	8442	3.32	292	340	292

CoreTSE Device Utilization

The following table describes the CoreTSE device utilization applicable for these (TBI, PACKET_SIZE = 32 KB, SAL-ON, WoL-ON, and STATS-ON) parameters.

Table 11-4. CoreTSE Device Utilization

Family (Device)	Utilization				Performance (MHz)		
	Sequential (DFF)	Combinational (LUT)	Total	%	PCLK	MTXCLK	MRXCLK
SmartFusion® 2 (M2S050)	6623	10206	16829	29.87	136	166	126
IGLOO® 2 (M2GL050)	6623	10206	16829	29.87	136	166	126
RTG4™ (RT4G150)	6633	10718	17315	11.43	120	127	90

Table 11-4. CoreTSE Device Utilization (continued)

Family (Device)	Utilization				Performance (MHz)		
	Sequential (DFF)	Combinational (LUT)	Total	%	PCLK	MTXCLK	MRXCLK
PolarFire® (MPF300T)	6341	10529	16870	5.63	207	290	191
PolarFire SoC (MPFS250T)	6341	10529	16870	6.64	203	256	174

12. Resolved Issues (Ask a Question)

The following table lists all the resolved issues for the various CoreTSE releases.

Table 12-1. Resolved Issues

Release	Description
4.0	The following is the list of all resolved issues in the v4.0 release: • Updated Register Configuration Sequence for Frame Filtering and Pause Frame Transmission. • Added support for AXI4Stream Interface along with Native interface. • 01559798 - Added option to filter out FCS Bytes on AXI4Stream RX interface. • 01311949 - Updated CAR1 and CAR2 register access types and updated the width mismatch for the registers: RBYT, RFCS, RXCF, RFLR and TNCL. • 01333337 - Updated Register "0x010 - Maximum_frame_length" description. • Added support for MRXACPT staying low beyond two cycles without data loss. • Added ECC feature with interrupt support • 01435110 and 01602479 - Resolved un-mitigated reset issues in RTG4™
3.2	The following is the list of all resolved issues in the v3.2 release: • 123029. Resolved issue on "SYNC" and "RX_SLIP" signal behavior. • 123323. Resolvd issues on Frame filtering for non matching unicast address. • 94247 109819 111670 119967 120547 121164 121995 Resolved data path issues for RTG4™ device family. • 102082 114353 123116 Resolved issue while accessing statistics counters. • 111681. Updated the reset synchronization scheme. • 96703 112075 112127 118053 122734 Minor corrections in the user guide. • 112587. Added Timing Constraints section in user guide. • 94321. Added Self Destruct evaluation support for CoreTSE. • 86393. CoreTSE User Guide does not mention SGMII. Added SGMII interface in features & SGMII/TBI refer to the same interface.
3.1	The following is the list of all resolved issues in the v3.1 release: • 79751. Typo in HB usage table content. • 83041. The default value of MAC-FIFO Configuration Register 5 in handbook is mismatched with actual default value. • 77385. Add RX_SLIP output port and remove the barrel shift word aligner for PolarFire®.

Table 12-1. Resolved Issues (continued)

Release	Description
3.0	The following is the list of all resolved issues in the v3.0 release: • 75227. Support for a single 125MHz TBI receive clock. • 75236. To add support for PolarFire. • 75072. CoreTSE GMII Mode, pins showing as unused after synthesis. • 71541. Simulation error when using CoreTSE and CoreTSE_AHB in single design.
2.0	Initial Release

13. Glossary (Ask a Question)

Following are the list of terms and definitions used in the document.

Table 13-1. Terms and Definitions

Term	Definition
DED	Double-bit Error Detection
G/MII	Gigabit Media Independent Interface
MAC	Media Access Controller
MDIO	Management Data Input or Output
MIB	Management Information Base
MMD	MDIO Manageable Device
RMON	Remote Network Monitoring
RX	Receiver
SEC	Single-bit Error Correction
SFD	Start Frame Delimiter
SGMII	Serial Gigabit Media Independent Interface
TBI	Ten Bit Interface
TSE	Triple Speed Ethernet
TX	Transmitter
WoL	Wake on LAN

14. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 14-1. Revision History

Revision	Date	Description
E	10/2025	Updated the width for registers: RBYT, RFCS, RXCF, RFLR, and TNCL in the Register Map and Descriptions section.
D	09/2025	The following is the list of changes in revision D of the document: • Updated Jumbo Frame Support section. • Updated Table 4-1 in Configuration Settings section. • Updated Table 4-2, Table 4-3 and Table 4-4 in Configuration Settings section. • Updated SmartDesign section. • Updated Figure 5-2 in Configuring CoreTSE in SmartDesign section. • Updated Simulation Flows section. • Updated Synthesis section. • Updated Place-and-Route section. • Updated User Testbench section. • Updated Timing Constraints section. • Updated Register Map and Descriptions section. • Added Migration section.
C	02/2022	The following is the list of changes in revision C of the document: • Updated CoreTSE Parameters and Interface Signals section.
B	01/2022	The following is the list of changes in revision B of the document: • Updated SGMII/Ten-Bit Interface. • Updated Timing Constraints. • Updated System Integration.
A	12/2021	The following is the list of changes in revision A of the document: • The document was migrated to the Microchip template. • The document number was updated to DS50003245A from 50200549. • Added Clocks and Reset and Design Constraints. • Updated Simulation Flows. • Updated Synthesis. • Updated Place-and-Route. • Replaced Transceiver with XCVR throughout the document. • Removed the Ordering Information section.
4	—	Updated changes related to CoreTSE v3.2.
3	—	Updated changes related to CoreTSE v3.1.
2	—	Updated changes related to CoreTSE v3.0.
1	—	Revision 1.0 was the first publication of this document. Created for CoreTSE v2.0.

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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.