

Introduction [\(Ask a Question\)](#)

CoreGbE_MR is designed to comply with the IEEE® 802.3-2022 specification and supports 1 Gbps and 2.5 Gbps data rates using a 20-bit XCVR interface for 1000BASE-X and 2500BASE-X operation. CoreGbE_MR provides an AXI4-Stream interface for both transmit and receive data paths to and from the client and an AXI4-Lite target interface for register access.

Summary

The following table provides the CoreGbE_MR characteristics.

Table 1. CoreGbE_MR Characteristics

Core Version	This document applies to the CoreGbE_MR v2.0.
Supported Device Families	• PolarFire® SoC • PolarFire® • RT PolarFire®
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Supported Interfaces	• AXI4Stream Interface • Transceiver 20-bit PMA interface • AXI4Lite Interface
Licensing	The core supports the generation of following versions: Obfuscated: Obfuscated version is available with obfuscated and encrypted Verilog RTL, Obfuscated version supports user testbench simulation and supports unlimited functionality on silicon. Obfuscated version is not license locked and will be available free. Note: If customer wants the Clear RTL license, they should contact the Microchip Technology Technical Support Portal.
Installation Instructions	CoreGbE_MR must be installed to the IP Catalog of Libero SoC automatically through the IP Catalog update function. Alternatively, it can be manually downloaded from the catalog. Once the IP core is installed, it is configured, generated and instantiated within SmartDesign for inclusion in the project.
Device Utilization and Performance	A summary of utilization and performance information is listed in Device Utilization and Performance .

Features [\(Ask a Question\)](#)

CoreGbE_MR has the following key features:

Media Access Control (MAC):

- Designed to IEEE 802.3-2022 specification with below feature supports

Table 2. IEEE 802.3-2022 Specification

Clause	Feature Description
4	Media Access Control
35	Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (SGMII)
36	PCS and PMA sublayer for 1Gb, type 1000BASE-X

- Configurable Preamble Size and Contents

- Programmable Frame Check Sequence (FCS) Insertion on transmit
- FCS checking on Receive
- Programmable FCS removal on receive
- Pad insertion and removal
- User Programmable IFG
- Jumbo frames up to 9216 bytes
- VLAN tag frames
- Optional Frame Statistics Counters
- Optional Pause frame insertion on transmit and flagging on receive
- Optional frame filtering based on destination address using hash algorithm
- Optional frame filtering based on specific drop reason of the frame
- Optional Wake on LAN (WoL) with magic packet detection

PCS:

- Elastic buffer on the receive path
- 16b/20b Encoder, 20b/16b Decoder and Word aligner

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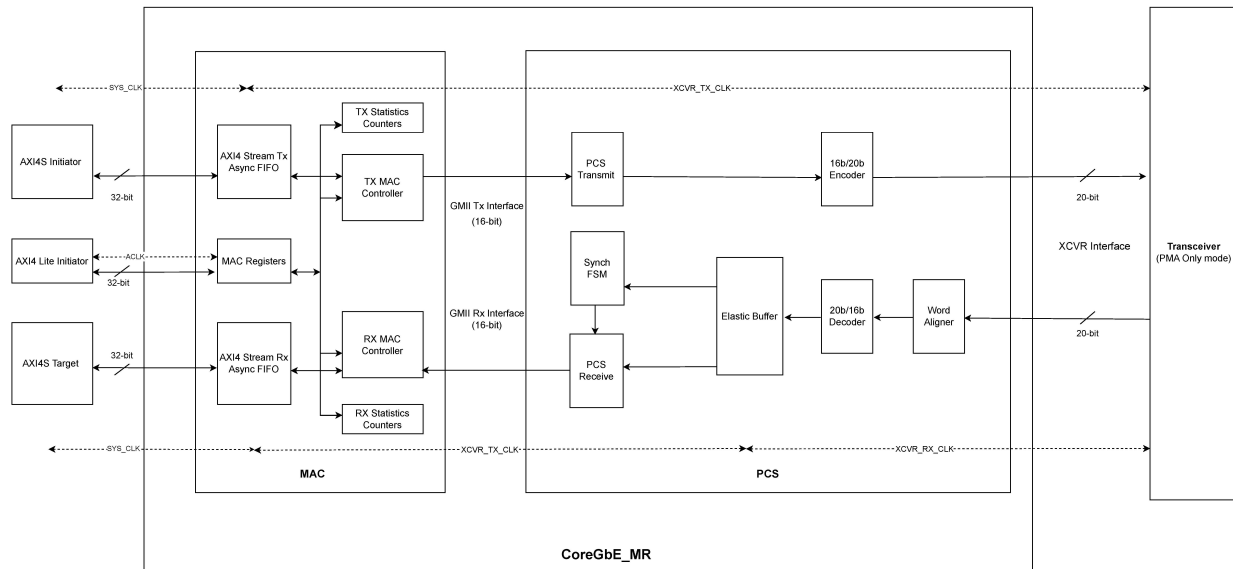
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1. Functional Description [\(Ask a Question\)](#)

CoreGbE_MR is designed for the IEEE® 802.3-2022 specification and supports Transceiver 20-bit PMA interface for 1 Gbps and 2.5 Gbps data rate.

Figure 1-1. CoreGbE_MR Block Diagram



1.1. MAC [\(Ask a Question\)](#)

This section describes various functions used in this IP core.

1.1.1. Tx/Rx AXI4-Stream FIFO [\(Ask a Question\)](#)

AXI4-Stream FIFO is an asynchronous FIFO having same write and read port widths. It is AXI4-Stream compatible. AXI4-Stream FIFO decouples system clock from transceiver clock. FIFO is used in First Word Fall Through (FWFT) mode. Both TX and RX FIFO in the CoreGbE_MR is operated in the cut-through mode (data is read from the FIFO as soon as there is data available) or Store-n-Forward mode (data is read from the FIFO when entire packet is received).

1.1.2. TX MAC Controller [\(Ask a Question\)](#)

The TX MAC Controller is responsible for constructing and transmitting Ethernet frames in compliance with the IEEE 802.3 standard. It interfaces with AXI4-Stream interface on the user side and performs the following key functions during the frame transmission process:

- **Framing the Packet:** The controller inserts the necessary Ethernet preamble and Start Frame Delimiter (SFD) at the beginning of each packet. The preamble is programmable in length (typically 7 bytes), and the SFD is fixed as 0xD5.
- **Programmable Preamble Length:** The length of the preamble (excluding the SFD) is configurable, allowing for support of non-standard preamble formats if needed, while maintaining compatibility with standard receivers.
- **FCS generation and insertion:** The controller computes a 32-bit CRC (Frame Check Sequence) over the entire Ethernet payload (excluding the preamble and SFD) using the standard Ethernet CRC-32 polynomial. The resulting FCS is appended to the end of the frame automatically.
- **Pad bytes for Short Packets:** To comply with the minimum Ethernet frame size of 64 bytes (excluding preamble and SFD), the controller adds zero-padding to short frames (frame size <64).

bytes). This ensures the transmitted frame meets protocol requirements regardless of payload length.

- **Programmable Inter-Packet Gap (IPG):** The IPG defines the idle period between two consecutive Ethernet frames and is programmable up to 48 bytes. The controller inserts the specified number of idle bytes between packet transmissions to meet timing requirements and ensure reliable data separation.
- **Pause Frame Insertion:** PAUSE frames are a type of control frame identified by the Ether Type value 0x8808, a specific destination address (01-80-c2-00-00-01), and an opcode of 0x0001. The transmit (TX) MAC controller automatically generates and sends a PAUSE(to stop transmission from link partner) frame when the receive asynchronous FIFO reaches a configurable high watermark. The pause duration is specified by the value set in MAC_TX_PAUSE_TIMER register. It also generates and sends a PAUSE(to resume transmission from link partner) frame when the receive async FIFO drops below a configurable low water mark.
- **Register Configuration for Pause Frames** To send the pause frames, the following registers must be configured:

Table 1-1. Register Configuration for Pause Frames

Action	Configuration Register	Description
Configure Pause timer value	MAC_TX_PAUSE_TIMER (0x170)	Set the pause timer value in bits [15:0]. This register takes effect only when the MAC TX Pause is enabled in the configurator.
Configure High and Low watermark levels of the RX FIFO	MAC_RX_PAUSE_WM (0x1F0)	Set the RX FIFO's high and low watermark levels, so the TX MAC controller knows when to send a PAUSE frame.
Configure the required Pause quanta value	MAC_RX_PAUSE_RTX (0x1F4)	This value tells you how many pause quanta (each equal to 64 byte-times) must pass after the first pause frame is acknowledged before we send another one—as long as the RX MAC FIFO is still above the low watermark.
Configure MAC Source Address	Program the below two registers to configure the Source Address: • MAC_ADDR_LOWER (0x24) • MAC_ADDR_UPPER (0x20)	Program these two registers with the Source Address.

This block ensures that all frames are properly formatted, error-checked and padded according to Ethernet standards, while also providing flexibility through programmable preamble and IPG lengths. The block also sends fully framed packets over SGMII (16-bit) interface at 156.25 MHz.

1.2. RX MAC Controller [\(Ask a Question\)](#)

The module is designed to process incoming Ethernet frames from SGMII interface and deliver clean, validated packets to the user through AXI4 streaming interface. It ensures data integrity, frame alignment and filtering of invalid or malformed frames and performs the following key functions during frame reception:

- **Preamble Detection and Frame Start Alignment:** Detects the Start Frame Delimiter (SFD, 0xD5) from the incoming stream. Ensure proper alignment of the frame start by identifying the preamble sequence. Supports detection of variable preamble lengths.
- **Frame Extraction and Validation:** Extracts the payload and control information from the incoming stream, separating it from preamble and SFD. Identifies start-of-packet and end-of-packet boundaries accurately.
- **Frame Check Sequence (FCS) Verification:** Computes the 32-bit CRC in real-time over the received payload data. Compare the computed CRC with the received Frame Check Sequence to validate data integrity. Marks frames with CRC errors as invalid and optionally drop or flags them for the upper layer.

- **Padding Removal (Optional):** Optionally removes padding bytes from short frames, if configured, based on length and type field parsing.
- **Inter-Packet Gap Handling:** Detects the inter-packet gap (that is, idle characters) and uses it to delimit frames. Ensures readiness for the next packet without data collision or corruption.
- **Pause Frame Detection:** When a frame is received and identified as a control frame, the MAC examines the Destination Address (DA) and the Opcode fields. If the DA matches either the reserved multicast address for PAUSE frames (01-80-c2-00-00-01) or the device's own unique address {MAC_ADDR_UPPER, MAC_ADDR_LOWER}, and the Opcode is 0x0001, the control frame is recognized as a PAUSE control frame. Upon receiving a PAUSE control frame with non-zero pause time value, the RX MAC controller instructs the TX MAC controller to halt data frame transmission and only allow control frames. The pause time received is stored internally and decrements with each 64 byte-times interval. Data transmission resumes when either a PAUSE frame with a zero-pause time is received or the pause timer counts down to zero, signaling that the MAC is un-paused.
- **Wake on LAN Support:**
 - a. This feature is based on AMD's Magic Packet Detection technology.
 - b. The first step of the detection procedure is to scan the first six bytes of the frame, which contain Destination address.
 - c. Magic Packet detection is only carried out when the incoming frame's destination address matches the configured destination {MAC_ADDR_UPPER, MAC_ADDR_LOWER} address, or if the frame's destination address is a multicast or broadcast address.
 - d. After the destination address match, core searches for the Magic Packet technology's defined preamble of six continuous aligned bytes with all bits asserted (0xFF).
 - e. Following this valid Magic Packet preamble, core immediately expects 16 back-to-back repetitions of the six-byte MAC destination address. Failure to achieve this exact pattern by a single byte at any time during the frame resets the circuitry back to the preamble search state.
 - f. After successful recognition of the Magic Packet payload, the output port WOL_DETECT is asserted, which is valid with corresponding end of frame.
- **Output Interface (AXI4-Stream):**
 - a. Delivers validated Ethernet frame payloads to upper layers through a streaming interface.
 - b. Provides sideband signals such as error, and user fields to indicate frame status, length and validity.

1.2.1. Frame Filtering [\(Ask a Question\)](#)

This module provides a method, hash-based filtering, to statistically filter out network frames that are not meant for the current node. For each incoming multicast or unicast frame, the core extracts the 48-bit MAC destination address and applies a hash function to reduce it to a 6-bit index into the 64-bit hash register. The hash function is an XOR of every sixth bit of the MAC destination address(mac-da) as shown in the table below:

Table 1-2. Example of Hash Table

Index Bit	MAC-DA Bits Used (XORed)
hash_index[0]	0, 6, 12, 18, 24, 30, 36, 42
hash_index[1]	1, 7, 13, 19, 25, 31, 37, 43
hash_index[2]	2, 8, 14, 20, 26, 32, 38, 44
hash_index[3]	3, 9, 15, 21, 27, 33, 39, 45
hash_index[4]	4, 10, 16, 22, 28, 34, 40, 46
hash_index[5]	5, 11, 17, 23, 29, 35, 41, 47

The resulting 6-bit index points to a specific bit in the 64-bit hash register. If the bit at this index is set, the frame is accepted; if not, it is filtered out. Users can configure which MAC addresses are accepted by calculating the index for each desired address and setting the corresponding bit in the hash register. This module also filters out frames with specific drop reason configured in the register MAC_RX_FRMFIL_PKT. This enables administrators to configure precise filtering rules and to monitor or troubleshoot network traffic by examining the reasons for dropped frames.

- **Register Configuration for Frame Filtering:** Enable either of the below two options in the configurator based on the requirement:
 - **Packet Based Frame Filtering:** Set to 1–Enables the frame filtering based on specific reason for the drop
 - **Registers to be configured:** Program the below two registers to configure the Destination Address:
 - MAC_ADDR_LOWER (0x24)
 - MAC_ADDR_UPPER (0x20)
- **Program the register MAC_RX_FRMFIL_PKT (0x190) as below:**
 - Configure the required field of bits for specific type of frame filtering. For example, if Unicast frame with mismatch in DA is to be filtered, set the bit[17] to 1.
 - Configuring this register is effective only when the **Packet Based Frame Filtering** option in the configurator is set to 1.
- **Hash Based Frame Filtering:** Set to 1–Enables the frame filtering based on hash-table algorithm
- **Registers to be configured:**
 - 0x1A0 - MAC_RX_FRMFIL_HTR0
 - 0x1A4 - MAC_RX_FRMFIL_HTR1

Example: hash-based frame filtering:

- The hash table registers are programmed in the following manner:
 - MAC_RX_FRMFIL_HTR0= 32'h00302069
 - MAC_RX_FRMFIL_HTR1= 32'hc038a108
 - For the destination mac address (mac_da) 48'h72cf11844923, lsb (mac_da[0]) is 1'b1 and msb (mac_da[47]) is 1'b0
 - Using the hash-index generation logic, the computed hash_index for this MAC address is hash_index = 6'd63. Hash index 63 maps to bit 31 of register **MAC_RX_FRMFIL_HTR1** (since HTR1 covers hash bits [63:32]).
 - Looking at the programmed value: MAC_RX_FRMFIL_HTR1[31] = 1. Since, the hash bit corresponding to this MAC address is 1, frames with this destination MAC address is accepted (not filtered out).

Note: Both the Packet Based and Hash Based frame filtering's are effective only when the MAC RX FIFO Mode is selected as **Store-n-Forward** mode in the Configurator.

1.3. TX/RX Statistics Counters [\(Ask a Question\)](#)

This module is configurable and designed to collect and report various statistics on received Ethernet frames in real-time. It provides detailed visibility into traffic characteristics and errors for performance monitoring, diagnostics and debugging of Ethernet interfaces. It tracks multicast, broadcast, VLAN-tagged frames, PAUSE, control, total frames, frame size, FCS errors, undersized frames, oversized frames, padded and length field errors in both transmit and receive paths.

1.4. PCS [\(Ask a Question\)](#)

The 2500BASE-X PCS operates similar to the 1000BASE-X PCS, which operates according to Clause 36 of the IEEE 802.3 2008 specification. The design implements transmit, receive and synchronization state machines in accordance with IEEE 802.3z Clause 36.

1. The PCS Transmit block implements 16b/20b encoder to convert SGMII data octets into a sequence of ordered sets as defined in IEEE 802.3-2008.
2. The Receive block contains the following blocks
 - **Word Aligner:** Performs block synchronization by detecting known bit patterns (for example, comma characters from /K28.5/) in the incoming serial bitstream. It ensures correct 10-bit boundary alignment before forwarding the data to downstream logic.
 - **Elastic Buffer:** The Elastic Buffer facilitates the transfer of 20-bit parallel XCVR data received synchronously with the XCVR_RX_CLK from the PMA sublayer into the core's internal XCVR_TX_CLK domain. To maintain a stable buffer occupancy, this Elastic Buffer dynamically inserts or removes Idle sequences as needed. This process ensures that data frames remain intact and uncorrupted.
 - **20b/16b Decoder:** Decodes the 20 bit input data from the Transceiver as defined in IEEE 802.3-2008.
 - **Synchronization FSM:** Implements the state machine logic for PCS synchronization, as specified in IEEE 802.3 Clause 36. It monitors sync headers, manages error counters and asserts SYNC output signal once a valid synchronization state is achieved.

2. CoreGbE_MR Parameters and Interface Signals [\(Ask a Question\)](#)

This section discusses the parameters in the CoreGbE_MR configurator settings and I/O signals.

Note: The Parameter Name column in the following table shows the actual parameter names used in RTL. The Description column starts with the parameter names as they appear in the CoreGbE_MR GUI configurator.

2.1. CoreGbE_MR Configuration Settings [\(Ask a Question\)](#)

Table 2-1. Configuration Parameters of CoreGbE_MR

Parameter Name	Valid Values	Default Value	Description
Configuration			
ECC_ENABLE	0-1	0	ECC Enable 0: ECC is disabled for embedded memories used in the Core. 1: ECC is enabled for embedded memories used in the Core. Note: Supported for PolarFire and PolarFire SoC families and LSRAMs only.
RESET_TYPE	0: Asynchronous 1: Synchronous	Asynchronous	Reset Type This Parameter is used to select reset type. 0 Asynchronous 1 Synchronous
MAC			
TX_MAC_CFG_FIFO_MODE	0: Cut-Through 1: Store-n-Forward	Cut-Through	MAC TX FIFO mode 0: Cut-Through: In this mode, data from the FIFO is read as soon as it is available 1: Store-n-Forward: In this mode, data is read from the FIFO when entire packet is received
TX_MAC_CFG_FIFO_DEPTH	32: 32 64: 64 128: 128 256: 256 512: 512 1024: 1024 2048: 2048 4096: 4096 8192: 8192	32	MAC TX FIFO Depth The depth of the transmit system FIFO. Each location stores 4 bytes Note: When MAC TX FIFO Mode is configured to e Store-n-Forward mode for the MAC TX FIFO, FIFO depth shall be set to handle the maximum frame size.
TX_MAC_CFG_PREAMBLE	0-1	0	MAC TX Preamble '1': Core is enabled to send custom preamble, and the associated signals are active. '0': Function is disabled.

Table 2-1. Configuration Parameters of CoreGbE_MR (continued)

Parameter Name	Valid Values	Default Value	Description
TX_MAC_CFG_CHECK_LT	0-1	0	MAC TX Check LT Field When '1' the core checks the LT field against the actual size of the packet. When '0' the core does not check the LT field against the actual size of the packet. The checking has no consequences for the data- path, that is, it only influences the statistics reporting.
TX_RAM_TYPE	1:Fabric 2:LSRAM 3:uSRAM	LSRAM	TX FIFO RAM Type This parameter is used to select RAM type for the transmit FIFO. uSRAM and LSRAM are embedded memory blocks. When Fabric is selected, core implements RAM using fabric resources that is, FFs and LUTs
RX_MAC_CFG_FIFO_MODE	0: Cut-Through 1: Store-n-Forward	Cut-Through	MAC RX FIFO Mode 0: Cut-Through: In this mode, data from the FIFO is read as soon as it is available 1: Store-n-Forward: In this mode, data is read from the FIFO when entire packet is received
RX_MAC_CFG_FIFO_DEPTH	32: 32 64: 64 128: 128 256: 256 512:512 1024:1024 2048:2048 4096:4096 8192:8192	32	MAC RX FIFO Depth The depth of the receive system FIFO. Each location stores 4 bytes Note: When MAC RX FIFO Mode is configured to Store-and-Forward mode for the MAC RX FIFO, FIFO depth shall be set to handle the maximum frame size.
RX_MAC_CFG_PREAMBLE	0-1	0	MAC RX Preamble '1': Core is enabled to receive custom preamble, and the associated signals are active. '0': Function is disabled.
RX_MAC_CFG_CHECK_LT	0-1	0	MAC RX Check LT Field When '1' the core checks the LT field against the actual size of the packet. When '0' the core does not check the LT field against the actual size of the packet. The checking has consequences for the data- path and the statistics reporting.

Table 2-1. Configuration Parameters of CoreGbE_MR (continued)

Parameter Name	Valid Values	Default Value	Description
RX_RAM_TYPE	1:Fabric 2:LSRAM 3:uSRAM	LSRAM	RX FIFO RAM Type This parameter is used to select RAM type for the receive FIFO. uSRAM and LSRAM are embedded memory blocks. When Fabric is selected, core implements RAM using fabric resources that is, FFs and LUTs
TX STATISTICS			
TX_MAC_STATS_PKT_CNT_EN	0-1	0	TX Packet
TX_MAC_STATS_PKT_ERR_CNT_EN	0-1	0	TX Errored Packet
TX_MAC_STATS_PKT_ERR_LEN_LONG_CNT_EN	0-1	0	TX Errored at length, with long
TX_MAC_STATS_PKT_ERR_LEN_CHECK_CNT_EN	0-1	0	TX Errored at length, with check
TX_MAC_STATS_PKT_ERR_LEN_SHORT_CNT_EN	0-1	0	TX Errored at length, with short
TX_MAC_STATS_PKT_ERR_FCS_CNT_EN	0-1	0	TX Errored at FCS
TX_MAC_STATS_PKT_ERR_FRM_CNT_EN	0-1	0	TX Errored at framing
TX_MAC_STATS_PKT_BROADCAST_CNT_EN	0-1	0	TX Broadcast packet
TX_MAC_STATS_PKT_MULTICAST_CNT_EN	0-1	0	TX Multicast packet
TX_MAC_STATS_PKT_PAUSE_CNT_EN	0-1	0	TX Pause packet
TX_MAC_STATS_PKT_CONTROL_CNT_EN	0-1	0	TX Control packet.
TX_MAC_STATS_PKT_VLAN_CNT_EN	0-1	0	TX VLAN packet
TX_MAC_STATS_PKT_PAD_CNT_EN	0-1	0	TX Padded packet
TX_MAC_STATS_PKT_64B_CNT_EN	0-1	0	TX 64Byte packet
TX_MAC_STATS_PKT_65BTO127B_CNT_EN	0-1	0	TX 65 to 127Byte packet
TX_MAC_STATS_PKT_128BTO255B_CNT_EN	0-1	0	TX 128 to 255Byte packet
TX_MAC_STATS_PKT_256BTO511B_CNT_EN	0-1	0	TX 256 to 511Byte packet
TX_MAC_STATS_PKT_512BTO1023B_CNT_EN	0-1	0	TX 512 to 1023Byte packet
TX_MAC_STATS_PKT_1024BTO1518B_CNT_EN	0-1	0	TX 1024 to 1518Byte packet
TX_MAC_STATS_PKT_1519BTO1522B_VLAN_CNT_EN	0-1	0	TX 1519 to 1522Byte packet
TX_MAC_STATS_PKT_GTMAXB_CNT_EN	0-1	0	TX greater than max bytes packet
TX_MAC_STATS_PKT_FIFO_SBCOR_CNT_EN	0-1	0	TX FIFO SB Correct count
TX_MAC_STATS_PKT_FIFO_DBDET_CNT_EN	0-1	0	TX FIFO DB Detect count
RX STATISTICS			
RX_MAC_STATS_PKT_CNT_EN	0-1	0	RX Packet
RX_MAC_STATS_PKT_ERR_CNT_EN	0-1	0	RX Errored Packet
RX_MAC_STATS_PKT_ERR_LEN_LONG_CNT_EN	0-1	0	RX Errored at length, with long
RX_MAC_STATS_PKT_ERR_LEN_CHECK_CNT_EN	0-1	0	RX Errored at length, with check
RX_MAC_STATS_PKT_ERR_LEN_SHORT_CNT_EN	0-1	0	RX Errored at length, with short
RX_MAC_STATS_PKT_ERR_FCS_CNT_EN	0-1	0	RX Errored at FCS
RX_MAC_STATS_PKT_ERR_FRM_CNT_EN	0-1	0	RX Errored at framing
RX_MAC_STATS_PKT_BROADCAST_CNT_EN	0-1	0	RX Broadcast packet
RX_MAC_STATS_PKT_MULTICAST_CNT_EN	0-1	0	RX Multicast packet
RX_MAC_STATS_PKT_PAUSE_CNT_EN	0-1	0	RX Pause packet
RX_MAC_STATS_PKT_CONTROL_CNT_EN	0-1	0	RX Control packet.
RX_MAC_STATS_PKT_VLAN_CNT_EN	0-1	0	RX VLAN packet
RX_MAC_STATS_PKT_PAD_CNT_EN	0-1	0	RX Padded packet

Table 2-1. Configuration Parameters of CoreGbE_MR (continued)

Parameter Name	Valid Values	Default Value	Description
RX_MAC_STATS_PKT_64B_CNT_EN	0-1	0	RX 64Byte packet
RX_MAC_STATS_PKT_65BTO127B_CNT_EN	0-1	0	RX 65 to 127Byte packet
RX_MAC_STATS_PKT_128BTO255B_CNT_EN	0-1	0	RX 128 to 255Byte packet
RX_MAC_STATS_PKT_256BTO511B_CNT_EN	0-1	0	RX 256 to 511Byte packet
RX_MAC_STATS_PKT_512BTO1023B_CNT_EN	0-1	0	RX 512 to 1023Byte packet
RX_MAC_STATS_PKT_1024BTO1518B_CNT_EN	0-1	0	RX 1024 to 1518Byte packet
RX_MAC_STATS_PKT_1519BTO1522B_VLAN_CNT_EN	0-1	0	RX 1519 to 1522Byte packet
RX_MAC_STATS_PKT_GTMAXB_CNT_EN	0-1	0	RX greater than max bytes packet
RX_MAC_STATS_PKT_FIFO_SBCOR_CNT_EN	0-1	0	RX FIFO SB Correct count
RX_MAC_STATS_PKT_FIFO_DBDET_CNT_EN	0-1	0	RX FIFO DB Detect count
RX_MAC_STATS_PKT_DROP_CNT_EN	0-1	0	RX Drop packet
RX_PCS_STATS_EB_DBDET_CNT_EN	0-1	0	RX EB SB Correct count
RX_PCS_STATS_EB_SBCOR_CNT_EN	0-1	0	RX EB DB Detect count
RX_PCS_STATS_CODE_ERROR_CNT_EN	0-1	0	RX PCS Code error count
RX_PCS_STATS_SYNC_LOST_ERROR_CNT_EN	0-1	0	RX PCS SYNC lost error count
PAUSE Feature			
TX_MAC_CFG_PAUSE_EN	0: Disabled 1: Enabled	Disabled	MAC TX Pause When disabled, the core support for pause is disabled. When enabled, the core support for pause is enabled.
RX_MAC_CFG_PAUSE_EN	0: Disabled 1: Enabled	Disabled	MAC RX Pause When disabled, the core doesn't support for pause. When enabled, the core is enabled to support pause port.
RX_MAC_CFG_PAUSE_CHECK_PUC	0 - 1	0	MAC RX Pause Unicast Check '1': The core is enabled to use the pause unicast-cast address to identify pause frames. '0': The function is not supported. You can configure this parameter only if MAC RX Pause parameter is not disabled.
Frame Filtering			
RX_MAC_CFG_FRMFIL_PKT	0-1	0	Packet Based Frame Filtering 0 - Disables packet-based frame filtering 1 - Enables packet-based frame filtering. Note: This feature is valid when MAC RX FIFO Mode is selected as Store-n-Forward mode only

Table 2-1. Configuration Parameters of CoreGbE_MR (continued)

Parameter Name	Valid Values	Default Value	Description
RX_MAC_CFG_FRMFIL_HASH	0-1	0	Hash Based Frame Filtering. 0 - Disables hash-based frame filtering on MAC destination address 1 - Enables hash-based frame filtering on MAC destination address. Note: This feature is valid when MAC RX FIFO Mode is selected as Store-n-Forward mode only
Wake-on-LAN			
RX_MAC_CFG_WOL	0-1	0	Wake on LAN (WoL) detection logic 0 - Disables Wake on LAN detection 1 - Enables Wake on LAN detection. Note: Supports Wake on LAN using AMD's Magic Packet™ Detection technology
PCS			
RX_EB_RAM_TYPE	1:Fabric 2:LSRAM 3:uSRAM	LSRAM	EB RAM Type: This parameter is used to select RAM type for the Elastic Buffer. uSRAM and LSRAM are embedded memory blocks. When Fabric is selected, core implements RAM using fabric resources that is, FFs and LUTs
Note: The elastic buffer's clock jitter permissible limit is -100 PPM to +100 PPM It is recommended to maintain a minimum difference of 8 words between the Almost-Full (RX_EB_AFULL_THR) and Almost-Empty (RX_EB_AEMPTY_THR) thresholds in the elastic buffer.			
RX_EB_AFULL_THR	12 - 60	40	RX Elastic Buffer Almost Full Threshold Sets elastic buffer almost full threshold
RX_EB_AEMPTY_THR	4 - 52	20	RX Elastic Buffer Almost Empty Threshold Sets elastic buffer almost empty threshold

2.2. Input and Output Signals [\(Ask a Question\)](#)

The following table lists the clock ports for CoreGbE_MR.

Table 2-2. CoreGbE_MR Clock Ports

Port Name	Width	Direction	Description
ACLK	1	Input	AXI4 Lite clock
SYS_CLK	1	Input	Clock for the system side clock domain
XCVR_TX_CLK	1	Input	Transmit clock for the line side clock domain
XCVR_RX_CLK	1	Input	Receive clock for the line side clock domain

The following table lists the input and output ports of CoreGbE_MR. The **Clock Domain** column in the table indicates the input ports and the output ports expected to be synchronized in the respective clock domain.

Table 2-3. CoreGbE_MR Input and Output Ports

Port Name	Width	Direction	Clock Domain	Description
Reset Ports				
SYS_TX_RESETN	1	Input	SYS_CLK	Active low reset of the transmit core with reference to the SYS_CLK domain. Note: This IP core do not implement any internal reset synchronizers.
SYS_RX_RESETN	1	Input	SYS_CLK	Active low synchronous reset of the receive core with reference to the SYS_CLK domain. Note: This IP core do not implement any internal reset synchronizers.
XCVR_TX_RESETN	1	Input	XCVR_TX_CLK	Active low reset of the transmit core with reference to the XCVR_TX_CLK domain. Note: This IP core do not implement any internal reset synchronizers.
XCVR_RX_RESETN	1	Input	XCVR_RX_CLK	Active low reset of the transmit core with reference to the XCVR_RX_CLK domain. Note: This IP core do not implement any internal reset synchronizers.
ARESETN	1	Input	ACLK	Active low synchronous reset.
Client Transmit Packet Interface (AXI4-Stream)				
AXI4S_TX_TARG_TVALID	1	Input	SYS_CLK	AXI4-Stream valid indicates that the initiator is driving a valid transfer.
AXI4S_TX_TARG_TREADY	1	Output	SYS_CLK	AXI4-Stream ready indicates that the target can accept a transfer in the current cycle. Core de-asserts this signal when transmit buffer is full.

Table 2-3. CoreGbE_MR Input and Output Ports (continued)

Port Name	Width	Direction	Clock Domain	Description
AXI4S_TX_TARG_TDATA	32	Input	SYS_CLK	AXI4-Stream data is the primary payload that is used to provide the data that is passing across the interface.
AXI4S_TX_TARG_TKEEP	4	Input	SYS_CLK	AXI4-Stream byte qualifier that indicates whether the content of the associated byte of data is processed as part of the data stream. Associated bytes that have the AXI4S_TX_TARG_TKEEP byte qualifier de-asserted are null bytes and can be removed from the data stream. Core does not support null bytes between the packet boundaries. Null bytes are supported when AXI4S_TX_TARG_TLAST is asserted that is, at the packet boundary.
AXI4S_TX_TARG_TLAST	1	Input	SYS_CLK	AXI4-Stream last indicates the boundary of a packet.
Client Transmit Status Interface				
SYS_MAC_TX_ERR_FIFO_UNDERRUN	1	Output	XCVR_TX_CLK	Transmit FIFO underrun error. This signal asserts for one cycle on a Tx FIFO underruns event. The event happens when the user does not deliver data fast enough.
MAC_TX_STATS_VECTOR	40	Output	XCVR_TX_CLK	The transmit statistics bus.
Client Receive Packet Interface (AXI4-Stream)				
AXI4S_RX_INITR_TVALID	1	Output	SYS_CLK	AXI4-Stream valid indicates that the initiator is driving a valid transfer.
AXI4S_RX_INITR_TDATA	32	Output	SYS_CLK	AXI4-Stream data.
AXI4S_RX_INITR_TREADY	1	Input	SYS_CLK	AXI4-Stream ready indicates that the target can accept a transfer in the current cycle. This port shall be tied high by the user in case if Pause is not enabled in CoreGbE_MR.

Table 2-3. CoreGbE_MR Input and Output Ports (continued)

Port Name	Width	Direction	Clock Domain	Description
AXI4S_RX_INITR_TKEEP	4	Output	SYS_CLK	AXI4-Stream byte qualifier that indicates whether the content of the associated byte of data is processed as part of the data stream. Associated bytes that have the AXI4S_RX_INITR_TKEEP byte qualifier de-asserted are null bytes and can be removed from the data stream. Core does not support null bytes between the packet boundaries. Null bytes are supported when AXI4S_RX_INITR_TLAST is asserted that is, at the packet boundary.
AXI4S_RX_INITR_TLAST	1	Output	SYS_CLK	AXI4-Stream last indicates the boundary of a packet. This port can be used as an EOP boundary of the packet.

Table 2-3. CoreGbE_MR Input and Output Ports (continued)

Port Name	Width	Direction	Clock Domain	Description
AXI4S_RX_INITR_TUSER	74	Output	SYS_CLK	Bit[73: 10] - Rx preamble. This signal contains the receive preamble and is valid with start of the transfer. Bit[9] - Reserved. Bit[8] - Rx_error. This signal indicates an error with the associated packet. The signal asserts when the error is discovered and stay asserted until AXI4S_RX_INITR_TLAST asserts. The source of the error can be FCS error, length error, framing error, pause frame, or an error received from the PCS layer during the packet reception. Bit[7] - Unused Bit[6] - Rx frame error. This signal indicates a PCS error or packet framing error with the packet. The signal asserts when the error is discovered and stay asserted until AXI4S_RX_INITR_TLAST asserts. When this signal asserts, Rx_error also asserts. Bit[5] - Rx CRC error. This signal indicates an FCS error with the associated packet. The signal asserts only when AXI4S_RX_INITR_TLAST asserts. When this signal asserts, Rx_error also asserts. Bit[4] - Rx FCS stomp error. This signal indicates an FCS stomp with the associated packet. The signal assert only when AXI4S_RX_INITR_TLAST transitions to assert. When this signal asserts, Rx_error also asserts. Note: Stomped packet is also flagged as a CRC errored packet. Hence, you can ignore the signal. Bit[3] - Rx short frame error. This signal indicates that the packet is less than 64 bytes long. The

Table 2-3. CoreGbE_MR Input and Output Ports (continued)

Port Name	Width	Direction	Clock Domain	Description
Client Receive Status Interface				
SYS_MAC_RX_FIFO_OVERFLOW	1	Output	XCVR_TX_CLK	Receive FIFO overflow error. This signal asserts for one cycle on an Rx FIFO overflow event. This happens only if SYS_CLK is not running fast enough. Note: Packets are dropped internally if RX FIFO is in Store-n-Forward mode.
MAC_RX_STATS_VECTOR	32	Output	XCVR_TX_CLK	The receive statistics bus.
AXI4 Lite Interface				
AXI4L_ARVALID	1	Input	ACLK	Read address valid
AXI4L_ARREADY	1	Output	ACLK	Read address ready
AXI4L_ARADDR	16	Input	ACLK	Read address
AXI4L_RVALID	1	Output	ACLK	Read data valid
AXI4L_RREADY	1	Input	ACLK	Read data ready
AXI4L_RDATA	32	Output	ACLK	Read data
AXI4L_RRESP	2	Output	ACLK	Read response
AXI4L_AWVALID	1	Input	ACLK	Write address valid
AXI4L_AWREADY	1	Output	ACLK	Write address ready
AXI4L_AWADDR	16	Input	ACLK	Write address
AXI4L_WVALID	1	Input	ACLK	Write data valid
AXI4L_WREADY	1	Output	ACLK	Write data ready
AXI4L_WDATA	32	Input	ACLK	Write data
AXI4L_WSTRB	4	Input	ACLK	Write strobe
AXI4L_BVALID	1	Output	ACLK	Write response valid
AXI4L_BREADY	1	Input	ACLK	Write response ready
AXI4L_BRESP	2	Output	ACLK	Write response
XCVR Interface (PMA only mode)				
LANEX_TX_DATA	20	Output	XCVR_TX_CLK	Transmit data towards transceiver
LANEX_RX_DATA	20	Input	XCVR_RX_CLK	Receive data from the transceiver
Miscellaneous Signals				
SYNC	1	Output	XCVR_TX_CLK	Receive link sync status.
WOL_DETECT	1	Output	XCVR_TX_CLK	Wake on LAN detected status. Note: This signal is asserted for a single cycle of XCVR_TX_CLK when magic packet is detected.

Table 2-3. CoreGbE_MR Input and Output Ports (continued)

Port Name	Width	Direction	Clock Domain	Description
TX_FIFO_SB_CORRECT	1	Output	XCVR_TX_CLK	1-bit error correction flag indicator for MAC TX FIFO, enabled when ECC_ENABLE parameter is set in PolarFire and PolarFire SoC families.
TX_FIFO_DB_DETECT	1	Output	XCVR_TX_CLK	2-bit error detection flag indicator for MAC TX FIFO, enabled when ECC_ENABLE parameter is set in PolarFire and PolarFire SoC families.
RX_FIFO_SB_CORRECT	1	Output	XCVR_TX_CLK	1-bit error correction flag indicator for MAC RX FIFO, enabled when ECC_ENABLE parameter is set in PolarFire and PolarFire SoC families.
RX_FIFO_DB_DETECT	1	Output	XCVR_TX_CLK	2-bit error detection flag indicator for MAC RX FIFO, enabled when ECC_ENABLE parameter is set in PolarFire and PolarFire SoC families.
EB_SB_CORRECT	1	Output	XCVR_TX_CLK	1-bit error correction flag indicator for RX Elastic Buffer, enabled when ECC_ENABLE parameter is set in PolarFire and PolarFire SoC families.
EB_DB_DETECT	1	Output	XCVR_TX_CLK	2-bit error detection flag indicator for RX Elastic Buffer, enabled when ECC_ENABLE parameter is set in PolarFire and PolarFire SoC families.
Debug Signals				
EB_OVERFLOW	1	Output	XCVR_TX_CLK	Receive Elastic buffer overflow error. This signal is asserted on the elastic buffer overflow event.
EB_UNDERRUN	1	Output	XCVR_TX_CLK	Receive Elastic buffer underrun error. This signal is asserted on the elastic buffer underrun event.

Table 2-3. CoreGbE_MR Input and Output Ports (continued)

Port Name	Width	Direction	Clock Domain	Description																						
PCS_RX_SYNC_FSM_CU R_STATE	4	Output	XCVR_TX_CLK	This port indicates the current state of PCS Receive Synchronization State machine. State Encodings:																						
				<table><tr><th>State</th><th>Encoding [3:0]</th></tr><tr><td>LOSS_OF_SYNC</td><td>4'b0000</td></tr><tr><td>ACQUIRE_SYNC_1</td><td>4'b0001</td></tr><tr><td>ACQUIRE_SYNC_2</td><td>4'b0010</td></tr><tr><td>SYNC_ACQUIRED_1</td><td>4'b0011</td></tr><tr><td>SYNC_ACQUIRED_2A</td><td>4'b0100</td></tr><tr><td>SYNC_ACQUIRED_2</td><td>4'b0101</td></tr><tr><td>SYNC_ACQUIRED_3A</td><td>4'b0110</td></tr><tr><td>SYNC_ACQUIRED_3</td><td>4'b0111</td></tr><tr><td>SYNC_ACQUIRED_4A</td><td>4'b1000</td></tr><tr><td>SYNC_ACQUIRED_4</td><td>4'b1001</td></tr></table>	State	Encoding [3:0]	LOSS_OF_SYNC	4'b0000	ACQUIRE_SYNC_1	4'b0001	ACQUIRE_SYNC_2	4'b0010	SYNC_ACQUIRED_1	4'b0011	SYNC_ACQUIRED_2A	4'b0100	SYNC_ACQUIRED_2	4'b0101	SYNC_ACQUIRED_3A	4'b0110	SYNC_ACQUIRED_3	4'b0111	SYNC_ACQUIRED_4A	4'b1000	SYNC_ACQUIRED_4	4'b1001
				State	Encoding [3:0]																					
				LOSS_OF_SYNC	4'b0000																					
				ACQUIRE_SYNC_1	4'b0001																					
				ACQUIRE_SYNC_2	4'b0010																					
				SYNC_ACQUIRED_1	4'b0011																					
				SYNC_ACQUIRED_2A	4'b0100																					
				SYNC_ACQUIRED_2	4'b0101																					
				SYNC_ACQUIRED_3A	4'b0110																					
				SYNC_ACQUIRED_3	4'b0111																					
				SYNC_ACQUIRED_4A	4'b1000																					
				SYNC_ACQUIRED_4	4'b1001																					

3. Timing Diagrams [\(Ask a Question\)](#)

This section discusses various timing diagrams.

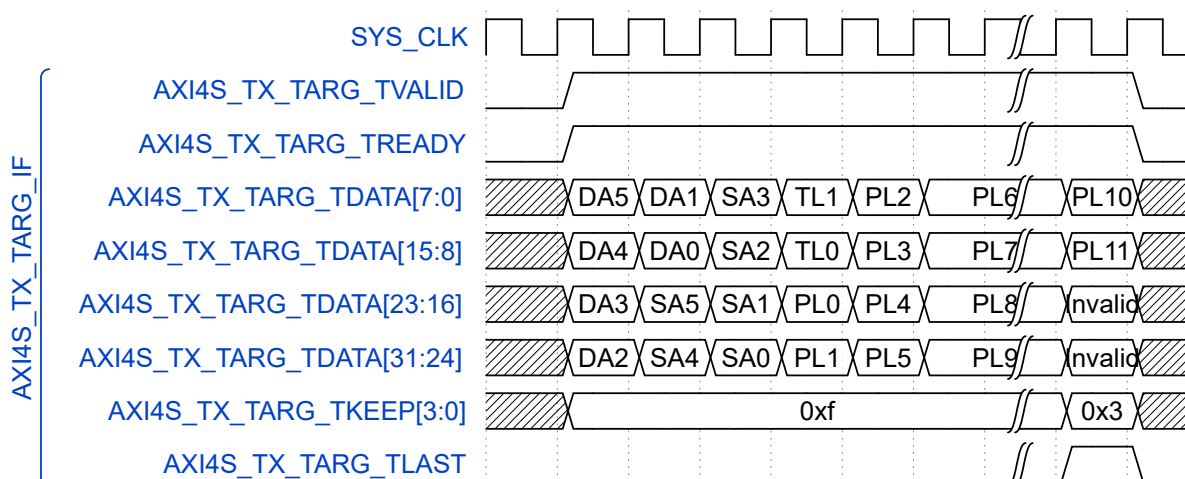
The timing diagrams for the AXI4Stream interface are shown below with following characteristics:

- DA0: Indicates Destination Address Byte 0
- DA1: Indicates Destination Address Byte 1 and ... so on
- SA0: Indicates Source Address Byte 0
- SA1: Indicates Source Address Byte 1 and ... so on
- LT0: Indicates Length/Type Byte 0
- LT1: Indicates Length/Type Byte 1 and ... so on
- D0: Indicates Payload Byte 0
- D1: Indicates Payload Byte 1 and ... so on
- Data on the AXI4Stream interface is expected or driven in big endian format.

3.1. AXI4Stream TX Target interface [\(Ask a Question\)](#)

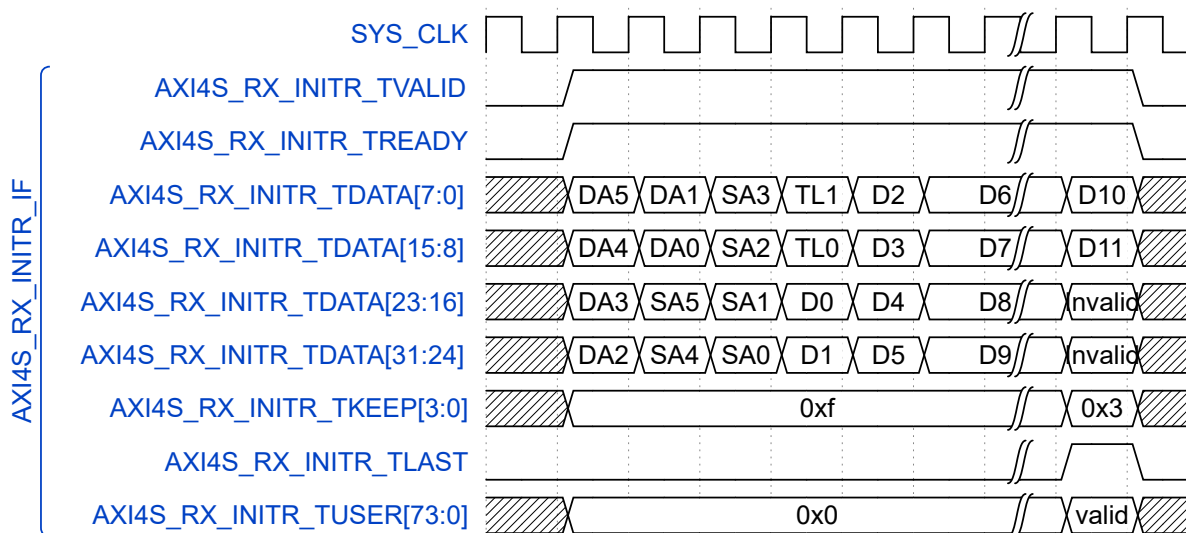
The following figure shows the timing diagram for AXI4Stream TX Target interface.

Figure 3-1. AXI4Stream TX Target Interface



3.2. AXI4Stream RX Initiator Interface [\(Ask a Question\)](#)

The following figure shows the timing diagram for AXI4Stream RX Initiator interface.

Figure 3-2. AXI4Stream RX Initiator Interface

4. Implementation of CoreGbE_MR IP in Libero Design Suite [\(Ask a Question\)](#)

The CoreGbE_MR IP is implemented in the Libero Design Suite by following a series of steps that ensure proper integration and functionality within the design environment.

For integration, perform the following steps:

Steps for Integration

1. Open the Libero Design Suite and create a new project or open an existing project.
2. Import the CoreGbE_MR IP into the project by selecting the appropriate IP catalog and adding it to the design.
3. Configure the CoreGbE_MR IP parameters as required for the specific application.
4. Connect the CoreGbE_MR IP to other design components using the design canvas and ensure proper signal routing.
5. Run design rule checks to verify the integration and resolve any issues that may arise.
6. Synthesize the design to generate the necessary netlist and other implementation files.
7. Perform place and route operations to map the design onto the target FPGA device.
8. Generate the bitstream file for programming the FPGA with the integrated CoreGbE_MR IP.
9. Program the FPGA and verify the functionality of the CoreGbE_MR IP within the overall design.



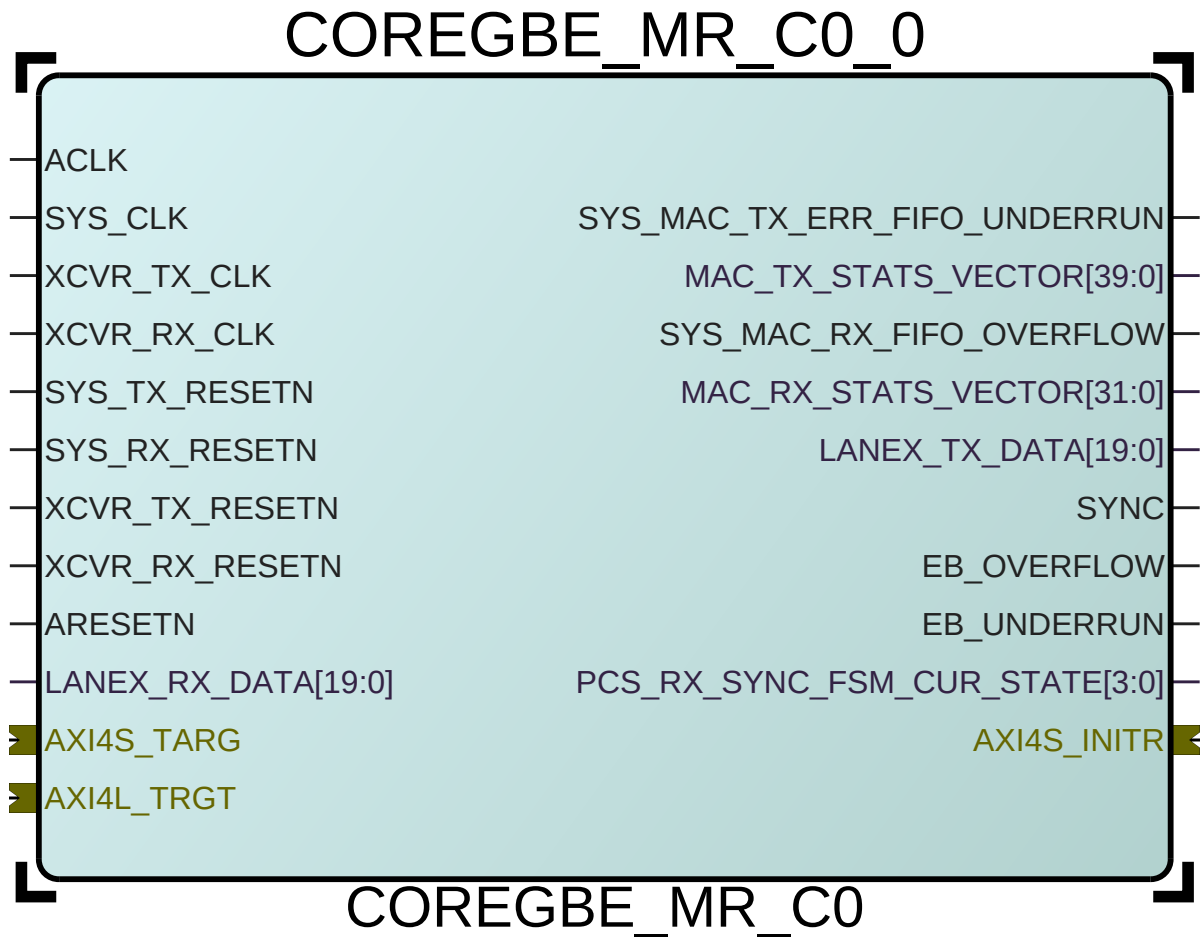
Important:

For information on using SmartDesign to instantiate, configure, connect, and generate cores, see the [Libero SOC online help](#).

4.1. SmartDesign [\(Ask a Question\)](#)

The following figure shows an example of an instantiated view of CoreGbE_MR on the SmartDesign canvas.

Figure 4-1. Instantiation of CoreGbE_MR on Smart Design Canvas



Steps for Instantiation, Configuration, and Core Generation in SmartDesign

1. Open the SmartDesign tool and navigate to the IP Catalog.
2. Search for the CoreGbE_MR IP in the catalog.
3. Drag and drop the CoreGbE_MR IP into your design canvas.
4. To open the configuration window, double-click the **CoreGbE_MR IP block**.
5. Configure the IP parameters as per your design requirements.
6. Click **OK** to save the configuration settings.
7. To generate the core, in the SmartDesign toolbar, click **Generate**.
8. Verify the generated core and integrate it into your overall design.

4.1.1. Configuration [\(Ask a Question\)](#)

This section describes how to configure the CoreGbE_MR instance using the configuration GUI.

To configure the CoreGbE_MR IP instance, perform the following steps:

1. Open the configuration GUI.
2. Select the CoreGbE_MR IP instance from the list of available IPs.
3. Adjust the configuration settings as required.
4. Save the configuration.

Figure 4-2. CoreGbE_MR Configurator

The screenshot shows the 'CoreGbE_MR Configurator' window with the 'Configuration' tab active. The window has five tabs: 'Configuration', 'MAC', 'TX Stat Counters', 'RX Stat Counters', and 'PCS'. In the 'Configuration' tab, there are four settings: 'ECC Enable' with an unchecked checkbox, 'Reset Type' with a dropdown menu showing 'Asynchronous', 'Testbench' with a dropdown menu showing 'User', and 'License' with the text 'Obfuscated'.

4.1.2. Synthesis in Libero SoC [\(Ask a Question\)](#)

To run synthesis, perform the following steps:

1. With the configuration selected in the configuration GUI, set the design root appropriately.
2. Under **Implement Design**, on the **Design Flow** tab, right click **Synthesize** and click **Run**.

Step-by-step guide to synthesizing the CoreGbE_MR IP

1. Open the Libero SoC software.
2. Create a new project or open an existing project.
3. Import the CoreGbE_MR IP into your project.
4. Configure the CoreGbE_MR IP according to your design requirements.
5. Run the synthesis tool to generate the synthesized netlist.
6. Review the synthesis report for any warnings or errors.
7. Make any necessary adjustments to the design and re-run the synthesis if needed.
8. Once the synthesis is successful, proceed to the implementation phase.

4.1.3. Place-and-Route in Libero SoC [\(Ask a Question\)](#)

To run the place and route, perform the following steps:

1. With the configuration selected in the configuration GUI, set the design root appropriately.
2. Under **Implement Design**, on the **Design Flow** tab, right click **Place and Route** and click **Run**.

Steps for Running Place-and-Route

To run place-and-route in Libero SoC, perform the following steps:

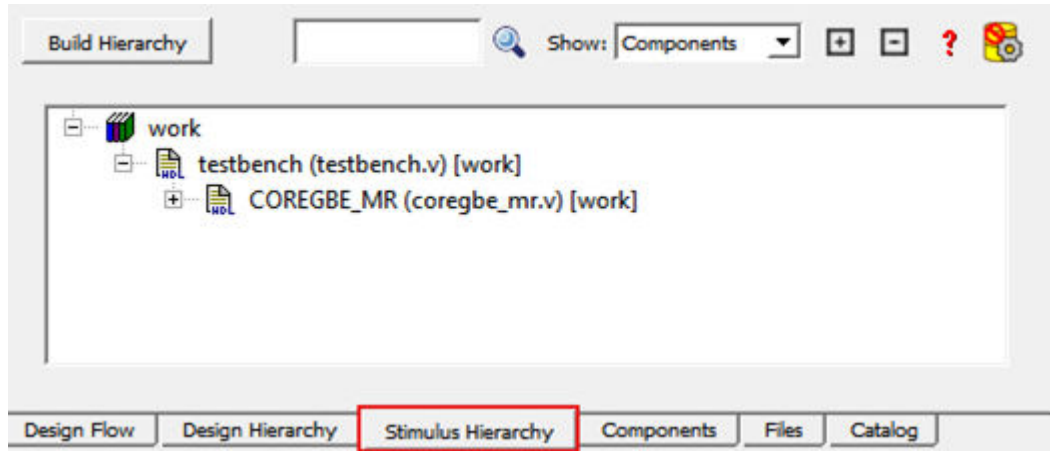
1. Open your project in Libero SoC.
2. Ensure that the design is synthesized and optimized.
3. Navigate to the Place-and-Route section in the design flow.
4. Configure the place-and-route settings as required for your design.
5. Run the place-and-route process.
6. Review the place-and-route report for any issues or optimizations.
7. Make any necessary adjustments and re-run the place-and-route if needed.

4.1.4. Simulation Flows [\(Ask a Question\)](#)

SmartDesign and Libero SoC facilitate running a user testbench for CoreGbE_MR. To run the user testbench, perform the following steps.

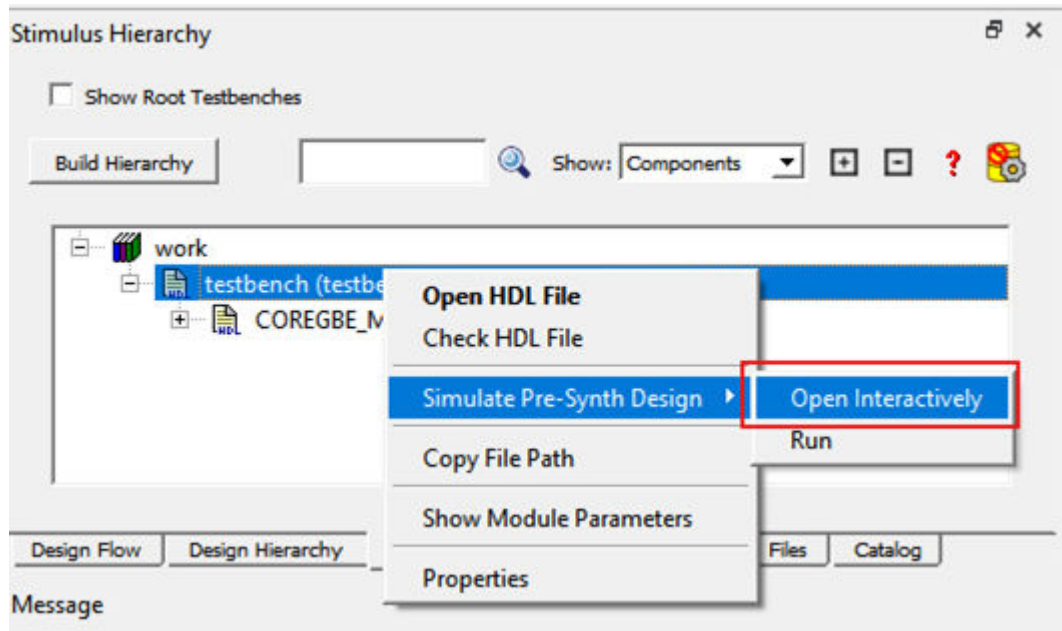
1. Set the design root to the CoreGbE_MR instantiation in the Libero SoC design hierarchy pane.
2. Click the **Stimulus Hierarchy** tab.

Figure 4-3. Stimulus Hierarchy Tab



3. Right-click testbench, under **Simulate Pre-Synthesis Design**, select **Open Interactively**.

Figure 4-4. Run Simulation



Separate Modelsim window opens; wait for Modelsim to complete the simulation and display results **Transcript** tab in Modelsim tool.

4.2. Verification [\(Ask a Question\)](#)

This section describes verification of the CoreGbE_MR.

4.3. Testbench [\(Ask a Question\)](#)

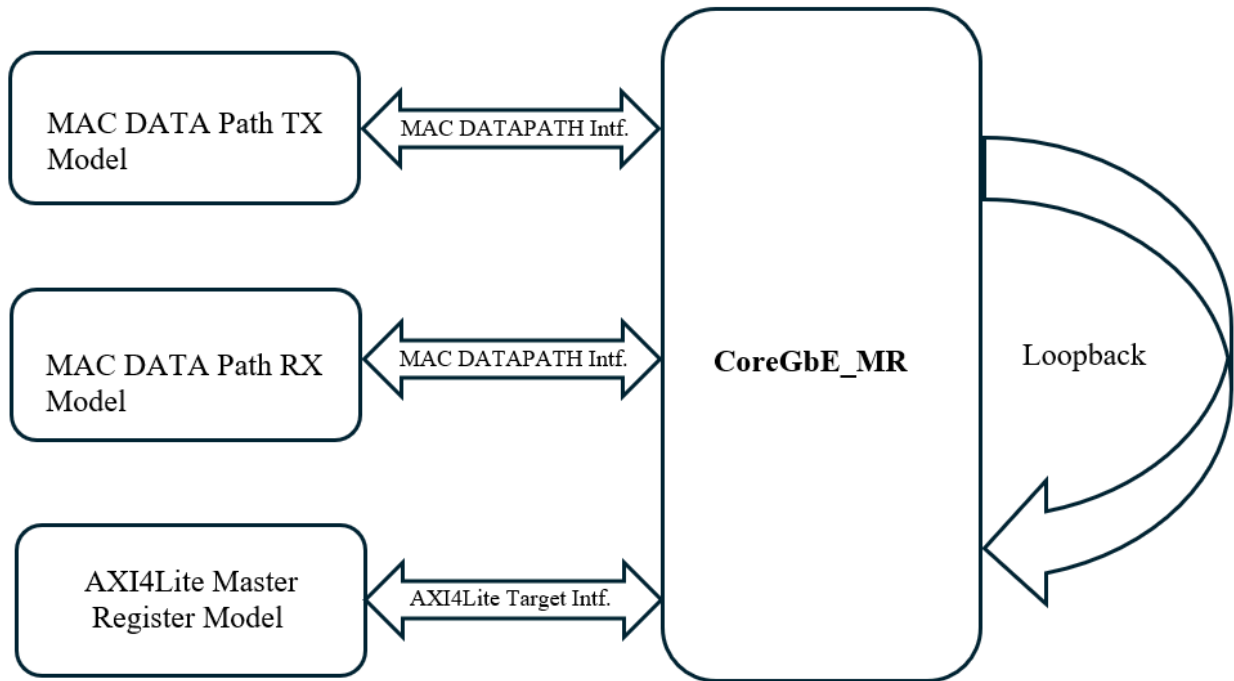
A unified testbench is used to verify and test CoreGbE_MR called as user testbench.

4.3.1. User Testbench [\(Ask a Question\)](#)

The following figure shows the user simulation testbench and it includes the instantiation of the CoreGbE_MR macro.

You can find all the testbench environment files from the path - <project_directory/component/Microchip/DirectCore/CoreGbE_MR/IP Core Version Number (ex 2.0.100)>/rtl/vlog/test/user.

Figure 4-5. CoreGbE_MR User Testbench



5. Design Constraints [\(Ask a Question\)](#)

This section describes the design constraints of the CoreGbE_MR.

5.1. Timing Constraints [\(Ask a Question\)](#)

This section provides the information on the timing constraints required for CoreGbE_MR.

CoreGbE_MR uses the following clocks:

- ACLK: AXI4 Lite clock
- SYS_CLK: Clock for the system side clock domain
- XCVR_TX_CLK: Transmit clock for the line side clock domain
- XCVR_RX_CLK: Receive clock for the line side clock domain

Note: The source clock name used in the reference sdc file is for reference only. The source name might be different in your design, and you must change the clock name in the constraint accordingly.

You can find reference sdc timing constraint file from the following path:

```
<project_directory/component/Microchip/DirectCore/CoreGbE_MR/ (example  
2.0.xxx)/constraints/CoreGbE_MR.sdc>
```

6. Register Map and Descriptions [\(Ask a Question\)](#)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CORE_VER	7:0								
		15:8								
		23:16	MINOR_VER[7:0]							
		31:24	MAJOR_VER[7:0]							
0x04	MAC_TX_PARAM1	7:0	MAC_TX_PARAM1[7:0]							
		15:8	MAC_TX_PARAM1[15:8]							
		23:16	MAC_TX_PARAM1[23:16]							
		31:24	MAC_TX_PARAM1[31:24]							
0x08	MAC_TX_PARAM2	7:0	MAC_TX_PARAM2[7:0]							
		15:8	MAC_TX_PARAM2[15:8]							
		23:16	MAC_TX_PARAM2[23:16]							
		31:24	MAC_TX_PARAM2[31:24]							
0x0C	MAC_RX_PARAM1	7:0	MAC_RX_PARAM1[7:0]							
		15:8	MAC_RX_PARAM1[15:8]							
		23:16	MAC_RX_PARAM1[23:16]							
		31:24	MAC_RX_PARAM1[31:24]							
0x10	MAC_RX_PARAM2	7:0	MAC_RX_PARAM2[7:0]							
		15:8	MAC_RX_PARAM2[15:8]							
		23:16	MAC_RX_PARAM2[23:16]							
		31:24	MAC_RX_PARAM2[31:24]							
0x14 ... 0x1F	Reserved									
0x20	MAC_ADDR_UPPER	7:0								
		15:8	MAC ADDR BYTE 5[7:0]							
		23:16								
		31:24								
0x24	MAC_ADDR_LOWER	7:0	MAC ADDR BYTE 0[7:0]							
		15:8	MAC ADDR BYTE 1[7:0]							
		23:16	MAC ADDR BYTE 2[7:0]							
		31:24	MAC ADDR BYTE 3[7:0]							
0x28 ... 0xFF	Reserved									
0x0100	MAC_TX_CFG	7:0	MAC_TX_MAX_PKT_LEN[3:0]				MAC_TX_PRE AMBLE_EN	MAC_TX_PREAMBLE_WCM1[2:0]		
		15:8	MAC_TX_MAX_PKT_LEN[11:4]							
		23:16	MAC_TX_FCS_ STOMP	MAC_TX_FCS_ ERR	MAC_TX_FCS_ INS	MAC_TX_PAD _EN	MAC_TX_MAX_PKT_LEN[15:12]			
		31:24	MAC_TX_EN		MAC_TX_IFG_CNT[5:0]					
0x0104	MAC_TX_PRE_UPPE R	7:0	MAC TX PREAMBLE UPPER 32 BITS[7:0]							
		15:8	MAC TX PREAMBLE UPPER 32 BITS[15:8]							
		23:16	MAC TX PREAMBLE UPPER 32 BITS[23:16]							
		31:24	MAC TX PREAMBLE UPPER 32 BITS[31:24]							
0x0108	MAC_TX_PRE_LOWE R	7:0	MAC TX PREAMBLE LOWER 32 BITS[7:0]							
		15:8	MAC TX PREAMBLE LOWER 32 BITS[15:8]							
		23:16	MAC TX PREAMBLE LOWER 32 BITS[23:16]							
		31:24	MAC TX PREAMBLE LOWER 32 BITS[31:24]							
0x010C ... 0x016F	Reserved									
0x0170	MAC_TX_PAUSE_TI MER	7:0	MAC TX PAUSE TIMER[7:0]							
		15:8	MAC TX PAUSE TIMER[15:8]							
		23:16								
		31:24								
0x0174 ... 0x017F	Reserved									

Register Map and Descriptions (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0180	MAC_RX_CFG	7:0	MAC_RX_MAX_PKT_LEN[3:0]					MAC_RX_PREAMBLE_WCM1[2:0]		
		15:8	MAC_RX_MAX_PKT_LEN[11:4]							
		23:16			MAC_RX_PAD REMOVAL	MAC_RX_FCS_ REMOVE	MAC_RX_MAX_PKT_LEN[15:12]			
		31:24	MAC_RX_EN	WOL_EN						
0x0184 ... 0x018F	Reserved									
0x0190	MAC_RX_FRMFIL_P KT	7:0	RX_LS_ERR	RX_LL_ERR	RX_LC_ERR	RX_FCS_ERR	RX_PCS_ERR			
		15:8		RX_VLAN	RX_CNTL_UN SUP	RX_CNTL_PAU SE	RX_CNTL	RX_UCAST	RX_BCAST	RX_MCAST
		23:16								
		31:24								
0x0194 ... 0x019F	Reserved									
0x01A0	MAC_RX_FRMFIL_H TR0	7:0	MAC RX HASH TABLE REGISTER 1[7:0]							
		15:8	MAC RX HASH TABLE REGISTER 1[15:8]							
		23:16	MAC RX HASH TABLE REGISTER 1[23:16]							
		31:24	MAC RX HASH TABLE REGISTER 1[31:24]							
0x01A4	MAC_RX_FRMFIL_H TR1	7:0	MAC RX HASH TABLE REGISTER 2[7:0]							
		15:8	MAC RX HASH TABLE REGISTER 2[15:8]							
		23:16	MAC RX HASH TABLE REGISTER 2[23:16]							
		31:24	MAC RX HASH TABLE REGISTER 2[31:24]							
0x01A8 ... 0x01EF	Reserved									
0x01F0	MAC_RX_PAUSE_W M	7:0	MAC RX PAUSE LWM[7:0]							
		15:8				MAC RX PAUSE LWM[12:8]				
		23:16	MAC RX PAUSE HWM[7:0]							
		31:24				MAC RX PAUSE HWM[12:8]				
0x01F4	MAC_RX_PAUSE_RT X	7:0	MAC RX PAUSE RETRANSMISSION[7:0]							
		15:8	MAC RX PAUSE RETRANSMISSION[15:8]							
		23:16								
		31:24								
0x01F8 ... 0x01FF	Reserved									
0x0200	MAC_TX_PKT	7:0	MAC_TPKT[7:0]							
		15:8	MAC_TPKT[15:8]							
		23:16	MAC_TPKT[23:16]							
		31:24	MAC_TPKT[31:24]							
0x0204	MAC_TX_ERR	7:0	MAC_TERR[7:0]							
		15:8	MAC_TERR[15:8]							
		23:16	MAC_TERR[23:16]							
		31:24	MAC_TERR[31:24]							
0x0208	MAC_TX_LL_ERR	7:0	MAC_TERR_LL[7:0]							
		15:8	MAC_TERR_LL[15:8]							
		23:16	MAC_TERR_LL[23:16]							
		31:24	MAC_TERR_LL[31:24]							
0x020C	MAC_TX_LC_ERR	7:0	MAC_TERR_LC[7:0]							
		15:8	MAC_TERR_LC[15:8]							
		23:16	MAC_TERR_LC[23:16]							
		31:24	MAC_TERR_LC[31:24]							
0x0210	MAC_TX_LS_ERR	7:0	MAC_TERR_LS[7:0]							
		15:8	MAC_TERR_LS[15:8]							
		23:16	MAC_TERR_LS[23:16]							
		31:24	MAC_TERR_LS[31:24]							

Register Map and Descriptions (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0214	MAC_TX_FCS_ERR	7:0					MAC_TERR_FCS[7:0]			
		15:8					MAC_TERR_FCS[15:8]			
		23:16					MAC_TERR_FCS[23:16]			
		31:24					MAC_TERR_FCS[31:24]			
0x0218	MAC_TX_FRM_ERR	7:0					MAC_TERR_FRM[7:0]			
		15:8					MAC_TERR_FRM[15:8]			
		23:16					MAC_TERR_FRM[23:16]			
		31:24					MAC_TERR_FRM[31:24]			
0x021C	MAC_TX_BCAST	7:0					MAC_TBICAST[7:0]			
		15:8					MAC_TBICAST[15:8]			
		23:16					MAC_TBICAST[23:16]			
		31:24					MAC_TBICAST[31:24]			
0x0220	MAC_TX_MCAST	7:0					MAC_TMCAST[7:0]			
		15:8					MAC_TMCAST[15:8]			
		23:16					MAC_TMCAST[23:16]			
		31:24					MAC_TMCAST[31:24]			
0x0224	MAC_TX_PF	7:0					MAC_TPF[7:0]			
		15:8					MAC_TPF[15:8]			
		23:16					MAC_TPF[23:16]			
		31:24					MAC_TPF[31:24]			
0x0228	MAC_TX_CF	7:0					MAC_TCF[7:0]			
		15:8					MAC_TCF[15:8]			
		23:16					MAC_TCF[23:16]			
		31:24					MAC_TCF[31:24]			
0x022C	MAC_TX_VLAN	7:0					MAC_TVLAN[7:0]			
		15:8					MAC_TVLAN[15:8]			
		23:16					MAC_TVLAN[23:16]			
		31:24					MAC_TVLAN[31:24]			
0x0230	MAC_TX_PAD	7:0					MAC_TPAD[7:0]			
		15:8					MAC_TPAD[15:8]			
		23:16					MAC_TPAD[23:16]			
		31:24					MAC_TPAD[31:24]			
0x0234	MAC_TX_64B	7:0					MAC_T64[7:0]			
		15:8					MAC_T64[15:8]			
		23:16					MAC_T64[23:16]			
		31:24					MAC_T64[31:24]			
0x0238	MAC_TX_127B	7:0					MAC_T127[7:0]			
		15:8					MAC_T127[15:8]			
		23:16					MAC_T127[23:16]			
		31:24					MAC_T127[31:24]			
0x023C	MAC_TX_255B	7:0					MAC_T255[7:0]			
		15:8					MAC_T255[15:8]			
		23:16					MAC_T255[23:16]			
		31:24					MAC_T255[31:24]			
0x0240	MAC_TX_511B	7:0					MAC_T511[7:0]			
		15:8					MAC_T511[15:8]			
		23:16					MAC_T511[23:16]			
		31:24					MAC_T511[31:24]			
0x0244	MAC_TX_1KB	7:0					MAC_T1K[7:0]			
		15:8					MAC_T1K[15:8]			
		23:16					MAC_T1K[23:16]			
		31:24					MAC_T1K[31:24]			
0x0248	MAC_TX_MAXB	7:0					MAC_TMAX_NVLAN[7:0]			
		15:8					MAC_TMAX_NVLAN[15:8]			
		23:16					MAC_TMAX_NVLAN[23:16]			
		31:24					MAC_TMAX_NVLAN[31:24]			
0x024C	MAC_TX_MAXB_VLAN	7:0					MAC_TMAXB_VLAN[7:0]			
		15:8					MAC_TMAXB_VLAN[15:8]			
		23:16					MAC_TMAXB_VLAN[23:16]			
		31:24					MAC_TMAXB_VLAN[31:24]			

Register Map and Descriptions (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0250	MAC_TX_GTMAXB	7:0	MAC_TGTMAXB[7:0]							
		15:8	MAC_TGTMAXB[15:8]							
		23:16	MAC_TGTMAXB[23:16]							
		31:24	MAC_TGTMAXB[31:24]							
0x0254 ... 0x025B	Reserved									
0x025C	MAC_TX_FIFO_SBCOR	7:0	MAC_TFIFO_SBCOR[7:0]							
		15:8	MAC_TFIFO_SBCOR[15:8]							
		23:16	MAC_TFIFO_SBCOR[23:16]							
		31:24	MAC_TFIFO_SBCOR[31:24]							
0x0260	MAC_TX_FIFO_DBDET	7:0	MAC_TFIFO_DBDET[7:0]							
		15:8	MAC_TFIFO_DBDET[15:8]							
		23:16	MAC_TFIFO_DBDET[23:16]							
		31:24	MAC_TFIFO_DBDET[31:24]							
0x0264 ... 0x03FF	Reserved									
0x0400	MAC_RX_PKT	7:0	MAC_RPKT[7:0]							
		15:8	MAC_RPKT[15:8]							
		23:16	MAC_RPKT[23:16]							
		31:24	MAC_RPKT[31:24]							
0x0404	MAC_RX_ERR	7:0	MAC_RERR[7:0]							
		15:8	MAC_RERR[15:8]							
		23:16	MAC_RERR[23:16]							
		31:24	MAC_RERR[31:24]							
0x0408	MAC_RX_LL_ERR	7:0	MAC_RERR_LL[7:0]							
		15:8	MAC_RERR_LL[15:8]							
		23:16	MAC_RERR_LL[23:16]							
		31:24	MAC_RERR_LL[31:24]							
0x040C	MAC_RX_LC_ERR	7:0	MAC_RERR_LC[7:0]							
		15:8	MAC_RERR_LC[15:8]							
		23:16	MAC_RERR_LC[23:16]							
		31:24	MAC_RERR_LC[31:24]							
0x0410	MAC_RX_LS_ERR	7:0	MAC_RERR_LS[7:0]							
		15:8	MAC_RERR_LS[15:8]							
		23:16	MAC_RERR_LS[23:16]							
		31:24	MAC_RERR_LS[31:24]							
0x0414	MAC_RX_FCS_ERR	7:0	MAC_RERR_FCS[7:0]							
		15:8	MAC_RERR_FCS[15:8]							
		23:16	MAC_RERR_FCS[23:16]							
		31:24	MAC_RERR_FCS[31:24]							
0x0418	MAC_RX_FRM_ERR	7:0	MAC_RERR_FRM[7:0]							
		15:8	MAC_RERR_FRM[15:8]							
		23:16	MAC_RERR_FRM[23:16]							
		31:24	MAC_RERR_FRM[31:24]							
0x041C	MAC_RX_BCAST	7:0	MAC_RBCAST[7:0]							
		15:8	MAC_RBCAST[15:8]							
		23:16	MAC_RBCAST[23:16]							
		31:24	MAC_RBCAST[31:24]							
0x0420	MAC_RX_MCAST	7:0	MAC_RMCAST[7:0]							
		15:8	MAC_RMCAST[15:8]							
		23:16	MAC_RMCAST[23:16]							
		31:24	MAC_RMCAST[31:24]							
0x0424	MAC_RX_PF	7:0	MAC_RPF[7:0]							
		15:8	MAC_RPF[15:8]							
		23:16	MAC_RPF[23:16]							
		31:24	MAC_RPF[31:24]							

Register Map and Descriptions (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0428	MAC_RX_CF	7:0					MAC_RCF[7:0]			
		15:8					MAC_RCF[15:8]			
		23:16					MAC_RCF[23:16]			
		31:24					MAC_RCF[31:24]			
0x042C	MAC_RX_VLAN	7:0					MAC_RVLAN[7:0]			
		15:8					MAC_RVLAN[15:8]			
		23:16					MAC_RVLAN[23:16]			
		31:24					MAC_RVLAN[31:24]			
0x0430	MAC_RX_PAD	7:0					MAC_RPAD[7:0]			
		15:8					MAC_RPAD[15:8]			
		23:16					MAC_RPAD[23:16]			
		31:24					MAC_RPAD[31:24]			
0x0434	MAC_RX_64B	7:0					MAC_R64[7:0]			
		15:8					MAC_R64[15:8]			
		23:16					MAC_R64[23:16]			
		31:24					MAC_R64[31:24]			
0x0438	MAC_RX_127B	7:0					MAC_R127[7:0]			
		15:8					MAC_R127[15:8]			
		23:16					MAC_R127[23:16]			
		31:24					MAC_R127[31:24]			
0x043C	MAC_RX_255B	7:0					MAC_R255[7:0]			
		15:8					MAC_R255[15:8]			
		23:16					MAC_R255[23:16]			
		31:24					MAC_R255[31:24]			
0x0440	MAC_RX_511B	7:0					MAC_R511[7:0]			
		15:8					MAC_R511[15:8]			
		23:16					MAC_R511[23:16]			
		31:24					MAC_R511[31:24]			
0x0444	MAC_RX_1KB	7:0					MAC_R1K[7:0]			
		15:8					MAC_R1K[15:8]			
		23:16					MAC_R1K[23:16]			
		31:24					MAC_R1K[31:24]			
0x0448	MAC_RX_MAXB	7:0					MAC_RMAX_NVLAN[7:0]			
		15:8					MAC_RMAX_NVLAN[15:8]			
		23:16					MAC_RMAX_NVLAN[23:16]			
		31:24					MAC_RMAX_NVLAN[31:24]			
0x044C	MAC_RX_MAXB_VLAN	7:0					MAC_RMAX_VLAN[7:0]			
		15:8					MAC_RMAX_VLAN[15:8]			
		23:16					MAC_RMAX_VLAN[23:16]			
		31:24					MAC_RMAX_VLAN[31:24]			
0x0450	MAC_RX_GTMAXB	7:0					MAC_RGTMAXB[7:0]			
		15:8					MAC_RGTMAXB[15:8]			
		23:16					MAC_RGTMAXB[23:16]			
		31:24					MAC_RGTMAXB[31:24]			
0x0454 ... 0x045B	Reserved									
0x045C	MAC_RX_FIFO_SBCOR	7:0					MAC_RFIFO_SBCOR[7:0]			
		15:8					MAC_RFIFO_SBCOR[15:8]			
		23:16					MAC_RFIFO_SBCOR[23:16]			
		31:24					MAC_RFIFO_SBCOR[31:24]			
0x0460	MAC_RX_FIFO_DBDET	7:0					MAC_RFIFO_DBDET[7:0]			
		15:8					MAC_RFIFO_DBDET[15:8]			
		23:16					MAC_RFIFO_DBDET[23:16]			
		31:24					MAC_RFIFO_DBDET[31:24]			
0x0464	MAC_RX_DROP	7:0					MAC_RDROP[7:0]			
		15:8					MAC_RDROP[15:8]			
		23:16					MAC_RDROP[23:16]			
		31:24					MAC_RDROP[31:24]			

Register Map and Descriptions (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0468 ... 0x04FF	Reserved									
0x0500	PCS_EB_SBCOR	7:0	PCS_EB_SBCOR[7:0]							
		15:8	PCS_EB_SBCOR[15:8]							
		23:16	PCS_EB_SBCOR[23:16]							
		31:24	PCS_EB_SBCOR[31:24]							
0x0504	PCS_EB_DBDET	7:0	PCS_EB_DBDET[7:0]							
		15:8	PCS_EB_DBDET[15:8]							
		23:16	PCS_EB_DBDET[23:16]							
		31:24	PCS_EB_DBDET[31:24]							
0x0508	PCS_CODE_ERR	7:0	PCS_CODE_ERR[7:0]							
		15:8	PCS_CODE_ERR[15:8]							
		23:16	PCS_CODE_ERR[23:16]							
		31:24	PCS_CODE_ERR[31:24]							
0x050C	PCS_SYNC_LOST_ERR	7:0	PCS_SYNC_LOST_ERR[7:0]							
		15:8	PCS_SYNC_LOST_ERR[15:8]							
		23:16	PCS_SYNC_LOST_ERR[23:16]							
		31:24	PCS_SYNC_LOST_ERR[31:24]							

6.1. PCS_SYNC_LOST_ERR [\(Ask a Question\)](#)

Name: PCS_SYNC_LOST_ERR

Offset: 0x50C

Reset: 0x0

Property: Read/Write-to Clear

PCS Code Error Frame Counter

Bit	31	30	29	28	27	26	25	24
	PCS_SYNC_LOST_ERR[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	PCS_SYNC_LOST_ERR[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	PCS_SYNC_LOST_ERR[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PCS_SYNC_LOST_ERR[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PCS_SYNC_LOST_ERR[31:0] PCS SYNC Lost error Counter. Incremented for each received PCS code error. This register is enabled when the RX PCS SYNC Lost Error count parameter in the MAC Rx Stat Counters tab is set

6.2. PCS_EB_SBCOR [\(Ask a Question\)](#)

Name: PCS_EB_SBCOR
Offset: 0x500
Reset: 0x0
Property: Read/Write-to Clear

PCS EB SB Correct Counter

Bit	31	30	29	28	27	26	25	24
	PCS_EB_SBCOR[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	PCS_EB_SBCOR[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	PCS_EB_SBCOR[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PCS_EB_SBCOR[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 - PCS_EB_SBCOR[31:0] PCS Elastic Buffer SB Correct Counter. Incremented for each received EB correct flag set. This register is enabled when the RX EB SB Correct count parameter in the MAC Rx Stat Counters tab is set

6.3. PCS_EB_DBDET [\(Ask a Question\)](#)

Name: PCS_EB_DBDET
Offset: 0x504
Reset: 0x0
Property: Read/Write-to Clear

PCS EB DB Detect Counter

Bit	31	30	29	28	27	26	25	24
	PCS_EB_DBDET[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	PCS_EB_DBDET[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	PCS_EB_DBDET[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PCS_EB_DBDET[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PCS_EB_DBDET[31:0] PCS Elastic Buffer DB Detect Counter. Incremented for each received EB DB detect flag set. This register is enabled when the RX EB DB Detect count parameter in the MAC Rx Stat Counters tab is set

6.4. PCS_CODE_ERR [\(Ask a Question\)](#)

Name: PCS_CODE_ERR
Offset: 0x508
Reset: 0x0
Property: Read/Write-to Clear

PCS Running Disparity Error Counter

Bit	31	30	29	28	27	26	25	24
	PCS_CODE_ERR[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	PCS_CODE_ERR[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	PCS_CODE_ERR[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PCS_CODE_ERR[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PCS_CODE_ERR[31:0] PCS Code error frame Counter. Incremented for each received PCS code error. This register is enabled when the RX PCS Code Error count parameter in the MAC Rx Stat Counters tab is set

6.5. MAC_TX_VLAN [\(Ask a Question\)](#)

Name: MAC_TX_VLAN
Offset: 0x22C
Reset: 0x0
Property: Read/Write-to Clear

Transmit packet VLAN counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TVLAN[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TVLAN[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TVLAN[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TVLAN[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TVLAN[31:0] Number of VLAN packets. System disables the function when the VLAN packet parameter in the MAC Tx Stat Counters tab is disabled.

6.6. MAC_TX_PRE_UPPER [\(Ask a Question\)](#)

Name: MAC_TX_PRE_UPPER
Offset: 0x104
Reset: 0x0
Property: Read/Write

MAC transmit preamble upper register

Bit	31	30	29	28	27	26	25	24
	MAC TX PREAMBLE UPPER 32 BITS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC TX PREAMBLE UPPER 32 BITS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC TX PREAMBLE UPPER 32 BITS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC TX PREAMBLE UPPER 32 BITS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC TX PREAMBLE UPPER 32 BITS[31:0] Tx preamble upper 32 bits. Use this field only for a custom preamble when the MAC TX Preamble parameter is enabled and MAC_TX_PREAMBLE_EN, bit[3] of MAC_TX_CFG register is set to 1.

6.7. MAC_TX_PRE_LOWER [\(Ask a Question\)](#)

Name: MAC_TX_PRE_LOWER

Offset: 0x108

Reset: 0x0

Property: Read/Write

MAC transmit preamble lower register

Bit	31	30	29	28	27	26	25	24
	MAC TX PREAMBLE LOWER 32 BITS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC TX PREAMBLE LOWER 32 BITS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC TX PREAMBLE LOWER 32 BITS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC TX PREAMBLE LOWER 32 BITS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC TX PREAMBLE LOWER 32 BITS[31:0] Tx Preamble lower 32 bit. Use this field only for a custom preamble when the MAC TX Preamble parameter is enabled and MAC_TX_PREAMBLE_EN, bit[3] of Tx MAC_TX_CFG register is set to 1.

6.8. MAC_TX_PKT [\(Ask a Question\)](#)

Name: MAC_TX_PKT
Offset: 0x200
Reset: 0x0
Property: Read/Write-to Clear

Transmit Packet Counter

Bit	31	30	29	28	27	26	25	24
	MAC_TPKT[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TPKT[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TPKT[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TPKT[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TPKT[31:0] Number of transmitted packets (including bad packets, all Unicast, Broadcast, and Multicast packets). This register is enabled when the TX packet parameter in the MAC Tx Stat Counters tab is set.

6.9. MAC_TX_PF [\(Ask a Question\)](#)

Name: MAC_TX_PF
Offset: 0x224
Reset: 0x0
Property: Read/Write-to Clear

Transmit pause counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TPF[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TPF[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TPF[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TPF[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TPF[31:0] Number of pause packets. This register is enabled when the TX Pause packet parameter in the MAC Tx Stat Counters tab is set.

6.10. MAC_TX_PAUSE_TIMER [\(Ask a Question\)](#)

Name: MAC_TX_PAUSE_TIMER
Offset: 0x170
Reset: 0xffff
Property: Read/Write

MAC transmit pause timer value

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	MAC TX PAUSE TIMER[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0
	MAC TX PAUSE TIMER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – MAC TX PAUSE TIMER[15:0] Tx Pause frame timer. This is the pause timer value to be sent as pause frame payload. This register is valid when the MAC TX Pause parameter is not set to Disabled.

6.11. MAC_TX_PARAM2 [\(Ask a Question\)](#)

Name: MAC_TX_PARAM2
Offset: 0x008
Reset: 0x20
Property: Read-only

MAC transmit parameter 2 register

Bit	31	30	29	28	27	26	25	24
	MAC_TX_PARAM2[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TX_PARAM2[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TX_PARAM2[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TX_PARAM2[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	1	0	0	0	0	0

Bits 31:0 – MAC_TX_PARAM2[31:0] {11b0, TX_MAC_CFG_PAUSE_EN, ECC_ENABLE, TX_MAC_CFG_CHECK_LT, TX_MAC_CFG_PREAMBLE, TX_RAM_TYPE, TX_MAC_CFG_FIFO_MODE, TX_MAC_CFG_FIFO_DEPTH}

6.12. MAC_TX_PARAM1 [\(Ask a Question\)](#)

Name: MAC_TX_PARAM1
Offset: 0x004
Reset: 0x0
Property: Read-only

MAC transmit parameter 1 register

Bit	31	30	29	28	27	26	25	24
	MAC_TX_PARAM1[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TX_PARAM1[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TX_PARAM1[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TX_PARAM1[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TX_PARAM1[31:0] {7b0,

TX_MAC_STATS_PKT_FIFO_DBDET_CNT_EN, TX_MAC_STATS_PKT_FIFO_SBCOR_CNT_EN, 2b0,
 TX_MAC_STATS_PKT_GTMAXB_CNT_EN, TX_MAC_STATS_PKT_1519BTO1522B_VLAN_CNT_EN,
 TX_MAC_STATS_PKT_1024BTO1518B_CNT_EN, TX_MAC_STATS_PKT_512BTO1023B_CNT_EN,
 TX_MAC_STATS_PKT_256BTO511B_CNT_EN, TX_MAC_STATS_PKT_128BTO255B_CNT_EN,
 TX_MAC_STATS_PKT_65BTO127B_CNT_EN, TX_MAC_STATS_PKT_64B_CNT_EN,
 TX_MAC_STATS_PKT_PAD_CNT_EN, TX_MAC_STATS_PKT_VLAN_CNT_EN,
 TX_MAC_STATS_PKT_CONTROL_CNT_EN, TX_MAC_STATS_PKT_PAUSE_CNT_EN,
 TX_MAC_STATS_PKT_MULTICAST_CNT_EN, TX_MAC_STATS_PKT_BROADCAST_CNT_EN,
 TX_MAC_STATS_PKT_ERR_FRM_CNT_EN, TX_MAC_STATS_PKT_ERR_FCS_CNT_EN,
 TX_MAC_STATS_PKT_ERR_LEN_SHORT_CNT_EN, TX_MAC_STATS_PKT_ERR_LEN_CHECK_CNT_EN,
 TX_MAC_STATS_PKT_ERR_LEN_LONG_CNT_EN, TX_MAC_STATS_PKT_ERR_CNT_EN,
 TX_MAC_STATS_PKT_CNT_EN }

6.13. MAC_TX_PAD [\(Ask a Question\)](#)

Name: MAC_TX_PAD
Offset: 0x230
Reset: 0x0
Property: Read/Write-to Clear

Transmit packet padded counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TPAD[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TPAD[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TPAD[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TPAD[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TPAD[31:0] Number of transmitted padded packets. Counts the number of packets padded with zero bytes when MAC_TX_PAD_EN bit in MAC_TX_CFG register is set. **Note:** This register is enabled when the TX Padded packet parameter in the MAC Tx Stat Counters tab is set.

6.14. MAC_TX_MCAST [\(Ask a Question\)](#)

Name: MAC_TX_MCAST
Offset: 0x220
Reset: 0x0
Property: Read/Write-to Clear

Transmit multicast counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TMCAST[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TMCAST[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TMCAST[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TMCAST[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TMCAST[31:0] Number of multicast packet. This register is enabled when the TX Multicast packet parameter in the MAC Tx Stat Counters tab is set.

6.15. MAC_TX_MAXB_VLAN [\(Ask a Question\)](#)

Name: MAC_TX_MAXB_VLAN

Offset: 0x24C

Reset: 0x0

Property: Read/Write-to Clear

Transmit 1519 to 1522 Byte VLAN Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_TMAXB_VLAN[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TMAXB_VLAN[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TMAXB_VLAN[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TMAXB_VLAN[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TMAXB_VLAN[31:0] Transmit 1519 to 1522 Byte VLAN Frame Counter. Incremented for each good VLAN frame transmitted which is 1519 to 1522 bytes in length inclusive (excluding framing bits but including FCS bytes). This register is enabled when the TX 1519 to 1522byte packet parameter in the MAC Tx Stat Counters tab is set

6.16. MAC_TX_MAXB [\(Ask a Question\)](#)

Name: MAC_TX_MAXB
Offset: 0x248
Reset: 0x0
Property: Read/Write-to Clear

Transmit 1024 to 1518 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_TMAX_NVLAN[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TMAX_NVLAN[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TMAX_NVLAN[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TMAX_NVLAN[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TMAX_NVLAN[31:0] Transmit 1024 to 1518 Byte Frame Counter. Incremented for each good or bad frame transmitted which is 1024 to 1518 bytes in length inclusive (excluding framing bits but including FCS bytes). This register is enabled when the TX 1024 to 1518byte packet parameter in the MAC Tx Stat Counters tab is set

6.17. MAC_TX_LS_ERR [\(Ask a Question\)](#)

Name: MAC_TX_LS_ERR
Offset: 0x210
Reset: 0x0
Property: Read/Write-to Clear

Transmit error length short counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TERR_LS[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TERR_LS[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TERR_LS[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TERR_LS[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TERR_LS[31:0] Number of length short errors. System flags a length short error when the packet is smaller than the 64 bytes. This register is enabled when the TX Errored at length, with short parameter in the MAC Tx Stat Counters tab is set

6.18. MAC_TX_LL_ERR [\(Ask a Question\)](#)

Name: MAC_TX_LL_ERR
Offset: 0x208
Reset: 0x0
Property: Read/Write-to Clear

Transmit error length long counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TERR_LL[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TERR_LL[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TERR_LL[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TERR_LL[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TERR_LL[31:0] Number of length long errors. System flags a length long error when the packet is larger than the configured maximum, MAC TX MAX PKT LEN (bits 19 down-to 4 of Tx Config Register). This register is enabled when the TX Errored at length, with long parameter in the MAC Tx Stat Counters tab is set.

6.19. MAC_TX_LC_ERR [\(Ask a Question\)](#)

Name: MAC_TX_LC_ERR
Offset: 0x20C
Reset: 0x0
Property: Read/Write-to Clear

Transmit error length check counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TERR_LC[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TERR_LC[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TERR_LC[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TERR_LC[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TERR_LC[31:0] Number of length check errors. System flags a length check error, when the LT field indicates length, and the value does not match the actual packet length. This register is enabled when the TX Errored at length, with check parameter in the MAC Tx Stat Counters tab is set.

6.20. MAC_TX_GTMAXB [\(Ask a Question\)](#)

Name: MAC_TX_GTMAXB
Offset: 0x250
Reset: 0x0
Property: Read/Write-to Clear

Transmit Oversize Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_TGTMAXB[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TGTMAXB[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TGTMAXB[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TGTMAXB[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TGTMAXB[31:0] Transmit Greater than Max Byte Frame Counter. Incremented for each transmitted frame with frame length > 1518 (for non VLAN) or 1522 (for VLAN). This register is enabled when the TX Greater than MAX byte packet parameter in the MAC Tx Stat Counters tab is set

6.21. MAC_TX_FRM_ERR [\(Ask a Question\)](#)

Name: MAC_TX_FRM_ERR
Offset: 0x218
Reset: 0x0
Property: Read/Write-to Clear

Transmit error frame counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TERR_FRM[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TERR_FRM[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TERR_FRM[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TERR_FRM[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TERR_FRM[31:0] Number of framing errors. System flags a framing error for the Transmit FIFO underruns. This register is enabled when the TX Errored at framing parameter in the MAC Tx Stat Counters tab is set.

6.22. MAC_TX_FIFO_SBCOR [\(Ask a Question\)](#)

Name: MAC_TX_FIFO_SBCOR
Offset: 0x25C
Reset: 0x0
Property: Read/Write-to Clear

Transmit FIFO SB Correct Counter

Bit	31	30	29	28	27	26	25	24
	MAC_TFIFO_SBCOR[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TFIFO_SBCOR[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TFIFO_SBCOR[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TFIFO_SBCOR[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TFIFO_SBCOR[31:0] Transmit FIFO SB Correct Counter. Incremented for each transmitted TX FIFO SB correct flag set. This register is enabled when the TX FIFO SB Correct count parameter in the MAC Tx Stat Counters tab is set

6.23. MAC_TX_FIFO_DBDET [\(Ask a Question\)](#)

Name: MAC_TX_FIFO_DBDET

Offset: 0x260

Reset: 0x0

Property: Read/Write-to Clear

Transmit FIFO DB Detect Counter

Bit	31	30	29	28	27	26	25	24
	MAC_TX_FIFO_DBDET[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TX_FIFO_DBDET[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TX_FIFO_DBDET[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TX_FIFO_DBDET[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TX_FIFO_DBDET[31:0] Transmit FIFO DB Detect Counter. Incremented for each transmitted TX FIFO DB detect flag set. This register is enabled when the TX FIFO DB Detect count parameter in the MAC Tx Stat Counters tab is set

6.24. MAC_TX_FCS_ERR [\(Ask a Question\)](#)

Name: MAC_TX_FCS_ERR
Offset: 0x214
Reset: 0x0
Property: Read/Write-to Clear

Transmit error FCS counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TERR_FCS[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TERR_FCS[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TERR_FCS[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TERR_FCS[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TERR_FCS[31:0] Number of FCS errors detected. Number of packets received with below register bits set: 1. SYS MAC TX FCS ERR (Bit[22] of MAC_TX_CFG Register) 2. SYS MAC TX FCS STOMP (Bit[23] of MAC_TX_CFG Register). This register is enabled when the TX Errored at FCS parameter in the MAC Tx Stat Counters tab is set.

6.25. MAC_TX_ERR [\(Ask a Question\)](#)

Name: MAC_TX_ERR
Offset: 0x204
Reset: 0x0
Property: Read/Write-to Clear

Transmit error counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TERR[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TERR[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TERR[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TERR[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TERR[31:0] Number of errored packets. This register counts all the received packets with below error conditions: 1. length errors (length-long, length-short, length-check errors), 2. fcs errors, 3. frame errors. This register is enabled when the TX Errored packet parameter in the MAC Tx Stat Counters tab is set.

6.26. MAC_TX_CFG [\(Ask a Question\)](#)

Name: MAC_TX_CFG
Offset: 0x100
Reset: 0x8C3C0000
Property: Read/Write

MAC transmit configuration register

Bit	31	30	29	28	27	26	25	24
	MAC_TX_EN			MAC_TX_IFG_CNT[5:0]				
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	1		0	0	1	1	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TX_FCS_STOMP	MAC_TX_FCS_ERR	MAC_TX_FCS_INS	MAC_TX_PAD_EN	MAC_TX_MAX_PKT_LEN[15:12]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TX_MAX_PKT_LEN[11:4]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TX_MAX_PKT_LEN[3:0]				MAC_TX_PREAMBLE_EN	MAC_TX_PREAMBLE_WCM1[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – MAC_TX_EN Tx enable. This bit enables the MAC TX core to send frames onto the line. When this signal is asserted low, data-frames does not flow. When the signal is asserted high, data flows normally. The signal is sampled on a packet boundary, so there are no partial packets as a consequence of changing the assertion of this signal. It is possible to change the signal dynamically.

Bits 29:24 – MAC_TX_IFG_CNT[5:0] Tx IFG Count. This field configures the IFG value. The standard is 12, but the core supports other values. The minimum supported IFG value is 2, and the maximum is 48. System considers values less than 2 as 2, and values above 48 as 48. Configuring the IFG to a value lower than the standard (12 bytes) may result in truncation up to a maximum of 4 bytes of the Ethernet preamble.

Bit 23 – MAC_TX_FCS_STOMP Tx FCS stomp This bit configures if the core must insert an FCS stomp. The FCS stomp is inserted by xor-ing the correct FCS with 0xFFFF_FFFF.

Bit 22 – MAC_TX_FCS_ERR Tx FCS error This bit configures if the core must insert an FCS error on the packet. The FCS error is inserted by xor-ing the correct FCS with 0x5555_5555.

Bit 21 – MAC_TX_FCS_INS Tx FCS insert This bit configures if the core must insert FCS on all the packets.

Bit 20 – MAC_TX_PAD_EN Set this bit to have the MAC pad all short frames (with payload length less than 46 bytes). Clear this bit if frames presented to the MAC have a valid length and contain a CRC.**Note:** This bit is valid when Bit[21] (MAC_TX_FCS_INS) is not set.

Bits 19:4 – MAC_TX_MAX_PKT_LEN[15:0] Tx Maximum packet length This is the maximum configured packet length. A valid packet length is less than or equal to this signal. The signal does not influence the transmit

data-path, but it is used by the transmit stats block. When [15:14] == 2b11, the max length check is disabled. It is possible to change the signal dynamically.

Bit 3 – MAC_TX_PREAMBLE_EN Tx Preamble Enable Configures the Tx core to use a customer preamble. The signal is valid when the MAC TX Preamble parameter is enabled.

Bits 2:0 – MAC_TX_PREAMBLE_WCM1[2:0] Tx Preamble size Configures the size of the custom preamble, measured in words. The value is Word Count Minus 1, for example, 3h0 = 1 word of preamble. The signal is valid when the MAC TX Preamble parameter is enabled. custom preamble is appended with SFD character. So the max value of this field is limited to 6

6.27. MAC_TX_CF [\(Ask a Question\)](#)

Name: MAC_TX_CF
Offset: 0x228
Reset: 0x0
Property: Read/Write-to Clear

Transmit packet control counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TCF[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TCF[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TCF[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TCF[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TCF[31:0] Number of control packets. System disables the function when the Control packet parameter in the MAC Tx Stat Counters tab is disabled.

6.28. MAC_TX_BCAST [\(Ask a Question\)](#)

Name: MAC_TX_BCAST
Offset: 0x21C
Reset: 0x0
Property: Read/Write-to Clear

Transmit broadcast counter register

Bit	31	30	29	28	27	26	25	24
	MAC_TBICAST[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_TBICAST[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_TBICAST[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_TBICAST[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_TBICAST[31:0] Number of broadcast packets. This register is enabled when the TX Broadcast packet parameter in the MAC Tx Stat Counters tab is set.

6.29. MAC_TX_64B [\(Ask a Question\)](#)

Name: MAC_TX_64B
Offset: 0x234
Reset: 0x0
Property: Read/Write-to Clear

Transmit 64 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_T64[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_T64[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_T64[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_T64[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_T64[31:0] Transmit 64 Byte Frame Counter Incremented for each good or bad frame transmitted which is 64 bytes in length inclusive (excluding framing bits but including FCS bytes).

6.30. MAC_TX_511B [\(Ask a Question\)](#)

Name: MAC_TX_511B
Offset: 0x240
Reset: 0x0
Property: Read/Write-to Clear

Transmit 256 to 511 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_T511[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_T511[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_T511[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_T511[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_T511[31:0] Transmit 256 to 511 Byte Frame Counter Incremented for each good or bad frame transmitted which is 256 to 511 bytes in length inclusive (excluding framing bits but including FCS bytes).

6.31. MAC_TX_255B [\(Ask a Question\)](#)

Name: MAC_TX_255B
Offset: 0x23C
Reset: 0x0
Property: Read/Write-to Clear

Transmit 128 to 255 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_T255[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_T255[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_T255[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_T255[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_T255[31:0] Transmit 128 to 255 Byte Frame Counter Incremented for each good or bad frame transmitted which is 128 to 255 bytes in length inclusive (excluding framing bits but including FCS bytes).

6.32. MAC_TX_1KB [\(Ask a Question\)](#)

Name: MAC_TX_1KB
Offset: 0x244
Reset: 0x0
Property: Read/Write-to Clear

Transmit 512 to 1023 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_T1K[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_T1K[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_T1K[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_T1K[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_T1K[31:0] Transmit 512 to 1023 Byte Frame Counter Incremented for each good or bad frame transmitted which is 51 to 1023 bytes in length inclusive (excluding framing bits but including FCS bytes). This register is enabled when the TX 512 to 1023byte packet parameter in the MAC Tx Stat Counters tab is set

6.33. MAC_TX_127B [\(Ask a Question\)](#)

Name: MAC_TX_127B
Offset: 0x238
Reset: 0x0
Property: Read/Write-to Clear

Transmit 65 to 127 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_T127[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_T127[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_T127[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_T127[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_T127[31:0] Transmit 65 to 127 Byte Frame Counter Incremented for each good or bad frame transmitted which is 65 to 127 bytes in length inclusive (excluding framing bits but including FCS bytes).

6.34. MAC_RX_VLAN [\(Ask a Question\)](#)

Name: MAC_RX_VLAN

Offset: 0x42C

Reset: 0x0

Property: Read/Write-to Clear

Receive packet VLAN counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RVLAN[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RVLAN[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RVLAN[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RVLAN[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RVLAN[31:0] Number of VLAN packets. This register is enabled when the RX VLAN packet parameter in the MAC Rx Stat Counter tab is set.

6.35. MAC_RX_PKT [\(Ask a Question\)](#)

Name: MAC_RX_PKT
Offset: 0x400
Reset: 0x0
Property: Read/Write-to Clear

Receive Packet Counter

Bit	31	30	29	28	27	26	25	24
	MAC_RPKT[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RPKT[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RPKT[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RPKT[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RPKT[31:0] Number of receive packets (including bad packets, all Unicast, Broadcast, and Multicast packets). This register is enabled when the RX packet parameter in the MAC Rx Stat Counters tab is set.

6.36. MAC_RX_PF [\(Ask a Question\)](#)

Name: MAC_RX_PF
Offset: 0x424
Reset: 0x0
Property: Read/Write-to Clear

Receive pause counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RPF[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RPF[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RPF[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RPF[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RPF[31:0] Number of pause packets. This register is enabled when the RX Pause packet parameter in the MAC Rx Stat Counter tab is set.

6.37. MAC_RX_PAUSE_WM [\(Ask a Question\)](#)

Name: MAC_RX_PAUSE_WM
Offset: 0x1F0
Reset: 0x0
Property: Read/Write

MAC receive pause water mark register to send PAUSE control frame to stop or resume transmission

Bit	31	30	29	28	27	26	25	24
	MAC RX PAUSE HWM[12:8]							
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC RX PAUSE HWM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC RX PAUSE LWM[12:8]							
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC RX PAUSE LWM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 28:16 – MAC RX PAUSE HWM[12:0] High Water Mark: This represents the high water mark of the receive asynchronous FIFO, at which point the TX MAC controller issues a PAUSE frame to pause data transmission.

Bits 12:0 – MAC RX PAUSE LWM[12:0] Low Water Mark: This represents the low water mark of the receive asynchronous FIFO, at which point the TX MAC controller issues a PAUSE frame to resume data transmission.

6.38. MAC_RX_PAUSE_RTX [\(Ask a Question\)](#)

Name: MAC_RX_PAUSE_RTX
Offset: 0x1F4
Reset: 0x8000
Property: Read/Write

MAC number of pause Quantas before PAUSE frame (to stop transmission) retransmission

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	MAC RX PAUSE RETRANSMISSION[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC RX PAUSE RETRANSMISSION[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – MAC RX PAUSE RETRANSMISSION[15:0] Number of pause quantas before pause retransmission. This hex value represents the number of pause quanta (64 byte times) after a pause frame(to stop transmission) has been acknowledged until the receive MAC FIFO storage level has remained higher than the low watermark.

6.39. MAC_RX_PARAM2 [\(Ask a Question\)](#)

Name: MAC_RX_PARAM2

Offset: 0x010

Reset: 0x20

Property: Read-only

MAC receive parameter 2 register

Bit	31	30	29	28	27	26	25	24
	MAC_RX_PARAM2[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RX_PARAM2[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RX_PARAM2[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RX_PARAM2[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	1	0	0	0	0	0

Bits 31:0 – MAC_RX_PARAM2[31:0] {7b0, RX_MAC_CFG_WOL, RX_MAC_CFG_FRMFIL_HASH, RX_MAC_CFG_FRMFIL_PKT, 1b0, RX_MAC_CFG_PAUSE_PUC, RX_MAC_CFG_PAUSE_EN, RX_MAC_CFG_CHECK_LT, RX_MAC_CFG_PREAMBLE, RX_RAM_TYPE, RX_MAC_CFG_FIFO_MODE, RX_MAC_CFG_FIFO_DEPTH}

6.40. MAC_RX_PARAM1 [\(Ask a Question\)](#)

Name: MAC_RX_PARAM1
Offset: 0x00C
Reset: 0x0
Property: Read-only

MAC receive parameter 1 register

Bit	31	30	29	28	27	26	25	24
	MAC_RX_PARAM1[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RX_PARAM1[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RX_PARAM1[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RX_PARAM1[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RX_PARAM1[31:0] {2b0, RX_PCS_STATS_SYNCLOST_CNT_EN, RX_PCS_STATS_CODEERR_CNT_EN, RX_PCS_STATS_EB_DBDET_CNT_EN, RX_PCS_STATS_EB_SBCOR_CNT_EN, RX_MAC_STATS_PKT_DROP_CNT_EN, RX_MAC_STATS_PKT_FIFO_DBDET_CNT_EN, RX_MAC_STATS_PKT_FIFO_SBCOR_CNT_EN, 2b0, RX_MAC_STATS_PKT_GTMAXB_CNT_EN, RX_MAC_STATS_PKT_1519BTO1522B_VLAN_CNT_EN, RX_MAC_STATS_PKT_1024BTO1518B_CNT_EN, RX_MAC_STATS_PKT_512BTO1023B_CNT_EN, RX_MAC_STATS_PKT_256BTO511B_CNT_EN, RX_MAC_STATS_PKT_128BTO255B_CNT_EN, RX_MAC_STATS_PKT_65BTO127B_CNT_EN, RX_MAC_STATS_PKT_64B_CNT_EN, RX_MAC_STATS_PKT_PAD_CNT_EN, RX_MAC_STATS_PKT_VLAN_CNT_EN, RX_MAC_STATS_PKT_CONTROL_CNT_EN, RX_MAC_STATS_PKT_PAUSE_CNT_EN, RX_MAC_STATS_PKT_MULTICAST_CNT_EN, RX_MAC_STATS_PKT_BROADCAST_CNT_EN, RX_MAC_STATS_PKT_ERR_FRM_CNT_EN, RX_MAC_STATS_PKT_ERR_FCS_CNT_EN, RX_MAC_STATS_PKT_ERR_LEN_SHORT_CNT_EN, RX_MAC_STATS_PKT_ERR_LEN_CHECK_CNT_EN, RX_MAC_STATS_PKT_ERR_LEN_LONG_CNT_EN, RX_MAC_STATS_PKT_ERR_CNT_EN, RX_MAC_STATS_PKT_CNT_EN}

6.41. MAC_RX_PAD [\(Ask a Question\)](#)

Name: MAC_RX_PAD
Offset: 0x430
Reset: 0x0
Property: Read/Write-to Clear

Receive packet padded counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RPAD[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RPAD[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RPAD[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RPAD[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RPAD[31:0] Number of received padded packets. Counts the number of packets received with pad bytes when MAC_RX_FCS_REMOVE bit in MAC_RX_CFG register is set. **Note:** This register is enabled when the RX Padded packet parameter in the MAC Rx Stat Counter tab is set.

6.42. MAC_RX_MCAST [\(Ask a Question\)](#)

Name: MAC_RX_MCAST

Offset: 0x420

Reset: 0x0

Property: Read/Write-to Clear

Receive multicast counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RMCAST[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RMCAST[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RMCAST[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RMCAST[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RMCAST[31:0] Number of multicast packet. This register is enabled when the RX Multicast packet parameter in the MAC Rx Stat Counter tab is set.

6.43. MAC_RX_MAXB_VLAN [\(Ask a Question\)](#)

Name: MAC_RX_MAXB_VLAN
Offset: 0x44C
Reset: 0x0
Property: Read/Write-to Clear

Receive 1519 to 1522 Byte VLAN Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_RMAX_VLAN[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RMAX_VLAN[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RMAX_VLAN[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RMAX_VLAN[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RMAX_VLAN[31:0] Receive 1519 to 1522 Byte VLAN Frame Counter. Incremented for each good VLAN frame received which is 1519 to 1522 bytes in length inclusive (excluding framing bits but including FCS bytes). This register is enabled when the RX 1519 to 1522byte packet parameter in the MAC Rx Stat Counters tab is set

6.44. MAC_RX_MAXB [\(Ask a Question\)](#)

Name: MAC_RX_MAXB
Offset: 0x448
Reset: 0x0
Property: Read/Write-to Clear

Receive 1024 to 1518 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_RMAX_NVLAN[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RMAX_NVLAN[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RMAX_NVLAN[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RMAX_NVLAN[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RMAX_NVLAN[31:0] Receive 1024 to 1518 Byte Frame Counter. Incremented for each good or bad frame received which is 1024 to 1518 bytes in length inclusive (excluding framing bits but including FCS bytes). This register is enabled when the RX 1024 to 1518byte packet parameter in the MAC Rx Stat Counters tab is set

6.45. MAC_RX_LS_ERR [\(Ask a Question\)](#)

Name: MAC_RX_LS_ERR
Offset: 0x410
Reset: 0x0
Property: Read/Write-to Clear

Receive error length short counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RERR_LS[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RERR_LS[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RERR_LS[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RERR_LS[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RERR_LS[31:0] Number of length short errors. System flags a length short error when the packet is smaller than the 64 bytes. This register is enabled when the RX Errored at length, with short parameter in the MAC Rx Stat Counters tab is set

6.46. MAC_RX_LL_ERR [\(Ask a Question\)](#)**Name:** MAC_RX_LL_ERR**Offset:** 0x408**Reset:** 0x0**Property:** Read/Write-to Clear

Receive error length long counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RERR_LL[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RERR_LL[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RERR_LL[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RERR_LL[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RERR_LL[31:0] Number of length long errors. System flags a length long error when the packet is larger than the configured maximum, MAC RX MAX PKT LEN (bits 19 down to 4 of MAC_RX_CFG Register). This register is enabled when the RX Errored at length, with long parameter in the MAC Rx Stat Counters tab is set.

6.47. MAC_RX_LC_ERR [\(Ask a Question\)](#)

Name: MAC_RX_LC_ERR
Offset: 0x40C
Reset: 0x0
Property: Read/Write-to Clear

Receive error length check counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RERR_LC[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RERR_LC[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RERR_LC[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RERR_LC[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RERR_LC[31:0] Number of length check errors. System flags a length check error when the LT field indicates length, and the value does not match the actual packet length. This register is enabled when the RX Errored at length, with check parameter in the MAC Rx Stat Counters tab is set.

6.48. MAC_RX_GTMAXB [\(Ask a Question\)](#)

Name: MAC_RX_GTMAXB
Offset: 0x450
Reset: 0x0
Property: Read/Write-to Clear

Receive >1518 byte for non-VLAN or > 1522byte for VLAN Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_RGTMAXB[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RGTMAXB[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RGTMAXB[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RGTMAXB[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RGTMAXB[31:0] Receive greater than max bytes frame Counter. Incremented for each received frame with frame length > 1518 (for non VLAN) or 1522 (for VLAN). This register is enabled when the RX Greater than MAX byte packet parameter in the MAC Rx Stat Counters tab is set

6.49. MAC_RX_FRMFIL_PKT ([Ask a Question](#))

Name: MAC_RX_FRMFIL_PKT
Offset: 0x190
Reset: 0x0
Property: Read/Write

Note: Packet based frame filter controls. This register is valid when RX_MAC_CFG_FRMFIL_PKT parameter is set.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
		RX_VLAN	RX_CNTL_UN SUP	RX_CNTL_PA USE	RX_CNTL	RX_UCAST	RX_BCAST	RX_MCAST
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	RX_LS_ERR	RX_LL_ERR	RX_LC_ERR	RX_FCS_ERR	RX_PCS_ERR			
Access	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0			

Bit 14 – RX_VLAN Frames length/type field contained 0x8100 which is the VLAN Protocol Identifier.

Bit 13 – RX_CNTL_UNSUP Current Frame was recognized as a Control frame by the PEMCS, but it contains an unknown Op-code

Bit 12 – RX_CNTL_PAUSE Current frame was recognized as a Control frame containing a valid PAUSE Frame Op-code and a valid address.

Bit 11 – RX_CNTL Current Frame was recognized as a Control frame for having a valid Type- Length designation.

Bit 10 – RX_UCAST Frames destination address is unicast address but didnt match the configured DA.

Bit 9 – RX_BCAST Frames destination address contained the broadcast address.

Bit 8 – RX_MCAST Frames destination address contained a multicast address.

Bit 7 – RX_LS_ERR Setting this bit causes the frame to be dropped if a receive frame is less than 64 bytes in length.

Bit 6 – RX_LL_ERR Indicates that frames length was larger than the hosts maximum frame length value.

Bit 5 – RX_LC_ERR Indicates that frame length field value in the frame does not match the actual data byte length and is not a type field.

Bit 4 – RX_FCS_ERR Frames CRC did not match the internally generated CRC.

Bit 3 – RX_PCS_ERR Code error or disparity error One or more nibbles were signaled as errors during the reception of the packet.

6.50. MAC_RX_FRM_ERR [\(Ask a Question\)](#)

Name: MAC_RX_FRM_ERR
Offset: 0x418
Reset: 0x0
Property: Read/Write-to Clear

Receive error frame counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RERR_FRM[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RERR_FRM[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RERR_FRM[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RERR_FRM[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RERR_FRM[31:0] Number of framing errors. It indicates that the packet has flagged an error by the MAC delineation process. This happens if the PCS flags the packet in error , or if the packet is corrupt so as not to allow for proper delineation. This register is enabled when the RX Errored at framing parameter in the MAC Rx Stat Counter tab is set.

6.51. MAC_RX_FRMFIL_HTR1 [\(Ask a Question\)](#)

Name: MAC_RX_FRMFIL_HTR1
Offset: 0x1A4
Reset: 0x0
Property: Read/Write

Hash Table Register 1

Bit	31	30	29	28	27	26	25	24
	MAC RX HASH TABLE REGISTER 2[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC RX HASH TABLE REGISTER 2[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC RX HASH TABLE REGISTER 2[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC RX HASH TABLE REGISTER 2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC RX HASH TABLE REGISTER 2[31:0] Hash Table Register 2 Hash Entries-[95:64] This register is valid when RX_MAC_CFG_FRMFIL_HASH parameter is set

6.52. MAC_RX_FRMFIL_HTR0 [\(Ask a Question\)](#)

Name: MAC_RX_FRMFIL_HTR0
Offset: 0x1A0
Reset: 0x0
Property: Read/Write

Hash Table Register 0

Bit	31	30	29	28	27	26	25	24
	MAC RX HASH TABLE REGISTER 1[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC RX HASH TABLE REGISTER 1[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC RX HASH TABLE REGISTER 1[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC RX HASH TABLE REGISTER 1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC RX HASH TABLE REGISTER 1[31:0] Hash Table Register 1 Hash Entries-[63:32] This register is valid when RX_MAC_CFG_FRMFIL_HASH parameter is set

6.53. MAC_RX_FIFO_SBCOR [\(Ask a Question\)](#)

Name: MAC_RX_FIFO_SBCOR

Offset: 0x45C

Reset: 0x0

Property: Read/Write-to Clear

Receive FIFO SB Correct Counter

Bit	31	30	29	28	27	26	25	24
	MAC_RFIFO_SBCOR[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RFIFO_SBCOR[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RFIFO_SBCOR[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RFIFO_SBCOR[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RFIFO_SBCOR[31:0] MAC Receive FIFO SB Correct Counter. Incremented for each received RX FIFO SB correct flag set. This register is enabled when the RX FIFO SB Correct count parameter in the MAC Rx Stat Counters tab is set

6.54. MAC_RX_FIFO_DBDET [\(Ask a Question\)](#)

Name: MAC_RX_FIFO_DBDET
Offset: 0x460
Reset: 0x0
Property: Read/Write-to Clear

Receive FIFO DB Detect Counter

Bit	31	30	29	28	27	26	25	24
	MAC_RFIFO_DBDET[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RFIFO_DBDET[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RFIFO_DBDET[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RFIFO_DBDET[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RFIFO_DBDET[31:0] MAC Receive FIFO DB Detect Counter. Incremented for each RX FIFO DB detect flag set. This register is enabled when the RX FIFO DB Detect count parameter in the MAC Rx Stat Counters tab is set

6.55. MAC_RX_FCS_ERR [\(Ask a Question\)](#)

Name: MAC_RX_FCS_ERR
Offset: 0x414
Reset: 0x0
Property: Read/Write-to Clear

Receive error FCS counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RERR_FCS[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RERR_FCS[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RERR_FCS[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RERR_FCS[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RERR_FCS[31:0] Number of FCS errors detected. This register is enabled when the RX Errored at FCS parameter in the MAC Rx Stat Counters tab is set

6.56. MAC_RX_ERR [\(Ask a Question\)](#)

Name: MAC_RX_ERR
Offset: 0x404
Reset: 0x0
Property: Read/Write-to Clear

Receive error counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RERR[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RERR[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RERR[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RERR[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RERR[31:0] Number of receive errored packets. This register counts all the received packets with below error conditions: 1. length errors (length-long, length-short, length-check errors), 2. fcs errors, 3. frame errors. This register is enabled when RX Errored packet parameter in the MAC Rx Stat Counters tab is set.

6.57. MAC_RX_DROP [\(Ask a Question\)](#)

Name: MAC_RX_DROP
Offset: 0x464
Reset: 0x0
Property: Read/Write-to Clear

PCS EB SB Correct Counter

Bit	31	30	29	28	27	26	25	24
	MAC_RDROP[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RDROP[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RDROP[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RDROP[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RDROP[31:0] Receive frame Drop Counter. Incremented for each received frame which is dropped internally and not forwarded to user (drops due to frame filtering feature RX_MAC_CFG_FRMFIL_PKT, RX_MAC_CFG_FRMFIL_HASH). This register is enabled when the RX Drop packet parameter in the MAC Rx Stat Counters tab is set and any one of Hash Based Frame Filtering or Packet based Frame Filtering is enabled

6.58. MAC_RX_CFG [\(Ask a Question\)](#)

Name: MAC_RX_CFG
Offset: 0x180
Reset: 0x803C0000
Property: Read/Write

MAC receive configuration register

Bit	31	30	29	28	27	26	25	24
	MAC_RX_EN	WOL_EN						
Access	R/W	R/W						
Reset	1	0						
Bit	23	22	21	20	19	18	17	16
			MAC_RX_PAD_REMOVAL	MAC_RX_FCS_REMOVE	MAC_RX_MAX_PKT_LEN[15:12]			
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RX_MAX_PKT_LEN[11:4]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RX_MAX_PKT_LEN[3:0]					MAC_RX_PREAMBLE_WCM1[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit 31 – MAC_RX_EN Rx enable This signal enables the reception of data from the PCS layer. When asserted data flows normally, when de-asserted the core is effectively disabled. It is possible to change the signal dynamically.

Bit 30 – WOL_EN Wake-on-LAN Magic Packet detection enable. Enables magic packet detection logic and asserts WOL_DETECT signal when magic packet is detected.

Bit 21 – MAC_RX_PAD_REMOVAL RX pad removal. Setting this bit removes pad bytes from received short packets before sending to the axi4 receive stream interface. This bit is valid when Bit[20] (MAC_RX_FCS_REMOVE) is set.

Bit 20 – MAC_RX_FCS_REMOVE Rx FCS remove. This bit configures the core to remove the FCS field. When asserted high the core strips the FCS.

Bits 19:4 – MAC_RX_MAX_PKT_LEN[15:0] Rx maximum packet length. A valid packet is less than or equal to this value. If a larger packet is received it inserts error in the bit[8]/bit[6] of AXI4S_RX_INTR_TUSER. When [15:14] == 2b11, the max length check is disabled. It is possible to change the signal dynamically.

Bits 2:0 – MAC_RX_PREAMBLE_WCM1[2:0] Rx Preamble size. Configures the size of the custom preamble, measured in bytes. The value is "byte count minus 1", for example, 3'h0 = 1 byte of preamble. The signal is active when the MAC RX Preamble parameter is enabled. custom preamble is appended with SFD character. So the max value of this field is limited to 6

6.59. MAC_RX_CF [\(Ask a Question\)](#)

Name: MAC_RX_CF
Offset: 0x428
Reset: 0x0
Property: Read/Write-to Clear

Receive packet control counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RCF[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RCF[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RCF[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RCF[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RCF[31:0] Number of control packets. This register is enabled when the RX Control packet parameter in the MAC Rx Stat Counter tab is set.

6.60. MAC_RX_BCAST [\(Ask a Question\)](#)

Name: MAC_RX_BCAST
Offset: 0x41C
Reset: 0x0
Property: Read/Write-to Clear

Receive broadcast counter register

Bit	31	30	29	28	27	26	25	24
	MAC_RBCAST[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_RBCAST[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_RBCAST[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_RBCAST[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_RBCAST[31:0] Number of broadcast packets. This register is enabled when the RX Broadcast packet parameter in the MAC Rx Stat Counter tab is set.

6.61. MAC_RX_64B [\(Ask a Question\)](#)

Name: MAC_RX_64B
Offset: 0x434
Reset: 0x0
Property: Read/Write-to Clear

Receive 64 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_R64[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_R64[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_R64[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_R64[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_R64[31:0] Receive 64 Byte Frame Counter. Incremented for each good or bad frame received which is 64 bytes in length inclusive (excluding framing bits but including FCS bytes). This register is enabled when the TRX 64byte packet parameter in the MAC Rx Stat Counters tab is set.

6.62. MAC_RX_511B [\(Ask a Question\)](#)

Name: MAC_RX_511B
Offset: 0x440
Reset: 0x0
Property: Read/Write-to Clear

Receive 256 to 511 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_R511[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_R511[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_R511[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_R511[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_R511[31:0] Receive 256 to 511 Byte Frame Counter. Incremented for each good or bad frame received which is 256 to 511 bytes in length inclusive (excluding framing bits but including FCS bytes). This register is enabled when the RX 256 to 511byte packet parameter in the MAC Rx Stat Counters tab is set

6.63. MAC_RX_1KB [\(Ask a Question\)](#)

Name: MAC_RX_1KB
Offset: 0x444
Reset: 0x0
Property: Read/Write-to Clear

Receive 512 to 1023 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_R1K[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_R1K[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_R1K[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_R1K[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_R1K[31:0] Receive 512 to 1023 Byte Frame Counter. Incremented for each good or bad frame received which is 51 to 1023 bytes in length inclusive (excluding framing bits but including FCS bytes). This register is enabled when the RX 512 to 1023byte packet parameter in the MAC Rx Stat Counters tab is set

6.64. MAC_RX_255B [\(Ask a Question\)](#)

Name: MAC_RX_255B
Offset: 0x43C
Reset: 0x0
Property: Read/Write-to Clear

Receive 128 to 255 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_R255[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_R255[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_R255[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_R255[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_R255[31:0] Receive 128 to 255 Byte Frame Counter. Incremented for each good or bad frame received which is 128 to 255 bytes in length inclusive (excluding framing bits but including FCS bytes). This register is enabled when the RX 128 to 255byte packet parameter in the MAC Rx Stat Counters tab is set

6.65. MAC_RX_127B [\(Ask a Question\)](#)

Name: MAC_RX_127B
Offset: 0x438
Reset: 0x0
Property: Read/Write-to Clear

Receive 65 to 127 Byte Frame Counter

Bit	31	30	29	28	27	26	25	24
	MAC_R127[31:24]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC_R127[23:16]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC_R127[15:8]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC_R127[7:0]							
Access	RWC	RWC	RWC	RWC	RWC	RWC	RWC	RWC
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MAC_R127[31:0] Receive 65 to 127 Byte Frame Counter. Incremented for each good or bad frame received which is 65 to 127 bytes in length inclusive (excluding framing bits but including FCS bytes). This register is enabled when the RX 65 to 127byte packet parameter in the MAC Rx Stat Counters tab is set.

6.66. MAC_ADDR_LOWER [\(Ask a Question\)](#)

Name: MAC_ADDR_LOWER
Offset: 0x024
Reset: 0x0
Property: Read/Write

MAC address lower 32 bits.

This is the configured MAC address lower 32 bit. This MAC address register holds the device's unique MAC address lower 32 bits. This register is combined with MAC address upper 16bits register to form the device's unique 48bit MAC address. The combined 48bit unique MAC address is used in the receive path to determine incoming packets are destined for the device and in the transmit path to populate the source MAC address field while sending the Ethernet frames.

Bit	31	30	29	28	27	26	25	24
	MAC ADDR BYTE 3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MAC ADDR BYTE 2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	MAC ADDR BYTE 1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MAC ADDR BYTE 0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:24 – MAC ADDR BYTE 3[7:0] MAC address lower 32 bits [31:24]

Bits 23:16 – MAC ADDR BYTE 2[7:0] MAC address lower 32 bits [23:16]

Bits 15:8 – MAC ADDR BYTE 1[7:0] MAC address lower 32bits [15:8]

Bits 7:0 – MAC ADDR BYTE 0[7:0] MAC address lower 32bits [7:0]

6.67. CORE_VER [\(Ask a Question\)](#)

Name: CORE_VER

Offset: 0x000

Reset: 0x0

Property: Read-only

Core version register. This register indicates current version of the core as shown in the example. Ex: If CORE_VER is set to 32h0201_0000, then it indicates major version of the core is 8h02 and minor version of the core is 8h01.

Bit	31	30	29	28	27	26	25	24
	MAJOR_VER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MINOR_VER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 31:24 – MAJOR_VER[7:0] Major version number of the Core

Bits 23:16 – MINOR_VER[7:0] Minor version number of the Core

6.68. MAC_ADDR_UPPER [\(Ask a Question\)](#)

Name: MAC_ADDR_UPPER

Offset: 0x020

Reset: 0x0

Property: Read/Write

MAC address upper 16 bits. This is the configured MAC address upper 16 bit. This MAC address register holds the device's unique MAC address upper 16 bits. This register is combined with MAC address lower 32bits register to form the device's unique 48bit MAC address. The combined 48bit unique MAC address is used in the receive path to determine incoming packets are destined for the device and in the transmit path to populate the source MAC address field while sending the Ethernet frames

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	MAC ADDR BYTE 5[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 15:8 – MAC ADDR BYTE 5[7:0] MAC address upper 16 bits [15:8]

Bits 15:8 – MAC ADDR BYTE 4[7:0] MAC address upper 16 bits [7:0]

7. Known Issues and Workarounds [\(Ask a Question\)](#)

As this is the first release, there are no known limitations and workarounds.

8. Discontinued Features and Devices [\(Ask a Question\)](#)

As this is the first release, there are no discontinued features and devices.

[illegible]

1Gbps:

- Data path of 1G Design is as below:**

2.5Gbps:

- Miv is Operating at 50Mhz used to configure the CoreGbE_MR registers
- 156.25MHZ XCVR_TX_CLK of CoreGbE_MR is driven by LANE0_RX_CLK_R of PF_XCVR_ERM
- 156.25MHZ XCVR_RX_CLK of CoreGbE_MR is driven by LANE0_TX_CLK_R of PF_XCVR_ERM
- SYS_CLK of CoreGbE_MR is driven by LANE0_TX_CLK_R of PF_XCVR_ERM
- SYS_TX_RESETN and XCVR_TX_RESETN of CoreGbE_MR are driven by LANE0_TX_CLK_STABLE of PF_XCVR_ERM
- SYS_RX_RESETN and XCVR_RX_RESETN of CoreGbE_MR are driven by LANE0_RX_VAL of PF_XCVR_ERM

- ARESETN of CoreGbE_MR is driven by FABRIC_RESET_N

Data path of 2.5Gbps is as below:

2.5G design: MiV <-> AxiProtconv + AXI4Interconnect <-> GbeMR <-> XCVR (PMA mode) <-> SMA
loop back (because we don't have HW which supports 2.5G PHY)

10. Glossary [\(Ask a Question\)](#)

Following are the list of terms and definitions used in the document.

Table 10-1. Terms and Definitions

Term	Definition
CSR	Control and Status Register
EB	Elastic Buffer
MAC	Media Access Controller
PCS	Physical Coding Sub-layer
PHY	Physical
PMA	Physical Medium Attachment
RWC	Read or Write to Clear
RX/Rx	Receiver
SERDES	SERIALISE / DESERIALISE
TX/Tx	Transmitter

11. Device Utilization and Performance [\(Ask a Question\)](#)

The data in this table is achieved using below configuration settings in Libero.

- **High-effort Layout** enabled in "Place and Route".
- Device **speed grade** is -1.
- Constraints given ***XCVR_TX_CLK/XCVR_RX_CLK*** - 156.25 MHz, ***SYS_CLK*** - 78.125 MHz, ***ACLK*** - 100 MHz

Table 11-1. CoreGbE_MR Utilization

Device Details		Resources			Performance	RAMs LSRAM
Family	Device	4LUT	DFF	Logic Elements		
PolarFire® SoC	MPFS095T-1FCS G536E	4477	2594	4852	ACLK- 258.799 MHz SYS_CLK- 235.349 MHz XCVR_TX_CLK- 278.396 MHz XCVR_RX_CLK- 285.225 MHz	5
RT PolarFire®	RTPF500ZTS-1FC 1509M	4477	2594	4871	ACLK- 216.123 MHz SYS_CLK- 241.138 MHz XCVR_TX_CLK- 273.149 MHz XCVR_RX_CLK- 292.740 MHz	5
PolarFire®	MPF100T-1FCG4 84E	4658	2594	4978	ACLK - 251.446 MHz SYS_CLK - 240.558 MHz XCVR_RX_CLK - 291.206 MHz XCVR_TX_CLK - 283.768 MHz	5

12. Revision History [\(Ask a Question\)](#)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	03/2026	Initial release.

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