Introduction (Ask a Question)

Core1588 provides hardware support for the implementation of an IEEE 1588 v2.0 Precision Time Protocol (PTP) capable system. This core parses the PTP frames and record the timestamp. Timestamp can be read by the firmware through APB target interface.

Core1588 Summary

Core Version	This document applies to Core1588 v3.0.
Supported Device Families	• SmartFusion® 2 • IGLOO® 2 • PolarFire® • PolarFire SoC • RT PolarFire
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Supported Interfaces	• **GMII**: Core1588 monitors the GMII interface between a MAC and PHY and detects the transmission and reception of IEEE 1588 frames. • **APB**: An APB (version 3) interface is included on the core to allow a system processor to access various registers in the core.
Licensing	**Obfuscated**: Obfuscated version is available with obfuscated Verilog RTL, obfuscated version supports unlimited functionality on silicon. Obfuscated version will be license locked and free with Libero Gold and Platinum license.
Installation Instructions	Core1588 must be installed to the IP Catalog of Libero SoC automatically through the update function. Alternatively, Core1588 could be manually downloaded from the catalog. Once the IP core is installed, it is configured, generated, and instantiated within SmartDesign for inclusion in the project.
Device Utilization and Performance	A summary of utilization and performance information for Core1588 is listed in the Device Utilization and Performance.

Core1588 Change Log Information

This section provides a comprehensive overview of the newly incorporated features, beginning with the most recent release. For more information about the problems resolved, see the Resolved Issues section.

Version	What's New
v3.0	• Added support for PTP v2.0 • Added support for one step timestamp insertion • Added support for PTP over UDP ipv4 and ipv6 • Added support for GMII interface
v2.0	First production release of Core1588

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1. Features (Ask a Question)

Core1588 has the following key features:

- IEEE 1588 v1.0 and v2.0 compatible
- Supports GMII interface (MAC to PHY) and APB interface for register access
- Supports the following different encapsulations for PTP event messages:
  - IEEE 1588 v1.0 (UDP/IPv4 multicast)
  - IEEE 1588 v1.0 (UDP/IPv4 multicast with VLAN)
  - IEEE 1588 v2.0 (UDP/IPv4 multicast)
  - IEEE 1588 v2.0 (UDP/IPv4 multicast with VLAN)
  - IEEE 1588 v2.0 (UDP/IPv4 unicast)
  - IEEE 1588 v2.0 (UDP/IPv4 unicast with VLAN)
  - IEEE 1588 v2.0(UDP/IPv6 unicast)
  - IEEE 1588 v2.0 (UDP/IPv6 unicast with VLAN)
  - IEEE 1588 v2.0 (UDP/IPv6 multicast)
  - IEEE 1588 v2.0 (UDP/IPv6 multicast with VLAN)
  - IEEE 1588 v2.0 (Ethernet multicast)
  - IEEE 1588 v2.0 (Ethernet multicast with VLAN)
- Supports to update timestamp field of PTP event messages when one step is enabled
- Supports the RTC counter with 48 bits second count, 32 bits nanosecond count and 24 bits sub-nanosecond count
- Supports interrupt when PTP event frame is transmitted or received

2. Core1588 Overview (Ask a Question)

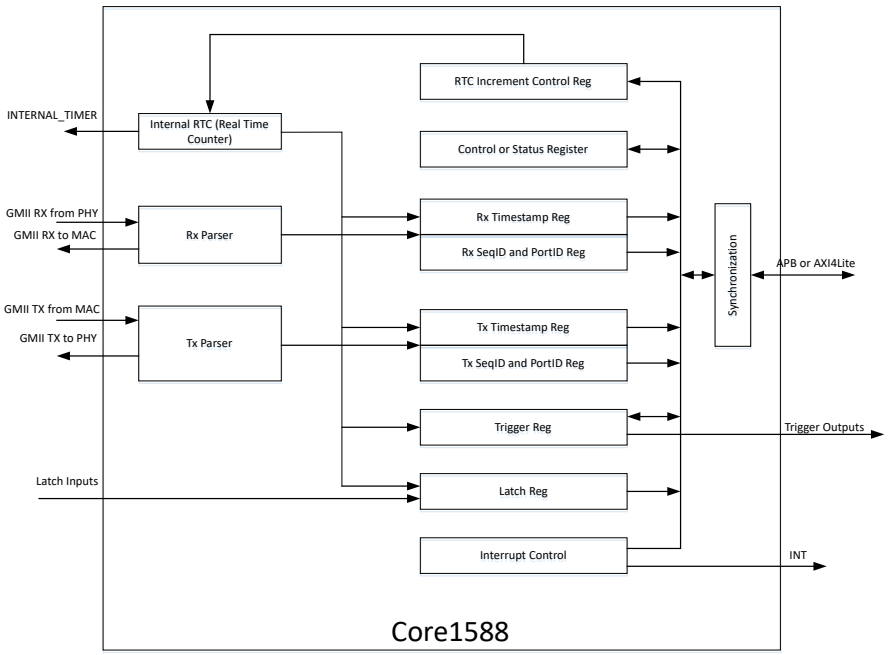
Core1588 provides hardware support for the implementation of an IEEE 1588 Precision Time Protocol (PTP) capable system. A firmware component that interacts with Core1588 will also form part of such a system. Core1588 maintains a Real Time Counter (RTC) and monitors the Ethernet GMII interface to identify IEEE 1588 type frames. The core timestamps receipt and transmission of PTP event message frames when enabled, can interrupt the system processor to cause action to be taken. Core1588 supports full duplex operation. An APB interface is present on the core and this allows the system processor to control how the core operates and to retrieve timestamp information.

Latch inputs and trigger outputs are present on Core1588 which provide the ability to accurately timestamp system events and to effect actions at predefined times. The interrupt mechanism can be used to alert the system processor when a latch or trigger event occurs but the processor does not necessarily have to be critically involved time wise in responding to latch and trigger events. For example, a trigger output could be used directly to cause some other action to occur in the system without waiting for the processor to do something.

3. Functional Description (Ask a Question)

This section describes the functional description of the Core1588.

Figure 3-1. Overview of Core1588



3.1. RTC (Ask a Question)

Core1588 contains 102 bits wide internal Real Time Counter (RTC). The upper 48 bits count seconds, the next 30 lower bits count nanoseconds, and the lowest 24 bits count sub nanoseconds. The lower 54 bits rollover when it counts one second. The counter increments by a programmable period with each PTP_CLK period and can be adjusted in 1ns resolution (incremented/decremented) through APB register access.

Writing to the RTCL, RTCM and RTCMSBSEC registers sets the internal RTC value. The value written to RTCL updates the 32-bit nanoseconds counter, value written to RTCM updates the lower 32 bits of seconds counter and value written to RTCMSBSEC updates upper 16 bits of seconds counter. The RTCL register should be written first, followed by a write to the RTCM register and followed by a write to RTCMSBSEC registers. The write to RTCL and RTCM only takes effect when the RTCMSBSEC register is written. In this way, all 80 bits of the internal RTC are updated on the same clock cycle.

When reading the internal RTC, RTCL should be read first followed by the RTCM register followed by the RTCMSBSEC register. Reading the RTCL register causes a snapshot to be taken of the lower 32-bit and upper 16 bits seconds counter and this snapshots value are returned on the subsequent read of the RTCM and RTCMSBSEC registers. This mechanism ensures that the RTCMSBSEC, RTCM and RTCL values are coincident.

The RTC is clocked by the PTP_CLK signal. On each rising edge of PTP_CLK the nanoseconds count of internal RTC increases by the increment value configured in RTCINCR register. Speeding up or slowing down of the internal RTC can be achieved in two ways.

3.1.1. Alternative Increment Mode (Ask a Question)

Increment internal RTC by a fixed value for a fixed number of input clocks, followed by an alternative increment value for a single clock. The ADJUST and RTCINCR bits [31:24] registers are used to control

adjustment of the internal RTC. ADJUST register contains a five-bit adjustment value to add to the nanoseconds count (when not adding the default of increment value configured in RTCINCR register bits [31:24]), an enable bit and 24 bits for a counter rollover value. (The remaining two bits of the 32 bits ADJUST register are reserved.)

When the enable bit is set, the 24-bit counter rollover value is used in conjunction with an independent 24-bit counter, also clocked by PTP_CLK. This counter increments by 1 on each PTP_CLK rising edge and when its value matches the 24-bit value held in the ADJUST register the counter returns to zero and begins to increment again. At the same time, the adjustment value held in the upper five bits of the ADJUST register is added to the internal RTC nanoseconds count instead of the usual value of increment configured in RTCINCR register bits [31:24]. In this way, the nanoseconds count can occasionally be updated by an amount greater than or less than increment value configured in RTCINCR bits [31:24], essentially allowing the internal RTC to be speeded up or slowed down. The adjusted value ranges from 0 to 31.

Important: Alternative increment mode is a legacy mode of operation, it is not recommended to use the alternative increment mode of operation. It is recommended to use increment mode by incrementing internal RTC by a fixed value every input clock by configuring RTCINCR register.

3.1.2. Increment Mode (Ask a Question)

In increment mode, internal RTC is incremented by a fixed value every PTP_CLK clock. The amount by which the counter increments each clock cycle is controlled by the RTCINCR register. Bits [31:24] are the default increment value in nanoseconds and lower 24 bits are the sub-nanoseconds resolution. The internal RTC increments by the value in bits [31:24] plus sub-nanoseconds bits [23:0], each clock cycle.

The bits representing sub-nanosecond intervals [23:0] allow a resolution of approximately 58.6 attoseconds (5.86E-17). To calculate the value to write to the sub-nanosecond register, the user should take the decimal value of the sub-nanosecond value, multiply it by 2 to the power of 24 (which is 16,777,216), and then convert the result to hexadecimal. For example, for a sub-nanosecond value of 0.5, the user should write 0x800000 (0.5 * 2^24). To increment the internal RTC by 5.5 ns each clock cycle, the user should configure the upper 8 bits [31:24] of the RTCINCR register to 5 and the lower 24 bits [23:0] of the RTCINCR register to 0x800000 (0.5 * 2^24).

3.2. Parsing of GMII Traffic (Ask a Question)

Two finite state machines are used within Core1588 for parsing transmit and receive traffic on the GMII interface. The core supports full duplex operation. When PTP event message frames are detected, the core records a timestamp for the relevant frame along with some identification fields from the frame. A timestamp is simply a record of the RTC value at the time when a particular point of the frame traverses the MAC-PHY interface. The timestamp reference point is defined by IEEE 1588 as the beginning of the first symbol after the Start of Frame (SOF) delimiter.

When ONE_STEP_SYNC_MODE bit is set to 1 in GCFG register, *originTimestamp* field of SYNC frame will be updated by the current RTC value (sampled on SOF) and then SYNC frame is transmitted. As the *originTimestamp* field is updated, Frame Check Sequence (FCS) will also be updated by Core1588.

3.3. Frames of Interest (Ask a Question)

Core1588 only responds to certain IEEE 1588 frames, partly depending on whether it is operating in requester or responder mode. The MST_EN bit of the GCFG register determines the mode of operation of the core.

Core1588 only detects transmission of Sync frame and Delay_Resp, when in requester mode.

Core1588 only detects transmission of Delay_Req frame, when in responder mode.

Transmission of Pdelay_Req and Pdelay_Resp frames are detected regardless of whether the core is operating in requester or responder mode.

Reception of Sync, Delay_Req, Pdelay_Req, and Pdelay_Resp frames are always detected in both requester and responder mode.

When receipt of a frame of interest is detected, the RIRTS bit of the Raw Interrupt Status (RIS) register is set to '1'. When transmission of a frame of interest is detected, the RITTS bit of the RIS register is set to '1'. These bits must be cleared by firmware before the receipt/transmission of another frame of interest can be detected and timestamped. It is envisaged that firmware will clear the RIRTS or RITTS bit after reading the relevant timestamp registers. The timestamp registers associated with a received frame are RTSL, RTSM, and RTSMSBSECSUBNS, and the timestamp registers for a transmitted frame are TTSL, TTSM, and TTSMSBSECSUBNS.

3.4. Latch Inputs (Ask a Question)

The core can be configured to support up to three latch inputs. The LATCH_NUM parameter, which can be set using the core's configuration GUI, controls the number of latch inputs supported.

When a rising edge is detected on a latch input, the current RTC value is recorded in latch registers and, if enabled, an interrupt is generated by asserting the INT output. A circuit clocked by the PTP_CLK clock signal detects the rising edges on the latch inputs. If the signal driving a latch input is not in the PTP_CLK clock domain then user must ensure that the signal is high for at least 3 clock cycles of PTP_CLK period, for a rising edge to be detected on the latch input.

The LT0L, LT0M, and LT0MSBSEC registers are used to record the RTC value when a rising edge is detected on the LATCH0 input. Similarly, the LT1L, LT1M, and LT1MSBSEC registers are associated with the LATCH1 input and the LT2L, LT2M, and LT2MSBSEC registers are associated with the LATCH2 input.

There is separate enable bits (LT0_EN, LT1_EN, and LT2_EN) in the GCFG register for each of the latch register pairs. If any of these enable bits is set to '0' then the corresponding latch register pair will not be updated when a rising edge is detected on the relevant latch input. The enable bit provide a mechanism to hold a value in a latch register pair even though subsequent rising edges may occur on the relevant latch input. For example, if the LT0_EN bit is '0' then the LT0L, LT0M, and LT0MSBSEC registers will not be updated when a rising edge occurs on the LATCH0 input.

The IELT0, IELT1, and IELT2 bits of the Interrupt Enable Register (IER) are used to control whether rising edges on the latch inputs cause an interrupt to be generated.

3.5. Trigger Outputs (Ask a Question)

When it is appropriately configured, up to three trigger outputs can be provided by the core. The TRIG_NUM parameter, which can be set using the core's configuration GUI, controls the number of trigger outputs supported.

When the RTC reaches a preset trigger value, a pulse is generated on the corresponding trigger output, if pulse generation has been enabled for the relevant trigger output. The pulse is a one clock cycle pulse in the PTP_CLK clock domain. The TT0_EN, TT1_EN, and TT2_EN bits of the GCFG register control whether pulses are generated on the trigger outputs.

An interrupt can also be generated on reaching a trigger time. The IETT0, IETT1, and IETT2 bits of the Interrupt Enable Register (IER) control whether an interrupt is generated on a time match.

The TT0L, TT0M, and TT0MSBSEC registers store the match time for the TRIG0 output. The TT1L, TT1M, and TT1MSBSEC registers relate to the TRIG1 output, and the TT2L, TT2M, and TT1MSBSEC registers relate to the TRIG2 output.

3.6. Interrupts (Ask a Question)

Core1588 can interrupt the system processor when various events occur. The IER and the Masked Interrupt Status (MIS) register can be accessed by the system processor to enable or disable interrupts and to identify the source of any pending interrupt. The core can generate an interrupt

when a frame of interest is detected on the RMII interface or when a latch or trigger event occurs. See the descriptions for the IER and MIS registers for more details on the bits within these registers.

Interrupts are cleared by writing a '1' to the appropriate bit position or positions in the Raw Interrupt Status (RIS) register.

The RIRTS/RITTS bit of the RIS register will be set on detection of the receipt/transmission of an IEEE 1588 frame of interest. The RIRTS/RITTS bit must be cleared by firmware before receipt/transmission of another frame of interest can be detected and timestamped.

4. IP Core Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the Core1558 Configurator settings and I/O signals.

4.1. Core1558 Configurator Settings (Ask a Question)

The following table lists the Core1558 for configuring the core.

Important: The Name column in the following table shows the actual parameter names used in RTL. The Description column starts with the parameter names as they appear in the Core1558 Configurator.

Table 4-1. Core1558 Parameter Descriptions

Parameter Name	Valid Values	Default Value	Description
TRIG_NUM	0:0 1:1 2:2 3:3	0	**Number Of Trigger Outputs** This parameter configures the number of trigger outputs
LATCH_NUM	0:0 1:1 2:2 3:3	0	**Number of Latch Inputs** This parameter configures the number of latch inputs

4.2. Input and Output Signals (Ask a Question)

This section discusses the parameters in the Core1558 I/O signals.

The following table lists the clock ports for Core1558.

Table 4-2. Core1558 Clock Ports

Parameter Name	Width (Bits)	Valid Range	Default Value
PCLK	1	Input	APB Clock
PTP_CLK	1	Input	Local clock for timer
TXCLK	1	Input	Ethernet MAC transmit clock. GMII interface transmit port should be synchronized with this clock.
RXCLK	1	Input	Ethernet MAC receive clock. GMII interface receive port should be synchronized with this clock.

The following table lists the Port Descriptions for Core1558.

Table 4-3. Core1588 Port Descriptions

Port Name	Width	Direction	Clock Domain	Description
PRESETN	1	Input	PCLK	Active-Low reset. It resets the PCLK clock domain logic to its initial state. PRESETN reset should be synchronized in PCLK clock domain externally.
PTPRSTN	1	Input	PTP_CLK	Active-Low reset. It resets the PTP_CLK clock domain logic to its initial state. PTPRSTN reset should be synchronized in PTP_CLK clock domain externally.
TXRSTN	1	Input	TXCLK	Active-Low reset. It resets the TXCLK clock domain logic to its initial state. TXRSTN reset should be synchronized in TXCLK clock domain externally.
RXRSTN	1	Input	RXCLK	Active-Low reset. It resets the RXCLK clock domain logic to its initial state. RXRSTN reset should be synchronized in RXCLK clock domain externally.

Table 4-3. Core1588 Port Descriptions (continued)

Port Name	Width	Direction	Clock Domain	Description
APB Interface Ports				
PSEL	1	Input	PCLK	APB select
PENABLE	1	Input	PCLK	APB enable
PWRITE	1	Input	PCLK	APB write
PADDR	9	Input	PCLK	APB address
PWDATA	32	Input	PCLK	APB write data
PRDATA	32	Output	PCLK	APB read data
PREADY	1	Output	PCLK	APB ready
PSLVERR	1	Output	PCLK	APB responder error
GMII Interface Ports (towards MAC)				
TXD_MAC	8	Input	TXCLK	GMII transmit data
TXEN_MAC	1	Input	TXCLK	GMII transmit enable
TXER_MAC	1	Input	TXCLK	GMII transmit error This port is not used in the core. It is just delayed by one clock cycle to align with delay of TXEN_MAC and TXD_MAC.
RXD_MAC	8	Output	RXCLK	GMII receive data
RXDV_MAC	1	Output	RXCLK	GMII receive data valid
RXER_MAC	1	Output	RXCLK	GMII receive error This port is used as pass through from input to output
CRS_MAC	1	Output	Asynchronous	GMII carrier sense flag This port is used as pass through from input to output.
COL_MAC	1	Output	Asynchronous	GMII collision detect flag This port is used as pass through from input to output.
GMII Interface Ports (towards SGMII)				
TXD	8	Output	TXCLK	Transmit data
TXEN	1	Output	TXCLK	Transmit enable
TXER	1	Output	TXCLK	Transmit error
RXD	8	Input	RXCLK	Receive data
RXDV	1	Input	RXCLK	Receive data valid
RXER	1	Input	RXCLK	Receive error
CRS	1	Input	Asynchronous	GMII carrier sense flag
COL	1	Input	Asynchronous	GMII collision detect flag
Latch and Trigger Ports				
TRIG0	1	Output	PTP_CLK	Trigger 0 A one clock cycle pulse (in the PTP_CLK clock domain) is generated on this output when the RTC value reaches the value preset in the TT0L, TT0M, and TT0MSBSEC registers. **Note:** This port is visible to the user only when **Number of Trigger Outputs** parameter is greater than 0.
TRIG1	1	Output	PTP_CLK	Trigger 1 A one clock cycle pulse (in the PTP_CLK clock domain) is generated on this output when the RTC value reaches the value preset in the TT1L, TT1M, and TT1MSBSEC registers. **Note:** This port is visible to the user only when **Number of Trigger Outputs** parameter is greater than 1.

Table 4-3. Core1588 Port Descriptions (continued)

Port Name	Width	Direction	Clock Domain	Description
TRIG2	1	Output	PTP_CLK	Trigger 2 A one clock cycle pulse (in the PTP_CLK clock domain) is generated on this output when the RTC value reaches the value preset in the TT2L, TT2M, and TT2MSBSEC registers. **Note:** This port is visible to the user only when **Number of Trigger Outputs** parameter is greater than 2.
LATCH0	1	Input	PTP_CLK	Latch 0 When a rising edge is detected on this input, the current RTC value is latched into the LT0L, LT0M, and LT0MSBSEC registers. This input is synchronized in PTP_CLK clock domain. User should ensure that it remains asserted for at least 3 clock cycles of PTP_CLK clock. **Note:** This port is visible to the user only when **Number of Latch Inputs** parameter is greater than 0.
LATCH1	1	Input	PTP_CLK	Latch 1 When a rising edge is detected on this input, the current RTC value is latched into the LT1L, LT1M, and LT1MSBSEC registers. This input is synchronized in PTP_CLK clock domain. User should ensure that it remains asserted for at least 3 clock cycles of PTP_CLK clock. **Note:** This port is visible to the user only when **Number of Latch Inputs** parameter is greater than 1.
LATCH2	1	Input	PTP_CLK	Latch 2 When a rising edge is detected on this input, the current RTC value is latched into the LT2L, LT2M, and L2MSBSEC registers. This input is synchronized in PTP_CLK clock domain. User should ensure that it remains asserted for at least 3 clock cycles of PTP_CLK clock. **Note:** This port is visible to the user only when **Number of Latch Inputs**parameter is greater than 2.
Interrupt Ports				
INT	1	Output	PCLK	Active-High interrupt signal. It is a level triggered interrupt. It will be asserted when any bit of MIS register is asserted. It will be de-asserted when all the bits of MIS register is de-asserted
Internal Timer Port				
INTERNAL_TIMER	102	Output	PTP_CLK	Internal RTC. RTC encoded is shown as follows: • [101:54] - 48 bits Second • [53:24] - 30 bits Nanosecond • [23:0] - 24 bits Sub-nanosecond The upper 48 bits indicate the seconds count, next lower 32 bits indicate nanosecond count, and the lowest 24 bits indicate the sub-nanoseconds count.
Debug Port				
PPS	1	Output	PTP_CLK	Pulse per second. One pulse is generated on PTP_CLK domain when second counter is incremented by 1.

5. Implementation of Core1588 (Ask a Question)

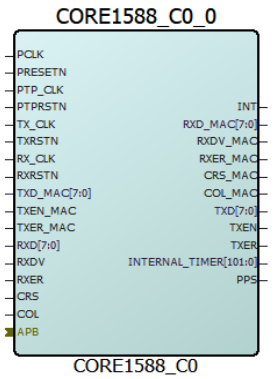
This section describes implementation of the Core1588 in Libero Design Suite.

5.1. SmartDesign (Ask a Question)

Core1588 is available for download to the SmartDesign IP Catalog through the Libero® SOC web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, see the Libero SOC online help.

The following figure shows an example of an instantiated view of Core1588 on the SmartDesign canvas. The core can be configured using its configuration GUI.

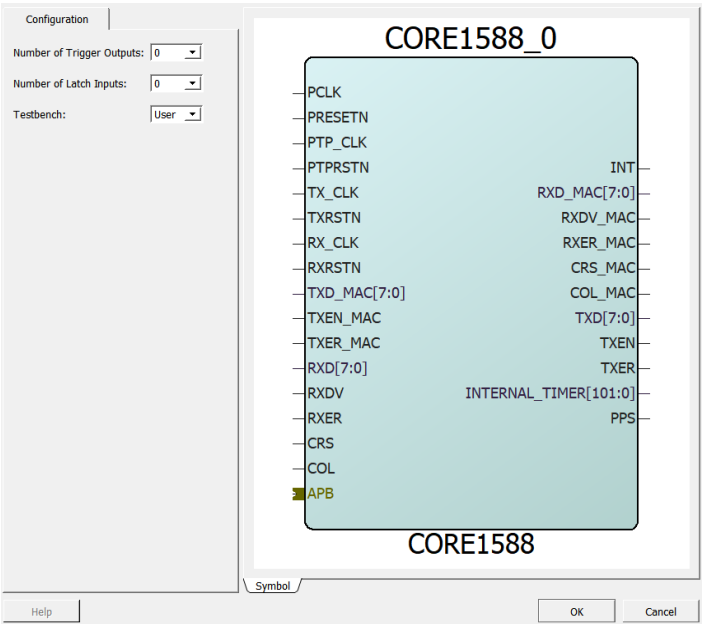
Figure 5-1. Example Instantiation of Core1588 on SmartDesign Canvas



5.1.1. Configuring the Core1588 (Ask a Question)

This section shows how the core instance can be configured using its configuration GUI.

Figure 5-2. Core1588 Configuration GUI



The configuration options displayed in the configuration GUI correspond with the configuration parameters listed in the Core1558 Configurator Settings.

5.1.2. Synthesis in Libero SoC (Ask a Question)

To run synthesis, perform the following steps:

1. To run synthesis with the configuration selected in the configuration GUI, set the design root appropriately.
2. Click the **Synthesis** icon in Libero IDE to launch the Synplicity synthesis tool and click **Run** button in the synthesis window to run synthesis.

5.1.3. Place-and-Route in Libero SoC (Ask a Question)

To run the place and route, perform the following steps:

1. Having set the design root appropriately and run **Synthesis**.
2. To invoke Designer, click the **Place and Route** icon in Libero SoC.

6. Register Map and Descriptions (Ask a Question)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	GCFG	7:0				PTP_UNICAST_EN	REQ_EN		ONE_STEP_SYNC	ENCOR
		15:8	LT2_EN	LT1_EN	LT0_EN	TT2_EN	TT1_EN	TT0_EN		
		23:16								
		31:24								
0x04	IER	7:0	IELT2	IELT1	IELT0	IETT2	IETT1	IETT0	IERTS0	IETTS0
		15:8	IEPTPRXDELAYREQ	IEPTPRXSYNC	IEPTPTXPDELAYRESP	IEPTPTXPDELAYREQ	IEPTPTXDELAYRESP	IEPTPTXDELAYREQ	IEPTPTXSYNC	IERTCSEC
		23:16		IEPEERRTSID	IEPEERTTSID	IERTSID	IETTSID	IEPTPRXPDELAYRESP	IEPTPRXPDELAYREQ	IEPTPRXDELAYRESP
		31:24								
0x08	MIS	7:0	ILT2	ILT1	ILT0	ITT2	ITT1	ITT0	IRTS	ITTS
		15:8	IPTPRXDELAYREQ	IPTPRXSYNC	IPTPTXPDELAYRESP	IPTPTXPDELAYREQ	IPTPTXDELAYRESP	IPTPTXDELAYREQ	IPTPTXSYNC	IRTCSEC
		23:16		IPEERRTSID	IPEERTTSID	IRTSID	ITTSID	IPTPRXPDELAYRESP	IPTPRXPDELAYREQ	IPTPRXDELAYRESP
		31:24								
0x0C	RIS	7:0	RILT2	RILT1	RILT0	RITT2	RITT1	RITT0	RIRTS	RITTS
		15:8	RIPTPRXDELAYREQ	RIPTPRXSYNC	RIPTPTXPDELAYRESP	RIPTPTXPDELAYREQ	RIPTPTXDELAYRESP	RIPTPTXDELAYREQ	RIPTPTXSYNC	RIRTCSEC
		23:16		RIPEERRTSID	RIPEERTTSID	RIRTSID	RITTSID	RIPTPRXPDELAYRESP	RIPTPRXPDELAYREQ	RIPTPRXDELAYRESP
		31:24								
0x10	TTSL	7:0	PTP_TX_NSEC[7:0]							
		15:8	PTP_TX_NSEC[15:8]							
		23:16	PTP_TX_NSEC[23:16]							
		31:24	PTP_TX_NSEC[31:24]							
0x14	TTSM	7:0	PTP_TX_SEC_LSB_32BITS[7:0]							
		15:8	PTP_TX_SEC_LSB_32BITS[15:8]							
		23:16	PTP_TX_SEC_LSB_32BITS[23:16]							
		31:24	PTP_TX_SEC_LSB_32BITS[31:24]							
0x18	TTSID	7:0	PTP_TX_SEQ_ID[7:0]							
		15:8	PTP_TX_SEQ_ID[15:8]							
		23:16								
		31:24								
0x1C	RTSL	7:0	PTP_RX_NSEC[7:0]							
		15:8	PTP_RX_NSEC[15:8]							
		23:16	PTP_RX_NSEC[23:16]							
		31:24	PTP_RX_NSEC[31:24]							
0x20	RTSM	7:0	PTP_RX_SEC_LSB_32BITS[7:0]							
		15:8	PTP_RX_SEC_LSB_32BITS[15:8]							
		23:16	PTP_RX_SEC_LSB_32BITS[23:16]							
		31:24	PTP_RX_SEC_LSB_32BITS[31:24]							
0x24	RTSID2	7:0	PTP_RX_SRC_PORTID_UPPER_16BITS[7:0]							
		15:8	PTP_RX_SRC_PORTID_UPPER_16BITS[15:8]							
		23:16	PTP_RX_SEQ_ID[7:0]							
		31:24	PTP_RX_SEQ_ID[15:8]							
0x28	RTSID1	7:0	PTP_RX_SRC_PORTID_MID_32BITS[7:0]							
		15:8	PTP_RX_SRC_PORTID_MID_32BITS[15:8]							
		23:16	PTP_RX_SRC_PORTID_MID_32BITS[23:16]							
		31:24	PTP_RX_SRC_PORTID_MID_32BITS[31:24]							
0x2C	RTSID0	7:0	PTP_RX_SRC_PORTID_LOWER_32BITS[7:0]							
		15:8	PTP_RX_SRC_PORTID_LOWER_32BITS[15:8]							
		23:16	PTP_RX_SRC_PORTID_LOWER_32BITS[23:16]							
		31:24	PTP_RX_SRC_PORTID_LOWER_32BITS[31:24]							

Register Map and Descriptions (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x30	RTCL	7:0	RTC_NSEC[7:0]							
		15:8	RTC_NSEC[15:8]							
		23:16	RTC_NSEC[23:16]							
		31:24			RTC_NSEC[29:24]					
0x34	RTCM	7:0	RTC_SEC_LSB_32BITS[7:0]							
		15:8	RTC_SEC_LSB_32BITS[15:8]							
		23:16	RTC_SEC_LSB_32BITS[23:16]							
		31:24	RTC_SEC_LSB_32BITS[31:24]							
0x38	ADJUST	7:0	ADJCM[7:0]							
		15:8	ADJCM[15:8]							
		23:16	ADJCM[23:16]							
		31:24	ADJVAL[4:0]					ADJEN		
0x3C ... 0x3F	Reserved									
0x40	TT0L	7:0	TT0_NSEC[7:0]							
		15:8	TT0_NSEC[15:8]							
		23:16	TT0_NSEC[23:16]							
		31:24	TT0_NSEC[31:24]							
0x44	TT0M	7:0	TT0_SEC_LSB_32BITS[7:0]							
		15:8	TT0_SEC_LSB_32BITS[15:8]							
		23:16	TT0_SEC_LSB_32BITS[23:16]							
		31:24	TT0_SEC_LSB_32BITS[31:24]							
0x48	TT1L	7:0	TT1_NSEC[7:0]							
		15:8	TT1_NSEC[15:8]							
		23:16	TT1_NSEC[23:16]							
		31:24	TT1_NSEC[31:24]							
0x4C	TT1M	7:0	TT1_SEC_LSB_32BITS[7:0]							
		15:8	TT1_SEC_LSB_32BITS[15:8]							
		23:16	TT1_SEC_LSB_32BITS[23:16]							
		31:24	TT1_SEC_LSB_32BITS[31:24]							
0x50	TT2L	7:0	TT2_NSEC[7:0]							
		15:8	TT2_NSEC[15:8]							
		23:16	TT2_NSEC[23:16]							
		31:24	TT2_NSEC[31:24]							
0x54	TT2M	7:0	TT2_SEC_LSB_32BITS[7:0]							
		15:8	TT2_SEC_LSB_32BITS[15:8]							
		23:16	TT2_SEC_LSB_32BITS[23:16]							
		31:24	TT2_SEC_LSB_32BITS[31:24]							
0x58	LT0L	7:0	LT0_NSEC[7:0]							
		15:8	LT0_NSEC[15:8]							
		23:16	LT0_NSEC[23:16]							
		31:24	LT0_NSEC[31:24]							
0x5C	LT0M	7:0	LT0_SEC_LSB_32BITS[7:0]							
		15:8	LT0_SEC_LSB_32BITS[15:8]							
		23:16	LT0_SEC_LSB_32BITS[23:16]							
		31:24	LT0_SEC_LSB_32BITS[31:24]							
0x60	LT1L	7:0	LT1_NSEC[7:0]							
		15:8	LT1_NSEC[15:8]							
		23:16	LT1_NSEC[23:16]							
		31:24	LT1_NSEC[31:24]							
0x64	LT1M	7:0	LT1_SEC_LSB_32BITS[7:0]							
		15:8	LT1_SEC_LSB_32BITS[15:8]							
		23:16	LT1_SEC_LSB_32BITS[23:16]							
		31:24	LT1_SEC_LSB_32BITS[31:24]							
0x68	LT2L	7:0	LT2_NSEC[7:0]							
		15:8	LT2_NSEC[15:8]							
		23:16	LT2_NSEC[23:16]							
		31:24	LT2_NSEC[31:24]							

Register Map and Descriptions (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x6C	LT2M	7:0	LT2_SEC_LSB_32BITS[7:0]							
		15:8	LT2_SEC_LSB_32BITS[15:8]							
		23:16	LT2_SEC_LSB_32BITS[23:16]							
		31:24	LT2_SEC_LSB_32BITS[31:24]							
0x70	TTSMSBSECSUBNS	7:0	PTP_TX_SEC_MSB_16BITS[7:0]							
		15:8	PTP_TX_SEC_MSB_16BITS[15:8]							
		23:16	PTP_TX_SUBNSEC[7:0]							
		31:24	PTP_TX_SUBNSEC[15:8]							
0x74	RTSMSBSECSUBNS	7:0	PTP_RX_SEC_MSB_16BITS[7:0]							
		15:8	PTP_RX_SEC_MSB_16BITS[15:8]							
		23:16	PTP_RX_SUBNSEC[7:0]							
		31:24	PTP_RX_SUBNSEC[15:8]							
0x78	RTCMSBSEC	7:0	RTC_SEC_MSB_16BITS[7:0]							
		15:8	RTC_SEC_MSB_16BITS[15:8]							
		23:16								
		31:24								
0x7C	TT0MSBSEC	7:0	TT0_SEC_MSB_16BITS[7:0]							
		15:8	TT0_SEC_MSB_16BITS[15:8]							
		23:16								
		31:24								
0x80	TT1MSBSEC	7:0	TT1_SEC_MSB_16BITS[7:0]							
		15:8	TT1_SEC_MSB_16BITS[15:8]							
		23:16								
		31:24								
0x84	TT2MSBSEC	7:0	TT2_SEC_MSB_16BITS[7:0]							
		15:8	TT2_SEC_MSB_16BITS[15:8]							
		23:16								
		31:24								
0x88	LT0MSBSEC	7:0	LT0_SEC_MSB_16BITS[7:0]							
		15:8	LT0_SEC_MSB_16BITS[15:8]							
		23:16								
		31:24								
0x8C	LT1MSBSEC	7:0	LT1_SEC_MSB_16BITS[7:0]							
		15:8	LT1_SEC_MSB_16BITS[15:8]							
		23:16								
		31:24								
0x90	LT2MSBSEC	7:0	LT2_SEC_MSB_16BITS[7:0]							
		15:8	LT2_SEC_MSB_16BITS[15:8]							
		23:16								
		31:24								
0x94	RTCCTRL	7:0	ADJ_VALUE[7:0]							
		15:8	ADJ_VALUE[15:8]							
		23:16	ADJ_VALUE[23:16]							
		31:24	ADD_SUBTRACT		ADJ_VALUE[29:24]					
0x98	RTCINCR	7:0	SUB_NS_INCR[7:0]							
		15:8	SUB_NS_INCR[15:8]							
		23:16	SUB_NS_INCR[23:16]							
		31:24	NS_INCR[7:0]							
0x9C	TXUCASTADDR0	7:0	TX_UNICAST_IP_ADDR0[7:0]							
		15:8	TX_UNICAST_IP_ADDR0[15:8]							
		23:16	TX_UNICAST_IP_ADDR0[23:16]							
		31:24	TX_UNICAST_IP_ADDR0[31:24]							
0xA0	TXUCASTADDR1	7:0	TX_UNICAST_IP_ADDR1[7:0]							
		15:8	TX_UNICAST_IP_ADDR1[15:8]							
		23:16	TX_UNICAST_IP_ADDR1[23:16]							
		31:24	TX_UNICAST_IP_ADDR1[31:24]							

Register Map and Descriptions (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xA4	TXUCASTADDR2	7:0	TX_UNICAST_IP_ADDR2[7:0]							
		15:8	TX_UNICAST_IP_ADDR2[15:8]							
		23:16	TX_UNICAST_IP_ADDR2[23:16]							
		31:24	TX_UNICAST_IP_ADDR2[31:24]							
0xA8	TXUCASTADDR3	7:0	TX_UNICAST_IP_ADDR3[7:0]							
		15:8	TX_UNICAST_IP_ADDR3[15:8]							
		23:16	TX_UNICAST_IP_ADDR3[23:16]							
		31:24	TX_UNICAST_IP_ADDR3[31:24]							
0xAC	RXUCASTADDR0	7:0	RX_UNICAST_IP_ADDR0[7:0]							
		15:8	RX_UNICAST_IP_ADDR0[15:8]							
		23:16	RX_UNICAST_IP_ADDR0[23:16]							
		31:24	RX_UNICAST_IP_ADDR0[31:24]							
0xB0	RXUCASTADDR1	7:0	RX_UNICAST_IP_ADDR1[7:0]							
		15:8	RX_UNICAST_IP_ADDR1[15:8]							
		23:16	RX_UNICAST_IP_ADDR1[23:16]							
		31:24	RX_UNICAST_IP_ADDR1[31:24]							
0xB4	RXUCASTADDR2	7:0	RX_UNICAST_IP_ADDR2[7:0]							
		15:8	RX_UNICAST_IP_ADDR2[15:8]							
		23:16	RX_UNICAST_IP_ADDR2[23:16]							
		31:24	RX_UNICAST_IP_ADDR2[31:24]							
0xB8	RXUCASTADDR3	7:0	RX_UNICAST_IP_ADDR3[7:0]							
		15:8	RX_UNICAST_IP_ADDR3[15:8]							
		23:16	RX_UNICAST_IP_ADDR3[23:16]							
		31:24	RX_UNICAST_IP_ADDR3[31:24]							
0xBC	PEERTTSL	7:0	PTP_PEER_TXNSEC[7:0]							
		15:8	PTP_PEER_TXNSEC[15:8]							
		23:16	PTP_PEER_TXNSEC[23:16]							
		31:24	PTP_PEER_TXNSEC[31:24]							
0xC0	PEERTTSM	7:0	PTP_PEER_TXSECLSB32BITS[7:0]							
		15:8	PTP_PEER_TXSECLSB32BITS[15:8]							
		23:16	PTP_PEER_TXSECLSB32BITS[23:16]							
		31:24	PTP_PEER_TXSECLSB32BITS[31:24]							
0xC4	PEERTTSMSBSECSUBNS	7:0	PTP_PEER_TXSECMSB16BITS[7:0]							
		15:8	PTP_PEER_TXSECMSB16BITS[15:8]							
		23:16	PTP_PEER_TXSUBNSEC[7:0]							
		31:24	PTP_PEER_TXSUBNSEC[15:8]							
0xC8	PEERTTSID	7:0	PTP_PEER_TXSEQID[7:0]							
		15:8	PTP_PEER_TXSEQID[15:8]							
		23:16								
		31:24								
0xCC	PEERRTSL	7:0	PTP_PEER_RXNSEC[7:0]							
		15:8	PTP_PEER_RXNSEC[15:8]							
		23:16	PTP_PEER_RXNSEC[23:16]							
		31:24	PTP_PEER_RXNSEC[31:24]							
0xD0	PEERRTSM	7:0	PTP_PEER_RXSEC_LSB32BITS[7:0]							
		15:8	PTP_PEER_RXSEC_LSB32BITS[15:8]							
		23:16	PTP_PEER_RXSEC_LSB32BITS[23:16]							
		31:24	PTP_PEER_RXSEC_LSB32BITS[31:24]							
0xD4	PEERRTSMSBSECSUBNS	7:0	PTP_PEER_RXSEC_MSB16BITS[7:0]							
		15:8	PTP_PEER_RXSEC_MSB16BITS[15:8]							
		23:16	PTP_PEER_RXSUBNSEC[7:0]							
		31:24	PTP_PEER_RXSUBNSEC[15:8]							
0xD8	PEERRTSID2	7:0	PTP_PEER_RXSRCPORTID_MSB16BITS[7:0]							
		15:8	PTP_PEER_RXSRCPORTID_MSB16BITS[15:8]							
		23:16	PTP_PEER_RXSEQID[7:0]							
		31:24	PTP_PEER_RXSEQID[15:8]							
0xDC	PEERRTSID1	7:0	PTP_PEER_RXSRCPORTID_MID32BITS[7:0]							
		15:8	PTP_PEER_RXSRCPORTID_MID32BITS[15:8]							
		23:16	PTP_PEER_RXSRCPORTID_MID32BITS[23:16]							
		31:24	PTP_PEER_RXSRCPORTID_MID32BITS[31:24]							

Register Map and Descriptions (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xE0	PEERRTSID0	7:0	PTP_PEER_RXSRCPORTID_LSB32BITS[7:0]							
		15:8	PTP_PEER_RXSRCPORTID_LSB32BITS[15:8]							
		23:16	PTP_PEER_RXSRCPORTID_LSB32BITS[23:16]							
		31:24	PTP_PEER_RXSRCPORTID_LSB32BITS[31:24]							

6.1. GCFG (Ask a Question)

Name: GCFG
Offset: 0x000
Reset: 0x0
Property: Read/Write

General configuration register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	LT2_EN	LT1_EN	LT0_EN	TT2_EN	TT1_EN	TT0_EN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
				PTP_UNICAST_EN	REQ_EN		ONE_STEP_SYNC	ENCOR
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0

Bit 15 – LT2_EN 0: Disable latch 2 timestamp registers 1: Enable latch 2 timestamp registers This bit must be set to 1 in order for the LT2L and LT2M registers to be updated with the RTC value when a rising edge is observed on the LATCH2 input.

Bit 14 – LT1_EN 0: Disable latch 1 timestamp registers 1: Enable latch 1 timestamp registers This bit must be set to 1 in order for the LT1L and LT1M registers to be updated with the RTC value when a rising edge is observed on the LATCH1 input.

Bit 13 – LT0_EN 0: Disable latch 0 timestamp registers 1: Enable latch 0 timestamp registers This bit must be set to 1 in order for the LT0L and LT0M registers to be updated with the RTC value when a rising edge is observed on the LATCH0 input

Bit 12 – TT2_EN 0: Disable TRIG2 output 1: Enable TRIG2 output This bit must be set to 1 in order for a pulse to be generated on the TRIG2 output when the RTC value reaches the time set in the TT2L and TT2M registers.

Bit 11 – TT1_EN 0: Disable TRIG1 output 1: Enable TRIG1 output This bit must be set to 1 in order for a pulse to be generated on the TRIG1 output when the RTC value reaches the time set in the TT1L and TT1M registers.

Bit 10 – TT0_EN 0: Disable TRIG0 output 1: Enable TRIG0 output This bit must be set to 1 in order for a pulse to be generated on the TRIG0 output when the RTC value reaches the time set in the TT0L and TT0M registers.

Bit 4 – PTP_UNICAST_EN Enable detection of PTP frames which uses unicast address. User can configure Unicast IP destination address for PTP transmit and receive frames in registers PTP_TX_UNICAST_ADDR and PTP_RX_UNICAST_ADDR respectively

Bit 3 – REQ_EN 0: Core is operating in responder mode 1: Core is operating in requestor mode

Bit 1 – ONE_STEP_SYNC One Step Sync Mode. Write 1 to enable. When set to 1, core replace timestamp field in the 1588 header for TX Sync Frames with current RTC value and updates the FCS.

Bit 0 – ENCOR 0: Disable core 1: Enable core

6.2. IER (Ask a Question)

Name: IER
Offset: 0x004
Reset: 0x0
Property: Read/Write

Interrupt enable register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		IEPEERRTSID	IEPEERTTSID	IERTSID	IETTSID	IEPTPRXPDELAYRESP	IEPTPRXPDELAYREQ	IEPTPRXDELAYRESP
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	IEPTPRXDELAYREQ	IEPTPRXSYNC	IEPTPTXPDELAYRESP	IEPTPTXPDELAYREQ	IEPTPTXDELAYRESP	IEPTPTXDELAYREQ	IEPTPTXSYNC	IERTCSEC
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IELT2	IELT1	IELT0	IETT2	IETT1	IETT0	IERTS0	IETTS0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 22 – IEPEERRTSID 0: Disable interrupt generation when sequenceID and sourcePortIdentity of PTP peer frame (PDELAY REQ or PDELAY RESP) are received at GMII RX interface 1: Enable interrupt generation when sequenceID and sourcePortIdentity of PTP peer frame (PDELAY REQ or PDELAY RESP) are received at GMII RX interface

Bit 21 – IEPEERTTSID 0: Disable interrupt generation when sequenceID of PTP peer frame (PDELAY REQ or PDELAY RESP) is transmitted at GMII TX interface 1: Enable interrupt generation when sequenceID of PTP frame is (PDELAY REQ or PDELAY RESP) is transmitted at GMII TX interface

Bit 20 – IERTSID 0: Disable interrupt generation when sequenceID and sourcePortIdentity of PTP frame (SYNC REQ, DELAY REQ or DELAY RESP) are received at GMII RX interface 1: Enable interrupt generation when sequenceID and sourcePortIdentity of PTP frame (SYNC REQ, DELAY REQ or PDELAY RESP) are received at GMII RX interface

Bit 19 – IETTSID 0: Disable interrupt generation when sequenceID of PTP frame (SYNC REQ,DELAY REQ or DELAY RESP) is transmitted at GMII TX interface 1: Enable interrupt generation when sequenceID of PTP frame is (SYNC REQ,DELAY REQ or DELAY RESP) transmitted at GMII TX interface

Bit 18 – IEPTPRXPDELAYRESP 0: Disable interrupt generation when PTP PDELAY RESPONSE frame is received at GMII RX interface 1: Enable interrupt generation when PTP PDELAY RESPONSE frame is received at GMII RX interface

Bit 17 – IEPTPRXPDELAYREQ 0: Disable interrupt generation when PTP PDELAY REQ frame is received at GMII RX interface 1: Enable interrupt generation when PTP PDELAY REQ frame is received at GMII RX interface

Bit 16 – IEPTPRXDELAYRESP 0: Disable interrupt generation when PTP DELAY RESPONSE frame is received at GMII RX interface 1: Enable interrupt generation when PTP DELAY RESPONSE frame is received at GMII RX interface

Bit 15 – IEPTPRXDELAYREQ 0: Disable interrupt generation when PTP DELAY REQ frame is received at GMII RX interface 1: Enable interrupt generation when PTP DELAY REQ frame is received at GMII RX interface

Bit 14 – IEPTPRXSYNC 0: Disable interrupt generation when PTP SYNC frame is received at GMII RX interface 1: Enable interrupt generation when PTP SYNC frame is received at GMII RX interface

Bit 13 – IEPTPTXPDELAYRESP 0: Disable interrupt generation when PTP PDELAY RESPONSE frame is transmitted at GMII TX interface 1: Enable interrupt generation when PTP PDELAY RESPONSE frame is transmitted at GMII TX interface

Bit 12 – IEPTPTXPDELAYREQ 0: Disable interrupt generation when PTP PDELAY REQ frame is transmitted at GMII TX interface 1: Enable interrupt generation when PTP PDELAY REQ frame is transmitted at GMII TX interface

Bit 11 – IEPTPTXDELAYRESP 0: Disable interrupt generation when PTP DELAY RESPONSE frame is transmitted at GMII TX interface 1: Enable interrupt generation when PTP DELAY RESPONSE frame is transmitted at GMII TX interface

Bit 10 – IEPTPTXDELAYREQ 0: Disable interrupt generation when PTP DELAY REQ frame is transmitted at GMII TX interface 1: Enable interrupt generation when PTP DELAY REQ frame is transmitted at GMII TX interface

Bit 9 – IEPTPTXSYNC 0: Disable interrupt generation when PTP SYNC frame is transmitted at GMII TX interface 1: Enable interrupt generation when PTP SYNC frame is transmitted at GMII TX interface

Bit 8 – IERTCSEC 0: Disable interrupt generation when RTC second counter increment by 1 1: Enable interrupt generation when RTC second counter increment by 1

Bit 7 – IELT2 0: Disable ILT2 Interrupt. 1: Enable ILT2 Interrupt.

Bit 6 – IELT1 0: Disable ILT1 Interrupt. 1: Enable ILT1 Interrupt.

Bit 5 – IELT0 0: Disable ILT0 Interrupt. 1: Enable ILT0 Interrupt.

Bit 4 – IETT2 0: Disable ITT2 Interrupt. 1: Enable ITT2 Interrupt.

Bit 3 – IETT1 0: Disable ITT1 Interrupt. 1: Enable ITT1 Interrupt.

Bit 2 – IETT0 0: Disable ITT0 Interrupt. 1: Enable ITT0 Interrupt.

Bit 1 – IERTS0 0: Disable IRTS0 Interrupt. 1: Enable IRTS0 Interrupt.

Bit 0 – IETTS0 0: Disable ITTS0 Interrupt. 1: Enable ITTS0 Interrupt.

6.3. MIS (Ask a Question)

Name: MIS
Offset: 0x008
Reset: 0x0
Property: Read-only

Masked interrupt status register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		IPEERRTSID	IPEERTTSID	IRTSID	ITTSID	IPTPRXPDELAYRESP	IPTPRXPDELAYREQ	IPTPRXDELAYRESP
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	IPTPRXDELAYREQ	IPTPRXSYNC	IPTPTXPDELAYRESP	IPTPTXPDELAYREQ	IPTPTXDELAYRESP	IPTPTXDELAYREQ	IPTPTXSYNC	IRTCSEC
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ILT2	ILT1	ILT0	ITT2	ITT1	ITT0	IRTS	ITTS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 22 – IPEERRTSID This bit is the logical AND of bit 22 of IER and bit 22 of RIS

Bit 21 – IPEERTTSID This bit is the logical AND of bit 21 of IER and bit 21 of RIS

Bit 20 – IRTSID This bit is the logical AND of bit 20 of IER and bit 20 of RIS

Bit 19 – ITTSID This bit is the logical AND of bit 19 of IER and bit 19 of RIS

Bit 18 – IPTPRXPDELAYRESP This bit is the logical AND of bit 18 of IER and bit 18 of RIS

Bit 17 – IPTPRXPDELAYREQ This bit is the logical AND of bit 17 of IER and bit 17 of RIS

Bit 16 – IPTPRXDELAYRESP This bit is the logical AND of bit 16 of IER and bit 16 of RIS

Bit 15 – IPTPRXDELAYREQ This bit is the logical AND of bit 15 of IER and bit 15 of RIS

Bit 14 – IPTPRXSYNC This bit is the logical AND of bit 14 of IER and bit 14 of RIS

Bit 13 – IPTPTXPDELAYRESP This bit is the logical AND of bit 13 of IER and bit 13 of RIS

Bit 12 – IPTPTXPDELAYREQ This bit is the logical AND of bit 12 of IER and bit 12 of RIS

Bit 11 – IPTPTXDELAYRESP This bit is the logical AND of bit 11 of IER and bit 11 of RIS

Bit 10 – IPTPTXDELAYREQ This bit is the logical AND of bit 10 of IER and bit 10 of RIS

Bit 9 – IPTPTXSYNC This bit is the logical AND of bit 9 of IER and bit 9 of RIS

Bit 8 – IRTCSEC This bit is the logical AND of bit 8 of IER and bit 8 of RIS

Bit 7 – ILT2 This bit is the logical AND of bit 7 of IER and bit 7 of RIS

Bit 6 – ILT1 This bit is the logical AND of bit 6 of IER and bit 6 of RIS

Bit 5 – ILT0 This bit is the logical AND of bit 5 of IER and bit 5 of RIS

Bit 4 – ITT2 This bit is the logical AND of bit 4 of IER and bit 4 of RIS

Bit 3 – ITT1 This bit is the logical AND of bit 3 of IER and bit 3 of RIS

Bit 2 – ITT0 This bit is the logical AND of bit 2 of IER and bit 2 of RIS

Bit 1 – IRTS This bit is the logical AND of bit 1 of IER and bit 1 of RIS

Bit 0 – ITTS This bit is the logical AND of bit 0 of IER and bit 0 of RIS

6.4. RIS (Ask a Question)

Name: RIS
Offset: 0x00C
Reset: 0x0
Property: Read/Write

Raw interrupt status register

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		RIPEERRTSID	RIPEERTTSID	RIRTSID	RITTSID	RIPTPRXPDELAYRESP	RIPTPRXPDELAYREQ	RIPTPRXDELAYRESP
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RIPTPRXDELAYREQ	RIPTPRXSYNC	RIPTPTXPDELAYRESP	RIPTPTXPDELAYREQ	RIPTPTXDELAYRESP	RIPTPTXDELAYREQ	RIPTPTXSYNC	RIRTCSEC
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RILT2	RILT1	RILT0	RITT2	RITT1	RITT0	RIRTS	RITTS
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 22 – RIPEERRTSID When this bit has a value of 1 it indicates that a sequenceID and sourcePortIdentity of PTP peer frame (PDELAY REQ or PDELAY RESP) are received at GMII RX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 21 – RIPEERTTSID When this bit has a value of 1 it indicates that a sequenceID of PTP peer frame (PDELAY REQ or PDELAY RESP) is transmitted at GMII RX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 20 – RIRTSID When this bit has a value of 1 it indicates that a sequenceID and sourcePortIdentity of PTP frame (SYNC REQ, DELAY REQ or DELAY RESP) are received at GMII RX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 19 – RITTSID When this bit has a value of 1 it indicates that a sequenceID of PTP frame (SYNC REQ, DELAY REQ or DELAY RESP) is transmitted at GMII RX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 18 – RIPTPRXPDELAYRESP When this bit has a value of 1 it indicates that a PTP PDELAY RESPONSE frame is received at GMII RX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 17 – RIPTPRXPDELAYREQ When this bit has a value of 1 it indicates that a PTP PDLAY REQUEST is received at GMII RX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 16 – RIPTPRXDELAYRESP When this bit has a value of 1 it indicates that a PTP DELAY RESPONSE frame is received at GMII RX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 15 – RIPTPRXDELAYREQ When this bit has a value of 1 it indicates that a PTP DELAY REQUEST frame is received at GMII RX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 14 – RIPTPRXSYNC When this bit has a value of 1 it indicates that a PTP SYNC frame is received at GMII RX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 13 – RIPTPTXPDELAYRESP When this bit has a value of 1 it indicates that a PTP PDELAY RESPONSE frame is transmitted at GMII TX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 12 – RIPTPTXPDELAYREQ When this bit has a value of 1 it indicates that a PTP PDELAY REQUEST frame is transmitted at GMII TX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 11 – RIPTPTXDELAYRESP When this bit has a value of 1 it indicates that a PTP DELAY RESPONSE frame is transmitted at GMII TX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 10 – RIPTPTXDELAYREQ When this bit has a value of 1 it indicates that a PTP DELAY REQUEST frame is transmitted at GMII TX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 9 – RIPTPTXSYNC When this bit has a value of 1 it indicates that a PTP SYNC frame is transmitted at GMII TX interface This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 8 – RIRTCSEC When this bit has a value of 1 it indicates that a RTC second counter is incremented by 1 This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 7 – RILT2 When this bit has a value of 1 it indicates that a rising edge has been observed on the LATCH2 input since this bit was last 0. This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 6 – RILT1 When this bit has a value of 1 it indicates that a rising edge has been observed on the LATCH1 input since this bit was last 0. This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 5 – RILT0 When this bit has a value of 1 it indicates that a rising edge has been observed on the LATCH0 input since this bit was last 0. This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 4 – RITT2 When this bit has a value of 1 it indicates that the time set in the trigger 2 registers (TT2L, TT2M and TT2MSBSEC) has been reached since this bit was last 0. This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 3 – RITT1 When this bit has a value of 1 it indicates that the time set in the trigger 1 registers (TT1L, TT1M and TT1MSBSEC) has been reached since this bit was last 0. This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 2 – RITT0 When this bit has a value of 1 it indicates that the time set in the trigger 0 registers (TT0L, TT0M and TT0MSBSEC) has been reached since this bit was last 0. This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 1 – RIRTS When this bit has a value of 1 it indicates that, since this bit was last 0, receipt of an IEEE 1588 frame has been detected and that the receive timestamp registers (RTSL, RTSM and RTSMSBSECSUBNS or PEERRTSL, PEERRTSM and PEERRTSMSBSECSUBNS) have been updated. This bit is cleared by writing 1 to it. Writing 0 has no effect.

Bit 0 – RITTS When this bit has a value of 1 it indicates that, since this bit was last 0, transmission of an IEEE 1588 frame has been detected and that the transmit timestamp registers (TTSL, TTSM and TTSMSBSECSUBNS or PEERTTSL, PEERTTSM and PEERTTSMSBSECSUBNS) have been updated. This bit is cleared by writing 1 to it. Writing 0 has no effect.

6.5. TTSL (Ask a Question)

Name: TTSL
Offset: 0x010
Reset: 0x0
Property: Read-only

PTP frame transmitted timestamp nanoseconds register

Bit	31	30	29	28	27	26	25	24
	PTP_TX_NSEC[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_TX_NSEC[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_TX_NSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_TX_NSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_TX_NSEC[31:0] PTP frame transmitted timestamp nanoseconds. The register is updated with the nanosecond count of RTC when SFD of a PTP transmit frame is detected at GMII interface. An interrupt is issued when the register is updated.

6.6. TTSM (Ask a Question)

Name: TTSM
Offset: 0x014
Reset: 0x0
Property: Read-only

Note: PTP frame transmitted timestamp seconds register [31:0].TTSMSBSECSUBNS register contains upper 16 bits [47:32] of seconds

Bit	31	30	29	28	27	26	25	24
	PTP_TX_SEC_LSB_32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_TX_SEC_LSB_32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_TX_SEC_LSB_32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_TX_SEC_LSB_32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_TX_SEC_LSB_32BITS[31:0] PTP frame transmitted timestamp seconds [31:0]. The register is updated with the lower 32 bits [31:0] of second count of RTC when SFD of a PTP transmit frame is detected at GMII interface. An interrupt is issued when the register is updated.

6.7. TTSID (Ask a Question)

Name: TTSID
Offset: 0x018
Reset: 0x0
Property: Read-only

PTP frame transmitted identification register. Contains the 16-bit sequence ID

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PTP_TX_SEQ_ID[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_TX_SEQ_ID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTP_TX_SEQ_ID[15:0] Contains the 16 bits sequenceID from the message header of the transmitted ptp frame associated with the current transmitted timestamp (in the TTSL, TTSM and TTSMSBSECSUBNS registers)

6.8. RTSL (Ask a Question)

Name: RTSL
Offset: 0x01C
Reset: 0x0
Property: Read-only

PTP frame received timestamp nanoseconds register

Bit	31	30	29	28	27	26	25	24
	PTP_RX_NSEC[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_RX_NSEC[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_RX_NSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_RX_NSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_RX_NSEC[31:0] PTP frame received timestamp nanoseconds. The register is updated with the nanosecond count of RTC when SFD of a PTP frame is received at GMII interface. An interrupt is issued when the register is updated.

6.9. RTSM (Ask a Question)

Name: RTSM
Offset: 0x020
Reset: 0x0
Property: Read-only

Note: PTP frame received timestamp seconds register [31:0].RTSMSBSECSUBNS register contains upper 16 bits [47:32] of seconds

Bit	31	30	29	28	27	26	25	24
	PTP_RX_SEC_LSB_32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_RX_SEC_LSB_32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_RX_SEC_LSB_32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_RX_SEC_LSB_32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_RX_SEC_LSB_32BITS[31:0] PTP frame received timestamp seconds [31:0]. The register is updated with the lower 32 bits [31:0] of second count of RTC when SFD of a PTP frame is received at GMII interface. An interrupt is issued when the register is updated.

6.10. RTSID2 (Ask a Question)

Name: RTSID2
Offset: 0x024
Reset: 0x0
Property: Read-only

PTP frame received identification register2. Contains the 16-bit sequence ID and the bits [79:64] of the sourcePortIdentity

Bit	31	30	29	28	27	26	25	24
	PTP_RX_SEQ_ID[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_RX_SEQ_ID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_RX_SRC_PORTID_UPPER_16BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_RX_SRC_PORTID_UPPER_16BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PTP_RX_SEQ_ID[15:0] Contains the 16 bits sequenceID from the message header of the ptp frame associated with the current receive timestamp (in the RTSL, RTSM and RTSMSBSECSUBNS egisters)

Bits 15:0 – PTP_RX_SRC_PORTID_UPPER_16BITS[15:0] Contains the upper 16 bits [79:64] of sourcePortIdentity from the message header of the received ptp frame associated with the current receive timestamp (in the RTSL, RTSM and RTSMSBSEC registers)

6.11. RTSID1 (Ask a Question)

Name: RTSID1
Offset: 0x028
Reset: 0x0
Property: Read-only

PTP frame received identification register1. Contains bits [63:32] of the sourcePortIdentity

Bit	31	30	29	28	27	26	25	24
	PTP_RX_SRC_PORTID_MID_32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_RX_SRC_PORTID_MID_32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_RX_SRC_PORTID_MID_32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_RX_SRC_PORTID_MID_32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_RX_SRC_PORTID_MID_32BITS[31:0] Contains the bits [63:32] of sourcePortIdentity from the message header of the received ptp frame associated with the current receive timestamp (in the RTSL, RTSM and RTSMSBSECSUBNS registers)

6.12. RTSID0 (Ask a Question)

Name: RTSID0
Offset: 0x02C
Reset: 0x0
Property: Read-only

PTP frame received identification register0. Contains bits [31:0] of the sourcePortIdentity

Bit	31	30	29	28	27	26	25	24
	PTP_RX_SRC_PORTID_LOWER_32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_RX_SRC_PORTID_LOWER_32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_RX_SRC_PORTID_LOWER_32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_RX_SRC_PORTID_LOWER_32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_RX_SRC_PORTID_LOWER_32BITS[31:0] Contains the bits [31:0] of sourcePortIdentity from the message header of the received ptp frame associated with the current receive timestamp (in the RTSL, RTSM and RTSMSBSECSUBNS registers)

6.13. RTCL (Ask a Question)

Name: RTCL
Offset: 0x030
Reset: 0x0
Property: Read/Write

Internal RTC nanoseconds register.When writing to the internal RTC, the RTCL register should be written first followed by a write to the RTCM and RTCMSBSEC registers.When reading the internal RTC value, the RTCL register should always be read first followed by a read of the RTCM and RTCMSBSEC registers.

Bit	31	30	29	28	27	26	25	24
			RTC_NSEC[29:24]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RTC_NSEC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RTC_NSEC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RTC_NSEC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 29:0 – RTC_NSEC[29:0] Internal RTC nanosecond count. When writing to the internal RTC, RTCL should be written first followed by write to the RTCM and RTCMSBSEC registers. This register can be adjusted by writing to the ADJUST register or RTCCTRL register. Its increment factor can be changed by writing to the RTCINCR register When reading to the internal RTC value, the RTCL register should always be read first followed by a read of the RTCM and RTCMSBSEC registers

6.14. RTCM (Ask a Question)

Name: RTCM
Offset: 0x034
Reset: 0x0
Property: Read/Write

Note: Internal RTC seconds register [31:0]. RTCMSBSEC register contains upper 16 bits [47:32] of seconds

Bit	31	30	29	28	27	26	25	24
	RTC_SEC_LSB_32BITS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RTC_SEC_LSB_32BITS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RTC_SEC_LSB_32BITS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RTC_SEC_LSB_32BITS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RTC_SEC_LSB_32BITS[31:0] Least significant 32 bits of internal RTC seconds count. When writing to the internal RTC, RTCL should be written first followed by write to the RTCM and RTCMSBSEC registers. This register can be incremented/decremented by writing to the RTCCTRL register. When reading to the internal RTC value, the RTCL register should always be read first followed by a read of the RTCM and RTCMSBSEC registers

6.15. ADJUST (Ask a Question)

Name: ADJUST
Offset: 0x038
Reset: 0xA0000000
Property: Read/Write

Internal RTC adjustment control register.This control register can be used to adjust the speed of the internal RTC. See the detailed description of this register.

Bit	31	30	29	28	27	26	25	24
	ADJVAL[4:0]					ADJEN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	1	0	1	0	0	0		

Bit	23	22	21	20	19	18	17	16
	ADJCM[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADJCM[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADJCM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:27 – ADJVAL[4:0] This five-bit field holds the amount to be added to Internal RTC least significant word (nanoseconds count) each time the adjustment counter returns to zero (and the ADJEN bit is set to 1). The internal RTC operates in the PTP_CLK clock domain and the nanoseconds count normally increments by the period of PTP_CLK clock on each rising edge of PTP_CLK. When the conditions described above are met, the internal RTC will be incremented by the value stored in ADJVAL, instead of by the normal amount of PTP_CLK clock period The value stored in ADJVAL can range from 0 to 31. Using adjustment with an ADJVAL value less than PTP_CLK clock period will result in a slowing down of the internal RTC. Similarly, using adjustment with an ADJVAL greater than PTP_CLK clock period will cause the internal RTC to speed up. The amount of slowing down or speeding up is a function of both the ADJVAL value and the ADJCM value

Bit 26 – ADJEN 0: Adjustment feature is disabled 1: Adjustment feature is enabled

Bits 23:0 – ADJCM[23:0] Adjustment counter maximum value. This field sets the rollover value for a 24-bit adjustment counter clocked by PTP_CLK clock. The adjustment counter is essentially a free running counter that increments by 1 on each rising edge of PTP_CLK. When the counter value reaches the ADJCM value it returns to zero and, if the ADJEN bit is set, the internal RTC nanoseconds count is incremented by the ADJVAL instead of by the normal amount of PTP_CLK clock period. The ADJCM field essentially controls how frequently the ADJVAL is used as the internal RTC increment.

6.16. TT0L (Ask a Question)

Name: TT0L
Offset: 0x040
Reset: 0x0
Property: Read/Write

Time trigger 0 nanoseconds register.When TRIG_NUM is greater than 0 and the TT0L, TT0M and TT0MSBSEC registers match the RTC value a pulse is generated on theTRIG0 output

Bit	31	30	29	28	27	26	25	24
	TT0_NSEC[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TT0_NSEC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TT0_NSEC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TT0_NSEC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TT0_NSEC[31:0] Time trigger 0 nanoseconds count This register is only relevant if the core has been configured to support 1 or more trigger outputs (TRIG_NUM parameter set to 1 or greater). When the RTC value reaches the time set in the TT0L, TT0M and TT0MSBSEC registers, the RITT0 bit of the RIS register will be set to 1 (or will remain at 1 if it is already 1). An interrupt can be generated on the time match (depending on the value of the IETT0 bit of the IER) and/or a pulse can be generated on the TRIG0 output (depending on the value of the TT0_EN bit of the GCFG register).

6.17. TT0M (Ask a Question)

Name: TT0M
Offset: 0x044
Reset: 0x0
Property: Read/Write

Note: Time trigger 0 seconds register [31:0].When TRIG_NUM is greater than 0 and the TT0L, TT0M and TT0MSBSEC registers match the RTC value a pulse is generated on the TRIG0 output.TT0MSBSEC register contains upper 16 bits [47:32] of seconds

Bit	31	30	29	28	27	26	25	24
	TT0_SEC_LSB_32BITS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TT0_SEC_LSB_32BITS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TT0_SEC_LSB_32BITS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TT0_SEC_LSB_32BITS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TT0_SEC_LSB_32BITS[31:0] Time trigger 0 least significant 32 bits of seconds count. This register is only relevant if the core has been configured to support 1 or more trigger outputs (TRIG_NUM parameter set to 1 or greater). When the RTC value reaches the time set in the TT0L, TT0M and TT0MSBSEC registers, the RITT0 bit of the RIS register will be set to 1 (or will remain at 1 if it is already 1). An interrupt can be generated on the time match (depending on the value of the IETT0 bit of the IER) and/or a pulse can be generated on the TRIG0 output (depending on the value of the TT0_EN bit of the GCFG register).

6.18. TT1L (Ask a Question)

Name: TT1L
Offset: 0x048
Reset: 0x0
Property: Read/Write

Time trigger 1 nanoseconds register.When TRIG_NUM is greater than 1 and the TT1L, TT1M and TT1MSBSEC registers match the RTC value a pulse is generated on the TRIG1 output

Bit	31	30	29	28	27	26	25	24
	TT1_NSEC[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TT1_NSEC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TT1_NSEC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TT1_NSEC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TT1_NSEC[31:0] Time trigger 1 nanoseconds count This register is only relevant if the core has been configured to support 2 or more trigger outputs (TRIG_NUM parameter set to 2 or greater). When the RTC value reaches the time set in the TT1L, TT1M and TT1MSBSEC registers, the RITT1 bit of the RIS register will be set to 1 (or will remain at 1 if it is already 1). An interrupt can be generated on the time match (depending on the value of the IETT1 bit of the IER) and/or a pulse can be generated on the TRIG1 output (depending on the value of the TT1_EN bit of the GCFG register).

6.19. TT1M (Ask a Question)

Name: TT1M
Offset: 0x04C
Reset: 0x0
Property: Read/Write

Note: Time trigger 1 seconds register [31:0].When TRIG_NUM is greater than 1 and the TT1L, TT1M and TT1MSBSEC registers match the RTC value a pulse is generated on the TRIG1 output. TT1MSBSEC register contains upper 16 bits [47:32] of seconds

Bit	31	30	29	28	27	26	25	24
	TT1_SEC_LSB_32BITS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TT1_SEC_LSB_32BITS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TT1_SEC_LSB_32BITS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TT1_SEC_LSB_32BITS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TT1_SEC_LSB_32BITS[31:0] Time trigger 1 least significant 32 bits of seconds count. This register is only relevant if the core has been configured to support 2 or more trigger outputs (TRIG_NUM parameter set to 2 or greater). When the RTC value reaches the time set in the TT1L, TT1M and TT1MSBSEC registers, the RITT1 bit of the RIS register will be set to 1 (or will remain at 1 if it is already 1). An interrupt can be generated on the time match (depending on the value of the IETT1 bit of the IER) and/or a pulse can be generated on the TRIG1 output (depending on the value of the TT1_EN bit of the GCFG register).

6.20. TT2L (Ask a Question)

Name: TT2L
Offset: 0x050
Reset: 0x0
Property: Read/Write

Time trigger 2 nanoseconds register.When TRIG_NUM is greater than 2 and the TT2L, TT2M and TT2MSBSEC registers match the RTC value a pulse is generated on the TRIG2 output

Bit	31	30	29	28	27	26	25	24
	TT2_NSEC[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TT2_NSEC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TT2_NSEC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TT2_NSEC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TT2_NSEC[31:0] Time trigger 2 nanoseconds count This register is only relevant if the core has been configured to support 3 trigger outputs (TRIG_NUM parameter set to 3). When the RTC value reaches the time set in the TT2L, TT2M and TT2MSBSEC registers, the RITT2 bit of the RIS register will be set to 1 (or will remain at 1 if it is already 1). An interrupt can be generated on the time match (depending on the value of the IETT2 bit of the IER) and/or a pulse can be generated on the TRIG2 output (depending on the value of the TT2_EN bit of the GCFG register).

6.21. TT2M (Ask a Question)

Name: TT2M
Offset: 0x054
Reset: 0x0
Property: Read/Write

Note: Time trigger 2 seconds register [31:0].When TRIG_NUM is greater than 2 and the TT2L, TT2M and TT2MSBSEC registers match the RTC value a pulse is generated on the TRIG2 output.TT2MSBSEC register contains upper 16 bits [47:32] of seconds

Bit	31	30	29	28	27	26	25	24
	TT2_SEC_LSB_32BITS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TT2_SEC_LSB_32BITS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TT2_SEC_LSB_32BITS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TT2_SEC_LSB_32BITS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TT2_SEC_LSB_32BITS[31:0] Time trigger 2 least significant 32 bits of seconds count. This register is only relevant if the core has been configured to support 3 trigger outputs (TRIG_NUM parameter set to 3). When the RTC value reaches the time set in the TT2L, TT2M and TT2MSBSEC registers, the RITT2 bit of the RIS register will be set to 1 (or will remain at 1 if it is already 1). An interrupt can be generated on the time match (depending on the value of the IETT2 bit of the IER) and/or a pulse can be generated on the TRIG2 output (depending on the value of the TT2_EN bit of the GCFG register).

6.22. LT0L (Ask a Question)

Name: LT0L
Offset: 0x058
Reset: 0x0
Property: Read-only

Latch 0 nanoseconds register.When LATCH_NUM is greater than 0 and a rising edge is detected on the LATCH0 input, nanoseconds count of RTC will be stored in LT0L

Bit	31	30	29	28	27	26	25	24
	LT0_NSEC[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	LT0_NSEC[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	LT0_NSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LT0_NSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – LT0_NSEC[31:0] Latch 0 nanoseconds count This register is only relevant if the core has been configured to support 1 or more latch inputs (LATCH_NUM parameter set to 1 or greater). When a rising edge is detected on the LATCH0 input, the value in the RTCL register will be stored in this register if the LT0_EN bit of the GCFG register is set to 1. This register will hold its current value if the LT0_EN bit of the GCFG register is 0. The detection of a rising edge on the LATCH0 input will also cause the RILT0 bit of the RIS register to be set to 1 (if it is not already set to 1). This can in turn cause assertion of the INT interrupt output if the IELT0 bit of the IER is set to 1.

6.23. LT0M (Ask a Question)

Name: LT0M
Offset: 0x05C
Reset: 0x0
Property: Read-only

Latch 0 seconds register [31:0].When LATCH_NUM is greater than 0 and a rising edge is detected on the LATCH0 input, lower 32 bits [31:0] of seconds count of RTC will be stored in LT0M

Bit	31	30	29	28	27	26	25	24
	LT0_SEC_LSB_32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	LT0_SEC_LSB_32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	LT0_SEC_LSB_32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LT0_SEC_LSB_32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – LT0_SEC_LSB_32BITS[31:0] Latch 0 least significant 32 bits of seconds count. This register is only relevant if the core has been configured to support 1 or more latch inputs (LATCH_NUM parameter set to 1 or greater). When a rising edge is detected on the LATCH0 input, the value in the RTCM register will be stored in this register if the LT0_EN bit of the GCFG register is set to 1. This register will hold its current value if the LT0_EN bit of the GCFG register is 0. The detection of a rising edge on the LATCH0 input will also cause the RILT0 bit of the RIS register to be set to 1 (if it is not already set to 1). This can in turn cause assertion of the INT interrupt output if the IELT0 bit of the IER is set to 1.

6.24. LT1L (Ask a Question)

Name: LT1L
Offset: 0x060
Reset: 0x0
Property: Read-only

Latch 1 nanoseconds register.When LATCH_NUM is greater than 1 and a rising edge is detected on the LATCH1 input, nanoseconds count of RTC will be stored in LT1L

Bit	31	30	29	28	27	26	25	24
	LT1_NSEC[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	LT1_NSEC[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	LT1_NSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LT1_NSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – LT1_NSEC[31:0] Latch 1 nanoseconds count This register is only relevant if the core has been configured to support 2 or more latch inputs (LATCH_NUM parameter set to 2 or greater). When a rising edge is detected on the LATCH1 input, the value in the RTCL register will be stored in this register if the LT1_EN bit of the GCFG register is set to 1. This register will hold its current value if the LT1_EN bit of the GCFG register is 0. The detection of a rising edge on the LATCH1 input will also cause the RILT1 bit of the RIS register to be set to 1 (if it is not already set to 1). This can in turn cause assertion of the INT interrupt output if the IELT1 bit of the IER is set to 1.

6.25. LT1M (Ask a Question)

Name: LT1M
Offset: 0x064
Reset: 0x0
Property: Read-only

Latch 1 seconds register [31:0].When LATCH_NUM is greater than 1 and a rising edge is detected on the LATCH1 input, lower 32 bits [31:0] of seconds count of RTC will be stored in LT1M

Bit	31	30	29	28	27	26	25	24
	LT1_SEC_LSB_32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	LT1_SEC_LSB_32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	LT1_SEC_LSB_32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LT1_SEC_LSB_32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – LT1_SEC_LSB_32BITS[31:0] Latch 1 least significant 32 bits of seconds count. This register is only relevant if the core has been configured to support 2 or more latch inputs (LATCH_NUM parameter set to 2 or greater). When a rising edge is detected on the LATCH1 input, the value in the RTCM register will be stored in this register if the LT1_EN bit of the GCFG register is set to 1. This register will hold its current value if the LT1_EN bit of the GCFG register is 0. The detection of a rising edge on the LATCH1 input will also cause the RILT1 bit of the RIS register to be set to 1 (if it is not already set to 1). This can in turn cause assertion of the INT interrupt output if the IELT1 bit of the IER is set to 1.

6.26. LT2L (Ask a Question)

Name: LT2L
Offset: 0x068
Reset: 0x0
Property: Read-only

Latch 2 nanoseconds register.When LATCH_NUM is greater than 2 and a rising edge is detected on the LATCH2 input, nanoseconds count of RTC will be stored in LT2L

Bit	31	30	29	28	27	26	25	24
	LT2_NSEC[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	LT2_NSEC[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	LT2_NSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LT2_NSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – LT2_NSEC[31:0] Latch 2 nanoseconds count This register is only relevant if the core has been configured to support 3 latch inputs (LATCH_NUM parameter set to 3). When a rising edge is detected on the LATCH2 input, the value in the RTCL register will be stored in this register if the LT2_EN bit of the GCFG register is set to 1. This register will hold its current value if the LT2_EN bit of the GCFG register is 0. The detection of a rising edge on the LATCH2 input will also cause the RILT2 bit of the RIS register to be set to 1 (if it is not already set to 1). This can in turn cause assertion of the INT interrupt output if the IELT2 bit of the IER is set to 1.

6.27. LT2M (Ask a Question)

Name: LT2M
Offset: 0x06C
Reset: 0x0
Property: Read-only

Latch 2 lower seconds register [31:0].When LATCH_NUM is greater than 2 and a rising edge is detected on the LATCH2 input, lower 32bits [31:0] of seconds count of RTC will be stored in LT2M

Bit	31	30	29	28	27	26	25	24
	LT2_SEC_LSB_32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	LT2_SEC_LSB_32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	LT2_SEC_LSB_32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LT2_SEC_LSB_32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – LT2_SEC_LSB_32BITS[31:0] Latch 2 least significant 32 bits of seconds count. This register is only relevant if the core has been configured to support 3 latch inputs (LATCH_NUM parameter set to 3). When a rising edge is detected on the LATCH2 input, the value in the RTCM register will be stored in this register if the LT2_EN bit of the GCFG register is set to 1. This register will hold its current value if the LT2_EN bit of the GCFG register is 0. The detection of a rising edge on the LATCH2 input will also cause the RILT2 bit of the RIS register to be set to 1 (if it is not already set to 1). This can in turn cause assertion of the INT interrupt output if the IELT2 bit of the IER is set to 1.

6.28. TTSMSBSECSUBNS (Ask a Question)

Name: TTSMSBSECSUBNS
Offset: 0x070
Reset: 0x0
Property: Read-only

PTP frame transmitted timestamp seconds [47:32] and sub-nanoseconds register

Bit	31	30	29	28	27	26	25	24
	PTP_TX_SUBNSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_TX_SUBNSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_TX_SEC_MSB_16BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_TX_SEC_MSB_16BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PTP_TX_SUBNSEC[15:0] PTP frame transmitted timestamp sub-nanosecond most significant 16 bits. These bits are updated with the upper 16 bits [23:8] of sub-nanosecond count of RTC when SFD of a PTP frame is transmitted at GMII interface. For transparent clock, residence time needs to be updated in correctionField which uses lower 16 bits for sub-nanosecond. For transparent and two step clock while transmitting PTP message, sub-nanosecond of egress PTP message should be used in updating correctionField

Bits 15:0 – PTP_TX_SEC_MSB_16BITS[15:0] PTP frame transmitted timestamp most significant 16 bits [47:32] of seconds count. These bits are updated with the upper 16 bits [47:32] of second count of RTC when SFD of a PTP transmit frame is detected at GMII interface..

6.29. RTSMSBSECSUBNS (Ask a Question)

Name: RTSMSBSECSUBNS
Offset: 0x074
Reset: 0x0
Property: Read-only

PTP frame received timestamp seconds [47:32] and sub-nanoseconds register

Bit	31	30	29	28	27	26	25	24
	PTP_RX_SUBNSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_RX_SUBNSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_RX_SEC_MSB_16BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_RX_SEC_MSB_16BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PTP_RX_SUBNSEC[15:0] PTP frame received timestamp sub-nanosecond most significant 16 bits. This field is updated with the upper 16 bits [23:8] of sub-nanosecond count of RTC when SFD of a PTP frame is received at GMII interface. For transparent clock, residence time needs to be updated in correctionField which uses lower 16 bits for sub-nanosecond. For transparent clock while transmitting PTP message, sub-nanosecond of ingress PTP message should be written into upper 16 bits of INGRSTSMSBSECSUBNS register.

Bits 15:0 – PTP_RX_SEC_MSB_16BITS[15:0] PTP frame received timestamp most significant 16 bits [47:32] of seconds count. These bits are updated with the upper 16 bits [47:32] of second count of RTC when SFD of a PTP frame is received at GMII interface.

6.30. RTCMSBSEC (Ask a Question)

Name: RTCMSBSEC
Offset: 0x078
Reset: 0x0
Property: Read/Write

Internal RTC seconds register [47:32]

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RTC_SEC_MSB_16BITS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RTC_SEC_MSB_16BITS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RTC_SEC_MSB_16BITS[15:0] Most significant 16 bits [47:32] of internal RTC seconds count. When writing to the internal RTC, RTCL should be written first followed by write to the RTCM and RTCMSBSEC registers. This register can be incremented/decremented by writing to the RTCCTRL register. When reading to the internal RTC value, the RTCL register should always be read first followed by a read of the RTCM and RTCMSBSEC registers

6.31. TT0MSBSEC (Ask a Question)

Name: TT0MSBSEC
Offset: 0x07C
Reset: 0x0
Property: Read/Write

Time trigger 0 seconds register [47:32].When TRIG_NUM is greater than 0 and the TT0L, TT0M and TT0MSBSEC registers match the RTC value a pulse is generated on the TRIG0 output

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TT0_SEC_MSB_16BITS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TT0_SEC_MSB_16BITS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TT0_SEC_MSB_16BITS[15:0] Time trigger 0 most significant 16 bits [47:32] of seconds count. This register is only relevant if the core has been configured to support 1 or more trigger outputs (TRIG_NUM parameter set to 1 or greater). When the RTC value reaches the time set in the TT0L, TT0M and TT0MSBSEC registers, the RITT0 bit of the RIS register will be set to 1 (or will remain at 1 if it is already 1). An interrupt can be generated on the time match (depending on the value of the IETT0 bit of the IER) and/or a pulse can be generated on the TRIG0 output (depending on the value of the TT0_EN bit of the GCFG register).

6.32. TT1MSBSEC (Ask a Question)

Name: TT1MSBSEC
Offset: 0x080
Reset: 0x0
Property: Read/Write

Time trigger 1 seconds register [47:32].When TRIG_NUM is greater than 1 and the TT1L, TT1M and TT1MSBSEC registers match the RTC value a pulse is generated on the TRIG1 output

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TT1_SEC_MSB_16BITS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TT1_SEC_MSB_16BITS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TT1_SEC_MSB_16BITS[15:0] Time trigger 1 most significant 16 bits [47:32] of seconds count. This register is only relevant if the core has been configured to support 2 or more trigger outputs (TRIG_NUM parameter set to 2 or greater). When the RTC value reaches the time set in the TT1L, TT1M and TT1MSBSEC registers, the RITT1 bit of the RIS register will be set to 1 (or will remain at 1 if it is already 1). An interrupt can be generated on the time match (depending on the value of the IETT1 bit of the IER) and/or a pulse can be generated on the TRIG1 output (depending on the value of the TT1_EN bit of the GCFG register).

6.33. TT2MSBSEC (Ask a Question)

Name: TT2MSBSEC
Offset: 0x084
Reset: 0x0
Property: Read/Write

Time trigger 2 seconds register [47:32].When TRIG_NUM is greater than 2 and the TT2L, TT2M and TT2MSBSEC registers match the RTC value a pulse is generated on the TRIG2 output

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TT2_SEC_MSB_16BITS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TT2_SEC_MSB_16BITS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TT2_SEC_MSB_16BITS[15:0] Time trigger 2 most significant 16 bits [47:32] of seconds count. This register is only relevant if the core has been configured to support 3 trigger outputs (TRIG_NUM parameter set to 3). When the RTC value reaches the time set in the TT2L, TT2M and TT2MSBSEC registers, the RITT2 bit of the RIS register will be set to 1 (or will remain at 1 if it is already 1). An interrupt can be generated on the time match (depending on the value of the IETT2 bit of the IER) and/or a pulse can be generated on the TRIG2 output (depending on the value of the TT2_EN bit of the GCFG register).

6.34. LT0MSBSEC (Ask a Question)

Name: LT0MSBSEC
Offset: 0x088
Reset: 0x0
Property: Read-only

Latch 0 seconds register [47:32].When LATCH_NUM is greater than 0 and a rising edge is detected on the LATCH0 input, upper 16 bits [47:32] of seconds count of RTC will be stored in LT0MSBSEC

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	LT0_SEC_MSB_16BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LT0_SEC_MSB_16BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LT0_SEC_MSB_16BITS[15:0] Latch 0 most significant 16 bits of seconds count. This register is only relevant if the core has been configured to support 1 or more latch inputs (LATCH_NUM parameter set to 1 or greater). When a rising edge is detected on the LATCH0 input, the value in the RTCMSBSEC register will be stored in this register if the LT0_EN bit of the GCFG register is set to 1. This register will hold its current value if the LT0_EN bit of the GCFG register is 0. The detection of a rising edge on the LATCH0 input will also cause the RILT0 bit of the RIS register to be set to 1 (if it is not already set to 1). This can in turn cause assertion of the INT interrupt output if the IELT0 bit of the IER is set to 1.

6.35. LT1MSBSEC (Ask a Question)

Name: LT1MSBSEC
Offset: 0x08C
Reset: 0x0
Property: Read-only

Latch 1 seconds register [47:32].When LATCH_NUM is greater than 1 and a rising edge is detected on the LATCH1 input, upper 16 bits [47:32] of seconds count of RTC will be stored in LT1MSBSEC

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	LT1_SEC_MSB_16BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LT1_SEC_MSB_16BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LT1_SEC_MSB_16BITS[15:0] Latch 1 most significant 16 bits of seconds count. This register is only relevant if the core has been configured to support 2 or more latch inputs (LATCH_NUM parameter set to 2 or greater). When a rising edge is detected on the LATCH1 input, the value in the RTCMSBSEC register will be stored in this register if the LT1_EN bit of the GCFG register is set to 1. This register will hold its current value if the LT1_EN bit of the GCFG register is 0. The detection of a rising edge on the LATCH1 input will also cause the RILT1 bit of the RIS register to be set to 1 (if it is not already set to 1). This can in turn cause assertion of the INT interrupt output if the IELT1 bit of the IER is set to 1.

6.36. LT2MSBSEC (Ask a Question)

Name: LT2MSBSEC
Offset: 0x090
Reset: 0x0
Property: Read-only

Latch 2 seconds register [47:32].When LATCH_NUM is greater than 2 and a rising edge is detected on the LATCH2 input, upper 16 bits [47:32] of seconds count of RTC will be stored in LT2MSBSEC

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	LT2_SEC_MSB_16BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LT2_SEC_MSB_16BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LT2_SEC_MSB_16BITS[15:0] Latch 2 most significant 16 bits of seconds count. This register is only relevant if the core has been configured to support 3 latch inputs (LATCH_NUM parameter set to 3). When a rising edge is detected on the LATCH2 input, the value in the RTCMSBSEC register will be stored in this register if the LT2_EN bit of the GCFG register is set to 1. This register will hold its current value if the LT2_EN bit of the GCFG register is 0. The detection of a rising edge on the LATCH2 input will also cause the RILT2 bit of the RIS register to be set to 1 (if it is not already set to 1). This can in turn cause assertion of the INT interrupt output if the IELT2 bit of the IER is set to 1.

6.37. RTCCTRL (Ask a Question)

Name: RTCCTRL
Offset: 0x094
Reset: 0x0
Property: Write-only

Internal RTC control register

Bit	31	30	29	28	27	26	25	24
	ADD_SUBTRACT		ADJ_VALUE[29:24]					
Access	W		W	W	W	W	W	W
Reset	0		0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADJ_VALUE[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADJ_VALUE[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADJ_VALUE[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit 31 – ADD_SUBTRACT 0: Adds adj_value to internal RTC 1: Subtracts adj_value from internal RTC

Bits 29:0 – ADJ_VALUE[29:0] Internal RTC adjust value. The number of nanoseconds to increment or decrement the internal RTC nanoseconds counter. If necessary the internal RTC seconds counter will be incremented or decremented

6.38. RTCINCR (Ask a Question)

Name: RTCINCR
Offset: 0x098
Reset: 0x0
Property: Write-only

Internal RTC Nanoseconds/Sub nanoseconds Count Increment Register

Bit	31	30	29	28	27	26	25	24
	NS_INCR[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SUB_NS_INCR[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SUB_NS_INCR[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SUB_NS_INCR[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:24 – NS_INCR[7:0] Internal RTC uses upper 8 bits of the register to increment nanosecond counter.

Bits 23:0 – SUB_NS_INCR[23:0] Internal RTC uses lower 24 bits of the register to increment sub-nanosecond counter. To calculate the value to write to the sub-nanosecond register user should take the decimal value of the sub-nanosecond value, then multiply it by 2 to the power of 24 and convert the result to hexadecimal. For example, for a sub-nanosecond value of 0.5 user should write 0x800000 (0.5 * 2^24).

6.39. TXUCASTADDR0 (Ask a Question)

Name: TXUCASTADDR0
Offset: 0x09C
Reset: 0x0
Property: Write-only

Unicast destination IP address bits 31 down to 0 for PTP transmit frames.

Bit	31	30	29	28	27	26	25	24
	TX_UNICAST_IP_ADDR0[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TX_UNICAST_IP_ADDR0[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TX_UNICAST_IP_ADDR0[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TX_UNICAST_IP_ADDR0[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TX_UNICAST_IP_ADDR0[31:0] User can configure Unicast IP destination address0 for transmit PTP frames. For IPv4 frames when the address configured in this register matches with the IP destination address of transmitted PTP frames and PTP_UNICAST_EN bit in General Configuration register is set, PTP event frames will be processed. For IPv6 frames when the address configured in registers TX_UNICAST_IP_ADDR0, TX_UNICAST_IP_ADDR1, TX_UNICAST_IP_ADDR2 and TX_UNICAST_IP_ADDR3 matches with the IP destination address of transmitted PTP frames and PTP_UNICAST_EN bit in General Configuration register is set, PTP event frames will be processed

6.40. TXUCASTADDR1 (Ask a Question)

Name: TXUCASTADDR1
Offset: 0x0A0
Reset: 0x0
Property: Write-only

Unicast destination IP address bits 63 down to 3 for PTP transmit frames.

Bit	31	30	29	28	27	26	25	24
	TX_UNICAST_IP_ADDR1[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TX_UNICAST_IP_ADDR1[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TX_UNICAST_IP_ADDR1[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TX_UNICAST_IP_ADDR1[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TX_UNICAST_IP_ADDR1[31:0] User can configure Unicast IP destination address1 for transmit PTP frames. For IPv6 frames when the address configured in registers TX_UNICAST_IP_ADDR0, TX_UNICAST_IP_ADDR1, TX_UNICAST_IP_ADDR2 and TX_UNICAST_IP_ADDR3 matches with the IP destination address of transmitted PTP frames and PTP_UNICAST_EN bit in General Configuration register is set, PTP event frames will be processed. For IPv4 frames, this register is not required and it will be ignored by the Core1588

6.41. TXUCASTADDR2 (Ask a Question)

Name: TXUCASTADDR2
Offset: 0x0A4
Reset: 0x0
Property: Write-only

Unicast destination IP address bits 95 down to 64 for PTP transmit frames.

Bit	31	30	29	28	27	26	25	24
	TX_UNICAST_IP_ADDR2[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TX_UNICAST_IP_ADDR2[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TX_UNICAST_IP_ADDR2[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TX_UNICAST_IP_ADDR2[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TX_UNICAST_IP_ADDR2[31:0] User can configure Unicast IP destination address2 for transmit PTP frames. For IPv6 frames when the address configured in registers TX_UNICAST_IP_ADDR0, TX_UNICAST_IP_ADDR1, TX_UNICAST_IP_ADDR2 and TX_UNICAST_IP_ADDR3 matches with the IP destination address of transmitted PTP frames and PTP_UNICAST_EN bit in General Configuration register is set, PTP event frames will be processed. For IPv4 frames, this register is not required and it will be ignored by the Core1588

6.42. TXUCASTADDR3 (Ask a Question)

Name: TXUCASTADDR3
Offset: 0x0A8
Reset: 0x0
Property: Write-only

Unicast destination IP address bits 127 down to 96 for PTP transmit frames.

Bit	31	30	29	28	27	26	25	24
	TX_UNICAST_IP_ADDR3[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TX_UNICAST_IP_ADDR3[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TX_UNICAST_IP_ADDR3[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TX_UNICAST_IP_ADDR3[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TX_UNICAST_IP_ADDR3[31:0] User can configure Unicast IP destination address3 for transmit PTP frames. For IPv6 frames when the address configured in registers TX_UNICAST_IP_ADDR0, TX_UNICAST_IP_ADDR1, TX_UNICAST_IP_ADDR2 and TX_UNICAST_IP_ADDR3 matches with the IP destination address of transmitted PTP frames and PTP_UNICAST_EN bit in General Configuration register is set, PTP event frames will be processed. For IPv4 frames, this register is not required and it will be ignored by the Core1588

6.43. RXUCASTADDR0 (Ask a Question)

Name: RXUCASTADDR0
Offset: 0x0AC
Reset: 0x0
Property: Write-only

Unicast destination IP address bits 31 down to 0 for PTP receive frames.

Bit	31	30	29	28	27	26	25	24
	RX_UNICAST_IP_ADDR0[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_UNICAST_IP_ADDR0[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_UNICAST_IP_ADDR0[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_UNICAST_IP_ADDR0[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_UNICAST_IP_ADDR0[31:0] User can configure Unicast IP destination address0 for receive PTP frames. For IPv4 frames when the address configured in this register matches with the IP destination address of recevied PTP frames and PTP_UNICAST_EN bit in General Configuration register is set, PTP event frames will be processed. For IPv6 frames when the address configured in registers RX_UNICAST_IP_ADDR0, RX_UNICAST_IP_ADDR1, RX_UNICAST_IP_ADDR2 and RX_UNICAST_IP_ADDR3 matches with the IP destination address of received PTP frames and PTP_UNICAST_EN bit in General Configuration register is set, PTP event frames will be processed

6.44. RXUCASTADDR1 (Ask a Question)

Name: RXUCASTADDR1
Offset: 0x0B0
Reset: 0x0
Property: Write-only

Unicast destination IP address bits 63 down to 32 for PTP receive frames.

Bit	31	30	29	28	27	26	25	24
	RX_UNICAST_IP_ADDR1[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_UNICAST_IP_ADDR1[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_UNICAST_IP_ADDR1[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_UNICAST_IP_ADDR1[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_UNICAST_IP_ADDR1[31:0] User can configure Unicast IP destination address1 for receive PTP frames. For IPv6 frames when the address configured in registers RX_UNICAST_IP_ADDR0, RX_UNICAST_IP_ADDR1, RX_UNICAST_IP_ADDR2 and RX_UNICAST_IP_ADDR3 matches with the IP destination address of received PTP frames and PTP_UNICAST_EN bit in General Configuration register is set, PTP event frames will be processed. For IPv4 frames, this register is not required and it will be ignored by the Core1588

6.45. RXUCASTADDR2 (Ask a Question)

Name: RXUCASTADDR2
Offset: 0x0B4
Reset: 0x0
Property: Write-only

Unicast destination IP address bits 95 down to 64 for PTP receive frames.

Bit	31	30	29	28	27	26	25	24
	RX_UNICAST_IP_ADDR2[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_UNICAST_IP_ADDR2[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_UNICAST_IP_ADDR2[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_UNICAST_IP_ADDR2[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_UNICAST_IP_ADDR2[31:0] User can configure Unicast IP destination address2 for receive PTP frames. For IPv6 frames when the address configured in registers RX_UNICAST_IP_ADDR0, RX_UNICAST_IP_ADDR1, RX_UNICAST_IP_ADDR2 and RX_UNICAST_IP_ADDR3 matches with the IP destination address of received PTP frames and PTP_UNICAST_EN bit in General Configuration register is set, PTP event frames will be processed. For IPv4 frames, this register is not required and it will be ignored by the Core1588

6.46. RXUCASTADDR3 (Ask a Question)

Name: RXUCASTADDR3
Offset: 0x0B8
Reset: 0x0
Property: Write-only

Unicast destination IP address bits 127 down to 96 for PTP receive frames.

Bit	31	30	29	28	27	26	25	24
	RX_UNICAST_IP_ADDR3[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RX_UNICAST_IP_ADDR3[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RX_UNICAST_IP_ADDR3[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RX_UNICAST_IP_ADDR3[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RX_UNICAST_IP_ADDR3[31:0] User can configure Unicast IP destination address3 for receive PTP frames. For IPv6 frames when the address configured in registers RX_UNICAST_IP_ADDR0, RX_UNICAST_IP_ADDR1, RX_UNICAST_IP_ADDR2 and RX_UNICAST_IP_ADDR3 matches with the IP destination address of received PTP frames and PTP_UNICAST_EN bit in General Configuration register is set, PTP event frames will be processed. For IPv4 frames, this register is not required and it will be ignored by the Core1588

6.47. PEERTTSL (Ask a Question)

Name: PEERTTSL
Offset: 0x0BC
Reset: 0x0
Property: Read-only

PTP peer frame transmitted timestamp nanoseconds register

Bit	31	30	29	28	27	26	25	24
	PTP_PEER_TXNSEC[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_PEER_TXNSEC[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_PEER_TXNSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_PEER_TXNSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_PEER_TXNSEC[31:0] PTP peer frame transmitted timestamp nanoseconds. The register is updated with the nanosecond count of RTC when SFD of a PTP peer frame (PDELAY Request or PDELAY Response) is transmitted at GMII interface. An interrupt is issued when the register is updated.

6.48. PEERTTSM (Ask a Question)

Name: PEERTTSM
Offset: 0x0C0
Reset: 0x0
Property: Read-only

Note: PTP peer frame transmitted timestamp seconds register [31:0].PEERTTSMSBSECSUBNS register contains upper 16 bits [47:32] of seconds

Bit	31	30	29	28	27	26	25	24
	PTP_PEER_TXSECLSB32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_PEER_TXSECLSB32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_PEER_TXSECLSB32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_PEER_TXSECLSB32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_PEER_TXSECLSB32BITS[31:0] PTP peer frame transmitted timestamp seconds [31:0]. The register is updated with the lower 32 bits [31:0] of second count of RTC when SFD of a PTP peer frame (PDELAY Request or PDELAY Response) is transmitted at GMII interface. An interrupt is issued when the register is updated.

6.49. PEERTTSMSBSECSUBNS (Ask a Question)

Name: PEERTTSMSBSECSUBNS
Offset: 0x0C4
Reset: 0x0
Property: Read-only

PTP peer frame transmitted timestamp seconds [47:32] and sub-nanoseconds register

Bit	31	30	29	28	27	26	25	24
	PTP_PEER_TXSUBNSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_PEER_TXSUBNSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_PEER_TXSECMSB16BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_PEER_TXSECMSB16BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PTP_PEER_TXSUBNSEC[15:0] PTP peer frame transmitted timestamp sub-nanosecond most significant 16 bits. These bits are updated with the upper 16 bits [23:8] of sub-nanosecond count of RTC when SFD of a PTP peer frame (PDELAY Request or PDELAY Response) is transmitted at GMII interface. For transparent clock, residence time needs to be updated in correctionField which uses lower 16 bits for sub-nanosecond. For transparent and two step clock while transmitting PTP peer message, sub-nanosecond of egress PTP peer message should be used in updating correctionField

Bits 15:0 – PTP_PEER_TXSECMSB16BITS[15:0] PTP peer frame transmitted timestamp most significant 16 bits [47:32] of seconds count. These bits are updated with the upper 16 bits [47:32] of second count of RTC when SFD of a PTP peer frame (PDELAY Request or PDELAY Response) is transmitted at GMII interface.

6.50. PEERTTSID (Ask a Question)

Name: PEERTTSID
Offset: 0x0C8
Reset: 0x0
Property: Read-only

PTP peer frame transmitted identification register. It contains the 16-bit sequence ID

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PTP_PEER_TXSEQID[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_PEER_TXSEQID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PTP_PEER_TXSEQID[15:0] Contains the 16 bits sequenceID from the message header of the transmitted ptp peer frame (PDELAY Request or PDELAY Response) associated with the current transmitted timestamp (in the PEERTTSL, PEERTTSM and PEERTTSMSBSECSUBNS registers)

6.51. PEERRTSL (Ask a Question)

Name: PEERRTSL
Offset: 0x0CC
Reset: 0x0
Property: Read-only

PTP peer frame received timestamp nanoseconds register

Bit	31	30	29	28	27	26	25	24
	PTP_PEER_RXNSEC[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_PEER_RXNSEC[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_PEER_RXNSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_PEER_RXNSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_PEER_RXNSEC[31:0] PTP peer frame received timestamp nanoseconds. The register is updated with the nanosecond count of RTC when SFD of a PTP peer frame (PDELAY Request or PDELAY Response) is received at GMII interface. An interrupt is issued when the register is updated.

6.52. PEERRTSM (Ask a Question)

Name: PEERRTSM
Offset: 0x0D0
Reset: 0x0
Property: Read-only

Note: PTP peer frame received timestamp seconds register [31:0].PEERRTSMSBSECSUBNS register contains upper 16 bits [47:32] of seconds

Bit	31	30	29	28	27	26	25	24
	PTP_PEER_RXSEC_LSB32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_PEER_RXSEC_LSB32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_PEER_RXSEC_LSB32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_PEER_RXSEC_LSB32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_PEER_RXSEC_LSB32BITS[31:0] PTP peer frame received timestamp seconds [31:0]. The register is updated with the lower 32 bits [31:0] of second count of RTC when SFD of a PTP peer frame (PDELAY Request or PDELAY Response) is received at GMII interface. An interrupt is issued when the register is updated.

6.53. PEERRTSMSBSECSUBNS (Ask a Question)

Name: PEERRTSMSBSECSUBNS
Offset: 0x0D4
Reset: 0x0
Property: Read-only

PTP peer frame received timestamp seconds [47:32] and sub-nanoseconds register

Bit	31	30	29	28	27	26	25	24
	PTP_PEER_RXSUBNSEC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_PEER_RXSUBNSEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_PEER_RXSEC_MSB16BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_PEER_RXSEC_MSB16BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PTP_PEER_RXSUBNSEC[15:0] PTP peer frame received timestamp sub-nanosecond most significant 16 bits. This field is updated with the upper 16 bits [23:8] of sub-nanosecond count of RTC when SFD of a PTP peer frame (PDELAY Request or PDELAY Response) is received at GMII interface. For transparent clock, residence time needs to be updated in correctionField which uses lower 16 bits for sub-nanosecond. For transparent clock while transmitting PTP peer message, sub-nanosecond of ingress PTP peer message should be written into upper 16 bits of PEERINGRSTSMSBSECSUBNS register.

Bits 15:0 – PTP_PEER_RXSEC_MSB16BITS[15:0] PTP peer frame received timestamp most significant 16 bits [47:32] of seconds count. These bits are updated with the upper 16 bits [47:32] of second count of RTC when SFD of a PTP peer frame (PDELAY Request or PDELAY Response) is received at GMII interface.

6.54. PEERRTSID2 (Ask a Question)

Name: PEERRTSID2
Offset: 0x0D8
Reset: 0x0
Property: Read-only

PTP peer frame received identification register2. Contains the 16-bit sequence ID and the bits [79:64] of the sourcePortIdentity

Bit	31	30	29	28	27	26	25	24
	PTP_PEER_RXSEQID[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_PEER_RXSEQID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_PEER_RXSRCPORTID_MSB16BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_PEER_RXSRCPORTID_MSB16BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – PTP_PEER_RXSEQID[15:0] Contains the 16 bits sequenceID from the message header of the ptp peer frame (PDELAY Request or PDELAY Response) associated with the current receive timestamp (in the PEERRTSL, PEERRTSM and PEERRTSMSBSECSUBNS egisters)

Bits 15:0 – PTP_PEER_RXSRCPORTID_MSB16BITS[15:0] Contains the upper 16 bits [79:64] of sourcePortIdentity from the message header of the received ptp peer frame (PDELAY Request or PDELAY Response) associated with the current receive timestamp (in the PEERRTSL, PEERRTSM and PEERRTSMSBSEC registers)

6.55. PEERRTSID1 (Ask a Question)

Name: PEERRTSID1
Offset: 0x0DC
Reset: 0x0
Property: Read-only

PTP peer frame received identification register1. Contains bits [63:32] of the sourcePortIdentity

Bit	31	30	29	28	27	26	25	24
	PTP_PEER_RXSRCPORTID_MID32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_PEER_RXSRCPORTID_MID32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_PEER_RXSRCPORTID_MID32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_PEER_RXSRCPORTID_MID32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_PEER_RXSRCPORTID_MID32BITS[31:0] Contains the bits [63:32] of sourcePortIdentity from the message header of the received ptp peer frame ((PDELAY Request or PDELAY Response)) associated with the current receive timestamp (in the PEERRTSL, PEERRTSM and PEERRTSMSBSECSUBNS registers)

6.56. PEERRTSID0 (Ask a Question)

Name: PEERRTSID0
Offset: 0x0E0
Reset: 0x0
Property: Read-only

PTP peer frame received identification register0. Contains bits [31:0] of the sourcePortIdentity

Bit	31	30	29	28	27	26	25	24
	PTP_PEER_RXSRCPORTID_LSB32BITS[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PTP_PEER_RXSRCPORTID_LSB32BITS[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PTP_PEER_RXSRCPORTID_LSB32BITS[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PTP_PEER_RXSRCPORTID_LSB32BITS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – PTP_PEER_RXSRCPORTID_LSB32BITS[31:0] Contains the bits [31:0] of sourcePortIdentity from the message header of the received ptp peer frame (PDELAY Request or PDELAY Response) associated with the current receive timestamp (in the PEERRTSL, PEERRTSM and PEERRTSMSBSECSUBNS registers)

7. Firmware Support (Ask a Question)

This IP core requires firmware driver.

8. Additional References (Ask a Question)

This section provides a list for additional information. For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microchip FPGAs and PLDs website.

8.1. Known Issues and Workarounds (Ask a Question)

There are no known limitations and workarounds for Core1558.

8.2. Discontinued Features and Devices (Ask a Question)

Support for RGMII is discontinued from Core1588 v3.0.

8.3. Ordering Codes (Ask a Question)

Order Core1558 through your local Microchip sales representative or through microchipDIRECT. Core1588 can be ordered through your local Sales Representative. It should be ordered using the following number scheme: Core1588-XX, where XX is listed in following table:

Table 8-1. Ordering Codes

XX	Description
OM	RTL for Obfuscated RTL—multiple use license

9. Glossary (Ask a Question)

Following are the list of terms and definitions used in the document.

Table 9-1. Terms and Definitions

Term	Definition
APB	Advanced Peripheral Bus
FCS	Frame Check Sequence
GMII	Gigabit Media-Independent Interface
IER	Interrupt Enable Register
MAC	Media Access Control
MIS	Masked Interrupt Status
PHY	Physical Layer
PTP	Precision Time Protocol
RIS	Raw Interrupt Status
RTC	Real Time Counter
SOF	Start of Frame

10. Resolved Issues (Ask a Question)

The following table lists all the resolved issues for the various Core1588 releases.

Table 10-1. Resolved Issues

Release	Description
3.0	Case Number: 493642-2577620875 Added support for PolarFire® family
2.0	Initial release

11. Device Utilization and Performance (Ask a Question)

The following table lists Core1588 summary of utilization and performance information.

Table 11-1. Core1588 Utilization (Default Configuration)

Device Details		Resources			Performance (MHz)
Family	Device	LUTs	DFF	Logic Elements	
PolarFire®	MPF300TS	3720	2662	4926	PCLK – 200 MHz PTP_CLK – 170 MHz RX_CLK – 200 MHz TX_CLK – 200 MHz
RT PolarFire	RTPF500TS	8508	7986	11787	PCLK – 125 MHz PTP_CLK – 130 MHz RX_CLK – 170 MHz TX_CLK – 150 MHz
PolarFire SoC	MPFS250TS	3720	2662	4926	PCLK – 200 MHz PTP_CLK – 170 MHz RX_CLK – 200 MHz TX_CLK – 200 MHz
SmartFusion® 2	M2S150TS	4033	2675	5105	PCLK – 150 MHz PTP_CLK – 125 MHz RX_CLK – 140 MHz TX_CLK – 140 MHz
IGLOO® 2	M2GL150	4033	2675	5096	PCLK – 150 MHz PTP_CLK – 125 MHz RX_CLK – 140 MHz TX_CLK – 140 MHz

Important:

- The data in all the preceding tables is achieved using Libero SoC v2024.1 and with default GUI parameter configuration.
- Enable block creation option is selected under **Project** > **Project Settings** > **Design Flow**.
- Clock constraints used to achieve the performance numbers are listed as follows:
  - PCLK – 100 MHz
  - PTP_CLK – 125 MHz
  - RX_CLK – 125 MHz
  - TX_CLK – 125 MHz

12. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	09/2024	The following is the list of changes in revision of the document: • The document is migrated to the Microchip template.
1.0	—	Initial Release.

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