Realtek Single Chip Fast Ethernet Controller

1. Features

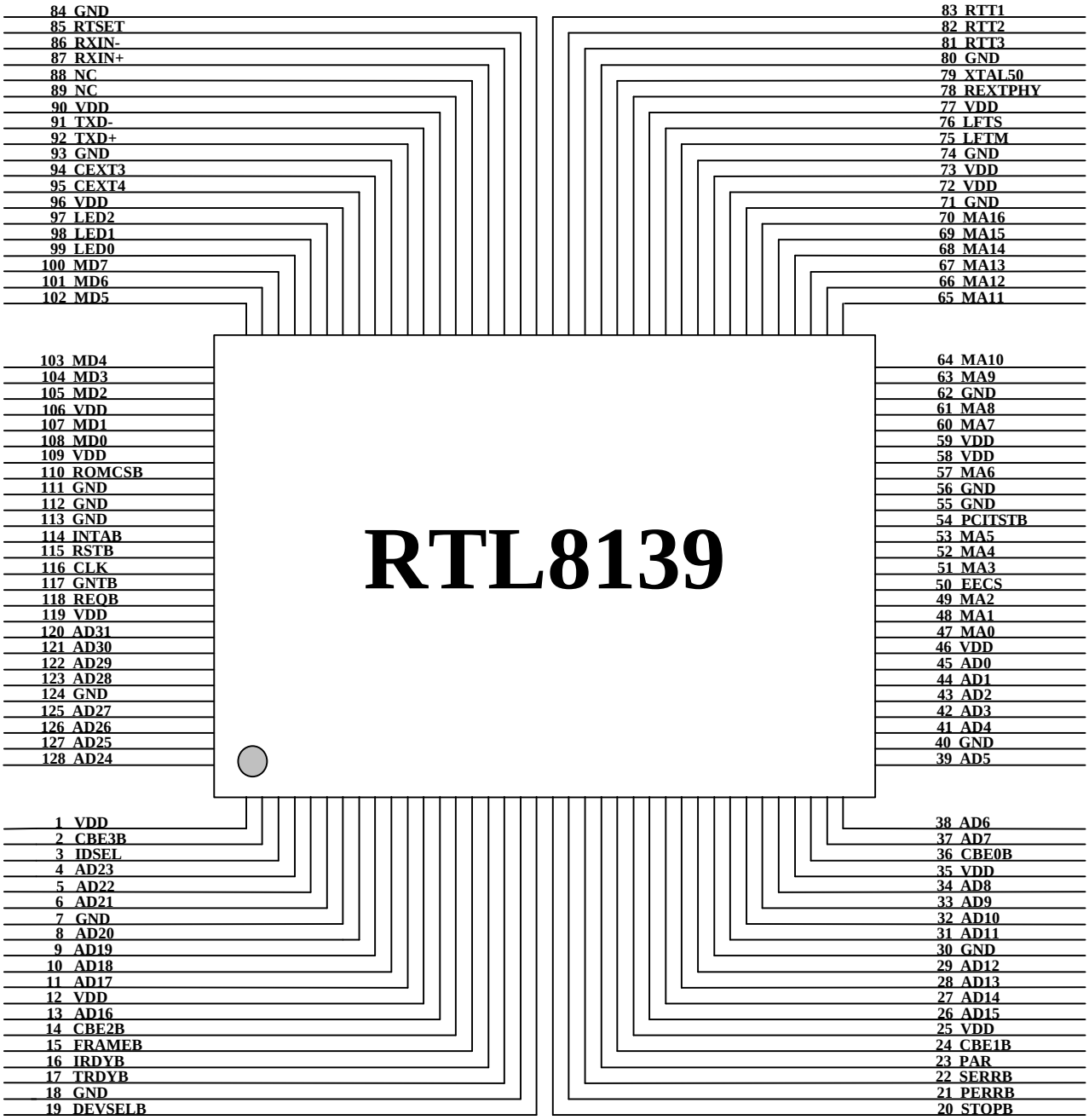
- Integrated Fast Ethernet MAC, Physical chip and transceiver in one chip
- 10 Mb/s and 100 Mb/s operation
- Support 10 Mb/s and 100 Mb/s N-way auto-negotiation
- Full compliance with PCI Revision 2.1
- Full duplex capability
- Support Full duplex flow control(IEEE 802.3x)
- PCI bus master data transfers
- Programmable PCI burst size
- Boot ROM interface (support 8K, 16K, 32K, 64K, 128K)
- Interface to 9346 (64*16-bit EEPROM) for storage of resource configuration and ID parameters
- Three level power down modes : sleep, power-down with internal clock running, and power-down with internal clock halted
- Large independent Rx and Tx FIFOs
- 128 pins PQFP with LED interface for network activity indications
- Digital and Analog loopback capability

2. General Description

The Realtek RTL8139 is a highly integrated and cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications.

The RTL8139 keeps network maintenance cost low and eliminates usage barriers. It is the easiest way to upgrade a network from 10 to 100Mbps. It also supports full-duplex operation, making possible 200Mbps of bandwidth at no addition cost. A built-in power-down function makes the RTL8139 ideal for green PC systems. The RTL8139 is highly integrated and requires no "glue" logic or external memory. It includes an interface for a boot ROM and can be used in diskless workstations, providing maximum network security and ease of management.

3. Pin Assignment



4. Pin Descriptions

4.1 PCI Interface

Symbol	Type	Pin No	Description
AD31-0	T/S	120-123, 125-128, 4-6, 8-11, 13, 26-29, 31-34, 37-39, 41-45	PCI address and data multiplexed pins
C/BE3-0	T/S	2, 14, 24, 36	PCI bus command and byte enables multiplexed pins
CLK	I	116	Clock provides timing for all transactions on PCI and is input to PCI device.
DEVSELB	S/T/S	19	Device Select : When actively driven, indicates the RTL8139 has decoded its address as the target of the current access, As an input, DEVSELB indicates whether any device on the bus has been selected.
FRAMEB	S/T/S	15	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAMEB is asserted to indicated a bus transaction is beginning. While FRAMEB is asserted, data transfers continue. When FRAMEB is deasserted, the transaction is in the final data phase.
GNTB	I	117	Grant : This signal is asserted low to indicate the RTL8139 that has been granted to access to the bus.
REQB	T/S	118	Request : The RTL8139 will assert this signal low to request to access to the bus.
IDSEL	I	3	Initialization Device Select is used as a chip select during configuration read and write transactions.
INTAB	O/D	114	INTAB is used to request an interrupt.
IRDYB	S/T/S	16	Initiator Ready indicates the initiating agent's ability to complete the current data phase of the transaction.
TRDYB	S/T/S	17	Target Ready indicates the target agent's ability to complete the current phase of the transaction.
PAR	T/S	23	Parity is even parity across AD31-0 and C/BE3-0.
PERRB	S/T/S	21	Parity Error : When the RTL8139 is in bus master access mode and a parity error is detected, the RTL8139 asserts both SERR bit in ISR and Configuration Space command bit 8 (SERRB enable). Next, it completes the current data burst transaction, then stops operation and resets itself. After the host clears the system error, the RTL8139 continues its operation. When the RTL8139 is the bus target and a parity error is detected, the RTL8139 asserts this PERRB pin.
SERRB	O/D	22	System Error : If an address parity error is detected and Configuration Space Status register bit 15 (detected parity error) is enabled, RTL8139 asserts both SERRB pin and bit 14 of Status register in Configuration Space.
STOPB	S/T/S	20	Stop : Indicates the current target is requesting the master to stop the current transaction.
RSTB	I	115	Reset : When RSTB is asserted low, the RTL8139 performs the internal system hardware reset. RSTB must be held for a minimum of 120 ns periods.

4.2 LED INTERFACE

Symbol	Type	Pin No	Description
LED0, 1, 2	O	99, 98, 97	LED pins

LEDS1-0	00	01	10	11
LED0	TX/RX	TX/RX	TX	TX
LED1	LINK100	LINK10/100	LINK10/100	LINK100
LED2	LINK10	FULL	RX	LINK10

4.3 EEPROM INTERFACE

Symbol	Type	Pin No	Description
MA16-3,	O	70-63, 61, 57, 53-51	Boot PROM address bus : used to access up to 128k byte boot PROM.
MA2/EESK,	O	49	These three pins are switched to EESK, EEDI, EEDO in 9346 programming or auto-load mode.
MA1/EEDI,	O	48	
MA0/EEDO	O/I	47	
EECS	O	50	9346 chip select
MD0-7	I/O	108, 107, 105-100	Boot PROM data bus
ROMCSB	O	110	ROM Chip Select : This is the chip select signal of the Boot PROM.

4.4 POWER PINS

Symbol	Type	Pin No	Description
VDD	P	1, 12, 25, 35, 46, 58, 59, 72, 73, 77, 90, 96, 106, 109, 119	+5V
GND	P	7, 18, 30, 40, 55, 56, 71, 74, 80, 84, 93, 111, 112, 113, 124	Ground

4.5 ATTACHMENT UNIT INTERFACE

Symbol	Type	Pin No	Description
TXD+	O	92	100/10BASE-T transmit data.
TXD-	O	91	
RXIN+	I	87	100/10BASE-T receive data.
RXIN-	I	86	
XTAL50	I	79	50Mhz oscillator clock input

4.6 TEST AND THE OTHER PINS

Symbol	Type	Pin No	Description
PCITSTB	TEST	54	PCI test pin
RTT1-3	TEST	81-83	Chip test pins
RTSET	I/O	85	This pin must pull low by 1.8K Ω resistor.
NC	-	75, 76, 78, 88, 89, 94, 95, 98, 99	No connect.

5. Register Descriptions

The RTL8139 provides the following set of operational registers mapped into PCI memory space or I/O space.

Offset	R/W	Tag	Description
0000h	R/W	IDR0	ID Register 0, The ID register0-5 are only permitted to read/write by 4-bye access.
0001h	R/W	IDR1	ID Register 1
0002h	R/W	IDR2	ID Register 2
0003h	R/W	IDR3	ID Register 3
0004h	R/W	IDR4	ID Register 4
0005h	R/W	IDR5	ID Register 5
0006h-0007h	-	-	Reserved
0008h	R/W	MAR0	Multicast Register 0, The MAR register0-7 are only permitted to read/write by 4-bye access.
0009h	R/W	MAR1	Multicast Register 1
000Ah	R/W	MAR2	Multicast Register 2
000Bh	R/W	MAR3	Multicast Register 3
000Ch	R/W	MAR4	Multicast Register 4
000Dh	R/W	MAR5	Multicast Register 5
000Eh	R/W	MAR6	Multicast Register 6
000Fh	R/W	MAR7	Multicast Register 7
0010h	R/W	TSD0	Transmit Status of Descriptor 0
0014h	R/W	TSD1	Transmit Status of Descriptor 1
0018h	R/W	TSD2	Transmit Status of Descriptor 2
001Ch	R/W	TSD3	Transmit Status of Descriptor 3
0020h	R/W	TSAD0	Transmit Start Address of Descriptor 0
0024h	R/W	TSAD1	Transmit Start Address of Descriptor 1
0028h	R/W	TSAD2	Transmit Start Address of Descriptor 2
002Ch	R/W	TSAD3	Transmit Start Address of Descriptor 3
0030h	R/W	RBSTART	Receive Buffer Start Address
0034h	R	ERBCR	Early Receive Byte Count Register
0036h	R	ERSR	Early Rx Status Register
0037h	R/W	CR	Command Register
0038h	R/W	CAPR	Current Address of Packet Read
003Ah	R	CBA	Current Buffer Address : The initial value is 0000h. It reflects total received byte-count in the Rx buffer.
003Ch	R/W	IMR	Interrupt Mask Register
003Eh	R/W	ISR	Interrupt Status Register
0040h	R/W	TCR	Transmit Configuration Register
0044h	R/W	RCR	Receive Configuration Register
0048h	R/W	TCTR	Timer Count Register : This register contains a 32-bit general-purpose timer. Writing any value to this 32-bit register will reset the original timer and begin to count from zero.

004Ch	R/W	MPC	Missed Packet Counter : Indicates the number of packets discarded due to Rx FIFO overflow. It is a 24-bit counter. After s/w reset, MPC is cleared. When written any value, MPC will be reset also.
0050h	R/W	9346CR	93C46 command register
0051h	R/W	CONFIG0	RTL8139 config0 register
0052h	R/W	CONFIG1	RTL8139 config1 register
0053h-0057h	-	-	Reserved
0058h	R/W	MSR	Media Status Register
0059h-005Ah	-	-	Reserved
005Bh	W	HLTCLK	Halt Clock Register : It is referenced by 25MHz.
005Ch	R/W	MULINT	Multiple Interrupt
005Eh	R	RERID	= 10h(PCI Revision ID)
005Fh	-	-	Reserved
0060h	R	TSAD	Transmit Status of All Descriptors : The TOK, TUN, TABT and OWN bits of all Descriptors.
0062h	R/W	BMCR	Basic Mode Control Register
0064h	R	BMSR	Basic Mode Status Register
0066h	R/W	ANAR	Auto-Negotiation Advertisement Register
0068h	R	ANLPAR	Auto-Negotiation Link Partner Ability Register
006Ah	R	ANER	Auto-Negotiation Expansion Register
006Ch	R	DIS	Disconnect Counter
006Eh	R	FCSC	False Carrier Sense Counter
0070h	R/W	NWAYTR	Nway Test Register
0072h	R	REC	RX_ER Counter
0074h	R/W	CSCR	CS Configurattion Register
0076h-007Fh	-	-	Reserved

5.1 Transmit Configuration Register(Offset 0040h-0043h, R/W)

Bit	R/W	Symbol	Description
31-26	-	-	Reserved
25-24	R/W	IFG1, 0	Interframe Gap Time : This field allows the user to adjust the interframe gap time below the standard : 9.6 us for 10Mbps, 960 ns for 100Mbps. The time can be programmed from 9.6 us to 8.4 us (10Mbps) and 960 ns to 840 ns (100Mbps). Note that any value other than one will violate the IEEE 802.3 standard. The formula for the inter frame gap is : 10Mbps 8.4 us + 0.4*(IFG(1:0))us 100 Mbps 840 ns + 40*(IFG(1:0))ns
23-19	-	-	Reserved
18, 17	R/W	LBK1, LBK0	Loopback test 00 : normal operation 01 : internal Loopback0(MAC internal loopback) 10 : internal Loopback1(loopback to Physical unit) 11 : internal Loopback2(loopback to transceiver unit)
16	R/W	CRC	0 : CRC appended 1 : CRC not appended

15-11	-	-	Reserved
10-8	R/W	MXDMA2, 1, 0	Max DMA Burst Size per Tx DMA Burst : This field sets the maximum size of transmit DMA data bursts according to the following table : 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = 2048 bytes
7-1	-	-	Reserved
0	W	CLRABT	Clear Abort : Setting this bit to 1 causes the RTL8139 to re-transmit the packet at the last transmitted descriptor when this transmission was aborted, Setting this bit is only permitted in the transmit abort state.

5.2 Transmit Status of Descriptor 0-3 (TSD0-3) Register(Offset 0010h-001Fh, R/W)

The read-only bits (CRS, TABT, OWC, CDH, NCC3-0, TOK, TUN) will be cleared by RTL8139 when the Transmit Byte Count (bit12-0) in the corresponding Tx descriptor is written. It is not affected when software writes to these bits. This register is only permitted to write by double-word access. After software reset, all bits except OWN bit are reset to "0".

Bit	R/W	Symbol	Description
31	R	CRSL	Carrier Sense Los : Set to 1 when the carrier is lost during transmitting a packet.
30	R	TABT	Transmit Abort : Set to 1 if transmission of this packet was aborted. This bit is read only, writing to this bit is not affected.
29	R	OWC	Out of Window Collision : Set to 1 if the RTL8139 encountered an "out of window" collision during the transmission of this packet.
28	R	CDH	CD Heart Beat : The same as RTL8029. This bit is cleared in the 100 Mbps mode.
27-24	R	NCC3-0	Number of Collision Count : Indicates that the number of collisions encountered during the transmission of this packet.
23-22	-	-	Reserved
21-16	R/W	ERTXTH5-0	Early Tx Threshold : Specifies the threshold level in the Tx FIFO to begin the transmission. When the byte count of the data in the FIFO reaches this level, (or the FIFO contains at least one complete packet) the RTL8139 will transmit this packet. 000000 = 8 bytes These fields count from 000001 to 111111 in unit of 32 bytes. This threshold must be avoided to exceed 2K byte.

15	R	TOK	Transmit OK : Set to 1 indicates that transmission of this packet was completed successfully and that no transmit underrun occurs.
14	R	TUN	Transmit FIFO Underrun : Set to 1 if the transmit FIFO was exhausted during the transmission of this packet. The RTL8139 can re-transfer data if the transmit FIFO underruns and can also transmit the packet to the wire successfully even though FIFO underruns. That is, when TSD<TUN>=1, TSD<TOK>=0 and ISR<TOK>=1 (or ISR<TER>=1).
13	R/W	OWN	OWN : The RTL8139 sets this bit to 1 when the Tx DMA operation of this descriptor was completed. The driver must set this bit to 0 when the Transmit Byte Count (bit0-12 is written. The default value is 1.
12-0	R/W	SIZE	Descriptor Size : indicates the total size in bytes of the data in this descriptor. If packet length is more than 1792 byte (0700h), Tx queue will be invalid. i.e. The next descriptor will be written only after the OWN bit of that long packet's descriptor has been set.

5.3 Interrupt Status Register(Offset 003Eh-003Fh, R/W)

Bit	R/W	Symbol	Description
15	R/W	SERR	System Error : Set to 1 when RTL8139 detected a system error on the PCI bus.
14 - 7	-	-	Reserved
6	R/W	FIFOOVW	Receive FIFO Overflow
5	R/W	PUN	Packet Underrun : Set to 1 when CAPR is written but Rx buffer is empty.
4	R/W	RXOVW	Rx Buffer Overflow : Set when receive buffer ring storage resources have been exhausted.
3	R/W	TER	Transmit Error : Indicates that a packet transmission was aborted, due to excessive collisions.
2	R/W	TOK	Transmit OK : Indicates that a packet transmission was completed.
1	R/W	RER	Receive Error : Indicates that a packet has CRC or frame alignment error. The collided frame will not be recognized as CRC error if the length of this frame is shorter than 16 byte.
0	R/W	ROK	Receive OK : In normal mode, indicates the completion of a packet reception. In early mode, indicates that the Rx byte-count of the arriving packet exceeds the Rx threshold.

5.4 Transmit Status of All Descriptors (TSAD) Register(Offset 0060h-061Fh, R/W)

Bit	R/W	Symbol	Description
15	R	TOK3	TOK bit of Descriptor 3
14	R	TOK2	TOK bit of Descriptor 2
13	R	TOK1	TOK bit of Descriptor 1
12	R	TOK0	TOK bit of Descriptor 0

11	R	TUN3	TUN bit of Descriptor 3
10	R	TUN2	TUN bit of Descriptor 2
9	R	TUN1	TUN bit of Descriptor 1
8	R	TUN0	TUN bit of Descriptor 0
7	R	TABT3	TABT bit of Descriptor 3
6	R	TABT2	TABT bit of Descriptor 2
5	R	TABT1	TABT bit of Descriptor 1
4	R	TABT0	TABT bit of Descriptor 0
3	R	OWN3	OWN bit of Descriptor 3
2	R	OWN2	OWN bit of Descriptor 2
1	R	OWN1	OWN bit of Descriptor 1
0	R	OWN0	OWN bit of Descriptor 0

5.5 Media Status Register(Offset 0058h, R/W)

Bit	R/W	Symbol	Description
7	R/W	TXFCE/ LdTXFCE	Tx Flow Control Enable : The flow control is valid in fullduplex mode only. This register default value come from 9346. The write value placed in LdTXFCE. The READ value is LdTXFCE when ANE=1, parallel detection mode and AEN = 0. The READ value is ANLPAR register bit -10h when AEN = 1, NWAY FLY mode.
6	R/W	RXFCE	RX Flow control Enable : The flow control is enabled in fullduplex mode only. The default value come from 9346.
5-4	-	-	Reserved
3	R	SPEED_10	Set when current media is 10 Mbps mode. Reset when current media is 100 Mbps mode.
2	R	LINKB	Inverse of Link status. 0 = Link OK. 1 = Link Fail.
1	R	TXPF	Set when RTL8139 send pause packet. Reset when RTL8139 send timer done packet.
0	R	RXPF	Pause Flag : Set when RTL8139 is in backoff state because a pause packet received. Reset when pause state is clear.

5.6 Receive Configuration Register(Offset 0044h-0047h, R/W)

Bit	R/W	Symbol	Description
31-28	-	-	Reserved
27-24	R/W	ERTH3, 2, 1, 0	Early Rx threshold bits : These bits are used to select the Rx threshold multiplier of the whole packet that has been transferred to the system buffer in early mode when the frame protocol is under the RTL8139's definition. If MISR register is not zero, these bits should be the nonzero value to select multiple interrupt. 0000 = no early Rx threshold 0001 = 1/16 0010 = 2/16 0011 = 3/16 0100 = 4/16 0101 = 5/16 0110 = 6/16 0111 = 7/16 1000 = 8/16 1001 = 9/16 1010 = 10/16 1011 = 11/16 1100 = 12/16 1101 = 13/16 1110 = 14/16 1111 = 15/16
23-16	-	-	Reserved
15-13	R/W	RXFTH2, 1, 0	Rx FIFO Threshold : Specifies FIFO Threshold level. When the number of the received data in the RTL8139's Rx FIFO has reached to this level(or the FIFO contains a complete packet), the receive PCI bus master function will begin the transfer of data from the FIFO to the host memory. This field sets the threshold level according to the following table : 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = no Rx threshold. The RTL8139 begins the transfer of data after receiving a whole packet in the FIFO.
12-11	R/W	RBLEN1, 0	Rx Buffer Length : This field indicates the size of the Rx ring buffer. 00 = 8k + 16 byte 01 = 16k + 16 byte 10 = 32K + 16 byte 11 = 64K + 16 byte
10-8	R/W	MXDMA2, 1, 0	Max DMA Burst Size per Rx DMA Burst : This field sets the maximum size of receive DMA data bursts according to the following table : 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = unlimited

7	R/W	WRAP	"0" : The RTL8139 will move the rest of the packet data to the beginning of the Rx buffer if this packet has not been moved completely but has arrived at the end of the Rx buffer. "1" : The RTL8139 will move the rest of the packet data immediately after the end of the Rx buffer . The software driver must reserve at least 1.5K bytes buffer to accept the remainder of the packet. We assume that the remainder of the packet is X bytes. The next packet will be moved from the X byte offset at the top of the Rx buffer. This bit is invalid when Rx buffer is selected to 64K bytes.
6	-	-	Reserved
5	R/W	AER	Accept Error Packet : When set to 1, all packets with CRC, alignment and/or collided fragments will be accepted. When set to 0, all packets with CRC, alignment and/or collided fragments will be rejected if possible.
4	R/W	AR	Accept Runt : This bit allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt.
3	R/W	AB	Accept Broadcast
2	R/W	AM	Accept Multicast
1	R/W	APM	Accept Physical Match
0	R/W	AAP	Accept All Physical

5.7 Multiple Interrupt Select Register(Offset 005Ch-005Dh, R/W)

If the received packet data is not the familiar protocol (IPX, IP, NDIS, etc.) to RTL8139, RCR<ERTH[3:0]> won't be used to transfer data in early mode. This register will be written to the received data length in order to make early Rx interrupt for the unfamiliar protocol.

When the multiple register is selected, the ERXTH bits in RCR must not be all zeroes.

Bit	R/W	Symbol	Description
15-12	-	-	Reserved
11-0	R/W	MISR11-0	Multiple Interrupt Select : Indicate that the RTL8139 makes an Rx interrupt after RTL8139 has transferred the byte data into the system memory. If the value of these bits is smaller than 24, there will be no early interrupt. Bit1, 0 must be zero.

5.8 Receive Status in Rx packet header

Bit	R/W	Symbol	Description
15	R	MAR	Multicast Address Received : Set to 1 indicates that a Multicast packet is received.
14	R	PAM	Physical Address Matched : Set to 1 indicates that the destination address of this packet matched the value written in ID registers.

13	R	BAR	Broadcast Address Received : Set to 1 indicates that a broadcast packet is received. BAR, NAR bit will not be set simultaneously.
12-6	-	-	Reserved
5	R	ISE	Invalid Symbol Error : (100BASE-TX only) An invalid symbol was encountered during the reception of this packet if this bit is set to 1.
4	R	RUNT	Runt Packet Received : Set to 1 indicates that the received packet length is smaller than 64 bytes(including CRC).
3	R	LONG	Long Packet : Set to 1 indicates that the size of the received packet exceeded 8k bytes.
2	R	CRC	CRC Error : When it sets it indicates a CRC error to occur on the received packet.
1	R	FAE	Frame Alignment Error : When it sets, it indicates that a frame alignment error on this received packet.
0	R	ROK	Receive OK : When it sets, it indicates that a good packet is received.

5.9 ERSR : Early Rx Status Register(Offset 0036h, R)

Bit	R/W	Symbol	Description
7-4	-	-	Reserved
3	R	ERGood	Early Rx Good packet : This bit is set whenever a packet is completely received and the packet is good. This bit is cleared when writing 1 to it.
2	R	ERBad	Early Rx Bad packet : This bit is set whenever a packet is completely received and the packet is bad. Writing 1 will clear this bit.
1	R	EROVW	Early Rx OverWrite : This bit is set when the RTL8139's local address pointer is equal to CAPR. In the early mode, this is different from buffer overflow. It happens that the RTL8139 detected an Rx error and wanted to fill another packet data from the beginning address of that error packet. Writing 1 will clear this bit.
0	R	EROK	Early Rx OK : The power-on value is 0. It is set when the Rx byte count of the arriving packet exceeds the Rx threshold. After the whole packet is received, the RTL8139 will set ROK or RER in ISR and clear this bit simultaneously. Setting this bit will invoke a ROK interrupt.

5.10 Command Register(Offset 0037h, R/W)

Bit	R/W	Symbol	Description
7-5	-	-	Reserved

4	R/W	RST	Reset : Setting to 1 forces the RTL8139 to a software reset state which disables the transmitter and receiver, reinitializes the FIFOs, resets the system buffer pointer to the initial value (Tx buffer is at TSAD0, Rx buffer is empty). The values of IDR0- 5 and MAR0-7 and MII Register (0062H-0074H) and PCI configuration space will have no changes. This bit will read back a 1 during the reset operation, and be cleared to 0 by the RTL8139 when the reset operation is complete.
3	R/W	RE	Receiver Enable
2	R/W	TE	Transmitter Enable
1	-	-	Reserved
0	R	BUFE	Buffer Empty : Rx Buffer Empty. There is no packet stored in the receive buffer ring.

5.11 9346CR : 9346 Command Register(Offset 0050h, R/W)

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7-6</td><td>R/W</td><td>EEM1-0</td><td>These 2 bits select the RTL8139 operating mode.
<table>
<tr><th>EEM1</th><th>EEM0</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (RTL8139 network/host communication mode)</td></tr>
<tr><td>0</td><td>1</td><td>Auto-load : Entering this mode will make the RTL8139 load the contents of 9346 like when the RSTB signal is asserted. This auto-load operation will take about 2 ms. After it is completed, the RTL8139 goes back to the normal mode automatically (EEM1 = EEM0 = 0) and all the other registers are reset to default values.</td></tr>
<tr><td>1</td><td>0</td><td>9346 programming : In this mode, both network and host bus master operations are disabled. The 9346 can be directly accessed via bit3-0 which now reflect the states of EECS, EESK, EEDI, & EEDO pins respectively.</td></tr>
<tr><td>1</td><td>1</td><td>Config register write enable : Before writing to CONFIG0, 1 registers, the RTL8139 must be placed in this mode. This will prevent RTL8139's configurations from accidental change.</td></tr>
</table></td></tr>
<tr><td>4-5</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>R/W</td><td>EECS</td><td rowspan="4">These bits reflect the state of EECS, EESK, EEDI & EEDO.
Note : EESK,EEDI and EEDO is valid after boot rom complete.</td></tr>
<tr><td>2</td><td>R/W</td><td>EESK</td></tr>
<tr><td>1</td><td>R/W</td><td>EEDI</td></tr>
<tr><td>0</td><td>R</td><td>EEDO</td></tr>
</table>

5.12 CONFIG 0 : Configuration Register 0(Offset 0051h, R/W)

Bit	R/W	Symbol	Description
7	R	SCR	Scrambler Mode : Always 0.
6	R	PCS	PCS mode : Always 0.
5	R	T10	10Mbps Mode : Always0.
4-3	R	PL1, PL0	Select 10Mbps medium types. Always (PL1, PL0) = (1, 0)
2-0	R	BS2, BS1, BS0	Select Boot ROM size

BS2	BS1	BS0	Description
0	0	0	No Boot ROM
0	0	1	8K Boot ROM
0	1	0	16K Boot ROM
0	1	1	32K Boot ROM
1	0	0	64K Boot ROM
1	0	1	128K Boot ROM
1	1	0	unused
1	1	1	unused

5.13 CONFIG 1 : Configuration Register 1(Offset 0052h, R/W)

Bit	R/W	Symbol	Description
7-6	R/W	LEDS1-0	See LED PIN define. This bit‘s initial value come from 9346.
5	R/W	DVRLOAD	Driver Load : Software maybe use this bit to make sure that the driver has been loaded. Writing 1 is 1. Writing 0 is 0. When the command register bits IOEN, MEMEN, BMEN of PCI configuration space are written, the RTL8139 will clear this bit automatically.
4	-	-	Reserved
3	R	MEMMAP	Memory Mapping : The operational registers are mapped into PCI memory space.
2	R	IOMAP	I/O Mapping : The operational registers are mapped into PCI I/O space.
1	R/W	SLEEP	This bit, when set, puts RTL8139 into sleep mode. In sleep mode, all LED signals except LINK100 are forced high to turn off the LEDs. The RTL8139 still handles the network transmission and reception like in normal mode, The LINK100 are not affected by this bit. This bit's power-up initial value is 0 and can be modified by software when EEM1= EEM0 = 1.
0	R/W	PWRDN	This bit, when set, puts RTL8139 into power down mode. RTL8139 supports two kinds of power down modes, which is selected by the contents of the HLTCLK register : (1) mode 1 : power down with clock running (2) mode 2 : power down with clock halted In both power down modes, the RTL8139's 10Base-T, MII modes are turned off. All network activities are ignored. In power down mode 2, the RTL8139 stops its internal clock for minimal power consumption. Registers except HLTCLK are typically not accessible in this mode. This bit's initial value comes from 9346 and can be modified if EEM1 = EEM0 = 1 in 9346CR register.

5.14 PCI Revision ID(Offset 005Eh, R)

Bit	R/W	Symbol	Description
7-0	R	Revision ID	The value in PCI Configuration Space offset 08h is 10h.

5.15 HLTCLK : Halt Clock Register(Offset 005Bh, W)

Writing to this register is invalid if RTL8139 is not in power down mode (if CONFIG1<PWRDN> bit is not zero). The data written to this register determines the RTL8139's power down mode.

Data	Power Down Mode
52H (ASCII code of 'R")	Mode 1 - clock **R**unning
48H (ASCII code of 'H")	Mode 2 - clock **H**alted
Other values	Ignored

5.16 Basic Mode Control Register(Offset 0062h-0063h, R/W)

Bit	Name	Description/Usage	Default/ Attribute
15	Reset	This bit sets the status and control registers of the PHY(register 0062-0074H) in a default state. This bit is self-clearing. 1 = software reset; 0 = normal operation.	0, RW
14	-	Reserved	-
13	Spd_Set	This bit sets the network speed. 1 = 100Mbps; 0 = 10Mbps. This bit‘s initial value come from 9346.	0, RW
12	Auto Negotiation Enable (ANE)	This bit enables/disables the NWay auto-negotiation function. 1 = enable auto-negotiation; bits 13 will be ignored. 0 = disable auto-negotiation; bits 13 and 8 will determine the link speed and the data transfer mode, respectively. This bit‘s initial value come from 9346.	0, RW
11-10	-	Reserved	-
9	Restart Auto Negotiation	This bits allows the NWay auto-negotiation function to be reset. 1 = re-start auto-negotiation; 0 = normal operation.	0, RW
8	Duplex Mode	This bit sets the duplex mode. 1 = full duplex; 0 = normal operation. This bit‘s initial value come from 9346. If bit12 = 1 ,read = status write = register value. If bit12 = 0, read = write = register value.	0, RW
7-0	-	Reserved	-

5.17 Basic Mode Status Register(Offset 0064h-0065h, R)

Bit	Name	Description/Usage	Default/ Attribute
15	100Base-T4	1 = enable 100Base-T4 support; 0 = suppress 100Base-T4 support.	0, RO
14	100Base_TX_ FD	1 = enable 100Base-TX full duplex support; 0 = suppress 100Base-TX full duplex support.	1, RO
13	100BASE_TX_HD	1 = enable 100Base-TX half duplex support; 0 = suppress 100Base-TX half duplex support.	1, RO

12	10Base_T_FD	1 = enable 10Base-T full duplex support; 0 = suppress 10Base-T full duplex support.	1, RO
11	10_Base_T_HD	1 = enable 10Base-T half duplex support; 0 = suppress 10Base-T half duplex support.	1, RO
10-6	-	Reserved	-
5	Auto Negotiation Complete	1 = auto-negotiation process completed; 0 = auto-negotiation process not completed.	0, RO
4	Remote Fault	1 = remote fault condition detected (cleared on read); 0 = no remote fault condition detected.	0, RO
3	Auto Negotiation	1 = Link had not been experienced fail state. 0 = Link had been experienced fail state	1, RD
2	Link Status	1 = valid link established; 0 = no valid link established.	0, RO
1	Jabber Detect	1 = jabber condition detected; 0 = no jabber condition detected.	0, RO
0	Extended Capability	1 = extended register capability; 0 = basic register capability only.	1, RO

5.18 Auto-negotiation Advertisement Register (Offset 0066h-0067h, R/W)

Bit	Name	Description/Usage	Default/ Attribute
15	NP	Next Page bit. 0 = transmitting the primary capability data page; 1 = transmitting the protocol specific data page.	0, RO
14	ACK	1 = acknowledge reception of link partner capability data word.	0, RO
13	RF	1 = advertise remote fault detection capability; 0 = do not advertise remote fault detection capability.	0, RW
12-11	-	Reserved	-
10	Pause	1 = flow control is supported by local node. 0 = folw control is not supported by local mode.	1, RO
9	T4	1 = 100Base-T4 is supported by local node; 0 = 100Base-T4 not supported by local node.	0, RO
8	TXFD	1 = 100Base-TX full duplex is supported by local node; 0 = 100Base-TX full duplex not supported by local node.	1, RW
7	TX	1 = 100Base-TX is supported by local node; 0 = 100Base-TX not supported by local node.	1, RW
6	10FD	1 = 10Base-T full duplex supported by local node; 0 = 10Base-T full duplex not supported by local node.	1, RW
5	10	1 = 10Base-T is supported by local node; 0 = 10Base-T not supported by local node.	1, RW
4-0	Selector	Binary encoded selector supported by this node. Currently only CSMA/ CD <00001> is specified. No other protocols are supported.	<00001>, RW

5.19 Auto-Negotiation Link Partner Ability Register(Offset 0068h-0069h, R)

Bit	Name	Description/Usage	Default/ Attribute
15	NP	Next Page bit. 0 = transmitting the primary capability data page; 1 = transmitting the protocol specific data page.	0, RO
14	ACK	1 = link partner acknowledges reception of local node's capability data word.	0, RO
13	RF	1 = link partner is indicating a remote fault.	0, RO
12-11	-	Reserved	-
10	Pause	1 = Flow control is supported by link parter , 0 = Flow control is not supported by link partner.	0, RO
9	T4	1 = 100Base-T4 is supported by link partner; 0 = 100Base-T4 not supported by link partner.	0, RO
8	TXFD	1 = 100Base-TX full duplex is supported by link partner; 0 = 100Base-TX full duplex not supported by link partner.	0, RO
7	TX	1 = 100Base-TX is supported by link partner; 0 = 100Base-TX not supported by link partner.	0, RO
6	10FD	1 = 10Base-T full duplex is supported by link partner; 0 = 10Base-T full duplex not supported by link partner.	0, RO
5	10	1 = 10Base-T is supported by link partner; 0 = 10Base-T not supported by link partner.	0, RO
4-0	Selector	Link Partner's binary encoded node selector. Currently only CSMA/ CD <00001> is specified.	<00000>, RO

5.20 Auto-negotiation Expansion Register(Offset 006Ah-006Bh, R)

This register contains additional status for NWay auto-negotiation.

Bit	Name	Description/Usage	Default/ Attribute
15-5	-	Reserved , This bit is always set to 0.	-
4	MLF	Status indicating if a multiple link fault has occurred. 1 = fault occurred; 0 = no fault occurred.	0, RO
3	LP_NP_ABLE	Status indicating if the link partner supports Next Page negotiation. 1 = supported; 0 = not supported.	0, RO
2	NP_ABLE	This bit indicates if the local node is able to send additional Next Pages.	0, RO
1	PAGE_RX	This bit is set when a new Link Code Word Page has been received. The bit is automatically cleared when the auto-negotiation link partner's ability register (register 5) is read by management.	0, RO
0	LP_NW_ABLE	1 = link partner supports NWay auto-negotiation.	0, RO

5.21 Disconnect Counter(Offset 006Ch-006Dh, R)

Bit	Name	Description/Usage	Default/ Attribute
15-0	DCNT	This 16-bit counter increments by 1 for every disconnect event. It rolls over when becomes full. It is clear to zero by read command.	h'[0000], R

5.22 False Carrier Sense Counter(Offset 006Eh-006Fh, R)

Bit	Name	Description/Usage	Default/ Attribute
15-0	FCSCNT	This 16-bit counter is increments for each false carrier event. It is cleared to zero by read command.	h'[0000], R

5.23 NWay Test Register(Offset 0070h-0071h, R/W)

Bit	Name	Description/Usage	Default/ Attribute
15-8	-	Reserved	-
7	NWLPBK	1 = set NWay to loopback mode.	0, RW
6-4	-	Reserved	-
3	ENNWLE	1 = LED0 Pin indicates linkpulse	0, RW
2	FLAGABD	1 = Auto-neg experienced ability detect state	0, RO
1	FLAGPDF	1 = Auto-neg experienced parallel detection fault state	0, RO
0	FLAGLSC	1 = Auto-neg experienced link status check state	0, RO

5.24 RX_ER Counter(Offset 0072h-0073h, R)

Bit	Name	Description/Usage	Default/ Attribute
15-0	RXERCNT	This 16-bit counter increments by 1 for each valid packet received . It is cleared to zero by read command.	h'[0000], R

5.25 CS Configuration Register(Offset 0074h-0075h, R/W)

Bit	Name	Description/Usage	Default/ Attribute
15	Testfun	1 = Auto-neg speeds up internal timer	0,WO
14-10	-	Reserved	-
9	LD	Active low TPI link disable signal. When low TPIstilltransmit link pulses and TPI stays in good link state.	1, RW
8	HEART BEAT	1 = HEART BEAT enable,0 = HEART BEAT disable. HEART BEATfunction is only valid in 10Mbps mode.	1, RW
7	JBEN	1 = enable jabber function. 0 = disable jabber function	1, RW
6	F_LINK_100	Used to login force good link in 100Mbps for diagnostic purposes. 1 = DISABLE , 0 = ENABLE.	1, RW
5	F_Connect	Assertion of this bit forces the disconnect function to be bypassed.	0, RW
4	-	Reserved.	-
3	Con_status	This bit indicates the status of the connection. 1 = valid connected link detected; 0 = disconnected link detected.	0, RO
2	Con_status_En	Assertion of this bit configures LED1 pin to indicate connection status.	0, RW
1	-	Reserved	-
0	PASS_SCR	Bypass Scramble	0, RW

6. EEPROM (9346) Contents

The 9346 is a 1K-bit EEPROM. Although it is actually addressed by words, we list its contents by bytes below for convenience.

After the valid duration of the RSTB pin or auto-load command in 9346CR, the RTL8139 performs a series of EEPROM read operation from the 9346 address 00H to 15H.

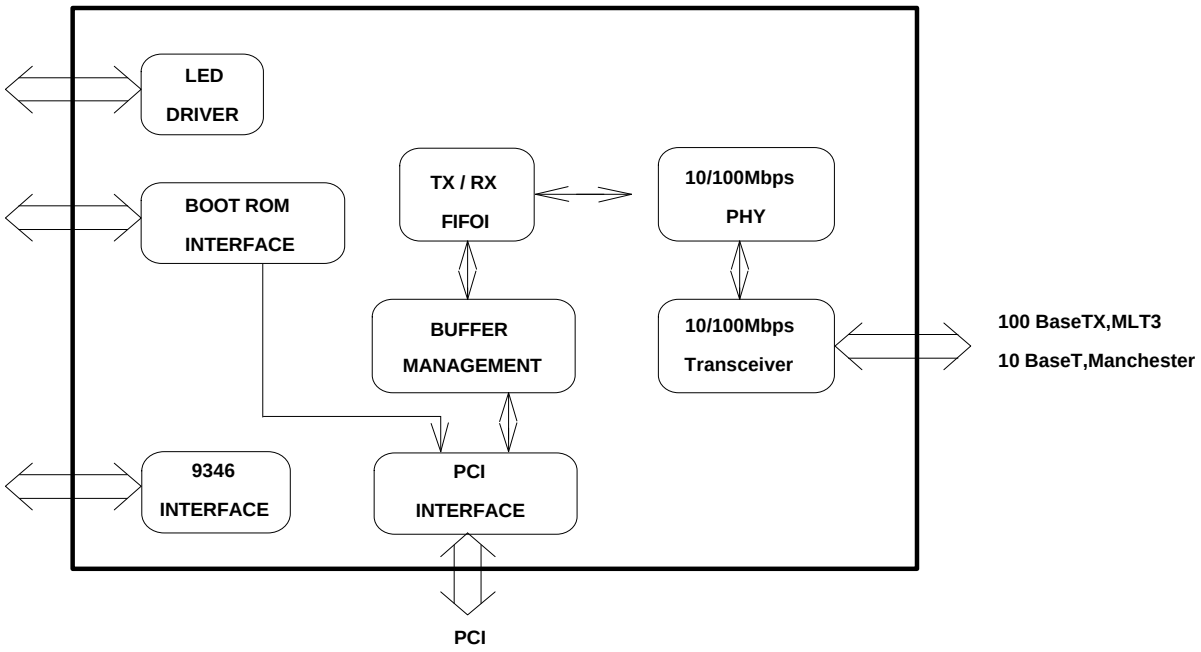
Bytes	Contents	Description
00H 01H	29h 81h	Byte0, 1 are the identify codes for the RTL8139. If the data of the EEPROM's address0, 1 are not 29H, 81H after the auto-load function, the RTL8139 will set default value (10ECH, 8129H) to the PCI vendor and device ID of the configuration space.
02H-03H	VID	PCI Vendor ID, PCI configuration space address 00H-01H
04H-05H	DID	PCI Device ID, PCI configuration space address 02H-03H
06H-07H	SVID	PCI Subsystem Vendor ID, PCI configuration space address 2CH-2DH
08H-09H	SMID	PCI Subsystem ID, PCI configuration space address 2EH-2FH
0AH	MNGNT	PCI Minimum Grant Timer, PCI configuration space address 3EH
0BH	MXLAT	PCI Maximum Latency Timer, PCI configuration space address 3FH
0CH	CONFIG2	RTL8139 Media Status Register.
0DH	-	Reserved
0EH-13H	Ethernet ID	Ethernet ID. After auto-load command or hardware reset, 9346 will load Ethernet ID to IDR0 - IDR5 of RTL8139's.
14H	CONFIG0	RTL8139 Configuration register 0, operational registers offset 51H
15H	CONFIG1	RTL8139 Configuration register 1, operational registers offset 52H

6.1 Summary of 9346CR and the registers in the EEPROM (9346)

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H-05H	IDR0-IDR5	R/W*								
50H	9346CR	R	EEM1	EEM0	-	-	EECS	EESK	EEDI	EEDO
		W	EEM1	EEM0	-	-	EECS	EESK	EEDI	-
51H	CONFIG0	R	-	-	-	-	-	BS2	BS1	BS0
		W*	-	-	-	-	-	-	-	-
52H	CONFIG1	R	LEDS1	LEDS0	DVRLOAD	-	MEMMAP	IOMAP	SLEEP	PWRDN
		W*	LEDS1	LEDS0	DVRLOAD	-	-	-	SLEEP	PWRDN
58H	CONFIG2	R	TxFCE	RxFCE	-	-	-	-	-	-
		W	TxFCE	RxFCE	-	-	-	-	-	-
62H		R	-	-	Spd_Set	ANE	-	-	-	FUDUP
		W	-	-	Spd_Set	ANE	-	-	-	FUDUP

Note : The registers marked with type = "W*" can be written only if bits EEM1 = EEM0 = 1.

7. Block Diagram



RTL8139 Block Diagram

8. Function Description

8.1 Transmit operation

The host CPU initiates a transmit by storing an entire packet of data in one of the descriptors in the main memory. When the entire packet has been transferred to the Tx buffer, the RTL8139 is instructed to move the data from the Tx buffer to the internal transmit FIFO in PCI bus master mode. When the transmit FIFO contains a complete packet or is filled to the programmed threshold level, the RTL8139 begins packet transmission.

8.2 Receive operation

The incoming packet is placed in the RTL8139's Rx FIFO. Concurrently, the RTL8139 performs address filtering of multicast packets according to its hash algorithms. When the amount of data in the Rx FIFO reaches the level defined in the Receive Configuration Register, the RTL8139 requests the PCI bus to begin transferring the data to the Rx buffer.

8.3 Loopback Operation

The RTL8139 supports two loopback modes : internal loopback and external loopback.

8.3.1 Internal Loopback Mode

Internal loopback mode is normally used to verify that the internal logic functions correctly. In loopback mode, the RTL8139 takes frames from the transmit descriptor and loops them back internally to the receive descriptor. In loopback mode, the RTL8139 disconnects from the Ethernet cable.

8.3.2 External Loopback Mode

External loopback mode is normally used to verify that the logic operations up to the Ethernet cable function correctly. In external loopback mode for 100Mbps, the RTL8139 takes frames from the transmit descriptor and transmits them to clock generator/recovery interface.

8.4 Tx Encapsulation

While operating either in 100Base-Tx mode, the RTL8139 encapsulates the frames that it transmits according to the 4B/5B code-groups table. The changes of the original packet data are listed as follows :

1. The first byte of the preamble in the MAC frame is replaced with the JK symbol pair.
2. After the CRC, the TR symbol pair is inserted.

8.5 Collision

If the RTL8139 is not in the full-duplex mode, a collision event occurs when the receive input is not idle while the RTL8139 transmits. If the collision was detected during the preamble transmission, the jam pattern is transmitted after completing the preamble (including the JK symbol pair).

8.6 Rx Decapsulation

The RTL8139 continuously monitors the network when reception is enabled. When activity is recognized it starts to process the incoming data.

After detecting receive activity on the line, the RTL8139 starts to process the preamble bytes based on the mode of operation.
While operating in 100Base-Tx mode, the RTL8139 expects the frame to start with the symbol pair JK in the first bye of the 8-byte preamble.
The RTL8139 checks the CRC bytes and checks if the packet data ends with the TR symbol pair, if not, the RTL8139 reports an CRC error RSR.

The RTL8139 reports a RSR<CRC> error in any of the following cases :

1. In the 100Base-Tx mode, one of the following occur.

a. An invalid symbol (4B/5B Table) is received in the middle of the frame.
   RSR<ISE> bit also sets.
b. The frame does not end with the TR symbol pair.

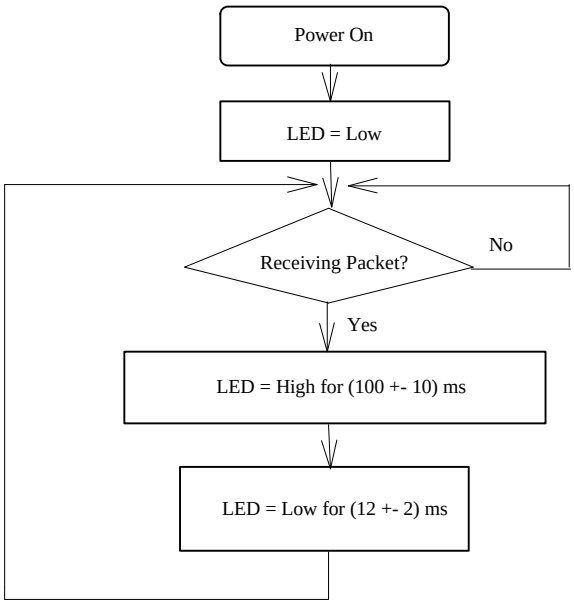
8.7 LED Functions

8.7.1 10/100 Mbps Link Monitor

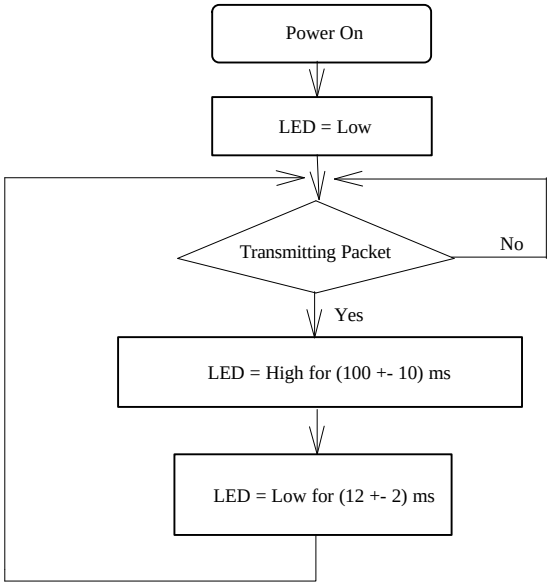
The Link Monitor senses the link integrity or if a station is down.

8.7.2 LED_RX

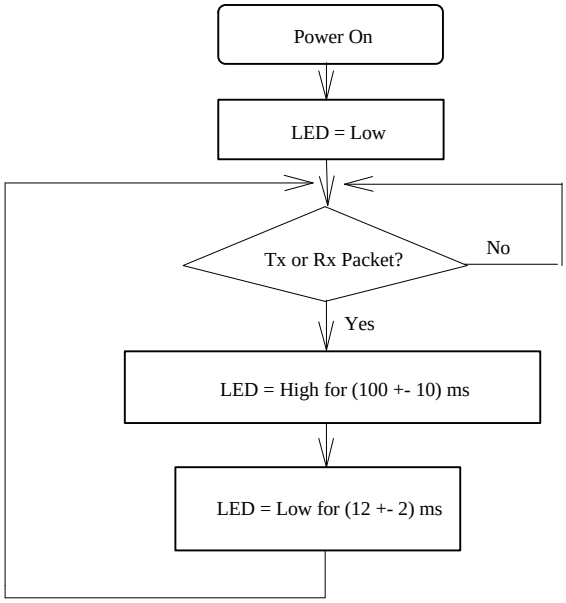
In 10/100 Mbps mode, the LED function is like RTL8129.



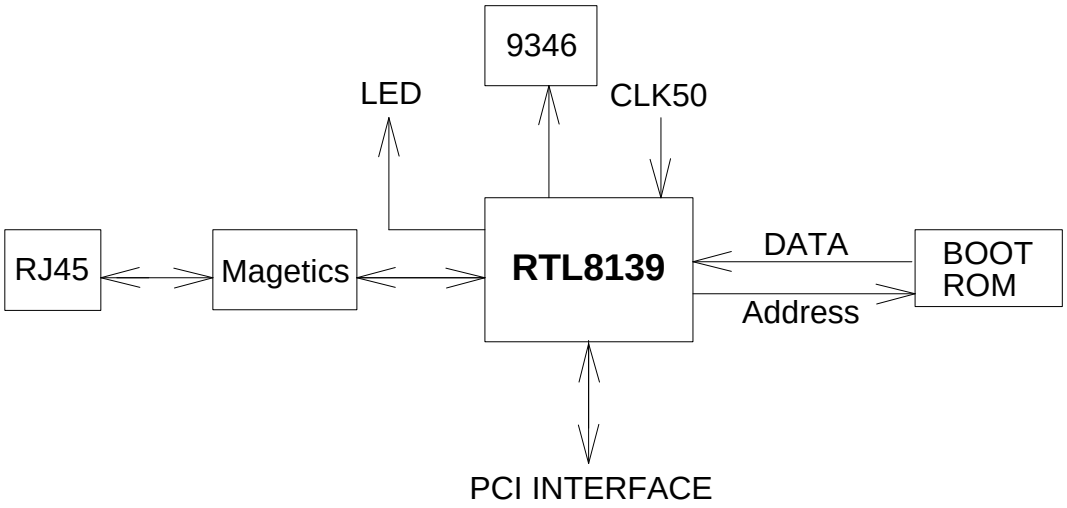
8.7.3 LED_TX



8.7.4 LED_TX+LED_RX



9. Application Diagram



10. Electrical Characteristics

10.1 Temperature Limit Ratings

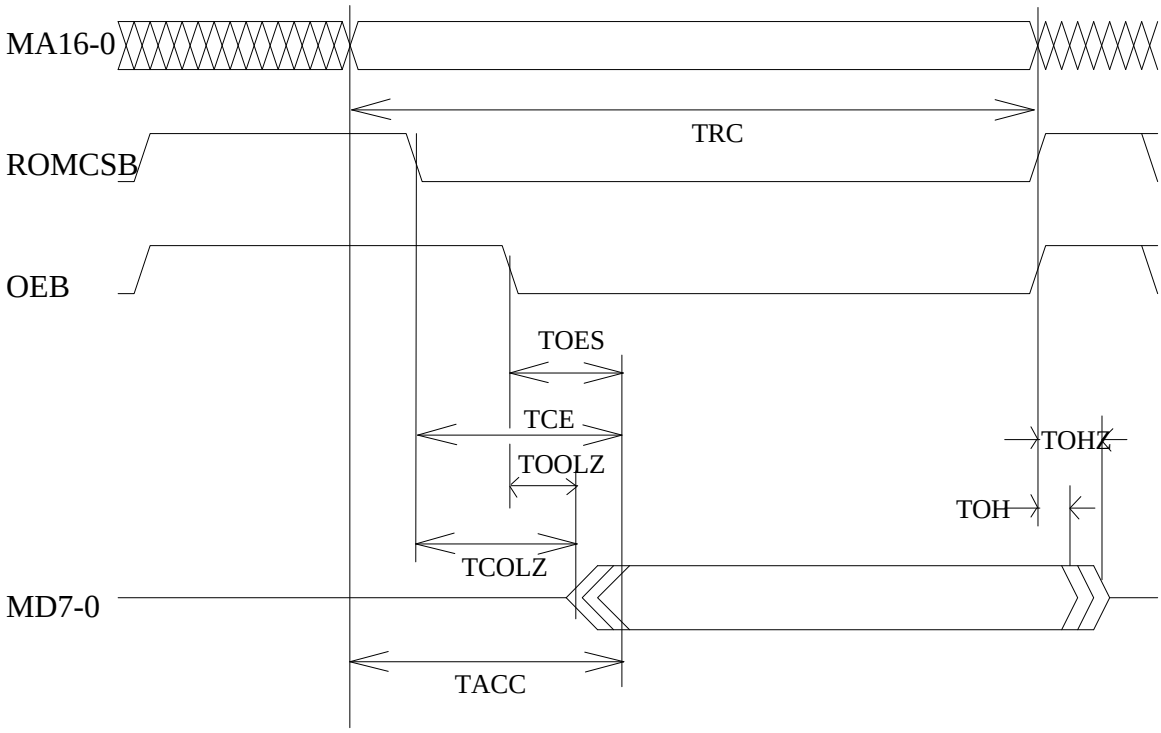
Parameter	Minimum	Maximum	Units
Storage temperature	-55	+125	¢ J
Operating temperature	0	70	¢ J

10.2 DC CHARACTERISTICS : Supply voltage V_{dd} = 5V ¡ Ó 5¢ M

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{OH}	Minimum High Level Output Voltage	I_{OH} = -8mA	3		V
V_{OL}	Maximum Low Level Output Voltage	I_{OL} = 8mA		0.4	V
V_{IH}	Minimum High Level Input Voltage		2.0	V_{dd}+0.5	V
V_{IL}	Maximum Low Level Input Voltage		-0.5	0.8	V
I_{IN}	Input Current	V_{IN} = V_{CC} or GND	-1.0	1.0	£ ¶A
I_{OZ}	Tri-State Output Leakage Current	V_{Out} = V_{CC} or GND	-10	10	£ ¶A
I_{CC}	Average Operating Supply Current	I_{OUT} = 0mA	40	330	mA

10.3 AC CHARACTERISTICS

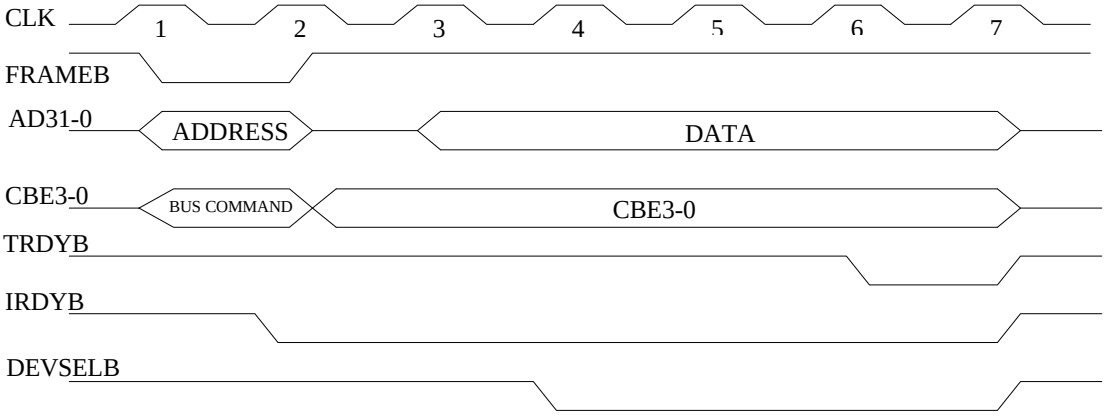
10.3.1 BOOT ROM Timing(Read)



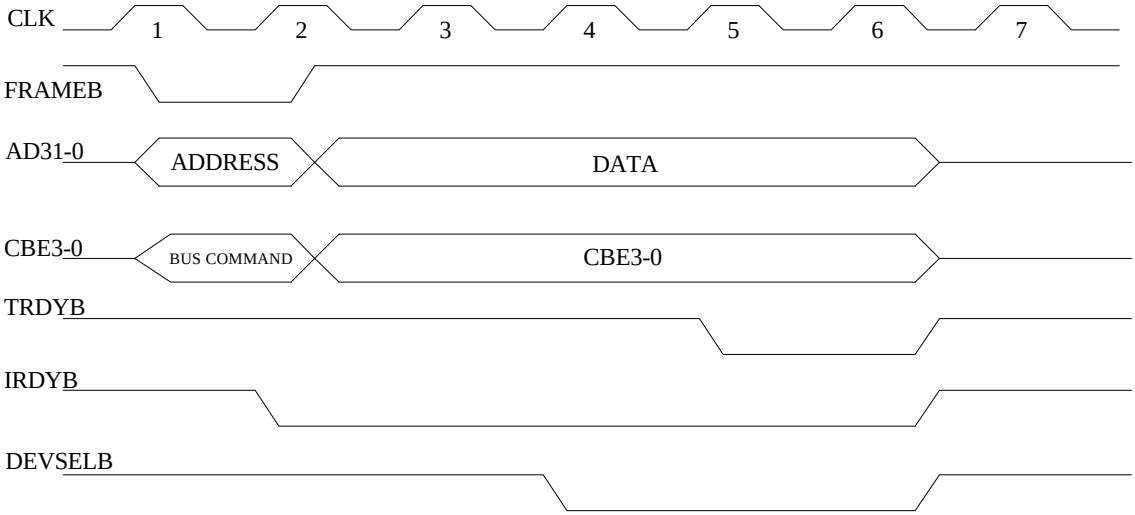
Symbol	Description	Minimum	Typical	Maximum	Units
TRC	Read Cycle	135	-	-	ns
TCE	Chip Enable Access Time	-	-	200	ns
TACC	Address Access Time	-	-	200	ns
TOES	Output Enable Access Time	-	-	60	ns
TCOLZ	Chip Enable to Output in Low Z	0	-	-	ns
TOOLZ	Output Enable to Output in Low Z	0	-	-	ns
TOHZ	Output Disable to Output in High Z	-	-	40	ns
TOH	Output Hold from Address, ROMCSB, or OEB	0	-	0	ns
TWRBR	Write Recovery time Before Read	6	-	-	us

10.3.2 PCI Bus Operation Timing

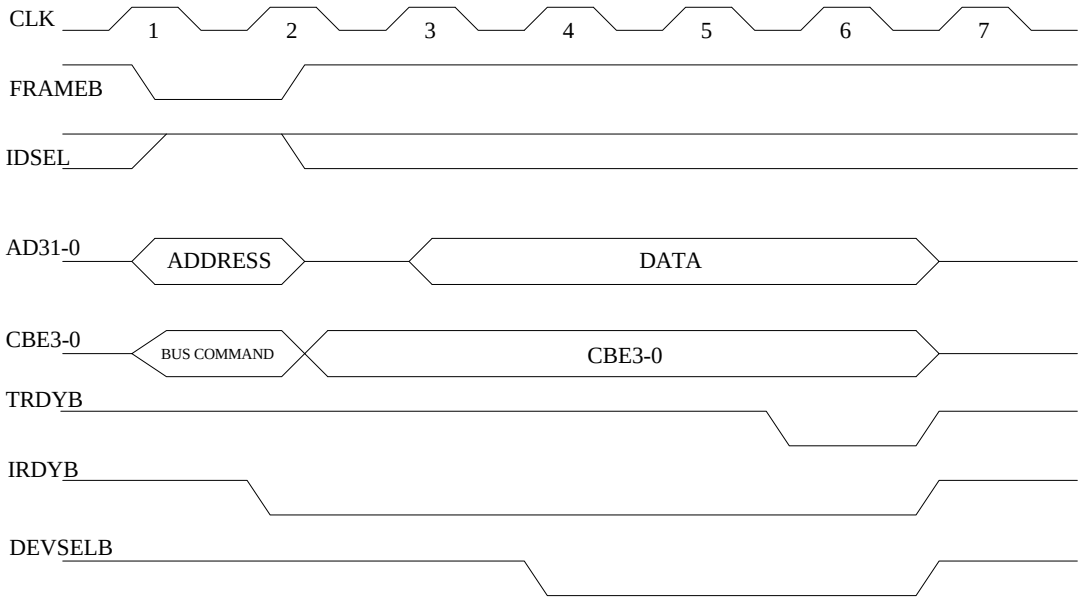
Target Read



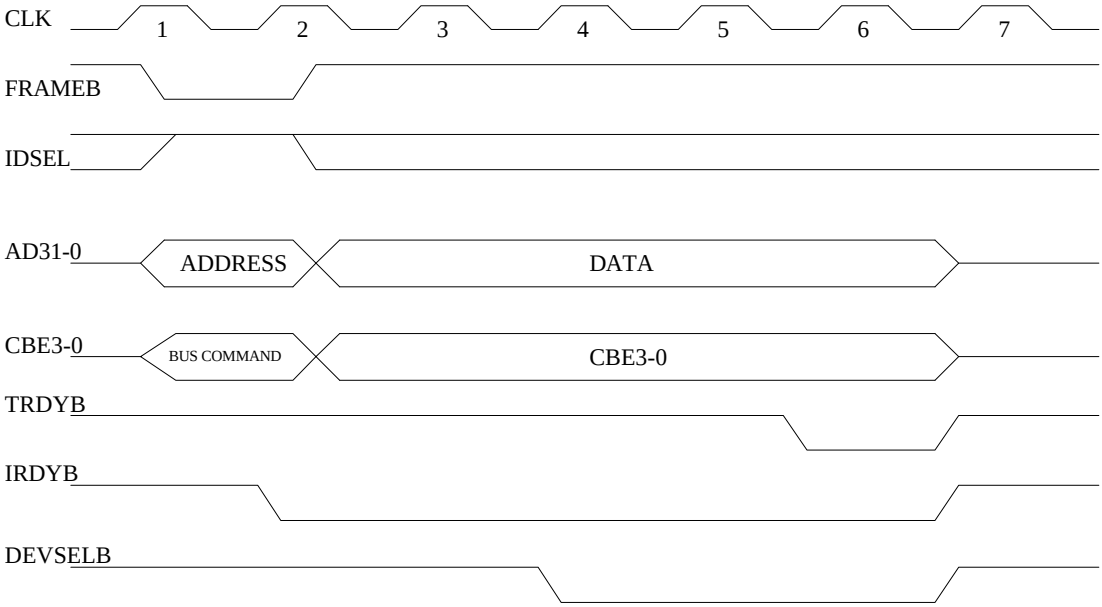
Target Write



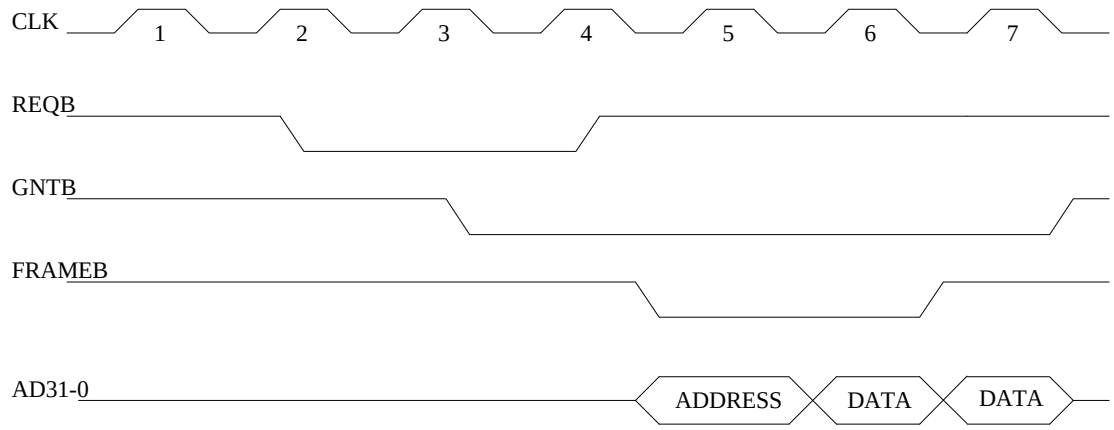
Configuration Read



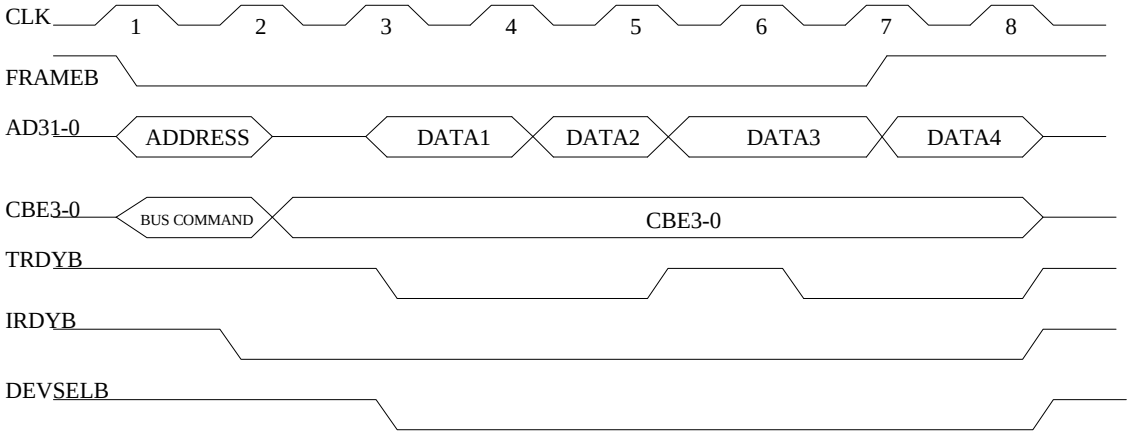
Configuration Write



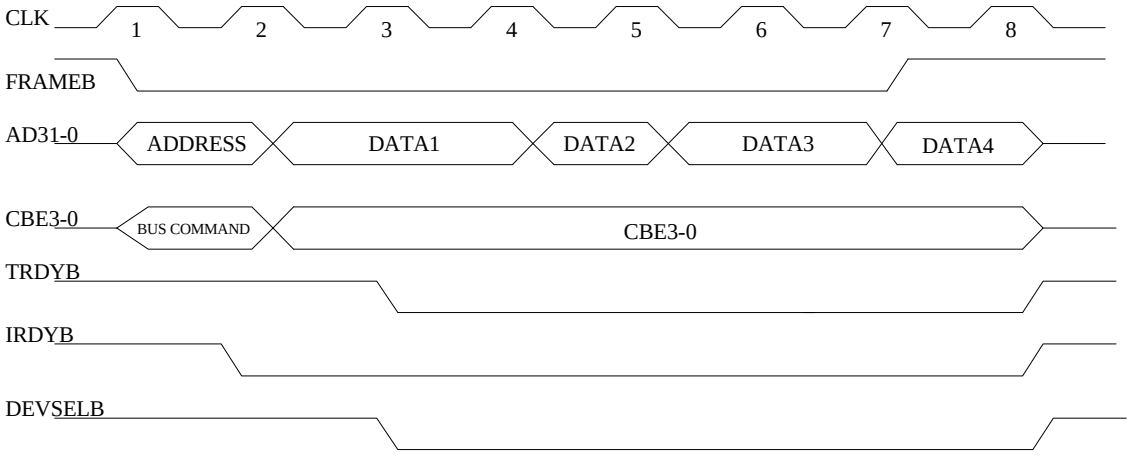
BUS Arbitration



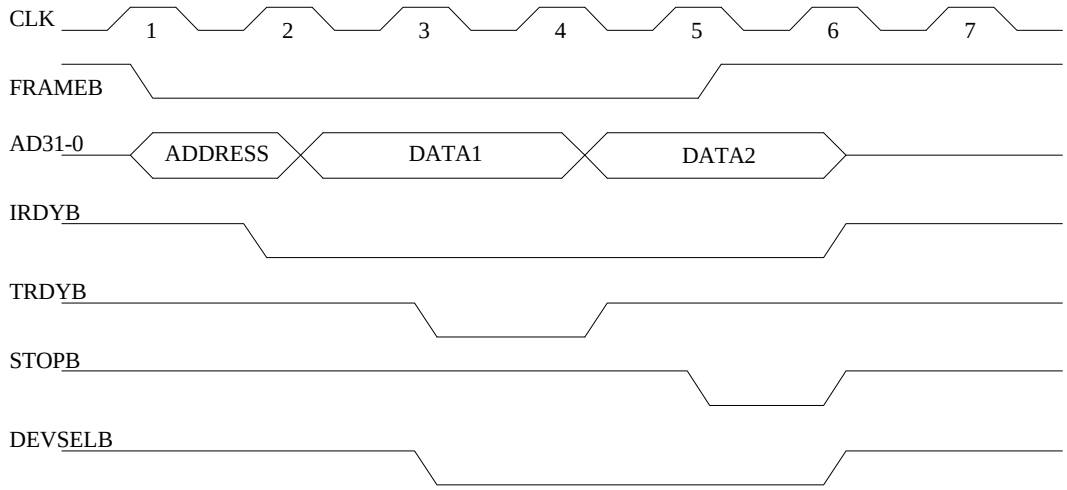
Memory Read



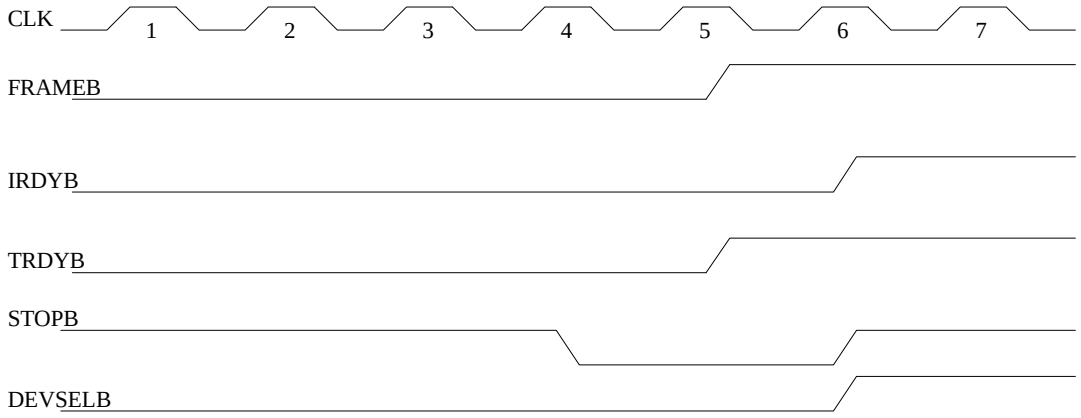
Memory Write



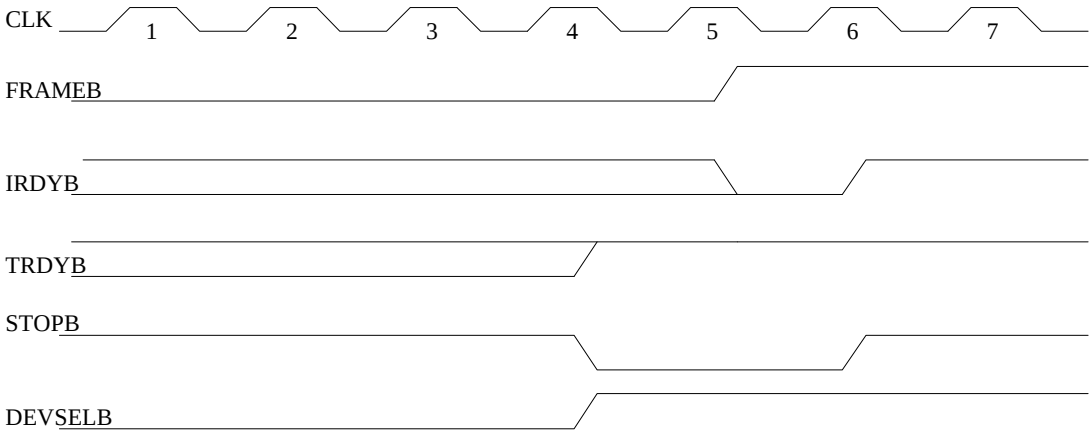
Target Initiated Termination - Retry



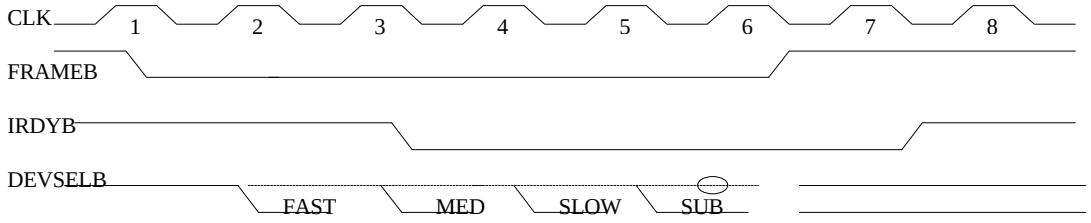
Target Initiated Termination - Disconnect



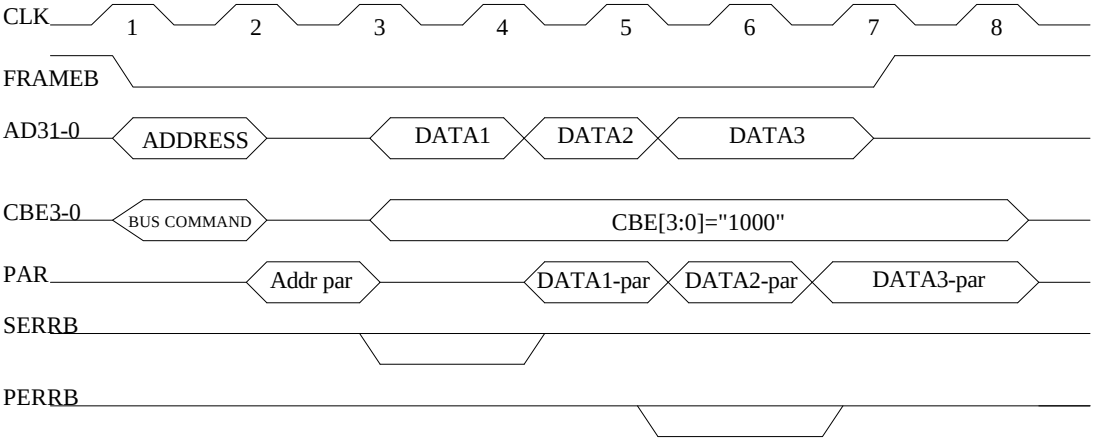
Target Initiated Termination - Abort



Master Initiated Termination - Abort



Parity Operation - one example



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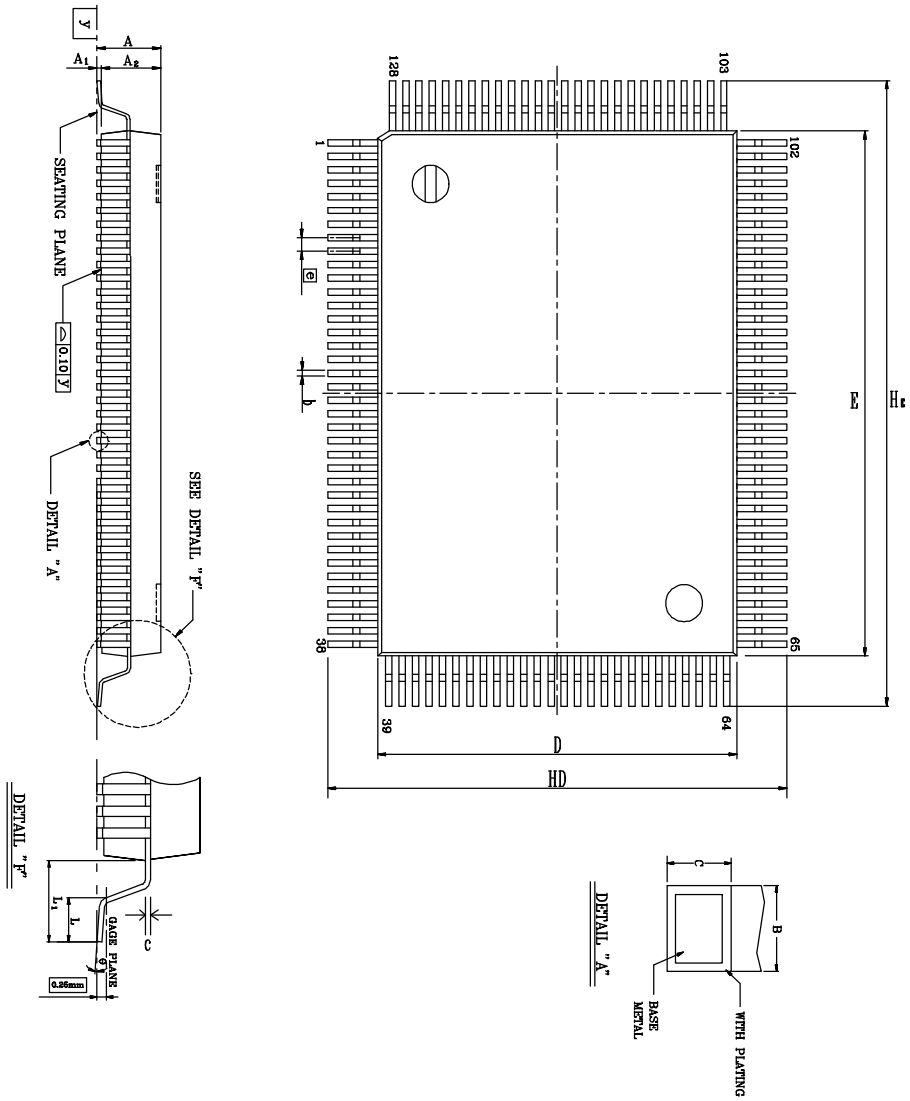

Symbol	Dimension in inch			Dimension in mm		
	Min	Type	Max	Min	Type	Max
A	¡ Ð		0.134	¡ Ð	¡ Ð	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	¡ Ð	¡ Ð	0.004	¡ Ð	¡ Ð	0.10
£ c	0¢ X	¡ Ð	12¢ X	0¢ X	¡ Ð	12¢ X

Note :

1.Dimension D & E do not include interlead flash.

2.Dimension b does not include dambar protrusion/intrusion

3.Controlling dimension : Millimeter

4.General appearance spec. should be based on final visual inspection spec.

TITLE : 128 QFP (14x20 mm) PACKAGE OUTLINE -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL :			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	Q128 - 1
		DATE	MAR. 25.1997
REALTEK SEMI-CONDUCTOR CO., LTD			