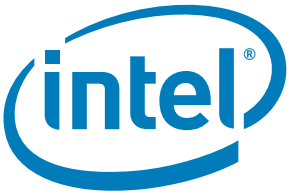


Intel® I/O Controller Hub 8/9 LAN NVM Map and Information Guide

April 2012

Revision 2.6

Contents

Tables

Revision History

Rev	Rev Date	Description
2.6	April 2012	Updated NVM words 13h (bit 0) and 15h (bits 15:8).
2.5	Jan 2012	Initial Release (Public).
2.4	Jan 2007	Updated sections 1.2, 1.4.6, 1.4.13, 1.4.14, 1.4.19, and 1.4.20. Added sections 1.4.25.1 through 1.4.25.4 (PXE words 30h through 33h).
2.3	Jan 2007	Added ICH9 and 82567 NVM information.
2.2	Oct 2006	Added device IDs for the 82562G and 82562GT 10/100 Mb/s Platform LAN Connects.
2.1	July 2006	Changed bit 1 of word 13h to 0b.
2.0	June 2006	Initial public release. Added new LAN Word Offset 19h description to Tables 1 and 17. Added new EEPROM images to Appendix A. Updated bit defaults and descriptions to Tables 9, 10, 13, 15, and 16.
1.75	April 2006	Updated bit descriptions for words 13h, 14h, and 19h.
1.5	Feb 2006	Initial Intel Confidential release. Converted this to a stand-alone document. Previously, it was AP-478 Addendum. Added Section 1.1, ”NVM Programming Procedure Overview,” and Section 1.2, ”EEUPDATE Utility.” Updated the following sections: Section 2.12, ”Shared Initialization Control (Word 13h),” bits 10 and 0 Section 2.13, ”Extended Configuration Word 1 (Word 14h),” bits 15, 14, and 11:0 Section 2.14, ”Extended Configuration Word 2 (Word 15h),” bits 15:8 Section 2.15, ”Extended Configuration Word 3 (Word 16h)” Section 2.16, ”LED 1 Configuration and Power Management (Word 17h),” bit 7 Section 2.17, ”LED 0 and 2 Configuration Defaults (Word 18h),” bit 7 Section 2.18, ”Future Initialization Word 1 (Words 19h)” Section 2.20, ”Checksum (Word 3Fh)” Appendix A.1 ”82566DM NVM Image with ICH8” Appendix A.3 ”82562V NVM Image with ICH8”
1.0	Dec 2005	Updated Section 2.12, ”Shared Initialization Control (Word 13h),” Table 9 to add the Ext Pwr Polarity bit. Added the 82566 NVM image to A.1 ”82566DM NVM Image with ICH8.”
0.75	July 2005	Initial release (Intel Secret).

1.0 Non-Volatile Memory (NVM)

1.1 Introduction

The document is intended for designs using the 10/100/1000 Mb/s LAN controller that is integrated into the Intel® I/O Control Hub 8 or I/O Control Hub 9 (ICH8/ICH9) device.

The Non-Volatile Memory (NVM) space is used for hardware and software configuration. It is read by software to determine and configure specific design features.

Unless otherwise specified, all numbers in this document use the following numbering convention:

- Numbers that do not have a suffix are decimal (base 10).
- Numbers with a suffix of "h" are hexadecimal (base 16).
- Numbers with a suffix of "b" are binary (base 2).

1.2 NVM Programming Procedure Overview

The LAN NVM shares space on an SPI Flash device (or devices) along with the BIOS, Manageability Firmware, and a Flash Descriptor Region. It is programmed through the ICH8/ICH9. This combined image is shown in Figure 1. The Flash Descriptor Region is used to define vendor specific information and the location, allocated space, and read and write permissions for each region. The Manageability (ME) Region contains the code and configuration data for ME functions such as Intel® Active Management Technology, ASF, and Advanced Fan Speed Control. The system BIOS is contained in the BIOS Region. The ME Region and BIOS Region are beyond the scope of this document and a more detailed explanation of these areas can be found in the *Intel® I/O Controller Hub 8 (ICH8) Family External Design Specification (ICH8 EDS)* and the *Intel® I/O Controller Hub 9 (ICH9) Family External Design Specification (ICH9 EDS)*. This document describes the LAN image contained in the Gigabit Ethernet (GbE) region. Fast Ethernet (**82562V**) images are also described.

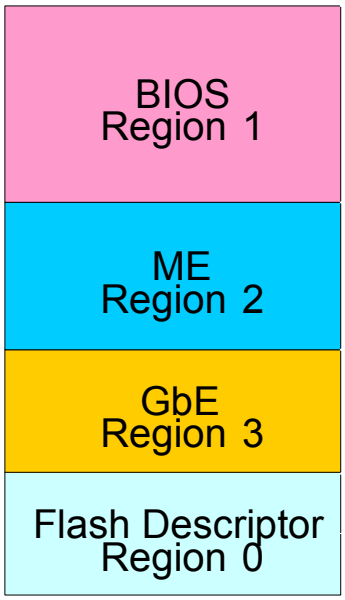
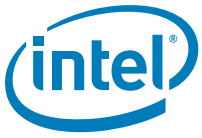


Figure 1. LAN NVM Regions

To access the NVM, it is essential to correctly setup the following:

1. A valid Flash Descriptor Region must be present. Details for the Flash Descriptor Region are contained in the ICH8/ICH9 EDS. The `FTOOL.exe` utility provides the easiest method of configuring this descriptor region. This process is described in detail in the *Intel® Active Management Technology OEM Bring-Up Guide*. `FTOOL.exe` and the *Intel® Active Management Technology OEM Bring-Up Guide* can be obtained as part of the Intel Active Client Manager kit on ARMS (https://platformsw.intel.com/) or by contacting your local Intel representative.
2. The GbE region must be part of the original image flashed onto the part.
3. For Intel LAN tools and drivers to work correctly, the BIOS must set the VSCC register(s) correctly.
   For the **ICH9**, there are two sets of VSCC registers, the upper (UVSCC) and lower (LVSCC). Note that the LVSCC register is only used if the NVM attributes change. For example, the use of a second flash component, a change in erase size between segments, etc. Due to the architecture of the **ICH8/ICH9**, if these registers are not set correctly, the LAN tools might not report an error message even though the NVM contents remain unchanged. Refer to the ICH8/ICH9 EDS for more information
4. The GbE region of the NVM must be accessible. To keep this region accessible, the Protected Range register of the GbE LAN Memory Mapped Configuration registers must be set to their default value of 0000 0000h. (The GbE Protected Range registers are described in the ICH8/ICH9 EDS).
5. If you are using the **82566/82567**, the ICH8/ICH9 soft strap for the GLCI interface must be set correctly. Bit 19 of STRP0 must be set to 1b (as described in the ICH8/ICH9 EDS). For the **82562V**, this bit can be set to 0b, since it does not use the GLCI bus.



6. The sector size of the NVM must equal 256 bytes, 4 KB, or 64 KB. When a Flash device that uses a 64 KB sector erase is used, the GbE region size must equal 128 KB. If the Flash part uses a 4 KB or 256-byte sector erase, then the GbE region size must be set to 8 KB.

The NVM image contains both static and dynamic data. The static data is the basic platform configuration, and includes OEM specific configuration bits as well as the unique Printed Circuit Board Assembly (PBA). The dynamic data holds the product's Ethernet Individual Address (IA) and Checksum. This file can be created in a simple text editor and follows the format shown in Appendix A, which provides examples of GbE Region NVM maps for ICH8/ICH9-based designs. Fast Ethernet (**82562V**) images are also provided.

1.3 EEUPDATE Utility

Intel has created an EEUPDATE utility that can be used to update the GbE region images during in-circuit programming. The tool uses two basic data files outlined in the following section (static data file and IA address file). The EEUPDATE utility is flexible and can be used to update the entire GbE region image or only the IA address of the LAN controller. In addition, it also corrects the GbE component checksum field after the region is modified (FTOOL does not have this ability). For more information on how to use EEUPDATE, refer to the `eeupdate.txt` file that is included with the EEUPDATE utility.

To obtain a copy of this program, contact your Intel representative.

1.3.1 Command Line Parameters

The DOS command format is as follows:

```
EEUPDATE Parameter_1 Parameter_2
```

where:

Parameter_1 = /D or /A

/D is used to update the entire GbE region image.

/A is used to update just the Ethernet Individual Address.

Parameter_2 = filename

In Example 1, Parameter_2 is `file1.eep`, which contains the complete NVM image in a specific format used to update the complete GbE region. All comments in the `.eep` file must be preceded by a semicolon (;).

Example 1. EEUPDATE /D file1.eep

In Example 1, Parameter 2 is `file2.dat`, which contains a list of IA addresses. The EEUPDATE utility finds the first unused address from this file and uses it to update the NVM. An address is marked used if it is followed by a date stamp. When the utility uses a specific address, a log file called eelog.dat is updated with that address. This updated file should be used as the `.dat` file for the next update.

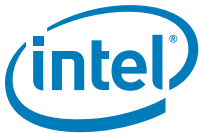
Appendix A provides an example of the raw GbE region contents. Fast Ethernet (**82562V**) images are also provided.

1.4 LAN NVM Format and Contents

Table 1 lists the NVM maps for the LAN region. Each word listed is described in detail in the following sections.

Table 1. LAN NVM Address Map

LAN Word Offset	NVM Byte Offset	HIgh Byte (Bits 15:8)	Low Byte (Bits 7:0)	Used By	Image Value
00h	00	Ethernet Individual Address Byte 2	Ethernet Individual Address Byte 1	HW-Shared	IA (2,1)
01h	02	Ethernet Individual Address Byte 4	Ethernet Individual Address Byte 3	HW-Shared	IA (4,3)
02h	04	Ethernet Individual Address Byte 6	Ethernet Individual Address Byte 5	HW-Shared	IA (6,5)
03h	06	Reserved		SW	0800h
04h	08	Reserved		SW	FFFFh
05h	0A	Image Version Information 1		SW	
06h	0Ch	Reserved		SW	FFFFh
07h	0Eh	Reserved		SW	FFFFh
08h	10h	PBA Low		SW	
09h	12h	PBA High		SW	
0Ah	14h	PCI Initialization Control Word		HW-PCI	
0Bh	16h	Subsystem ID		HW-PCI	
0Ch	18h	Subsystem Vendor ID		HW-PCI	
0Dh	1Ah	Device ID		HW-PCI	
0Eh	1Ch	Vendor ID		HW-PCI	
0Fh	1Eh	Device Rev ID (**ICH9**) Reserved (**ICH8**)		HW-PCI	
10h	20h	LAN Power Consumption		HW-PCI	
11h	22h	Reserved			
12h	24h	Reserved			
13h	26h	Shared Initialization Control Word		HW-Shared	
14h	28h	Extended Configuration Word 1		HW-Shared	
15h	2Ah	Extended Configuration Word 2		HW-Shared	
16h	2Ch	Extended Configuration Word 3		HW-Shared	
17h	2Eh	LEDCTL 1		HW-Shared	
18h	30h	LEDCTL 0 2		HW-Shared	
19h	32h	Future Initialization Word (**ICH8**) Future Initialization Word 1 (**ICH9**)		HW-Shared	0000h[1]
1Ah	34h	Future Initialization Word 2 (**ICH9**)		HW-Shared	0000h[1]



LAN Word Offset	NVM Byte Offset	HIgh Byte (Bits 15:8)	Low Byte (Bits 7:0)	Used By	Image Value
1Bh	36h	Reserved (**ICH9**)			
1Ch	38h	Reserved (**ICH9**)			294Ch[1]
1Dh	3Ah	Reserved (**ICH9**)			294Ch[1]
1Eh	3Ch	**82567MM** Device ID (**ICH9**)			10BEh
1Fh	3Eh	**82567MC** Device ID (**ICH9**)			10BFh
20h	40h	Reserved (**ICH9**)			294Ch
21h	42h	Reserved (**ICH9**)			294Ch
22h	44h	**82566DC** Device ID (**ICH9**)			10BDh
23h	46h	**82566DM** Device ID (**ICH9**)			294Ch
20h to 2Fh	34h to 5Eh	Reserved (**ICH8**)			
24h to 2Fh	48h to 5Eh	Reserved (**ICH9**)			
30h to 3Eh	60h to 7Dh	PXE Software Region		PXE	
3Fh	7Eh to 7Fh	Software Checksum (bytes 00h through 7Dh)		SW	

1. ICH9 only.

Notes:
1. SW = Software: This is access from the network configuration tools and drivers.
2. PXE = PXE Boot Agent: This is access from the PXE Option ROM code in BIOS.
3. HW-Shared = Hardware - Shared: This is read on when the Shared Configuration is reset.
4. HW-PCI = Hardware - PCI: This is read when the PCI Configuration is reset.
5. HW-PCIm = Hardware - PCIm: This is read when the PCIm Configuration is reset.

1.4.1 Ethernet Individual Address (Words 00h - 02h)

The Ethernet Individual Address (IA) is a six-byte field that must be unique for each adapter card or LOM and unique for each copy of the NVM image. The first three bytes are vendor specific. (For example, these bytes equal 00 AA 00 or 00 A0 C9 for Intel products.) The last three bytes must be unique for each copy of the NVM. OEM versions of the product might be required to have non-Intel ID's in the first three byte positions. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0). The Intel default is listed in Table 2.

Table 2. Ethernet Individual Address (Words 00h - 02h)

		Individual Address Byte					
		Word 00		Word 01		Word 02	
Manufacturer	MAC Address	Byte 2	Byte 1	Byte 4	Byte 3	Byte 6	Byte 5
Intel (original)	00AA00XXYYZZh	AAh	00h	XXh	00h	ZZh	YYh
Intel (new)	00A0C9XXYYZZh	A0h	00h	XXh	C9h	ZZh	YYh

Note: The Ethernet IA is byte swapped, as listed in Table 2.

The IA bytes read from the NVM are used by the ICH8/ICH9 until an IA Setup command is issued by software. The IA defined by the IA Setup command overrides the IA read from the NVM.

1.4.2 Reserved (Words 03h and 04h)

Table 3. Reserved (Words 03h and 04h)

Bit	Name	Default	Description
15:12	Reserved Word 03h	0000b	These bits are reserved and should be set to 0000b.
11	IBA LOM	1b	Must be set to 1b for Intel Boot Agent (IBA) to function correctly.
10:0	Reserved Word 03h	0h	These bits are reserved and should be set to 0h.
15:0	Reserved Word 04h	FFFFh	These bits are reserved and should be set to FFFFh.

1.4.3 Image Version Information (Word 05h)

Table 4. Image Version Information (Word 05h)

Bit	Name	Default	Description
15	Reserved	0b	This bit is reserved and should be set to 0b.
14:12	NVM Major Version	--	This field represents the LAN NVM major version number.
11:4	NVM Minor Version	--	This field represents the LAN NVM minor version number.
3:0	Image ID	2h	This field represents the NVM image identification. This field equals 2h (default) for the **82562V** PHY and 0h for the **82566/82567** PHY.

1.4.4 Reserved (Words 06h and 07h)

Table 5. Reserved (Words 06h and 07h)

Bit	Name	Default	Description
15:0	Reserved Word 06h	FFFFh	This field is reserved and should be set to FFFFh.
15:0	Reserved Word 07h	FFFFh	This field is reserved and should be set to FFFFh.

1.4.5 PBA Low, PBA High (Words 08h and 09h)

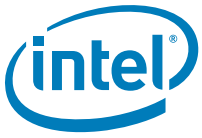
The nine digit printed board assembly (PBA) number used for Intel manufactured adapter cards are stored in a four-byte field. The dash and the first digit of the three-digit suffix are not stored.

1.4.5.1 PBA Example

If the PBA Number is “123456-003”

then word 08h = 1234h and word 09h = 5603h.

Through the course of hardware changes, the suffix field (byte 4) is incremented. The purpose of this information is to enable customer support (or any user) to identify the exact revision level of a product. The software device driver should not rely on this field to identify the product or its capabilities.



1.4.6 PCI Initialization Control (Word 0Ah)

This word contains initialization values that:

- Set defaults for some internal registers.
- Enable/disable specific features.
- Determine which PCI configuration space values are loaded from the NVM.

Table 6. Initialization Control Word (Word 0Ah)

Bit	Name	Default	Description
15:12	Reserved	0001b	This field is reserved and should be set to 0001b.
11:8	Reserved	0000b	These bits are reserved and should be set to 0000b.
7	AUX PWR	1b	This bit is used as an auxiliary power indication. It is used in conjunction with the *PM Enable* bit. 0b = D3cold wake-up is not advertised. 1b = D3cold wake-up is advertised in the PMC register of the PCI function if the *PM Enable* bit is also set.
6	PM Enable	1b	This bit enables the assertion of a PME in the PCI function at any power state. 0b = PME functionality is disabled. 1b = PME functionality is enabled. This bit affects the advertised PME_Support indication in the PMC register of the PCI function.
5:3	Reserved	00b	This bit is reserved and should be set to 00b.
2	APM Enable	1b	When APM Enable is set, both the PHY (**82566** or **82562V**) and the MAC should be initialized to a functional state following power up. 0b = APM functionality is disabled. 1b = APM functionality is enabled. **Note:** This is a reserved bit for the **ICH8** (B1 stepping) and the **ICH9**.
1	Load Subsystem IDs	1b	0b = Device loads the default PCI Subsystem ID and Subsystem Vendor ID. 1b = Device loads its PCIe* Subsystem ID and Subsystem Vendor ID from the NVM (words 0Bh and 0Ch).
0	Load Vendor/Device IDs	1b	0b = Device loads the default PCI Vendor and Device IDs. 1b = Device loads the default values for PCI Vendor and Device IDs from the NVM (words 0Dh and 0Eh).

1.4.7 Subsystem ID (Word 0Bh)

If Load Subsystem IDs bit of word 0Ah is set to 1b, this word is read in to initialize the Subsystem ID. The Subsystem ID default value is 0000h.

1.4.8 Subsystem Vendor ID (Word 0Ch)

If Load Subsystem IDs bit of word 0Ah is set to 1b, this word is read in to initialize the Subsystem Vendor ID. The Subsystem Vendor ID default value is 8086h.

1.4.9 Device ID (Word 0Dh)

If the *Load Vendor/Device IDs* bit in word 0Ah is set to 1b, this word is read to initialize the Device ID of the LAN function.

Table 7. Device IDs for Intel® Platform LAN Connects

Device ID	Adapter
1049h	Intel® **82566MM** Gigabit Ethernet Controller
104Ah	Intel® **82566DM** Gigabit Ethernet Controller
104Bh	Intel® **82566DC** Gigabit Ethernet Controller
104Ch	Intel® **82562V** 10/100 Mb/s Platform LAN Connect Device
104Dh	Intel® **82566MC** Gigabit Ethernet Network Controller
10BEh	Intel® **82567MM** Gigabit Ethernet Controller
10BFh	Intel® **82567MC** Gigabit Ethernet Controller

1.4.10 Vendor ID (Word 0Eh)

If the Load Vendor/Device IDs bit in word 0Ah is set to 1b, this word is read to initialize the Vendor ID. The default Vendor ID value is 8086h.

1.4.11 ICH9 Device Rev ID (Word 0Fh)

Table 8. ICH9 Device Rev ID (Word 0Fh)

Bit	Name	Default	Description
15:8	Reserved	00h	Reserved.
7:0	DEVREVID	00h	Device rev ID The actual device revision ID is the NVM value XORed with the default value of the **82567**.

1.4.12 LAN Power Consumption (Word 10h)

This word is only relevant when power management is enabled.

Table 9. LAN Power Consumption (Word 10h)

Bit	Name	Default	Description
15:8	LAN D0 Power	0Dh for **82566** 00h for **82567** 04h for **82562V**	The value in this field is reflected in the PCI Power Management Data Register of the LAN function for D0 power consumption and dissipation (Data_Select = 0 or 4). Power is defined in 100 mW units and includes the external logic required for the LAN function.
7:5	Reserved	000b	These bits are reserved and should be set to 000b.
4:0	LAN D3 Power	00001b for **82566** 00000h for **82567** 00010b for **82562V**	The value in this field is reflected in the PCI Power Management Data Register of the LAN function for D3 power consumption and dissipation (Data_Select = 3 or 7). Power is defined in 100 mW units and includes the external logic required for the LAN function. The most significant bits in the Data Register that reflects the power values are padded with zeros.

1.4.13 Shared Initialization Control (Word 13h)

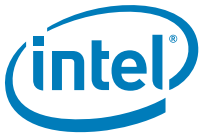
This word controls general initialization values.

Table 10. Shared Initialization Control (Word 13h)

Bit	Name	Default	Description
15:14	SIGN	10b	This is a 2-bit field indicating whether a valid NVM is present to the MAC. If this field does not equal 10b, the MAC does not read the NVM data and uses default values for device configuration. 00b = Invalid NVM. 01b = Invalid NVM. 10b = Valid NVM present. 11b = Invalid NVM.
13:12	Reserved	01b	These bits are reserved and should be set to 01b.
11	Ext Pwr Polarity	0b	This bit defines whether the LAN Power Control (LAN_PHYPC) signal is active high or active low. The LAN PHY Power Control signal can be used to shut off the power rails to the LAN connected device (only supported with the **82566/82567** PHY). LAN PHY Power Control is generally used for Intel® Auto Connect Battery Saver (ACBS) implementations on **82566** mobile SKUs. 0b = LAN PHY Power Control is active high. 1b = LAN PHY Power Control is active low. **Note:** For the **ICH9**, this bit is loaded to the *EXTPPOL* bit in the CTRL_EXT register.
10	Reserved	1b	Reserved. Always set to 1b.
9	PHY PD Enable	1b	For **ICH8** designs that support an ACBS implementation using LAN Power Control (LAN_PHYPC), this bit enables or disables PHY power down. 0b = PHY power down feature is disabled. 1b = PHY power down feature is enabled to power down at DMoff/ D3 without Wake on LAN. This bit is loaded to the *PHY Power Down Enable* bit in the CTRL_EXT register.

Table 10. Shared Initialization Control (Word 13h)

Bit	Name	Default	Description
8	Reserved	0b	This bit is reserved and should be set to 0b.
7:6	PHYT	00b	This field indicates the PHY device type. 00b = **82566**/**82567** PHY - GLCI mode 01b = Reserved 10b = **82562V** PHY - PCIe mode, LCI mode 11b = Reserved This field is reflected in the PHYTYPE field in the Status register.
5	D/UD Polarity	0b	This bit defines the polarity of the dock/undock indication as defined. 0b = GBEDOCKB pin value of 0 = dock; 1 = undock. 1b = GBEDOCKB pin value of 0 = undock; 1 = dock. This bit is loaded in the automatic read process to bit 14 of the Device Control register.
4	FRCSPD	0b	Force Speed Default setting for the *Force Speed* bit in the Device Control register (CTRL[11]). The hardware default value is 1b. **Note:** This is a reserved bit for the **82566** and **82562V**.
4:3	FD	0b	Duplex Setting Default setting for duplex setting. Mapped to CTRL[0]. The hardware default value is 1b. **Note:** This is a reserved bit for the **82566** and **82562V**.
2	CLK_CNT_1_16	1b	This bit is loaded to the CTRL_EXT.EnaKumCK16 bit and enables the reduction of the internal JCLK to one-sixteenth of the external NJCLK at the GLCI interface in Gigabit Ethernet mode. 0b = Reduction is disabled. 1b = Reduction is enabled.
1	CLK_CNT_1_4	1b 0b for **ICH9**	This bit enables the automatic reduction of DMA frequency. It is mapped to STATUS[31]. 0b = Automatic reduction disabled. 1b = Automatic reduction enabled.
0	Dynamic Clock Gating	1b	When set, this bit enables the dynamic clock gating of the DMA and MAC units. This bit is loaded to the *DynCK* bit in the CTRL_EXT register. **Note:** This is a reserved bit for the **82566** and **82562V** and should be set to 1b.



1.4.14 Extended Configuration Word 1 (Word 14h)

Table 11. Extended Configuration Word 1 (Word 14h)

Bit	Name	Default	Description
15	D/UD Enable	0b	In the **82566/82567** PHY, this bit enables the extended dock or undock configuration area in the MAC. It is loaded to the EXTCNF_CTRL register. This setting is only available for the **82566/82567** PHY when used in conjunction with the **ICH8M/ ICH9M** (Mobile **ICH8/ICH9**). **Note:** Contact your Intel Field Service Representative for information on implementing this feature. 0b = Extended Dock and Undock Configuration areas are ignored. 1b = Enables loading the Extended Dock or Undock Configuration area in the LAN controller. This bit is reserved for other devices and must be set to 0b in those components.
14	Reserved	1b	1b = **ICH8** (B0/B1 stepping). 0b = **ICH8** (A0 stepping). **Note:** For the **ICH9**, this is a reserved bit.
13	PHY Write Enable	1b	This bit loads the extended PHY configuration area in the MAC. It is loaded to the EXTCNF_CTRL register. 0b = Extended PHY configuration area is ignored. 1b = Enables the PHY configuration area in the MAC. **Note:** This bit is reserved for the **82566** and **82562V** when used with the **ICH8**. This bit should be set to 0b.
12	OEM Write Enable	1b	When set, enables auto load of the OEM bits from the PHY_CTRL register to the **82567**. It is loaded to the EXTCNF_CTRL register. **Note:** This bit is reserved for the **82566** and **82562V** and should be set to 1b.
11:0	Extended Configuration Pointer	020h	This field defines the base address (in Dwords) of the extended configuration area in the NVM. It should equal a non-zero value.

1.4.15 Extended Configuration Word 2 (Word 15h)

Table 12. Extended Configuration Word 2 (Word 15h)

Bit	Name	Default	Description
15:8	Extended PHY Length		• Desktop ICH8 with the **82566** = 38h. • Mobile ICH8m with the **82566** = 50h. • Desktop and mobile ICH9 with the **82566** = 3Bh. For the **82566/82567** PHY, if the extended PHY configuration area is disabled, the length must be set to 00h.
7:0	Reserved	00h	These bits are reserved and should be set to 00h.

1.4.16 Extended Configuration Word 3 (Word 16h)

Table 13. Extended Configuration Word 3 (Word 16h)

Bit	Name	Default	Description
15:8	Extended Dock Length	00h	This field identifies the size (in dwords) of the Extended Dock/ Undock Configuration area. For the **82566/82567** PHY, if the Extended Dock/Undock Configuration area is disabled, the length must be set to 00h.
7:0	Reserved	00h	These bits are reserved and should be set to 00h.

1.4.17 LED 1 Configuration and Power Management (Word 17h)

This field specifies the default values for the LEDCTL register fields controlling the LED1 (LINK_1000) output behaviors and the OEM fields defining the PHY power management parameters loaded to the PHY_CTRL register.

Table 14. LED 1 Configuration and Power Management (Word 17h)

Bit	Name	Default	Description
15	B2B Enable	1b	This bit enables Smart Power Down in back-to-back link setup. 0b = B2B disabled. 1b = B2B enabled.
14	GbE Disable	0b	For **ICH9**, when this bit is set, GbE operation is disabled in all power states (including D0a).
13:12	Reserved	00b	These bits are reserved and should be set to 000b.
11	GbE Disable in non-D0a	1b	For **ICH9**, this bit disables GbE operation in non-D0a states. This bit must be set since GbE is not supported in Sx mode by the platform. This is a reserved bit for the **82566**.
10	LPLU Enable in non-D0a	1b	The Low Power Link Up enables link at the lowest speed supported by both link partners in non-D0a states. This bit must be set if LPLU Enable bit is set. 0b = Low Power Link Up is disabled. 1b = Low Power Link Up is enabled in all non-D0a states.
9	LPLU Enable	0b	The Low Power Link Up enables link at the lowest speed supported by both link partners in all power states. This bit enables a decrease in link speed in all power states. 0b = Low Power Link Up is disabled. 1b = Low Power Link Up is enabled in all power states.
8	SPD Enable	1b	0b = PHY Smart Power Down mode is disabled. 1b = PHY Smart Power Down mode is enabled.
7	LED1 Blink	0b	This bit indicates the initial value of the LED1_BLINK field. 0b = LED1 is non-blinking (recommended). 1b = LED1 is blinking.
6	LED1 Invert	0b	This bit indicates the initial value of the LED1_IVRT field. 0b = LED1 has an active low output. 1b = LED1 has an active high output.

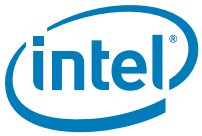


Table 14. LED 1 Configuration and Power Management (Word 17h)

5	LED1 Blink Mode	0b	This bit defines the LED1 blink mode: 0b = Blink at 200 ms on and 200 ms off (slow rate for **ICH9**). 1b = Blink at 83 ms on and 83 ms off (fast rate for **ICH9**). This field should be identical to LED0 Blink Mode.
4	Filtered ACT LED	0b	Enable Filtered Activity LED (while operating with the **82562V**) When set to 0b, the activity LED is activated by the PHY. when set to 1b, the activity LED is driven by Tx activity or Rx traffic that match any of the MAC's MAC addresses. For the **82566/82567**, this bit is reserved and should be set to 0b.
3:0	LED1 Mode	0111b	These bits represent the initial value of the LED1_MODE field, which specifies the event, state, or pattern displayed on LED1 (LINK_1000) output. Table 15 defines the values for LED1 Mode. A value of 0111b indicates that a 1000 Mb/s link is established and maintained.

The following table lists the LED modes defined in bits 3:0 of this word.

Table 15. LED Modes

Mode (Bits 3:0)	Selected Mode	Source Indication
0000b	LINK_10/1000	Asserted when either 10 Mb/s or 1000 Mb/s link is established and maintained.
0001b	LINK_100/1000	Asserted when either 100 Mb/s or 1000 Mb/s link is established and maintained.
0010b	LINK-UP	Asserted when any speed link is established and maintained.
0011b	FILTER_ACTIVITY	Asserted when link is established and packets are being transmitted or received that passed MAC filtering.
0100b	LINK/ACTIVITY	Asserted when link is established and when there is no transmit or receive activity.
0101b	LINK_10	Asserted when a 10 Mb/s link is established and maintained.
0110b	LINK_100	Asserted when a 100 Mb/s link is established and maintained.
0111b	LINK_1000	Asserted when a 1000 Mb/s link is established and maintained.
1000b	Reserved	Reserved.
1001b	FULL_DUPLEX	Asserted when the link is configured for full duplex operation.
1010b	COLLISION	Asserted when a collision is observed.
1011b	ACTIVITY	Asserted when link is established and packets are being transmitted or received.
1100b	BUS_SIZE	Asserted when the MAC detects a 1-lane PCIe* connection.
1101b	PAUSED	Asserted when the MAC transmitter is flow controlled.
1110b	LED_ON	Always asserted.
1111b	LED_OFF	Always de-asserted.

1.4.18 LED 0 and 2 Configuration Defaults (Word 18h)

This NVM word specifies the hardware defaults for the LEDCTL register fields controlling the LED0 (LINK_UP; LINK/ACTIVITY for **ICH9**) and LED2 (LINK_100) output behaviors.

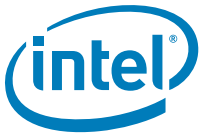
Table 16. LED 0 and 2 Configuration Defaults (Word 18h)

Bit	Name	Default	Description
15	LED2 Blink	0b	This bit indicates the initial value of the LED2_BLINK field. 0b = LED2 is non-blinking. 1b = LED2 is blinking.
14	LED2 Invert	0b	This bit indicates the initial value of the LED2_IVRT field. 0b = LED2 has an active low output. 1b = LED2 has an active high output.
13	LED2 Blink Mode	0b	This bit defines the LED2 blink mode: 0b = Blink at 200 ms on and 200 ms off (slow rate for **ICH9**). 1b = Blink at 83 ms on and 83 ms off (fast rate for **ICH9**). For **ICH8**, this field should be identical to the LED0 Blink Mode.
12	Reserved	0b	This bit is reserved and should be set to 0b.
11:8	LED2 Mode	0110b	These bits represent the initial value of the LED2_MODE field, which specifies the event, state, or pattern displayed on LED2 (LINK_100) output. A value of 0110b causes this to indicate 100 Mb/s operation.
7	LED0 Blink	1b	This bit indicates the initial value of the LED0_BLINK field. 0b = LED0 is non-blinking (recommended). 1b = LED0 is blinking.
6	LED0 Invert	0b	This bit indicates the initial value of the LED0_IVRT field. 0b = LED0 has an active low output. 1b = LED0 has an active high output.
5	LED0 Blink Mode	0b	This bit define the LED0 blink mode: 0b = Blink at 200 ms on and 200 ms off (slow rate for **ICH9**). 1b = Blink at 83 ms on and 83 ms off (fast rate for **ICH9**). For **ICH8**, this field initializes the GLOBAL_BLINK_MODE field in the LEDCTL register.
4	Reserved	0b	This bit is reserved and should be set to 0b.
3:0	LED0 Mode	0100b	These bits represent the initial value of the LED0_MODE field, which specifies the event, state, or pattern displayed on LED0 (Link/Activity; LINK_UP/Activity for **ICH9**) output. Table 15 defines the values for LED0 Mode.

Table 15, "LED Modes" above summarizes the LED modes defined in bits 3:0 of this word.

1.4.19 Future Initialization Word 1 (Words 19h)

Bit	Name	Default	Description
15:0	Reserved		Reserved This field is loaded to bits 15:0 of the FEXTNVM register. For the **82562V**, must be set to 301h. For **82566** SKUs that include ACBS, must be set to 181h. For **82566** SKUs without ACBS, must be set to 101h. For the **82567**, must be set to TBDF.



1.4.20 Future Init Word 2 (Word 1Ah)

For **ICH9**, This word is loaded to bits 31:16 of the FEXTNVM register.

Bit	Name	Default	Description
0	APM Enable	1	Initial value of *Advanced Power Management Wake Up Enable* in the *Wake Up Control Register* (WUC.APME). Also mapped to CTRL[6]. When the *APM Enable* bit is set, both the PHY and MAC should be initialized to a functional state following power up. This bit is also loaded to the FEXTNVM register (bit 16); however, the bit in the FEXTNVM does not impact the device functionality.
15:1	Reserved	00h	Reserved

For **ICH8**:

Bit	Name	Default	Description
15:0	Reserved	0800h	Reserved This field is loaded to bits 15:0 of the FEXTNVM register.

1.4.21 82567MM Device ID (Word 1Eh)

Bit	Name	Default	Description
15:0	**82567MM** DeviceID	10BEh	**82567** Mobile Consumer DeviceID ICH9 Device ID on PCI configuration space when the PHY is the 82567MM.

1.4.22 82567MC Device ID (Word 1Fh)

Bit	Name	Default	Description
15:0	**82567MC** DeviceID	10BFh	**82567** Mobile Corporate DeviceID ICH9 Device ID on PCI configuration space when the PHY is the 82567MC.

1.4.23 82566DC Device ID (Word 22h)

Bit	Name	Default	Description
15:0	**82566DC** DeviceID	10BDh	**82566** Desktop Corporate DeviceID **ICH9** Device ID on PCI configuration space when the PHY is the **82566DC**.

1.4.24 82566DM Device ID (Word 23h)

Bit	Name	Default	Description
15:0	**82566DM** DeviceID	294Ch	**82566** Desktop Consumer DeviceID **ICH9** Device ID on PCI configuration space when the PHY is the **82566DM**.

1.4.25 PXE Words (Words 30h - 3Eh)

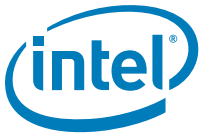
Words 30h through 3Eh (bytes 60h through 7Dh) have been reserved for configuration and version values to be used by PXE code.

1.4.25.1 Boot Agent Main Setup Options (Word 30h)

The boot agent software configuration is controlled by the NVM with the main setup options stored in word 30h. These options are those that can be changed by using the Control-S setup menu or by using the IBA Intel Boot Agent utility. Note that these settings only apply to Boot Agent software.

Table 17. Boot Agent Main Setup Options

Bit	Name	Description
15	PPB	PXE Presence. Setting this bit to 0b Indicates that the image in the Flash contains a PXE image. Setting this bit to 1b indicates that no PXE image is contained. The default for this bit is 0b for backwards compatibility with existing systems already in the field. If this bit is set to 0b, EEPROM word 32h (PXE Version) is valid. When EPB is set to 1b and this bit is set to 0b, indicates that both images are present in the Flash.
14	EPB	EFI Presence. Setting this bit to 1b Indicates that the image in the Flash contains an EFI image. Setting this bit to 0b indicates that no EFI image is contained. The default for this bit is 0b for backwards compatibility with existing systems already in the field. If this bit is set to 1b, EEPROM word 33h (EFI Version) is valid. When PPB is set to 0b and this bit is set to 1b, indicates that both images (PXE and EFI) are present in the Flash.
13	Reserved	Reserved for future use. This bit must be set to 0b.
12	FDP	Force Full Duplex. Set this bit to 0b for half duplex and 1b for full duplex. Note that this bit is a don't care unless bits 10 and 11 are set.
11:10	FSP	Force Speed. These bits determine speed. 01b = 10 Mb/s 10b = 100 Mb/s 11b = Not allowed. All zeros indicate auto-negotiate (the current bit state). Note that bit 12 is a don't care unless these bits are set.
9	Reserved	Reserved Set this bit to 0b.



Bit	Name	Description
8	DSM	Display Setup Message. If this bit is set to 1b, the "Press Control-S" message appears after the title message. The default for this bit is 1b.
7:6	PT	Prompt Time. These bits control how long the "Press Control-S" setup prompt message appears, if enabled by DIM. 00b = 2 seconds (default) 01b = 3 seconds 10b = 5 seconds 11b = 0 seconds Note that the Ctrl-S message does not appear if 0 seconds prompt time is selected.
5	Reserved	Reserved
4:3	DBS	Default Boot Selection. These bits select which device is the default boot device. These bits are only used if the agent detects that the BIOS does not support boot order selection or if the MODE field of word 31h is set to MODE_LEGACY. 00b = Network boot, then local boot 01b = Local boot, then network boot 10b = Network boot only 11b = Local boot only
2	Reserved	Reserved
1:0	PS	Protocol Select. These bits select the boot protocol. 00b = PXE (default value) 01b = RPL protocol Other values are undefined.

1.4.25.2 Boot Agent Configuration Customization Options (Word 31h)

Word 31h contains settings that can be programmed by an OEM or network administrator to customize the operation of the software. These settings cannot be changed from within the Control-S setup menu or the IBA Intel Boot Agent utility. The lower byte contains settings that would typically be configured by a network administrator using the Intel Boot Agent utility; these settings generally control which setup menu options are changeable. The upper byte are generally settings that would be used by an OEM to control the operation of the agent in a LOM environment, although there is nothing in the agent to prevent their use on a NIC implementation.

Table 18. Boot Agent Configuration Customization Options (Word 31h)

Bit	Name	Description
15:14	SIG	Signature. These bits must be set to 01b to indicate that this word has been programmed by the agent or other configuration software.
13:11	Reserved	Reserved for future use. All bits must be set to 0b.
10:8	MODE	Selects the agent's boot order setup mode. This field changes the agent's default behavior in order to make it compatible with systems that do not completely support the BBS and PnP Expansion ROM standards. Valid values and their meanings are: 000b = Normal behavior. The agent attempts to detect BBS and PnP Expansion ROM support as it normally does. 001b = Force Legacy mode. The agent does not attempt to detect BBS or PnP Expansion ROM supports in the BIOS and assumes the BIOS is not compliant. The BIOS boot order can be changed in the Setup Menu. 010b = Force BBS mode. The agent assumes the BIOS is BBS-compliant, even though it may not be detected as such by the agent's detection code. The BIOS boot order CANNOT be changed in the Setup Menu. 011b = Force PnP Int18 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 18h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu. 100b = Force PnP Int19 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 19h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu. 101b = Reserved for future use. If specified, treated as value 000b. 110b = Reserved for future use. If specified, treated as value 000b. 111b = Reserved for future use. If specified, treated as value 000b.
7:6	Reserved	Reserved for future use. These bits must be set to 0b.
5	DFU	Disable Flash Update. If set to 1b, no updates to the Flash image using PROSet is allowed. The default for this bit is 0b; allow Flash image updates using PROSet.
4	DLWS	Disable Legacy Wakeup Support. If set to 1b, no changes to the Legacy OS Wakeup Support menu option is allowed. The default for this bit is 0b; allow Legacy OS Wakeup Support menu option changes.
3	DBS	Disable Boot Selection. If set to 1b, no changes to the boot order menu option is allowed. The default for this bit is 0b; allow boot order menu option changes.

Bit	Name	Description
2	DPS	Disable Protocol Select. If set to 1b, no changes to the boot protocol is allowed. The default for this bit is 0b; allow changes to the boot protocol.
1	DTM	Disable Title Message. If set to 1b, the title message displaying the version of the boot agent is suppressed; the Control-S message is also suppressed. This is for OEMs who do not want the boot agent to display any messages at system boot. The default for this bit is 0b; allow the title message that displays the version of the boot agent and the Control-S message.
0	DSM	Disable Setup Menu. If set to 1b, no invoking the setup menu by pressing Control-S is allowed. In this case, the EEPROM can only be changed via an external program. The default for this bit is 0b; allow invoking the setup menu by pressing Control-S.

1.4.25.3 Boot Agent Configuration Customization Options (Word 32h)

Word 32h is used to store the version of the boot agent that is stored in the Flash image. When the Boot Agent loads, it can check this value to determine if any first-time configuration needs to be performed. The agent then updates this word with its version. Some diagnostic tools to report the version of the Boot Agent in the Flash also read this word. This word is only valid if the PPB is set to 0b. Otherwise the contents might be undefined.

Table 19. Boot Agent Configuration Customization Options (Word 32h)

Bit	Name	Description
15:12	MAJOR	PXE boot agent major version. The default for these bits is 0b.
11:8	MINOR	PXE boot agent minor version. The default for these bits is 0b.
7:0	BUILD	PXE boot agent build number. The default for these bits is 0b.

1.4.25.4 IBA Capabilities (Word 33h)

Word 33h is used to enumerate the boot technologies that have been programmed into the Flash. It is updated by IBA configuration tools and is not updated or read by IBA.

Table 20. IBA Capabilities

Bit	Name	Description
15:14	SIG	Signature. These bits must be set to 01b to indicate that this word has been programmed by the agent or other configuration software.
13:5	Reserved	Reserved for future use. All bits must be set to 0b.
4	SAN	SAN capability is present in Flash. 0b = The SAN capability is not present (default). 1b = The SAN capability is present.
3	EFI	EFI UNDI capability is present in Flash. 0b = The RPL code is not present (default). 1b = The RPL code is present.
2	RPL	RPL capability is present in Flash. 1b = The RPL code is present (default). 0b = The RPL code is not present.
1	UNDI	PXE/UNDI capability is present in Flash. 1b = The PXE base code is present (default). 0b = The PXE base code is not present.
0	BC	PXE base code is present in Flash. 0b = The PXE base code is present (default). 1b = The PXE base code is not present.

1.4.26 Checksum (Word 3Fh)

The Checksum word (NVM bytes 7Eh and 7Fh) is used to ensure that the base NVM image is valid. Its value should be calculated by adding all words (00h through 3Fh)/ bytes (00h-7Eh), including the Checksum word itself. The sum, including the Checksum, should equal BABAh. The initial value before the values are added together should be 0000h, and the carry bit should be ignored after each addition. If the OEM does not desire to calculate the checksum, LAD programming tools and drivers will detect if the checksum is incorrect and fix it in the image.

Note: The default image always has a checksum value of 0. The default image always has a checksum value of 0b. The LAD programming tools (EEUPDATE or LANCONF) update the checksum when the image is programmed.

1.5 ICH9 Extended Configuration

Table 21 lists the contents of the extended configuration area. The base address for this area is contained in the Extended Configuration Pointer. Each entry is defined as a Dword, where the LSBs [15:0] occupy the lower-address word.

Table 21. NVM Map - Extended Configuration

Word Address (relative to base address)	Used By	15:8	7:0
00h 01h	HW	PHY Extended Configuration Dword 0	
…	HW	…	
(2(N-1))h (2N-1)h	HW	PHY Extended Configuration Dword (N-1)[1]	
(2N)h (2N+1)h	HW	Dock Extended Configuration Dword 0	
…	HW	…	
(2N+2L-2)h (2N+2L-1)h	HW	Dock Extended Configuration Dword (L-1)[2]	
(2N+2L)h (2N+2L+1)h	HW	Undock Extended Configuration Dword 0	
…	HW	…	
(2N+4L-2)h (2N+4L-1)h	HW	Undock Extended Configuration Dword (L-1)[3]	

1. N = number of PCIe* Dwords as determined in the *Extended PCIe* Length* field.
2. M = number of PHY Dwords as determined in the *Extended PHY Length* field.
3. L = number of Dock/Undock Dwords as determined in the *Extended Dock Length* field.

Note: The extended configuration space in the NVM must not set the PHY reset bit in PHY Control register (bit 15). If set, the PHY enters an internal initialization loop.

1.5.1 PHY Extended Configuration (Words 00h – (2N-1)h From Base)

There are N valid Dwords in this range, where N = number of PHY Dwords as determined in the *Extended LCD Length* field. Table 22 lists the structure of each Dword.

Table 22. PHY Extended Configuration (Words 00h – (2N-1)h From Base)

Bit	Name	Default	Description
31:21	Reserved	00h	Reserved
20:16	Register	00h	Contains the address of the PHY register to write to. A value of 1Fh indicates that this is a command to switch to another MDIO page.
15:0	Data	00h	Data to be written to the PHY register. When the register field above equals 1F, the *Data* field indicates the page number to switch to. Note that the page number should be programmed to the 11 MSB while bits 4:0 should be set to 00h.

1.5.2 Dock Extended Configuration (Words (2N)h – (2N+2L-1)h From Base)

There are L valid Dwords in this range, where L = number of Dock Dwords as determined in the *Extended Dock Length* field. The structure of each entry is the same as in the PHY Extended Configuration listed in Table 22.

1.5.3 Undock Extended Configuration (Words (2N+2L)h – (2N+4L-1)h From Base)

There are L valid Dwords in this range, where L = number of Undock Dwords as determined in the *Extended Dock Length* field. The structure of each entry is the same as in the PHY Extended Configuration listed in Table 22.

Appendix A ICH8/ICH9 NVM Contents

This section contains the NVM contents for the ICH8/ICH9. All values are in hexadecimal.

Table 23. LAN NVM Contents

Word	Description
00:02h	Ethernet Individual Address
03:04h	Reserved
05h	Image Version Information 1
06:07h	Reserved
08:09h	PBA Bytes
0Ah	PCI Initialization Control Word
0Bh	Subsystem ID
0Ch	Subsystem Vendor ID
0Dh	Device ID
0Eh	Vendor ID
0Fh	Device Revision ID (**ICH9**); Reserved (**ICH8**)
10h	LAN Power Consumption
11:12h	Reserved
13h	Shared Initialization Control Word
14:16h	Extended Configuration Words
17:18h	LEDCTRL Words
19h	Future Initialization Word (**ICH8**); Future Initialization Word 1 (**ICH9**)
1Ah	Future Initialization Word 2 (**ICH9**)
1Bh:1Dh	Reserved (**ICH9**)
1Eh	**82567MM** Device ID (**ICH9**)
1Fh	**82567MC** Device ID (**ICH9**)
20:21h	Reserved (**ICH9**)
22h	**82566DC** Device ID (**ICH9**)
23h	**82566DM** Device ID (**ICH9**)
20:2Fh	Reserved (**ICH8**)
24:2Fh	Reserved (**ICH9**)
30:3Eh	PXE Region
3Fh	Software Checksum

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