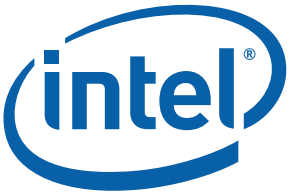

Intel® Ethernet Network Connection I347-AT4

Networking Division (ND)

Revision 1.2
September 2013

Legal

Revisions

Date	Revision	Description
January 2013	1.0	Initial release (Intel Public).
September 2013	1.1	Added erratum #10.
September 2013	1.2	Revised erratum #10.

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1. Introduction

This document applies to the Intel® Ethernet Controller Connection I347-AT4 (I347-AT4).

This document is an update to a published specification, the *Intel® Ethernet Controller Connection I347-AT4 Datasheet*. It is intended for use by system manufacturers and software developers. All product documents are subject to frequent revision and new order numbers may apply. New documents may be added. Be sure you have the latest information before finalizing your design.

1.1 Product Code and Device Identification

Product Code: G16778-001

The following tables and drawings describe the various identifying markings on each device package:

Table 1-1. Markings

Device	Stepping	Top Marking	Q-Specification	Description
I347-AT4	A0	G16778-001	N/A	Pre-production (limited).
I347-AT4	A0	G16778-001	QNGC	Pre-production
I347-AT4	A0	TBD	N/A	Production

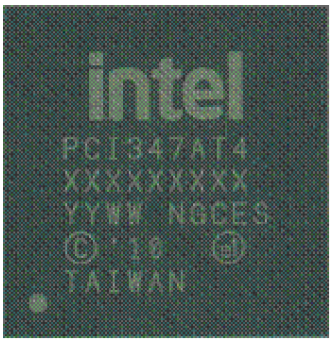
Table 1-2. Device ID

I347-AT4 Device ID Code	Vendor ID	Device ID	Revision ID
Intel® PCI347AT4 Gigabit Ethernet PHY, Quad Port	8086	0438	0

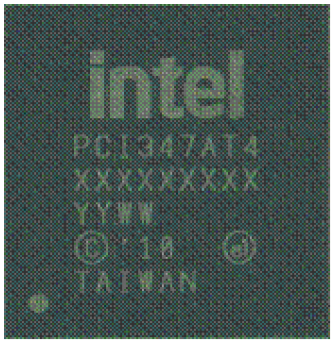
Table 1-3. MM Numbers

Product	Tray MM#	Tape and Reel MM#	Reserved
G16778-001	911237		
G16778-001	914097		

1.2 Marking Diagram



Engineering Mark



Production Mark

1.3 Nomenclature Used In This Document

This document uses specific terms, codes, and abbreviations to describe changes, errata, sightings and/or clarifications that apply to silicon/steppings. See Table 1-4 for a description.

Table 1-4. Nomenclature

Name	Description
Specification Changes	Modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
Errata	Design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.
Sightings	Observed issues that are believed to be errata, but have not been completely confirmed or root caused. The intention of documenting sightings is to proactively inform users of behaviors or issues that have been observed. Sightings may evolve to errata or may be removed as non-issues after investigation completes.
Specification Clarifications	Greater detail or further highlights concerning a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
Documentation Changes	Typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
A1, B1, etc.	Stepping to which the status applies.
Doc	Document change or update that will be implemented.
Fix	This erratum is intended to be fixed in a future stepping of the component.
Fixed	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.
Red Change Bar/ or Bold	This item is either new or modified from the previous version of the document.

2. Hardware, Clarifications, Changes, Updates and Errata

See Section 1.3 for an explanation of terms, codes, and abbreviations.

Table 2-1. Summary of Clarifications, Changes and Errata; Errata Include Steppings

Specification Clarifications	Status
1. PHY Initialization #1	N/A
2. PHY Initialization #2	N/A
3. DTE and Cable Detector TDR	N/A
4. Forced Modes and Sleep Modes	N/A
5. Link Drop to Interrupt Delay	N/A
6. IEEE Test Modes	N/A
7. Mode Change Matrix	N/A
8. INTn Pull-up Resistor and VDDOL	N/A
9. LED Behavior at Hardware-reset	N/A
10. Px_S_INP/N and Px_S_OUTP/N Polarity	N/A
11. Read/Write Access to Register 29 - 31	N/A
12. Using Oscillator/Clock Buffer to the XTAL_IN	N/A
13. MAC Loopback Speed-up for Manufacturing Tests	N/A
Specification Changes	**Status**
None.	
Documentation Updates	**Status**
None.	N/A
Errata	**Status**
1. LEDs Driven High and Cannot be Forced/Overridden During Hardware-reset, Software-reset, and Power-down Mode	A0-Yes; No Fix
2. System Interface Loopback in /SGMII Media Mode Requires Link to be Up	A0-Yes; No Fix
3. SGMII Interface Lockup	A0-Yes; No Fix
4. Cable Detector in First Peak Mode or Alternate Cable Detector Control	A0-Yes; No Fix
5. CRC Error Counter Showed an Error When Enabled While Traffic is Running	A0-Yes; No Fix
6. Wider Operating Temperature Range	A0-Yes; No Fix
7. 10BASE-T IEEE-Specific Harmonic Content Level Issue	A0-Yes; No Fix
8. 100BASE-TX Marginal Rise/Fall Time Performance	A0-Yes; No Fix
9. 1000BASE-T Cable Length	A0-Yes; No Fix
10. I347 Might Not Respond Correctly to the First Read of the MDIO Interface	A0-Yes; No Fix

2.1 Specification Clarifications

1. PHY Initialization #1

PHY initialization #1 can be implemented in any order.

The following registers must be written once after a hard reset, de-asserted for PHY initialization.

- Write register 22 = 0x00FF (set register 22 page to 0x00FF)
- Write register 24 = 0x2800
- Write register 23 = 0x2001
- Write register 22 = 0x0000 (set register 22 page to 0x0000)

To verify whether the register has been written correctly, do the following:

- Write register 22 = 0x00FF (set register 22 page to 0x00FF)
- Write register 23 = 0x1001
- Read register 25 = (must return 0x2800)
- Write register 22 = 0x0000 (set register 22 page to 0x0000)

2. PHY Initialization #2

The following registers must be written once after a hard reset, de-asserted for PHY initialization.

- Write register 22 = 0x0000 (set register 22 page to 0x0000)
- Write register 29 = 0x0003 (set register 29 page to 0x0003)
- Write register 30 = 0x0002
- Write register 29 = 0x0000 (set register 29 page to 0x0000)

To verify whether the register has been written correctly, do the following:

- Write register 22 = 0x0000 (set register 22 page to 0x0000)
- Write register 29 = 0x0003 (set register 29 page to 0x0003)
- Read register 30 = (must return 0x0002)
- Write register 29 = 0x0000 (set register 29 page to 0x0000)

3. DTE and Cable Detector TDR

When running the cable detector TDR test, disable the DTE detect feature. Once the cable detector TDR test completes, you can enable the DTE detect. This is because both features send test pulses, which might interfere with each other.

4. Forced Modes and Sleep Modes

When placing the port into 10 Mb/s or 100 Mb/s forced mode of operation, disable the energy detect (sleep mode) feature. The energy detect (sleep mode) feature should only be used if copper auto-negotiation is enabled.

5. Link Drop to Interrupt Delay

The IEEE 802.3 Clause 40 standard specifies that each time the PHY loses link due to a link dropping event like unplugging the cable, there is a delay from the time the link dropping event occurs to the time the link status actually de-asserts and thus the time the interrupt asserts. This delay varies according to the link speed as follows:

- For 10 Mb/s mode: 125 ms delay
- For 100 Mb/s mode: 5 µs delay
- For 1000 Mb/s mode: 750 ms delay

In some applications, such as in metro Ethernet applications, a fast failover in 50 ms is specified, which cannot be met if the PHY follows the 750 ms wait time.

The device can be programmed to enable faster GbE link down delay through register settings. If register 26_0.9 is set to 1b, it enables faster GbE link down time; otherwise it follows IEEE GbE link down requirements. If faster GbE link down time is enabled, register 26_0.11:10 bits control the GbE link down delay time to 0 ms, 10 ms ± 2 ms, 20 ms ± 2 ms, or 40 ms ± 2 ms.

6. IEEE Test Modes

Register bits 9.15:13 are used to select one of the four IEEE 802.3ab test modes. The PHY can be configured to provide a TX_TCLK signal that can be used for device testing purposes. The TX_TCLK signal is driven from the HSDACP pin.

When TX_TCLK output is enabled on more than one port, the port that has the highest physical address value drives the HSDACP pin. For example, if port 2 and port 1, enable TX_TCLK, HSDACP pin output reflects TX_TCLK output of port 2.

Test Mode 1, 2, or 4:

- Write register 22 = 0x0000 - set register 22 page to 0x0000
- Write register 9 = 0x1F00 - set PHY to master mode
- Write register 0 = 0x8140 - soft-reset
- Write register 29 = 0x0007 - set register 29 page to 0x0007 (register 30 and 31 page)
- Write register 30 = 0x0008 - set PHY to 1000 Mb/s mode
- Write register 22 = 0x0006 - points to page 6 (register 0 to 28)
- Write register 26 = 0x8000 - enable TX_TCLK

- For test mode 1: write register 9 = 0x3F00
- For test mode 2: write register 9 = 0x5F00
- For test mode 4: write register 9 = 0x9F00
- Take desired measurements. Restore normal values to register 9 and exit the test mode by clearing bits 9.15:13
- Write register 0 = 0x9140 - soft-reset

Test Mode 3:

- Write register 22 = 0x0000 - set register 22 page to 0x0000
- Write register 9 = 0x1700 - set PHY to slave mode
- Write register 0 = 0x8140 - soft-reset
- Write register 29 = 0x0007 - points to page 7 (register 30 and 31)
- Write register 30 = 0x0008 - set PHY to 1000 Mb/s mode
- Write register 22 = 0x0006 - points to page 6 (register 0 to 28)
- Write register 26 = 0x8000 - enable TX_TCLK
- Write register 9 = 0x7700 - enable test mode 3
- Take desired measurements. Restore normal values to register 9 and exit the test mode by clearing bits 9.15:13
- Write register 0 = 0x9140 - soft-reset

7. Mode Change Matrix

The device mode of operation can be changed through MDC/MDIO register writes to register 20_6.2:0 (MODE[2:0]) followed by mode soft-reset (register 20_6.15). When changing the mode through register access, some of the registers might need to be set manually as listed in Table 2-1.

Table 2-1. Mode Change Matrix

Hard Config →	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
Soft Config ↓								
000	N/A	OK	OK	OK	OK	OK	OK	OK
001	OK	N/A	OK	OK	OK	OK	OK	OK
010	OK	OK	N/A	OK	OK	OK	OK	OK
011	OK	OK	OK	N/A	OK	OK	OK	OK
100	OK	OK	OK	OK	N/A	OK	OK	OK
101	OK	OK	OK	OK	OK	N/A	OK	OK
110	OK	OK	OK	OK	OK	OK	N/A	OK
111	OK	OK	OK	OK	OK	OK	OK	N/A

8. INTn Pull-up Resistor and VDDOL

INTn pin is an open-drain output. The pull-up resistor used for the INTn must be connected to the VDDOL level. The pull-up resistor should not be connected to voltage higher than VDDOL.

9. LED Behavior at Hardware-reset

PDOWN (CONFIG[2] Bit[0]) device hardware configuration bit affects the LED behavior when hardware reset is asserted.

PDOWN = 0b, LEDs blink for 100 ms after the hardware-reset deasserted.

PDOWN = 1b, LEDs do not blink. All the ports are in powered-down mode after hardware-reset deasserted.

10. Px_S_INP/N and Px_S_OUTP/N Polarity

Reg 15_254.15 controls S_INP/N polarity. 0b = Invert. 1b = normal (default).

Reg 15_254.14 controls S_OUTP/N polarity. 0b = Invert. 1b = normal (default).

The polarity of the Px_S_INP/N and Px_S_OUTP/N can be inverted with the following procedure:

- Write register 22 = 0x00FE (set register 22 page to 0x00FE)
- Write register 15_254.15 = 0b (Invert S_INP/N), or/and write register 15_254.14 = 0b (Invert S_OUTP/N)
- Write register 22 = 0x0000 (set register 22 page to 0x0000)

11. Read/Write Access to Register 29 - 31

Register 22 must be set to 0x0000 before reading and writing from/to register 29, 30, and 31.

12. Using Oscillator/Clock Buffer to the XTAL_IN

XTAL_IN should be left floating when it is not used. When XTAL_IN is driven directly from the oscillator or clock buffer, this pin should be ac-coupled with a 0.1 nF capacitor. No additional AC capacitor is needed if a capacitor divider is already used for level shifting.

13. MAC Loopback Speed-up for Manufacturing Tests

The device supports MAC interface loopback (0_0.14 = 1b) mode for diagnostic purposes and manufacturing testing. If the MAC loopback testing is done during the time when the link is up/coming up, the packets sent from the MAC interface might be lost. The PHY takes a few seconds to bring the link down and perform MAC loopback. If the MAC loopback is enabled when the link is down or without a cable connected, there should be no issue with looping back packets. MAC side loopback operates correctly when the link speed is 10/100 Mb/s.

There are two possible workarounds to shorten the diagnostic MAC side loopback testing time. Note that it is important that these workarounds are applicable only when the diagnostic MAC loopback is enabled. This does not affect the normal mode of operation.

Option 1: Add a 1.5 second delay after the MAC loopback is enabled:

Write register 22 = 0x0000 `/* Set Page number to 0b`

Set register 0.14 = 1b `/* Enable MAC loop-back`

Wait 1.5 seconds
```
/* Add 1.5 seconds delay before sending packets from MAC interface to
/* ensure link partner stops idle transmission
```

Send and receive packets on the MAC interface

Set Reg 0.14 = 0b `/* Disable MAC loopback`

Resume normal operation.

Option 2: Use the following register writes to immediately send packets after the MAC loopback is enabled:

Write register 22 = 0x00FA `/* Set Page number to 250`

Write register 29 = 0x0001 `/* Set Page number to 1 to access through Register 30`

Write register 30 = 0x0418
```
/* Disable PHY's receiver to ignore incoming
idles from the link partner
```

Set Reg 0.14 = 1b `/* Enable MAC loopback`

```
/* Disable workaround
```

Write Reg 22 = 0x0000

Write Reg 29 = 0x0001

Write Reg 30 = 0x0400

Set Reg 0.14 = 0b `/* Disable MAC loopback`

Resume normal operation.

2.2 Specification Changes

None.

2.3 Documentation Updates

None.

2.4 Errata

Note: If the errata applies to a stepping, "Yes" is indicated for the stepping (for example: "A0=Yes" indicates errata applies to stepping A0). If the errata does not apply to the stepping, "No" is indicated (for example: "A0=No" indicates the errata does not apply to stepping A0).

1. LEDs Driven High and Cannot be Forced/Overridden During Hardware-reset, Software-reset, and Power-down Mode

Problem: When the PHY is in hardware-reset, software reset, or powered down mode, the LED pins are driven high and cannot be forced/overridden.

Implication: For applications that use active-low LEDs, this is not an issue as the LEDs are driven to an inactive state.

For applications that use active-high LEDs, the LEDs react to the following behavior:

- Hardware-reset: When a hardware-reset is asserted, the LEDs are turned on until the hardware-reset is de-asserted. If this is an issue, use active-low LEDs.
- Software-reset: When the software-reset is set (register 0.15 = 1b), the LEDs are briefly driven high. However, since the period is very short, it is not visible to the human eye and therefore a non-issue.
- Power-down (register 0.11): When the device enters power-down mode, the LEDs are turned on. Note that a software workaround is available.

Workaround: For applications that use active-high LEDs, the following procedure can be used to force the LED pins to drive low (LED turned off) when entering power-down mode.

- Write register 22 = 0x0000 (set register 22 page to 0x0000)
- Write register 29 = 0x0000 (set register 29 Page to 0x0000)
- Write register 30 = 0x0020
- Write register 0_0.11 = 1b (copper media power down)

When exiting power-down state, do the following

- Write register 22 = 0x0000 (set register 22 page to 0x0000)
- Write register 29 = 0x0000 (set register 29 page to 0x0000)
- Write register 30 = 0x0000
- Write register 0_0.11 = 0b (copper media power up)

Status: A0=Yes; No Fix

2. System Interface Loopback in /SGMII Media Mode Requires Link to be Up

Problem: In SGMII media mode, system interface loopback requires the SGMII link to be up or register 16_1.3 = 1b.

Implication: System interface looback cannot be ran if the link is not up.

Workaround: If the SGMII link is not up and register 16_1.3 = 0b, do the following:

- Write register 16_1.3 = 1b followed by register 0_1.15 = 1b (soft-reset)
- Enable system interface loopback (register 0_1.14 = 1b)

Status: A0=Yes; No Fix

3. SGMII Interface Lockup

Problem: The SGMII interface can lockup occasionally after hard-reset de-asserted or when the SGMII interface is powered down and up.

Implication: Occasional SGMII interface lockup.

The SGMII interface can be powered down in the following scenarios:

- SGMII interface manual power down (register 0_1.11)
- If the MAC/system *Interface Power Down* bit = 0b (register 16_2.3), the SGMII interface can be powered down. This scenario applies if the MAC/system interface is the SGMII interface.
- If register 16_2.3 = 0b (MAC interface can be powered down) and the register 0_0.11 (copper interface power down) is set to 1b, the MAC interface is powered down.
- If register 16_2.3 = 0b (MAC interface can be powered down) and energy detect mode is enabled (register 16_0.9:8 = 10b, 11b), the port enters into the sleep mode after there is no energy detected on the copper interface for five seconds. When the port enters the energy detect/sleep state, the MAC interface is powered down.

Workaround: This workaround checks the SGMII interface sync bit. If the sync bit is good, the workaround is skipped.

- The following workaround must be implemented to all ports of the PHY that uses the SGMII interface after hard-reset de-asserted or when the SGMII interface is powered down and up (register 0_1.11 is set to 1b and then 0b):

  For i = 1 to 5

```
{
Write Register 22 =0x0001  // Change Page Register to Page 1
If Register 17.5=1         // If SGMII sync is good, exit the for loop and continue traffic test.
         Exit;
Else                       // If SGMII sync is not good, continue the workaround procedure
// (Power down the PHY)
Write Register 22 (decimal) = 0x0000
Write Register 0 (decimal) = 0x1940
// (Reset PCS digital logic - copper side )
Write Register 29 (decimal) = 0x001D
Write Register 30 (decimal) = 0xEF00
```

```
// (Reset PCS digital logic - SGMII side )

Write Register 22 (decimal) = 0x00FE
Write Register 26 (decimal) = 0x803F

// (Reset PLL and RX)

Write Register 24 (decimal) = 0x9300 (Reset PLL and RX)
Write Register 24 (decimal) = 0x9100 (Release PLL reset)
Write Register 24 (decimal) = 0x8100 (Release RX reset)
Write Register 24 (decimal) = 0x0000 (Disable override)
Wait 5ms

// (De-assert PCS reset - SGMII side )

Write Register 26 (decimal) = 0x8000
Write Register 26 (decimal) = 0x0000
Write Register 22 (decimal) = 0x0000

// (De-assert PCS reset- copper side)

Write Register 29 (decimal) = 0x001D

Write Register 30 (decimal) = 0x0000

// (Release PHY port from Power down mode)

Write Register 22 (decimal) = 0x0000 // (if not already page 0)
Write Register 0 (decimal) = 0x9140 // (Power up device and soft reset)
Wait 100ms.
Write Register 22 (decimal) = 0x0001 // change back to page 1

i++;

} // go to beginning of For loop

} // end of for loop for all the ports.
```

- MAC interface power down (register 16_2.3) and the MAC/system interface is SGMII. The default value for register 16_2.3 is 1b (MAC/system interface always powered up). For this revision, this bit must not be set to 0b. In this case, the MAC interface is always powered up even in low-power mode (copper interface power down or energy detect/sleep mode). No additional workaround is required (except after hard-reset or SGMII interface manual power down and up).
- Auto-media detect (MODE[2:0 = 110b, 111b) with first media link up or copper preferred applications.
- When the copper link is up, the SGMII interface is powered down to conserve power. When the copper link is down, both the SGMII and copper interfaces are up/ active. When the SGMII interface transitions from down to up, this issue might occur.

Status: A0=Yes; No Fix

4. Cable Detector in First Peak Mode or Alternate Cable Detector Control

Problem: The results in cable length measurement in first peak mode or alternate cable detector are inconsistent, if the default setting for the TDR pulse width (register 28_5.11:10 = 00b) is used.

Implication: TDR pulse setting might be too high.

Workaround: Reduce the TDR pulse setting to ¼ width by writing register 28_5.11:10 = 11b.

Status: A0=Yes; No Fix

5. CRC Error Counter Showed an Error When Enabled While Traffic is Running

Problem: CRC error counter showed an error when enabled while traffic is running.

Implication: When traffic is running and the CRC error counter is enabled, the counter might be enabled in the middle of the packet and treats the packet as an error packet.

Workaround:

- The CRC error counter should be enabled when there is no traffic
- If the CRC error counter is enabled when traffic is running, the first error should be ignored

Status: A0=Yes; No Fix

6. Wider Operating Temperature Range

Problem: The device operates correctly over a wide operating temperature range and does not have an issue under normal operating conditions. However, if the device is subjected to a wider operating temperature range, for example, the device is powered up at 0 °C and forced to run at 120 °C during a temperature cycle test.

Implication: Operating range not wide enough during temperature cycle test. Use the following workaround to increase the operating temperature range.

Workaround: Write register 22 = 0x00FF (set register 22 page to 0x00FF)

- • Write register 24 = 0x4D50
- • Write register 23 = 0x2003
- • Write register 22 = 0x0000 (set register 22 Page to 0x0000)

Status: A0=Yes; No Fix

7. 10BASE-T IEEE-Specific Harmonic Content Level Issue

Problem: On some board designs, the I347 might not meet the IEEE specification (1411.10.03) that states that the harmonic content is to be at least 27 dB below the 10 MHz fundamental frequency.

Implication: IEEE conformance is marginal. There is no impact on system level performance; however, care should be taken to verify the impact of radiated Electromagnetic Interference (EMI) on system-level EMI tests.

Workaround: There is no silicon/firmware/software workaround; however, using short low-resistance traces (less than four inches and without a LAN switch) can help reduce harmonic content.

Status: A0=Yes; No Fix

8. 100BASE-TX Marginal Rise/Fall Time Performance

Problem: The I347 rise/fall time has been marginal compared to the IEEE specification (5 ns).

Implication: IEEE conformance is marginal. Depending on system topology (LAN switch/no LAN switch), MDI trace lengths, and configuration (docked/undocked), the 100BASE-TX rise/fall time might not meet the IEEE specification. Note that there is no impact on system level performance.

Workaround: Use 100BASE-TX Class A by writing register 26_0.12 = 1b.

Status: A0=Yes; No Fix

9. 1000BASE-T Cable Length

Problem: If using a worst case cable (120 Ω), the I347 might not operate correctly with cables longer than 105 m.

Implication: N/A.

Workaround: N/A

Status: A0=Yes; No Fix

10. I347 Might Not Respond Correctly to the First Read of the MDIO Interface

Problem: Some I347 devices might return 0x0000 for the first read of the MDIO interface instead of the actual register value being read.

Implication: Is dependent on what the software does with the information returned in error. Intel supplied drivers that do not implement the workaround will fail to load if 0x0000 is returned for the first read. If you are using other software you will have to determine how it will behave.

Workaround: Perform a double read for the first read access for each active PHY in the I347 and only use the data from the second read. In all cases tested, the second and every subsequent read retrieved the correct value.

Status: A0=Yes; No Fix

3. Software Clarifications

Table 3-1. Summary or Software Clarifications

Software Clarifications	Status
None.	N/A

Note: This page intentionally left blank.