82546EB to 82546GB Migration

Application Note (AP-484)

Revision 1.0
June 2005

Revision History

Revision	Revision Date	Description
1.0	June 2005	Initial release

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1.0 Introduction and Scope

The document explains the differences between an Intel® 82546EB Gigabit Ethernet Controller-based design and an Intel® 82546GB Ethernet Controller-based design. The primary differences are:

- Device IDs
- New 82546GB Features
- Resolved 82546EB Errata

2.0 Reference Documents

- 8254x Family of Gigabit Ethernet Controllers Software Developer's Manual, Intel Corporation.
- 82546GB Dual Port Gigabit Ethernet Controller Datasheet, Intel Corporation.
- 82546EB Dual Port Gigabit Ethernet Controller Datasheet, Intel Corporation.
- 82545EM, 82545GM, 82546EB, and 82546GB Gigabit Ethernet Controllers Design Guide.
- PCI Local Bus Specification, Revision 2.3, PCI Special Interest Group.
- PCI-X Specification, Revision 1.0a, PCI Special Interest Group.
- PCI Bus Power Management Interface Specification, Rev. 1.1, PCI Special Interest Group.

3.0 Pin Compatibility

The 82546GB is a pin compatible drop-in replacement for the 82546EB. Refer to the *82546GB Dual Port Gigabit Ethernet Controller Datasheet* for package and pinout information.

4.0 Device IDs

Table 1 lists the device IDs for both the 82546EB and 82546GB Gigabit Ethernet Controllers.

Table 1. Component Identification

Stepping	Vendor ID	Device ID	Description
82546GB	8086h	1079h	Copper; Dual Port
82546GB	8086h	107Ah	Fiber; Dual Port
82546GB	8086h	107Bh	SerDes; Dual Port
82546EB	8086h	1010h	Copper; Dual Port
82546EB	8086h	1012h	Fiber; Dual Port

5.0 New 82546GB Features

- Device ID - Created a new default device ID to identify the 82546GB
- PCI Configuration Map:
  - PCI: 00-3Ch
  - PCI Power Management: DC-E0h
  - PCI-X: E4-E8h
  - Message Signaled Interrupt: F0-FCh
- EEPROM Circuit Control Word 21h setting for PCI-X Driver Strength: FF63h
- Improved PCI-X V/I curves - V/I curves are centered relative to specification minima and maxima
- PICMG 3.1 compliant SerDes interface - Stronger drive strength and lower pre-emphasis to the SerDes transmitter
- VLAN management filters - Able to filter up to four different VLAN IDs for management
- IPMI I^2C addressing capability - Allows IPMI implementations to follow I^2C formats instead of SMBus formats
- IPMI MAC read capability - Enables the BMC to read the assigned MAC address of the 82546GB
- PCI 2.3 compliance - Includes PCI 2.3 compatible interrupt bits
- Full 2/3-wire downshift capabilities:
  - Enables downshift to 10/100 link when pair three or four is damaged
  - Enabled by default instead of requiring driver initialization
- Disabled gigabit half-duplex advertisement in copper PHY - Saves the software device driver from a re-negotiation event

6.0 Resolved 82546EB Errata

The following 82546EB Errata were resolved in the 82546GB Gigabit Ethernet Controller:

- Erratum #08 – 1.5V Regulator Control Circuit Start Up:
  - A generic BCP69 can be used without a CTRL15 pull-down resistor
- Erratum #12 – Bus Initialization With Some Chipsets:
  - A 0 ns hold time relative to RST# is now acceptable for a PCI-X configuration
- Erratum #14 – ASF Lockup Upon Resetting MAC:
  - A lockup condition was removed by changing the manageability logic
- Erratum #15 – REQ# Pin Requires Pull-Up Resistor in PCI-X Mode:
  - REQ# logic was changed to always drive thus eliminating the need for a pull-up resistor
- Erratum #16 – INTA# / INTB# Configuration on 82546EB Controller:
  - Interrupts are now correctly routed to the correct INTx# pins when the ports are disabled
- Erratum #17 – MWI Trans. May Terminate on Non-Cacheline Boundary:
  - PCI logic was changed to use a memory write transaction on non-cacheline writes
- Erratum #19 – PCI-X Maximum Read Burst When Programmed:
  - PCI-X logic was changed to use the smaller of the two values
- Erratum #20 – Master Aborts With Some Chipsets During Driver Reset:
  - An additional register with a software reset bit was added to the high DWORD to avoid a master abort
- Erratum #24 – Address Error Crossing 64KB Boundary:
  - An error condition was corrected to allow for 64 KB boundary crossings
- Erratum #25 – Intermittent Issues with TCO Receive Packets in IPMI Mode:
  - Corrected the TCO Receive FIFO logic to avoid an indeterminate state
- Erratum #29 – ASF RMCP ACK Packets May be Incorrectly ACK’ed:
  - A logic issue in the ASF logic was corrected to avoid sending an ACK to a received ACK
- Erratum #31 - Memory Access Must be Enabled in Order to Read Device Registers in I/O Mode:
  - Device registers can now be accessed in I/O mode with only the I/O Access Enable bit set

Note: Refer to the *82546GB Gigabit Ethernet Controller Specification Update* for additional Errata information.

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