82540EM to 82541ER Migration

Application Note (AP-452)

Revision 2.12

October 2004

Revision History

Date	Revision	Description
October 2004	2.12	Changed Pins A10, B10 and C9 to RESERVED_VCC; Pin C8 to NC; removed references to CLKRUN# in 82541ER.
August 2004	2.11	Added Pin J13 (NC v. XTAL18) to Table 1
April 2004	2.1	Added information for oscillator support.
August 2003	2.0	Non-classified release.
August 2003	1.0	Initial release (Intel Confidential).

Contents

1.0 Introduction

The goal of this document is to enable the migration of an Intel® 82540 Gigabit Ethernet controller based design to an Intel® 82541ER Gigabit Ethernet controller. The primary differences to consider between the 82540 and 82541ER are:

- Power Supplies
- Manageability Features
- EEPROM Configuration
- Support for SPI and Microwire EEPROMs
- TBI Support
- Pinout Differences

Note: Only the differences between these devices are listed in this application note. Please refer to the Ethernet controller's respective updated specification update, datasheet and design guide for additional information of the device.

Note: When '82540' is being referenced in this document it implies that it is applicable to both the 82540EM and the 82540EP Ethernet Controllers.

2.0 Power Supplies

The 82540's power supplies include 3.3V, 2.5V, and 1.5V. The 82541ER uses the 3.3V like the 82540, but the other power supplies needed are 1.8V and 1.2V which differ from the 82540. As a result of the differences in power supplies between the two components, less power is consumed with the 82541ER device.

3.0 Manageability Features

The 82541ER does not support an onboard SMB port, hence the manageability features that may have been available for the 82540 will not be for the 82541ER. If manageability features are desired, then the 82541EI should be used instead. Some manageability features may include: ASF (1.0 for the 82540 and 2.0 for the 82541EI), Wake on LAN, and PXE.

4.0 EEPROM Configuration

The 82540 and 82541ER use an EEPROM device for storing the Ethernet controller's configuration information. If migrating from one controller to another, the EEPROM must be updated according to the respective Ethernet Controller. Please refer to the 82541EI/82547EI EEPROM Programming Information Guide (AP-446) and the 82546EB Gigabit Ethernet Controller Networking Silicon Developer's Manual + Appendices for 82545EM, 82540EM, 82544EI/GC (Ref# 13659) for more information on EEPROM settings.

5.0 Support for SPI and Microwire EEPROMs

The 82541ER supplies ball J4, EEMODE, to indicate what EEPROM interface is being used, whether it be an SPI or Microwire. EEMODE (J4) should be pulled down to ground via a 1kohm resistor to indicate it uses a Microwire device. Otherwise, if an SPI device is being used, then EEMODE (J4) should be left unconnected. The 82540 only supports a Microwire interfaced EEPROM and therefore ball J4 is NC (no connect).

6.0 CLKRUN# Signal

Not supported.

7.0 TBI Support

The 82541ER does not support TBI modes, while the 82540 does.

8.0 Pin Differences

Both the 82540 and 82541ER have a 196 Ball Grid Array package. The pin out diagrams for the 82540 and 82541ER are illustrated in the following pages. However, there are 15 (14 for the 82540EP) pins to note that differ between the 82540EM and 82541ER:

Table 1. Pin Differences between the 82540 and 82541ER

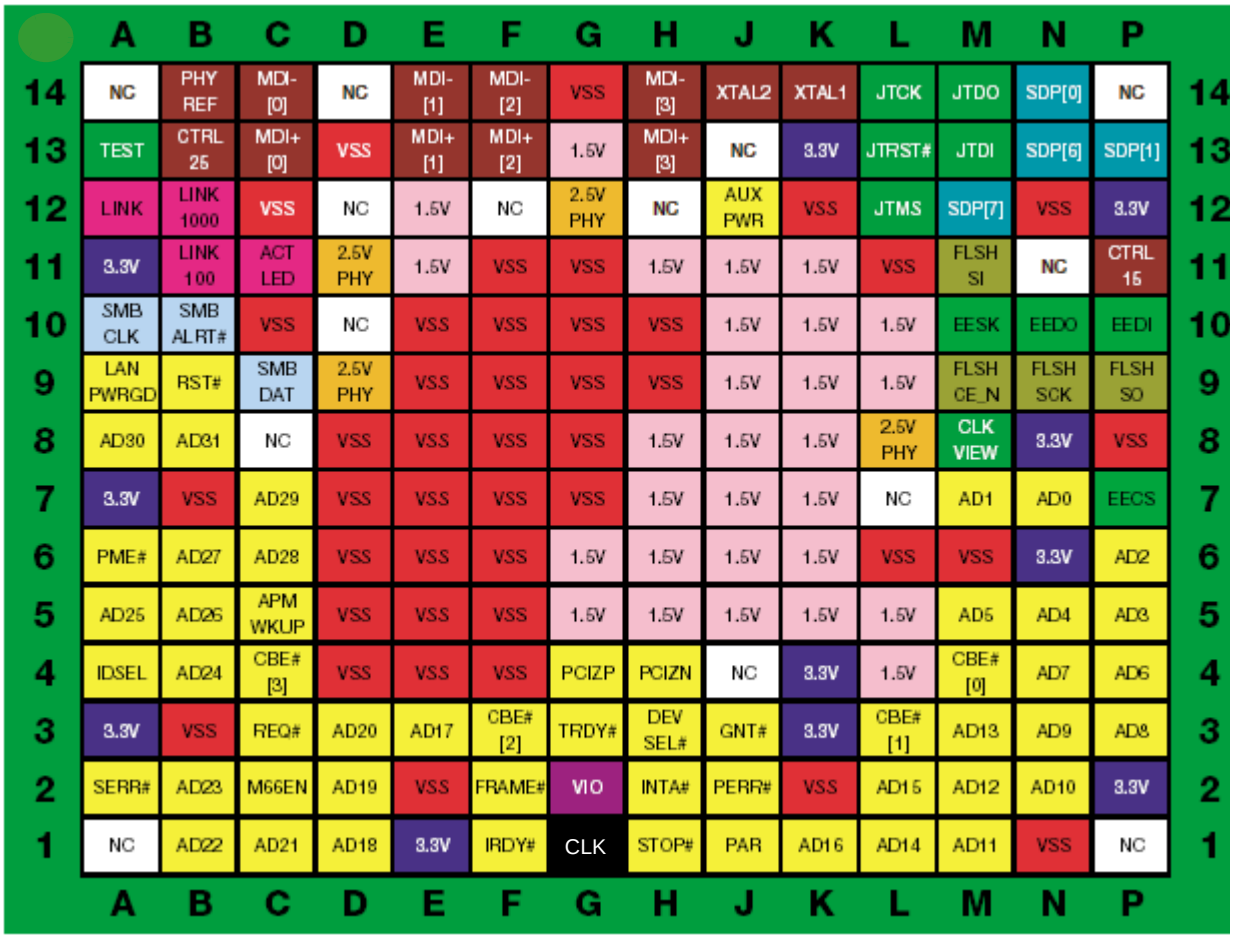
Pin	82540 Function	82541ER Function
A6	PME#	NC
B14	PHYREF	DIF_P
D14	NC	DIF_N
D12	NC	VDDC1.8V
F12	NC	NC
H12	NC	NC
J13	NC	XTAL18
A10	SMBCLK	RESERVED_VCC[1]
B10	SMBALERT#	RESERVED_VCC[1]
C9	SMBDATA	RESERVED_VCC[1]
D9	2.5V	NC
M8	CLKVIEW	NC
L8	2.5V	NC
C8	NC (***only*** for 82540EM)	NC
G4	PCIZP	PLL_1.2

Table 1. Pin Differences between the 82540 and 82541ER

Pin	82540 Function	82541ER Function
H4	PCIZN	PLL_1.2
J4	NC	EE_MODE
J13	NC	XTAL_18

1. 1K pull-up to Vcc recommended.

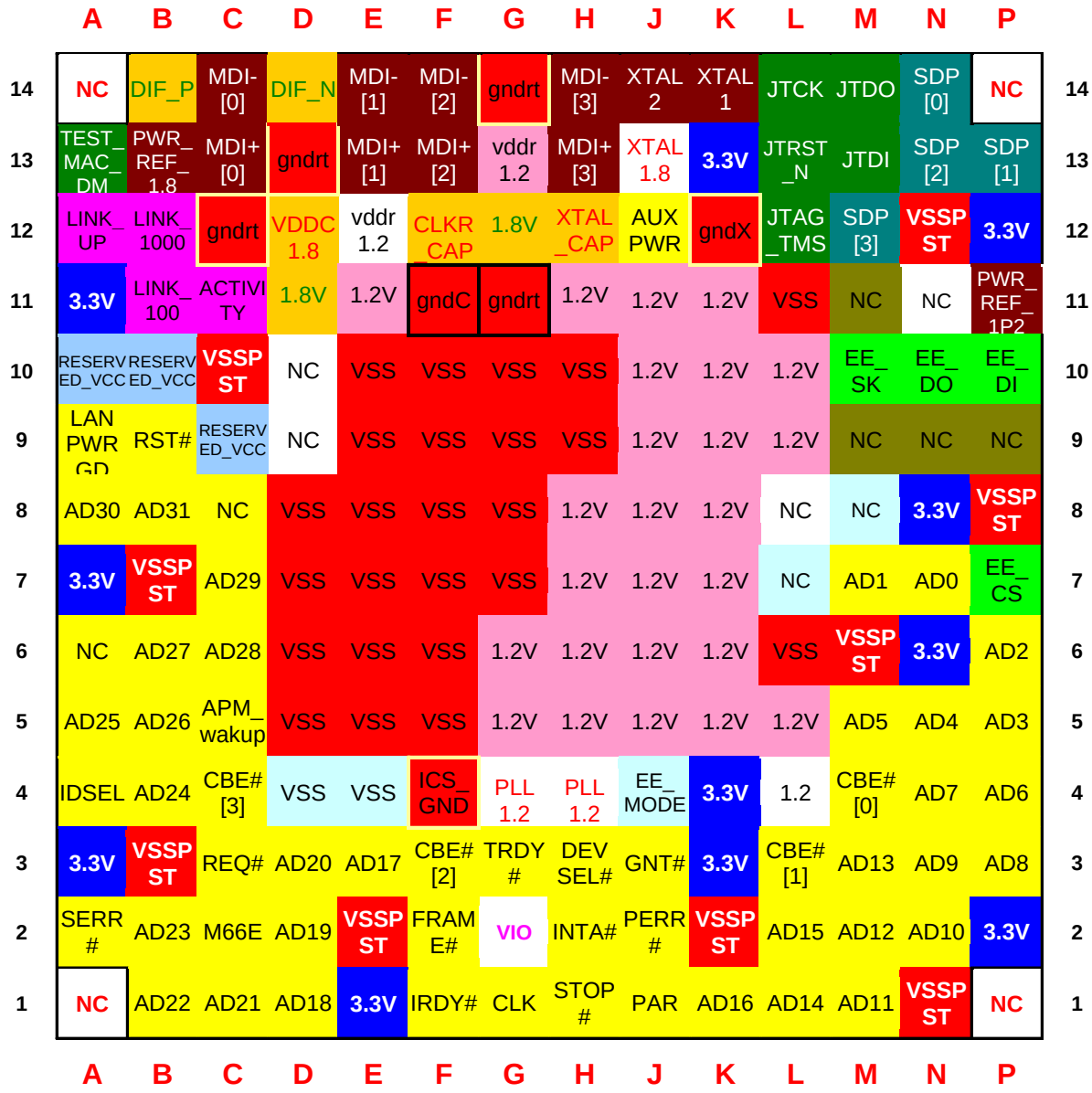
Figure 1. 82540 Ball Grid Array Diagram



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	NC	PHY REF	MDI-[0]	NC	MDI-[1]	MDI-[2]	VSS	MDI-[3]	XTAL2	XTAL1	JTCK	JTDO	SDP[0]	NC	14
13	TEST	CTRL 25	MDI+[0]	VSS	MDI+[1]	MDI+[2]	1.5V	MDI+[3]	NC	3.3V	JTRST#	JTDI	SDP[6]	SDP[1]	13
12	LINK	LINK 1000	VSS	NC	1.5V	NC	2.5V PHY	NC	AUX PWR	VSS	JTMS	SDP[7]	VSS	3.3V	12
11	3.3V	LINK 100	ACT LED	2.5V PHY	1.5V	VSS	VSS	1.5V	1.5V	1.5V	VSS	FLSH SI	NC	CTRL 15	11
10	SMB CLK	SMB ALRT#	VSS	NC	VSS	VSS	VSS	VSS	1.5V	1.5V	1.5V	EESK	EEDO	EEDI	10
9	LAN PWRGD	RST#	SMB DAT	2.5V PHY	VSS	VSS	VSS	VSS	1.5V	1.5V	1.5V	FLSH CE_N	FLSH SCK	FLSH SO	9
8	AD30	AD31	NC	VSS	VSS	VSS	VSS	1.5V	1.5V	1.5V	2.5V PHY	CLK VIEW	3.3V	VSS	8
7	3.3V	VSS	AD29	VSS	VSS	VSS	VSS	1.5V	1.5V	1.5V	NC	AD1	AD0	EECS	7
6	PME#	AD27	AD28	VSS	VSS	VSS	1.5V	1.5V	1.5V	1.5V	VSS	VSS	3.3V	AD2	6
5	AD25	AD26	APM WKUP	VSS	VSS	VSS	1.5V	1.5V	1.5V	1.5V	1.5V	AD5	AD4	AD3	5
4	IDSEL	AD24	CBE#[3]	VSS	VSS	VSS	PCIZP	PCIZN	NC	3.3V	1.5V	CBE#[0]	AD7	AD6	4
3	3.3V	VSS	REQ#	AD20	AD17	CBE#[2]	TRDY#	DEV SEL#	GNT#	3.3V	CBE#[1]	AD13	AD9	AD8	3
2	SERR#	AD23	M66EN	AD19	VSS	FRAME#	VIO	INTA#	PERR#	VSS	AD15	AD12	AD10	3.3V	2
1	NC	AD22	AD21	AD18	3.3V	IRDY#	CLK	STOP#	PAR	AD16	AD14	AD11	VSS	NC	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

NOTE: The 82540EP and 82540EM have only two differences between their ballouts:
1. C5 - For the 82540EP, C5 is a no connect (NC); for the 82540EM, it is the APM_WAKEUP signal.
2. C8 - For the 82540EP, C8 is the Clock Run (CLKRUN#) signal; for the 82540EM, it is a no connect (NC).

Figure 2. 82541ER Ball Grid Array Diagram



9.0 Oscillator Support

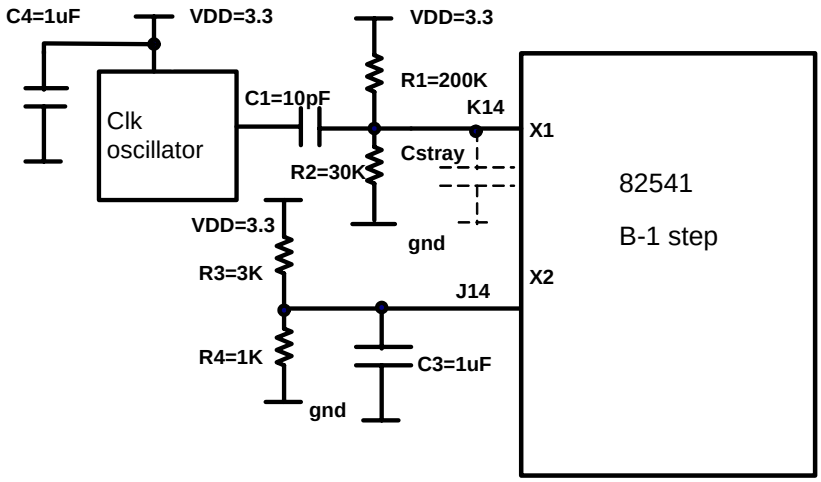
The 82541 clock input circuit is optimized for use with an external crystal. However, an oscillator may also be used in place of the crystal with the proper design considerations:

- The clock oscillator has an internal voltage regulator of 1.2 V to isolate it from the external noise of other circuits to minimize jitter. If an external clock is used, this imposes a maximum input clock amplitude of 1.2 V.
- The input capacitance introduced by the 82541 (approximately 20 pF) is greater than the capacitance specified by a typical oscillator (approximately 15 pF).
- The input clock jitter from the oscillator can impact the 82541 clock and its performance.

Table 2. Clock Oscillator Specifications

Symbol	Parameter	Specifications			Units
		Min	Typical	Max	
f0	Frequency		25		MHz
df0	Frequency Variation	-50		+50	ppm
Dc	Duty Cycle	40		60	%
tr	Rise Time			5	ns
tf	Fall Time			5	ns
σi	Clock Jitter, rms (if specified)			50	ps
C1	Clock Capacitance (pushed by clock)		15	50	pF
VDD	Supply Voltage		3.3 or 1.8		V
Operating temperature				70	° C
CMOS output levels	Voltage Output High (Voh), Voltage Output Low (Vol)	80% VDD		 20% VDD	V V

9.1 82541GI (B-1 Stepping) Oscillator Solution



The oscillator solution for the 82541GI includes capacitor C1, which forms a capacitor divider with capacitor C_{stray} of approximately 20 pF. This attenuates the input clock amplitude and adjusts the oscillator load capacitance where

$$V_{in} = VDD * (C1/(C1 + C_{stray}))$$

$$V_{in} = 3.3 * (C1/(C1 + C_{stray}))$$

This enables load clock oscillators of 15 pF to be used. If the value of C_{stray} is unknown, C1 should be adjusted by tuning the input clock amplitude to approximately 1 V_{ptp}. If C_{stray} equals 20 pF, then C1 is 10 pF ±10%.

The architecture of the 82541 crystal oscillator requires a differential clock on the X1 and X2 input signals or a single ended clock input on the X1 pin with common mode biasing of the X2 pin. A relatively low drive strength of the 82541GI crystal driver does not guarantee the differential X1 and X2 inputs with a single ended external clock oscillator. Therefore, the resistive common mode bias circuitry should be added to produce a common mode voltage (V_{CM}) of approximately 0.6 V on the X2 pin. The resistive divider (R3 and R4) and the decoupling capacitor (C3) are required to form and stabilize the biasing circuit for the X2 pin. The resistive divider R1 and R2 produces a V_{CM} of about 0.6 V for the input clock of the X1 pin.

Note: The resistor tolerance should be within ±10%.

Note: The power consumption of additional circuitry equals about 1.5 mW.

9.2 82541PI (C-0 Stepping) Oscillator Solution

There are two oscillator solutions for the 82541PI: high voltage and low voltage.

9.2.1 High Voltage Solution (VDD=3.3V)

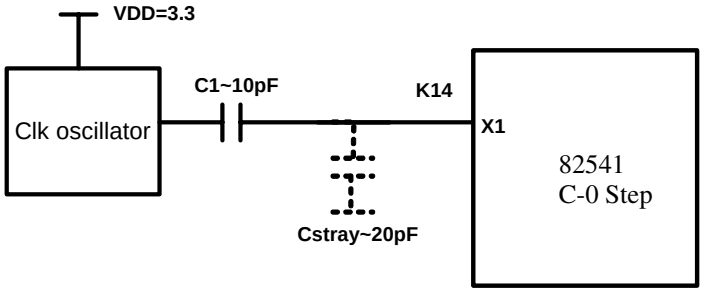
This solution involves capacitor C1, which forms a capacitor divider with C_{stray} of about 20 pF. This attenuates the input clock amplitude and adjusts the clock oscillator load capacitance.

$$V_{in} = VDD * (C1/(C1 + C_{stray}))$$
$$V_{in} = 3.3 * (C1/(C1 + C_{stray}))$$

This enables load clock oscillators of 15 pF to be used. If the value of C_{stray} is unknown, C1 should be adjusted by tuning the input clock amplitude to approximately 1 V_{ptp}. If C_{stray} equals 20 pF, then C1 is 10 pF ±10%.

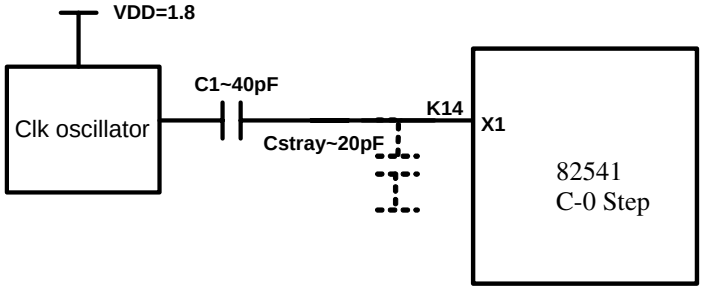
A low capacitance, high impedance probe (C < 1 pF, R > 500 KΩ) should be used for testing. Probing the parameters can affect the measurement of the clock amplitude and cause errors in the adjustment. A test should also be done after the probe has been removed for circuit operation.

If jitter performance is poor, a lower jitter clock oscillator can be implemented.



9.2.2 Low Voltage Solution (VDD=1.8V)

The low voltage solution is similar to the high voltage solution. However, the low voltage includes a low consumption and low jitter clock oscillator that uses a 1.8V external power supply. In this case, C1 will require adjusting according to the stray capacitance from X1.



10.0 Summary

If migrating from the 82540 to the 82541ER, there are a few things to consider. Both controllers need different power supplied to them.

Some features that may have been available with the 82540 design may not be available when transitioning to an 82541ER. These are features that utilize the SMB port of the 82540 that is not available with the 82541ER. Also, the Wake on LAN feature supported by the 82540 devices is not supported by the 82541ER.

Ensure appropriate EEPROM configuration is taken into account when transitioning as the settings are different between controllers.