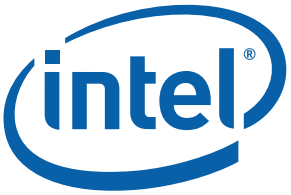


Intel® 82579 GbE PHY Specification Update

October 2012
v2.5

Reference Number: 324967-005

Revision History

Date	Revision	Description
March 2010	1.0	Initial Public Release.
April 2010	1.5	Added Specification Changes #2 and #3.
May 2010	1.6	Added A-2 Markings information to Table 1.
August 2010	1.61	Added B-0 MM number, QDF numbers, and production phase indicator.
October 2010	1.9	Added C-0 MM number, QDF numbers, and production phase indicator. Removed all specification changes (incorporated into datasheet). Updated product markings and codes.
January 2011	2.0	Added Software Clarification.
January 2011	2.1	Prepared for posting on public site.
April 2011	2.2	Added Errata 1.
August 2011	2.3	Added Errata 2.
November 2011	2.4	Added Specification Clarification and Documentation Changes 1, 2, and 3
October 2012	2.5	Added Errata 3 (applies to "V" version only)

1. Introduction and Scope

This document applies to the Intel® 82579 GbE Ethernet PHY, incuding both the “LM and “V” versions.

This document is an update to a published specification, the *Intel® 82579 Gigabit Ethernet Controller Datasheet*. It is intended for use by system manufacturers and software developers. All product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

1.1 Product Code and Device Identification

Table 1 and Figure 1 describe the various identifying markings on each lead-free device package:

Table 1. Markings

Device	Stepping	MM #	Specification Code	Type	Std Pack Qty	Type	Lead (Pb) Free
WG82579LM	C-0	MM# 909805	S LHA5	T&R	2000/T&R	production	RoHS
WG82579LM	C-0	MM# 909806	S LHA6	Tray	490 / Tray	production	RoHS
WG82579V	C-0	MM# 909807	S LHA7	T&R	2000/T&R	production	RoHS
WG82579V	C-0	MM# 909808	S LHA8	Tray	490 / Tray	production	RoHS

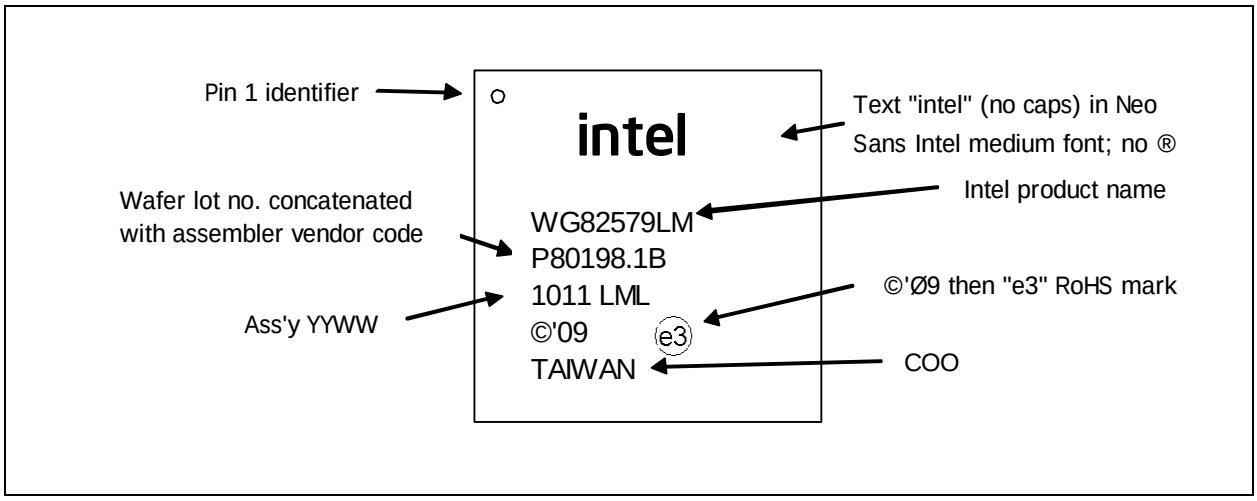


Figure 1. Typical Top Marking Example With Identifying Marks

Table 2. Device IDs

Device ID Code	Vendor ID	Device ID
82579LM	0x8086	0x1502
82579V	0x8086	0x1503

1.2 Nomenclature Used In This Document

This document uses specific terms, codes, and abbreviations to describe changes, errata, sightings and/or clarifications that apply to silicon/steppings. See Table 3 for a description.

Table 3. Terms, Codes, Abbreviations

Name	Description
Specification Changes	Modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
Errata	Design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.
Specification Clarifications	Greater detail or further highlights concerning a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
Documentation Changes	Typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
Yes or No	If the errata applies to a stepping, "Yes" is indicated for the stepping (for example: "A0=Yes" indicates errata applies to stepping A0). If the errata does not apply to stepping, "No" is indicated (for example: "A0=No" indicates the errata does not apply to stepping A0).
Doc	Document change or update that will be implemented.
Fix	This erratum is intended to be fixed in a future stepping of the component.
Fixed	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Red Change Bar / or Bold	This Item is either new or modified from the previous version of the document.
DS	Datasheet
PDG	Platform Design Guide
EDS	External Data Specification

1.3 Changes, Errata, and Clarifications

See Section 1.2 for an explanation of terms, codes, and abbreviations used in the following tables and discussions.

Table 4. Summary of Changes

1.3.1 Specification Changes

None active.

1.3.2 Specification Clarifications

1. PCIe Clock Level Reduced to Half During Rx/Tx.

Clarification: When the 82579 is transmitting or receiving data the PCIe Clock signal is reduced to half its normal level. This is normal for this device.

1.3.3 Software Clarifications

1. Driver 15.6 Causes LAN to be Disabled in Device Manager.

Clarification: Release 15.6 driver, supporting the 82579 PHY, introduced an issue where the LAN becomes disabled in Device manager when the system resumes from Sx states. The PHY could lock up due to an incorrect handling of the PHY shared semaphore. To resolve the issue, the driver now takes control of the PHY semaphore before accessing a specific PHY register. To ensure smooth transition in and out of Sx states, a HW reset to the driver Sx resume flow was also added. The initial release for this resolution is available in Release 15.7.1.

1.3.4 Documentation Changes

1. Document: *Intel® 82579 (Lewisville) and Cougar Point Integrated GbE LAN Bring Up Guide*: Text Change.

Change: In the table in Section 6, for the Power on Test: "Measure magnetics center tap voltage," under Debug Suggestions, **delete** the following text: "Inspect the trace for the magnetics center tap, if connected to the 82579 pin 6." This action is not required.

2. Document: *Intel® 82579 PHY ARP/NS Offload Basic Test Plan v0.5*: Text Change.

Change: In Section 1.3-Overview, the Configuration/Proxy table and table footnote should read as follows:

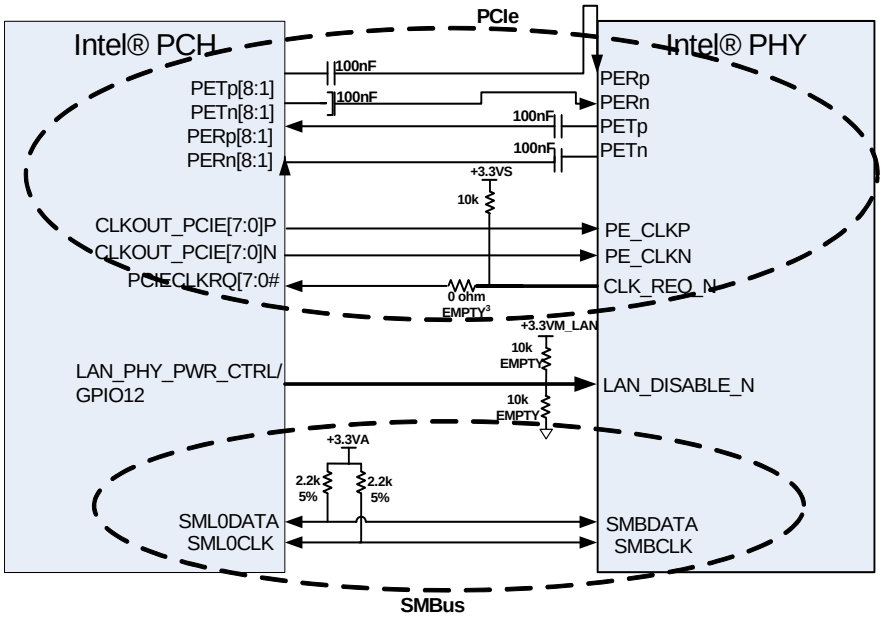
.

CONFIGURATION	PROXY
System without Intel® ME enabled Microsoft Windows 7* † 82579 C0 PHY with NDIS	Intel® 82579 PHY responds to ARP/NS requests.
System with Intel® ME enabled and in PP1 (S0 state) Microsoft Windows 7* † Intel® 82579 C0 PHY with NDIS	No Proxy Support (Intel® ME 7.0) Intel® ME responds to ARP/NS requests (Only supported in Intel® ME 8.0)
System with Intel® ME enabled and in PP2 (S0 & Sx state) Microsoft Windows 7* † Intel® 82579 C0 PHY with NDIS	Intel® ME responds to ARP/NS requests.

† Microsoft Windows 7* does not require ARP offload support on platforms until Q4'11. Certification for ARP/NS offload will be in Windows* Lab Kit (WLK) 1.6.

3. Document: *Intel® 82579 Gigabit Ethernet PHY v2.1*: Text Change.

Change: Chapter 2, Figure 2 Intel 6 Series Express Chipset/82579 Interconnects; Chapter 16, Figure 16-9; and Chapter 17, Figure 17-9 should appear as follows:



1.3.5 Errata

1. IEEE Std 802.3*-2008 Tx Distortion Marginality.

Problem: The Intel® 82579 Gigabit Ethernet Controller may not meet the IEEE Std 802.3™-2008 specification (40.6.1.2.4) that states that the Tx Distortion must meet the following criteria. “A PHY is considered to pass this test if the peak distortion is below 10mV for at least 60% of the UI within the eye opening.” The 82579 may marginally fail this requirement.

Implication: IEEE conformance is marginal.

The TX distortion is less than 10 mV during the critical time when the signal is actually sampled therefore no impact on system performance is observed with the 82579 due to this marginality.

Workaround: None.

Status: NoFix

2. Controller May Show Excessive Packet Loss In 100 Mbps/Half-Duplex Mode.

Problem: When in 100 Mbps/Half-Duplex only, the controller may show excessive packet loss. Platforms may show dropped packets during ping test at 100 Mbps/Half-Duplex under all OS's supported. Packet loss in the worst cases has been seen up to 50%. Upon inspection, the majority of the dropped packets were found to be 200 bytes or less.

Any board with the 82579LM or 82579V, with driver release version 16.4 or older and where the connection mode is 100 Mbps/half-duplex, could be affected by dropped packets. This includes all driver versions released before July 17, 2011.

Note: The 1 Gbps and 10 Mbps modes, and the 100 Mbps/full-duplex are unaffected.

Implication: Platforms with the 82579LM or 82579V may show drop packets during ping test at 100Mbps/half-duplex under all OS's supported. Packet loss in the worst cases has been up to 50%. Upon inspection, the majority of the dropped packets are found to be 200 bytes or less.

Root Cause: The MAC/PHY interface, when working in 100M/Half Duplex, was dropping packets.

When the MAC initiates K1 entrance (analogous to P1 state in the PCI Express specification), it sends a K1 request and put its TX lanes into electrical idle (EI). When the PHY receives the K1 request, it sends a K1 response and put its TX lanes into EI. When the PHY gets a packet from the wire it starts sending a beacon signal for 10us. After 10usec, it begins searching for synchronization pattern. When the MAC senses activity on its RX lines, it sends its beacon signal for 16us. After 16usec, it begins searching for synchronization pattern.

Allowable noise levels within the PCI-Express specifications are misinterpreted as synchronization patterns from the MAC and the PHY locks its PLL. After 2us the PHY will accomplish K1 exit. When the packet is entirely in the PHY buffer, it will be sent the packet to the MAC. When the MAC is sending beacon it will drop any RX packet. Any packet under the length 200 bytes will be entirely received in less than 16us and thus will be uploaded to the MAC during beacon transmission.

The failed behavior is described in the following timing diagram showing the K1 exit mechanism.

3. Windows Code 10 Error may be observed on Intel® 82579V Ethernet Controller (applies to “V” version only)

Problem: During system resume from SX states, the Intel 82579V Ethernet Controller erroneously updates the device id in the PCIE configuration space to the 82579LM device Id, resulting in a Windows Code 10 error message. The issue is caused due to a HW bug.

Implication: Not all platforms with 82579V will see this problem. Platforms configured with Win 8 O.S are more susceptible to the issue and will experience the loss of LAN connectivity along with Windows Code 10 error message in the device manager.

Root Cause: Run the SW utility available on the Intel portal at:

http://www.intel.com/support/go/network/82579v/nvramupdate.htm

Status: NoFix

§ §