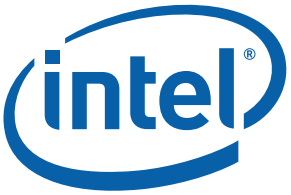

Intel® 82578 GbE PHY Specification Update

January 2010
Revision 1.4

322615-002

Revision History

Date	Revision	Description
January 2010	1.4	Added Specification Clarification #1. Removed Erratum #2.
December 2009	1.3	Added Erratum #2.
September 2009	1.2	Initial Public Release.

1.1 Introduction and Scope

This document applies to the 82578 GbE PHY.

This document is an update to a published specification, the *Intel® 82578 GbE PHY Datasheet*. It is intended for use by system manufacturers and software developers. All product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

1.2 Product Code and Device Identification

Table 1 and Figure 1 describe the various identifying markings on each lead-free device package:

Table 1. Markings

Device	Stepping	Top Marking	MM #	Description	Tray/Tape and Reel
82578DM	C0	WG82578DM	903518	Corporate Desktop	Tape and Reel
82578DM	C0	WG82578DM	903519	Consumer Desktop	Tray
82578DC	C0	WG82578DC	903520	Corporate Desktop	Tape and Reel
82578DC	C0	WG82578DC	903521	Consumer Desktop	Tray

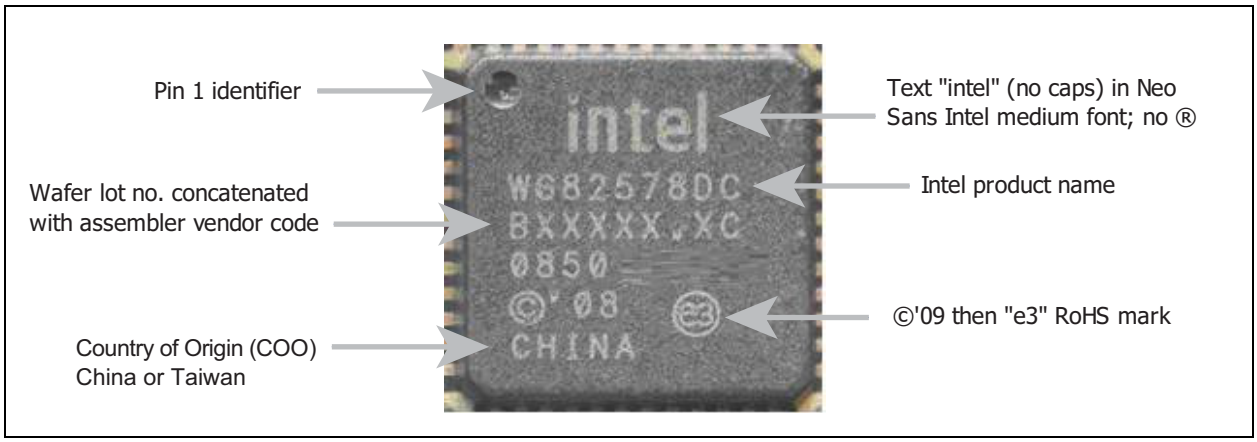

Figure 1. Typical Top Marking Example With Identifying Marks (82578DC Shown)

Table 2. Device IDs

Device ID Code	Vendor ID	Device ID	Revision ID
82578DM	0x8086	0x10EF	0
82578DC	0x8086	0x10F0	0

1.3 Nomenclature Used In This Document

This document uses specific terms, codes, and abbreviations to describe changes, errata, sightings and/or clarifications that apply to silicon/steppings. See Table 3 for a description.

Table 3. Terms, Codes, Abbreviations

Name	Description
Specification Changes	Modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
Errata	Design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.
Specification Clarifications	Greater detail or further highlights concerning a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
Documentation Changes	Typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
Yes or No	If the errata applies to a stepping, "Yes" is indicated for the stepping (for example: "A0=Yes" indicates errata applies to stepping A0). If the errata does not apply to stepping, "No" is indicated (for example: "A0=No" indicates the errata does not apply to stepping A0).
Doc	Document change or update that will be implemented.
Fix	This erratum is intended to be fixed in a future stepping of the component.
Fixed	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Red Change Bar / or Bold	This Item is either new or modified from the previous version of the document.
DS	Datasheet
PDG	Platform Design Guide
EDS	External Data Specification

1.4 Changes, Errata, and Clarifications

See Section 1.3 for an explanation of terms, codes, and abbreviations used in the following tables and discussions.

Table 4. Summary of Changes

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1.4.1 Specification Changes

None active.

1.4.2 Specification Clarifications

1. PHY Does Not Maintain Gigabit Link in Low Power States

Clarification: While operating in power states less than D0 or operating system states other than S0, the PHY is designed to negotiate to the lowest speed possible, and maintains a link in those states only at 10 Mb/s or 100 Mb/s. If the PHY is connected to a link partner that is only capable of gigabit connections, the link is lost in these lower power states. This limitation is due to power requirements imposed by energy saving initiatives (such as Energy Star), as the additional power required to maintain gigabit connections might cause the system to exceed the level needed to meet the specifications.

Impact: When attached to a port that is limited to gigabit speed connections, the PHY loses link in low power states, and therefore network functions normally available in those states, such as Wake on LAN (WoL) or remote management, is not possible in that environment.

1.4.3 Documentation Changes

None active.

1.4.4 Errata

1. Jumbo Frames Not Supported With PCI Express* (PCIe*) Spread Spectrum Clocking (SSC)

Problem: 82578 is unable to support 9 KB jumbo frames when PCIe SSC is enabled in Intel® 5 Series Express Chipset.

Implication: Enabling 9 KB jumbo frames with PCIe SSC enabled might result in data overflow/ underflow errors resulting in packets transmitted/received with CRC errors.

Workaround: For 9 KB jumbo frames support, PCIe SSC must be disabled.

Status: No fix for 9 KB jumbo frames.