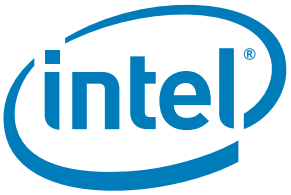


Intel® 82575 GbE Controller EEPROM Information Guide

June 2008

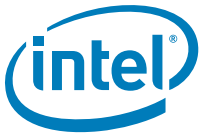
317290-004
Revision 1.3

Contents

Tables

Revision History

Date	Revision	Description
June 2008	1.3	• Updated section 1.6.1.5 (changed default device ID to 10A7h. • Updated section 1.6.1.1 (removed note concerning MAC addresses).
January 2008	1.2	• Updated bit 13 description in word 15h. • Updated sections 1.8.2 and 1.8.3. • Updated section 1.7.1.7 (bits 4:0 descriptions). • Updated EEPROM sizes.
September 2007	1.1	Updated section 1.7.1.7.
June 2007	1.0	Initial public release
November 2006	0.75	Initial release (Intel Confidential)
June 2006	0.5	Initial release (Intel Secret)



1.0 EEPROM and Flash Interface

1.1 Introduction

This Application Note describes the EEPROM and Flash interfaces supported by 82575.

1.2 EEPROM Device

The 82575 uses an EEPROM device to store product configuration information. The EEPROM is divided into three general regions:

- **Hardware Accessed —** Loaded by the 82575 after power-up, PCI reset de-assertion, a D3 to D0 transition, or a software commanded EEPROM read (CTRL_EXT.EE_RST). Refer to the *Intel® 82575 Gigabit Ethernet Controller Software Developer's Manual* for more details.
- **Manageability Firmware Accessed**
  - In ASF mode, loaded by the 82575 in ASF mode after power-up, ASF Soft Reset (ASF FRC_RST), or software commanded ASF EEPROM read (ASF FRC_EELD). Refer to the *Alert Standards Format (ASF) Design Guide* for more details.
  - In Pass-Through (PT) mode, loaded by the 82575 in PT mode after power up or a firmware reset. Refer to the *Intel® 82575 GbE Controller System Manageability Interface* Application Note for more information.
- **Software Accessed —** Used by software only. These registers are listed in this document for convenience and are only for software and are ignored by the 82575.

The EEPROM interface supports Serial Peripheral Interface (SPI) mode 0 and expects the EEPROM to be capable of 2 MHz operation.

The 82575 is compatible with many sizes of 4-wire serial EEPROM devices. If ASF mode functionality is desired, a 2 KB (16 Kb) serial SPI-compatible EEPROM is recommended. If PT mode functionality (SMBus or NC-SI) is desired, a 32 KB (256 Kb) serial SPI-compatible EEPROM is recommended. If no manageability mode is desired, a 16 KB (128 Kb) serial SPI-compatible EEPROM can be used. All EEPROMs are accessed in 16-bit words although the EEPROM is designed to also accept 8-bit data accesses.

The 82575 automatically determines the address size to be used with the SPI EEPROM it is connected to and sets the *EEPROM Size* field of the EEPROM/Flash Control (EEC) and Data Register (EEC.EE_ADDR_SIZE; bit 10). Software uses this size to determine the EEPROM access method. The exact size of the EEPROM is stored within one of the EEPROM words.

Note: The different EEPROM sizes have two different numbers of address bits (8 bits or 16 bits). As a result, they must be accessed with a slightly different serial protocol. Software must be aware of this if it accesses the EEPROM using direct access.

1.2.1 Software Accesses

The 82575 provides two different methods for software access to the EEPROM. It can either use the built-in controller to read the EEPROM or access the EEPROM directly using the EEPROM's 4-wire interface.

Software can use the EEPROM Read register (EERD) to cause the 82575 to read a word from the EEPROM that the software can then use. To do this, software writes the address to read into the *Read Address* field (EERD.ADDR; bits 15:2) and simultaneously writes a 1b to the *Start Read* bit (EERD.START; bit 0). The 82575 then reads the word from the EEPROM, sets the *Read Done* bit (EERD.DONE; bit 1), and puts the data in the *Read Data* field (EERD.DATA; bits 31:16). Software can poll the EEPROM Read register until it sees the *Read Done* bit set, then use the data from the *Read Data* field. Any words read this way are not written to the 82575's internal registers.

Software can also directly access the EEPROM's 4-wire interface through the EEPROM/Flash Control register (EEC). It can use this for reads, writes, or other EEPROM operations.

To directly access the EEPROM, software should follow these steps:

1. Write a 1b to the *EEPROM Request* bit (EEC.EE_REQ; bit 6).
2. Read the *EEPROM Grant* bit (EEC.EE_GNT; bit 7) until it becomes 1b. It remains 0b as long as the hardware is accessing the EEPROM.
3. Write or read the EEPROM using the direct access to the 4-wire interface as defined in the EEPROM/Flash Control & Data register (EEC). The exact protocol used depends on the EEPROM placed on the board and can be found in the appropriate datasheet.
4. Write a 0b to the *EEPROM Request* bit (EEC.EE_REQ; bit 6).

Finally, software can cause the 82575 to re-read part of the hardware accessed fields of the EEPROM (setting the 82575's internal registers appropriately) by writing a 1b to the *EEPROM Reset* bit of the *Extended Device Control Register* (CTRL_EXT.EE_RST; bit 13).

Note: If the EEPROM does not contain a valid signature, the 82575 assumes 16-bit addressing. In order to access an EEPROM requiring 8-bit addressing, software must use the direct access mode.

1.2.2 Signature and CRC Fields

The only way the 82575 can discover whether an EEPROM is present is by trying to read the EEPROM. The 82575 first reads the EEPROM *Sizing & Protected* field Word at address 12h. The 82575 checks the signature value for bits 15 and 14. If bit 15 is 0b and bit 14 is 1b, it considers the EEPROM to be present and valid and reads additional EEPROM words and programs its internal registers based on the values read. Otherwise, it ignores the values it read from that location and does not read any other words.

In ASF Mode, the 82575's ASF function reads the ASF CRC word to determine if the EEPROM is valid. If the CRC is not valid, the ASF Configuration registers retain their default values. This CRC does not affect the remaining 82575 configuration, including the Management Control register. For details on how the CRC is calculated see Section 1.6.1.31.

1.2.3 Initial EEPROM Programming

In most applications, initial EEPROM programming is done directly on the EEPROM pins. Nevertheless, it is desirable to enable existing software utilities (accessing the EEPROM via the host interface) to initially program the whole EEPROM without breaking the protection mechanism. Following a power-up sequence, the 82575 reads the hardware initialization words in the EEPROM. If the signature in word 12h does not equal 01b the EEPROM is assumed as non-programmed. There are two effects for non-valid signature:

- The 82575 stops reading EEPROM data and sets the relevant registers to default values.
- The 82575 enables access to any location in the EEPROM via the EEPROM CSR registers.

1.2.4 EEPROM-Less Operation

The 82575 loads information from the EEPROM non-volatile memory storage into the device registers during the power-up sequence. If an EEPROM is not present, either by design or by fault, some of the device registers might not be tuned for normal operation. It is required that the following script be run immediately after an 82575 reset and before normal operation if an EEPROM is not detected.

Note: These actions are presented without comment because most of the settings involved are not customer tunable. They must be performed in order, and the loader function is included as follows. The example code is designed to be extensible to include other hardware families.

```
Definitions:

u32 is unsigned 32 bit value,

s32 is signed 32 bit value,

u8 is unsigned 8 bit value.

#define E1000_CCMCTL     0x05B48 /* CCM Control Register */

#define E1000_GIOCTL       0x05B44 /* GIO Analog Control Register */

#define E1000_SCCTL         0x05B4C /* PCIc PLL Cfg Register */

#define E1000_SCTL            0x00024  /* SerDes Control */

#define E1000_EECD           0x00010  /* EEPROM Control */

#define E1000_EECD_PRES      0x00000100 /* NVM Present */

#define E1000_GEN_CTL_READY             0x80000000

#define E1000_GEN_CTL_ADDRESS_SHIFT     8

#define E1000_GEN_POLL_TIMEOUT          640

Error codes are not required to be standard; programmers can define them as needed.
```

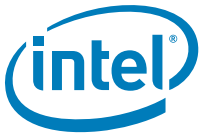
```
/* Is the EEPROM present?  If not then run the tuning script*/
if ((E1000_READ_REG(hw, E1000_EECD) & E1000_EECD_PRES) == 0)
    if (hw->mac.type == e1000_82575) {
        /* SerDes configuration via SERDESCTRL */
        e1000_write_8bit_ctrl_reg(E1000_SCTL, 0x00, 0x0C);
        e1000_write_8bit_ctrl_reg(E1000_SCTL, 0x01, 0x78);
        e1000_write_8bit_ctrl_reg(E1000_SCTL, 0x1B, 0x23);
        e1000_write_8bit_ctrl_reg(E1000_SCTL, 0x23, 0x15);

        /* CCM configuration via CCMCTL register */
        e1000_write_8bit_ctrl_reg(E1000_CCMCTL, 0x14, 0x00);
        e1000_write_8bit_ctrl_reg(E1000_CCMCTL, 0x10, 0x00);

        /* PCIe lanes configuration */
        e1000_write_8bit_ctrl_reg(E1000_GIOCTL, 0x00, 0xEC);
        e1000_write_8bit_ctrl_reg(E1000_GIOCTL, 0x61, 0xDF);
        e1000_write_8bit_ctrl_reg(E1000_GIOCTL, 0x34, 0x05);
        e1000_write_8bit_ctrl_reg(E1000_GIOCTL, 0x2F, 0x81);

        /* PCIe PLL Configuration */
        e1000_write_8bit_ctrl_reg(E1000_SCCTL, 0x02, 0x47);
        e1000_write_8bit_ctrl_reg(E1000_SCCTL, 0x14, 0x00);
        e1000_write_8bit_ctrl_reg(E1000_SCCTL, 0x10, 0x00);
             }
}

/**
 *  e1000_write_8bit_ctrl_reg - Write a 8bit CTRL register
 *  INPUTS
 *    reg: 32-bit register offset such as E1000_SCTL
 *   offset: register offset to write to
 *   data: data to write at register offset
 *
```



```
 *  Writes an address/data control type register.  There are several of these
 *  and they all have the format address << 8 | data and bit 31 is polled for
 *  completion.
 **/
s32
e1000_write_8bit_ctrl_reg (u32 reg, u32 offset, u8 data)
{
    u32 i, regvalue = 0;
    s32 ret_val = E1000_SUCCESS;

    /* Set up the address and data */
    regvalue = ((u32)data) | (offset << E1000_GEN_CTL_ADDRESS_SHIFT);
    E1000_WRITE_REG(reg, regvalue);

    /* Poll the ready bit to see if the MDI read completed */
    for (i = 0; i < E1000_GEN_POLL_TIMEOUT; i++) {
        usec_delay(5);
        regvalue = E1000_READ_REG(reg);
        if (regvalue & E1000_GEN_CTL_READY)
            break;
    }
    if (!(regvalue & E1000_GEN_CTL_READY)) {
        DEBUGOUT1("Reg %08x did not indicate ready\n", reg);
        ret_val = -E1000_ERR_PHY;
        }
    return ret_val;
}
```

1.3 Flash Interface Operation

The 82575 provides two different methods for software access to the Flash.

Using legacy Flash transactions, the Flash is read from, or written to, each time the host processor performs a read or a write operation to a memory location that is within the FLASH address mapping or at boot via accesses in the space indicated by the Expansion ROM Base Address register. All accesses to the Flash require the appropriate command sequence for the 82575 used. Refer to the specific Flash data sheet for more details on reading from or writing to Flash.

Accesses to the Flash are based on a direct decode of processor accesses to a memory window defined in either:

1. The 82575's Flash Base Address register (PCIe* Control register at offset 14h or 18h).
2. A certain address range of the IOADDR register defined by the IO Base Address register (PCIe* Control register at offset 18h or 20h).
3. The Expansion ROM Base Address register (PCIe* Control register at offset 30h).

The 82575 controls accesses to the Flash when it decodes a valid access.

Note: Flash read accesses must always be assembled by the 82575 each time the access is greater than a byte-wide access.

Note: The 82575 byte reads or writes to the Flash take on the order of 2 μs. The 82575 continues to issue retry accesses during this time.

Note: The 82575 supports only byte writes to the Flash.

Another way for software to access the Flash is directly using the Flash's 4-wire interface through the Flash Access register (FLA). It can use this for reads, writes, or other Flash operations (accessing the Flash status register, erase, etc.).

To directly access the Flash, software needs to:

1. Write a 1b to the Flash Request bit (FLA.FL_REQ)
2. Read the Flash Grant bit (FLA.FL_GNT) until it = 1b. It remains 0b as long as there are other accesses to the Flash.
3. Write or read the Flash using the direct access to the 4-wire interface as defined in the Flash Access register (FLA). The exact protocol used depends on the Flash placed on the board and can be found in the appropriate datasheet.
4. Write a 0b to the *Flash Request* bit (FLA.FL_REQ).

1.4 Shared EEPROM

The 82575 uses a single EEPROM device to configure hardware default parameters for both LAN devices including Ethernet Individual Addresses (IA), LED behaviors, receive packet-filters for manageability, and wakeup capability). Certain EEPROM words are used to specify hardware parameters that are LAN device-independent (such as those which affect circuits behavior). Other EEPROM words are associated with a specific LAN device. Both LAN devices access the EEPROM to obtain their respective configuration settings.

1.4.1 EEPROM Map Shared Words

The EEPROM map lists those words configuring either LAN devices or the entire 82575 as LAN 0/LAN 1 Both. Those words configuring a specific LAN's device parameters are identified as either LAN 0 or LAN 1.

The following EEPROM words warrant additional notes specifically related to dual-LAN support:

Ethernet Address (IA) (LAN 0/LAN 1 shared)	The EEPROM specifies the IA associated with the LAN 0 device and used as the hardware default of the Receive Address registers for that device. The hardware-default IA for the LAN 1 device is automatically determined by the same EEPROM word and is set to the value of {$IA_{LAN\ 0}$ XOR 010000000000h}.
Initialization Control 1, Initialization Control 2 (LAN 0/LAN 1 shared)	These EEPROM words specify hardware-default values for parameters that apply a single value to both LAN devices, such as link configuration parameters required for auto-negotiation, wakeup settings, PCI/PCI-X bus advertised capabilities, etc.
Initialization Control 3 (LAN 0, LAN 1 unique)	This EEPROM word configures default values associated with each LAN device's hardware connections, including which link mode (internal PHY) is used with this LAN device. Because a separate EEPROM word configures the defaults for each LAN, extra care must be taken to ensure that the EEPROM image does not specify a resource conflict.

1.5 Shared FLASH

The 82575 provides an interface to an external serial Flash/ROM memory device. This Flash/ROM device can be mapped into memory and/or I/O address space for each LAN device through the use of Base Address Registers (BARs). Bit 13 of the EEPROM Initialization Control Word 3 associated with each LAN device selectively disables/ enables whether the Flash can be mapped for each LAN device by controlling the BAR register advertisement and write ability.

1.6 EEPROM Map

Table 1 lists the EEPROM map for the 82575.

Table 1. 82575 EEPROM Map

Word	Used By[1]	High Byte (15:8)	Low Byte (7:0)	Image Value	LAN 0/1
00h	HW	Ethernet Address Byte 2	Ethernet Address Byte 1	IA(2,1)	Both
01h	HW	Ethernet Address Byte 4	Ethernet Address Byte 3	IA(4,3)	Both
02h	HW	Ethernet Address Byte 6	Ethernet Address Byte 5	IA(6,5)	Both
03h: 07h	SW	Compatibility (High Byte)	Compatibility (Low Byte)	0000h	Both
08h	SW	PBA Byte 1	PBA Byte 2		
09h	SW	PBA Byte 3	PBA Byte 4		
0Ah	HW	Initialization Control 1			All
0Bh	HW	Subsystem ID			Both
0Ch	HW	Subsystem Vendor ID			All
0Dh	HW	Device ID			LAN 0
0Eh	HW	Reserved			All
0Fh	HW	Initialization Control 2			All
10h	HW	Software Defined Pins Control			LAN 1
11h	HW	Device ID			LAN 1
12h	HW	EEPROM Sizing & Protected Fields			Both
13h	HW	Reserved			Both
14h	HW	Initialization Control 3		XXXXh	LAN 1
15h	HW	NC-SI Configuration	PCIe* Completion Timeout Configuration		Both
16h	HW	MSI-X Configuration			Both
17h	FW	Firmware Start Address (Including PHY Initialization Address)			Both
18h	HW	PCIe* Initialization Configuration 1			Both
19h	HW	PCIe* Initialization Configuration 2			Both
1Ah	HW	PCIe* Initialization Configuration 3			Both
1Bh	HW	PCIe* Control			Both
1Ch	HW	LEDCTL 1 3 Default			Both
1Dh	HW	Dummy Function Device ID			Both
1Eh	HW	Device Revision ID			Both
1Fh	FW	LEDCTL 0 2 Default			Both
20h	HW	Software Defined Pins Control			LAN 0
21h	HW	Functions Control			Both
22h	HW	LAN Power Consumption		280Ch	Both
23h	HW	Management Hardware Configuration Control			Both
24h	HW	Initialization Control 3		XXXXh	LAN 0
25h: 2Bh	HW	Reserved			Both
2Ch	HW	End of RO Area			Both

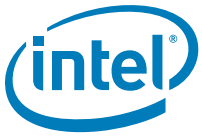


Table 1. 82575 EEPROM Map

Word	Used By[1]	High Byte (15:8)	Low Byte (7:0)	Image Value	LAN 0/1
2Dh	HW	Start of RO Area			Both
2Eh	HW	Watchdog Configuration			Both
2Fh	OEM	VPD Pointer			
30h	PXE	PXE Word 0 (Software Use) Configuration			
31h	PXE	PXE Word 1 (Software Use) Configuration			
32h	PXE	PXE Word (Software Use) PXE Version			
33h	PXE	PXE Word (Software Use) EFI Version			
34h: 3Ch	PXE	PXE Words			
3Dh	PXE	iSCSI Boot Configuration Start Address			
3Eh	PXE	PXE Word			
3Fh	PXE	Software Checksum (words 00h to 3Fh)			
40h: 4Fh	HW	Reserved			
50h: 53h	FW	Common Firmware Pointers			MNG
54h	FW	MNG Capabilities			MNG
55h: 5Ah	FW	ASF/PT Pointers			MNG
5Bh: . . .	FW	Firmware Structure			MNG

1. This column specifies whether this byte is used by hardware (HW), software (SW) or firmware (FW). EEPROM words can also be used by Preboot eXecution Environment (PXE) code or Alert Standard Format (ASF).

1.6.1 Hardware Accessed Words

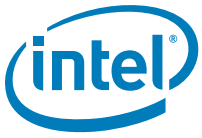
This section describes the EEPROM words that are loaded by the 82575 hardware. Most of these bits are located in configuration registers. The words are only read and used if the signature field in the EEPROM Sizing & Protected Fields (word 12h) is valid.

Note: When changing the default value of a reserved bit, 82575 behavior is undefined.

The following table lists the auto-load sequence.

Table 2. EEPROM Auto-Load Sequence

Full Reset	Reset of LAN0 Only	Reset of LAN1 Only	Comments
012	012	012	
00A	00A	00A	
018			
019			
01A			
01B			
026			
027			
028			
029			
02A			
02B			
025			
021			
01E			
015			
016			
014			
024			
01C			
01F			
02C			
02D			
022			
00B			Loaded only if load subsystem ID bit is set
00C			
00D			Loaded only if load device ID bit is set
01D			
011			
00F	00F	00F	
040			
041			



Full Reset	Reset of LAN0 Only	Reset of LAN1 Only	Comments
044			
047			
04E			
04F			
000	000	000	
001	001	001	
002	002	002	
020	020		
010		010	
02E	02E	02E	

1.6.1.1 Ethernet Address (Words 00h – 02h)

The Ethernet Individual Address (IA) is a 6-byte field that must be unique for each Ethernet port and each copy of the EEPROM image. The first three bytes are vendor specific. The value from this field is loaded into the Receive Address Register 0 (RAL0/ RAH0).

The Ethernet address is loaded for LAN0 and bit 41 (8th MSB) is inverted for LAN1 (bit 0 byte 6 in the EEPROM = bit 8 in EEPROM word 2.

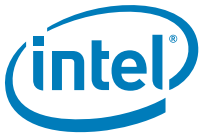
1.6.1.2 Initialization Control 1 (Word 0Ah)

This word read by the 82575 contains initialization values that:

- Set defaults for some internal registers.
- Enable or disable specific features.
- Determine which PCI configuration space values are loaded from the EEPROM.

Table 3. Initialization Control 1 (Word 0Ah)

Bit(s)	Name	Default	Description
15:12	Reserved	0000b	Reserved
11	FRCSPD	1b	Default setting for the *Force Speed* bit in the Device Control register (CTRL[11]). The hardware default value is 1b. 0b = Do not force. 1b = Force.
10	FD	1b	Default for duplex setting. Mapped to Device Control register bit 0. The hardware default value is 1b. 0b = Half duplex. 1b = Full duplex.
9	LRST	1b	Default setting for link reset (CTRL[3]). It should set to 0b for hardware to initiate Auto-Negotiation upon power up or assertion of a PCIe* reset without driver intervention. The hardware default value is 1b. 0b = Initiate auto-negotiation. 1b = Do not initiate auto-negotiation.
8:7	Reserved	00b	Reserved.
6	SDP_ IDDQ_EN	0b	When set, SDP keeps their value and direction when the 82575 enters dynamic IDDQ mode. Otherwise, SDP moves to HighZ and pull up mode in dynamic IDDQ mode.
5	Deadlock Timeout Enable	1b	If set, a device granted access to the EEPROM that does not toggle the interface for more than 1 second might have the grant revoked. 0b = Disable. 1b - Enable.
4	ILOS	0b	Default setting for the Loss-of-Signal Polarity setting for CTRL[7]. The hardware default value is 0b.
3	Power MNG	1b	This bit defines the 82575 power management support: 0b = The power management registers set is read only. The 82575 does not execute a hardware transition to D3. **Note:** This setting is for testing purposes only. 1b = Full support for power management. For normal operation, this bit must be set to 1b.
2	Reserved	0b	Reserved.
1	Load Subsys-tem ID	1b	When this bit equals 1b, the 82575 loads its PCIe* Subsystem ID and Subsystem Vendor ID from the EEPROM words 0Bh and 0Ch. 0b = Do not load. 1b = Load.
0	Load Vendor/ Device ID	1b	When this bit is set to 1b, the 82575 loads its PCIe* device ID from EEPROM words 0Dh, 11h, and 1Dh. 0b = Do not load. 1b = Load.



1.6.1.3 Subsystem ID (Word 0Bh)

If the Load Subsystem IDs bit in the Initialization Control Word 1 (0Ah) is set, this word is used to initialize the Subsystem ID. Its default value is 0h.

1.6.1.4 Subsystem Vendor ID (Word 0Ch)

If the Load Subsystem IDs bit in the Initialization Control Word 1 (0Ah) is set, this word is used to initialize the Subsystem Vendor ID. Its default value is 8086h.

1.6.1.5 Device ID (Word 0Dh, 11h)

If the Load Device IDs bit in the Initialization Control Word 1 (0Ah) is set, this word is used to initialize the Device ID of LAN0 and LAN1 functions, respectively. Its default value is 10A7h.

1.6.1.6 Dummy Device ID (Word 1Dh)

If the Load Device IDs in word 0Ah is set, this word is used to initialize the Device ID of dummy devices. Its default value is 10A6h

1.6.1.7 Initialization Control 2 (Word 0Fh)

This is the second word read by the 82575 and contains additional initialization values that:

- Set defaults for some internal registers.
- Enable and disable specific features.

Table 4. Initialization Control 2 (Word 0Fh)

Bit(s)	Name	Default	Description
15	APM PME# Enable	0b	The *APM PME# Enable* bit represents the initial value of the Assert PME On APM Wakeup bit in the Wake Up Control Register (WUC.APMPME). 0b = Disable 1b = Enable
14	Reserved	0b	Reserved. Should be set to 0b.
13:12	Pause Capability	11b	These bits enable the desired PAUSE capability for the advertised configuration base page. Mapped to PCS_ANADV.ASM.
11	ANE	0b	This bit enables Auto-Negotiation and is mapped to PCS_LCTL.AN_ENABLE. 0b = Disable. 1b = Enable.
10:8	Flash Size Indication	000b	Requested flash Memory Space: 000b = 64 KB 001b = 128 KB 010b = 256 KB 011b = 512 KB 100b = 1 MB 101b = 2 MB 110b = 4 MB 111b = 8 MB
7	DMA Clock Gating Enable	1b	Enables automatic reduction of DMA and MAC frequency. Mapped to STATUS[31]. This bit is relevant only if the L1 indication enable is set. 0b = Disable. 1b = Enable.

Table 4. Initialization Control 2 (Word 0Fh)

Bit(s)	Name	Default	Description
6	PHY Power Down Enable	1b	This bit enables the PHY to power down. When it is set, the PHY can enter into a low power state. 0b = Disable. 1b = Enable.
5	Reserved	0b	Reserved.
4	CCM PLL Shutdown Enable	0b	When set, the CCM PLL can be shut down in low power states when the PHY is in power-down (link disconnect). When cleared, the CCM PLL is not shut down in a low-power state. 0b = Disable. 1b = Enable.
3	L1 Indication Enable	0b	When set, enables idle indication to the L1 mechanism. 0b = Disable. 1b = Enable.
2	SerDesLow Power Enable	0b	When this bit is set, the SerDes can enter a low power state when the function is in Dr state. This bit is mapped to CTRL_EXT[18]. 0b = Disabled. 1b = Enabled.
1	Reserved	0b	Reserved. Should be set to 0b.
0	LPLU	1b	Low Power Link Up Enables the decrease in link speed in non-D0a states when dictated by power policy and the power management state. This bit is loaded to each of the PHYs only when LAN0/1 OEM bits disable (word 23 bit 7/8) respectively, are cleared. 0b = Disable. 1b = Enable.

1.6.1.8 Software Defined Pins Control (Word 10h)

This word configures initial settings for the Software Definable Pins.

Note: Word 10h is for LAN1.

Table 5. Software Defined Pins Control (Word 10h)

Bit(s)	Name	Default	Description
15	SDPDIR[3]	0b	SDP3 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP3_IODIR* bit in the Extended Device Control (CTRL_EXT) register following power up. 0 = Input. 1b = Output. Set to 1b if not using SDP.
14	SDPDIR[2]	0b	SDP2 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP2_IODIR* bit in the Extended Device Control (CTRL_EXT) register following power up. 0 = Input. 1b = Output. Set to 1b if not using SDP.
13	PHY_in_ LAN_ disable	0b	Determines the behavior of the MAC and PHY when a LAN port is disabled through an external pin. 0b = MAC and PHY maintain functionality while in LAN Disable (to support manageability). 1b = MAC and PHY are powered down in LAN Disable (manageability cannot access the network through this port).
12	Reserved	0b	Reserved. Should be set to 0b.

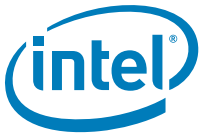


Table 5. Software Defined Pins Control (Word 10h)

Bit(s)	Name	Default	Description
11	LAN_DIS	0b	LAN Disable. When this bit is set to 1b, the appropriate LAN is disabled. 0b = Enable. 1b = Disable.
10	LAN_PCI_DIS	0b	LAN PCI Disable. When this bit is set to 1b, the appropriate LAN PCI function is disabled. For example, the LAN is functional for MNG operation but is not connected to the host through PCIe*. 0b = Enable. 1b = Disable.
9	SDPDIR[1]	0b	SDP1 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP1_IODIR* bit in the Device Control (CTRL) register following power up. 0b = Input. 1b = Output. Set to 0b is not using SDP.
8	SDPDIR[0]	0b	SDP0 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP00_IODIR* bit in the Device Control (CTRL) register following power up. 0b = Input. 1b = Output. Set to 0b is not using SDP.
7	SDPVAL[3]	0b	This bit holds the value of the SDP3 pin (Initial Output Value). It configures the initial power-on value output of SDP3 when it is configured as an output. This is accomplished by configuring the initial hardware value of the SDP3_DATA bit in the Extended Device Control (CTRL_EXT) register after power up.
6	SDPVAL[2]	0b	SDP2 Pin - Initial Output Value. This bit configures the initial power on value output of SDP2 (when it is configured as an output) by configuring the initial hardware value of the *SDP2_DATA* bit in the Extended Device Control (CTRL_EXT) register after power up.
5	WD_SDP0	0b	When set, SDP[0] is used as watchdog timeout indication. When reset, it is used as a Software Defined Pin (as per bits 8 and 0). This bit is mapped to SDP0_WDE[21] in the CTRL register. 0b = SDP0 is used normally as SDP. 1b = SDP0 is used as a watchdog timeout indication.
4	Gigabit Disable	0b	When this bit is set, the Gigabit Ethernet operation is disabled. An example of when this might be used is if Gigabit Ethernet operation exceeds system power limits. Software configures this bit only if the LAN1/LAN0 OEM Bit configuration disable (word 23h, bits 8:7) are cleared. Hardware does not use this bit. 0b = Enable. 1b = Disable.
3	Disable 1000 in non-D0a	0b	Disables 1000 Mb/s operation in non-D0a states. This bit is for software use. Hardware does not use this bit. 0b = Enable. 1b = Disable
2	D3COLD_WAKEUP_ADVEN	1b	Configures the initial hardware default value of the *ADVD3WUC* bit in the Device Control register (CTRL) after power up. 0b = Advertised. 1b = Not advertised.
1	SDPVAL[1]	0b	SDP1 Pin - Initial Output Value. This bit configures the initial power on value output of SDP2 (when it is configured as an output) by configuring the initial hardware value of the *SDP1_DATA* bit in the Device Control (CTRL) register after power up.
0	SDPVAL[0]	0b	SDP0 Pin - Initial Output Value. This bit configures the initial power on value output of SDP2 (when it is configured as an output) by configuring the initial hardware value of the *SDP0_DATA* bit in the Device Control (CTRL) register after power up.

1.6.1.9 EEPROM Sizing & Protected Fields (Word 12h)

Provides common power consumption and other indications about EEPROM size and protection.

Note: The software driver can only read this word. It has no write access to this word through the EEC and EERD registers. Write access is possible only through an authenticated firmware interface.

Table 6. EEPROM Sizing & Protected Fields (Word 12h)

Bit(s)	Name	Default	Description
15:14	Signature	01b	The Signature field indicates to the device that there is a valid EEPROM present. If the Signature field is not 01b, the other bits in this word are ignored, no further EEPROM read is performed and default values are used for the configuration space IDs.
13:10	EEPROM Size	0010b	These bits indicate the actual EEPROM size and are mapped to EEC[14:11]: 0000b = 128 bytes 0001b = 256 bytes 0010b = 512 bytes 0011b = 1 KB 0100b = 2 KB 0101b = 4 KB 0110b = 8 KB 0111b = 16 KB 1000b = 32 KB 1001b - 1011b = Reserved
9:0	Reserved	00h	Reserved. Should be set to 00h.

1.6.1.10 Initialization Control 3 (Word 14h, 24h)

This word controls general initialization values. Word 14h is used for LAN1. Word 24 is used for LAN0.

Table 7. Initialization Control 3 (Word 14h and 24h High Byte)

Bit(s)	Name	Default	Description
15	SerDes Energy Source	0b	SerDes Energy Source Detection When 0b, internal SerDes Rx electrical Idle indication. When 1b, external LOS signal. This bit also indicates the source of the signal detect while establishing a link in SerDes mode. This bit sets the default value of the CONNSW.ENRGSRC bit.
14	I2C SFP Enable	0b	I2C SFP Enable 0b = Disabled. When disabled, the I2C pads are isolated. 1b = Enabled. Used to set the default value of CTRL_EXT[25].
13	LAN Flash Disable	1b	A bit value of 1b disables the Flash logic. The Flash access BAR in the PCI Configuration space is disabled.

Table 7. Initialization Control 3 (Word 14h and 24h High Byte)

Bit(s)	Name	Default	Description
12:11	Interrupt Pin	0b for LAN 0 1b for LAN 1	This bit controls the value advertised in the *Interrupt Pin* field of the PCI Configuration header for this device and function. A value of 0b reflected in the *Interrupt Pin* field indicates that this device uses INTA#; a value of 1b indicates that this device uses INTB#. If only a single port of the 82575 is enabled, this value is ignored and the *Interrupt Pin* field of the enabled port reports INTA# usage. 0 = INT#A 1 = INT#B 2 = INT#C 3 = INT#D
10	APM Enable	1b	This field controls the initial value of Advanced Power Management Wake Up Enable in the Wake Up Control Register (WUC.APME) and is mapped to CTRL[6] and to WUC[0]. 0b = APM wakeup disabled. 1b= =APM wakeup enable.
9:8	Link Mode	00b	This field controls the initial value of Link Mode bits of the Extended Device Control Register (CTRL_EXT.LINK_MODE), specifying which link interface and protocol is used by the MAC. 00b = MAC operates in 1000Base-T mode with the internal copper PHY. 01b = MAC operates using internal SerDes module (legacy). 10b = MAC operates in SGMII mode. 11b = MAC operates in internal SerDes mode (recommended).
7	Expansion BAR Enable	0b	Enable/disable Expansion ROM BAR 0b = Enable. 1b = Disable.
6:5	Reserved	-	Reserved.
4:2	Reserved	000b	Reserved.
1	Ext_VLAN	0b	Sets the default for CTRL_EXT[26] bit. Indicates that additional VLAN is expected in the system. 1b = Expect additional VLAN in all packets. 0b = Don't expect additional VLAN.
0	Keep_ PHY_ Link_Up_ En	0b	Enables No PHY Reset when the BMC indicates that the PHY should be kept on. When asserted, this bit prevents the PHY reset signal and the power changes reflected to the PHY according to the MANC.Keep_PHY_Link_Up value. This bit should be set to the same value at both words (14h, 24h) to reflect the same option to both LANs. 1b = Enable. 0b = Disable.

The description of bits 13 and 11 in various combinations are as follows:

Flash Disable (Bit 13)	Boot Disable (Bit 11)	Functionality (Active Windows)
0b	0b	Flash and Expansion ROM Bars are active.
0b	1b	Flash BAR is enabled and Expansion ROM BAR is disabled.
1b	0b	Flash BAR is disabled and Expansion ROM BAR is enabled.
1b	1b	Flash and Expansion ROM BARs are disabled.

1.6.1.11 NC-SI and PCIe* Completion Timeout Configuration (Word 15h)

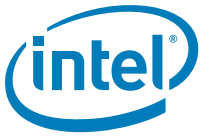
Table 8. NC-SI and PCIe* Completion Timeout Configuration (Word 15h)

Bit(s)	Name	Default	Description
15	NC-SI Clock Pad Drive Strength	0b	Defines the driving strength of the NC-SI_CLK_OUT pad.
14	NC-SI Data Pad Drive Strength	0b	Defines the drive strength of the NC-SI_DV & NC-SI_RXD pads.
13	NC-SI Output Clock Disable	0b	If set, the clock source is external. In this case, the NC-SI_CLK_OUT pad is kept stable at zero and the NC-SI_CLK_IN pad is used as an input source of the clock. If cleared, the 82575 outputs the NC-SI clock through the NC-SI_CLK_OUT pad. The NC-SI_CLK_IN pad is still used as an NC-SI clock input. If NC-SI is not used, then this bit is set. If this bit is cleared, the Device Dr Power Down Enable in word 0Fh should not be set. 0b = Output clock enabled. 1b = Output clock enable.
12:8	Reserved	-	Reserved.
7	Com-pletion Timeout Disable	0b	This bit is loaded into the GCR.Completion_Timeout_Disable bit. 0b = Completion timeout enabled. 1b = Completion timeout disabled.
6:5	Com-pletion Timeout Value	00b	These bits are loaded into the GCR.Completion_Timeout_Value bit. 00b = 50 µs - 10 ms. 01b = 10 ms - 200 ms. 10b = 200 ms - 4 s. 11b = 4 s - 64 s.
4	Com-pletion Timeout Resend	1b	This bit is loaded into the GCR.Completion_Timeout_Resend bit. 0b = Do not resend request on completion timeout. 1b = Resend request on completion timeout.
3:0	Reserved	0000b	Reserved.

1.6.1.12 MSI-X Configuration (Word 16h)

Table 9. MSI-X Configuration (Word 16h)

Bit(s)	Name	Default	Description
15:12	MSI-X0_N	9h	This field specifies the number of entries in MSI-X tables of LAN 0. The range is 0-15. MSI_X_N is equal to the number of entries minus one.
11:8	MSI-X1_N	9h	This field specifies the number of entries in MSI-X tables of LAN 0. The range is 0-15. MSI_X_N is equal to the number of entries minus one.
7:5	Reserved	-	Reserved.
4:0	PCIE_ EIDLE_ DLY	0h	PCIe* Electrical Idle Delay Delay cycles before entering electrical idle to allow a data path flush.



1.6.1.13 PLL/Lane/PHY Initialization Pointer (Word 17h)

Bit(s)	Name	Default	Description
15:0			PLL/Lane/PHY Initialization Pointer

1.6.1.14 PCIe* Initialization Configuration 1 (Word 18h)

This field sets default values for some internal registers and enables or disables specific features.

Table 10. PCIe* Initialization Configuration 1 (Word 18h)

Bit(s)	Name	Default	Description
15	Reserved	0b	Reserved. Should be set to 0b.
14:12	L1 Act Exit Latency	110b	This field represents the L1 active exit latency for the configuration space. When it is set to 110b, the latency range is 32 µs to 64 µs.
11:9	L1 Act Accept Latency	110b	This field represents the L1 active acceptable latency for the configuration space. When it is set to 110b, the acceptable latency range is 32 µs to 64 µs.
8:6	L0s Accept Latency	011b	This field represents the L0s acceptable latency for the configuration space. When it is set to 011b, the acceptable latency is 512 ns.
5:3	L0s Separated Exit Latency	001b	This field represents the L0s exit latency for active state power management with a separated reference clock. When it is set to 001b, the latency range is between 64 ns and 128 ns.
2:0	L0s Common Exit Latency	001b	This field represents the L0s exit latency for active state power management with a common reference clock. When it is set to 001b, the latency range is between 64 ns and 128 ns.

1.6.1.15 PCIe* Initialization Configuration 2 (Word 19h)

This word sets default values for some internal registers.

Table 11. PCIe* Initialization Configuration 2 (Word 19h)

Bit(s)	Name	Default	Description
15	DLLP Timer Enable	0b	When it is set to 1b, the DLLP timer counter is enabled. 0b = Disable. 1b = Enable.
14	Reserved	0b	Reserved.
13	Reserved	0b	Reserved.
12	Serial Number Capability	1b	Serial Number Capability Enable. Should be set to 1b.
11:8	Extra NFTS	0000b	Extra NFTS (Number of Fast Training Signal) that is added to the original requested number of NFTS (as requested by the upstream component).
7:0	NFTS	50h	This field identifies the number of special sequences for L0s transition to L0.

1.6.1.16 Software Defined Pins Control (Word 20h)

This configures initial settings for the Software Definable Pins.

Note: Word 20h is for LAN0.

Table 12. Software Defined Pins Control (Word 20h)

Bit(s)	Name	Default	Description
15	SDPDIR[3]	0b	SDP3 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP3_IODIR* bit in the Extended Device Control (CTRL_EXT) register following power up. 0b = Input. 1b = Output. Set to 1b if not using SDP.
14	SDPDIR[2]	0b	SDP2 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP2_IODIR* bit in the Extended Device Control (CTRL_EXT) register following power up. 0b = Input. 1b = Output. Set to 1b if not using SDP.
13	PHY_in_ LAN_ disable	0b	Determines the behavior of the MAC and PHY when a LAN port is disabled through an external pin. 0b = MAC and PHY maintain functionality while in LAN Disable (to support manageability). 1b = MAC and PHY are powered down in LAN Disable (manageability cannot access the network through this port).
12:10	Reserved	000b	Reserved. Should be set to 000b.
9	SDPDIR[1]	0b	SDP1 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP1_IODIR* bit in the Device Control (CTRL) register following power up. 0b = Input. 1b = Output. Set to 0b if not using SDP.
8	SDPDIR[0]	0b	SDP0 Pin - Initial Direction. This bit configures the initial hardware value of the *SDP00_IODIR* bit in the Device Control (CTRL) register following power up. 0b = Input. 1b = Output. Set to 1b if not using SDP.
7	SDPVAL[3]	0b	This bit holds the value of the SDP3 pin (Initial Output Value). It configures the initial power-on value output of SDP3 when it is configured as an output. This is accomplished by configuring the initial hardware value of the SDP3_DATA bit in the Extended Device Control (CTRL_EXT) register after power up.
6	SDPVAL[2]	0b	SDP2 Pin - Initial Output Value. This bit configures the initial power on value output of SDP2 (when it is configured as an output) by configuring the initial hardware value of the *SDP2_DATA* bit in the Extended Device Control (CTRL_EXT) register after power up.
5	WD_SDP0	0b	When set, SDP[0] is used as watchdog timeout indication. When reset, it is used as a Software Defined Pin (as per bits 8 and 0). This bit is mapped to SDP0_WDE[21] in the CTRL register. 0b = SDP0 is used normally as SDP. 1b = SDP0 is used as a watchdog timeout indication.

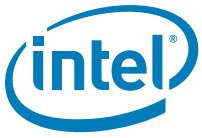


Table 12. Software Defined Pins Control (Word 20h)

Bit(s)	Name	Default	Description
4	Gigabit Disable	0b	When this bit is set, the Gigabit Ethernet operation is disabled. An example of when this might be used is if Gigabit Ethernet operation exceeds system power limits. Software configures this bit only if the LAN1/LAN0 OEM Bit configuration disable (word 23h, bits 8:7) are cleared. Hardware does not use this bit. 0b = Enable. 1b = Disable.
3	Disable 1000 in non-D0a	0b	Disables 1000 Mb/s operation in non-D0a states. This bit is for software use. Hardware does not use this bit. 0b = Enable. 1b = Disable.
2	D3COLD_WAKEUP_ADVEN	1b	Configures the initial hardware default value of the *ADVD3WUC* bit in the Device Control register (CTRL) after power up. 0b = Advertised. 1b = Not advertised.
1	SDPVAL[1]	0b	SDP1 Pin - Initial Output Value. This bit configures the initial power on value output of SDP2 (when it is configured as an output) by configuring the initial hardware value of the *SDP1_DATA* bit in the Device Control (CTRL) register after power up.
0	SDPVAL[0]	0b	SDP0 Pin - Initial Output Value. This bit configures the initial power on value output of SDP2 (when it is configured as an output) by configuring the initial hardware value of the *SDP0_DATA* bit in the Device Control (CTRL) register after power up.

1.6.1.17 PCIe* Initialization Configuration 3 (Word 1Ah)

This word sets default values for some internal registers.

Table 13. PCIe* Initialization Configuration 3 (Word 1Ah)

Bit(s)	Name	Default	Description
15	Master Enable	1b	When this bit is set to 1b, the PHY can act as a master (upstream component with cross link functionality). 0b = Disable. 1b = Enable.
14	Scramble Disable	0b	When this bit is set to 1b, the PCIe* LFSR scrambling feature is disabled. 0b = Enable. 1b = Disable.
13	Ack/Nak Scheme	0b	This field identifies the acknowledgement/no acknowledgement scheme for the 82575. 0b = Scheduled for transmission following any TLP. 1b = Scheduled for transmission according to time-outs specified in the PCIe* specification.
12	Cache Line Size	0b	This bit represents the cache line size. 0b = 64 bytes. 1b = 128 bytes. **Note:** The value loaded must be equal to the actual cache line size used by the platform as configured by system software.

Table 13. PCIe* Initialization Configuration 3 (Word 1Ah)

Bit(s)	Name	Default	Description
11:10	GIO Capability	01b	PCIe* Capability Version The value of this field is reflected in the two LSBs of the capability version in the PCIe* CAP register (configuration space - A2h). Note that this is not the PCIe* version. It is the PCIe* capability version. This version is a field in the PCIe* capability structure and is not the same as the PCIe* version. It changes only when the content of the capability structure changes. For example, PCIe* 1.0, 1.0a and 1.1 all have a capability version of 1. PCIe* 2.0 has a version 2 because it added registers to the capabilities structures.
9	IO Support	1b	This bit represents the status of I/O support (I/O BAR request). When it is set to 1b, I/O is supported. 0b = Not supported. 1b = Supported.
8	Max Packet Size	1b	This bit identifies the status of the default packet size. 0b = 128 bytes. 1b = 256 bytes.
7:6	Lane Width	10b	This field identifies the maximum link width. 00b = 1 lane. 01b = 2 lanes. 10b = 4 lanes. 11b = Reserved.
5	Elastic Buffer Diff1	0b	When this bit is set to 1b, the elastic buffers are activated in a more limited mode (read and write pointers).
4	Elastic Buffer Control	0b	When this bit equals 1b, the elastic buffers operate under phase-only mode during electrical idle states.
3:2	Active State PM Support	11b	This field determines support for Active State Link Power Management. It is loaded into the PCIe* Active State Link PM Support register. 00b = Reserved. 01b = L0s entry supported. 10b = Reserved. 11b = L0s and L1 supported.
1	Slot Clock Cfg	1b	When this bit is set, the 82575 uses the PCIe* reference clock supplied on the connector. This is primarily used for add-in solutions.
0	Loopback Polarity Inversion	0b	This field verifies the polarity inversion in loopback master entry.

1.6.1.18 PCIe* Control (Word 1Bh)

This word configures initial settings for the PCIe* default functionality.

Table 14. PCIe* Control (Word 1Bh)

Bit(s)	Name	Default	Description
15	Reserved	0b	Reserved.
14	Dummy Function Enable	0b	Dummy Function Enable 0b = Disabled function 0 is replace with function 1. 1b = Disabled function 0 is replaced with dummy function.
13	GIO Down Reset Disable	0b	This bit disables a core reset when the PCIe* link goes down. 0b = Enable. 1b = Disable.

Table 14. PCIe* Control (Word 1Bh)

Bit(s)	Name	Default	Description
12	Lane Reversal Disable	0b	This bit disables the ability to negotiate lane reversal. 0b = Enable. 1b = Disable.
11	Good Recovery	0b	When set to 1b, the LTSSM Recovery states always progresses towards LinkUp (force a good recovery, when a recovery occurs). 0b = Normal mode.
10	Reserved	1b	Reserved. Should always be set to 1b. 0b - Enable. 1b = Disable.
9:7	Reserved	000b	Reserved. Always set to 000b.
6	GIO TS Retrain Mode	0b	This bit controls the condition of LTSSM entry to recovery. 0b = Normal mode. 1b = Special mode.
5	L2 Disable	0b	This bit disables the link from entering L2 state. 0b = Enable. 1b = Disable.
4	Skip Disable	0b	This bit disables the SKIP symbol insertion in the elastic buffer. 0b = Enable. 1b = Disable.
3	Reserved	0b	Reserved.
2	Electrical Idle	0b	Electrical Idle Mask. When set to 1b, disables the check for illegal electrical idle sequence (for example, eidle ordered set without common mode and vise versa). Also excepts any of them as a correct eidle sequence. 0b = Enable. 1b = Disable **Note:** Specification can be interpreted so that the eidle ordered set is sufficient for transition to power management states. The use of this bit allows an exception for such interpretation and avoids the possibility of correct behavior being understood as illegal sequences.
1:0	Latency to Enter L1	11b	These bits identify the period in L0s state before transitioning into an L1 state. 00b = 64 µs 01b = 256 µs 10b = 1 ms 11b = 4 ms

1.6.1.19 LED 1, 3 Configuration Defaults (Word 1Ch)

This EEPROM word specifies the hardware defaults for the LEDCTL register fields controlling the LED1 (ACTIVITY indication) and LED3 (LINK_1000 indication) output behaviors.

Table 15. LED 1-3 Configuration Defaults (Word 1Ch)

Bit(s)	Name	Default	Description
15	LED3 Blink	0b	This bit represents the initial value of the LED3_BLINK field. If it equals 0b, the LED is non-blinking.
14	LED3 Invert	0b	This bit represents the initial value of the LED3_IVRT field. If it equals 0b, it is an active low output.
13	Reserved	0b[1]	Reserved.
12	Reserved	0b	This bit is reserved and should be set to 0b.

Table 15. LED 1-3 Configuration Defaults (Word 1Ch)

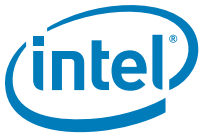
Bit(s)	Name	Default	Description
11:8	LED3 Mode	0111b	This field represents the initial value of the LED3_MODE specifying the event, state, and pattern displayed on the LED3 (LINK_1000) output. A value of 0111b (or 7h) causes this to indicate 1000 Mb/s operation. See Table 16 for all available LED modes.
7	LED1 Blink	1b	This field holds the initial value of LED1_BLINK field and is equal to 0b for non-blinking.
6	LED1 Invert	0b	This field holds the initial value of LED1_IVRT field and is equal to 0b for an active low output.
5	Reserved	0b[a]	Reserved.
4	Reserved	0b	This bit is reserved and should be set to 0b.
3:0	LED1 Mode	0011b	This field represents the initial value of the LED1_MODE specifying the event, state, and pattern displayed on the LED1 (ACTIVITY) output. A value of 0011b (3h) causes this to indicate ACTIVITY state. See Table 16 for all available LED modes.

1. These bits are read from the EEPROM.

Note: A value of 0703h is used to configure default hardware LED behavior equivalent to 82544-based copper Ethernet controllers (LED0=LINK_UP, LED1=blinking ACTIVITY, LED2=LINK_100, and LED3=LINK_1000).

Table 16. LED Mode

Mode	Selected Mode	Source Indication
0000b	LINK_10/1000	Asserted when either 10 or 1000 Mb/s link is established and maintained.
0001b	LINK_100/1000	Asserted when either 100 or 1000 Mb/s link is established and maintained.
0010b	LINK_UP	Asserted when any speed link is established and maintained.
0011b	FILTER_ACTIVITY	Asserted when link is established and packets are being transmitted or received that passed MAC filtering.
0100b	LINK/ACTIVITY	Asserted when link is established and when there is no transmit or receive activity.
0101b	LINK_10	Asserted when a 10 Mb/s link is established and maintained.
0110b	LINK_100	Asserted when a 100 Mb/s link is established and maintained.
0111b	LINK_1000	Asserted when a 1000 Mb/s link is established and maintained.
1000b	SDP_MODE	LED activation is a reflection of the SDP signal. SDP0, SDP1, SDP2, SDP3 are reflected to LED0, LED1, LED2, LED3 respectively.
1001b	FULL_DUPLEX	Asserted when the link is configured for full duplex operation (de-asserted in half-duplex).
1010b	COLLISION	Asserted when a collision is observed.
1011b	ACTIVITY	Asserted when link is established and packets are being transmitted or received.
1100b	BUS_SIZE	Asserted when the 82575 detects a 1-lane PCIe* connection.



Mode	Selected Mode	Source Indication
1101b	PAUSED	Asserted when the 82575's transmitter is flow controlled.
1110b	LED_ON	Always high (Asserted)
1111b	LED_OFF	Always low (De-asserted)

1.6.1.20 Device Revision ID (Word 1Eh)

Table 17. Device Revision ID (Word 1Eh)

Bit(s)	Name	Default	Description
15	DEV_OFF_EN	0b	When set, enables the 82575 to enter power down. 0b = Disable. 1b = Enable.
14	Reserved	1b	Reserved.
13	Reserved	0b	Reserved.
12	LAN 1 iSCSI Enable	0b	When set, LAN 1 class code is set to 010000h (SCSI) When reset, LAN 1 class code is set to 020000h (LAN)
11	LAN 0 iSCSI Enable	0b	When set, LAN 0 class code is set to 010000h (SCSI) When reset, LAN 0 class code is set to 020000h (LAN)
10:8	Reserved	0h	Reserved.
7:0	Device Revision ID	00h	Device Revision ID.

1.6.1.21 LED 0, 2 Configuration Defaults (Word 1Fh)

This EEPROM word specifies the hardware defaults for the LEDCTL register fields controlling the LED0 (LINK_UP) and LED2 (LINK_100) output behaviors.

Table 18. LED 0-2 Configuration Defaults (Word 1Fh)

Bit(s)	Name	Default	Description
15	LED2 Blink	0b	This bit represents the initial value of the LED2_BLINK field. If it equals 0b, the LED is non-blinking.
14	LED2 Invert	0b	This bit represents the initial value of the LED2_IVRT field. If it equals 0b, it is an active low output.
13	Reserved	0b[1]	Reserved.
12	Reserved	0b	This bit is reserved and should be set to 0b.
11:8	LED2 Mode	0110b	This field represents the initial value of the LED2_MODE specifying the event, state, and pattern displayed on the LED2 (LINK_1000) output. A value of 0110b (or 6h) causes this to indicate 100 Mb/s operation. See Table 16 for all available LED modes.
7	LED0 Blink	0b	This field holds the initial value of LED0_BLINK field and is equal to 0b for non-blinking.
6	LED0 Invert	0b	This field holds the initial value of LED0_IVRT field and is equal to 0b for an active low output.

Table 18. LED 0-2 Configuration Defaults (Word 1Fh)

Bit(s)	Name	Default	Description
5	Global Blink Mode	0b[a]	Global Blink Mode 0b = Blink at 200 ms on and 200ms off. 1b = Blink at 83 ms on and 83 ms off.
4	Reserved	0b	This bit is reserved and should be set to 0b.
3:0	LED0 Mode	0010b	This field represents the initial value of the LED0_MODE specifying the event, state, and pattern displayed on the LED0 (ACTIVITY) output. A value of 0010b (2h) causes this to indicate link up state. See Table 16 for all available LED modes.

1. These bits are read from the EEPROM.

Note: A value of 0602h is used to configure default hardware LED behavior equivalent to 82544-based copper 82575s (LED0=LINK_UP, LED1=blinking ACTIVITY, LED2=LINK_100, and LED3=LINK_1000).

1.6.1.22 Functions Control (Word 21h)

Table 19. Functions Control (Word 21h)

Bit(s)	Name	Default	Description
15:13	Reserved	000b	Reserved.
12	LAN Function Select	0b	When both LAN ports are enabled and the LAN function select equals 0b, LAN 0 is routed to PCI function 0 and LAN 1 is routed to PCI function 1. If the LAN function select bit equals 1b, LAN 0 is routed to PCI function 1 and LAN 1 is routed to PCI function 0. This bit is mapped to FACTPS[30].
11:0	Reserved	0h	Reserved.

1.6.1.23 LAN Power Consumption (Word 22h)

This word is meaningful only if the EEPROM signature in word 0Ah is valid and Power Management is enabled.

Table 20. LAN Power Consumption (Word 22h)

Bit(s)	Name	Default	Description
15:8	LAN D0 Power	0h	The value in this field is reflected in the PCI Power Management Data Register of the LAN functions for D0 power consumption and dissipation (Data_Select = 0 or 4). Power is defined in 100 mW units and includes the external logic required for the LAN function.
7:5	Function 0 Common Power	0h	The value in this field is reflected in the PCI Power Management Data Register of function 0 when the Data_Select field is set to 8 (common function). The most significant bits in the Data Register that reflect the power values are padded with zeros.
4:0	LAN D3 Power	0h	The value in this field is reflected in the PCI Power Management Data Register of the LAN functions for D3 power consumption and dissipation (Data_Select = 3 or 7). Power is defined in 100 mW units and includes the external logic required for the LAN function. The most significant bits in the Data Register that reflect the power values are padded with zeros.

1.6.1.24 Management Hardware Configuration Control (Word 23h)

This word contains bits that direct special firmware behavior when configuring the PHY/ PCIe*/SerDes.

Bit	Name	Description
15	LAN1_FTCO_DIS	LAN1 force TCO reset disable (1 disable, 0 enable).
14	LAN0_FTCO_DIS	LAN0 force TCO reset disable (1 disable, 0 enable).
13:10	Reserved	Reserved.
9	Firmware Code Exist	If set, indicates to the firmware that there is firmware EEPROM code at address 50h.
8	LAN1_OEM_DIS	LAN1 OEM bits configuration disable. 0b = Enable. 1b = Disable.
7	LAN0_OEM_DIS	LAN0 OEM bits configuration disable. 0b = Enable. 1b = Disable.
6	CRC_DIS	PHY / SERDES / PCIe* CRC disable. 0b = Enable. 1b = Disable.
5	LAN1_ROM_DIS	LAN1 ROM Disable Disables PHY and SerDes ROM configuration for port 1. 0b = Enable. 1b = Disable.
4	LAN0_ROM_DIS	LAN0 ROM Disable Disables PHY and SerDes ROM configuration for port 0. 0b = Enable. 1b = Disable.
3	MNG_wake_check_dis	When set, indicates that the firmware is always to configure the PHY after power-up without checking that manageability or wake-up are enabled. 0b = Enable. 1b = Disable.
2	PCIe* ROM Disable	When set, indicates that the firmware is not to configure the PCIe* from the ROM tables. 0b = Enable. 1b = Disable.
1	PHY ROM Disable	When set, indicates that the firmware is not to configure the PHY of both ports from the ROM tables. 0b = Enable. 1b = Disable.
0	SERDES ROM Disable	When set, indicates that the firmware is not to configure the SerDes of both ports from the ROM tables. 0b = Enable. 1b = Disable.

1.6.1.25 End of RO Area (Word 2Ch)

Table 21. End of RO Area (Word 2Ch)

Bit(s)	Name	Default	Description
15	Reserved	0b	Reserved.
14:0	EORO_ area	0h	Defines the end of the area in the EEPROM that is RO. The resolution is one word and can be up to byte address FFFFh (7FFFh words). A value of zero indicates no RO area.

1.6.1.26 Start of RO Area (Word 2Dh)

Table 22. Start of RO Area (Word 2Dh)

Bit(s)	Name	Default	Description
15	Reserved	0b	Reserved.
14:0	SORO_ area	0h	Defines the start of the area in the EEPROM that is RO. The resolution is one word and can be up to byte address FFFFh (7FFFh words). Should be smaller or equal to Word 2Ch.

1.6.1.27 Watchdog Configuration (Word 2Eh)

Table 23. Watchdog Configuration (Word 2Eh)

Bit(s)	Name	Default	Description
15	Watchdog Enable	0b	Enable watchdog interrupt.
14:11	Watchdog Timeout	2h	Watchdog timeout period (in seconds).
10:0	Reserved	-	Reserved.

1.6.1.28 PXE Words (Words 30h:3Eh)

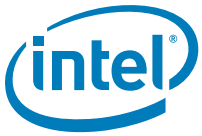
Words 30h through 3Eh have been reserved for configuration and version values to be used by PXE code. The only exception is word 3Dh. 3Dh is used for iSCSI boot configuration.

1.6.1.29 iSCSI Boot Configuration Start Address (Word 3Dh)

Table 24. iSCSI Boot Configuration Start Address (Word 3Dh)

Bit(s)	Name	Default	Description
15:0	Address	0b	This field defines the word address in the EEPROM space of the iSCSI Boot Configuration structure.

The iSCSI module structure is listed in the following table.



Configuration Item	Max Size (Byte)	Comments
iSCSI Boot Signature	2	This is the ASCII characters “iS”.
Total Size	2	The structure size is stored in this field and is set depending on the amount of free EEPROM space available. The total size of this structure, including variable length fields, must fit within this space.
Structure Version	1	The version number of this structure is stored in this field and should be set to 1b.
Checksum	1	This field holds the 8-bit checksum of this structure.
Flags	2	01h → Enable iSCSI Boot 02h → Valid Configuration This should be set to 1b if the configuration information in this structure is valid, and 0b, otherwise. 03h → Enable DHCP 04h:05h → Configuration Prompt 0 = 0 seconds 1 = 2 seconds 2 = 3 seconds 3 = 5 seconds 06h:0Ah → Number of Connection Retries
Initiator IP	4	If the DHCP flag is not set, this field should contain the configured IP address. If the DHCP flag is set, this field should be set to 0b or the last configured IP address should be saved.
Initiator Subnet Mask	4	If the DHCP flag is not set, this field should contain the configured subnet mask. If the DHCP flag is set, this field should be set to 0b or the last configured subnet mask should be saved.
Target IP	4	This is the IP address of the iSCSI target.
Target Port	2	This is the IP port of the iSCSI target. The default is 3260.
CHAP Password	32	
CHAP User Name	255 + 1	This is a variable length field.
Initiator Name	255 + 1	This is a variable length field.
User Name	255 + 1	This is a variable length field.

The maximum amount of boot configuration information stored is 834 bytes (417 words); however, the iSCSI boot implementation can limit this value in order to work with a smaller EEPROM.

Variable length fields are used to limit the total amount of EEPROM that is used for iSCSI boot information. Each field is preceded by a single byte that indicates how much space is available for that field. For example, if the Initiator Name field is being limited to 128 bytes, then it is preceded with a single byte with the value 128. The following field begins 128 bytes after the beginning of the Initiator Name field regardless of the actual size of the field. The variable length fields must be null terminated unless they reach the maximum size specified in the length byte.

1.6.1.30 VPD Pointer (Word 2Fh)

This word points to the Vital Product Data (VPD) structure. This structure is available for the NIC/LOM vendor to store it's own data.

1.6.1.31 Checksum Word Calculation (Word 3Fh)

The Checksum word (3Fh) is used to ensure that the base EEPROM image is a valid image. The value of this word should be calculated such that after adding all the words (00h:3Fh), including the Checksum word itself, the sum should be BABAh. The initial value in the 16-bit summing register should be 0000h and the carry bit should be ignored after each addition.

Note: Hardware does not calculate checksum word 3Fh during EEPROM write; it must be calculated by software independently and included in the EEPROM write data. Hardware does not compute a checksum over words 00h-0Fh during EEPROM reads in order to determine the validity of the EEPROM image; this field is provided strictly for software verification of EEPROM validity. All hardware configuration based on word 00h-0Fh content is based on the validity of the Signature field of EEPROM Initialization Control Word 1. Signature must be 01b.

1.7 Manageability Control Sections

1.7.1 Sideband Configuration Structure

1.7.1.1 Section Header - (0ffset 0h)

Bit	Name	Description
15:8	Block CRC8	
7:0	Block Length	

1.7.1.2 SMBus Max Fragment Size - (0ffset 01h)

Bit	Name	Description
15:0	SMBus Max Fragment Size (bytes)	

1.7.1.3 SMBus Notification Timeout and Flags - (0ffset 02h)

Bit	Name	Description
15:8	SMBus Notification Timeout (ms)	Timeout until discarding a packet not read by the BMC. 00h = No discard.
7:6	SMBus Connection Speed	00b = Slow SMBus connection. 01b = Fast SMBus connection (1 MHz). 10b = Reserved. 11b = Reserved.
5	SMBus Block Read Command	0b = Block read command is C0h. 1b = Block read command is D0h.

Bit	Name	Description
4	SMBus Addressing Mode	0b = Single-address mode. 1b = Dual-address mode.
3	Reserved	
2	Disable SMBus ARP Functionality	
1	SMBus ARP PEC	
0	Reserved	

1.7.1.4 SMBus Slave Addresses - (0ffset 03h)

Bit	Name	Description
15:9	SMBus 1 Slave Address	Dual-address mode only.
8	Reserved	
7:1	SMBus 0 Slave Address	
0	Reserved	

1.7.1.5 SMBus Fail-Over Register (Low Word) - (0ffset 04h)

Bit	Name	Description
15:12	Gratuitous ARP Counter	
11:10	Reserved	
9	Enable Teaming Fail-Over on DX	
8	Remove Promiscuous on DX	
7	Enable MAC Filtering	
6	Enable Repeated Gratuitous ARP	
5	Reserved	
4	Enable Preferred Primary	
3	Preferred Primary Port	
2	Transmit Port	
1:0	Reserved	

1.7.1.6 SMBus Fail-Over Register (High Word) - (0ffset 05h)

Bit	Name	Description
15:8	Gratuitous ARP Transmission Interval (seconds)	
7:0	Link Down Fail-Over Time	

1.7.1.7 NC-SI Configuration (0ffset 06h)

Bit	Name	Description
15:8	Reserved	
7:5	Package ID	
4:0	Reserved	Must be set to 00h.

1.7.2 Flex TCO Filter Configuration Structure

1.7.2.1 Section Header - (0ffset 0h)

Bit	Name	Description
15:8	Block CRC8	
7:0	Block Length	

1.7.2.2 Flex Filter Length and Control - (0ffset 01h)

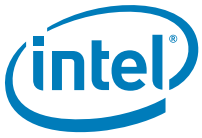
Bit	Name	Description
15:8	Flex Filter Length (bytes)	
7:5	Reserved	
4	Last Filter	
3:2	Filter Index (0-3)	
1	Apply Filter to LAN 1	
0	Apply Filter to LAN 0	

1.7.2.3 Flex Filter Enable Mask - (0ffset 02 - 09h)

Bit	Name	Description
15:0	Flex Filter Enable Mask	

1.7.2.4 Flex Filter Data - (0ffset 0Ah - Block Length)

Bit	Name	Description
15:0	Flex Filter Data	



1.7.3 NC-SI Microcode Download Structure

1.7.3.1 Data Patch Size (Offset 0h)

Bit	Name	Description
15:0	Data Size	

1.7.3.2 Rx and Tx Code Size (Offset 1h)

Bit	Name	Description
15:8	Rx Code Length in Dwords	
7:0	Tx Code Length in Dwords	

1.7.3.3 Download Data (Offset 2h - Data Size)

Bit	Name	Description
15:0	Download Data	

1.7.4 NC-SI Configuration Structure

1.7.4.1 Section Header - (0ffset 0h)

Bit	Name	Description
15:8	Block CRC8	
7:0	Block Length	

1.7.4.2 Rx Mode Control1 (RR_CTRL[15:0]) (Offset 01h)

Bit	Name	Description
15:8	Reserved	Should be 0b.
7:5	Reserved	Reserved.
4	False Carrier Enable	
3	NC-SI Speed	When set, the NC-SI MAC speed is 100 Mb/s. When reset, NC-SI MAC speed is 10 Mb/s.
2	Receive Without Leading Zeros	If set, packets without leading zeros (such as /J/K/ symbols) between TXEN assertion and TXD first preamble byte can be received.
1	Clear Rx Error	Should be set when the Rx path is stuck because of an overflow condition.
0	NC-SI Loopback Enable	When set, Enables NC-SI Tx to Rx loop. All data that is transmitted from NC-SI is returned to it. No data is actually transmitted from the NC-SI.

1.7.4.3 Rx Mode Control2 (RR_CTRL[31:16]) (Offset 02h)

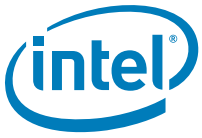
Bit	Name	Description
15:0	Reserved	Should be 0b.

1.7.4.4 Tx Mode Control1 (RT_CTRL[15:0]) (Offset 03h)

Bit	Name	Description
15:3	Reserved	Should be 0b.
2	Transmit With Leading Zeros	When set, send leading zeros (such as /J/K/ symbols) from CRS_DV assertion to start of preamble (PHY Mode). When deasserted, doesn't send leading zeros (MAC mode).
1	Clear Tx Error	Should be set when Tx path is stuck because of an underflow condition Cleared by hardware when release is done.
0	Enable Tx Pads	When set, the NC-SI Tx pads are driving, else they are isolated.

1.7.4.5 Tx Mode Control2 (RT_CTRL[31:16]) (Offset 04h)

Bit	Name	Description
15:0	Reserved	Should be 0b.



1.7.4.6 MAC Tx Control Reg1 (TxCntrlReg1 (15:0]) (Offset 05h)

Bit	Name	Description
15:7	Reserved	Should be 0b.
6	NC-SI_en	Enable the MAC internal NC-SI mode of operation (disables external NC-SI gasket).
5	Two_part_deferral	When set, perform the optional two part deferral.
4	Append_fcs	When set, compute and append FCS on TX frames.
3	Pad_enable	Pad the TX frames, which are less than the minimum frame size.
2	Rtry_col	Retry frames on collision until the max retry limit is reached. Note that this bit has no effect when working in full duplex.
1	Half Duplex	Half-duplex mode of operation, when set. Else Full duplex is assumed.
0	Reserved	Reserved

1.7.4.7 MAC Tx Control Reg2 (TxCntrlReg1 (31:16]) (Offset 06h)

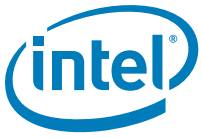
Bit	Name	Description
15:0	Reserved	Should be 0b.

1.7.5 Common Firmware Pointer

Word 54h is used to point to firmware structures common to ASF, pass through, and non-manageability modes.

1.7.5.1 Manageability Capability / Manageability Enable (Word 54h)

Bit	Name	Description
15	Enable Firmware Reset	0b = Firmware reset via HICR is disabled. 1b = Firmware reset via HICR is enabled.
14	Pass Through LAN Interface:	0b = SMBus. 1b = NC-SI.
13:11	Reserved	Reserved.
10:8	Manageability Mode	0h = None. 1h = ASF mode. 2h = PT mode. 3h = Reserved. 4h = Host interface enable only. 5h:7h = Reserved.
7	Port1 Manageability Capable	1b = Bits 3:0 are applicable to port 1.
6	Port0 Manageability Capable	1b = Bits 3:0 are applicable to port 0.
5:4	Reserved	Reserved.
3	Pass Through Capable	0b = Disable. 1b = Enable.
2	Reserved	Reserved.
1	ASF 2 Capable	0b = Disable. 1b = Enable.
0	ASF 1 Capable	0b = Disable. 1b = Enable.



1.7.6 Pass Through Pointers

1.7.6.1 PT LAN0 Configuration Pointer (Word 56h)

Bit	Name	Description
15:0	Pointer	Pointer to the PT LAN0 configuration pointer structure.

1.7.6.2 SMBus Configuration Pointer (Word 57h)

Bit	Name	Description
15:0	Pointer	Pointer to the SMBus configuration pointer structure.

1.7.6.3 Flex TCO Filter Configuration Pointer (Word 58h)

Bit	Name	Description
15:0	Pointer	Pointer to the flex TCO configuration pointer structure.

1.7.6.4 PT LAN1 Configuration Pointer (Word 59h)

Bit	Name	Description
15:0	Pointer	Pointer to the PT LAN1 configuration pointer structure.

1.7.6.5 NC-SI Microcode Download Pointer (Word 5Ah)

Bit	Name	Description
15:0	Pointer	Pointer to the NC-SI microcode download configuration pointer structure.

1.7.6.6 NC-SI Configuration Pointer (Word 5Bh)

Bit	Name	Description
15:0	Pointer	Pointer to the NC-SI configuration pointer structure.

1.7.7 PT LAN Configuration Structure

1.7.7.1 Section Header (Offset 0h)

Bit	Name	Description
15:8	Block CRC8	
7:0	Block Length	

1.7.7.2 LAN0 IPv4 Address 0 LSB, MIPAF0 (Offset 01h)

Bit	Name	Description
15:8	LAN0 IPv4 Address 0 (Byte 1)	
7:0	LAN0 IPv4 Address 0 (Byte 0)	

1.7.7.3 LAN0 IPv4 Address 0 LSB, MIPAF0 (Offset 02h)

Bit	Name	Description
15:8	LAN0 IPv4 Address 0 (Byte 3)	
7:0	LAN0 IPv4 Address 0 (Byte 2)	

1.7.7.4 LAN0 IPv4 Address 1; MIPAF1 (Offset 03h:04h)

Same structure as LAN0 IPv4 Address 0.

1.7.7.5 LAN0 IPv4 Address 2; MIPAF2 (Offset 05h:06h)

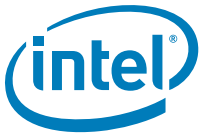
Same structure as LAN0 IPv4 Address 0.

1.7.7.6 LAN0 IPv4 Address 3; MIPAF3 (Offset 07h:08h)

Same structure as LAN0 IPv4 Address 0.

1.7.7.7 LAN0 MAC Address 0 LSB, MMAL0 (Offset 09h)

Bit	Name	Description
15:8	LAN0 MAC Address 0 (Byte 1)	
7:0	LAN0 MAC Address 0 (Byte 0)	



1.7.7.8 LAN0 MAC Address 0 LSB, MMAL0 (Offset 0Ah)

Bit	Name	Description
15:8	LAN0 MAC Address 0 (Byte 3)	
7:0	LAN0 MAC Address 0 (Byte 2)	

1.7.7.9 LAN0 MAC Address 0 MSB, MMAH0 (Offset 0Bh)

Bit	Name	Description
15:8	LAN0 MAC Address 0 (Byte 5)	
7:0	LAN0 MAC Address 0 (Byte 4)	

1.7.7.10 LAN0 MAC Address 1; MMAL/H1 (Offset 0Ch:0Eh)

Same structure as LAN0 MAC Address 0.

1.7.7.11 LAN0 MAC Address 2; MMAL/H2 (Offset 0Fh:11h)

Same structure as LAN0 MAC Address 0.

1.7.7.12 LAN0 MAC Address 3; MMAL/H3 (Offset 12h:14h)

Same structure as LAN0 MAC Address 0.

1.7.7.13 LAN0 UDP Flex Filter Ports 0:15; MFUTP Registers (Offset 15h:24h)

Bit	Name	Description
15:0	LAN UDP Flex Filter Value	

1.7.7.14 LAN0 VLAN Filter 0:7; MAVTV Registers (Offset 25h:2Ch)

Bit	Name	Description
15:12	Reserved	
11:0	LAN0 VLAN Filter Value	

1.7.7.15 LAN0 Manageability Filters Valid; MFVAL LSB (Offset 2Dh)

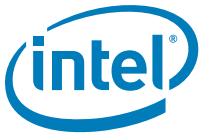
Bit	Name	Description
15:8	VLAN	Indicates if the VLAN filter registers (MAVTV) contain valid VLAN tags. Bit 8 corresponds to filter 0, etc.
7:4	Reserved	Reserved.
3:0	MAC	Indicates if the MAC unicast filter registers (MMAH and MMAL) contain valid MAC addresses. Bit 0 corresponds to filter 0, etc.

1.7.7.16 LAN0 Manageability Filters Valid; MFVAL MSB (Offset 2Eh)

Bit	Name	Description
15:12	Reserved	Reserved.
11:8	IPv6	Indicates if the IPv6 address filter registers (MIPAF) contain valid IPv6 addresses. Bit 8 corresponds to address 0, etc. Bit 11 (filter 3) applies only when IPv4 address filters are not enabled (MANC.EN_IPv4_FILTER=0b).
7:4	Reserved	Reserved.
3:0	IPv4	Indicates if the IPv4 address filters (MIPAF) contains a valid IPv4 address. These bits apply only when IPv4 address filters are enabled (MANC.EN_IPv4_FILTER=1b)

1.7.7.17 LAN0 MAC Value MSB (Offset 2Fh)

Bit	Name	Description
15:0	Reserved	Reserved.



1.7.7.18 LAN0 MANC Value LSB (Offset 30h)

Bit	Name	Description
15:9	Reserved	Reserved.
8	Enable IPv4 Address Filters	When set, the last 128 bits of the MIPAF register are used to store four IPv4 addresses for IPv4 filtering. When cleared, these bits store a single IPv6 filter.
7	Enable Xsum Filtering to MNG	When this bit is set, only packets that pass the L3 and L4 checksum are send to the MNG block.
6	Reserved	Reserved.
5	Enable MNG Packets to Host Memory	This bit enables the functionality of the MANC2H register. When set, the packets that are specified in the MANC2H registers are also sent to host memory if they pass the manageability filters.
4:0	Reserved	Reserved.

1.7.7.19 LAN0 Receive Enable 1(Offset 31h)

Bit	Name	Description
15:8	Receive Enable Byte 12	BMC SMBus slave address.
7	Enable BMC Dedicated MAC	
6	Reserved	Always set to 1b.
5:4	Notification Method	00b = SMBus alert. 01b = Asynchronous notify. 10b = Direct receive. 11b = Reserved.
3	Enable ARP Response	
2	Enable Status Reporting	
1	Enable Receive All	
0	Enable Receive TCO	

1.7.7.20 LAN0 Receive Enable 2 (Offset 32h)

Bit	Name	Description
15:8	Receive Enable Byte 14	Alert value.
7:0	Receive Enable Byte 13	Interface value.

1.7.7.21 LAN0 MANC2H Value LSB (Offset 33h)

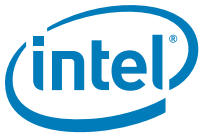
Bit	Name	Description
15:8	Reserved	Reserved.
7:0	Host Enable	When set, indicates that packets routed by the manageability filters to manageability are also sent to the host. Bit 0 corresponds to decision rule 0, etc.

1.7.7.22 LAN0 MANC2H Value MSB (Offset 34h)

Bit	Name	Description
15:0	Reserved	Reserved.

1.7.7.23 Manageability Decision Filters; MDEF0,1 (Offset 35h)

Bit	Name	Description
15:12	Flex Port	Controls the inclusion of flex port filtering in the manageability filter decision (OR section). Bit 12 corresponds to flex port 0, etc. (see also bits 11:0 of the next word).
11	Port 26Fh	Controls the inclusion of port 26Fh filtering in the manageability filter decision (OR section).
10	Port 298h	Controls the inclusion of port 298h filtering in the manageability filter decision (OR section).
9	Neighbor Discovery	Controls the inclusion of neighbor discovery filtering in the manageability filter decision (OR section).
8	ARP Response	Controls the inclusion of ARP response filtering in the manageability filter decision (OR section).
7	ARP Request	Controls the inclusion of ARP request filtering in the manageability filter decision (AND section).
6	Multicast	Controls the inclusion of multicast addresses filtering in the manageability filter decision (OR section).
5	Broadcast	Controls the inclusion of broadcast address filtering in the manageability filter decision (OR section).
4	Unicast	Controls the inclusion of unicast address filtering in the manageability filter decision (OR section).
3	IP Address	Controls the inclusion of IP address filtering in the manageability filter decision (AND section).
2	VLAN	Controls the inclusion of VLAN addresses filtering in the manageability filter decision (AND section).
1	Broadcast	Controls the inclusion of broadcast address filtering in the manageability filter decision (AND section).
0	Unicast	Controls the inclusion of unicast address filtering in the manageability filter decision (AND section).



1.7.7.24 Manageability Decision Filters; MDEF0, 2 (Offset 36h)

Bit	Name	Description
15:12	Flex TCO	Controls the inclusion of flex TCO filtering in the manageability filter decision (OR section). Bit 12 corresponds to flex TCO filter 0, etc.
11:0	Flex Port	Controls the inclusion of flex port filtering in the manageability filter decision (OR section). Bit 11 corresponds to flex port 0, etc. (see bits 15:12 of previous word).

1.7.7.25 Manageability Decision Filters; MDEF1:6, 1:2 (Offset 37h:42h)

Same as words 35h and 36h for MDEF1:MDEF6.

1.7.7.26 ARP Response IPv4 Address 0 LSB (Offset 43h)

Bit	Name	Description
15:8	ARP Response IPv4 Address Byte 1	
7:0	ARP Response IPv4 Address Byte 0	

1.7.7.27 ARP Response IPv4 Address 0 MSB (Offset 44h)

Bit	Name	Description
15:8	ARP Response IPv4 Address Byte 3	
7:0	ARP Response IPv4 Address Byte 2	

1.7.7.28 LAN0 IPv6 Address 0 LSB; MIPAF (Offset 45h)

Bit	Name	Description
15:8	LAN0 IPv6 Address 0 Byte 1	
7:0	LAN0 IPv6 Address 0 Byte 0	

1.7.7.29 LAN0 IPv6 Address 0 MSB; MIPAF (Offset 46h)

Bit	Name	Description
15:8	LAN0 IPv6 Address 0 Byte 3	
7:0	LAN0 IPv6 Address 0 Byte 2	

1.7.7.30 LAN0 IPv6 Address 0 LSB; MIPAF (Offset 47h)

Bit	Name	Description
15:8	LAN0 IPv6 Address 0 Byte 5	
7:0	LAN0 IPv6 Address 0 Byte 4	

1.7.7.31 LAN0 IPv6 Address 0 MSB; MIPAF (Offset 48h)

Bit	Name	Description
15:8	LAN0 IPv6 Address 0 Byte 7	
7:0	LAN0 IPv6 Address 0 Byte 6	

1.7.7.32 LAN0 IPv6 Address 0 LSB; MIPAF (Offset 49h)

Bit	Name	Description
15:8	LAN0 IPv6 Address 0 Byte 9	
7:0	LAN0 IPv6 Address 0 Byte 8	

1.7.7.33 LAN0 IPv6 Address 0 MSB; MIPAF (Offset 4Ah)

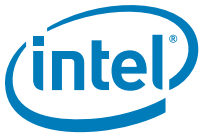
Bit	Name	Description
15:8	LAN0 IPv6 Address 0 Byte 11	
7:0	LAN0 IPv6 Address 0 Byte 10	

1.7.7.34 LAN0 IPv6 Address 0 LSB; MIPAF (Offset 4B)

Bit	Name	Description
15:8	LAN0 IPv6 Address 0 Byte 13	
7:0	LAN0 IPv6 Address 0 Byte 12	

1.7.7.35 LAN0 IPv6 Address 0 MSB; MIPAF (Offset 4Ch)

Bit	Name	Description
15:8	LAN0 IPv6 Address 0 Byte 15	
7:0	LAN0 IPv6 Address 0 Byte 14	



1.7.7.36 LAN0 IPv6 Address 1; MIPAF (Offset 4Dh)

Same structure as LAN0 IPv6 Address 0.

1.7.7.37 LAN0 IPv6 Address 2; MIPAF (Offset 55h:5Ch)

Same structure as LAN0 IPv6 Address 0.

1.7.8 ASF Controller Words

When the 82575 is in ASF mode, the 82575 ASF function reads words 40h through F7h from the EEPROM. These words are read after power up (Internal_Power_On_Reset assertion), ASF Soft Reset (ASF FRC_RST), or software commanded ASF EEPROM read (ASF FRC_EELD). Refer to the *Alert Standards Format (ASF) Design Guide* for more details.

Note: These words should be programmed by ASF configuration software. The value of the words from the factory should be all FFh.

1.7.8.1 ASF Words – Content

The interpretation of these words depends on the ASF mode functionality.

1.7.8.2 ASF Words – EEPROM Checksum (CRC)

While the ASF EEPROM words are read, the 82575 also computes the ASF CRC word. Words 40h to F7h are included in the CRC calculation and compared against the CRC value present in word F7h. If the CRC values do not match, the 82575 does not overwrite the ASF configuration registers with the EEPROM values. Therefore, if the ASF CRC is invalid, hardware default values will initially be present in ASF registers and any subsequent re-read of EEPROM leaves the ASF registers unchanged (from values current at the time of the EEPROM read).

The details of this CRC can be found at:

http://cell-relay.indiana.edu/cell-relay/publications/software/CRC/32bitCRC.tutorial.html

1.8 Software Owned EEPROM Words

This section describes the software owned EEPROM words (words 03h:09h).

1.8.1 Compatibility Fields (Word 03h, 04h, 06h, and 07h)

Four words in the EEPROM image are reserved for compatibility information. New bits within these fields will be defined as the need arises for determining software compatibility between various hardware revisions.

1.8.2 EEPROM Image Version Word (Word 05h)

Table 25. EEPROM Image Version Word (Word 05h)

Bit	Name	Default	Description
15:8	EEPROM Image Major Version		EEPROM Image major version number.
7:0	EEPROM Image Minor Version		EEPROM Image minor version number.

1.8.3 PBA Number or OEM Version (Words 08h, 09h)

Words 08h and 09h are dual-purpose words: PBA number (used for Intel manufactured adapter cards) and OEM version.

The nine-digit Printed Board Assembly (PBA) number (Table 26), used for Intel manufactured adapter cards, is stored in a four-byte field. The dash itself is not stored, neither is the first digit of the 3-digit suffix, as it will always be 0b for the affected products. Note that through the course of hardware ECOs, the suffix field (byte 4) is incremented. The purpose of this information is to allow Customer Support (or any user) to identify the exact revision level of a product. Network driver software should not rely on this field to identify the product or its capabilities.

Note: The PBA number is not related to the Packet Buffer Allocation (PBA) register or to the MSI-X PBA (Pending Bit Array).

Table 26. PBA Number (Words 08h, 09h)

Product	PWA Number	Byte 1	Byte 2	Byte 3	Byte 4
Example	123456-003	12	34	56	03

OEMs can also use these words for the revisioning level of their products. The use of these words is completely up to the OEM. However, if the EEPROM image is created using Intel's internal tools, this is where the contents of the OEM_version keyword is placed. The internal tools writes these values after all other rules are applied. This enables the internal tools to overwrite all values. Writes are denoted as follows:

;0x8 [15:12] - 0x9 - ;OEM Version Major <Set By Definition File: OEM_Version>

;0x8 [11:4] - 0x1 - ;OEM Version Minor <Set By Definition File: OEM_Version>

;0x8 [3:0] - 0x2 - ;OEM ID 2 = OEM <Set By Definition File: OEM_ID>

OEM_Version: Major #. Minor # - The major # is written to the top four bits of word 8h. The minor # is written to the middle eight bits of word 8h.

OEM_ID: OEM ID - The internal tools converts this string to a given value mapping and writes it to the last four bits of word 8h.

Note: Network driver software should not rely on this field to identify the product or its capabilities.