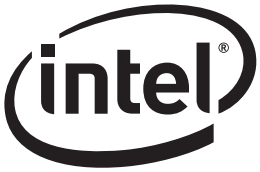

Intel® 82567 Gigabit Ethernet Controller Specification Update and Sighting Information

Networking Silicon

Order Number: 321791-001

Revision 2.0
April 2009

Revision History

Revision	Revision Date	Description
0.25	Aug 2007	Initial release.
0.5	Nov 2007	Added Specification Change #2; added Errata #3.
1.5	Nov 2007	Re-worded Errata #1
1.6	Dec 2007	Corrected tolerances for 1.05 V power rail in specification change #1.
1.7	Mar 2008	Added FET switch clarification; changed device ID
1.8	Apr 2008	Corrected leaded device part number; removed confidential designation for release to public web site; consolidated Tables 3 & 5 into a new Table 3, removed pre-production errata.
1.9	July 2008	Added Pin 1 Indicator illustration.
2.0	April 2009	Deleted Specification Changes—all are documented in the datasheet. Updated Markings diagram. Deleted Specification Clarification—information applied only to pre-production units.

Note: The revision level numbering scheme was changed beginning with Revision 1.5 to align with the platform versioning scheme; there are no versions between 0.5 and 1.5.

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Contents

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Preface

This document applies to the Intel® 82567 Gigabit Ethernet Controller. In this document it is commonly referred to as "the device."

This document is an update to published specifications. Specification documents for this product include:

- *82567 Gigabit Ethernet Controller Datasheet*, Intel Corporation.
- *82566/82567/82562V Gigabit Ethernet PHY and ICH8/9/10 – Software Developer Manual (SDM),* Intel Corporation

This document is intended for hardware system manufacturers and software developers of applications, operating systems or tools. It may contain Specification Changes, Errata, and Specification Clarifications.

All product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

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Nomenclature

This document uses various definitions, codes, and abbreviations to describe the Specification Changes, Errata, Sightings and/or Specification Clarifications that apply to the listed silicon/steppings:

Table 1 Definitions

Name	Description
Specification Changes	Modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
Errata	Design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.
Sightings	Observed issues that are believed to be errata, but have not been completely confirmed or root caused. The intention of documenting sightings is to proactively inform users of behaviors or issues that have been observed. Sightings may evolve to errata or may be removed as non-issues after investigation completes.
Specification Clarifications	Greater detail or further highlights concerning a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
Documentation Changes	Typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Table 2 Codes and Abbreviations

Name	Description
X	Specification Change, Erratum, or Specification Clarification that applies to this stepping.
Doc	Document change or update that will be implemented.
Fix	This erratum is intended to be fixed in a future stepping of the component.
Fixed	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded	This Item is either new or modified from the previous version of the document.
DS	Data Sheet
DG	Design Guide

Name	Description
SDM	Software Developer's Manual
EDS	External Data Specification
AP	Application Note

Product Code & Device Identification

Product Code: :WG82567 (unleaded), HG82567 (leaded)

The following tables and drawings describe the various identifying markings on each device package:

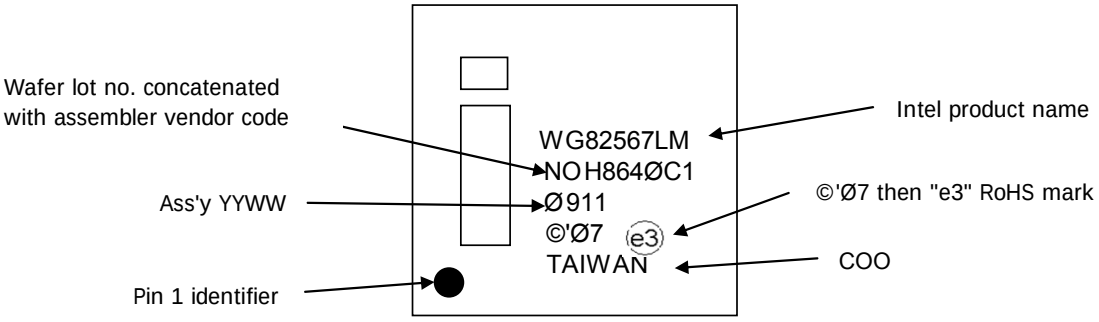
Table 3 Markings

Package Marking	Step	Intel Spec Number Field	Intel Material Master#	Description	Type
82567 Corporate					
WG82567LM	B0	S LAVU	896255	PAS compliant, Tape and Reel	Production
WG82567LM	B0	S LAVV	896256	PAS compliant, Tray	Production
82567 B-0, Fundamental					
WG82567LF	B0	S LAW3	896258	PAS compliant, Tape and Reel	Production
WG82567LF	B0	S LAW4	896259	PAS compliant, Tray	Production
82567 B-0, Value					
WG82567V	B0	S LAW6	896261	PAS compliant, Tape and Reel	Production
WG82567V	B0	S LAW7	896262	PAS compliant, Tray	Production
82567 B-0, Pb Corporate					
HG82567LM	B0	S LAVX	896264	PAS compliant, Tape and Reel	Production
HG82567LM	B0	S LAVY	896265	PAS compliant, Tray	Production

Table 4 Vendor, Device, and Revision IDs

Device	ICH	Vendor ID	Device ID	Revision ID*
82567LM	9	8086	10E5	0x0
82567LM	9M	8086	10F5	0x0
82567LM	10	8086	10CC	0x0
82567LM	10D	8086	10DE	0x0
82567LF	9M	8086	10BF	0x0
82567LF	10	8086	10CD	0x0
82567LF	10D	8086	10DF	0x0
82567V	8M	8086	1501	0x0
82567V	9M	8086	10CB	0x0
82567V	10	8086	10CE	0x0

Markings


Wafer lot no. concatenated with assembler vendor code
Ass'y YYWW
Pin 1 identifier
WG82567LM
NOH864ØC1
Ø911
©'Ø7
e3
TAIWAN
Intel product name
©'Ø7 then "e3" RoHS mark
COO

Summary of Changes From last Version

No.	A0	A1	B0	Plans	Specification Changes	Page
					None	
No.	A0	A1	B0	Plans	Errata	Page
1	X	X	X	NoFix	10BASE-T IEEE-Specified Harmonic Content Level Issue.	8
2	X	X	X	NoFix	1000BASE-TX IEEE-Marginal Rise/Fall Time Performance.	8
No.	A0	A1	B0	Plans	Sightings	
					None.	
No.	A0	A1	B0	Plans	Specification Clarifications	
					None.	

Specification Changes

None.

Errata

1. 10BASE-T IEEE-Specified Harmonic Content Level Issue.

Problem: On some board designs, the 82567 may not meet the IEEE specification (1411.10.03) that states that the harmonic content is to be at least 27 dB below the 10 MHz fundamental frequency.

Implication: IEEE conformance is marginal. There is no impact on system level performance, however, care should be taken to verify the impact of radiated EMI (Electromagnetic Interference) on system-level EMI tests.

Status: No Fix: There are no plans to fix this erratum.

2. 1000BASE-TX Marginal Rise/Fall Time Performance.

Problem: The 82567 rise/fall time has been marginal compared to the specification (5 ns).

Implication: IEEE conformance is marginal. Depending on system topology (LAN switch/no LAN switch), MDI trace lengths, and configuration (docked/undocked), the 100BASE-TX rise/fall time may not meet the specification.

There is no impact on system level performance.

Workaround: There is no silicon/firmware/software workaround.

Status: No Fix: There are no plans to fix this erratum.

Sightings

None.

Specification Clarifications

None.

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