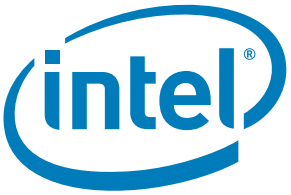


Intel® 82566 Gigabit Platform LAN Connect

Specification Update

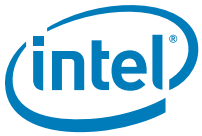
January 2012

Revision 2.4

Contents

Revision History

Date	Revision	Description
2.4	Jan 2012	Added Specification Clarification #2.
2.3	March 2010	Added Specification Clarification #1.
2.2	July 2009	Added Erratum #10.
2.1	August 2007	Updated the “Affected Documents/Related Documents” section. Added device MM #s to the “Identification Information” section.
2.0	May 2007	Added Erratum #9.
1.9	Mar 2007	Initial public release.
1.8	Feb 2007	Updated Erratum #6.
1.7	Jan 2007	Added Errata #7 & #8.
1.6	Oct 2006	Added Errata #6.
1.5	Apr 2006	Updated Table 3 (Added Identifying Marks and Order Codes for B-1 Stepping).
1.1	Jan 2006	Added Errata #5. Updated Errata #1 through #4.
1.0	Oct 2005	Initial Release.



Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title
Intel® 82566 Gigabit Platform LAN Connect Datasheet, Intel Corporation.
Intel® Q96x, G965, P965 Express Chipset Platform Design Guide, Intel Corporation.
Intel® Centrino® Pro Processor Technology and Intel® Centrino® Duo Processor Technology Design Guide. For Intel® Core™2 Duo Processor, Mobile Intel® 965 Express Chipset Family and Intel® 82801HBM ICH8M & Intel® 82801HEM ICH8M-E I/O Controller Hub Based Systems, Intel Corporation.
Intel® I/O Controller Hub 8 (ICH8) Family Datasheet, Intel Corporation.
Intel® I/O Controller Hub 9 (ICH8) Family Datasheet, Intel Corporation.
Intel® ICH8/ICH9 (MAC) GbE LAN Controller and 82566/82562V (PHY) Software Developer's Manual, Intel Corporation.
Intel® I/O Control Hub 8 (ICH8) LAN NVM Map and Programming Guide, Intel Corporation.
Intel® I/O Control Hub 9 (ICH8) LAN NVM Map and Programming Guide, Intel Corporation.

Nomenclature

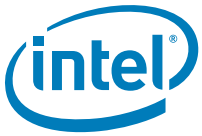
Errata are design defects or errors. These may cause the 82566's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).



Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the 82566 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings		Page	Status	ERRATA
	A0	B1			
1	X		9	Fixed	MDI Return Loss Marginal for 115 ohm Load.
2	X		9	Fixed	High In-Rush Current During Power Up.
3	X	X	10	No Fix	10BASE-T Link Pulse Hit the Template Mask.
4	X	X	11	No Fix	10BASE-T TP_IDL Template Failure.
5	X	X	12	No Fix	Excess Noise on 1.8V Supply.
6	X	X	13	No Fix	Intel® 82566 100 Mb/s Output Amplitude.
7	X	X	14	Fixed	Failure to WOL/S5 When Performing Stress Testing
8	X	X	15	Fixed	Stressful Traffic May Result in a Packet Transmitted with 16 Bytes of Incorrect Data
9	X	X	15	Fixed	ICH9 Link-Loss Issue Due To 82566 PHY Reset
10	X	X	15	NoFix	Missing Interrupt Following ICR Read

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	A0	B1			
					None for this revision of this specification update.

Specification Clarifications

No.	Steppings		Page	Status	SPECIFICATION CLARIFICATIONS
	A0	B1			
1	X	X	16	NoFix	PHY Does Not Maintain Gigabit Link in Low Power States
2	X	X	16	NoFix	While In TCP Segmentation Offload, Each Buffer is Limited to 64 KB

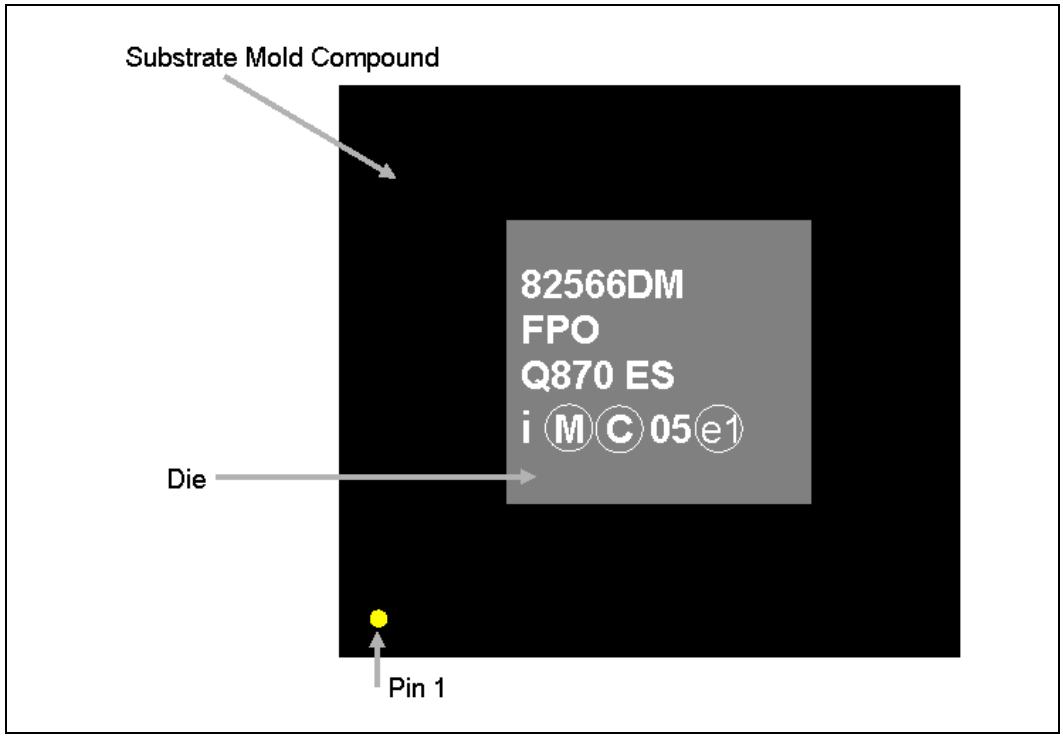
Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

Identification Information

Markings

Figure 1. Marking Information



Device	Stepping	MM Number	Specification	Notes
RU82566DC	B-1	879298	L97Z	Production (Tray)
RU82566DM	B-1	878628	L95J	Production (Tray)
RU82566MC	B-1	885898	L99J	Production (Tray)
RU82566MM	B-1	885396	L983	Production (Tray)

Errata

Note: ICH8 (Intel LAN MAC) related errata are released through the *Intel® ICH8 Family EDS Specification Update*, which is available on IBL.

1. MDI Return Loss Marginal for 115 ohm Load

Problem: Return loss for 115 ohm load is marginal and occasionally fails to conform to the Gigabit IEEE specification (Section 40.8.3.1) near the frequency of 40 MHz. Return loss is fine throughout the rest of the frequency spectrum and conforms to the 10BASE-T and 100BASE-TX specification limits

Implication: IEEE conformance is marginal. There is no impact in system level performance.

Workaround: There is currently no workaround for A-0 stepping.

Status: This issue is resolved in the B-0 silicon stepping. The 82566 device now has an average of 2 dB margin to the specification when measured at the 115 ohm limit.

2. High In-Rush Current During Power Up

Problem: In-rush current of up to 2.3 A might occur during voltage supply power up.

Implication: This issue might affect the platform by causing the over-current protection circuit to engage, cutting off power to the platform. If the protection circuit does not turn off the power supply, the current surge might cause a voltage droop on the local LAN supply, preventing the LAN from powering up correctly. This prevents the LAN from achieving link.

Workaround: This problem can be mitigated by adding more than 100 µF of capacitance on the 3.3V supply to the LAN.

Status: This issue was resolved in the A-1 silicon stepping.

3. 10BASE-T Link Pulse Touches the Template Mask

Problem: The 10BASE-T link pulse waveform touches the template mask due to a small voltage glitch, as measured per the TP_IDLE silence duration and silence voltage test (IEEE 10 Mb test case ID 1411.01.06).

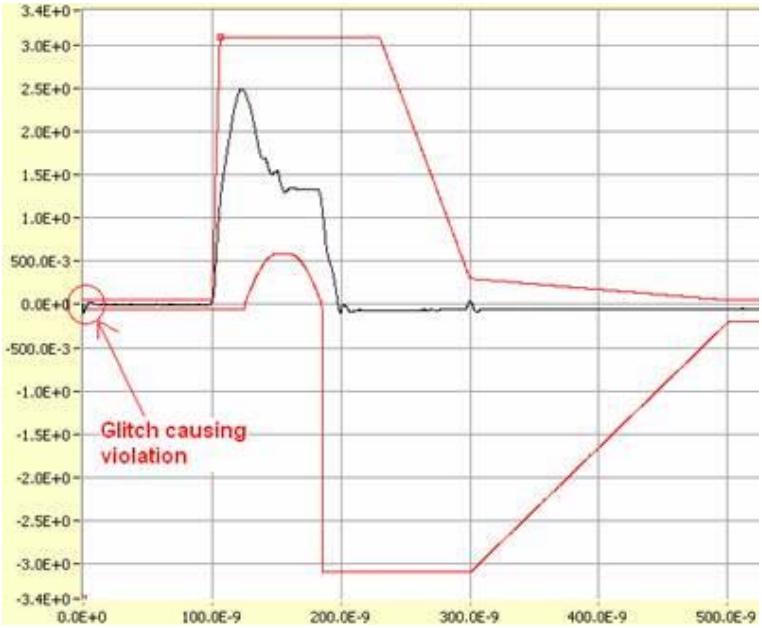


Figure 2. TP_IDLE Silence Duration and Silence Voltage Template Mask

Implication: IEEE conformance is marginal. There is no impact to system level performance. This issue only occurs during 10 Mb Idle Mode. The voltage glitch occurs because the 82566, by default, powers down the transmitter between link pulses (during the 0V output period) to save power. The glitch is visible slightly before the transmission of the link pulse.

Workaround: The workaround prevents transmitter power-down during silence periods. This workaround increases the power consumption of the 82566 ~180mW during 10 Mb idle mode. Customers that desire to implement this workaround should contact their Intel representative for more information.

Status: Intel does not plan to resolve this issue in a future stepping.

4. 10BASE-T TP_IDL Template Marginality

Problem: The 10BASE-T TP_IDL waveform touches the template mask when tested with twisted-pair model combined with test load 2, per IEEE test case 1411.10.06. There is no issue with the other test loads.

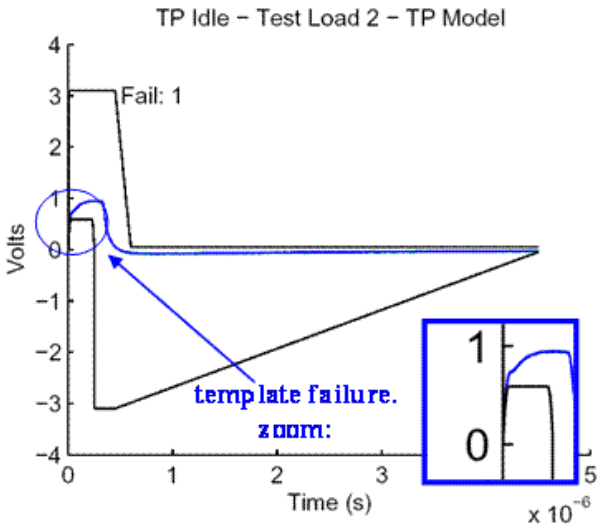


Figure 3. Typical Scope Measurement of TP Idle with Test Load 2

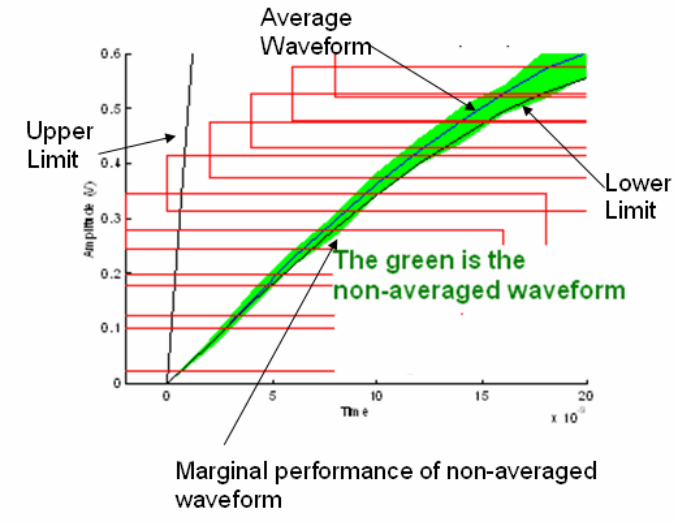


Figure 4. Typical Scope Measurement of TP Idle with Test Load 2 (Zoomed in with Non-Averaged Waveform

Implication: Per the IEEE specification, the TP_IDL pulse must fit into a template when measured with and without the twisted-pair model for two types of loads (load1 and load2). The combination of the twisted-pair model together with load2 is the challenging one because the waveform is the most attenuated. Some test conditions and methodologies do not apply averaging during the waveform measurement (see non-averaged waveform in Figure 4) and might show marginal IEEE conformance. There is no impact in system level performance.

Workaround: There is currently no workaround.

Status: Intel does not plan to resolve this issue in a future stepping.

5. Excess Noise on 1.8V Supply

Problem: The 82566 internal LVR controller, when used, creates excessive noise on the LAN 1.8V power supply.

Implication: In some platforms, excess noise has been seen on the LAN 1.8V supply when using the 82566 internal voltage regulator controllers. The issue was observed in both the IVRI and the IVRD modes. The LAN 1.8V noise might feedback into the 3.3V supply as well. This noise could affect the 82566's ability to meet IEEE specifications.

Workaround: Add a 10 nF cap as shown in Figure 5 and Figure 6. Intel also recommends adding a stuffing option for a 10 nF capacitor (marked do not populate) to the 1.0V linear regulator when in IVRD mode.

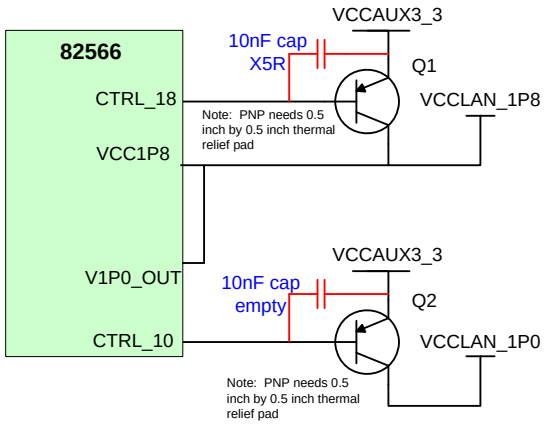


Figure 5. IVRD Implementation

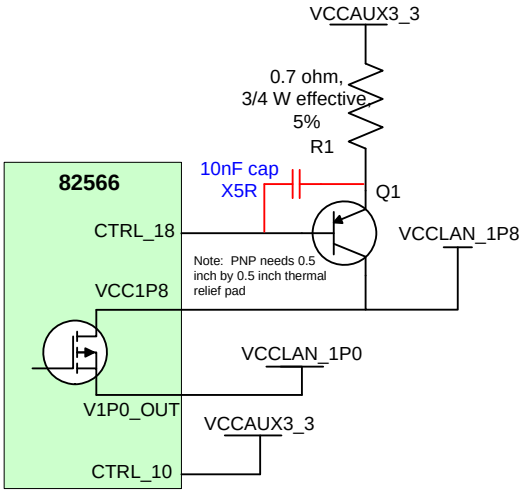


Figure 6. IVRI Implementation

6. Intel® 82566 100 Mb/s Output Amplitude

Problem: The 82566 LAN transmitter output might exceed the IEEE 100 Mb/s output amplitude specification by as much as 20% when operating at 100 Mb/s in one of the following configurations:

1. Without the Intel® LAN Platform Driver version 9.4.17.0 or later. Note that all production release drivers for the 82566 meet this criteria.

Or

2. Platforms with Intel® Active Management Technology (Intel® AMT) or ASF enabled without the Intel® Manageability Engine firmware version 2.1 or later and without the Intel® LAN Platform Driver version 9.4.17.0 or later.

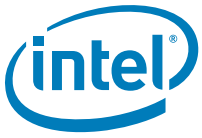
Or

3. Platforms that do not support Intel® AMT (platforms with 82566 DC/MC SKUs) or ASF and in cases when the NDIS driver (9.4.17.0 or later) is not loaded like a DOS*/EFI shell environment, boot to operating system load time.

Implication: If the link partner is sensitive to excessive 100 Mb/s output amplitude, the LAN link might be lost or not established, which would prevent Wake on LAN. If the 82566 is transmitting data to the link partner the Bit Error Rate (BER) might be higher than normal. Note that these implications are purely theoretical. No BER or link issues have been seen as a result of this specification violation.

Workaround: All platforms should use the Intel LAN Platform Driver version 9.4.17.0 or later. Platforms that are using manageability should upgrade to the Intel Manageability Engine firmware version 2.1 or later.

Status: Intel does not plan to resolve this issue for the 82566 with I/O Controller Hub 8. Intel plans to fix this issue in the I/O Controller Hub 9.



7. Failure to WOL/S5 When Performing Stress Testing

Problem: When performing WOL/S5 stress testing, the system would fail to wake when using a Procurve Switch with some test systems after 200+ iterations.

Implication: On the transition from force gig mode to 10/100, a timing issue might happen in Nahum that would cause the receive clock to stop working.

Workaround: Changed the PHY configuration timing to not execute force gig to the Nahum.

Status: Fixed-will be corrected in all future EEPROM images.

8. Stressful Traffic May Result in a Packet Transmitted with 16 Bytes of Incorrect Data

Problem: With Circuit Breaker enabled, stressful traffic may result in a packet being transmitted with 16 bytes of incorrect data. Empirical testing has shown that this will occur on average once every 4-16 hours using maximum stress under Chariot. The incorrect data will normally result in a TCP checksum error observed at the peer.

Implication: This packet will be dropped and retransmitted by the TCP protocol. In a very rare instance, the TCP checksum might be correct by chance and the packet could be received by the TCP stack on the peer, resulting in "incorrect silent data".

Workaround: A software driver workaround has been identified and validated. If the software driver ensures that the last descriptor points to at least 33 bytes of data, this issue will not occur.

Status: Fixed-will be corrected in the next driver delivery.

9. ICH9 Link-Loss Issue Due To 82566 PHY Reset

Problem: The Intel® 82566 LAN device might randomly go into reset mode and temporarily cease communicating with the network under long-term testing.

Implication: The system can temporarily lose connection with the network. The LAN indicator LEDs are not lit and the link partner reports that the link has been lost. It remains in this condition until the system is reset by the software device driver, which can take up to several minutes. Internal testing has shown that this only occurs on a small subset of systems.

Workaround: The latest NVM EEPROM image resolves this issue by modifying the ICH9 interface timing.

Status: This issue is resolved in version 1.3.1 of the base EEPROM image and is also incorporated into the latest sample validation kit.

10. Missing Interrupt Following ICR Read

Problem: If the Interrupt Cause Register (ICR) is read when at least one bit is set in the interrupt mask register and INT_ASSERTED is set to 0b, a new interrupt event occurring on the same clock cycle as the ICR read is ignored.

Implication: Missed interrupts leading to delays in responding to interrupt events. Specifically, this can cause a delay in processing a received packet.

Typically, the ICR is only read in response to an interrupt so this problem does not occur. However, when using legacy interrupts and sharing interrupts between devices, software might poll all the devices to find the source of the interrupt, including those devices that did not assert an interrupt. There might also be other situations in non-Intel drivers where ICR is polled even when no interrupt has been asserted.

Workaround: If reading ICR when there is no active interrupt cannot be avoided, clear the mask register (by writing 0xFFFFFFFF to IMC) before reading ICR. Note that in this case the ICR is cleared when read even if INT_ASSERTED is set 0b.

Status: NoFix. There are no plans to fix this erratum.

Specification Changes

None for this revision of this specification update.

Specification Clarifications

1. PHY Does Not Maintain Gigabit Link in Low Power States

While operating in power states less than D0 or operating system states other than S0, the PHY is designed to negotiate to the lowest speed possible, and maintains a link in those states only at 10 Mb/s or 100 Mb/s. If the PHY is connected to a link partner that is only capable of gigabit connections, the link is lost in these lower power states. This limitation is due to power requirements imposed by energy saving initiatives (such as Energy Star), as the additional power required to maintain gigabit connections might cause the system to exceed the level needed to meet the specifications.

When attached to a port that is limited to gigabit speed connections, the PHY loses link in low power states, and therefore network functions normally available in those states, such as Wake on LAN (WoL) or remote management, is not possible in that environment.

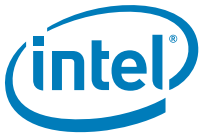
2. While In TCP Segmentation Offload, Each Buffer is Limited to 64 KB

The 82566 supports 256 KB TCP packets; however, each buffer is limited to 64 KB since the data length field in the transmit descriptor is only 16 bits. This restriction increases driver implementation complexity if the operating system passes down a scatter/gather element greater than 64 KB in length. This can be avoided by limiting the offload size to 64 KB.

Investigation has concluded that the increase in data transfer size does not provide any noticeable improvements in LAN performance. As a result, Intel network software drivers limit the data transfer size in all drivers to 64 KB.

Please note that Linux operating systems only support 64 KB data transfers.

For further details about how Intel network software drivers address this issue, refer to Technical Advisory TA-191.



Documentation Changes

None for this revision of this specification update.

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