82563EB/82564EB Gigabit Platform LAN Connect Specification Update

Networking Silicon

Revision 2.8
March 2010

Revision History

Revision	Revision Date	Description
0.25	Dec 2004	Initial release (Intel Secret).
0.30	Feb 2005	Added Erratum #2 (In-band messages at end of packet may cause MAC to detect CRC errors).
1.75	July 2005	Added order codes for C0 stepping. Added Specification Clarification #1.
2.0	Dec 2005	Initial release (Intel Confidential).
2.5	May 2006	Initial public release.
2.6	Jan 2007	Updated Table 3 “Identifying Marks and Order Codes”.
2.7	Aug 2007	Added Erratum #2.
2.8	Mar 2010	Added Erratum #3.

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Contents

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1.0 Preface

This document is applicable to the dual port Intel® 82563EB Gigabit Platform LAN Connect and the single port Intel® 82564EB Gigabit Platform LAN Connect.

This document is an update to published specifications. Specification documents for this product include:

- 82563EB/82564EB Gigabit Platform LAN Connect Datasheet, Intel Corporation.
- 82563EB/82564EB LAN on Motherboard Design Guide AP-467, Intel Corporation.
- Intel® 631xESB/632xESB I/O Controller Hub EEPROM Information Guide Application Note (AP-477), Intel Corporation.
- Intel® 631xESB/632xESB I/O Controller Hub External Design Specification (EDS), Volumes 1-3, Intel Corporation.
- Bensley/Bensley-VS Platform Design Guide (PDG), Intel Corporation.

The intention for this document is for hardware system manufacturers and software developers of applications, operating systems, or tools. It may contain Specification Changes, Errata, Documentation Changes, and Specification Clarifications.

All product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

2.0 Nomenclature

This document uses various definitions, codes, and abbreviations to describe the Specification Changes, Errata, Documentation Changes, and/or Specification Clarifications that apply to the listed silicon/steppings:

Table 1. Definitions

Name	Description
Specification Changes	Modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
Errata	Design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.
Specification Clarifications	Greater detail or further highlights concerning a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
Documentation Changes	Typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Table 2. Codes and Abbreviations

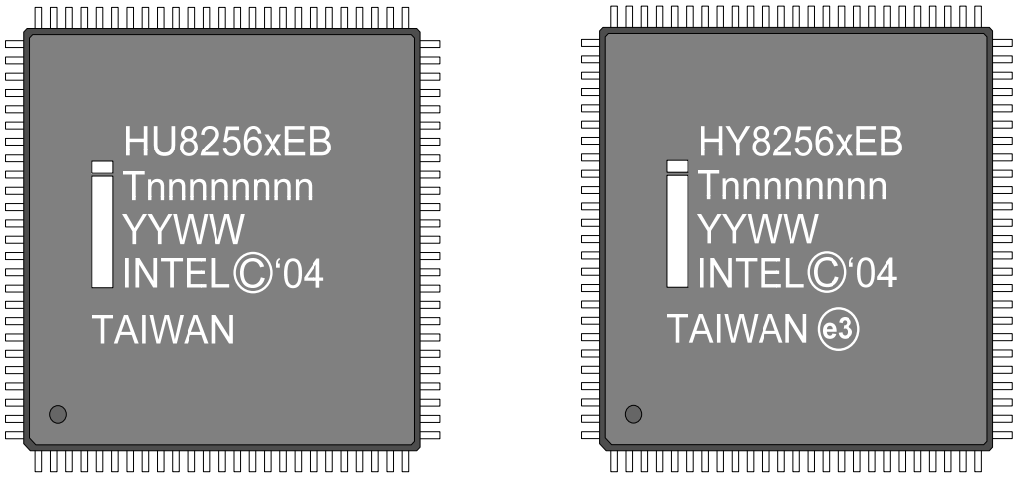
Name	Description
X	Specification Change, Erratum, or Specification Clarification that applies to this stepping.
Doc	Document change or update that will be implemented.
Fix	This erratum is intended to be fixed in a future stepping of the component.
Fixed	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded	This Item is either new or modified from the previous version of the document.
DS	Datasheet
SDM	Software Developer's Manual
AP	Application Note

3.0 Device Identification

The following table and drawings describe the various identifying markings on each device package:

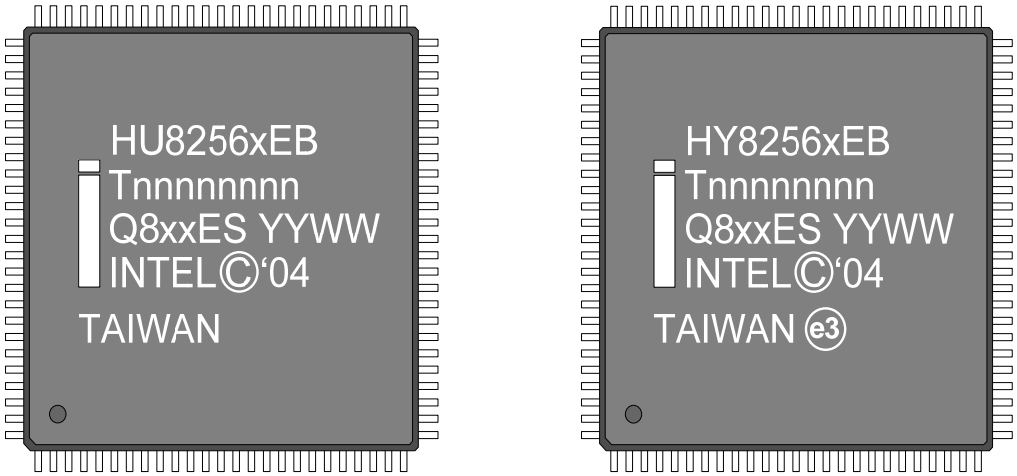
Table 3. Table of Identifying Marks and Order Codes

Device	Stepping	MM Number	S-Specification	Notes
HY82563EB	C-0	864991	S L7WG	Dual Port - Lead Free Production Units (T&R)
HY82563EB	C-0	864999	864999	Dual Port - Lead Free Production Units (Tray)



Leaded Version **Lead-Free Version**

Figure 1. 82563EB/82564EB Production Identifying Marks (not to scale)



Leaded Version **Lead-Free Version**

Figure 2. 82563EB/82564EB Engineering Samples Identifying Marks (not to scale)

4.0 Summary of Table Changes

No.	Plans	Specification Changes	Page
1	-	(None)	-
No.	**Plans**	**Errata**	**Page**
1	NoFix	Unwanted Start of Frame Delimiter (SFD) removal	13
2	NoFix	LAN Link Failure in the 82563EB/82564EB	14
3	NoFix	Tx Packet Lost After PHY Speed Change Using Auto-Negotiation	14
No.	**Plans**	**Specification Clarifications**	
1		Carrier Extension and Frame Bursting not Supported in any Mode	15
No.	**Plans**	**Documentation Changes**	**Page**
1	-	(None)	16

5.0 Specification Changes

1 (None)

6.0 Errata

1 Unwanted Start of Frame Delimiter (SFD) Removal

Problem: During 1000 Mbps operation, if the PHY receives a frame with only one byte of preamble followed by the SFD, the SFD will on occasion be replaced with the constant 0x55. In this scenario, there are only 2 bytes of header in the arriving frame. The first of these bytes is considered mutable by IEEE in that PHY's will substitute and later re-constitute the first preamble byte with special Start of Stream delimiters. However, the serial MAC-PHY interface used in the device requires that proper odd/even alignment be achieved before a frame can be delivered to its associated MAC. This re-alignment of the frame, when necessary, is accomplished by deleting a byte of the header. In a reduced header of only two bytes, this second deletion removes the SFD byte instead of a preamble byte.

Implication: Removing the SFD from any frame will cause the associated MAC to either miss the frame entirely or detect it with a CRC error present. In either case, the frame will not be delivered to the host system.

Workaround: There is no workaround available; however, IEEE mandates that all MAC transmitters send the full 7 bytes of preamble followed by SFD virtually ensuring that this erratum not impact existing networks.

Status: Intel does not plan to resolve this erratum in a future stepping of the Gigabit platform LAN connect.

2 LAN Link Failure in the 82563EB/82564EB

Problem: Under high stress conditions, the 82563EB/82564EB might exhibit link failure. The link failure can be either protocol corruption via the GLCI link or physical link down or via the MDI link. Although the problem can occur at any link speed, with MDIO transaction padding of 100 Mb-10x and 10 Mb-100x, failures have also occurred with 100 Mb/s and 10 Mb/s connections. The failure is a result of attempts to write to the PHY before the PHY is ready for a write instruction.

Note: This erratum is platform independent.

Implication: When software reads register 16 in page 193 of the 82563EB/ 82564EB (PHY), the in-band message has an incorrect address (0 instead of 16). Software then uses the incorrect address for a read-modify-write of register 16 in page 193 and clears bit 8. Clearing bit 8 puts the PHY in 631xESB/632xESB (MAC) mode, which stops normal operation.

Workaround: Check the address field (REGADDR, bits 20:16) in the MDIC register when the *Ready* bit is set. If the address is different then the address written then the read request must be issued a second time.

Status: Intel does not plan to resolve this erratum in a future stepping of the Gigabit platform LAN connect.

3 Tx Packet Lost After PHY Speed Change Using Auto-Negotiation

Problem: If the PHY establishes a link at 10/100 Mb/s and then auto-negotiation is re-started and a link is established at 1 Gb/s without resetting the PHY in between, the first 1-to-3 Tx packets provided by the MAC might not be transmitted.

Implication: This situation is generally seen during testing where the speed of the link partner is intentionally changed. During normal operation, the packet loss could occur if the cable was moved to a different port. In most cases, the higher layers would handle the packet loss and it would not be visible to the end user.

Workaround: If it is critical that no packets be lost, the software driver could be modified to perform a PHY reset each time it is notified of a speed change.

Status: Intel does not plan to resolve this erratum in a future stepping of the Gigabit platform LAN connect.

Specification Clarifications

1 Carrier Extension and Frame Bursting not Supported in any Mode

Problem: The 82563EB/82564EB does not support half-duplex operation at 1000 Mb/s. As a result, half-duplex features such as carrier extension and frame bursting are also unsupported in any link mode.

Affected Specs: 82563EB/82564EB Gigabit Platform LAN Connect Datasheet and 82563EB/82564EB LAN on Motherboard Design Guide.

7.0 Documentation Changes

1 (None)

8.0 Reference Schematics

Reference schematics describing a typical design layout for the 82563EB/82564EB Gigabit Ethernet Platform LAN Connect are contained in the Bensley/Bensley-VS Platform Design Guide (PDG).