# 82547GI(EI)/82541(PI/GI/EI)/ 82541ER EEPROM Map/ Programming Information Guide

## Application Note (AP-446)

Revision Number 2.5
June 2008

# Revision History

| Date | Revision | Description |
|---|---|---|
| June 2008 | 2.5 | Updated Word 21h bit definitions (changed word value to 93A7h). |
| May 2006 | 2.4 | Added lead-free version device ID for the 82541PI C0 to Table 7 and under “Component Identification Via Programming Interface”. |
| Apr 2005 | 2.3 | Updated Word 0Ah bit assignments (Table 6, bits 10 and 3) to match EEPROM image. |
| Feb 2005 | 2.2 | • Updated bit assignments for Words 0Fh and 21h. |
| Nov 2004 | 2.1 | • Updated EEPROM bit assignments to match EEPROM images. |
| Oct 2004 | 2.0 | • Added “Only if instructed to do so” to section 1.2.9.<br>• Removed section 1.2.11.<br>• Changed Word 0A bits 3 and 10 settings from 0 to 1 to match example images.<br>• Added 82541PI stepping information.<br>• Added new EEPROM images. |
| Apr 2004 | 1.61 | Changed Section 1.0; added OEM Configuration and EEPROM Image Version Sections. |
| Dec 2003 | 1.6 | Changed value of word 0x1f from “3649” to “0000” |
| Aug 2003 | 1.5 | Updated detail<br>Combined data from DOC 13401<br>Structure and grammar corrections |
| Oct 2002 | 1.0 | Initial release |

*Note:* This page is intentionally left blank.

# Contents

# 1.0 Introduction

The 82547GI(EI)/82541(PI/GI/EI) family of Gigabit Ethernet Controllers requires an external EEPROM that details the LOM (LAN on Motherboard) configuration data. These EEPROM images include configuration information to optimize the device performance as it relates to the specific design. For these controllers, performance is enhanced if the EEPROM includes information on the system design, for example if a combination magnetic-jack is used, or if a discrete magnetic component is used.

The 82547GI(EI)/82541(PI/GI/EI) family can use either a Microwire* or an SPI* EEPROM. The EEPROM mode is selected on the EE_MODE input (Ball J4). This pin should be pulled low for Microwire through a 1K Ohm resistor. For SPI mode, the pin can be left as a No Connect. The 82547GI(EI)/82541(PI/GI/EI) automatically reads several words after power-up to retrieve configuration information. The remainder of the EEPROM space is available to software for storing the MAC address, serial numbers, and additional information.

Intel has provided several reference EEPROM images located in Appendix A of this guide that can be used to generate an initial EEPROM image for a particular system, including:

- Systems with no management capability (integrated or discrete magnetics)
  - These EEPROM images include no system management support, and the motherboard design uses an integrated magnetic and board connector for the LAN connection.
- Systems that support ASF V1.0
- Systems that support ASF V2.0

  These EEPROM images include ASF V1.0 or ASF V2.0 system management support.
- Systems that support basic (TCO Basic) and advanced (TCO Advanced) pass through mode.
  - These EEPROM images include TCO Basic or TCO Advanced.

The 82541ER controller EEPROM map and image are explained in Appendix B.

Any one of these images may be used to generate the system manufacturer’s custom EEPROM image. The hardware system manufacture will review this document and update the EEPROM image for their particular implementation. Any text editor may be used to update the EEPROM image file. Once the image is finalized, EEUPDATE.EXE may be used to program the image. Comments in the file are acceptable as long as they are delimited with a semi-colon; a single semi-colon is all that is required. EEUPDATE.EXE will update all of the checksums within the device during the programming process.

The EEPROM access algorithm programmed into the controllers are compatible with most, but not all, commercially available 3.3V Microwire* interface serial EEPROM devices, with 64 x 16 (or 256 x 16) organization and a 2 MHz speed rating. The controller’s EEPROM access algorithms drives extra pulses on the shift clock at the beginning and end of read and write cycles. The extra pulses may violate the timing specifications of some EEPROM devices. In selecting a serial EEPROM, choose a device that specifies “don't care” shift clock states between accesses.

### EEPROM Size

For non-manageability applications, a 64 register by 16-bit Microwire serial or SPI EEPROM. For ASF 2.0 applications, the larger SPI EEPROM is required. For AoL/ASF 1.0, use at least a 4K SPI serial EEPROM. See table below for reference:

| Management | Microwire* | SPI | Notes |
|---|---|---|---|
| No | x | x | at least 1kbit |
| ASF 1.0 | | x | at least 4kbit |
| ASF 2.0 | | x | at least 8kbit |
| TCO Basic | | x | at least 4kbit |
| TCO Advanced | | x | at least 64kbit |

Microwire EEPROMs that have been found to work satisfactorily with the 82547GI(EI)/82541(PI/GI/EI)/82541ER Gigabit Ethernet Controller for non-manageability applications are listed in Table 1:

**Table 1. Microwire 64 x 16 Serial EEPROMs (no management)**

| Manufacturer | Manufacturer Part Number |
|---|---|
| Atmel | AT93C46 |
| Catalyst | CAT93C46 |

SPI EEPROMs that have been found to work satisfactorily with the 82547GI(EI)/82541(PI/GI/EI) device for manageability applications are listed in Table 2:

**Table 2. Serial EEPROMs for the 82547GI(EI)/82541(PI/GI/EI) Controller (Management Applications)**

| Manufacturer | Part Number | Interface | Size (Kbit) |
|---|---|---|---|
| Catalyst | CAT9366S-TE13 | uWire | 4 |
| Atmel | AT93C66-10SI-2.7 | uWire | 4 |
| STMicroElectronics | 95010W6 | SPI | 1 |
| Catalyst | CAT25010S | SPI | 1 |
| Atmel | AT25010N-10SI-2.7 | SPI | 1 |
| STMicroElectronics | 95040W6 | SPI | 4 |
| Catalyst | CAT25040S | SPI | 4 |
| Atmel | AT25040N-10SI-2.7 | SPI | 4 |
| STMicroElectronics | 95080W6 | SPI | 8 |
| Catalyst | CAT250C80S | SPI | 8 |
| Atmel | AT25080N-10SI-2.7 | SPI | 8 |
| STMicroElectronics | 95160W6 | SPI | 16 |
| Catalyst | CAT25C160S | SPI | 16 |

**Table 2. Serial EEPROMs for the 82547GI(EI)/82541(PI/GI/EI) Controller (Management Applications)**

| Manufacturer | Part Number | Interface | Size (Kbit) |
|---|---|---|---|
| Atmel | AT25160N-10SI-2.7 | SPI | 16 |
| STMicroElectronics | 95320W6 | SPI | 32 |
| Catalyst | CAT25C320S | SPI | 32 |
| Atmel | AT25320N-10SI-2.7 | SPI | 32 |
| STMicroElectronics | 95640W6 | SPI | 64 |
| Catalyst | 25C640S | SPI | 64 |
| Atmel | AT25640N-10SI-2.7 | SPI | 64 |

### Nomenclature

- Numbers without a suffix are decimal (base 10).
- Numbers with a suffix of “h” are hexadecimal (base 16).
- Numbers with a suffix of “b” are binary (base 2).

### Component Identification Via Programming Interface

The 82547 controller stepping will be identified by the following register contents:

| Stepping | Vendor ID | Device ID |
|---|---|---|
| 82547EI - A0 | 8086h | 1019h |
| 82547EI - A1 | 8086h | 1019h |
| 82547EI - B0 | 8086h | 1019h |
| 82547EI - B0 | 8086h | 101Ah (mobile) |
| 82547GI - B1 | 8086h | 1075h |

These devices also provide identification data through the Test Access Port (TAP).

The 82541 controller stepping will be identified by the following register contents:

| Stepping | Vendor ID | Device ID |
|---|---|---|
| 82541EI - A0 | 8086h | 1013h |
| 82541EI - A1 | 8086h | 1013h |
| 82541EI - B0 | 8086h | 1013h |
| 82541EI - B0 | 8086h | 1018h |
| 82541GI - B1 | 8086h | 1076h |
| 82541GI - B1 | 8086h | 1077h (mobile) |
| 82541PI - C0 | 8086h | 1076h |
| 82541PI - C0 | 8086h | 107Ch[a] |

a. Lead-free version. See Table 7 for default device ID values.

***Note:*** The 82541PI stepping is differentiated from the 82541GI stepping by revision ID and not by device ID.

The 82541ER controller stepping is identified by the following register content:

| Stepping | Vendor ID | Device ID |
|---|---|---|
| 82541ER | 8086h | 1078h |

This device also provides identification data through the Test Access Port (TAP).

## 1.1 EEPROM Map Information

Table 3 summarizes the full EEPROM map for the 82547GI(EI)/82541(PI/GI/EI) Gigabit Ethernet Controller.

**Table 3. 82547GI(EI)/82541(PI/GI/EI) EEPROM Memory Layout**

| | |
|---|---|
| **00h ... 3Fh** | HW/SW Reserved Area |
| **40h ... FFh** | ASF 1.0<br>Legacy Manageability |
| **100h ... 19F** | Manageability Packet Filter data |
| **1A0 ... EEPROM END** | Loadable Manageability Firmware Code |

**NOTE:**This map supports full ASF 2.0 manageability.

## 1.2 EEPROM Address Map

The following table is a more detailed EEPROM address map for the 82547GI(EI)/82541(PI/GI/EI) Gigabit Ethernet Controllers. Each of the data words is described in the following subsections. Note that these maps extend only through the address range for legacy manageability.

**Table 4. 82547GI(EI)/82541(PI/GI/EI) EEPROM Address Map (Sheet 1 of 2)**

| Word | Description: High Byte | Description: Low Byte | Hardware Access |
|---|---|---|---|
| 0 | IA Byte 2 | IA Byte 1 | Yes |
| 1 | IA Byte 4 | IA Byte 3 | Yes |
| 2 | IA Byte 6 | IA Byte 5 | Yes |
| 3 | Compatibility High Byte | Compatibility Low Byte | No |
| 4 | SW/HW Reserved | | No |
| 5 | EEPROM Image Version | | No |
| 6-7 | HW Reserved | | No |
| 8 | PBA, Byte 1 | PBA, Byte 2 | No |
| 9 | PBA, Byte 3 | PBA, Byte 4 | No |
| A | Initial Control 1, High Byte | Initial Control 1, Low Byte | Yes |
| B | Subsystem ID, High Byte | Subsystem ID, Low Byte | Yes |
| C | Subsystem Vendor ID, High Byte | Subsystem Vendor ID, Low Byte | Yes |
| D | Device ID, High Byte | Device ID, Low Byte | Yes |
| E | Vendor ID, High Byte | Vendor ID, Low Byte | Yes |
| F | Initial Control 2, High Byte | Initial Control 2, Low Byte | Yes |
| 10 - 11 | PHY Registers | | No |
| 12 | EEPROM Size | | Yes |
| 13-1E | PHY Registers | | No |
| 1F | IDDQ Configuration/CSA Port Config 1 | | Yes |
| 20 | Software Defined Pins Control | Software Defined Pins Control | Yes |
| 21 | HW Reserved/CSA Port Config 2 | | Yes |
| 22 | D0 Power | D3 Power | Yes |
| 23 | Management Control | Management Control | Yes |
| 24 | Initial Control 3 | SMB Address | Yes |
| 25 | IPv4 Address Byte 2 | IPv4 Address Byte 1 | Yes |
| 26 | IPv4 Address Byte 4 | IPv4 Address Byte 3 | Yes |
| 27 | IPv6 Address Byte 2 | IPv6 Address Byte 1 | Yes |
| 28 | IPv6 Address Byte 4 | IPv6 Address Byte 3 | Yes |
| 29 | IPv6 Address Byte 6 | IPv6 Address Byte 5 | Yes |
| 2A | IPv6 Address Byte 8 | IPv6 Address Byte 7 | Yes |
| 2B | IPv6 Address Byte 10 | IPv6 Address Byte 9 | Yes |
| 2C | IPv6 Address Byte 12 | IPv6 Address Byte 11 | Yes |

**Table 4. 82547GI(EI)/82541(PI/GI/EI) EEPROM Address Map (Sheet 2 of 2)**

| Word | Description: High Byte | Description: Low Byte | Hardware Access |
|---|---|---|---|
| 2D | IPv6 Address Byte 14 | IPv6 Address Byte 13 | Yes |
| 2E | IPv6 Address Byte 16 | IPv6 Address Byte 15 | Yes |
| 2F | LED Configuration Defaults | | Yes |
| 30 - 3E | PXE Configuration | | No |
| 3F | Checksum, High Byte | Checksum, Low Byte | No |
| 40 - F7 | Configured by ASF software | | Yes |
| F8 - FF | Reserved for software use | | Yes |

**NOTE:** Values listed in the EEPROM map table are hexadecimal.

## 1.2.1 Ethernet Address (Words 00h - 02h)

The Ethernet Individual Address (IA) is a 6-byte field that must be unique for each Ethernet port (and for each copy of the EEPROM image). The first three bytes are vendor specific. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0). For a MAC address of 12-34-56-78-90-AB, words 0-2 should be loaded as follows:

- Word 0 = 3412
- Word 1 = 7856
- Word 2 = AB90

***Note:*** These values are byte-swapped

## 1.2.2 Compatibility Fields (Word 03h)

Word 03h in the EEPROM image is reserved for compatibility information to be used by software drivers.

**Table 5. Compatibility Fields (Word 03h)**

| Bit | Name | Value |
|---|---|---|
| 15:12 | Reserved | 0000 |
| 11 | LOM Design 0 = No 1 = Yes (default) | 1 |
| 10 | Server Design 0 = No (Default) 1 = Yes | 0 |
| 9 | Client Design 0 = No 1 = Yes (Default) | 1 |
| 8 | OEM Design 0 = Intel Adapter 1 = OEM Adapter | 1 |
| 7:5 | Reserved | 000 |
| 4 | SMBus routed to Chipset[a] 0 = No 1 = Yes | 1 |
| 3 | Reserved | 0 |
| 2 | PCI Bridge Device Present 0 = No 1 = Yes | 0 |
| 1:0 | Reserved | 00 |

a. The default is dependent upon whether system management is supported or not

### 1.2.3 OEM Configuration Fields (Word 04h)

Word 04h in the EEPROM image is reserved for OEM configuration.

### 1.2.4 EEPROM Image Version Fields (Word 05h)

Word 05h in the EEPROM image is EEPROM image version.

| Bit | Name | Value |
|---|---|---|
| 15:12 | EEPROM major version | 0000 |
| 11:8 | EEPROM minor version | 0000 |
| 7:0 | EEPROM fix | 00000000 |

### 1.2.5 PBA Number (Words 08h - 09h)

A nine-digit printed board assembly (PBA) number used for Intel manufactured adapter cards is stored in a four-byte field. Other hardware manufacturers may use these fields for other purposes. The network driver should not rely on this field to identify the product or its capabilities.

### 1.2.6 Initialization Control Word 1 (Word 0Ah)

This is the first word read by the controller that contains initialization values to:

Set default values for some internal registers

Enable and disable specific features

Determine which PCI configuration space values will be loaded from the EEPROM

**Table 6. Initialization Control Word 1 (Word 0Ah)**

| Bit | Name | Description |
|---|---|---|
| 15:14 | Signature | The Signature field contains a signature of 01b indicating a valid EEPROM. If this field contains a value other than 01b, the EEPROM is invalid and the values in the EEPROM are not read. Therefore, default values are used for the configuration space IDs. |
| 13 | 64/32 BAR | This bit indicates whether the device is using 32-bit or 64-bit memory mapping.<br>0 = 64-bit memory mapping (default)<br>1 = 32-bit memory mapping<br>82547GI Reserved. Default setting = 1 |
| 12 | Reserved | Reserved. Set to 0 |
| 11 | Reserved | Reserved. Set to 0 |
| 10 | Reserved | Reserved. Set to 1 |
| 9 | Reserved | Reserved. Set to 0 |
| 8 | Reserved | Reserved. Set to 0 |
| 7 | Internal VREG Power down Control | This bit is used to define usage of internal 1.2V and 1.8V regulators to supply power<br>0 = Yes (Default)<br>1 = No (external regulators are being used) |

**Table 6. Initialization Control Word 1 (Word 0Ah)**

| Bit | Name | Description |
|---|---|---|
| 6:4 | Reserved | Reserved. Set to 0 |
| 3 | Reserved | Reserved. Set to 1 |
| 2 | Reserved | Reserved. Set to 0 |
| 1 | Subsystem and Subsystem Vendor ID | This bit indicates whether or not to load the Subsystem ID and Subsystem Vendor ID from the EEPROM.<br>0 = Do not load the Subsystem and subsystem vendor ID from the EEPROM<br>1 = Load the Subsystem and subsystem vendor ID from the EEPROM (Default) |
| 0 | PCI Device and Vendor ID | This bit indicates whether or not to load the Vendor ID and Device ID from the EEPROM<br>0 = Do not load the Vendor ID from the EEPROM<br>1 = Load the Vendor ID from the EEPROM (Default |

## 1.2.7 Identification Words (Words 0Bh - 0Eh)

These words contain the Subsystem ID, Subsystem Vendor ID, Device ID, and Vendor ID. Table 7 lists examples of the different identification word settings.

**Table 7. Identification Words**

| Vendor ID | Device ID | Subsystem Vendor ID | Subsystem ID | Comments |
|---|---|---|---|---|
| 8086 | 1013 | 8086 | 1013 | **82541EI LOM.** Default value if EEPROM not present. |
| 8086 | 1018 | 8086 | 1018 | **82541EI.** Mobile applications. |
| 8086 | 1076 | 8086 | 1076 | **82541GI LOM.** Default value if EEPROM not present. |
| 8086 | 1077 | 8086 | 1077 | **82541GI.** Mobile applications. |
| 8086 | 1076 | 8086 | 1076 | **82541PI LOM.** Default value if EEPROM not present. |
| 8086h | 107C | 8086 | 107C | **82541PI LF LOM.** Default Device ID and Subsystem ID values are 1076 if EEPROM is not present. |
| 8086 | 1019 | 8086 | 1019 | **82547EI LOM.** Default value if EEPROM not present |
| 8086 | 101A | 8086 | 101A | **82547EI.** Mobile applications. |
| 8086 | 1075 | 8086 | 1075 | **82547GI LOM.** Default value if EEPROM not present. |
| 8086 | 1078 | 8086 | 1078 | **82541ER LOM.** Default value if EEPROM not present. |

**NOTE:** The values in this table are in hexadecimal.

#### 1.2.7.1 Subsystem ID (Word 0Bh)

If the Signature bits (15:14) and Load Subsystem IDs bit (1) in word 0Ah are valid, this word will be read in to initialize the Subsystem ID.

#### 1.2.7.2 Subsystem Vendor ID (Word 0Ch)

If the Signature bits (15:14) and Load Subsystem IDs bit (1) of word 0Ah are valid, this word will be read in to initialize the Subsystem Vendor ID.

#### 1.2.7.3 Device ID (Word 0Dh)

If the Signature bits (15:14) and Load Vendor/Device IDs bit (0) of EEPROM word 0Ah are valid, this word will be read in to initialize the Device ID.

#### 1.2.7.4 Vendor ID (Word 0Eh)

If the Signature bits (15:14) and Load Vendor/Device IDs bit (0) of EEPROM word 0Ah are valid, this word will be read in to initialize the Device ID.

### 1.2.8 Initialization Control Word 2 (Word 0Fh)

This is the second word read by the controller and contains additional initialization values to:

- Set defaults for some internal registers
- Enable and disable specific features

**Table 8. Initialization Control Word 2 (Word 0Fh)**

| Bit | Name | Description |
|---|---|---|
| 15 | APM PME# Enable | This bit is the initial value of the Assert PME on APM Wake Up bit in the Wake Up Control Register (WUC.APMPME). It is typically set to 1 for Intel LAN adapters. |
| 14 | ASDE | This bit reflects the initial value of the Auto-Speed Detection Enable bit of the Device Control Register (CTRL). The hardware default value is 0 (the PHY tells MAC the speed). |
| 13:11 | Reserved | Reserved. Set to 0. |
| 10:9 | Flash Size | This field indicates the Flash size:<br>00 = 64 Kbytes (hardware default)<br>01 = 128 Kbytes<br>10 = 256 Kbytes<br>11 = 512 Kbytes<br>These bits impact the requested memory space for the Flash and Expansion ROM BARs in the PCI configuration space. |
| 8 | MAC Clock Speed (82541PI/GI) | When programmed to 0, MAC runs at full speed.<br>When set as 1, MAC runs at 1/4 speed on any drop from 1000 mb/s. |
| | Reserved (82547GI/EI) | Reserved. Set to 0 |
| 7 | Reserved | Reserved. Set to 0 |
| 6:3 | Reserved | Reserved. Set to 0 |

### Table 8. Initialization Control Word 2 (Word 0Fh)

| Bit | Name | Description |
|---|---|---|
| 2 | Reserved | Reserved. Set to 0 |
| 1 | Reserved | Reserved. Set to 0 |
| 0 | Reserved (82547GI/EI) | Reserved. Set to 0 |
| | 8254EI | Set to 0. |

**NOTE:** The values in this table are hexadecimal.

## 1.2.9 PHY Register Address Data (Words 10h, 11h, and 13h-1Eh)

These settings are specific to individual platform configurations and should not be altered from the reference designs unless you are instructed to do so. Refer to Appendix for reference settings specific to a particular platform design. Future Intel devices may use this space differently.

## 1.2.10 EEPROM size (word 12h)

This word is only applicable to SPI EEPROMS which are typically need for manageability applications. Unused bits are reserved and should be programmed to 0. Bits 15:13 and 8:0 are reserved. See the table below:.

### Table 9. SPI EEPROM Size

| Bits 12:10 | Bit 9 | EEPROM Size (Bits) | EEPROM Size (Bytes) |
|---|---|---|---|
| 000 | 0 | 1Kbit | 128byte |
| 001 | 1 | 4Kbit | 512byte |
| 010 | 1 | 8Kbit | 1Kbyte |
| 011 | 1 | 16Kbit | 2Kbyte |
| 100 | 1 | 32Kbit | 4Kbyte |
| 101 | 1 | 64Kbit | 8Kbyte |
| 110 | 1 | 128Kbit | 16Kbyte |
| 111 | 1 | Reserved | Reserved |

### 1.2.11 CSA Port Configuration 1 (Word 1Fh) (82547GI(EI) Only)

For the 82547GI(EI), this word controls the CSA hublink port configuration and must be programmed to 0000h for regular operation. Note that this word should maintain constant values. Do not change any values unless you are instructed to do so.

**Table 10. CSA Port Configuration 1**

| Bit | Name | Description |
|---|---|---|
| 15 | Hub interface mode | 4 bit =1 8 bit =0 (Default =0) |
| 14:12 | CSA N-Comp Buffer Strength (MSBs) | Default setting 0 |
| 8:11 | CSA N-Comp buffer Strength (LSBs) | Default setting 0 |
| 7 | CSA R-Comp Not overridden | Default 0 |
| 6:4 | CSA P-Comp buffer strength (MSBs) | Default 0 |
| 3:0 | CSA P-Comp buffer (LSBs) | Default 0 |

### 1.2.12 Software Defined Pins Control (Word 20h)

**Table 11. Software Defined Pins Control (Word 20h)**

| Bit | Name | Description |
|---|---|---|
| 15 | SDPDIR[3] | **SDP3 Pin - Initial Direction.** This bit configures the initial HW value of the SDP3_IODIR bit in the Extended Device Control Register (CTRL_EXT) following powerup.<br>0 = In; 1 = Out |
| 14 | SDPDIR[2] | **SDP2 Pin - Initial Direction.** This bit configures the initial HW value of the SDP2_IODIR bit in the Extended Device Control Register (CTRL_EXT) following powerup.<br>0 = In; 1 = Out |
| 13:10 | Reserved | **Reserved.** Set to 0 |
| 9 | SDPDIR[1] | **SDP1 Pin - Initial Direction.** This bit configures the initial HW value of the SDP1_IODIR bit in the Device Control Register (CTRL) following powerup.<br>0 = In; 1 = Out |
| 8 | SDPDIR[0] | **SDP0 Pin - Initial Direction.** This bit configures the initial HW value of the SDP0_IODIR bit in the Device Control Register (CTRL) following powerup.<br>0 = In; 1 = Out |
| 7 | SDPVAL[3] | **SDP3 Pin - Initial Output Value.** This bit configures the initial power-on value output on SDP3 (when configured as an output) by configuring the initial HW value of the SDP3_DATA bit in the Extended Device Control Register (CTRL_EXT) after powerup. |
| 6 | SDPVAL[2] | **SDP2 Pin - Initial Output Value.** This bit configures the initial power-on value output on SDP2 (when configured as an output) by configuring the initial HW value of the SDP2_DATA bit in the Extended Device Control Register (CTRL_EXT) after powerup. |
| 5:4 | Reserved | Reserved. Set to 0 |
| 3 | EN_PHY_PWR_MGMT | Configures the initial HW default value of this bit in the Device Control Register (CTRL) following powerup. |

| Bit | Name | Description |
|---|---|---|
| 2 | D3_COLD_WAKEUP_ADV_EN | Configures the initial HW default value of the ADVD3WUC bit in the Device Control Register (CTRL) following powerup. |
| 1 | SDPVAL[1] | **SDP1 Pin - Initial Output Value.** This bit configures the initial power-on value output on SDP1 (when configured as an output) by configuring the initial HW value of the SDP1_DATA bit in the Device Control Register (CTRL) after powerup. |
| 0 | SDPVAL[0] | **SDP0 Pin - Initial Output Value.** This bit configures the initial power-on value output on SDP0 (when configured as an output) by configuring the initial HW value of the SDP0_DATA bit in the Device Control Register (CTRL) after powerup. |

### 1.2.13 CSA Port Configuration 2 (word 21h) (82547EI/GI only)

This word controls the CSA port configuration and must be programmed to 93A7h for regular operation.

**Table 12. CSA Port Configuration 2**

| Bit # | Description | Default |
|---|---|---|
| 15:13 | Reserved | Set to 100 |
| 12 | Reserved | Set to 1 |
| 11:2 | Reserved | Set to 0011101001 |
| 1 | Dock/ Undock polarity | 1 (Indicates docked) |
| 0 | Reserved | 1 |

### 1.2.14 D0 Power (word 22h high byte)

If the signature bits are valid and Power Management is not disabled, then the value in this field is used in the PCI Power Management Data Register when the Data_Select field of the Power Management Control/Status Register (PMCSR) is set to 0 or 4. It indicates the power usage and heat dissipation of the networking function (including the Ethernet controller and any other devices controlled by the chip in tenths of a watt. Example:

```
If Word 22 = 290E, POWER CONSUMPTION (in 1/10W, hex), then:

    bits 15:8 = 29h Power in D0a, 29h = 4.1W

    bits 7:0 = 0Eh Power in D3h, 0Eh = 1.4W
```

### 1.2.15 D3 Power (word 22h low byte)

If the signature bits are valid and Power Management is not disabled, then the value in this field is used in the PCI Power Management Data Register when the Data_Select field of the Power Management Control/Status Register (PMCSR) is set to 3 or 7. It indicates the power usage and heat dissipation of the networking function (including the Ethernet controller and any other devices controlled by the chip in tenths of a watt (see the example above: Section 1.2.14).

### 1.2.16 Management Control (word 23h)

This word contains initial settings for the Management Control Register as well as valid bits for the IPv4 Address and IPv6 Address.

**Table 13. Management Control (word 23h)**

| Bit | Name | Description |
|---|---|---|
| 15 | Reserved | Reserved. Set to 0. |
| 14 | Neighbor Discovery Packets | Initial value of MANC.NEIGHBOR_EN bit.<br>1 = IPv6 Neighbor Discovery packets are Management packets for delivery to external TCO controller (82559 mode).<br>0 = IPv6 Neighbor Discovery packets go to host memory. If SMBus is disabled, then program this bit to 0. |
| 13 | Enable ARP Filtering | This bit controls the initial value of the MANC.ARP_EN bit.<br>1=Send ARP Request packets to SMBus (in 82559 mode after a *Receive Enable* SMBus command enabling packet filtering) or automatically generate ARP Reply packets (in ASF mode)<br>0=Send ARP Request packets to host memory<br>**Note:** Refer to the ARP Support section of the *Total Cost of Ownership (TCO) System Management Bus Interface* Application Note (AP-430) for the 82541xx controllers. This document provides information regarding the usage of flexible filters for handling ARP Request packets. |
| 12:10 | Reserved | Reserved. Set to 0 |
| 9 | Enable RMCP 0298h filtering | This bit controls the initial value of the MANC.0298_EN bit, which permits sending UDP packets of port 0298h to the SMBus or ASF controller.<br>1 = Allow; 0 = Don't allow |
| 8 | Enable RMCP 026F filtering | This bit controls the initial value of the MANC.RMCP_EN bit, which permits sending UDP packets of port 026Fh to the SMBus or ASF controller.<br>1 = Allow; 0 = Don't allow |
| 7 | IPv6 Address Valid | IPv6 Address in the *IP Address* EEPROM register is valid. This is written to bit 16 of the *IP Address Valid* (IPAV[16]) register. |
| 6 | IPv4 Address Valid | IPv4 Address in the *IP Address* EEPROM register is valid. This is written to bit 0 of the *IP Address Valid* (IPAV[0]) register. |
| 5 | Flex Filter Enable | This bit enables the flexible filter loaded from the EEPROM.<br>0 = Disable, 1 = Enable |
| 4:3 | Reserved | Reserved. Set to 0. |
| 2 | Reset on ForceTCO | Reset the 82547EI on a ForceTCO SMBus Command with the "Force" bit set to 1 in 82559 mode, or on various conditions in ASF mode.<br>Program to 0 if SMBus is not used. |
| 1 | ASF Mode | 1=ASF mode, 0=82559 compatible mode |
| 0 | SMBus Enable | Enables SMBus functionality.<br>1 = Enable; 0 = Disable |

### 1.2.17 Initialization Control 3 (Word 24h)

The word controls general initialization values.

| 82541PI(GI) / 82547PI(GI) | | |
|---|---|---|
| **Bit** | **Name** | **Description** |
| 15:13 | Reserved | See configuration options in Appendix A |
| 12 | PCI Interrupt | See configuration options in Appendix A |
| 11 | Enable/Disable FLASH Logic | Set by IBA |
| 10 | Enable/Disable APM | See configuration options in Appendix A |
| 9:8 | Reserved | See configuration options in Appendix A |
| 7:0 | Reserved | See configuration options in Appendix A |

| 82541EI / 82547EI | | |
|---|---|---|
| **Bit** | **Name** | **Description** |
| 15:4 | Reserved | See configuration options in Appendix A |
| 3 | Enable/Disable FLASH Logic | A value of 1 disables the FLASH logic. The expansion ROM and secondary FLASH access BARs in the PCI config space are disabled. |
| 2 | APM Enable | Initial value of *Advanced Power Management Wake Up Enable* in the *Wake Up Control Register* (WUC.APME). |
| 1:0 | Reserved | See configuration options in Appendix A |

### 1.2.18 SMBus Slave Address (word 24h low byte)

| Bit | Name | Description |
|---|---|---|
| 7:1 | SMBus Slave Address | Contains the SMBus slave address for 82559 compatible SMBus mode. This must be 1100 100(b) for ASF mode. |
| 0 | Reserved | Reserved. Set to 0 |

***Note:*** Note: This byte must be C8h for ASF mode.

### 1.2.19 IPv4 Address (words 25h-26h)

Not used – should be FFFFh

### 1.2.20 IPv6 Address (words 27h-2Eh)

Not used – should be FFFFh

### 1.2.21 LED Configuration Defaults (Word 2Fh)

This EEPROM word specifies the hardware defaults for the LED Control Register (LEDCTL) fields controlling the LED0 (LINK_UP) and LED2 (LINK_100) output behaviors.

A value of 0602h configures the LED behavior to be equivalent to a LAN port based on the legacy 82544EI/GC controller.

**Table 14. LED Configuration (Word 0Fh)**

| Bit | Name | Description |
|---|---|---|
| 15 | LED2 Blink | This bit reflects the initial value of the LED2 blink field in the LED control register:<br>0 = Non-blinking<br>1 = Blinking |
| 14 | LED2 Invert | This bit reflects the initial value of the LED2 invert field in the LED control register:<br>0 = Do not invert output (active low)<br>1 = Invert output |
| 13:12 | Reserved | Reserved. Set to 0. |
| 11:8 | LED2 Mode | This bit reflects the initial value of the LED2 mode field in the LED control register. It specifies which event, state, or pattern will be displayed on LED2 (LINK_100) output. For example, a value of 0111 indicates 1000 Mbps link operation. |
| 7 | LED0 Blink | This bit reflects the initial value of the LED0 blink field in the LED control register:<br>0 = Non-blinking<br>1 = Blinking |
| 6 | LED0 Invert | This bit reflects the initial value of the LED0 invert field in the LED control register:<br>0 = Do not invert output (active low)<br>1 = Invert output |
| 5:4 | Reserved | Reserved. Set to 0 |
| 3:0 | LED0 Mode | This bit reflects the initial value of the LED0 mode field in the LED control register. It specifies which event, state, or pattern will be displayed on LED0 (LINK_UP) output. For example, a value of 0010 indicates activity. |

### 1.2.22 Boot Agent Main Setup Options (Word 30h)

The boot agent software configuration is controlled by the EEPROM with the main setup options stored in word 30h. These options are those that can be changed by using the Control-S setup menu or by using the IBA Intel Boot Agent utility. Note that these settings only apply to Boot Agent software.

### Table 15. Boot Agent Main Setup Options

| Bit | Name | Description |
|---|---|---|
| 15 | PPB | PXE Presence.<br>Setting this bit to 0b Indicates that the image in the FLASH contains a PXE image.<br>Setting this bit to 1b indicates that no PXE image is contained.<br>The default for this bit is 0b in order to be backwards compatible with existing systems already in the field.<br>If this bit is set to 0b, EEPROM word 32h (PXE Version) is valid. When EPB is set to 1 and this bit is set to 0, indicates that both images are present in the FLASH. |
| 14 | EPB | EFI Presence.<br>Setting this bit to 1b Indicates that the image in the FLASH contains an EFI image.<br>Setting this bit to 0b indicates that no EFI image is contained.<br>The default for this bit is 0 in order to be backwards compatible with existing systems already in the field.<br>If this bit is set to 1b, EEPROM word 33h (EFI Version) is valid. When PPB is set to 0b and this bit is set to 1b, indicates that both images (PXE and EFI) are present in the FLASH. |
| 13 | Reserved | Reserved for future use. Set this bit to 0b. |
| 12 | FDP | Force Full Duplex.[a]<br>Set this bit to 0b for half duplex; set to 1b for full duplex.<br>Note that this bit is a don't care unless bits 10 and 11 are set. |
| 11:10 | FSP | Force Speed.[b]<br>These bits determine speed. 01b = 10Mbs, 10b = 100Mbs, 11b = Not allowed.<br>All zeros indicate Auto-negotiate (the current bit state).<br>Note that bit 12 is a don't care unless these bits are set. |
| 9 | LWS | Legacy OS Wakeup Support (for 82559-based adapters only).<br>If set to 1b, the agent enables PME in the adapter's PCI configuration space during initialization. This allows remote wakeup under legacy operating systems that don't normally support it. Note that enabling this bit makes the network controller technically non-compliant with the ACPI specification.<br>0b = Disabled (Default Value)<br>1b = Enabled |
| 8 | DSM | Display Setup Message.<br>If this bit is set to 1b, the "Press Control-S" message appears after the title message.<br>The default for this bit is 1b. |

### Table 15. Boot Agent Main Setup Options

| Bit | Name | Description |
|---|---|---|
| 7:6 | PT | Prompt Time. These bits control how long the "Press Control-S" setup prompt message appears, if enabled by DIM.<br>00b = 2 seconds (default)<br>01b = 3 seconds<br>10b = 5 seconds<br>11b = 0 seconds<br>Note that the Ctrl-S message does not appear if 0 seconds prompt time is selected. |
| 5 | LBS | Local Boot Selection (OBSOLETE). In previous versions of the agent, this bit enables or disables local boot, if the DBS bit selects it.<br>The default for this bit is 1b; enable local booting. The boot agent, at runtime, no longer uses this bit. |
| 4:3 | DBS | Default Boot Selection. These bits select which device is the default boot device. These bits are only used if the agent detects that the BIOS does not support boot order selection or if the MODE field of word 31h is set to MODE_LEGACY.<br>00b = Network boot, then local boot<br>01b = Local boot, then network boot<br>10b = Network boot only<br>11b = Local boot only |
| 2 | BBS | BIOS Boot Specification (OBSOLETE). In previous versions of the agent, this bit enables or disables use of the BBS to determine boot order. If set to 1, the BIOS boot order is used, and the DBS bits are ignored. The boot agent at runtime no longer uses this bit. The runtime checks for BBS/PnP and the setting in the MODE field of word 31h are used instead. |
| 1:0 | PS | Protocol Select. These bits select the boot protocol.<br>00b = PXE (default value)<br>01b = RPL protocol<br>Other values are undefined. |

a. This setting only applies to the Boot Agent software.
b. This setting only applies to the Boot Agent software.

### 1.2.23 Boot Agent Configuration Customization Options (Word 31h)

Word 31h contains settings that can be programmed by an OEM or network administrator to customize the operation of the software. These settings cannot be changed from within the Control-S setup menu or the IBA Intel Boot Agent utility. The lower byte contains settings that would typically be configured by a network administrator using the Intel Boot Agent utility; these settings generally control which setup menu options are changeable. The upper byte are generally settings that would be used by an OEM to control the operation of the agent in a LOM environment, although there is nothing in the agent to prevent their use on a NIC implementation.

**Table 16. Boot Agent Configuration Customization Options (Word 31h)**

| Bit | Name | Description |
|---|---|---|
| 15:14 | SIG | Signature. These bits must be set to 1b to indicate that this word has been programmed by the agent or other configuration software. |
| 13:11 | Reserved | Reserved for future use. Set these bits to 0b. |
| 10:8 | MODE | Selects the agent's boot order setup mode. This field changes the agent's default behavior in order to make it compatible with systems that do not completely support the BBS and PnP Expansion ROM standards. Valid values and their meanings are:<br>000b - Normal behavior. The agent attempts to detect BBS and PnP Expansion ROM support as it normally does.<br>001b - Force Legacy mode. The agent does not attempt to detect BBS or PnP Expansion ROM supports in the BIOS and assumes the BIOS is not compliant. The BIOS boot order can be changed in the Setup Menu.<br>010b - Force BBS mode. The agent assumes the BIOS is BBS-compliant, even though it may not be detected as such by the agent's detection code. The BIOS boot order CANNOT be changed in the Setup Menu.<br>011b - Force PnP Int18 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 18h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu.<br>100b - Force PnP Int19 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 19h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu.<br>101b - Reserved for future use. If specified, treated as value 000b.<br>110b - Reserved for future use. If specified, treated as value 000b.<br>111b - Reserved for future use. If specified, treated as value 000b. |
| 7:6 | Reserved | Reserved for future use. Set these bits to 0b. |
| 5 | DFU | Disable FLASH Update.<br>If set to 1b, no updates to the FLASH image using PROSet is allowed.<br>The default for this bit is 0b; allow FLASH image updates using PROSet. |
| 4 | DLWS | Disable Legacy Wakeup Support.<br>If set to 1b, no changes to the Legacy OS Wakeup Support menu option is allowed.<br>The default for this bit is 0b; allow Legacy OS Wakeup Support menu option changes. |

**Table 16. Boot Agent Configuration Customization Options (Word 31h)**

| Bit | Name | Description |
|---|---|---|
| 3 | DBS | Disable Boot Selection.<br>If set to 1b, no changes to the boot order menu option is allowed.<br>The default for this bit 0; allow boot order menu option changes. |
| 2 | DPS | Disable Protocol Select.<br>If set to 1b, no changes to the boot protocol is allowed.<br>The default for this bit is 0b; allow changes to the boot protocol. |
| 1 | DTM | Disable Title Message.<br>If set to 1b, the title message displaying the version of the boot agent is suppressed; the Control-S message is also suppressed. This is for OEMs who do not wish the boot agent to display any messages at system boot.<br>The default for this bit is 0b; allow the title message that displays the version of the boot agent and the Control-S message. |
| 0 | DSM | Disable Setup Menu.<br>If set to 1b, no invoking the setup menu by pressing Control-S is allowed. In this case, the EEPROM can only be changed via an external program.<br>The default for this bit is 0b; allow invoking the setup menu by pressing Control-S. |

## 1.2.24 Boot Agent Configuration Customization Options (Word 32h)

Word 32h is used to store the version of the boot agent that is stored in the FLASH image. When the Boot Agent loads, it can check this value to determine if any first-time configuration needs to be performed. The agent then updates this word with its version. Some diagnostic tools to report the version of the Boot Agent in the FLASH also read this word. This word is only valid if the PPB is set to 0. Otherwise the contents may be undefined.

**Table 17. Boot Agent Configuration Customization Options (Word 32h)**

| Bit | Name | Description |
|---|---|---|
| 15:12 | MAJOR | PXE boot agent major version. The default for these bits is 0b. |
| 11:8 | MINOR | PXE boot agent minor version. The default for these bits is 0b. |
| 7:0 | BUILD | PXE boot agent build number. The default for these bits is 0b. |

### 1.2.25 IBA Capabilities (Word 33h)

Word 33h is used to enumerate the boot technologies that have been programmed into the FLASH. It is updated by IBA configuration tools and is not updated or read by IBA.

**Table 18. IBA Capabilities**

| Bit | Name | Description |
|---|---|---|
| 15:14 | SIG | Signature. These bits must be set to 1b to indicate that this word has been programmed by the agent or other configuration software. |
| 13:5 | Reserved | Reserved for future use. Set these bits to 0b. |
| 4 | SAN | SAN capability is present in FLASH.<br>0b = The SAN capability is not present (default).<br>1b = The SAN capability is present. |
| 3 | EFI | EFI UNDI capability is present in FLASH.<br>0b = The RPL code is not present (default).<br>1b = The RPL code is present. |
| 2 | RPL | RPL capability is present in FLASH.<br>1b = The RPL code is present (default).<br>0b = The RPL code is not present. |
| 1 | UNDI | PXE/UNDI capability is present in FLASH.<br>1b = The PXE base code is present (default).<br>0b = The PXE base code is not present. |
| 0 | BC | PXE base code is present in FLASH.<br>0b = The PXE base code is present (default).<br>1b = The PXE base code is not present. |

### 1.2.26 Intel Boot Agent (Word 34h - 3Eh)

Reserved.

### 1.2.27 Checksum Word Calculation (Word 3Fh)

The Checksum word (3Fh) is calculated by adding all EEPROM words (00h - 3Fh), including the Checksum word itself. The sum should equal BABAh. The initial value in the 16-bit summing register should be 0000h, and the carry bit should be ignored after each addition. This checksum is not accessed by the controller device. If CRC checking is required, it must be performed by software.

### 1.2.28 Word 40h - F7h

These words are configured by ASF software.

### 1.2.29 ASF 2.0 Configuration Area Pointer (Word F8h)

This value holds a pointer (offset in 16 bit words from address 0) to the start of the ASF 2.0 configuration area [in the EEPROM]. If this pointer equals 0, the EEPROM will not contain an ASF 2.0 configuration area. If the EEPROM contains an ASF 2.0 configuration area, this pointer will contain this area's address.

***Note:*** A CRC field does not protect this pointer.

### 1.2.30 Code Upgrade Ara Pointer (Word F9h)

This value holds a pointer (offset in 16 bit words from address 0) to the start of the ASF 2.0 code upgrade area. If this pointer equals 0, the EEPROM will not contain a Code Upgrade area. If the EEPROM contains a Code Upgrade area, this pointer will contain this area's address.

***Note:*** A CRC field does not protect this pointer

# Appendix A Sample Starter EEPROM Images

## A.1 82541(PI/GI/EI) No Management and No Integrated Magnetics

```
0/8  1/9  2/A  3/B  4/C  5/D  6/E  7/F
FFFF FFFF FFFF 0210 FFFF 1000 FFFF FFFF
FFFF FFFF 640B 1076 8086 1076 8086 B284
20DD 2222 0000 2F90 2380 0012 1E20 0012
1E20 0012 1E20 0012 1E20 0009 0200 0000
000C 93A6 280B 0000 0400 FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF 0602
0100 4000 1210 4007 FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```

## A.2 82547GI(EI) No Management and No Integrated Magnetics

```
0/8  1/9  2/A  3/B  4/C  5/D  6/E  7/F
FFFF FFFF FFFF 0B10 FFFF 2066 FFFF FFFF
FFFF FFFF 640B 1075 8086 1075 8086 B204
20DD 2222 0000 2F90 2380 0012 1E20 0012
1E20 0012 1E20 0012 1E20 0009 0200 0000
000C 93A7 290E 0000 0400 FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF 0602
0100 4000 1210 4007 FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```

# Appendix B 82541ER Programmers' Supplement

The following table is a more detailed EEPROM address map for the 82541ER Gigabit Ethernet Controller. Each of the data words is described in the following subsections.

### Table 19. 82541ER EEPROM Address Map

| Word | Description: High Byte | Description: Low Byte | Hardware Access |
|---|---|---|---|
| 0 | IA Byte 2 | IA Byte 1 | Yes |
| 1 | IA Byte 4 | IA Byte 3 | Yes |
| 2 | IA Byte 6 | IA Byte 5 | Yes |
| 3 | Compatibility High Byte | Compatibility Low Byte | No |
| 4 | HW Reserved | | No |
| 5 | EEPROM Image Version | | No |
| 6-7 | HW Reserved | | No |
| 8 | PBA, Byte 1 | PBA, Byte 2 | No |
| 9 | PBA, Byte 3 | PBA, Byte 4 | No |
| A | Initial Control 1, High Byte | Initial Control 1, Low Byte | Yes |
| B | Subsystem ID, High Byte | Subsystem ID, Low Byte | Yes |
| C | Subsystem Vendor ID, High Byte | Subsystem Vendor ID, Low Byte | Yes |
| D | Device ID, High Byte | Device ID, Low Byte | Yes |
| E | Vendor ID, High Byte | Vendor ID, Low Byte | Yes |
| F | Initial Control 2, High Byte | Initial Control 2, Low Byte | Yes |
| 10 - 11 | Reserved | | No |
| 12 | Reserved | | Yes |
| 13-1E | Reserved | | No |
| 1F | Reserved | | Yes |
| 20 | Software Defined Pins Control | Software Defined Pins Control | Yes |
| 21 | HW Reserved/CSA Port Config 2 | | Yes |
| 22 | D0 Power | D3 Power | Yes |
| 23 | Reserved | Reserved | Yes |
| 24 | Initial Control 3 | Reserved | Yes |
| 25 | Reserved | Reserved | Yes |
| 26 | Reserved | Reserved | Yes |
| 27 | Reserved | Reserved | Yes |
| 28 | Reserved | Reserved | Yes |
| 29 | Reserved | Reserved | Yes |
| 2A | Reserved | Reserved | Yes |
| 2B | Reserved | Reserved | Yes |
| 2C | Reserved | Reserved | Yes |

### Table 19. 82541ER EEPROM Address Map

| Word | Description: High Byte | Description: Low Byte | Hardware Access |
|---|---|---|---|
| 2D | Reserved | Reserved | Yes |
| 2E | Reserved | Reserved | Yes |
| 2F | LED Configuration Defaults | | Yes |
| 30 - 3E | Reserved | | No |
| 3F | Checksum, High Byte | Checksum, Low Byte | No |

**NOTE:** Values listed in the EEPROM map table are hexadecimal.

## B.3 Ethernet Address (Words 00h - 02h)

The Ethernet Individual Address (IA) is a 6-byte field that must be unique for each Ethernet port (and for each copy of the EEPROM image). The first three bytes are vendor specific. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0). For a MAC address of 12-34-56-78-90-AB, words 0-2 should be loaded as follows:

- Word 0 = 3412
- Word 1 = 7856
- Word 2 = AB90

***Note:*** These values are byte-swapped

## B.4 Compatibility Fields (Word 03h)

Word 03h in the EEPROM image is reserved for compatibility information to be used by software drivers.

### Table 20. Compatibility Fields (Word 03h)

| Bit | Name | Value |
|---|---|---|
| 15:12 | Reserved | 0000 |
| 11 | LOM Design 0 = No 1 = Yes (default) | 1 |
| 10 | Server Design 0 = No (Default) 1 = Yes | 0 |
| 9 | Client Design 0 = No 1 = Yes (Default) | 1 |
| 8 | OEM Design 0 = Intel Adapter 1 = OEM Adapter | 1 |
| 7:5 | Reserved | 000 |
| 4 | Reserved | 0 |
| 3 | Reserved | 0 |
| 2 | PCI Bridge Device Present 0 = No 1 = Yes | 0 |
| 1:0 | Reserved | 00 |

## B.5 PBA Number (Words 08h - 09h)

A nine-digit printed board assembly (PBA) number used for Intel manufactured adapter cards is stored in a four-byte field. Other hardware manufacturers may use these fields for other purposes. The network driver should not rely on this field to identify the product or its capabilities.

## B.6 Initialization Control Word 1 (Word 0Ah)

This is the first word read by the controller that contains initialization values to:

Set default values for some internal registers

Enable and disable specific features

Determine which PCI configuration space values will be loaded from the EEPROM

**Table 21. Initialization Control Word 1 (Word 0Ah)**

| Bit | Name | Description |
|---|---|---|
| 15:14 | Signature | The Signature field contains a signature of 01b indicating a valid EEPROM. If this field contains a value other than 01b, the EEPROM is invalid and the values in the EEPROM are not read. Therefore, default values are used for the configuration space IDs. |
| 13 | 64/32 BAR | This bit indicates whether the device is using 32-bit or 64-bit memory mapping.<br>0 = 64-bit memory mapping (default)<br>1 = 32-bit memory mapping |
| 12 | Reserved | Reserved. Set to 0 |
| 11 | Reserved | Reserved. Set to 0 |
| 10 | Reserved | Reserved. Set to 1 |
| 9 | Reserved | Reserved. Set to 0 |
| 8 | Reserved | Reserved. Set to 0 |
| 7 | Internal VREG Power down Control | This bit is used to define usage of internal 1.2V and 1.8V regulators to supply power<br>0 = Yes (Default)<br>1 = No (external regulators are being used) |
| 6:4 | Reserved | Reserved. Set to 0 |
| 3 | Reserved | Reserved. Set to 1 |
| 2 | Reserved | Reserved. Set to 0 |
| 1 | Subsystem and Subsystem Vendor ID | This bit indicates whether or not to load the Subsystem ID and Subsystem Vendor ID from the EEPROM.<br>0 = Do not load the Subsystem and subsystem vendor ID from the EEPROM<br>1 = Load the Subsystem and subsystem vendor ID from the EEPROM (Default) |
| 0 | PCI Device and Vendor ID | This bit indicates whether or not to load the Vendor ID and Device ID from the EEPROM<br>0 = Do not load the Vendor ID from the EEPROM<br>1 = Load the Vendor ID from the EEPROM (Default |

## B.7 Identification Words (Words 0Bh - 0Eh)

These words contain the Subsystem ID, Subsystem Vendor ID, Device ID, and Vendor ID. The table below is an example of settings for the 82541ER..

**Table 22. Identification Words**

| Vendor ID | Device ID | Subsystem Vendor ID | Subsystem ID | Comments |
|---|---|---|---|---|
| 8086 | 1078 | 8086 | 1078 | **82541ER LOM.** Default value if EEPROM not present |

**NOTE:** The values in this table are hexadecimal.

### B.7.1 Subsystem ID (Word 0Bh)

If the Signature bits (15:14) and Load Subsystem IDs bit (1) in word 0Ah are valid, this word will be read in to initialize the Subsystem ID.

### B.7.2 Subsystem Vendor ID (Word 0Ch)

If the Signature bits (15:14) and Load Subsystem IDs bit (1) of word 0Ah are valid, this word will be read in to initialize the Subsystem Vendor ID.

### B.7.3 Device ID (Word 0Dh)

If the Signature bits (15:14) and Load Vendor/Device IDs bit (0) of EEPROM word 0Ah are valid, this word will be read in to initialize the Device ID.

### B.7.4 Vendor ID (Word 0Eh)

If the Signature bits (15:14) and Load Vendor/Device IDs bit (0) of EEPROM word 0Ah are valid, this word will be read in to initialize the Device ID.

## B.8 Initialization Control Word 2 (Word 0Fh)

This is the second word read by the controller and contains additional initialization values to:

- Set defaults for some internal registers
- Enable and disable specific features

### Table 23. Initialization Control Word 2 (Word 0Fh)

| Bit | Name | Description |
|---|---|---|
| 15 | APM PME# Enable | This bit is the initial value of the Assert PME on APM Wake Up bit in the Wake Up Control Register (WUC.APMPME). It is typically set to 1 for Intel LAN adapters. |
| 14 | ASDE | This bit reflects the initial value of the Auto-Speed Detection Enable bit of the Device Control Register (CTRL). The hardware default value is 0 (the PHY tells MAC the speed). |
| 13:12 | Pause Capability | This bit reflects the pause capability for the advertised configuration base page and is mapped to TXCW[8:7]. |
| 11 | Reserved | Reserved. Set to 0 |
| 10:9 | Flash Size | This field indicates the Flash size:<br>00 = 64 Kbytes (hardware default)<br>01 = 128 Kbytes<br>10 = 256 Kbytes<br>11 = 512 Kbytes<br>These bits impact the requested memory space for the Flash and Expansion ROM BARs in the PCI configuration space. |
| 8 | MAC Clock Speed (82541EI) | When programmed to 0, MAC runs at full speed.<br>When set as 1, MAC runs at 1/4 speed on any drop from 1000 mb/s. |
| 7 | Reserved | Reserved. Set to 1. |
| 6:3 | Reserved | Reserved. Set to 0. |
| 2 | Reserved | Reserved. Set to 1. |
| 1 | Force CSR Read Split | Used to force all device control/status register-reads to be split when operating in a PCI-X environment. When set to 0 (default), certain critical registers are decoded for non-split access. |
| 0 | Reserved | Set to 0. |

**NOTE:** Values in this table are hexadecimal

## B.9 EEPROM Size (word 12h)

This word is only applicable to SPI EEPROMS which are typically need for manageability applications. Unused bits are reserved and should be programmed to 0. Bits 8:0 are reserved. See the table below:.

### Table 24. SPI EEPROM Size

| Bits 12:10 | Bit 9 | EEPROM Size (Bits) | EEPROM Size (Bytes) |
|---|---|---|---|
| 000 | 0 | 1Kbit | 128byte |
| 001 | 1 | 4Kbit | 512byte |
| 010 | 1 | 8Kbit | 1Kbyte |
| 011 | 1 | 16Kbit | 2Kbyte |
| 100 | 1 | 32Kbit | 4Kbyte |

### Table 24. SPI EEPROM Size

| Bits 12:10 | Bit 9 | EEPROM Size (Bits) | EEPROM Size (Bytes) |
|---|---|---|---|
| 101 | 1 | 64Kbit | 8Kbyte |
| 110 | 1 | 128Kbit | 16Kbyte |
| 111 | 1 | Reserved | Reserved |

## B.10 Software Defined Pins Control (word 20h)

| Bit | Name | Description |
|---|---|---|
| 15 | SDPDIR[3] | **SDP3 Pin - Initial Direction.** This bit configures the initial HW value of the SDP3_IODIR bit in the Extended Device Control Register (CTRL_EXT) following powerup.<br>0 = In; 1 = Out |
| 14 | SDPDIR[2] | **SDP2 Pin - Initial Direction.** This bit configures the initial HW value of the SDP2_IODIR bit in the Extended Device Control Register (CTRL_EXT) following powerup.<br>0 = In; 1 = Out |
| 13:10 | Reserved | **Reserved.** Set to 0 |
| 9 | SDPDIR[1] | **SDP1 Pin - Initial Direction.** This bit configures the initial HW value of the SDP1_IODIR bit in the Device Control Register (CTRL) following powerup.<br>0 = In; 1 = Out |
| 8 | SDPDIR[0] | **SDP0 Pin - Initial Direction.** This bit configures the initial HW value of the SDP0_IODIR bit in the Device Control Register (CTRL) following powerup.<br>0 = In; 1 = Out |
| 7 | SDPVAL[3] | **SDP3 Pin - Initial Output Value.** This bit configures the initial power-on value output on SDP3 (when configured as an output) by configuring the initial HW value of the SDP3_DATA bit in the Extended Device Control Register (CTRL_EXT) after powerup. |
| 6 | SDPVAL[2] | **SDP2 Pin - Initial Output Value.** This bit configures the initial power-on value output on SDP2 (when configured as an output) by configuring the initial HW value of the SDP2_DATA bit in the Extended Device Control Register (CTRL_EXT) after powerup. |
| 5:4 | Reserved | **Reserved.** Set to 0 |
| 3 | EN_PHY_PWR_MGMT | Configures the initial HW default value of this bit in the Device Control Register (CTRL) following powerup. |
| 2 | D3_COLD_WAKEUP_ADV_EN | Configures the initial HW default value of the ADVD3WUC bit in the Device Control Register (CTRL) following powerup. |
| 1 | SDPVAL[1] | **SDP1 Pin - Initial Output Value.** This bit configures the initial power-on value output on SDP1 (when configured as an output) by configuring the initial HW value of the SDP1_DATA bit in the Device Control Register (CTRL) after powerup. |
| 0 | SDPVAL[0] | **SDP0 Pin - Initial Output Value.** This bit configures the initial power-on value output on SDP0 (when configured as an output) by configuring the initial HW value of the SDP0_DATA bit in the Device Control Register (CTRL) after powerup. |

## B.11 D0 Power (word 22h high byte)

If the signature bits are valid and Power Management is not disabled, then the value in this field is used in the PCI Power Management Data Register when the Data_Select field of the Power Management Control/Status Register (PMCSR) is set to 0 or 4. It indicates the power usage and heat dissipation of the networking function (including the Ethernet controller and any other devices controlled by the chip in tenths of a watt. Example:

```
If Word 22 = 290E, POWER CONSUMPTION (in 1/10W, hex), then:

    bits 15:8 = 29h Power in D0a, 29h = 4.1W

    bits 7:0 = 0Eh Power in D3h, 0Eh = 1.4W
```

## B.12 D3 Power (word 22h low byte)

If the signature bits are valid and Power Management is not disabled, then the value in this field is used in the PCI Power Management Data Register when the Data_Select field of the Power Management Control/Status Register (PMCSR) is set to 3 or 7. Its indicates the power usage and heat dissipation of the networking function (including the Ethernet controller and any other devices controlled by the chip in tenths of a watt (see Section B.11).

## B.13 Initialization Control 3 (Word 24h)

The word controls general initialization values.

| 82541ER | | |
|---|---|---|
| **Bit** | **Name** | **Description** |
| 15:13 | Reserved | See configuration options in Appendix B.16 |
| 12 | PCI Interrupt | See configuration options in Appendix B.16 |
| 11 | Enable/Disable FLASH Logic | Set by IBA |
| 10 | Enable/Disable APM | See configuration options in Appendix B.16 |
| 9:8 | Reserved | See configuration options in Appendix B.16 |
| 7:0 | Reserved | See configuration options in Appendix B.16 |

## B.14 LED Configuration Defaults (Word 2Fh)

This EEPROM word specifies the hardware defaults for the LED Control Register (LEDCTL) fields controlling the LED0 (LINK_UP) and LED2 (LINK_100) output behaviors.

A value of 0602h configures the LED behavior to be equivalent to a LAN port based on the legacy 82544EI/GC controller.

**Table 25. LED Configuration (Word 0Fh)**

| Bit | Name | Description |
|---|---|---|
| 15 | LED2 Blink | This bit reflects the initial value of the LED2 blink field in the LED control register:<br>0 = Non-blinking<br>1 = Blinking |
| 14 | LED2 Invert | This bit reflects the initial value of the LED2 invert field in the LED control register:<br>0 = Do not invert output (active low)<br>1 = Invert output |
| 13:12 | Reserved | Reserved. Set to 0. |

**Table 25. LED Configuration (Word 0Fh)**

| Bit | Name | Description |
|---|---|---|
| 11:8 | LED2 Mode | This bit reflects the initial value of the LED2 mode field in the LED control register. It specifies which event, state, or pattern will be displayed on LED2 (LINK_100) output. For example, a value of 0111 indicates 1000 Mbps link operation. |
| 7 | LED0 Blink | This bit reflects the initial value of the LED0 blink field in the LED control register:<br>0 = Non-blinking<br>1 = Blinking |
| 6 | LED0 Invert | This bit reflects the initial value of the LED0 invert field in the LED control register:<br>0 = Do not invert output (active low)<br>1 = Invert output |
| 5:4 | Reserved | Reserved. Set to 0 |
| 3:0 | LED0 Mode | This bit reflects the initial value of the LED0 mode field in the LED control register. It specifies which event, state, or pattern will be displayed on LED0 (LINK_UP) output. For example, a value of 0010 indicates activity. |

## B.15 Checksum Word Calculation (Word 3Fh)

The Checksum word (3Fh) is calculated by adding all EEPROM words (00h - 3Fh), including the Checksum word itself. The sum should equal BABAh. The initial value in the 16-bit summing register should be 0000h, and the carry bit should be ignored after each addition. This checksum is not accessed by the controller device. If CRC checking is required, it must be performed by software.

## B.16 82541ER No Management and No Integrated Magnetics

```
0/8  1/9  2/A  3/B  4/C  5/D  6/E  7/F
FFFF FFFF FFFF 0300 FFFF 1000 FFFF FFFF
FFFF FFFF 640B 1078 8086 1078 8086 3284
20DD 5555 0000 2F90 3200 0012 1E20 0012
1E20 0012 1E20 0012 1E20 0009 0200 0000
000C 93A6 280B 0000 0800 FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF 0602
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
```

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