82547GI/82547EI Gigabit Ethernet Controller Specification Update

June 23, 2006

The 82547GI/82547EI Gigabit Ethernet Controller may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

CONTENTS **1**
PREFACE **4**
NOMENCLATURE **4**
COMPONENT IDENTIFICATION VIA PROGRAMMING INTERFACE **5**
GENERAL INFORMATION **5**
82547GI/82547EI Component Marking Information 5
SUMMARY TABLE OF CHANGES **6**
Codes Used in Summary Tables 6
SPECIFICATION CHANGES **8**
1. (Deleted) 8
ERRATA **9**
1. ASF Manageability Not Fully Functional 9
2. (Deleted) 9
3. (Deleted) 9
4. 1.2V Power Regulation 9
5. 1000BASE-T PHY Performance Problems 9
6. JTAG Boundary Scan 9
7. PEC Utilized Incorrectly When SMB Master 10
8. RMCP Responses Use Erroneous Sequence Number 10
9. ASF Push Messages 10
10. SMB Pass Through Mode 10
11. No Response to ASF ARP Requests 10
12. Crystal Oscillator Operation at High Temperature 11
13. PHY Link Stability Problem at 100 Mbps and 1000 Mbps 11
14. LAN Disable Not Signaled to Chipset 11
15. RMCP Remote Commands 11
16. Watchdog Expiration Does Not Enable RMCP and ARP Reception 11
17. Non-Compliant 100BASE-TX Hubs 12
18. VLAN Filtering 12
19. Multicast Filtering 12
20. Software Reset Initiated by I/O Cycle 12
21. LAN Manageability Packets with Don’t Fragment Flag Set 12
22. Forced TCO Reset Not Functional 12
23. Non-Compliant Gigabit Scrambler Support 13
24. Microwire EEPROM Unusable for Manageability Applications 13
25. LAN Disable Floats Voltage Regulator Control Outputs 13
26. Marginal Internal Power on Reset Function 13
27. Transmit Amplitude 13
28. PHY Write Command Incorrectly Writes to MAC Registers 14
29. No Link with Forced 100 Mbps Partner if 10 Mbps Link Up Feature Selected 14
30. Excessive Gigabit Link Time 15

31. Smart Speed Does Not Transition to 100 Mbps 15
32. Partner Assumed Full Duplex when Shifting from 1000 Mbps to 100 Mbps 15
33. Transmit Stop in High Collision Environment 15
34. PHY Write Mechanism Supercedes EEPROM LED1/ACT# Configuration 16
35. Long Link Time to Busy 100BASE-TX Hub 16
36. SMB ARP Get UDID Commands 17
37. DHCP Not Supported 17
38. Watchdog Initialization upon Exiting Reset 17
39. PET Transient Event Processing During LAN Link Down 17
40. I2C Short Transactions Not Supported for Address C8h 17
41. MDI-X Operation 17
42. Software Resets Do Not Cause Status Change in TCO Mode 18
43. Security Key Synchronization Error 18
44. Initial TCO Resets Do Not Succeed 18
45. First SMB Transaction after System Power-Up is NACK'ed 18
46. 1000 Mbps Slave Link failures With High Jitter Link Partners and Short Cables 19

SPECIFICATION CLARIFICATION 20

1. Substrate Suppliers Migrating to a Thinner Substrate 20
2. External Oscillator Support Clarification 20
3. Resistor Value Changes for 82547GI Stepping 20

DOCUMENTATION CHANGES 21

1. (Deleted) 21
2. (Deleted) 21
3. (Deleted) 21
4. (Deleted) 21
5. (Deleted) 21
6. (Deleted) 21
7. (Deleted) 21

REVISION HISTORY

82547GI/82547EI Gigabit Ethernet Controller Specification Update

October 13, 2004	**Initial Public Release.**
June 23, 2006	**Added Specification Clarification #2 and #3.**

PREFACE

This document is an update to published specifications. Specification documents for this product include:

- 82547GI/82547EI Gigabit Ethernet Controller Datasheet.
- 82562EZ(EX) & 82547GI(EI) Dual Footprint Design Guide Application Note (AP-440)
- 82541GI(EI) & 82547GI(EI) EEPROM Map and Programming Information Guide (AP-446)

This document is intended for hardware system manufacturers and software developers of applications, operating systems or tools. It may contain Specification Changes, Errata, and Specification Clarifications.

All 82547GI/82547EI product documents are subject to revision. Be sure you have the latest information before finalizing your design.

NOMENCLATURE

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

COMPONENT IDENTIFICATION VIA PROGRAMMING INTERFACE

82547GI/82547EI controller steppings can be identified by the following register contents:

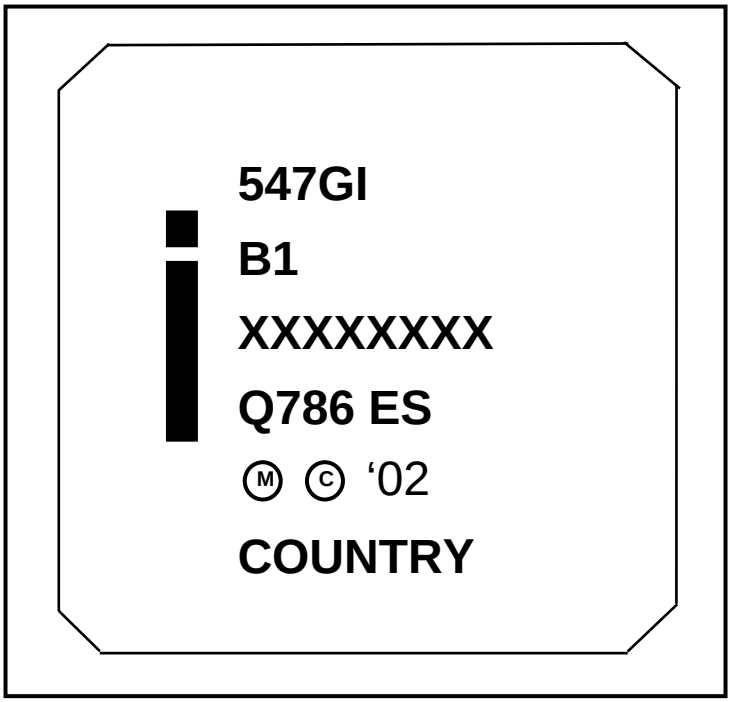
Stepping	Vendor ID	Device ID	Revision Number
82547EI A0	8086h	1019h	00h
82547EI A1	8086h	1019h	01h
82547EI B0	8086h	1019h	00h
82547GI B1	8086h	1075h	00h

GENERAL INFORMATION

This section covers the 82547GI and 82547EI devices.

82547GI/82547EI COMPONENT MARKING INFORMATION

Product	Stepping	QDF Number	Top Marking	Notes
82547EI	A0	Q 520	547EI	Engineering Samples
82547EI	A1	Q777	547EI	Engineering Samples
82547EI	B0	Q779	547EI	Engineering Samples
82547EI	B0		82547EI	Production Units
82547GI	B1	Q786	547EI or 547GI	Engineering Samples
82547GI	B1		547GI	Production Units



SUMMARY TABLE OF CHANGES

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82547GI/82547EI steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLES

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

No.	EI A0	EI A1	EI B0	GI B1	Plans	SPECIFICATION CHANGES	Page	Notes
1						(Deleted)	8	
No.	**EI A0**	**EI A1**	**EI B0**	**GI B1**	**Plans**	**ERRATA**	**Page**	**Notes**
1	X	X			Fixed	ASF Manageability Not Fully Functional	9	
2						(Deleted)	9	
3						(Deleted)	9	
4	X				Fixed	1.2V Power Regulation	9	
5	X	X			Fixed	1000BASE-T PHY Performance Problems	9	
6	X	X			Fixed	JTAG Boundary Scan	9	
7	X	X	X		Fixed	PEC Utilized Incorrectly When SMBus Master	10	
8	X				Fixed	RMCP Responses Use Erroneous Sequence Number	10	
9	X				Fixed	ASF Push Messages	10	
10	X				Fixed	SMBus Pass Through Mode	10	
11	X				Fixed	No Response to ASF ARP Requests	10	
12	X				Fixed	Crystal Oscillator Operation at High Temperature	11	
13	X				Fixed	PHY Link Stability Problem at 100 and 1000 Mb/s	11	
14	X	X			Fixed	LAN Disable Not Signaled to Chipset	11	
15	X				Fixed	RMCP Remote Commands	11	
16	X	X			Fixed	Watchdog Expiration Does Not Enable RMCP and ARP Reception	11	
17	X	X			Fixed	Non-Compliant 100BASE-TX Hubs	12	
18	X	X			Fixed	VLAN Filtering	12	
19	X	X			Fixed	Multicast Filtering	12	
20	X	X			Fixed	Software Reset Initiated by I/O Cycle	12	
21	X				Fixed	LAN Manageability Packets with Don't Fragment Flag Set	12	
22	X	X			Fixed	Forced TCO Reset Not Functional	12	
23	X	X			Fixed	Non-Compliant Gigabit Scrambler Support	13	
24	X	X	X		Fixed	Microwire* EEPROM Unusable for Manageability Applications	13	
25	X	X			Fixed	LAN Disable Floats Voltage Regulator Control Outputs	13	
26	X	X	X	X	NoFix	Marginal Internal Power On Reset Function	13	

No.	EI A0	EI A1	EI B0	GI B1	Plans	ERRATA	Page	Notes
27	X	X			Fixed	Transmit Amplitude	13	
28			X		Fixed	PHY Write Command Incorrectly Writes to MAC Registers	14	
29			X		Fixed	No Link with Forced 100Mb Partner if 10Mb Link Up Feature Selected	14	
30	X	X	X		Fixed	Excessive Gigabit Link Time	15	
31			X		Fixed	Smart Speed Does Not Transition to 100Mb	15	
32	X	X	X	X	NoFix	Partner Assumed Full Duplex when Shifting from 1000 Mbps to 100 Mbps	15	
33	X	X	X		Fixed	Transmit Stop in High Collision Environment	15	
34			X		Fixed	PHY Write Mechanism Supercedes EEPROM LED1/ACT# Configuration	16	
35	X	X	X		Fixed	Long Link Time to Busy 100BASE-TX Hub	16	
36	X	X	X		Fixed	SMBus ARP Get UDID Commands	17	
37	X	X	X	X	NoFix	DHCP Not Supported	17	
38	X	X	X		Fixed	Watchdog Initialization Upon Exiting Reset	17	
39	X	X	X	X	NoFix	PET Transient Event Processing During LAN Link Down	17	
40	X	X	X	X	NoFix	I2C Short Transactions Not Supported for Address C8h	17	
41	X	X	X		Fixed	MDI-X Operation	17	
42	X	X	X		Fixed	Software Resets Do Not Cause Status Change in TCO Mode	18	
43	X	X	X		Fixed	Security Key Synchronization Error	18	
44	X	X	X		Fixed	Initial TCO Resets Do Not Succeed	18	
45	X	X	X	X	NoFix	First SMB Transaction after System Power-Up is NACK'ed	18	
46	X	X	X	X	NoFix	1000 Mbps Slave Link failures With High Jitter Link Partners and Short Cables	18	
No.	**EI A0**	**EI A1**	**EI B0**	**GI B1**	**Plans**	**SPECIFICATION CLARIFICATIONS**	**Page**	**Notes**
1	X	X	X	X	Fixed	Substrate Supplier's Migrating to a Thinner Substrate	22	
2	X	X	X	X	Fixed	External Oscillator Support Clarification	22	New
3				X	Fixed	Resistor Value Changes for 82547GI Stepping	22	New
No.	**EI A0**	**EI A1**	**EI B0**	**GI B1**	**Plans**	**DOCUMENTATION CHANGES**	**Page**	**Notes**
1						(Deleted)	21	
2						(Deleted)	21	
3						(Deleted)	21	
4						(Deleted)	21	
5						(Deleted)	21	
6						(Deleted)	21	
7						(Deleted)	21	

SPECIFICATION CHANGES

1. (Deleted)

ERRATA

1. ASF Manageability Not Fully Functional

Problem: The 82547 Gigabit Ethernet Controller does not exhibit full ASF 2.0 functionality.

Implication: Multiple features are affected. Implementing ASF manageability in customer systems with the A0 stepping is not fully supported.

Workaround: The 82547 controller provides a method to apply ASF firmware changes in the EEPROM. Application of these flexible firmware upgrades has been demonstrated to provide ASF 1.0 and legacy alerting capability.

These firmware patches require significant amounts of program memory, which results in the use of larger EEPROMs than expected. Intel required a minimum 8-Kbyte EEPROM size to support manageability during the early development cycle of the 82547 controller. (Non-manageability applications were not affected.)

Status: Intel resolved this erratum in the B0 stepping of the 82547EI Gigabit Ethernet Controller. The minimum EEPROM size to implement manageability is now 5 bytes. However, some implementations will need as much as 8 Kbytes to support future enhancements. Erratum 24, “Microwire EEPROM Unusable for Manageability Applications,” also applies.

2. (Deleted)

3. (Deleted)

4. 1.2V Power Regulation

Problem: The on-board power regulator control circuit used with an external PNP transistor does not have adequate internal grounds. As a result, it does not keep the 1.2V within its regulation band and the voltage may oscillate at a rate of approximately 200 KHz.

Implication: The PHY transmit and receive clocks may have excessive jitter, affecting overall PHY performance.

Workaround: Using a short wide trace from the CTRL_18 output to the PNP transistor is desirable. However, this technique is not completely effective.

Status: Intel resolved this erratum in the A1 stepping of the 82547 Gigabit Ethernet Controller.

5. 1000BASE-T PHY Performance Problems

Problem: The PHY exhibits several performance problems at 1000 Mbps:

- Link acquisition may be slow, taking more than 3.5 seconds.
- It may not be possible to achieve link with cables more than 80 meters long.
- Bit Error Rates may exceed 10^{-10}, failing IEEE 802.3 specifications.

These problems are caused by the DSP receive clock recovery unit being unable to lock properly and are related to erratum 16, “PHY Link Stability Problem at 100 and 1000 Mbps.”

Implication: The PHY will not be able to achieve link across the full range of operating conditions. Large numbers of receive data errors may occur as cable lengths increase, requiring data to be re-transmitted.

Workaround: Perform early evaluations with short cables, using slower (10/100 Mbps) data rates.

Status: Intel has partially resolved this erratum in the A1 stepping of the device and has fully resolved it in the B0 stepping of the 82547 Gigabit Ethernet Controller. However, erratum 31, “Excessive Gigabit Link Time,” should be considered.

6. JTAG Boundary Scan

Problem: The JTAG SAMPLE and EXTEST instructions do not correctly capture pin input data into the scan cells for all signals. On the 82547 device, many inputs are affected, including the PCI bus.

This erratum is caused by incorrect connections between the affected pad cells and boundary scan cells.

Implication: Boundary scan will not be able to capture signals asserted on all input pins by a functional tester during board tests.

Workaround: Use boundary scan with reduced functionality. The port declarations in the BSDL file reflect the reduced boundary scan functionality for each pin where applicable. For example, both the FL_SO and FL_SI pins are denoted as “out” (output) pins even though FL_SO is an input. This declaration will prevent a JTAG-based test program from scanning erroneous input data from the FL_SO pin.

Status: Intel resolved this erratum in the B0 stepping of the 82547 Gigabit Ethernet Controller. A new BSDL file reflects the full functionality.

7. PEC Utilized Incorrectly When SMB Master

Problem: When the 82547 controller is an SMB master device, it may calculate the Packet Error Correction (PEC) incorrectly, causing SMB master write transactions to send an incorrect PEC value. In addition, SMB master read transactions may disregard the received PEC value during operations such as ASF sensor polling.

Implication: When the 82547 controller acts as an SMB master device, it may calculate the Packet Error Correction (PEC) incorrectly, causing SMB master write transactions to send an incorrect PEC value. In addition, SMB master read transactions may disregard the received PEC value during operations such as ASF sensor polling.

Workaround: Currently, there are no workarounds for this anomaly.

Status: This has been partially corrected in the B0 stepping of the 82547 controller and fully corrected in the B1 stepping (82547GI) of the 82547 controller.

8. RMCP Responses Use Erroneous Sequence Number

Problem: Remote Management Control Protocol (RMCP) responses should return a sequence number from ASF register F4h. Instead, responses will return the sequence number found in the request packet.

Implication: This problem impairs the ASF manageability packet security mechanism for RMCP. Thus, the 82547 controller’s RMCP responses may be rejected. This occurs only in ASF 2.0.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the A1 stepping of the 82547 Gigabit Ethernet Controller.

9. ASF Push Messages

Problem: ASF only supports a single push request. The queue for multiple push requests was not correctly implemented.

Implication: The ASF subsystem sends push requests multiple times over a one-minute period. During this time, no other push requests can be issued.

Workaround: There are no workarounds for this anomaly.

Status: This has been resolved in the A1 stepping of the 82547 Gigabit Ethernet Controller.

10. SMB Pass Through Mode

Problem: SMB pass through mode is not functional. Specific pass through mode functions affected include: SMB ARP, alert responses, manageability ARP response, and receive enable status report. The problem occurs because pass through mode uses registers that are cleared at startup.

Implication: In a multiple SMB slave environment such as IPMI, the SMB alert functionality will not be functional. This problem affects ASF 2.0 operation.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the A1 stepping of the 82547 Gigabit Ethernet Controller.

11. No Response to ASF ARP Requests

Problem: The Address Resolution Protocol (ARP) filter in the manageability block incorrectly resets. This action causes the 82547 to ignore ASF ARP requests. Responses are not sent back to the network.

Implication: Routers on the network commonly send ARP requests. When ARP requests are not acknowledged, these routers may have difficulty locating 82547-based manageability devices on the network.

Workaround: A firmware patch is available for the A1 stepping.

Status: Intel resolved this erratum in the A1 stepping of the 82547 Gigabit Ethernet Controller.

12. Crystal Oscillator Operation at High Temperature

Problem: The crystal oscillator may stop at case temperatures higher than 70° C. The failure is due to higher than expected XTAL1/XTAL2 pad leakage in conjunction with the high resistance of the internal feedback resistor.

Implication: If the 82547 oscillator fails, internal clocks will not run and the device will not operate.

Workaround: Connect a resistor of approximately 500 KΩ value from XTAL1 to XTAL2. The exact value of the resistor is not critical. In other words, a 470 KΩ or 510KΩ resistor may be used. The parallel combination of the internal feedback resistor and the external resistor will be low enough to ensure oscillation.

Status: Intel resolved this erratum in the A1 stepping of the 82547 Gigabit Ethernet Controller.

13. PHY Link Stability Problem at 100 Mbps and 1000 Mbps

Problem: The 82547 controller may occasionally lose and re-acquire link. This problem is caused by the DSP receive clock recovery unit being unable to lock properly. The problem is related to erratum 6, “1000BASE-T PHY Performance Problems.”

Implication: The PHY will not be able to maintain link across the full range of operating conditions. Due to the instability, the receiver may drop some packets. The missing packets will be indicated in appropriate statistics registers.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the A1 stepping of the 82547 Gigabit Ethernet Controller. However, erratum 30, “Excessive Gigabit Link Time,” should be looked at.

14. LAN Disable Not Signaled to Chipset

Problem: When the 82547 controller is disabled through the FL_SO/LAN_DISABLE# pin, the device de-activates as intended. However, it does not signal this condition back to the MCH device by setting the CI_9 signal on the CSA port.

Implication: Shortly after the 82547 controller enters the disabled state, the system BIOS attempts to configure the LAN controller (typically, as device 3). The controller is no longer able to respond on the CSA port, and the system may hang.

Workaround: None.

Status: Intel resolved this erratum in the B0 stepping of the 82547EI Gigabit Ethernet Controller.

15. RMCP Remote Commands

Problem: The manageability module will send incorrect remote commands over the SMB for legacy device descriptors with non-zero status values.

The RMCP remote command (power up, power down, power cycle and reset) for a legacy device consists of an SMB read byte transaction followed by an SMB write byte transaction. The write data is supposed to consist of the read data OR-ed with a command mask. The problem is that the manageability module sends the command mask instead.

Implication: If the legacy device has a non-zero status value, the remote command associated with the data will be incorrect. This means that older sensors may be handled incorrectly under ASF 1.0 and 2.0.

Workaround: There are no workarounds for this erratum.

Status: Intel resolved this erratum in the A1 stepping of the 82547 Gigabit Ethernet Controller.

16. Watchdog Expiration Does Not Enable RMCP and ARP Reception

Problem: Watchdog expiration should cause the manageability module to enable receiving all incoming Remote Management Control Protocol (RMCP) and Address Resolution Protocol (ARP), regardless of whether it was enabled before the watchdog expired. Instead, the enabled/disabled condition does not change.

Implication: If the system was not configured to receive or respond to RMCP commands and ARP requests prior to watchdog expiration, watchdog expiration will not enable those activities. If the system ignores an important RMCP command, it may not be able to recover from the condition that led to the watchdog expiration.

Workaround: Always leave ARP and RMCP reception enabled. ASF firmware patches work around this erratum successfully.

Status: Intel resolved this erratum in the B0 stepping of the 82547 Gigabit Ethernet Controller.

17. Non-Compliant 100BASE-TX Hubs

Problem: If Auto-Negotiation is enabled, the 82547 PHY will not establish link with certain 100BASE-TX hubs that transmit unscrambled idles when their receivers are idle. The PHY does not support unscrambled idles causing parallel detection to fail.

Implication: The 82547 device will not achieve link with some legacy 100 Mbps hubs (for example, a Bay Networks hub). No problem occurs for hubs that transmit scrambled idles unconditionally.

Workaround: For non-compliant hubs, force link by setting PHY register 0 to 2100h.

Status: Intel resolved this erratum in the B0 stepping of the 82547 Gigabit Ethernet Controller.

18. VLAN Filtering

Problem: VLAN packets (register bit RCTL.VFE) do not pass the packet filter because of a problem with the memory that stores the filter table values.

Implication: VLAN packets will not be received from the network. Exact filters are not affected. This erratum is closely related to erratum 21, “Multicast Filtering.”

Workaround: There is no workaround for the VLAN Filtering erratum.

Status: Intel resolved this erratum in the B0 stepping of the 82547 Gigabit Ethernet Controller.

19. Multicast Filtering

Problem: Multicast packets (register bit RCTL.MPE) do not pass the packet filter due to a problem with the memory that stores the filter table values.

Implication: Multicast packets will not be received from the network. Exact filters are not affected. This erratum is closely related to erratum 18, “VLAN Filtering.”

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the B0 stepping of the 82547 Gigabit Ethernet Controller.

20. Software Reset Initiated by I/O Cycle

Problem: The 82547EI does not respond with completion to an I/O cycle issued for a software reset. The primary software that uses an I/O cycle reset is the Intel Boot Agent.

Implication: This erratum can cause a system to hang.

Workaround: Intel has an updated version of the Boot Agent firmware that prevents this problem.

Status: Intel resolved this erratum in the B0 stepping of the 82547EI Gigabit Ethernet Controller.

21. LAN Manageability Packets with Don’t Fragment Flag Set

Problem: If an incoming packet is received and the Don’t Fragment Flag is set in the IP header (4000h), the packet will be discarded. This problem only affects manageability packets.

Implication: Manageability packets are unnecessarily discarded.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the A1 stepping of the 82547 Gigabit Ethernet Controller.

22. Forced TCO Reset Not Functional

Problem: TCO packets have the ability to force reset to the controller. If reset is forced in this way, the TCO controller will start reading from the EEPROM before the reset is completed.

Implication: TCO control registers will be corrupted, and the manageability block will no longer be able to send or receive packets.

Workaround: The Device Reset upon Force TCO Command should be disabled through the EEPROM. This is accomplished by programming bit 2 of word 23h to 0.

Status: Intel resolved this erratum in the B0 stepping of the 82547 Gigabit Ethernet Controller.

23. Non-Compliant Gigabit Scrambler Support

Problem: The PHY fails to communicate with a non-compliant gigabit scrambler in a gigabit link partner due to a DSP timing problem. This capability is enabled in PHY register 18, bit 9.

Implication: An early gigabit PHY incorrectly implemented the Channel C scrambler polynomial in the Physical Coding Sub-layer. If the 82547 controller encounters this PHY as a link partner, the controller is unable to adapt to the incorrect coding and obtain link.

Workaround: A short cable should be used to avoid this anomaly.

Status: Intel resolved this erratum in the B0 stepping of the 82547 Gigabit Ethernet Controller.

24. Microwire EEPROM Unusable for Manageability Applications

Problem: The manageability firmware cannot access Microwire EEPROMs. This problem is not specific to any particular alerting activity.

Another erratum prevented the manageability hardware block from accessing the EEPROM and was capable of causing system lockups. However, that erratum was corrected in the 82547 controller B0 stepping.

Implication: Manageability firmware cannot read or write Microwire EEPROMs.

Workaround: An SPI* EEPROM should be used in all systems with ASF 1.0 or ASF 2.0 alerting. Microwire EEPROMs may be used in non-alerting applications. The SMB should be disabled by programming EEPROM word 23h, bit 0.

Status: Intel resolved this erratum in the 82547 B1 step (82547GI) Gigabit Ethernet Controller.

25. LAN Disable Floats Voltage Regulator Control Outputs

Problem: The LAN_DISABLE# pin is sampled during reset. When the controller is disabled, it floats the CTRL_12 and CTRL_18 regulator control outputs and the external PNP transistors will not be biased correctly across their collector-base junctions.

Implication: Regulation will not occur and the 1.2V and 1.8V supply rails will move toward 3.3V. However, minimal current will flow because the controller is disabled. Systems that do not use the internal voltage regulator controls are not affected.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the B0 stepping of the 82547 Gigabit Ethernet Controller.

26. Marginal Internal Power on Reset Function

Problem: Power on (internal) reset is not dependable in the event of a slow power ramp. If the 3.3V supply ramps slowly, the 1.2V supply (from the collector of the external PNP pass transistor) may not be stable when reset occurs. Voltage thresholds are not within design targets.

Implication: Internal power on reset is an alternative to using the LAN_PWR_GOOD input. To enable power on reset, LAN_PWR_GOOD must be connected to 3.3V through a pull-up resistor. For this configuration, a power ramp specification **must** be imposed and that the 3.3V supply ramps from its 10% point to its 90% point in less than 15 ms. this requirement is more restrictive than the general recommendation that all power supplies should ramp to within their regulation bands in less than 20 ms.

Workaround: The LAN_PWR_GOOD signal should be connected to the system's voltage supervisor function. Using LAN_PWR_GOOD as the external reset input is the preferred method.

Status: Intel does not intend to resolve this erratum in the 82547 Gigabit Ethernet controller family.

27. Transmit Amplitude

Problem: Some electrical parameters of the 82547 controller are trimmed as the devices are being tested. One of the parameters trimmed is the differential output amplitude. The IEEE specifications for this parameter are:

- 1000BASE-T specification: 670 mV – 920 mV
- 100BASE-TX specification: 950 mV – 1050 mV
- 10BASE-T specification: 2.2 V – 2.8 V

Due to a test program error, A0 and A1 device trimming made the PHY differential output amplitude low. Observed amplitudes were as follows:

- 1000BASE-T: ~710 mV
- 100BASE-TX: ~900 mV
- 10BASE-T: ~2.2V

The test program was improved during B0 manufacturing validation. For B0 engineering samples, device trimming made the PHY differential output amplitude high. Observed amplitudes were as follows:

- 1000BASE-T : ~850 mV
- 100Base-TX: ~1120 mV
- 10BASE-T: near the middle of the specification range

The test program was fully calibrated for B0 production. B0 production devices are trimmed and tested so that output amplitudes are distributed near the middle of all three specification ranges.

Implication: Systems built with A0, A1and B0 sample devices may not pass IEEE PHY conformance tests for 10/100 Mbps operation. Link acquisition should not be significantly affected.

Note: Other A0 and A1 PHY problems could also affect IEEE conformance tests.

Workaround: There are no workarounds for this erratum.

Status: Intel resolved this erratum in the production test program used for the 82547 device B0 stepping.

28. PHY Write Command Incorrectly Writes to MAC Registers

Problem: The B0 stepping contains a mechanism to alter internal PHY configuration registers from EEPROM settings. If the PHY has been processing data and a PHY write is invoked, the logic can become confused and write MAC registers instead.

Implication: The PHY must be preconditioned by reset just prior to PHY write commands. Certain reset situations will require special attention because they do not automatically reset the PHY:

- Forced TCO resets. A device reset may be requested before sending out manageability packets for system hangs.
- Global software resets of the Ethernet controller.

Other types of resets (for example, LAN_PWR_GOOD and PCI Reset) automatically reset the PHY.

Workaround: To perform global resets, software should first reset the PHY by writing a 1 to bit 15 in the PHY Control Register (Address 00). After a fresh PHY reset, the state logic will not become confused.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping).

29. No Link with Forced 100 Mbps Partner if 10 Mbps Link Up Feature Selected

Problem: If the EEPROM is programmed to the power-on link up mode and advertises 10 Mbps only, the Ethernet controller will not link with a partner that is forced to 100 Mbps. This behavior occurs because the PHY inherently does not attempt parallel detection to a partner at the unadvertised speed.

Implication: The low power link up function was added on the B0 stepping. The 10 Mbps EEPROM setting will not result in reliable link at 100 Mbps.

Workaround: The Advertise 10 Mbps and Link Up function should be disabled by programming EEPROM register 21h bit 3 to 0.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping).

30. Excessive Gigabit Link Time

Problem: Time for circuits to obtain lock is intermittently longer than the three second IEEE specification when connected to a gigabit link partner. Link time variability increases as cable lengths approach 100-meter specification cable. However, testing has demonstrated instances of exceeding the 3-second limit with shorter cable lengths.

Excessive link time can occur when link is established or re-established, including power-up, driver load, some power state changes, and PROSet configuration changes. If the first link attempt fails, subsequent link attempts can take between 2.5 and 3 seconds to complete. With longer cable lengths, over two attempts have been observed.

Implication: As the system boots and the driver initializes, the Ethernet controller is required to re-negotiate link. Excessive link time could delay network availability for mapping resources such as network drives.

When the system returns from a suspend state (S3 or S5 transitions to S0), the Ethernet controller is required to re-negotiate link. If the link time is longer than the time it takes to return from the power managed state, network access will not occur until link completes. At longer cable lengths the link speed is also subject to change after power managed states if convergence does not occur after four negotiation attempts.

When PROSet changes are made, the Ethernet controller is required to re-negotiate link. If link time is longer than the time to return from the PROSet dialog box network access will be delayed until link is re-established.

Workaround: The PHY should be adjusted through special EEPROM settings provided by Intel.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping), allowing driver patches to be removed and freeing up EEPROM capability. As expected, some EEPROM adjustments are still used to optimize the PHY receive path for particular board configurations.

31. Smart Speed Does Not Transition to 100 Mbps

Problem: When the PHY is configured to automatically assume master/slave status in gigabit mode, the smart speed function does not downshift to 100 Mbps.

Implication: Smart speed will not function without additional configuration.

Workaround: The workaround for the 82547 B0 stepping consists of forcing the PHY to Slave Mode with the EEPROM-based PHY write mechanism. The software driver will change to detect the situation where both link partners are slaves. If a slave-to-slave conflict exists, the driver toggles the mode to attempt gigabit link.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping).

32. Partner Assumed Full Duplex when Shifting from 1000 Mbps to 100 Mbps

Problem: For a link partner that advertises 1000BASE-T full duplex and 100BASE-TX half duplex capabilities, the 82547 controller will attempt to link at 1000 Mbps, followed by 100 Mbps. However, it will assume the link partner is capable of full duplex operation at both speeds.

Implication: If the advertisement is correct, a problem could occur obtaining link. Practical Gigabit Ethernet devices are by default capable of full duplex operation. Thus, the possibility of this advertisement is very low.

Workaround: There is no workaround for this erratum.

Status: Intel does not intend to resolve this erratum in the 82547 Gigabit Ethernet controller family.

33. Transmit Stop in High Collision Environment

Problem: When the 82547EI controller is configured for 10 Mbps or 100 Mbps half duplex operation, the device will discard packets when the maximum collision discard threshold is reached. When a packet is discarded **and** the data in that packet wraps around in the transmit FIFO, the next packet address can be miscalculated. If an invalid next packet address is used upon the discard event, then the MAC DMA controller will lose track of FIFO pointers and become locked.

Implication: When the controller is connected to a hub and encounters collisions, it will attempt to re-send packets. If 16 successive collisions occur when attempting to transmit a particular packet, that packet is discarded (according to the IEEE specification). The controller only manifests the transmit lock-up problem when the packet is discarded.

Workaround: Intel modified the driver software, including workarounds for TCP segmentation (“Large Send”) offloading and the Intel Boot Agent. This problem only affects the 82547EI controller.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping), allowing the software workaround to be removed. The silicon change results in a packet buffer granularity of 2 Kbytes and restricts packet size to 2 Kbytes in half duplex operation.

34. PHY Write Mechanism Supercedes EEPROM LED1/ACT# Configuration

Problem: The 82547 B0 stepping added a feature to make LED1/ACT# programmable from the EEPROM in the same manner as LED0 and LED2. LED settings are loaded from the EEPROM upon reset (RST#, LAN_PWR_GOOD, or software global reset). The settings are contained in word 21h bits 15:8. However, the PHY write mechanism used to work around the Gigabit Link Time and Smart Speed problems must be turned on by setting word 21h bits 10 and 8 to 1b. This configuration defeats many of the possible LED modes, including ACTIVITY# (mode = 0011b). Some of the other LED modes, for example LINK_10# (mode = 0101b) and LINK_1000 (mode = 0111b) are still possible.

Implication: LED1 is typically used as the ACTIVITY# LED. When the PHY write mechanism is used, ACTIVITY# EEPROM programmability is not available on LED1. If LED1 is wired up as ACTIVITY#, it will not be functional until the driver loads and programs the LED control register (LEDCTL) at offset 0E00h from the register base address.

Workaround: The system BIOS can write a copy of the desired EEPROM LED configurations to the LEDCTL register immediately after PCI enumeration. For example, writing binary 0000 0111 XXXX XXXX 1000 0011 XXXX XXXX to register offset 0E00h will program LED3 to be LINK1000# (mode = 0111b) and LED1 to be ACTIVITY# (mode = 0011b), with ACTIVITY# blinking (bit 15 = 1). This operation allows these LEDs to function in the interval before the software driver loads.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping). The PHY write mechanism now uses different EEPROM bits that do not conflict with LED programming.

35. Long Link Time to Busy 100BASE-TX Hub

Problem: At 100 Mbps, the 82547 controller may encounter a delay longer than 3 seconds to link when the LAN traffic consists of non-stop back-to-back packets. The problem occurs because the PCS scrambler is expects to receive idles to ensure correct DSP lock. The scrambler resets the PHY DSP when 3 µs has elapsed without idle pulses.

Implication: The problem occurs when the inter-packet gap (IPG) is minimal between packets over a lengthy period. In lab testing, the problem was seen on hubs with sustained utilization above 50%.

In a typical LAN, IPG is rarely at the minimum because:

- On half-duplex hubs, there are collisions causing back-off.
- Upon link to a full duplex switch, LAN traffic does not instantaneously increase.
- Traffic consists of bursts since network protocols typically wait for acknowledgement.

If link is forced (speed and duplex) through the driver setup, the problem does not occur. This problem is independent of cable length.

Workaround: Some improvement may be obtained by monitoring the PHY Parallel Detect Fault Bit with software. If the bit is set, software can alternately disable and enable DSP resets, pausing in an attempt to get link. This workaround has not been incorporated into the Intel software driver.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping).

36. SMB ARP Get UDID Commands

Problem: ARP is used on the SMB to reconcile address conflicts. The SMB specification defines the SMB ARP Get Unique Device ID commands (general and directed) to always return 1b in the reserved address field of byte 17 bit 0. The manageability block will always return zero in this bit.

Implication: The bit is stuck at 0b. Although this behavior does not meet SMB specifications, Intel has not observed any SMB agent to be sensitive to the value of this bit.

Workaround: If possible, firmware in the external manageability device should ignore the value of this bit on a Get UDID response.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping).

37. DHCP Not Supported

Problem: The management block DHCP function has problems renewing IP addresses at the end of the lease. Therefore, typically an IP address will not be renewed upon link restoration.

Implication: The manageability DHCP function is not supported. This issue primarily affects mobile ASF applications.

Workaround: An upgrade firmware patch will be available through Intel in the future.

Status: Intel does not plan to resolve this erratum in the 82547 Gigabit Ethernet controller family.

38. Watchdog Initialization upon Exiting Reset

Problem: After the de-assertion of reset, the controller reads initialization values from the EEPROM. However, the manageability watchdog timer counts down from its previous value and not from the value loaded from the EEPROM.

Implication: After system startup or return from power-down, the watchdog timer is subject to counting down from the default minimum value programmed by BIOS. Timer expirations could be premature relative to timer expirations based on the EEPROM value.

Workaround: There is no workaround for this issue.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping).

39. PET Transient Event Processing During LAN Link Down

Problem: The manageability block will send transient SOS alert events when the LAN link is down.

Implication: A transient event is defined as a change of state followed by a return to the original state. This behavior does not meet ASF specifications.

Workaround: There is no workaround for this issue.

Status: Intel does not plan to resolve this erratum in the 82547Gigabit Ethernet Controller family.

40. I2C Short Transactions Not Supported for Address C8h

Problem: In TCO mode, the manageability block will not support I2C short read block transactions for SMB address C8h.

Implication: This behavior is a manageability usage limitation. Other addresses are available.

Workaround: A firmware workaround patch may be possible.

Status: Intel does not plan to resolve this erratum in the 82547Gigabit Ethernet controller family.

41. MDI-X Operation

Problem: MDI-X is a PHY capability that allows it to switch data pairs if the wrong cable (in other words, straight cable versus cross-over cable) is used in a particular application. Under MDI-X configuration, pair A swaps with pair B and, for Gigabit, pair C swaps with pair D. MDI-X operation does not work correctly and is not supported.

Implication: A LAN port based on the 82547 controller can communicate with its link partner if the cable correctly connects transmitters and receivers or if the partner supports MDI-X. If the cabling is incorrect and the partner does not have MDI-X capability, link will not occur.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping).

42. Software Resets Do Not Cause Status Change in TCO Mode

Problem: Software resets involving the MAC (for example, Global Resets) do not cause the manageability block to send a status change to the BMC master device if one is present in the system. This problem is a manageability firmware erratum that affects compatibility with legacy 82559 operation.

Implication: The system could experience a loss of link without any notification to the BMC device.

Workaround: A firmware workaround patch exists and is available through your local Intel representative.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping). An upgraded firmware patch is still used.

43. Security Key Synchronization Error

Problem: RAKP1 security key retransmissions may overwrite security keys generated by the previous RAKP1 message. This behavior can cause synchronization errors with the management console.

Implication: The secure ASF session associated with the security keys could be lost. This problem is a manageability firmware erratum.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping).

44. Initial TCO Resets Do Not Succeed

Problem: The first TCO reset after a power-up does not succeed in resetting TCO bits in the MANC and RCTL registers. This problem is a manageability firmware erratum that affects compatibility with legacy 82559 operation.

Implication: TCO mode operation will not be correct until subsequent resets.

Workaround: An SMB transaction can be performed (for example, a read status request) prior to the first TCO reset. After the prior transaction history is created, all subsequent TCO resets will succeed.

Status: Intel resolved this erratum in the 82547GI Gigabit Ethernet Controller (B1 stepping).

45. First SMB Transaction after System Power-Up is NACK'ed

Problem: This issue is relevant only for the first power-up, signified by a change in the auxiliary power state, caused by a physical disconnection or connection of the AC power cord. The 82547 controller will Not Acknowledge (NACK) the address byte of the first SMB access transaction received after the first power up event. All subsequent SMB transactions will be acknowledged (ACK'ed), responded and processed correctly.

Implication: Configuration changes may be lost by the 82547 controller, causing synchronization loss between the SMB master and the 82547 controller.

Workaround: The SMB master should implement an SMB retransmission mechanism after all failed SMB transactions. This mechanism will solve this issue as well as SMB failures resulting from a noisy electrical environment. A retransmission count of 2 transactions will suffice to solve this issue completely.

Status: Intel does not plan to resolve this erratum in the 82547 Gigabit Ethernet controller family.

46. 1000 Mbps Slave Link failures With High Jitter Link Partners and Short Cables

Problem: When configured to 1000 Mbps slave mode, the 82547 device PHY has an unstable link with high jitter link partners. This issue is relevant only for shorter cable connections, where the cable length is approximately less than 20 meters. The instability is characterized with frequent link drops or high bit error rate if a valid link is present. On master mode the connection is stable and link is established and maintained.

Implication: An unstable and unreliable connection may be obtained when connected to high jitter link partners with short cable. For B0 steppings or earlier, the PHY default configuration is slave mode. Therefore, the problem may be observed if no action is taken.

For the B1 stepping and later versions, the PHY default is automatic, meaning it becomes either master or slave. Thus, the problem is only observed if the PHY was placed into slave mode as result of the Auto-Negotiation process.

Workaround: For proper link with the high jitter link partners, it is required to set the PHY to master mode via a software driver version that can force the PHY into master mode.

Status: Intel does not plan to resolve this erratum in the 82547 Gigabit Ethernet controller family.

SPECIFICATION CLARIFICATION

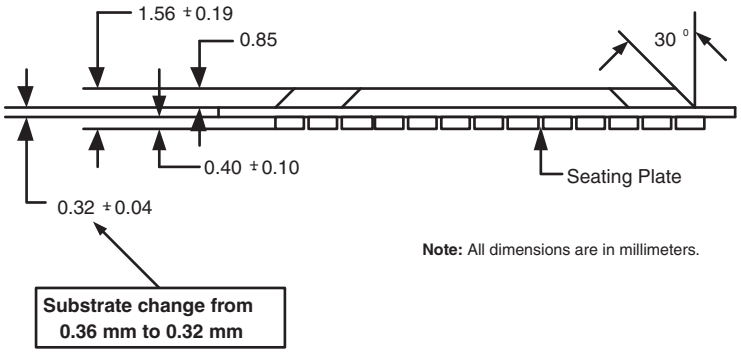
1. Substrate Suppliers Migrating to a Thinner Substrate

Clarification: 196-pin BGA substrate suppliers migrating from a 2-layer 0.36 mm wide-trace substrate to a 2-layer 0.32 mm wide-trace substrate.

PCN 104210-00

Implication: This migration allows flexibility with new substrate suppliers to support Intel demands on PBGA.

This migration does not affect fit, form, or function.



2. External Oscillator Support Clarification

Problem: The supporting 82547 Ethernet controller documentation does not specify support of an external oscillator.

The 82547 clock input circuit is optimized for use with an external crystal. However, an oscillator may also be used for the 82547GI/EI in place of a crystal with proper design considerations. The latest 82562EZ(EX)/82547GI(EI) Dual Footprint Design Guide should be consulted for further details.

Affected Specs: 82562EZ(EX)/82547GI(EI) Dual Footprint Design Guide, Revision 1.9; 82547GI/82547EI Gigabit Ethernet Controller Datasheet, Revision 2.1; Intel Ethernet Controllers Timing Device Selection Guide, Application Note.

3. Resistor Value Changes for 82547GI Stepping

Problem: The 82547GI (B1 stepping) has new I/O drivers that have a lower internal pull-up resistance value than previous versions of the 82547. Thus, some designs will require a change to the value of the pull-down resistors.

On ball C4, the EE_MODE pin, use a recommended value of 100 Ω, instead of the 1 K Ω used in previous 82547 steppings, if a MicroWire EEPROM is used in the current solution. There is no impact to designs using an SPI EEPROM.

On ball L13, the JTAG_TRST pin, use a recommended value of 100 Ω, instead of the1 K Ω used in previous 82547 steppings.

For 82547GI, verify vendor specifications to ensure that Vol is less than 0.7 V on ball N10, EEDO, and ball P9, FLSH_SO/LAN_DISABLE#.

Affected Specs: For more information refer to the design schematics (design guide) and datasheet for the 82547 Ethernet Controller.

DOCUMENTATION CHANGES

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