82541 Family
Gigabit Ethernet Controller
Specification Update

May 2006

82541 family Gigabit Ethernet controllers may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

82541PI/GI/EI Gigabit Ethernet Controller Specification Update

Date of Revision	Description
May 2006	Added new description for section "Component Identification Via Programming Interface".
April 2006	Changed 82541PI C0 lead-free component identification device ID from 00h to 05h.
December 2005	Added 82541PI C0 lead-free component identification device ID.
August 2005	Changed Device ID for the 82541PI C0 from 01h to 05h. Added Errata #51.
July 2005	Removed Spec Clarification #1 and updated Erratum #50.
June 2005	Added erratum number 50 "82547EI/82541EI will fail to establish 1000Mbps link when connected peer-to-peer with another 82547EI/82541EI" Added Specification Clarification #6 "82541EI & 82547EI EEPROM images impact PHY performance"
February 2005	Added erratum number 49, "82541 Gigabit Ethernet Controller Might Fail to Wake Up a System". Changed Specification Clarification #4. Changed text from: "… larger internal pull-up resistance …" to "… lower internal pull-up resistance …".
March 2004	Added 82551PI (C0 stepping) to the specification update. Included Specification Change 1, "General Operating Conditions for 1.8V and 1.2V." Added erratum number 48, "Possible Ripple on 1.8V and 1.2V Regulator Outputs."
November 2003	Initial Public Release

PREFACE

This document is an update to published specifications. Specification documents for this product include:

- 82541 Family of Gigabit Ethernet Controllers Datasheet.
- 82540EP/82541(PI/GI/EI) and 82562EZ(EX) Dual Footprint Design Guide Application Note (AP-444).
- 82541PI(ER) and 82562EZ(EX) Dual Footprint LOM Design Guide Application Note (AP-468).
- 82547GI(EI)/82541(PI/GI/EI)/82541ER EEPROM Map and Programming Information Guide (AP-446).

For software driver programming information, please contact your Intel representative.

This document is intended for hardware system manufacturers and software developers of applications, operating systems or tools. It may contain Specification Changes, Errata, and Specification Clarifications.

All 82541product family documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

NOMENCLATURE

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

COMPONENT IDENTIFICATION VIA PROGRAMMING INTERFACE

The 82541 Family of GbE controllers require the appropriate EEPROM images described in *Application Note (AP-446) 82547GI(EI)/82541(PI/GI/EI)/82541ER EEPROM Map and Programming Information Guide* and can be identified by the following register contents:

Stepping	Vendor ID	Device ID	Revision Number
82541EI A0	8086h	1013h	00h
82541EI A1	8086h	1013h	01h
82541EI B0	8086h	1013h	00h
82541GI B1	8086h	1076h	00h
82541PI C0	8086h	1076h	05h
82541PI C0	8086h	107Ch[1]	05h

[1] Lead-free version.

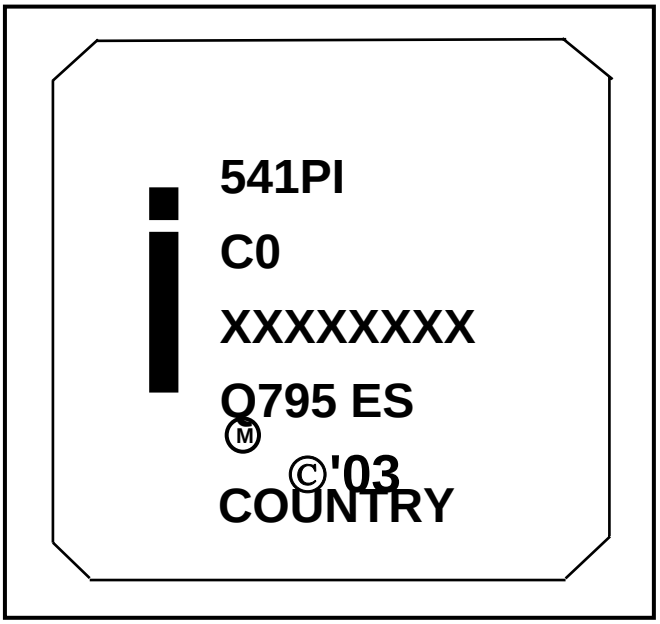
GENERAL INFORMATION

This section covers 82541PI/GI/EI devices.

82541 FAMILY COMPONENT MARKING INFORMATION

Product	Stepping	QDF Number	Top Marking	Notes
82541EI	A0	Q 516	541EI	Engineering Samples
82541EI	A1	Q 776	541EI	Engineering Samples
82541EI	B0	Q 778	541 EI	Engineering Samples
82541EI	B0		82541EI	Production Units
82541GI	B1	Q787	541EI or 541GI	Engineering Samples
82541GI	B1		82541GI	Production Units
82541PI	C0	Q795	541PI	Engineering Samples
82541PI	C0		541PI	Production Units

Note: 82541PI devices that are lead-free are marked with a circled "e1" and have a product code prefix: LUxxxxxx.



SUMMARY TABLE OF CHANGES

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82541PI/82541GI/82541EI steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLES

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to the listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

No.	EI A0	EI A1	EI B0	GI B1	PI C0	Plans	SPECIFICATION CHANGES	Page	Notes
1							General Operating Conditions for 1.8V and 1.2V	5	
2							DC Power Specifications for 1.8V, 1.2V, and 3.3V	5	
No.	**EI A0**	**EI A1**	**EI B0**	**GI B1**	**PI C0**	**Plans**	**ERRATA**	**Page**	**Notes**
1	X	X	X	X	X	NoFix	Master-Aborts with Some Chipsets During Driver-Initiated Controller Reset	7	
2	X	X				Fixed	ASF Manageability Not Fully Functional	7	
3								7	(Deleted)
4								7	(Deleted)
5	X					Fixed	1.2V Power Regulation	7	
6	X	X				Fixed	1000BASE-T PHY Performance Problems	8	
7	X	X				Fixed	JTAG Boundary Scan	8	
8	X	X	X			Fixed	PEC Utilized Incorrectly When SMB Master	8	
9	X					Fixed	RMCP Responses Use Erroneous Sequence Number	8	
10	X					Fixed	ASF Push Messages	9	
11	X					Fixed	SMB Pass Through Mode	9	
12	X					Fixed	No Response to ASF ARP Requests	9	
13	X	X				Fixed	Power Savings Techniques When Operating at 1000 Mbps	9	
14	X	X				Fixed	Smart Powerdown Operation	9	
15	X					Fixed	Crystal Oscillator Operation at High Temperature	9	
16	X					Fixed	PHY Link Stability Problem at 100 Mbps and 1000 Mbps	10	
17	X					Fixed	RMCP Remote Commands	10	
18	X	X				Fixed	Watchdog Expiration Does Not Enable RMCP and ARP Reception	10	
19	X	X				Fixed	Non-Compliant 100BASE-TX Hubs	10	
20	X	X				Fixed	VLAN Filtering	10	
21	X	X				Fixed	Multicast Filtering	11	
22	X					Fixed	LAN Manageability Packets with Don’t Fragment Flag Set	11	
23	X	X				Fixed	Forced TCO Reset Not Functional	11	
24	X	X				Fixed	Non-Compliant Gigabit Scrambler Support	11	

No.	EI A0	EI A1	EI B0	GI B1	PI C0	Plans	ERRATA	Page	Notes
25	X	X	X			Fixed	Microwire* EEPROM Unusable for Manageability Applications	11	
26	X	X				Fixed	LAN Disable Floats Voltage Regulator Control Outputs	11	
27	X	X	X	X	X	NoFix	Marginal Internal Power On Reset Function	12	
28	X	X	X			Fixed	Transmit Amplitude	12	
29			X			Fixed	PHY Write Command Incorrectly Writes to MAC Registers	12	
30			X			Fixed	No Link with Forced 100 Mbps Partner if 10 Mbps Link Up Feature Selected	13	
31	X	X	X			Fixed	Excessive Gigabit Link Time	13	
32			X			Fixed	Smart Speed Does Not Transition to 100 Mbps	13	
33	X	X	X	X	X	NoFix	Partner Assumed to Be Full Duplex When Downshifting from 1000BASE-T to 100BASE-TX	14	
34			X			Fixed	PHY Write Mechanism Supercedes EEPROM LED1/ACT# Configuration	14	
35	X	X	X			Fixed	Long Link Time to Busy 100BASE-TX Hub	14	
36	X	X	X			Fixed	SMB ARP Get UDID Commands	15	
37	X	X	X	X	X	NoFix	DHCP Not Supported	15	
38	X	X	X			Fixed	Watchdog Initialization Upon Exiting Reset	15	
39	X	X	X	X	X	NoFix	PET Transient Event Processing During LAN Link Down	15	
40	X	X	X	X	X	NoFix	I2C Short Transactions Not Supported for Address C8h	15	
41	X	X	X			Fixed	MDI-X Operation	15	
42	X	X	X			Fixed	Software Resets Do Not Cause Status Change in TCO Mode	16	
43	X	X	X			Fixed	Security Key Synchronization Error	16	
44	X	X	X			Fixed	Initial TCO Resets Do Not Succeed	16	
45	X	X	X	X	X	NoFix	Message Signaled Interrupt Feature May Corrupt Write Transactions	16	
46	X	X	X	X	X	NoFix	First SMB Transaction after System Power-Up is NACKed	17	
47	X	X	X	X	X	NoFix	1000 Mbps Slave Link Failures with High Jitter Link Partners and Short Cables	17	
48	X	X	X	X	X	NoFix	Possible Ripple on 1.8V and 1.2V Regulator Outputs	17	
49	X	X	X	X	X	Fix	82541 Gigabit Ethernet Controller Might Fail to Wake Up a System	18	
50	X	X	X			Fixed	82541EI Fails to Establish 1000Mbps Link When Connected Peer-to-Peer with Another 82541EI	18	
51					X	NoFix	Intermittent Issues with TCO Receive Packets in IPMI Mode (82541PI)	18	
No.	**EI A0**	**EI A1**	**EI B0**	**GI B1**	**PI C0**	**Plans**	**SPECIFICATION CLARIFICATIONS**	**Page**	**Notes**
1	X	X	X	X	X	NoFix	LEDs Inactive Until Driver Loads	20	
2	X	X	X	X		NoFix	Crystal Specification Revised Due to Low Clock Drive Strength	20	
3	X	X	X			Fixed	External Oscillator Support Clarification	20	
4					X	NoFix	Resistor Value Changed for 82541PI stepping	20	
5	X	X	X	X	X	NoFix	PCI-X Capability Register in PCI Configuration Space	21	
6	X	X	X	X	X	Fixed	82541EI & 8247EI EEPROM Images Impact PHY Performance	21	
No.	**EI A0**	**EI A1**	**EI B0**	**GI B1**	**PI C0**	**Plans**	**DOCUMENTATION CHANGES**	**Page**	**Notes**

SPECIFICATION CHANGES

General Operating Conditions for 1.8V and 1.2V

Problem: This change is related to erratum 48, "Possible Ripple on 1.8V and 1.2V Regulator Outputs," listed in this document. Due to this anomaly, the following specifications were modified to the following:

Symbol	Parameter	Min	Max	Units
VDD(1.8)	DC supply Voltage on 1.8V pins	1.71	1.89	V
VDD(1.2)	DC supply Voltage on 1.2V pins	1.14	1.26	V
Voltage Ramps				
1.8V Ripple	Maximum voltage ripple at frequency below 1 MHz		280	$mV_{pk\text{-}to\text{-}pk}$
1.8V Ripple	Maximum voltage ripple at frequency below 1 MHz Note: This is the lowest absolute voltage for the frequency range below 1 MHz.	1.55		V
1.2V Ripple	Maximum voltage ripple at frequency below 1 MHz		180	$mV_{pk\text{-}to\text{-}pk}$
1.2V Ripple	Maximum voltage ripple at frequency below 1 MHz Note: This is the lowest absolute voltage for the frequency range below 1 MHz.	1		V

DC Power Specifications for 1.8V, 1.2V and 3.3V

Problem: The subsystem power consumption in D3 cold wake-enabled @ 100Mbps and D0 active @ 10Mbps is not specified. Also power specifications may be rounded off.

The subsystem power consumption has been updated in the subsystem power specification table. The modified Power specifications are listed below. These specifications are updated in the 82541 Datasheet (Revision 3.1).

Power Specifications - Doa

	D0a							
	Unplugged no link		@ 10 Mbps		@ 100 Mbps		@ 1000 Mbps	
	Typ Icc (mA)[a]	Typ Icc (mA)[b]	Typ Icc (mA)[a]	Typ Icc (mA)[b]	Typ Icc (mA)[a]	Typ Icc (mA)[b]	Typ Icc (mA)[a]	Typ Icc (mA)[b]
3.3V	3	5	5	10	13	15	30	40
1.8V	14	15	85	85	110	115	315	320
1.2V	30	35	85	90	90	100	380	400
Total Device Power	75 mw	85 mW	270 mW	295 mW	350 MW	380 mW	1.1 W	1.2 W

a. Typical conditions: operating temperature (TA) = 25 C, nominal voltages, moderate network traffic at full duplex, and PCI 33 MHz system interface.

b. Maximum conditions: minimum operating temperature (TA) values, maximum voltage values, continuous network traffic at full duplex, and PCI 33 MHz system interface.

Power Specifications – D3cold

	D3cold – wake-up enabled[a]						D3cold – wake disabled	
	Unplugged link		@ 10 Mbps		@ 100 Mbps			
	Typ Icc (mA)[b]	Typ Icc (mA)[c]	Typ Icc (mA)[b]	Typ Icc (mA)[c]	Typ Icc (mA)[b]	Typ Icc (mA)[c]	Typ Icc (mA)[b]	Typ Icc (mA)[c]
3.3V	2	3	2	3	2	3	4	5
1.8V	14	15	20	25	110	115	1	2
1.2V	21	25	30	35	80	85	7	10
Total Device Power	60 mw	70 mW	80 mW	100 mW	300 MW	320 mW	25 mW	35 mW

a. At 1000 Mbps, power consumption is not shown since the controller switches to the 10/100 Mbps state before entering D3 to conserve power.

b. Typical conditions: operating temperature (TA) = 25 C, nominal voltages, moderate network traffic at full duplex, and PCI 33 MHz system interface.

c. Maximum conditions: minimum operating temperature (TA) values, maximum voltage values, continuous network traffic at full duplex, and PCI 33 MHz system interface.

Power Specifications – Complete Subsystem

	Complete Subsystem (Reference Design) including Magnetics, LED, Regulator Circuits											
	D3cold – wake disabled		D3cold wake-enabled @ 10 Mbps		D3cold wake-enabled @ 100 Mbps		D0 @ 10 Mbps active		D0 @ 100 Mbps active		D0 @ 1000 Mbps active	
	Typ Icc (mA)[a]	Typ Icc (mA)[b]	Typ Icc (mA)[a]	Typ Icc (mA)[b]	Typ Icc (mA)[a]	Typ Icc (mA)[b]	Typ Icc (mA)[a]	Typ Icc (mA)[b]	Typ Icc (mA)[a]	Typ Icc (mA)[b]	Typ Icc (mA)[a]	Typ Icc (mA)[b]
3.3 V	4	5	2	3	6	7	7	12	19	21	36	46
1.8 V	1	2	20	25	110	115	85	85	110	115	315	320
1.2 V	7	10	30	35	80	85	85	90	90	100	380	400
Subsystem Power	40 mW	60 mW	170 mW	210 mW	650 mW	685 mW	585 mW	620 mW	725 mW	780 mW	2.4 W	2.5 W

a. Typical conditions: operating temperature (TA) = 25 C, nominal voltages, moderate network traffic at full duplex, and PCI 33 MHz system interface.

b. Maximum conditions: minimum operating temperature (TA) values, maximum voltage values, continuous network traffic at full duplex, and PCI 33 MHz system interface.

ERRATA

1. Master-Aborts with Some Chipsets during Driver-Initiated Controller Reset

Problem: 82541 family Gigabit Ethernet controllers implement a software-Initiated device reset function through the control register space (Control Register, bit 31). This software-initiated reset re-initializes all functional state of the controllers except for PCI/PCI-X configuration. When the reset is written, the controllers require a few internal clock cycles to complete the reset operation. During this brief time, they will not respond to additional register accesses.

Some PCI/PCI-X bridge components implemented with internal 64-bit architectures may initiate an additional zero byte write immediately following a 32-bit write to the device CTRL register. This zero byte write is essentially padding for a 64-bit transaction. In cases where the CTRL register access performs a software reset of the controller, the zero byte operation may encounter a master abort due to the controller reset in progress.

Implication: In most system configurations, a master abort on an outbound 0-byte write operation will not result in any adverse system behavior, though the event may be logged at the chipset, bridge, or operating system level.

If the bridge/chipset is configured to promote the master abort to a Non-Maskable Interrupt (NMI) **and** the operating system cannot discern and handle NMI events, then a fatal operating system error may occur.

Workaround: The 82541 family device can only be accessed using DWord (32-bit) software operations. Since the potential zero byte write immediately following a device CTRL register write is a hardware event created by the chipset bridge components, no software mechanism can be used to eliminate the 0-byte write operation.

When an operating system is incapable of handling the NMI event, the chipset or bridge should be configured to avoid promoting this master abort to a fatal NMI event. Alternatively, the software-initiated device reset may be performed using an I/O access in place of a memory-mapped device access. The latter solution is effective if master aborts on I/O writes do not result in NMI.

Status: Intel does not plan to resolve this erratum in the 82541 Gigabit Ethernet Controller.

2. ASF Manageability Not Fully Functional

Problem: The 82541 Gigabit Ethernet Controller does not exhibit full ASF 2.0 functionality.

Implication: Multiple features are affected. Implementing ASF manageability in customer systems with the A0 stepping is not fully supported.

Workaround: The 82541 controller provides a method to apply ASF firmware changes in the EEPROM. Application of these flexible firmware upgrades has been demonstrated to provide ASF 1.0 and legacy alerting capability.

These firmware patches require significant amounts of program memory, which requires the use of a larger than expected EEPROM. Intel required a minimum 8-Kbyte EEPROM size to support manageability during the early development cycle of the 82541 controller. (Non-manageability applications were not affected.)

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller. The minimum EEPROM size to implement manageability is now 500 bytes. However, some implementations will need up to 8 Kbytes for supporting future enhancements. Erratum #25, “Microwire EEPROM Unusable for Manageability Applications” also applies.

3. (Deleted)

4. (Deleted)

5. 1.2V Power Regulation

Problem: The on-board power regulator control circuit used with an external PNP transistor does not have adequate internal grounds. As a result, it does not keep the 1.2V within its regulation band and the voltage may oscillate at a rate of approximately 200 KHz.

Implication: The PHY transmit and receive clocks may have excessive jitter, affecting overall PHY performance.

Workaround: Using a short wide trace from the CTRL_18 output to the PNP transistor is desirable. However, this technique is not completely effective.

Status: Intel resolved this erratum in the A1 stepping of the 82541 Gigabit Ethernet Controller.

6. 1000BASE-T PHY Performance Problems

Problem: The PHY exhibits several performance problems at 1000 Mbps:

- Link acquisition may be slow, taking more than 3.5 seconds.
- It may not be possible to achieve link with cables more than 80 meters long.
- Bit Error Rates may exceed 10^{-10}, failing IEEE 802.3 specifications.

These problems are caused by the DSP receive clock recovery unit being unable to lock properly and are related to erratum 16, “PHY Link Stability Problem at 100 and 1000 Mbps.”

Implication: The PHY will not be able to achieve link across the full range of operating conditions. Large numbers of receive data errors may occur as cable lengths increase, requiring data to be re-transmitted.

Workaround: Perform early evaluations with short cables, using slower (10/100 Mbps) data rates.

Status: Intel has partially resolved this erratum in the A1 stepping of the device and has fully resolved it in the B0 stepping of the 82541 Gigabit Ethernet Controller. However, erratum 31, “Excessive Gigabit Link Time,” should be considered.

7. JTAG Boundary Scan

Problem: The JTAG SAMPLE and EXTEST instructions do not correctly capture pin input data into the scan cells for all signals. On the 82541 device, many inputs are affected, including the PCI bus.

This erratum is caused by incorrect connections between the affected pad cells and boundary scan cells.

Implication: Boundary scan will not be able to capture signals asserted on all input pins by a functional tester during board tests.

Workaround: Use boundary scan with reduced functionality. The port declarations in the BSDL file reflect the reduced boundary scan functionality for each pin where applicable. For example, both the FL_SO and FL_SI pins are denoted as “out” (output) pins even though FL_SO is an input. This declaration will prevent a JTAG-based test program from scanning erroneous input data from the FL_SO pin.

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller. A new BSDL file reflects the full functionality.

8. PEC Utilized Incorrectly When SMB Master

Problem: When the 82541 controller is an SMB master device, it may calculate the Packet Error Correction (PEC) incorrectly, causing SMB master write transactions to send an incorrect PEC value. In addition, SMB master read transactions may disregard the received PEC value during operations such as ASF sensor polling.

Implication: When the 82541 controller acts as an SMB master device, it may calculate the Packet Error Correction (PEC) incorrectly, causing SMB master write transactions to send an incorrect PEC value. In addition, SMB master read transactions may disregard the received PEC value during operations such as ASF sensor polling.

Workaround: Currently, there are no workarounds for this anomaly.

Status: This has been partially corrected in the B0 stepping of the 82541 controller and fully corrected in the B1 stepping (82541GI) of the 82541 controller.

9. RMCP Responses Use Erroneous Sequence Number

Problem: Remote Management Control Protocol (RMCP) responses should return a sequence number from ASF register F4h. Instead, responses will return the sequence number found in the request packet.

Implication: This problem impairs the ASF manageability packet security mechanism for RMCP. Thus, the 82541 controller’s RMCP responses may be rejected. This occurs only in ASF 2.0.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the A1 stepping of the 82541 Gigabit Ethernet Controller.

10. ASF Push Messages

Problem: ASF only supports a single push request. The queue for multiple push requests was not correctly implemented.

Implication: The ASF subsystem sends push requests multiple times over a one-minute period. During this time, no other push requests can be issued.

Workaround: There are no workarounds for this anomaly.

Status: This has been resolved in the A1 stepping of the 82541 Gigabit Ethernet Controller.

11. SMB Pass Through Mode

Problem: SMB pass through mode is not functional. Specific pass through mode functions affected include: SMB ARP, alert responses, manageability ARP response, and receive enable status report. The problem occurs because pass through mode uses registers that are cleared at startup.

Implication: In a multiple SMB slave environment such as IPMI, the SMB alert functionality will not be functional. This problem affects ASF 2.0 operation.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the A1 stepping of the 82541 Gigabit Ethernet Controller.

12. No Response to ASF ARP Requests

Problem: The Address Resolution Protocol (ARP) filter in the manageability block incorrectly resets. This action causes the 82541 to ignore ASF ARP requests. Responses are not sent back to the network.

Implication: Routers on the network commonly send ARP requests. When ARP requests are not acknowledged, these routers may have difficulty locating 82541-based manageability devices on the network.

Workaround: A firmware patch is available for the A1 stepping.

Status: Intel resolved this erratum in the A1 stepping of the 82541 Gigabit Ethernet Controller.

13. Power Saving Techniques When Operating at 1000 Mbps

Problem: Power saving techniques at gigabit speeds are not fully operational.

Implication: For the 82541 controller A0 stepping, PHY power consumption in gigabit operation is approximately 30 mW more than anticipated. The increase will be seen on the 1.2V power rail.

Workaround: There are no workarounds for this erratum.

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller.

14. Smart Powerdown Operation

Problem: Powerdown techniques in the D0 No Link Mode (Smart Powerdown) are not fully operational.

Implication: For the 82541 controller A0 stepping, PHY power consumption in D0 (without link) is approximately 30 mW more than anticipated. The increase will be seen on the 1.2V power rail.

Workaround: There are no workarounds for this erratum.

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller.

15. Crystal Oscillator Operation at High Temperature

Problem: The crystal oscillator may stop at case temperatures higher than 70° C. The failure is due to higher than expected XTAL1/XTAL2 pad leakage in conjunction with the high resistance of the internal feedback resistor.

Implication: If the 82541 oscillator fails, internal clocks will not run and the device will not operate.

Workaround: Connect a resistor of approximately 500 KΩ value from XTAL1 to XTAL2. The exact value of the resistor is not critical. In other words, a 470 KΩ or 510KΩ resistor may be used. The parallel combination of the internal feedback resistor and the external resistor will be low enough to ensure oscillation.

Status: Intel resolved this erratum in the A1 stepping of the 82541 Gigabit Ethernet Controller.

16. PHY Link Stability Problem at 100 Mbps and 1000 Mbps

Problem: The 82541 controller may occasionally lose and re-acquire link. This problem is caused by the DSP receive clock recovery unit being unable to lock properly. The problem is related to erratum 6, “1000BASE-T PHY Performance Problems.”

Implication: The PHY will not be able to maintain link across the full range of operating conditions. Due to the instability, the receiver may drop some packets. The missing packets will be indicated in appropriate statistics registers.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the A1 stepping of the 82541 Gigabit Ethernet Controller. However, erratum 31, “Excessive Gigabit Link Time,” should be looked at.

17. RMCP Remote Commands

Problem: The manageability module will send incorrect remote commands over the SMB for legacy device descriptors with non-zero status values.

The RMCP remote command (power up, power down, power cycle and reset) for a legacy device consists of an SMB read byte transaction followed by an SMB write byte transaction. The write data is supposed to consist of the read data OR-ed with a command mask. The problem is that the manageability module sends the command mask instead.

Implication: If the legacy device has a non-zero status value, the remote command associated with the data will be incorrect. This means that older sensors may be handled incorrectly under ASF 1.0 and 2.0.

Workaround: There are no workarounds for this erratum.

Status: Intel resolved this erratum in the A1 stepping of the 82541 Gigabit Ethernet Controller.

18. Watchdog Expiration Does Not Enable RMCP and ARP Reception

Problem: Watchdog expiration should cause the manageability module to enable receiving all incoming Remote Management Control Protocol (RMCP) and Address Resolution Protocol (ARP), regardless of whether it was enabled before the watchdog expired. Instead, the enabled/disabled condition does not change.

Implication: If the system was not configured to receive or respond to RMCP commands and ARP requests prior to watchdog expiration, watchdog expiration will not enable those activities. If the system ignores an important RMCP command, it may not be able to recover from the condition that led to the watchdog expiration.

Workaround: Always leave ARP and RMCP reception enabled. ASF firmware patches work around this erratum successfully.

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller.

19. Non-Compliant 100BASE-TX Hubs

Problem: If Auto-Negotiation is enabled, the 82541 PHY will not establish link with certain 100BASE-TX hubs that transmit unscrambled idles when their receivers are idle. The PHY does not support unscrambled idles causing parallel detection to fail.

Implication: The 82541 device will not achieve link with some legacy 100 Mbps hubs (for example, a Bay Networkshub). No problem occurs for hubs that transmit scrambled idles unconditionally.

Workaround: For non-compliant hubs, force link by setting PHY register 0 to 2100h.

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller.

20. VLAN Filtering

Problem: VLAN packets (register bit RCTL.VFE) do not pass the packet filter because of a problem with the memory that stores the filter table values.

Implication: VLAN packets will not be received from the network. Exact filters are not affected. This erratum is closely related to erratum 21, “Multicast Filtering.”

Workaround: There is no workaround for the VLAN Filtering erratum.

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller.

21. Multicast Filtering

Problem: Multicast packets (register bit RCTL.MPE) do not pass the packet filter due to a problem with the memory that stores the filter table values.

Implication: Multicast packets will not be received from the network. Exact filters are not affected. This erratum is closely related to erratum 20, “VLAN Filtering.”

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller.

22. LAN Manageability Packets with Don’t Fragment Flag Set

Problem: If an incoming packet is received and the Don’t Fragment Flag is set in the IP header (4000h), the packet will be discarded. This problem only affects manageability packets.

Implication: Manageability packets are unnecessarily discarded.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the A1 stepping of the 82541 Gigabit Ethernet Controller.

23. Forced TCO Reset Not Functional

Problem: TCO packets have the ability to force reset to the controller. If reset is forced in this way, the TCO controller will start reading from the EEPROM before the reset is completed.

Implication: TCO control registers will be corrupted, and the manageability block will no longer be able to send or receive packets.

Workaround: The Device Reset Upon Force TCO Command should be disabled through the EEPROM. This is accomplished by programming bit 2 of word 23h to 0.

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller.

24. Non-Compliant Gigabit Scrambler Support

Problem: The PHY fails to communicate with a non-compliant gigabit scrambler in a gigabit link partner due to a DSP timing problem. This capability is enabled in PHY register 18, bit 9.

Implication: An early gigabit PHY incorrectly implemented the Channel C scrambler polynomial in the Physical Coding Sub-layer. If the 82541 controller encounters this PHY as a link partner, the controller is unable to adapt to the incorrect coding and obtain link.

Workaround: A short cable should be used to avoid this anomaly.

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller.

25. Microwire EEPROM Unusable for Manageability Applications

Problem: The manageability firmware cannot access Microwire EEPROMs. This problem is not specific to any particular alerting activity.

Another erratum prevented the manageability hardware block from accessing the EEPROM and was capable of causing system lockups. However, that erratum was corrected in the 82541 controller B0 stepping.

Implication: Manageability firmware cannot read or write Microwire EEPROMs.

Workaround: An SPI* EEPROM should be used in all systems with ASF 1.0 or ASF 2.0 alerting. Microwire EEPROMs may be used in non-alerting applications. The SMB should be disabled by programming EEPROM word 23h, bit 0.

Status: Intel resolved this erratum in the 82541 B1 step (82541GI) Gigabit Ethernet Controller.

26. LAN Disable Floats Voltage Regulator Control Outputs

Problem: The LAN_DISABLE# pin is sampled during reset. When the controller is disabled, it floats the CTRL_12 and CTRL_18 regulator control outputs and the external PNP transistors will not be biased correctly across their collector-base junctions.

Implication: Regulation will not occur and the 1.2V and 1.8V supply rails will move toward 3.3V. However, minimal current will flow because the controller is disabled. Systems that do not use the internal voltage regulator controls are not affected.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the B0 stepping of the 82541 Gigabit Ethernet Controller.

27. Marginal Internal Power on Reset Function

Problem: Power on (internal) reset is not dependable in the event of a slow power ramp. If the 3.3V supply ramps slowly, the 1.2V supply (from the collector of the external PNP pass transistor) may not be stable when reset occurs. Voltage thresholds are not within design targets.

Implication: Internal power on reset is an alternative to using the LAN_PWR_GOOD input. To enable power on reset, LAN_PWR_GOOD must be connected to 3.3V through a pull-up resistor. For this configuration, a power ramp specification **must** be imposed and that the 3.3V supply ramps from its 10% point to its 90% point in less than 15 ms. This requirement is more restrictive than the general recommendation that all power supplies should ramp to within their regulation bands in less than 20 ms.

Workaround: The LAN_PWR_GOOD signal should be connected to the system's voltage supervisor function. Using LAN_PWR_GOOD as the external reset input is the preferred method.

Status: Intel does not intend to resolve this erratum in the 82541 Gigabit Ethernet controller family.

28. Transmit Amplitude

Problem: Some electrical parameters of the 82541 controller are trimmed as the devices are being tested. One of the parameters trimmed is the differential output amplitude. The IEEE specifications for this parameter are:

- 1000BASE-T specification: 670 mV – 920 mV
- 100BASE-TX specification: 950 mV – 1050 mV
- 10BASE-T specification: 2.2 V – 2.8 V

Due to a test program error, A0 and A1 device trimming made the PHY differential output amplitude low. Observed amplitudes were as follows:

- 1000BASE-T: ~710 mV
- 100BASE-TX: ~900 mV
- 10BASE-T: ~2.2V

The test program was improved during B0 manufacturing validation. For B0 engineering samples, device trimming made the PHY differential output amplitude high. Observed amplitudes were as follows:

- 1000BASE-T : ~850 mV
- 100Base-TX: ~1120 mV
- 10BASE-T: near the middle of the specification range

The test program was fully calibrated for B0 production. B0 production devices are trimmed and tested so that output amplitudes are distributed near the middle of all three specification ranges.

Implication: Systems built with A0, A1and B0 sample devices may not pass IEEE PHY conformance tests for 10/100 Mbps operation. Link acquisition should not be significantly affected.

Note: Other A0 and A1 PHY problems could also affect IEEE conformance tests.

Workaround: There are no workarounds for this erratum.

Status: Intel resolved this erratum in the production test program used for the 82541 device B0 stepping.

29. PHY Write Command Incorrectly Writes to MAC Registers

Problem: The B0 stepping contains a mechanism to alter internal PHY configuration registers from EEPROM settings. If the PHY has been processing data and a PHY write is invoked, the logic can become confused and write MAC registers instead.

Implication: The PHY must be preconditioned by reset just prior to PHY write commands. Certain reset situations will require special attention because they do not automatically reset the PHY:

- Forced TCO resets. A device reset may be requested before sending out manageability packets for system hangs.
- Global software resets of the Ethernet controller.

Other types of resets (for example, LAN_PWR_GOOD and PCI Reset) automatically reset the PHY.

Workaround: To perform global resets, software should first reset the PHY by writing a 1 to bit 15 in the PHY Control Register (Address 00). After a fresh PHY reset, the state logic will not become confused.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping).

30. No Link with Forced 100 Mbps Partner if 10 Mbps Link Up Feature Selected

Problem: If the EEPROM is programmed to the power-on link up mode and advertises 10 Mbps only, the Ethernet controller will not link with a partner that is forced to 100 Mbps. This behavior occurs because the PHY inherently does not attempt parallel detection to a partner at the unadvertised speed.

Implication: The low power link up function was added on the B0 stepping. The 10 Mbps EEPROM setting will not result in reliable link at 100 Mbps.

Workaround: **T**he Advertise 10 Mbps and Link Up function should be disabled by programming EEPROM register 21h bit 3 to 0.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping).

31. Excessive Gigabit Link Time

Problem: Time for circuits to obtain lock is intermittently longer than the three second IEEE specification when connected to a gigabit link partner. Link time variability increases as cable lengths approach 100-meter specification cable. However, testing has demonstrated instances of exceeding the 3-second limit with shorter cable lengths.

Excessive link time can occur when link is established or re-established, including power-up, driver load, some power state changes, and PROSet configuration changes. If the first link attempt fails, subsequent link attempts can take between 2.5 and 3 seconds to complete. With longer cable lengths, over two attempts have been observed.

Implication: As the system boots and the driver initializes, the Ethernet controller is required to re-negotiate link. Excessive link time could delay network availability for mapping resources such as network drives.

When the system returns from a suspend state (S3 or S5 transitions to S0), the Ethernet controller is required to re-negotiate link. If the link time is longer than the time it takes to return from the power managed state, network access will not occur until link completes. At longer cable lengths the link speed is also subject to change after power managed states if convergence does not occur after four negotiation attempts.

When PROSet changes are made, the Ethernet controller is required to re-negotiate link. If link time is longer than the time to return from the PROSet dialog box network access will be delayed until link is re-established.

Workaround: The PHY should be adjusted through special EEPROM settings provided by Intel.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping), allowing driver patches to be removed and freeing up EEPROM capability. As expected, some EEPROM adjustments are still used to optimize the PHY receive path for particular board configurations.

32. Smart Speed Does Not Transition to 100 Mbps

Problem: When the PHY is configured to automatically assume master/slave status in gigabit mode, the smart speed function does not downshift to 100 Mbps.

Implication: Smart speed will not function without additional configuration.

Workaround: The workaround for the 82541 B0 stepping consists of forcing the PHY to Slave Mode with the EEPROM-based PHY write mechanism. The software driver will change to detect the situation where both link partners are slaves. If a slave-to-slave conflict exists, the driver toggles the mode to attempt gigabit link.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping).

33. Partner Assumed to Be Full Duplex When Downshifting from 1000BASE-T to 100BASE-TX

Problem: For a link partner that advertises 1000BASE-T full duplex and 100BASE-TX half duplex capabilities, the 82541family controller will attempt to link at 1000 Mbps, followed by 100 Mbps. However, it will assume the link partner is capable of full duplex operation at both speeds.

Implication: If the advertisement is correct, a problem could occur obtaining link. Practical Gigabit Ethernet devices are by default capable of full duplex operation. Thus, the possibility of this advertisement is very low.

Workaround: There is no workaround for this erratum.

Status: Intel does not intend to resolve this erratum in the 82541 Gigabit Ethernet controller family.

34. PHY Write Mechanism Supercedes EEPROM LED1/ACT# Configuration

Problem: The 82541 B0 stepping added a feature to make LED1/ACT# programmable from the EEPROM in the same manner as LED0 and LED2. LED settings are loaded from the EEPROM upon reset (PCI_RST#, LAN_PWR_GOOD, or software global reset). The settings are contained in word 21h bits 15:8. However, the PHY write mechanism used to work around the Gigabit Link Time and Smart Speed problems must be turned on by setting word 21h bits 10 and 8 to 1b. This configuration defeats many of the possible LED modes, including ACTIVITY# (mode = 0011b). Some of the other LED modes, for example LINK_10# (mode = 0101b) and LINK_1000 (mode = 0111b) are still possible.

Implication: LED1 is typically used as the ACTIVITY# LED. When the PHY write mechanism is used, ACTIVITY# EEPROM programmability is not available on LED1. If LED1 is wired up as ACTIVITY#, it will not be functional until the driver loads and programs the LED control register (LEDCTL) at offset 0E00h from the register base address.

Workaround: The system BIOS can write a copy of the desired EEPROM LED configurations to the LEDCTL register immediately after PCI enumeration. For example, writing binary 0000 0111 XXXX XXXX 1000 0011 XXXX XXXX to register offset 0E00h will program LED3 to be LINK1000# (mode = 0111b) and LED1 to be ACTIVITY# (mode = 0011b), with ACTIVITY# blinking (bit 15 = 1). This operation allows these LEDs to function in the interval before the software driver loads.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping). The PHY write mechanism now uses different EEPROM bits that do not conflict with LED programming.

35. Long Link Time to Busy 100BASE-TX Hub

Problem: At 100 Mbps, the 82541 controller may encounter a delay longer than 3 seconds to link when the LAN traffic consists of non-stop back-to-back packets. The problem occurs because the PCS scrambler is expects to receive idles to ensure correct DSP lock. The scrambler resets the PHY DSP when 3 µs has elapsed without idle pulses.

Implication: The problem occurs when the interpacket gap (IPG) is minimal between packets over a lengthy period. In lab testing, the problem was seen on hubs with sustained utilization above 50%.

In a typical LAN, IPG is rarely at the minimum because:

- On half-duplex hubs, there are collisions causing backoff.
- Upon link to a full duplex switch, LAN traffic does not instantaneously increase.
- Traffic consists of bursts since network protocols typically wait for acknowledgement.

If link is forced (speed and duplex) through the driver setup, the problem does not occur. This problem is independent of cable length.

Workaround: Some improvement may be obtained by monitoring the PHY Parallel Detect Fault Bit with software. If the bit is set, software can alternately disable and enable DSP resets, pausing in an attempt to get link. This workaround has not been incorporated into the Intel software driver.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping).

36. SMB ARP Get UDID Commands

Problem: ARP is used on the SMB to reconcile address conflicts. The SMB specification defines the SMB ARP Get Unique Device ID commands (general and directed) to always return 1b in the reserved address field of byte 17 bit 0. The manageability block will always return zero in this bit.

Implication: The bit is stuck at 0b. Although this behavior does not meet SMB specifications, Intel has not observed any SMB agent to be sensitive to the value of this bit.

Workaround: If possible, firmware in the external manageability device should ignore the value of this bit on a Get UDID response.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping).

37. DHCP Not Supported

Problem: The management block DHCP function has problems renewing IP addresses at the end of the lease. Therefore, typically an IP address will not be renewed upon link restoration.

Implication: The manageability DHCP function is not supported. This issue primarily affects mobile ASF applications.

Workaround: An upgrade firmware patch will be available through Intel in the future.

Status: Intel does not plan to resolve this erratum in the 82541 Gigabit Ethernet controller family.

38. Watchdog Initialization upon Exiting Reset

Problem: After the deassertion of reset, the controller reads initialization values from the EEPROM. However, the manageability watchdog timer counts down from its previous value and not from the value loaded from the EEPROM.

Implication: After system startup or return from powerdown, the watchdog timer is subject to counting down from the default minimum value programmed by BIOS. Timer expirations could be premature relative to timer expirations based on the EEPROM value.

Workaround: There is no workaround for this issue.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping).

39. PET Transient Event Processing During LAN Link Down

Problem: The manageability block will send transient SOS alert events when the LAN link is down.

Implication: A transient event is defined as a change of state followed by a return to the original state. This behavior does not meet ASF specifications.

Workaround: There is no workaround for this issue.

Status: Intel does not plan to resolve this erratum in the 82541Gigabit Ethernet Controller family.

40. I2C Short Transactions Not Supported for Address C8h

Problem: In TCO mode, the manageability block will not support I2C short read block transactions for SMB address C8h.

Implication: This behavior is a manageability usage limitation. Other addresses are available.

Workaround: A firmware workaround patch may be possible.

Status: Intel does not plan to resolve this erratum in the 82541Gigabit Ethernet controller family.

41. MDI-X Operation

Problem: MDI-X is a PHY capability that allows it to switch data pairs if the wrong cable (in other words, straight cable versus cross-over cable) is used in a particular application. Under MDI-X configuration, pair A swaps with pair B and, for Gigabit, pair C swaps with pair D. MDI-X operation does not work correctly and is not supported.

Implication: A LAN port based on the 82541 controller can communicate with its link partner if the cable correctly connects transmitters and receivers or if the partner supports MDI-X. If the cabling is incorrect and the partner does not have MDI-X capability, link will not occur.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping).

42. Software Resets Do Not Cause Status Change in TCO Mode

Problem: Software resets involving the MAC (for example, Global Resets) do not cause the manageability block to send a status change to the BMC master device if one is present in the system. This problem is a manageability firmware erratum that affects compatibility with legacy 82559 operation.

Implication: The system could experience a loss of link without any notification to the BMC device.

Workaround: A firmware workaround patch exists and is available through your local Intel representative.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping). An upgraded firmware patch is still used.

43. Security Key Synchronization Error

Problem: RAKP1 security key retransmissions may overwrite security keys generated by the previous RAKP1 message. This behavior can cause synchronization errors with the management console.

Implication: The secure ASF session associated with the security keys could be lost. This problem is a manageability firmware erratum.

Workaround: There is no workaround for this erratum.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping).

44. Initial TCO Resets Do Not Succeed

Problem: The first TCO reset after a power-up does not succeed in resetting TCO bits in the MANC and RCTL registers. This problem is a manageability firmware erratum that affects compatibility with legacy 82559 operation.

Implication: TCO mode operation will not be correct until subsequent resets.

Workaround: An SMB transaction can be performed (for example, a read status request) prior to the first TCO reset. After the prior transaction history is created, all subsequent TCO resets will succeed.

Status: Intel resolved this erratum in the 82541GI Gigabit Ethernet Controller (B1 stepping).

45. Message Signaled Interrupt Feature May Corrupt Write Transactions

Problem: The problem is with the implementation of the Message Signaled Interrupt (MSI) feature in the Ethernet controllers. During MSI writes, the controller incorrectly accesses the write data FIFO. If there are pending write transactions when this occurs, these transactions may become corrupted, which may cause the network controller to lock up and become unresponsive.

For a normal PCI write transaction, the controller's PCI logic receives data to be written from an internal FIFO. Once the controller is given bus ownership, the PCI logic pulls the data out of this FIFO and performs the write transaction.

For systems using MSI writes, the data, which is constant, should be pulled from the controller's PCI Configuration Space rather than the internal FIFO. The affected devices are not pulling this data from PCI Configuration Space. Instead, they are pulling data from the internal FIFO.

Implication: If the affected products are used with a future OS that uses Message Signal Interrupts and no accommodations are made to mitigate the use of these interrupts, data integrity issues may occur.

Workaround: For PCI systems, advertisement of the MSI capability can be turned off by setting the MSI Disable bit in the EEPROM (Init Control Word 2, bit 7).

Status: Intel does not plan to resolve this erratum in the 82541 Gigabit Ethernet controller family.

46. First SMB Transaction after System Power-Up is NACKed

Problem: This issue is relevant only for the first power-up, signified by a change in the auxiliary power state, caused by a physical disconnection or connection of the AC power cord. The 82541 controller will Not Acknowledge (NACK) the address byte of the first SMB access transaction received after the first power up event. All subsequent SMB transactions will be Acknowledged (ACKed), responded and processed correctly.

Implication: Configuration changes may be lost by the 82541 controller, causing synchronization loss between the SMB master and the 82541 controller.

Workaround: The SMB master should implement an SMB retransmission mechanism after all failed SMB transactions. This mechanism will solve this issue as well as SMB failures resulting from a noisy electrical environment. A retransmission count of 2 transactions will suffice to solve this issue completely.

Status: Intel does not plan to resolve this erratum in the 82541 Gigabit Ethernet controller family.

47. 1000 Mbps Slave Link failures With High Jitter Link Partners and Short Cables

Problem: When configured to 1000 Mbps slave mode, the 82541 device PHY has an unstable link with high jitter link partners. This issue is relevant only for shorter cable connections, where the cable length is approximately less than 20 meters. The instability is characterized with frequent link drops or high bit error rate if a valid link is present. On master mode the connection is stable and link is established and maintained.

Implication: An unstable and unreliable connection may be obtained when connected to high jitter link partners with short cable. For B0 steppings or earlier, the PHY default configuration is slave mode. Therefore, the problem may be observed if no action is taken.

For the B1 stepping and later versions, the PHY default is automatic, meaning it becomes either master or slave. Thus, the problem is only observed if the PHY was placed into slave mode as result of the Auto-Negotiation process.

Workaround: For proper link with the high jitter link partners, it is required to set the PHY to master mode via a software driver version that can force the PHY into master mode.

Status: Intel does not plan to resolve this erratum in the 82541 Gigabit Ethernet controller family.

48. Possible Ripple on 1.8V and 1.2V Regulator Outputs

Problem: The internal ground bounce that occurs when the 82541 drives the PCI bus can introduce ripple on the 1.2V and 1.8V linear voltage regulator (LVR) outputs. This ripple violates the published DC specification (nominal voltage of –7% and +5%).

Implication: The ripple of concern occurs at a frequency below 1 MHz. When these voltage levels are measured, higher frequency noise components will be seen super-imposed on the lower frequency (less than 1 MHz) ripple. These higher frequency glitches are unrelated to the LVR functionality and should be disregarded. When measuring this ripple, it is to recommended that the scope bandwidth is limited to the greatest extent to filter out noise greater than 1 MHz.

Under normal network data conditions (random data patterns), this ripple does not violate the current DC specification values. However, under heavy simultaneous switching loads presented over prolonged periods of time (such as sequential large packets with worst case data transition patterns received over the network), the ripple can violte the specified DC values. Worst case data patterns are those that cause the majority of 32 PCI data outputs to simultaneously switch from one to zero in a repeated pattern, such as FFFF FFFFh, 0000 0000h, FFFF FFFFh, 0000 0000h, etc.

Note: There have been no customer reports related to this ripple component. The specification violation has only been observed during testing using a SmartBits network exerciser to generate sustained worse case loads.

The 82541 can tolerate a periodic voltage variation beyond the existing DC specification to a degree specified in a revised DC and new AC ripple specification without impact to device functionality or reliability. If the ripple component exceeds the value of the new AC specification, decreased BER performance may result. The Ethernet link may also be reset, causing link to be lost and re-established.

Root Cause: Extreme switching (for example, sequences of sequential packets with worst case pattern type data) of the PCI data output buffers causes internal switching currents that disrupt the LVR reference voltage.

Workaround: There is no workaround for this switching noise when an internal LVR is used. If external voltage regulators are used, switching noise will not occur since the external regulators are not affected by the internal ground bounce on the LVR.

Status: The updated specifications are listed in the Specification Changes section of this document.

49. 82541 Gigabit Ethernet Controller Might Fail to Wake Up a System

Problem: An 82541 Gigabit Ethernet controller might fail to wake up a system upon receiving a “magic” packet.

Implication: Under extreme circumstances (approximately 1500 to 2000 continuous boots), an 82541 Ethernet controller might fail to wake up a system upon receiving and correctly identifying a magic packet from a LINK partner.

Workaround: Always send a second packet to wake the system up. If the first magic packet fails to wake up the system, then a second packet always succeeds. If the first magic packet wakes up the system, then hardware simply ignores the second packet.

Status: Intel does not plan to resolve this erratum in the 82541 Gigabit Ethernet controller family.

50. 82541EI Fails to Establish 1000Mbps Link When Connected Peer-to-Peer with Another 82541EI

Problem: When the 82541EI is connected peer-to-peer with another 82541EI, no 1000Mbps link is established and the link is then downgraded to 100Mbps. The default configuration of the 82541EI is to be a "slave" only on the physical link (in order to achieve better performance), and due to this, two EI devices connected peer-to-peer cannot establish 1000Mbps link (both can only be a slave). This is relevant only for devices that run with a default configuration without any Intel device drivers.

Implication: 82541EI devices connected in peer-to-peer connection, without an Intel device driver running on top of them, cannot establish 1000Mbps link. When using an Intel device driver, 1000Mbps link can be achieved, but with less performance than connecting the 82541EI to another link partner.

Workaround: To enable 1000Mbps link without an Intel device driver, the software running on top of the device should change the default configuration to enable the PHY to run in master mode.

Status: Intel resolved this in the PI stepping of the 82541 Gigabit Ethernet Controller.

51. Intermittent Issues with TCO Receive Packets in IPMI Mode (82541PI)

Problem: The TCO Receive FIFO is implemented as a pair of buffers utilized in an alternating fashion. Under a specific timing condition where a new packet arrives from the Ethernet for the TCO receive FIFO coincident with a previous TCO packet being read from the FIFO to the SMBus, logic tracking the occupied/empty state of the buffers can enter an inconsistent state. This problem does not occur if only a single TCO packet is passed through the TCO Receive FIFO at a time.

Implication: When the LAN controller is in this erratum state, symptoms may include (a) corrupted packets delivered to the SMBus, (b) packets received to the SMBus twice, or (c) a received TCO packet appearing to be "stuck" in the TCO Receive FIFO until a new TCO packet arrives. Most network operations are only mildly affected, as most network protocols allow for lost or late packets and support header/payload integrity checksums.

Workaround(s): To address this problem, a series of steps should be taken in BMC firmware:

- First, the BMC firmware should check integrity of all TCO packets received by checking the IP/UDP checksums and discarding any corrupted packets.
- Second, the BMC firmware should implement a "check for erratum state" function using the following conditions:
    a) Check to see if two sequential packets received are exact duplicates.

b) Attempt to check for "stuck" packets to determine whether a packet received has simply been delayed on the network versus "stuck" in the TCO Receive FIFO. The IPMI specification defines an 8 sequence-number window; received TCO packets exceeding that window may be good indications of being “stuck”. Depending upon application, BMC firmware may be able to implement additional mechanisms to detect when a TCO packet received from the LAN controller appears to be one that had been given up as “lost” on the network.

- Finally, upon detecting a likely "TCO erratum state”, BMC firmware should implement a specific "TCO Abort" operation on the SMBus to return the LAN controller from an erroneous state back to a normal, operational state without requiring a LAN controller reset. A "TCO Abort" operation is an intentionally abnormally terminated SMBus transaction. The specific TCO Abort transaction recommended by Intel consists of an N-byte SMBus write (N>1) to the LAN controller where the BMC only provides 1 byte of data before initiating a STOP.

  Note that issuing this “TCO Abort” operation while the LAN controller is in a normal, healthy operational state can in fact induce the erratum condition. Therefore, checks for the erratum condition should be considered carefully so as to avoid excessive TCO Aborts while the LAN device is in a healthy state. However, if the TCO Abort were to be errantly issued while the LAN controller is in a normal healthy state, and the erratum state were to be induced, it is expected that the erratum-check criteria would again detect & correct the state back to normal, healthy state.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82541PI Gigabit Ethernet Controller.

SPECIFICATION CLARIFICATIONS

1. (Deleted)

2. Crystal Specification Revised Due to Low Clock Drive Strength

Problem: The 25 MHz base clock may not oscillate when using crystals with high equivalent series resistance (ESR) parameter due to low drive strength of the crystal block. Thus, the Ethernet controller may not be identified on the system host bus due to the absence of the main 25 MHz clock.

In B1 silicon and earlier versions, it is required to use crystals with ESR less than or equal to 20 Ω and a capacitance load of 18 pF. This alleviates the problem by avoiding the required high drive strength of the crystal block.

B1 silicon and earlier versions also require using crystals with specific parameters. C0 silicon was improved to support a higher drive strength, which can provide support for use of crystals with ESR less than 50 Ω and a capacitance load of up to 24 pF.

Affected Specs: Intel Ethernet Controllers Timing Device Selection Guide, Application Note (AP-419).

3. External Oscillator Support Clarification

Problem: The supporting 82541 Ethernet controller documentation does not specify support of an external oscillator.

The 82541 clock input circuit is optimized for use with an external crystal. However, an oscillator may also be used for the 82541EI/GI and the 82541PI in place of a crystal with proper design considerations. The same circuit applies to the 82541EI and 82541GI. The latest 82540EP/82541 Family & 82562EZ(EX) Dual Footprint Design Guide and 82541 Datasheet should be consulted for further details.

Affected Specs: 82541 Family of Gigabit Ethernet Controller Datasheet, Revision 3.1; 82540EP/82541 Family & 82562EZ(EX) Dual Footprint Design Guide, Revision 2.0; Intel Ethernet Controllers Timing Device Selection Guide, Application Note.

4. Resistor Value Changes for 82541PI Stepping

Problem: The 82541PI (C0 stepping) has new I/O drivers have a lower internal pull-up resistance value than previous versions of the 82541. Thus, some designs will require a change to the value of the pull-down resistors,

On ball J4, the EE_MODE pin, use a recommended value of 100 Ω, instead of the1 K Ω used in previous 82541 steppings, if a MicroWire EEPROM is used in the current solution. There is no impact to designs using an SPI EEPROM.

On ball L13, the JTAG_TRST pin, use a recommended value of 100 Ω, instead of the1 K Ω used in previous 82541 steppings.

For 82541PI, verify vendor specifications to ensure that Vol is less than 0.7V on ball N10, EEDO, and ball P9, FLSH_SO/LAN_DISABLE#.

Affected Specs: For more information refer to the design schematics (design guide) and datasheet for the 82541 Ethernet Controller.

5. PCI-X Capability Register in PCI Configuration Space

Problem: The 82541 controller includes the PCI-X Capability register (capability ID = 0x07) in its PCI configuration space. If the system software were to look only at configuration space it might mistakenly determine that the controller was capable of operation in PCI-X mode, when in fact the 82541 does not support PCI-X mode.

Affected Specs: None.

6. 82541EI & 82547EI EEPROM Images Impact PHY Performance

Problem: Using outdated EEPROM images will result in poor PHY performance. The problem image has the following values for words 10-1f:

10	1F35	002A	0A00	0012	0C00	20DD	2222	2F90
18	0280	1F73	0098	1F72	3FB0	0009	1A00	3649

Implication: When using an EEPROM image that doesn't support proper PHY settings, the 82541EI will have performance issues on the external LINK (downshift to 100MB or high BER)

Workaround: Make sure to use the latest EEPROM image dated 3/28/2005 or later.

Status: Intel resolved this issue in a later version of the EEPROM image; please contact your Intel representative with the latest EEPROM image version.

DOCUMENTATION CHANGES

There are currently no documentation changes for the 82541 family.