82540EM Gigabit Ethernet Controller Specification Update

October 10, 2005

The 82540EM Gigabit Ethernet Controller may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

82540EM Gigabit Ethernet Controller Specification Update

Date of Revision	Description
April 1, 2004	Initial public release. Added Errata #23 and 24 and spec clarification #3.
August 3, 2004	Added Errata # 25, 26, and 27.
January 10, 2005	Added Spec Clarification #4. Removed Spec Change #1. Removed Spec Clarification # 1.
July 8, 2005	Removed Documentation Changes #8 and #10. Removed Spec Clarification #2. Removed the power table reference in Erratum #26. Corrected RMCP spelling in Erratum #25.
October 10, 2005	Added Errata #28.

PREFACE

This document is an update to published specifications. Specification documents for this product include:

- 82540EM Gigabit Ethernet Controller Datasheet, Intel Corporation.
- 82540EM Design Guide, Intel Corporation.
- 82551QM/82540EM Interchangeable LOM Design Application Note (AP-432), Intel Corporation.

This document is intended for hardware system manufacturers and software developers of applications, operating systems or tools. It may contain Specification Changes, Errata, and Specification Clarifications.

All 82540EM product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

NOMENCLATURE

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

COMPONENT IDENTIFICATION VIA PROGRAMMING INTERFACE

82540EM controller steppings will be identified by the following register contents:

Stepping	Vendor ID	Device ID	Revision Number
82540EM A0	8086h	100Eh	00h
82540EM A1	8086h	100Eh	01h
82540EM A2	8086h	100Eh	02h

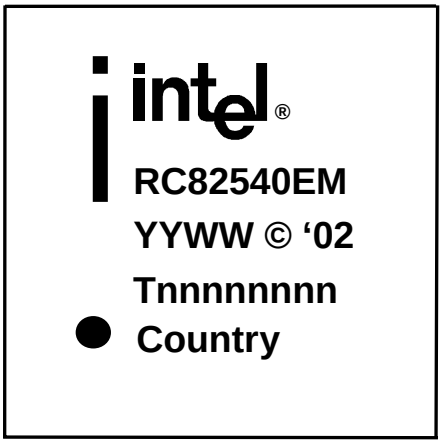
These devices also provide identification data through the Test Access Port.

GENERAL INFORMATION

This section covers the 82540EM device.

82540EM COMPONENT MARKING INFORMATION

Product	Stepping	QDF Number	Top Marking	Notes
82540EM	A0	Q 488	RC82540EM	Engineering Samples
82540EM	A1	Q 489	RC82540EM	Engineering Samples
82540EM	A2	Q 490	RC82540EM	Engineering Samples
82540EM	A2	-	RC82540EM	Production



SUMMARY TABLE OF CHANGES

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82540EM steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLES

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

No.	A0	A1	A2	Plans	SPECIFICATION CHANGES	Page	Notes
1	X	X	X	Doc Change	Specification Parameters for 1.5V Regulator Circuit Operation	8	-
2	X	X	X	Doc Change	Internal Pull-up Impedance Value	8	-
No.	**A0**	**A1**	**A2**	**Plans**	**ERRATA**	**Page**	**Notes**
1	X	-	-	Fixed	Collision/ASF/Manageability Data Re-Transmit Problem	9	-
2	X	-	-	Fixed	Transmit DMA Problem Due to Re-Transmit Timing Event	9	-
3	X	-	-	Fixed	DMA and ASF/Manageability Concurrency Problems	9	-
4	X	-	-	Fixed	MDI/MDIX Crossover Auto-Detection Not Working	10	-
5	X	X	-	Fixed	ASF/Manageability Transmit and Receive Not Functional in D3 State Without APM	10	-
6	X	-	-	Fixed	Wakeup Disable Control for TCO/Manageability Packets	10	-
7	X	-	-	Fixed	I/O Register Access Decoder	11	-
8	X	X	-	Fixed	ASF State Machines Out of Sync on Power Up	11	-
9	X	X	-	Fixed	Short Packets Under Heavy Transmit Load	11	-
10	X	X	-	Fixed	LED[0] (LINK_UP) Not Programmable	11	-
11	X	X	X	NoFix	1.5V Regulator Control Circuit Start Up	11	-
12	X	X	-	Fixed	Retransmit Requests for 10Mb Half-Duplex Collisions	12	-
13	X	X	-	Fixed	Excessive PCI Bus Hold Time	13	-
14	X	X	-	Fixed	SMBALRT# Output Driven in ASF Mode	13	-
15	X	X	X	NoFix	ASF Lockup Upon Resetting MAC	13	-
16	X	X	X	NoFix	MWI Transactions May Terminate on Non-Cacheline Boundary	13	-
17	X	X	-	Fixed	Some LEDs Asserted in D3 State with Wakeup and Manageability Disabled	14	-
18	X	X	X	NoFix	Master-Aborts with Some Chipsets During Driver-Initiated Controller Reset	14	-
19	X	X	X	NoFix	LSO Premature Descriptor Write Back	14	-
20	X	X	X	NoFix	XOFF from Link Partner can Pause Flow-Control (XON/XOFF) Transmission	15	-
21	X	X	X	NoFix	Transmit Descriptor use of RS for non-data (Context & Null) Descriptors	15	-
22	X	X	X	NoFix	Intermittent Issues with TCO Receive Packets in IPMI Mode	15	-
23	X	X	X	NoFix	Message Signaled Interrupt Feature May Corrupt Write Transactions	16	-
24	X	X	X	NoFix	Wakeup Packet Memory (WUPM) cleared upon reset	16	-
25	X	X	X	NoFix	Unexpected RCMP ACK packets in ASF mode	16	-
26	X	X	X	NoFix	Exceeding PCI Power Management Specification Limit of 375mA current during reset and power state transitions	16	**-**
27	X	X	X	NoFix	Memory Access must be enabled in order to Read Device Registers in I/O mode	17	**-**
28	X	X	X	NoFix	Legacy Transmit Descriptor Write-Back May Occur Before the Packet Data Associated with the Descriptor is Fetched	17	New

No.	A0	A1	A2	Plans	SPECIFICATION CLARIFICATIONS	Page	Notes
1	X	X	X	Doc Change	Advertisement of PCI-X Capability	18	-
2	X	X	X	Doc Change	TTL inputs not 5V tolerant	18	-
-	-	-	-	-	-	-	-
No.	**A0**	**A1**	**A2**	**Plans**	**DOCUMENTATION CHANGES**	**Page**	**Notes**
1	X	X	X	Doc Change	82540EM Controller Errors in Pin Number to Signal Mapping Table	19	-
2	X	X	X	Doc Change	82540EM Controller Error in Pin Description Tables	20	-
3	X	X	X	Doc Change	Errors in 82551QM/82540EM Controllers Combined Reference Schematics	20	-
4	X	X	X	Doc Change	82540EM Controller May Need Larger EEPROM	20	-
5	X	X	X	Doc Change	82540EM Controller Package Information	21	-
6	X	X	X	Doc Change	Omissions in 82540EM Controller Pin Description Table	21	-
7	X	X	X	Doc Change	Impedance Compensation Resistor Connections	21	-
8	-	-	X	Doc Change	Automatic EEPROM Reload of Hardware Defaults Following Software Reset	22	-

SPECIFICATION CHANGES

1. Specification Parameters for 1.5V Regulator Circuit Operation

Problem: Correct operation of the 1.5V regulation circuit depend on several factors: presence of minimum leakage current from the CTRL_15 output, supported min/max values for external PNP transistor gain (Beta), and the generation of sufficient 1.5V rail current/voltage to supply the regulator circuit. These parameters relate to Erratum #11, "1.5V Regulator Start Up."

The minimum leakage current provided from the CTRL_15 regulator control pin during startup will be 0 μA. Maximum leakage current when the regulator circuit is operating and providing minimum transistor base current is 1 μA.

The minimum 1.5V rail current (PNP collector current) required for the regulator control circuitry to start up reliably is 5 mA. The system designer must ensure that the total collector current, $I_C = (I_B * Beta)$, satisfies this requirement at startup conditions. For the recommended bias resistor R3 value of 30K ohm, the selected PNP device must exhibit minimum gain (Beta) of approximately 75 during operation at <5 mA and V_{CE} of approximately 1.0-1.8V at the worst-case temperature of 0°C.

To ensure proper 1.5V rail regulation during operation, the system designer must further ensure that the highest-gain PNP transistors used do not produce I_C currents significantly in excess of the 1.5V actual power consumption (approximately 10 mA at $D3_{cold}$ with no wakeup/SMBus, 30 mA with WOL/SMBus enabled). For the recommended bias resistor R3 value of 30K ohm and recommended SMBus-enabled configuration, the selected PNP device must exhibit maximum H_{FE} gain (Beta) of no more than 275 during high-temperature operation (70°C) to source less than 30 mA of current.

Affected Docs: 82540EM Gigabit Ethernet Controller Preliminary Datasheet and Software Design Guide Rev. 0.5.

2. Internal Pull-up Impedance Value

Problem: The 82540EM Gigabit Ethernet Controller Preliminary Datasheet indicates the nominal impedance for I/O cell internal pull-up devices is 50KΩ. This specification is incorrect. The actual internal pull-up impedance is nominally 20KΩ, minimum 15KΩ and maximum 30KΩ.

Affected Docs: 82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide.

ERRATA

1. Collision/ASF/Manageability Data Re-Transmit Problem

Problem: Re-transmission attempts due to link up/down state transitions or due to collisions in half-duplex mode will have problems due to a logic error in the 82540EM Controller manageability subsystem.

When the problem occurs, an arbiter selecting transmit packets from ASF/management data and regular transmit DMA sources will “lock on” to the data source for an extended sequence of transmit data. There are three problem scenarios:

- The controller is operating with ASF/management transmission and regular data transmission enabled concurrently. In this case, the behavior can appear as a transmit hang.
- The controller is operating with only ASF/management transmission enabled. In this case, the controller will successfully transmit all ASF/management packets. However, an ASF/management packet may occasionally be partially transmitted as a short fragment before being successfully re-transmitted in its entirety.
- The controller is operating in half duplex mode for regular data transmission and collisions occur. In this case, the behavior can appear as a delayed transmit hang after 64Kbytes of successful re-transmission.

Implication: If a lockup occurs, either a hardware or software reset will be required.

Workaround: Avoid operating in half duplex mode. In particular, run ASF/manageability functions with a stable, full-duplex link to avoid re-transmit events.

Implement a software timer to check for a stopped DMA transmit path. If a long interval elapses without expected packet transmission, reset the device.

Status: Intel resolved this erratum in the A1 stepping of the 82540EM Gigabit Ethernet Controller.

2. Transmit DMA Problem Due to Re-Transmit Timing Event

Problem: The 82540EM Controller permits DMA transfers to the transmit FIFO even if link is down. At the outbound end of the FIFO, an arbiter buffer selects whether to transmit either regular FIFO packet data or ASF/management data. If a new packet becomes available to the arbiter for transmission on the same cycle as a link up or collision-induced re-transmission, the state machine logic may fail.

The problem will appear externally as a transmitter lockup. It is possible that one or more erroneous packets will be transmitted before the lockup.

The problem can also occur if the link up or collision-induced retransmission occurs on exactly the same cycle that a new ASF/management packet becomes available for transmission.

Implication: The likelihood of new packet availability at exactly the same moment as a link status or collision induced re-transmit event may be low in some systems. The likelihood may be especially low for ASF/management packet availability. The frequency of lockup will increase if the overall DMA transmit rate increases or if either collisions or link change events increase.

If a lockup occurs, either a hardware or software reset will be required.

Workaround: Implement a software timer to check for a stopped DMA transmit path. If a long interval elapses without expected packet transmission, reset the device. Restrict concurrent ASF operations to stable full-duplex link operation.

Status: Intel resolved this erratum in the A1 stepping of the 82540EM Gigabit Ethernet Controller.

3. DMA and ASF/Manageability Concurrency Problems

Problem: The 82540EM Controller is anticipated to exhibit problems when DMA and ASF/management operations occur simultaneously. The following situations are expected to be problematic:

- ASF/management packet becomes available for transmit while an ordinary DMA packet transmission is in progress.
- A hardware-generated XON or XOFF flow-control request occurs while an ASF/management packet transmission is in progress

The problem will result in transmitter lockup, manifested either in the regular DMA transmit path or in the ASF/TCO controller.

Implication: If lockup occurs, either a hardware or software reset will be required.

The rate of transmitter lockups will depend on the rate of event alignment and will increase under stress tests. Lockups due to XON/XOFF generation are expected to be less likely in routine traffic due to the infrequent nature of both XOFF and ASF/management transmits.

Workaround: Implement a software timer to check for a stopped transmitter on both the regular DMA and management paths. If a long interval elapses and transmit progress has not occurred, perform a software reset of the device. If regularly occurring manageability functions do not increment a statistics register, also perform a software reset.

Consider disabling ASF manageability operations while the operating system is running, restricting ASF functions to pre-boot and suspended states only. XON/XOFF flow control generation may be disabled through register programming.

Status: Intel resolved this erratum in the A1 stepping of the 82540EM Gigabit Ethernet Controller.

4. MDI/MDI-X Crossover Auto-Detection Not Working

Problem: The 82540EM Controller feature for automatically detecting crossover cables fails to clearly detect the cable type. If a crossover cable is used when it is not required, the controller will not establish link.

Implication: Crossover cables to hubs and switches cannot be used unless the transmit/receive pairs are known to be crossed at the link partner. Using MII management registers to manually set the specific MDI or MDI-X configuration corresponding to the cable will allow link to be successfully established.

Workaround: Use straight-through cables to hubs and switches, unless the hub or switch port is crossed. Intel's driver code will disable auto MDI-X detection/correction and configure the 82540EM Controller for fixed MDI behavior. Alternatively, MII Management registers can be used to manually configure a particular forced MDI/MDI-X configuration. To do so, bits 6:5 of MII Register 16 should be set to 00 (for uncrossed MDI) or 01 (for crossed MDI-X). Follow this operation with a write to MII Register 0 with bit 15 set to 1 in order to reset the PHY.

Status: Intel resolved this erratum in the A1 stepping of the 82540EM Gigabit Ethernet Controller.

5. ASF/Manageability Transmit and Receive Not Functional in D3 State without APM

Problem: If the controller is in the Dr, D0u, or D3 power states, manageability functions do not work unless APM is enabled. Without power management wake-up enabled, part of an internal clock tree is becomes disabled.

Implication: Power management wake-up must be enabled if low power and pre-boot manageability operation is desired.

Workaround: Enable APM in the EEPROM image by setting bit 2 of the Management Control Word (word 23h) to 1. If APM wake-ups from D3 state are not desired, ignore or mask APM_WAKEUP, and disable APM wakeups from being promoted to PME# assertions by programming bit 15 of the EEPROM Initialization Control Word 2 (word 0Fh) to zero.

Status: Intel resolved this erratum in the A2 stepping of the 82540EM Gigabit Ethernet Controller.

6. Wake-Up Disable Control for TCO/Manageability Packets

Problem: The 82540EM Controller A0 stepping did not implement the RMCP and Ignore TCO wake-up disable bits planned for the Wakeup Filter Control Register (WUFC). These bits were intended to provide control over whether specific packet types that are received and detected as TCO/management packets per the Manageability Control Register (MANC) settings can initiate ACPI wakeup events.

Implication: If ACPI wakeups that overlap with TCO/Management packets are enabled, the TCO/management packets (directed RMCP and/or ARPs) will cause wakeup events from D3 state, even if these packets are expected to be received and serviced quietly by the TCO controller. It may not be possible to configure ACPI wakeups to occur on a specific desired subset of non-TCO packets.

Workaround: If ACPI wakeups due to TCO/management packets are unwanted during D3 state ASF/Manageability operation, disable all relevant bits associated with Individual Address (IA) match conditions (EX, BC, MC) as well as ARP and Directed IP match conditions (ARP, IPV4) in the Wakeup Filter Control Register (WUFC).

Status: Intel resolved this erratum in the A1 stepping of the 82540EM Gigabit Ethernet Controller. The Ignore TCO bit was implemented to allow all packets classified as TCO packets to be specifically excluded from wake-up generation. Intel has determined that the RMCP bit is an unnecessary control and did not implement it.

7. I/O Register Access Decoder

Problem: The I/O Base Address Register indicates that it will decode a 32-byte I/O register address space. However, the 82540EM Controller actually decodes a 64-byte window, ignoring the least significant bit (Bit 5) of the programmed base address.

Implication: The 82540EM Gigabit Ethernet Controller may have address conflicts with other devices. This behavior is dependent on how the system BIOS enumerates the PCI bus devices. In a LAN on motherboard implementation, the system may work properly until one or more add-in cards are introduced to the system.

Workaround: If I/O devices appear to be working incorrectly due to address conflicts, check to see if a manual BIOS or operating system configuration will overcome the problem. If the conflict occurs between an 82540EM controller LOM port and an add-in adapter, consider removing the adapter card.

Status: Intel resolved this erratum in the A1 stepping of the 82540EM Gigabit Ethernet Controller. The controller now both advertises and decodes a 64-byte I/O space.

8. ASF State Machines Out of Sync on Power Up

Problem: Upon power up, two state machines in the ASF logic may intermittently be out of sync, causing the ASF core to be locked up. The problem is due to an internal signal that does not remain valid long enough to assure sampling.

Implication: If the ASF state logic is deadlocked, no ASF/manageability operations can occur.

Workaround: Reset the ASF core prior to first use. For OS-present ASF operation, the reset code can be in the ASF driver. For pre-OS ASF operation, the reset code can be placed in the system BIOS.

To perform the reset operation, issue an SMBus Byte Write with the following parameters:

- SMBus Address = Configured ASF address (typically C8h or 64h)
- Command Code = F3h (selects the register)
- Data value = 80h (selects the software reset bit)

Status: Intel resolved this erratum in the A2 stepping of the 82540EM Gigabit Ethernet Controller.

9. Short Packets under Heavy Transmit Load

Problem: Packets containing 48 or fewer bytes can lock up the transmitter, especially at 10 Mbps and 100 Mbps. The problem occurs because a very small packet can fit completely in a shallow buffer between the DMA unit and the MAC while the previous packet is being transmitted.

Implication: The transmitter lock up has only been observed with ARP request packets transmitted by the regular software driver. Note that later in the pipeline the controller pads all packets to the minimum IEEE length of 64 bytes. Transmission of short packets from the SMBus or ASF logic is not affected by the problem.

Workaround: Driver software will be modified to pad packets to at least 49 bytes.

Status: Intel resolved this erratum in the A2 stepping of the 82540EM Gigabit Ethernet Controller.

10. LED [0] (LINK_UP) Not Programmable

Problem: The programming logic for the LED [0] pin is not properly connected. The pin always indicates whether link is present or not, regardless of programming.

Implication: Software programming or EEPROM configuration is not available on the LED [0] pin.

Workaround: If programmable LED functions are desired, use LED [1] through LED [3]. LED [2] can also be configured through bits in the EEPROM.

Status: Intel resolved this erratum in the A2 stepping of the 82540EM Gigabit Ethernet Controller.

11. 1.5V Regulator Control Circuit Start Up

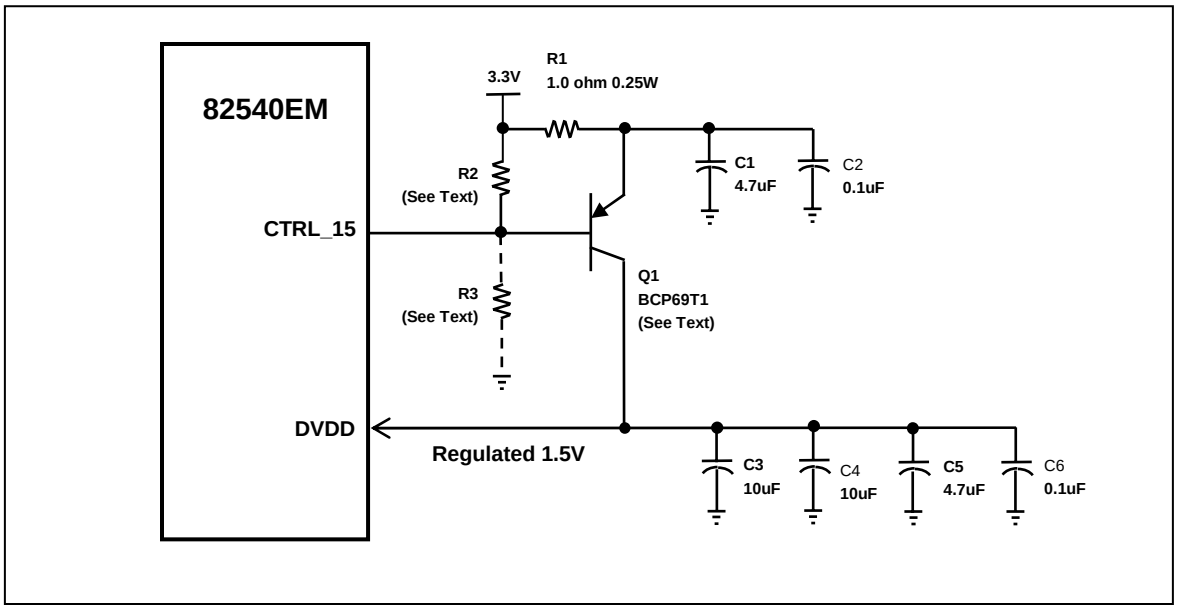
Problem: The 82540EM product contains on-chip LDO voltage regulation controllers for both 1.5V and 2.5V. The 1.5V regulator control output, CTRL_15, sometimes powers up in a high impedance state due to a digital portion of the feedback-control circuit which requires 1.5V to be present to operate correctly. The rate of occurrence of this problem may appear to vary from device to device or with different PNP transistors.

Implication: When drive is absent on the CTRL_15 output, only leakage current from the CTRL_15 output will be present. Depending on the amount of leakage current and the gain (Beta) of the external PNP transistor, there may be

insufficient collector current ($I_C = I_B$ * Beta) to adequately supply the 1.5V rail, and the 1.5V regulator circuit may not turn on. The 1.5V rail requires a minimum collector current of 5 mA to be generated and a 1.5V rail voltage of at least 600 mV to ensure that the digital portion of the circuit turns on correctly.

When the 1.5V regulator control output fails, the 2.5V regulator control output(s) may also fail, driving the 2.5V supply toward either 0V or the 3.3V rail. The absence of one or both of the 1.5V and/or 2.5V supplies prevents the Ethernet controller from operating correctly.

Workaround: Refer to the figure below. The regulator control output is Ball P11 on the 82540EM controller. Intel's original reference designs showed two external resistors, R1 and R2, in this circuit. The workaround is to completely remove R2 (shown in reference schematics as 5.1K) and place another resistor, R3, to connect between the CTRL_15 output and ground, in order to create additional base current and ensure sufficient collector current is generated.



Due to variations in PNP minimum/maximum transistor gain, this circuit must adhere to specific requirements for the PNP transistor, R3 resistor value, and configuration of the 82540EM controller. Follow **workaround instructions** in Technical Advisory TA-147, "Possibility of 1.5 Voltage Regulator Failures on 82540EM LOM Designs." **Special Note:** Workarounds differ among the 82540EM, 82545EM and 82546EB controllers and each controller has a separate technical advisory.

Systems that generate 1.5V without using the Ethernet controller's onboard regulator control (at a central power supply, for example) do not need a workaround. No changes are required for the 2.5V regulator circuit.

Specifications for minimum CTRL_15 leakage current, min/max supported ranges for PNP transistor gain (Beta), 1.5V rail input voltage/current requirements, and the lowest supported value for resistor R3 will be provided in the 82540EM Gigabit Ethernet Controller Datasheet and Hardware Design Guide. See Specification Change #2 of this document.

Status: This erratum has been fixed in a compatible, newer device, the 82540EP GbE Controller.

12. Retransmit Requests for 10Mb Half-Duplex Collisions

Problem: In 10 Mb operation, data transfer handshake synchronization from the DMA clock domain into the transmit MAC clock domain can take more time than it takes for the DMA clock domain to observe a collision event and re-try the transmit request. If a collision occurs at the exact moment that a data transfer from the DMA to MAC occurs, the discrepancy in synchronization delays can cause the logic to become confused about which data has been transferred.

Implication: When the device confuses the order of the data events, the transmitter will lock up. The long synchronization delays inherent in 10 Mb mode of operation can readily cause this situation.

Workaround: Operate the 82540EM controller in full duplex mode. If half duplex operation is required, run the device at the 100Mb speed.

Status: Intel resolved this erratum in the A2 stepping of the 82540EM Gigabit Ethernet Controller.

13. Excessive PCI Bus Hold Time

Problem: The PCI Local Bus Specification calls for 0 ns input hold time on the address/data bus (AD [63:0]) and the byte enables (CBE [7:0] #). However, the 82540EM controller requires approximately 3.5 ns input hold time for 33MHz operation and approximately 1 ns input hold time for 66 MHz operation. This problem is due to incorrect hook-up of the clocks and the affected I/O cells.

Implication: The controller may read data incorrectly, causing parity errors, erratic Ethernet port operation, and possible system lockups.

The severity of the problem depends on several factors, varying from system to system. In some designs the bridge connected to the 82540EM controller will provide adequate hold time and problems will not be seen. If the 82540EM device is on an add-in board, the problem may vary from slot to slot.

Workaround: Operate the 82540EM controller with 66 MHz timings, since most bridge devices provide enough level of margin to the PCI hold time to meet the 82540EM controller's 1 ns requirement. There are two ways to force the controller to use 66 MHz timings:

- Place the 82540EM controller on a 66 MHz PCI bus, with the M66EN (66 MHz Enable) signal connected to the system in the usual way. If the device is on an add-in card, place the card on a 66 MHz slot.
- Leave the 82540EM controller on a 33 MHz PCI bus, but break the connection between the controller's M66EN signal (Ball C2) and the system. Use a pull-up resistor to connect the controller's M66EN signal to the 3.3V supply. The value of the pull-up resistor is not critical and can be as high as 100K ohms.

Status: Intel resolved this erratum in the A2 stepping of the 82540EM Gigabit Ethernet Controller. Be sure the controller's M66EN signal is connected to the system for A2.

14. SMBALRT# Output Driven in ASF Mode

Problem: The SMBALRT# output signal has an additional function as a PCI_POWER_GOOD input in ASF mode operation. However, the controller does not disable the SMBALRT# open drain output and contention between the external PCI_POWER_GOOD signal and the internal SMBALRT# signal can result.

Implication: The Ethernet controller drives SMBALRT# low during communication between the ASF controller and the main LAN controller logic. Depending on the drive strength of the external PCI_POWER_GOOD signal (or the value of a pull-up resistor attached to the ball), the ASF controller may not observe PCI_POWER_GOOD asserted.

If PCI_POWER_GOOD cannot be observed following "OS Hang" event detection, the ASF controller may fail to observe reset on the PCI bus, continuing to perform remote control operations such as EEPROM reloads.

Workaround: Drive the PCI_POWER_GOOD input from a low impedance source (25 ohms or less).

Status: Intel resolved this erratum in the A2 stepping of the 82540EM Gigabit Ethernet Controller.

15. ASF Lockup upon Resetting MAC

Problem: The ASF logic has a handshake problem at the expiration of its watchdog timer. When the ASF block attempts to reset the MAC, an ASF lockup can occur.

Implication: The "Force TCO MAC Reset" operation of the ASF controller cannot be used.

Workaround: Intel has workaround ASF software and modified EEPROM settings to accompany the workaround. The workaround disables MAC resets by the ASF logic (EEPROM Word 23h, Bit 2) and enables the ASF logic to request ARP packets following the watchdog event.

Status: This erratum has been fixed in a compatible, newer device, the 82540EP GbE Controller.

16. MWI Transactions May Terminate on Non-Cacheline Boundary

Problem: When PCI MWI (Memory Write Invalidate) transactions are enabled, the Ethernet controller will use MWI opcodes whenever possible for highest bus efficiency. For receive packets that do not neatly align to cacheline boundaries, the 82540EM device may continue an MWI burst to end-of-packet, then disconnect at the end-of-packet, resulting in the transfer of a partially filled cacheline in spite of the MWI operation.

Implication: Some chipsets may have a problem dealing with prematurely-terminated MWI transactions. One legacy PCI chipset was observed to clear the entire cacheline in memory, leading to packet corruption. Contemporary chipsets were observed to handle the transaction as follows:

- Treat it like an ordinary Memory Write (MW) transaction, without data errors, or

- Pad the remainder of the cacheline with random data. Data errors do not occur because the entire packet is written correctly to the receive buffer memory and the MWI burst remains within the allocated receive buffer region.

Workaround: For systems with chipsets that do not tolerate partially filled cachelines, disable the MWI opcode. The 82540EM controller will use MW operations instead.

Status: This erratum has been fixed in a compatible, newer device, the 82540EP GbE Controller.

17. Some LEDs Asserted in D3 State with Wakeup and Manageability Disabled

Problem: When the controller is in a D3 state (system suspended) with manageability and wake-ups disabled, the clock circuit used for some of the LED sources is stopped. As a result, some of the LED's can potentially exhibit unusual behavior in this configuration. The LED's may remain asserted in this D3 state, despite a change in the state/status of the LED source, due to the lack of clock to the circuit. The following LED indications are affected: for flow-control, full-duplex, collision, activity, link, and activity/link.

Implication: Configurations other than Wake on LAN configurations will encounter this behavior.

Workaround: Enabling wake-on-LAN or SMBus manageability ensures that the clock circuits are not stopped in D3 state and the LED indications remain valid.

Status: Intel resolved this erratum in the A2 stepping of the 82540EM Gigabit Ethernet Controller.

18. Master-Aborts with Some Chipsets during Driver-Initiated Controller Reset

Problem: The 82540EM Gigabit Ethernet Controller implements a software-Initiated device reset function through its control register space (CTRL Register Bit 31). This software-initiated reset re-initializes all functional state of the controller except for PCI/PCI-X configuration. When the reset is written, the controller requires a few internal clock cycles to complete the reset operation. During this brief time, it will not respond to additional register accesses.

Some PCI/PCI-X bridge components implemented with internal 64-bit architectures may initiate an additional zero byte write immediately following a 32-bit write to the device CTRL register. This zero byte write is essentially padding for a 64-bit transaction. In cases where the CTRL register access performs a software reset of the controller, the zero byte operation may encounter a master-abort due to the controller reset in progress.

Implication: In most system configurations, a master-abort on an outbound 0-byte write operation will not result in any adverse system behavior, though the event may be logged at either the chipset bridge or operating system level.

If the bridge/chipset is configured to promote the master-abort to a Non-Maskable-Interrupt (NMI) **and** the operating system cannot discern and handle NMI events, then a fatal operating system error may occur.

Workaround: The 82540EM controller can only be accessed using DWord (32-bit) software operations; since the potential zero byte write immediately following a device CTRL register write is a hardware event "created" by the chipset bridge components, no software mechanism can be used to eliminate the 0-byte write operation.

When an operating system is incapable of handling the NMI event, the chipset bridge should be configured to avoid promoting this master-abort to a fatal NMI event. Alternatively, the software-initiated device reset may be performed using an I/O access in place of a memory-mapped device access. The latter solution is effective if master-aborts on I/O writes do not result in NMI.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82540EM Gigabit Ethernet Controller.

19. LSO Premature Descriptor Write Back

Problem: For large send fetches ONLY (not normal or jumbo frames) the internal DMA engine will decompose the large-send data fetch into a series of individual requests that are completed sequentially. When all read data associated with the first internal DMA request has been fetched, the descriptor is flagged as ready for write back. Though all data associated with the entire LSO descriptor will eventually be fetched, the descriptor write back may occur prematurely. The device should wait until all bytes associated with the data descriptor have been completely fetched before writing back the transmit descriptor.

Implication: Due to premature write back, an operating system may release and reallocate the buffer, potentially causing buffer re-use and transmission of incorrect data.

Workaround: Utilize a second descriptor to point to the last four bytes of the large-send transmit data, and ensure that the buffer is not freed to the operating system/application until the second descriptor has been marked as complete via a status write back operation.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82540EM Gigabit Ethernet Controller.

20. XOFF from Link Partner can Pause Flow-Control (XON/XOFF) Transmission

Problem: When the 82540EM transmitter is paused (by having received an XOFF from link partner), not only is the transmit of normal packets paused, but also of outbound XON/XOFF frames resulting from Receive Packet Buffer levels and Flow-Control Thresholds. Normally, partner's XOFF packets only pause the LAN controller for a finite time interval, after which outbound XON/XOFF's due to Receive Packet-Buffer fullness are again permitted to be sent.

Implication: If the transmitter is paused when a Receive FIFO XOFF threshold is reached, the transmission of XOFF frames does not occur and Receive FIFO overrun may potentially occur, resulting in lost packets. This is only expected to be seen with an abnormally high pause time from link partner's XOFF packet(s).

Workaround: Receive Flow-Control Thresholds may be tuned/lowered based on the expected maximum pause interval expected from link partner's XOFF packet in order to minimize the likelihood of Receive FIFO overruns.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82540EM Gigabit Ethernet Controller.

21. Transmit Descriptor use of RS for non-data (Context & Null) Descriptors

Problem: Due to an internal logic error in the descriptor internal queue, if the internal descriptor queue becomes completely full of pending descriptor status write backs, the descriptor logic may issue a write back request with an incorrect write back amount. The internal descriptor queue may accumulate pending write backs if transmit descriptors that do not directly refer to transmit data buffers (e.g. context or Null descriptors) are submitted with a status-write back request (RS asserted) and legacy write back (status byte write back only) is utilized.

Implication: Due to the invalid internal write back request size, the PCI logic may hang.

Workaround: Ensure that status-write back reporting (RS) is not set on context or Null descriptors. Alternatively, utilize full-descriptor write backs (TXDCTL.WTHRESH >= 1). The former workaround is the recommended alternative.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82540EM Gigabit Ethernet Controller.

22. Intermittent Issues with TCO Receive Packets in IPMI Mode

Problem: The TCO Receive FIFO is implemented as a pair of buffers utilized in an alternating fashion. Under a specific timing condition where a new packet arrives from the Ethernet for the TCO receive FIFO coincident with a previous TCO packet being read from the FIFO to the SMBus, logic tracking the occupied/empty state of the buffers can enter an inconsistent state. This problem does not occur if only a single TCO packet is passed through the TCO Receive FIFO at a time.

Implication: When the LAN controller is in this erratum state, symptoms may include (a) corrupted packets delivered to the SMBus, (b) packets received to the SMBus twice, or (c) a received TCO packet appearing to be "stuck" in the TCO Receive FIFO until a new TCO packet arrives. Most network operations are only mildly affected, as most network protocols allow for lost or late packets and support header/payload integrity checksums.

Workaround(s): To address this problem, a series of steps should be taken in BMC firmware:

- First, the BMC firmware should check integrity of all TCO packets received by checking the IP/UDP checksums and discarding any corrupted packets.
- Second, the BMC firmware should implement a "check for erratum state" function using the following conditions:

  a) Check to see if two sequential packets received are exact duplicates.

  b) Attempt to check for "stuck" packets to determine whether a packet received has simply been delayed on the network versus "stuck" in the TCO Receive FIFO. The IPMI specification defines an 8 sequence-number window; received TCO packets exceeding that window may be good indications of being "stuck". Depending upon application, BMC firmware may be able to implement additional mechanisms to detect when a TCO packet received from the LAN controller appears to be one that had been given up as "lost" on the network.

- Finally, upon detecting a likely "TCO erratum state", BMC firmware should implement a specific "TCO Abort" operation on the SMBus to return the LAN controller from an erroneous state back to a normal, operational state without requiring a LAN controller reset. A "TCO Abort" operation is an intentionally abnormally terminated SMBus transaction. The specific TCO Abort transaction recommended by Intel consists of an N-byte SMBus write (N>1) to the LAN controller where the BMC only provides 1 byte of data before initiating a STOP.

  Note that issuing this "TCO Abort" operation while the LAN controller is in a normal, healthy operational state can in fact induce the erratum condition. Therefore, checks for the erratum condition should be considered carefully so as to avoid excessive TCO Aborts while the LAN device is in a healthy state. However, if the TCO Abort were to be errantly issued while the LAN controller is in a normal healthy state, and the erratum state were to be induced, it is expected that the erratum-check criteria would again detect & correct the state back to normal, healthy state.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82540EM Gigabit Ethernet Controller.

23. Message Signaled Interrupt Feature May Corrupt Write Transactions

Problem: The problem is with the implementation of the Message Signaled Interrupt (MSI) feature in the Ethernet controller. During MSI writes, the controller should use the MSI message data value in PCI configuration space.

At the same time, for normal write transactions (received packet data and/or descriptor writebacks), the controller temporarily stores the data for write transactions in a small memory until it is granted ownership of the PCI bus. The error condition occurs when during the MSI operation the controller incorrectly pulls data from the memory storing the data waiting to be written. If there are any write transactions waiting when this occurs, these transactions may become corrupted. This, in turn, may cause the network controller to lock up and become unresponsive.

Implication: If the affected products are used with an OS that utilizes Message Signal Interrupts and no accommodations are made to mitigate the use of these interrupts, data integrity issues may occur.

Workaround: For PCI systems, advertisement of the MSI capability can be turned off by setting the MSI Disable bit in the EEPROM (Init Control Word 2, bit 7).

Status: Intel does not plan to resolve this erratum in a future stepping of the 82540EM Gigabit Ethernet Controllers.

24. Wakeup Packet Memory (WUPM) cleared upon reset

Problem: The 82540EM specifications state that the Wakeup Packet Memory (WUPM) is not cleared on any reset. This is incorrect. Any reset or power-state transition will clear the contents of these registers.

Implication: Because a power-state transition takes place on wakeup, the Wakeup Packet Memory will always be cleared before it can be read by software. This makes the memory effectively unable to provide the capability for inspecting the wakeup packet content.

Workaround: There is no workaround. WUPM will be considered to be defeatured for the affected controllers.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82540EM Gigabit Ethernet Controllers.

25. Unexpected RMCP ACK packets in ASF mode

Problem: According to the RMCP protocol, the response to all RMCP commands (except ACK) should be an RMCP ACK packet. In ASF mode, the Ethernet Controller responds to RMCP ACK packets with a second ACK.

Implication: Any management software should be aware of this behavior and not respond to the additional RMCP ACK packets.

Workaround: None.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82540EM Gigabit Ethernet Controllers.

26. Exceeding PCI Power Management Specification Limit of 375mA current during reset and power state transitions

Problem: During resets and power state transitions the controller may briefly draw more than 375 mA of current as the digital signal processors in the PHY attempt to converge. The excessive current draw persists for approximately 100 milliseconds.

Implication: If an application has current limiting circuitry in place, the Ethernet Controller may trigger these safeguards in power-up or during transitions between D0 and D3 power states.

Workaround: None.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82540EM Gigabit Ethernet Controllers.

27. Memory Access must be enabled in order to Read Device Registers in I/O mode

Problem: The Ethernet controller will not respond to I/O transaction after a reset until its Memory Access Enable (MAE) bit has been set.

Implication: Attempts to access the Ethernet controller via I/O transactions without the MAE bit set will result in a master abort on the PCI bus.

Workaround: In order to access registers on the Ethernet Controller using I/O mode, both the I/O Access Enable and the Memory Access Enable bits in PCI configuration space must be set.

Status: Intel has resolved this erratum in the 82540EP Gigabit Ethernet Controller.

28. Legacy Transmit Descriptor Write-Back May Occur Before the Packet Data Associated with the Descriptor is Fetched

Problem: If a legacy transmit operation directly follows a TCP Segmentation Offload transmit operation, the logic may incorrectly associate the successful completion of the TSO transmit with the next descriptor. If the next descriptor is a legacy descriptor, under certain timing scenarios it is possible for the legacy descriptor to be incorrectly written back to host memory with the DD bit set. This might occur even though the packet data for the legacy descriptor has not yet been fetched.

Implication: Due to the premature write back, an operating system may release and reallocate the transmit buffer, potentially causing buffer re-use or transmission of incorrect data.

Workaround: Utilize at least two descriptors for any legacy transmit operation. Do not reallocate any buffers associated with the transmit operation until the last descriptor has been written back.

Status: Intel does not plan to resolve this erratum in a future stepping of the 82540EM Gigabit Ethernet Controller.

SPECIFICATION CLARIFICATIONS

1. Advertisement of PCI-X Capability

Problem: The Ethernet controller includes the PCI-X Capability register (capability ID = 0x07) in the list of Capabilities Registers of its PCI configuration space. If the system software were to look only at configuration space it might mistakenly determine that the controller was capable of operation in PCI-X mode, when in fact, it does not.

According to PCI-X specification, all hardware-level negotiation of PCI vs. PCIX capability is performed without software intervention via each bus component's hardware-level assertion on the PCIXCAP signal. As the 82540 are PCI-only devices, design applications of the 82540 must connect PCIXCAP correctly so as to indicate PCI-only capability during the hardware-level negotiation of bus mode. Correct application of the 82540 will always result in PCI mode bus operation, regardless of the device's advertisement of PCI-X capabilities to software.

2. TTL inputs not 5V tolerant

Problem: The TTL inputs on the Ethernet controller are not 5V tolerant. If these inputs are connected to 5V, then damage to the controller is likely to occur. TTL inputs include the JTAG interface pins, the FLASH interface pins, the EEPROM interface pins, the LED pins, the software definable pins, and the LAN_PWR_GOOD pin.

Affected Specs: 82540EM Gigabit Ethernet Controller Datasheet.

DOCUMENTATION CHANGES

1. 82540EM Controller Errors in Pin Number to Signal Mapping Table

Problem: In the design guide, some signals are listed twice and some referenced balls do not exist. The following signal/pin combinations should be ignored:

REQ64#	U14
ACK64#	W16
INTB#	T1
PAR64	V15
NO_CONNECT	P9
NO_CONNECT	A13
NO_CONNECT	A9
NO_CONNECT	B10
NO_CONNECT	C11
NO_CONNECT	C12
NO_CONNECT	C9
NO_CONNECT	B12
NO_CONNECT	B9
NO_CONNECT	E11
NO_CONNECT	E9
NO_CONNECT	E15
NO_CONNECT	E10
NO_CONNECT	D9
NO_CONNECT	C7
NO_CONNECT	C8
NO_CONNECT	B7
NO_CONNECT	D10
NO_CONNECT	A6
NO_CONNECT	A7
NO_CONNECT	A14
NO_CONNECT	C13
NO_CONNECT	C14
NO_CONNECT	E14
NO_CONNECT	D13
NO_CONNECT	E12
NO_CONNECT	D12
NO_CONNECT	E13
LOCK#	Y9

In the design guide and LOM design note, some ball numbers are shown incorrectly in the tables, but the reference schematic shows them correctly. The corrected ball numbers are as follows:

MDIA[0]+	C13
MDIA[1]+	E13
MDIA[1]-	E14
MDIA[2]+	F13
MDIA[2]-	F14
MDIA[3]-	H14

In the design guide and LOM design note (to a lesser extent), some signals need only to have the negation symbol added:

IRDY#	F1
TRDY#	G3
STOP#	H1
CBE0#	M4
CBE1#	L3
CBE2#	F3
CBE3#	C4

Affected Docs: 82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide Rev. 0.5 and 82551QM/82540EM Interchangeable LOM Design Application Note (AP-432) Rev. 0.5.

2. 82540EM Controller Error in Pin Description Tables

Problem: In the 82540EM Ethernet Controller datasheet, the text for M66EN says it is ignored but "should be connected properly for future compatibility". In fact, it **must** be connected to enable the controller to set device operation to match the clock speed. The documents will be corrected.

Erratum #13, "Excessive PCI Bus Hold Time," contains special instructions for the M66EN signal applicable only to A0 and A1 component steppings.

Affected Docs: 82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide Rev. 0.5.

3. Errors in 82551QM/82540EM Controllers Combined Reference Schematics

Problem: There are several errors in older versions of reference design schematics for the 82551QM and 82540EM controllers. Most of the errors affect the design when the board is populated with the 82551QM controller option. The following errors are contained in the reference design schematic dated 8/18/01:

- R7 is shown connected to RBIAS100-CTRL25 for an 82550EM controller design ("K"). The schematic should show R7 connected for an 82551QM controller design ("L").
- The center taps of the magnetics T1 on the controller side are shown connected together. In an 82551QM controller design ("L"), the center tap for transmit (Pin 1) and the center tap for receive (Pin 4) should not be connected to the center taps for unused pairs (Pins 7 and 10). It is acceptable to leave Pins 7 and 10 connected together.
- In an 82551QM controller design ("L"), the center tap for the receive pair on magnetics module T1 (Pin 4) should remain connected to 0.1uF capacitor C22. The schematic only shows it connected for an 82540EM controller design ("K").

The following errors are contained in the reference design schematic dated 11/14/01:

- Resistors R117 and R106 are shown connected across the first MDI analog pair for an 82550EM controller design ("K32"). The schematic notation should change to "K32/L" to denote that these resistors are also required for an 82551QM controller design.

The following errors are contained in some versions of the reference design dated "12/05/02":

- The schematic needs pulldown resistors on the TRST# and TCK signals to make certain the Test Access Port is disabled when it is not in use. Never leave the TRST# input to float. A suggested pull-down resistor value is approximately 1K ohms.

The newest schematic attached to this specification update corrects these errors. In addition, recent schematics use the 82551QM and 82540EM product names instead of project names.

Affected Docs: 82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide Rev. 0.5 and 82551QM/82540EM Interchangeable LOM Design Application Note (AP-432) Rev. 0.5.

4. 82540EM Controller May Need Larger EEPROM

Problem: The design guide text refers to the 93C46 64 X 16 EEPROM, which is not large enough for alerting (ASF) applications.

The text should change to recommend the 93C46 device for non-alerting applications and the 93C66 (256 x 16) device for alerting applications. Reference design schematics show the 93C66.

Affected Docs: 82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide Rev. 0.5.

5. 82540EM Controller Package Information

Problem: Some of the mechanical drawings were incomplete or incorrect. In addition, the text for the 82540EM controller incorrectly describes the package dimensions.

The dimensional drawing for the 82540EM controller is attached. The 82540EM overall dimensions are 15mm x 15mm.

Affected Docs: 82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide Rev. 0.5.

6. Omissions in 82540EM Controller Pin Description Table

Problem: The pin description table in the datasheet for the 82540EM Ethernet controller does not describe the CTRL_15 and CTRL_25 signals. These outputs from the on-board low drop out voltage regulator circuitry are intended to drive PNP pass transistors rated at 1A minimum collector current. The reference schematic illustrates the circuit connections. The pin description table also does not list the CLK_VIEW signal.

The 82540EM pin description table will add the following entries:

Signal Name	Type	Name and Function
CTRL_15	A	**1.5V Control.** LDO voltage regulator output to drive external pass transistor. If 1.5V is already present in the system, leave output unconnected.
CTRL_25	A	**2.5V Control.** LDO voltage regulator output to drive external pass transistor. If 2.5V is already present in the system, leave output unconnected.
CLK_VIEW	TS	**Clock View.** Output for GTX_CLK and RX_CLK during IEEE PHY conformance testing. The clock is selected by register programming.

Affected Docs: 82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide Rev. 0.5.

7. Impedance Compensation Resistor Connections

Problem: The stuffing option table in the 82551QM/82540EM Interchangeable LOM Design AP Note suggests incorrect (reversed) connections to the impedance compensation pins for a system built with the 82540EM device.

The correct circuit recommendation for ball G4, ZP_COMP, is:

Pull-down
Stuff precision 53-ohm resistor **pull-down** for 82540EM.

The correct circuit recommendation for ball H4, ZN_COMP, is:

Pull-up
Stuff precision 35-ohm resistor **pull-up** for 82540EM.

Affected Docs: 82551QM/82540EM Interchangeable LOM Design Application Note (AP-432) Rev. 0.5, Ref. No. 10565. Other documents and schematics reference these pins correctly.

8. Automatic EEPROM Reload of Hardware Defaults Following Software Reset

Problem: For the 82540EM A0 and A1 steppings, software drivers were required to initiate a hardware reload of the default configuration settings from EEPROM whenever a software reset occurred. In the A2 stepping, this operation occurs automatically. Overall system response and driver load time are improved.

The datasheets and design guides will change to indicate the improved operation.

Affected Docs: 82540EM Gigabit Ethernet Controller Preliminary Datasheet and Software Design Guide Rev. 0.5.