82559/82559ER to 82551ER/IT/QM Migration

Application Note (AP-442)

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Revision History

Revision	Revision Date	Description
1.0	Nov 2002	Initial release (Intel Confidential)
2.0	Oct 2004	• Added miscellaneous information relating to NAND/XOR testing, Reset (RST#), Isolate (ISOLATE#), and Alternate Reset (ALTRST#) signal definitions, and driver images. • Added a new pin differences table for the 82559, 82559ER, 82551ER, 82551IT, and 82551QM. • Removed Figure 1 “82559 Ball Grid Array Diagram” and Figure 2 “82551 Ball Grid Array Diagram”.
2.1	Dec 2004	• Added information about migrating from a 2-layer 0.36 mm wide-trace substrate to a 2-layer 0.32 mm wide-trace substrate. Refer to the section on Package and Pinout Information. • Added statement that no changes to existing soldering processes are needed for the 2-layer 0.32 mm wide-trace substrate change in the section describing “Package Information”.

1.0 Introduction and Scope

The document explains how to migrate from an Intel® 82559/82559ER Fast Ethernet controller-based design to an Intel® 82551xx Fast Ethernet based-controller design. The primary differences to consider between the 82559/82559ER and 82551xx are:

- 82551xx programmable device IDs
- 82551QM integrated UNDI ROM
- A second 82551xx General Control Register in the Control/Status Register (CSR)
- Pinout differences

Note: Throughout this application note, the notation "82551xx" is used to denote the 82551 Family of Fast Ethernet Controllers (82551ER, 82551IT, and 82551QM). Also, only the differences between these devices are listed.

The first two issues are addressed in the device EEPROM as detailed in the following sections. Note that the 82551ER/IT and the 82559/82559ER do not support an integrated UNDI ROM.

2.0 Programmable Device IDs

The Device ID is a fixed value in the 82559/82559ER. However, it is programmable in the 82551xx with its contents contained in word 23h of the EEPROM. Word 23h is reserved (0000h) in the 82559/82559ER, thus the Device ID is set to 0000h for EEPROMs mapped to the 82559/82559ER when they are used with the 82551xx. This prevents the 82551xx driver from loading because the device is not recognized. The only way to correct this problem is to physically remove the EEPROM and reprogram it for use with an 82551xx device.

Note: Tools for reprogramming the EEPROM, such as EEUPDATE, will not work on 82551xx silicon with an EEPROM mapped for the 82559/82559ER since the Device ID initially equals 0000h in the 82551xx device before it is properly programmed to the correct value.

If the EEPROM is programmed as follows, no problems should occur:

- EEPROM word 0Ah, bit 13 equals 0b:
  - — On the 82559/82559ER, if this bit is clear, then the Device and Vendor IDs are set to their default values.
  - — On the 82551xx, if bit 13 is clear and bits 15 & 14 equal 01b, the Device ID is programmed with the contents of EEPROM word 23h (1229h or 1059h for the 82551QM and 1209h for the 82551ER/82551IT). The Vendor ID is loaded with the contents of EEPROM word 0Ch (8086h).

Note: Device ID 1059h is for an 82551QM mobile solution.

- EEPROM word 0Ah, bit 13 equals 1b:
  - — If bits 15 and 14 are 01b and bit 13 is set, the PCI Device ID is programmed from the contents of EEPROM word 23h (1229h or 1059h for the 82551QM and 1209h for the 82551ER/82551IT). The Vendor ID is automatically loaded with a value of 8086h, regardless of the contents in EEPROM word 0Ch.

Some 82551xx designs do not use an EEPROM. Instead, the controller is programmed through the PCI interface using these Device ID and Vendor ID defaults:

- 82551QM - 1229h or 1059h
- 82551ER/82551IT - 1209h
- 8086h (Vendor ID for all devices)

3.0 UNDI ROM Support (82551QM Only)

The 82551QM has an embedded Universal Network Driver Interface (UNDI) ROM. This ROM can be enabled or disabled through the EEPROM in word 0Ah, bit 12, UNDI Disable. When the EEPROM is updated, this bit can be set, enabling the integrated UNDI. Note that the integrated UNDI ROM conflicts with older UNDI/Pre-boot eXecution Environment (PXE) ROMs typically built in the PC BIOS and stored in the system flash device. This conflict can cause the system to lock up during the Power-on Self Test (POST). If this occurs, only one method exists to unlock the system: power down and physically remove the EEPROM and reprogram it to clear bit 12 of word 0Ah.

If the UNDI bit of the EEPROM is cleared, which disables the internal UNDI, BIOS defaults need to be updated (external UNDI and PXE ROM) to prevent conflicts from occurring.

The 82551QM includes an initialization code (without a setup menu), driver loader, and UNDI driver. The Remote Program Load (RPL) module is not included. If a setup screen or RPL module is required, a larger module needs to be added to the BIOS instead of using the internal UNDI.

Note: The driver loader and UNDI driver are the exact same ones that were released with the Intel® Boot Agent (IBA), version 4.0.19.

Due to size limitations in the 82551QM internal ROM (16 KB), only these components can be included. To use the internal UNDI for booting a system, the BIOS must include the PXE base code (30 KB) as a separate flash image.

Note: The size and behavior of the integrated 82551QM UNDI is similar to that of the UNDI found in the 82550.

The Boot Disable bit in the EEPROM can disable the internal UNDI driver. However, the UNDI Disable bit (bit 12 of EEPROM word 0Ah) determines whether the design uses the internal UNDI or an external flash device when the Boot Disable bit is 0b. This allows the device to be used with either the internal UNDI driver or an external UNDI driver in either the BIOS or external Flash.

The UNDI driver in the 82551QM will function with the 8255x base code. If the latest Fast Ethernet Intel Boot Agent (IBA) monolithic image is stored in the BIOS, it will function with any 8255x design, excluding the 82559ER and 82551ER/IT).

The UNDI driver version in the 82551QM can be used with the latest Fast Ethernet IBA base code image in the BIOS without causing conflicts. The primary concern is that if a problem is found with that UNDI code, it cannot be fixed in ROM since the actual silicon design would need to be redone. In this case, the internal UNDI would have to be disabled and replaced with an UNDI in the BIOS, which is similar to using the standard monolithic IBA image. If the standard IBA image is located in the BIOS, it will function on any 8255x adapter supporting PXE since they are all compatible.

Note: The 82550 also had an integrated UNDI driver, however, it was not reliable. By keeping the Boot Disable bit set to 1 in designs incorporating the 82550, the internal UNDI driver was disabled to avoid conflicts.

4.0 Second General Control Register

82551xx devices have a second general control register, SCB General Control 2, in the Control/ Status Register (CSR). The SCB General Control 2 register is located in the CSR at offset 1Dh. It provides additional configuration parameters for EEPROM and Flash reads, writes, and power management capabilities:

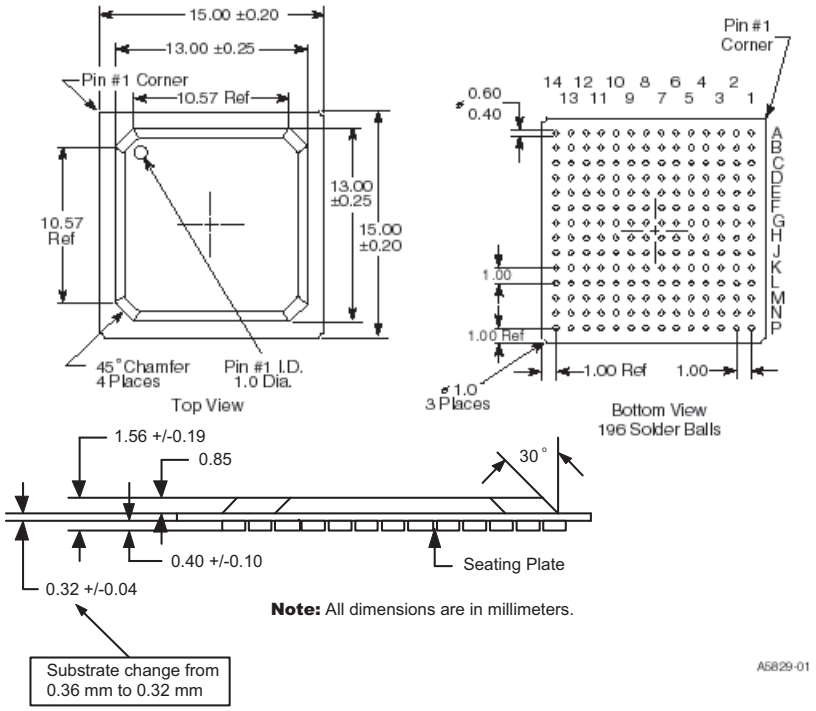
- **Bit 23** - Bit 23 enables software read and write access to the EEPROM and Flash. If this bit is set to 1, software access is allowed. If it is cleared to 0, software access to the EEPROM or Flash is denied.
- **Bit 19** - Bit 19 is used to enable Link Status Change Interrupt. When bit 19 is set to 1, an interrupt is asserted on any link status change. The interrupt is masked (when bit 19 equals 0) by default to ensure backward compatibility.

All other bits in this byte (22, 21, 20, 18, 17, and 16) are reserved and should not be used.

5.0 Package Information

82559/82551ER and 82551xx Fast Ethernet Controllers are 196-pin Ball Grid Array (BGA) packages as shown in Figure 1. You can find more information on Intel® device packaging in the Intel Packaging Handbook.

Figure 1. Dimension Diagram for the 196-pin BGA



Note: No changes to existing soldering processes are needed for the 0.32 mm substrate change.

6.0 Pin Differences

Table 1 lists the pin differences between each of the controllers. For a complete listing of pins, refer to the controller's respective Datasheet.

Table 1. Pin Differences Between 82559/82559ER and 82551xx Controllers

Ball Reference	82559 Pin Name	82559ER Pin Name	82551ER/IT Pin Name	82551QM Pin Name
A10	SMBCLK	NC	NC	SMBCLK
B10	SMB_ALERT#	NC	NC	SMB_ALERT#/ LAN_PWR_GOOD
C5	CSTSCHG	NC	NC	CSTSCHG
C9	SMBDATA	NC	NC	SMBDATA
D11	VSS	VSS	NC	NC
E11	VSS	VSS	NC	NC
H11	VSS	VSS	NC	NC
L7	CFCS#	NC	NC	MDMCS#
L8	CFCLK	NC	NC	NC

Note: Since pins D11, E11, H11, and L8 are not connected internally, there is no problem leaving these 82551xx pins connected the same as they were when replacing an 82559/82559ER in a design with an 82551xx part. No hardware changes are required.

7.0 Miscellaneous Information

7.1 Testing

For NAND tree mode, the difference between the 82559/82559ER and 82551xx controllers is that the 82551xx uses XOR testing. During 82551xx XOR testing, the ISOLATE# signal must be driven high in order to enter the test mode and it must be kept high throughout the test. Otherwise, the two chains are the same (except ISOLATE#). For 82551xx controllers, ISOLATE# is removed from the chain. The XOR tree test mode was inadvertently left out when the 82551xx Datasheets were originally released. This has been identified as a change and is now included in the latest Datasheet release for the 82551ER/IT and is currently being added to the next Datasheet release for the 82551QM.

7.2 Reset

The definitions for the Reset (RST#), Isolate (ISOLATE#), and Alternate Reset (ALTRST#) pins of the 82551xx (as it was with the 82550 on which the 82551xx is based) have changed slightly. These changes can be found in the 82551xx controller's respective Datasheet under the pin description section.

7.2.1 Impact

Some designs in existence may implement the previous recommendations for the RST#, ISOLATE# and ALTRST# input pins. In these cases, the PCI Reset signal is connected to the RST# pin, the PCI power source's stable power (LAN_PWR_GOOD) to the ISOLATE# pin, and the auxiliary power source's stable power (AUX_PWR_GOOD) to the ALTRST# pin. It is not necessary for existing working designs to make changes for these signals; however, it is recommended that the new changes contained in the Datasheet should be included when possible. New designs should implement these recommendations.

7.2.2 Reason For Change

This change is not required for working existing designs, but recommended for new designs. The issue has to do with the functionality of the ISOLATE# pin. An active ISOLATE# causes the silicon to ignore PCI inputs including the RST# pin. The issue was seen with designs where the RST# pin (connected to PCI_RST signal) was active before ISOLATE# went active, causing the silicon to get a partial reset. The recommendation was designed to prevent this potential and extremely rare problem.

It should not be an issue on existing working 82559/82559ER designs if the change is not made and is not needed on 82559/82559ER-based designs. 82559/82559ER-based designs should continue to connect PCI reset (PCI_RST) to the 82559/82559ER's RST# pin and pull-up ISOLATE# to VCC.

7.3 Driver Images

Device IDs are identified in a driver's INF file so you can identify the device, the device ID, the manufacturer's code, and the rev number of the device. While the manufacturer and device ID can be changed to match, the rev number can not be changed in the EEPROM. If a customer has an early driver version, it will see only a revision number of 08h (82559 B-step) and possibly 09h (82559 C-step) but not 0Fh, which is for the 82551xx, so the 551xx and possibly the 82559 C-step will not be identified. The latest driver has revision 09 making this not an issue for many customers but it is an issue for customers who have operating system images. The images need to be changed to the latest driver to ensure recognition of the 82559 C-step and the 82551xx.

8.0 Summary

If a device EEPROM is present, it must be programmed to supply the Device ID; otherwise, it holds a value that is not recognized by current Intel drivers. Instead, it shows Device and Vendor IDs determined by EEPROM word 0Ah, bits 15:13.

Drivers program the 82551QM if the integrated UNDI ROM is disabled (through EEPROM word 0Ah) and the IBA in the BIOS.

The 82551xx devices include SCB General Control 2 register in the CSR, whereas the 82559/ 82559ER devices, do not.

The only hardware changes, as listed in Table 1 and as noted following Table 1, require no changes when “dropping” an 82551QM into an existing 82559 design or an 82551ER/IT into an existing 82559ER design, making the devices fully pin-to-pin compatible.