ICHx Integrated LAN Controller Function Disable and Power Control for Fast Ethernet

Application Note (AP-417)

Revision 3.0
October 2003

Revision History

Revision	Revision Date	Description
1.0	April 2001	Added design detail for the Exclusive OR (XOR) Tree Test and Isolate Mode. • Added 100 Ω series resistors to Figures 1, 3, and 4, for the XOR Tree Test and Isolate Mode. • Added a table to Section 2.3.2 ”82562ET/EM PLC Device Disable for Lower Power Consumption” for configuration of various modes.
2.0	Nov 2002	Changed document status to Intel Confidential. No content changes were made.
3.0	Oct 2003	LAN disable circuit updated to reflect ICH3 and later (ICHx); removed “confidential” status.

Contents

1.0 Introduction

This application note provides guidelines for function disable of the Intel® 82562 Platform LAN Connect (PLC) devices.

1.1 Scope

This application note covers the function disable that supports the I/O Control Hub 3 and later (ICHx), 82562 Platform LAN Connect (PLC) design. The 82562 PLC design supports two types of devices:

- The 82562ET and 82562EZ supports basic 10/100 Mbps Ethernet connection.
- The 82562EM, 82562EP, 82562EX supports 10/100 Mbps Ethernet connection and integrated alert capabilities, which are covered in the 82562EM 10/100Mbps Platform LAN Connect Datasheet.

1.2 Reference Documents

It is assumed that the designer has a working knowledge of high-speed design and layout issues and the Advanced Configuration and Power Interface (ACPI) Specification. An understanding of power management industry initiatives is valuable prior to beginning the integration of the 82562ET into any platform. The following reference list provides sufficient background material.

- 82562ET (EM, EZ, EP, EX) 10/100 Mbps Platform LAN Connect (PLC) Datasheet. Intel Corporation.
- I/O Control Hub 3 (or later) Datasheet. Intel Corporation.
- LAN on Motherboard Design Guide Application Note (AP-414). Intel Corporation.
- I/O Control Hub 2 (and 3) EEPROM Map and Programming Information Application Note (AP-409). Intel Corporation.
- Network Device Class Reference, Revision 1.0a. Intel Corporation, Microsoft Corporation, and Toshiba.

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2.0 ICHx and 82562 Integrated LAN Function Disable and Power Control

2.1 ICHx Integrated LAN Function Enable/Disable Controls

To control LAN function enable and disable, the system state enable/disable policy control, hardware control, and BIOS need to be considered to work with the OS and driver. The implementation conditions are listed below:

System state and BIOS considerations:

- The physical ICHx Integrated LAN Function enable and disable switch is only allowed during an S5 power state to S0 power state transition (in other words, full OS boot).
- The physical ICHx Integrated LAN Function Enable/Disable hardware control must not change in the S0 power state or during an S1 to S4 power state exit.

  The appearance or disappearance of the ICHx Integrated LAN function confuses the OS. Current operating systems have no direct methods of dealing with this. Current BIOS setup implementations prohibit entry into BIOS setup when the platform is in an S1 to S4 power state change.
- Hardware control must retain its state while the ICHx Integrated LAN is powered on until the next S5 power state exit. This includes the S1 through S5 power states.

  A platform Resume-well General Purpose Output (GPO) or Super IO GPIO can be used for this functionality. If the hardware control loses state, the ICHx Integrated LAN must be non-functional until the next S5 power state exit. (This does not cause any problems since the ICHx Integrated LAN's normal operation is dependent upon the platform Resume-well power.)

LAN Enable/Disable policy control (CMOS RAM bit), hardware control, and BIOS considerations:

- The ICHx Integrated LAN Enable/Disable policy control must be separate from the physical ICHx Integrated LAN Enable/Disable hardware control.

  The policy control information is a bit in the CMOS RAM.
- The ICHx Integrated LAN Enable/Disable hardware control must be written by the BIOS during the Power On Self Test (POST) whenever exiting the S5 power state.
- The BIOS copies the CMOS RAM bit to the hardware control.

  The physical ICHx Integrated LAN Enable/Disable transition occurs if the state of the CMOS RAM bit differs from the previous hardware control setting.

2.2 BIOS Setup for ICHx Integrated LAN Function Enable/ Disable

The recommended procedure to enable or disable the ICHx Integrated LAN function is outlined in the following steps:

1. Launch BIOS Setup (various vendor-specific methods used).
2. Change "ICHx LAN Function Enable/Disable" setting in BIOS Setup.

   This sets or clears the ICHx Integrated LAN enable flag bit in the CMOS RAM. The physical hardware control is not changed at this time.

   Note: The ICHx Integrated LAN Enable/Disable policy control bit (CMOS RAM) must be separate from the physical ICHx Integrated LAN Enable/Disable hardware control.

   The ICHx Integrated LAN enable flag bit can only be changed in BIOS Setup by the user. A failure of the on-board battery well power (e.g., a real time clock failure) is detected on the platform and also forces BIOS setup with the default choices presented. The BIOS should default to ICHx Integrated LAN enabled mode since this is what the proposed hardware implementation does after a Resume-well power failure.

   If an ICHx or Resume-well General Purpose Input/Output (GPIO) is used for ICHx Integrated LAN enable, it defaults to high after a Resume-well power failure, which is the setting for ICHx Integrated LAN enable mode. In this case, ICHx Integrated LAN enable signal remains asserted (high) until it is changed by the BIOS POST at the next S5 exit. This enables the ICHx Integrated LAN function through hardware by default. It remains enabled if BIOS writes 1b to the ICHx Integrated LAN enable flag and is disabled if 0b is written to the flag.

   Note: For ICHx, Resume-well GPIOs are GPIO[24:25] and GPIO[27:28].

3. A full platform reset and OS boot (S5 power state exit) must follow the BIOS Setup exit, which is normal behavior for current platforms. This enables the various CMOS RAM settings to be loaded into hardware. The physical ICHx Integrated LAN hardware control is always loaded by BIOS during platform S5 power state exit, except after a battery well power failure. This ensures that hardware is always synchronized with the ICHx Integrated LAN enable flag setting.

   The hardware control configuration remains unchanged until it is changed by BIOS during the next S5 power state exit. This insures that the ICHx Integrated LAN remains enabled if it is powered on during platform sleep states.

2.3 ICHx Integrated LAN Function Enable/Disable Hardware Control

2.3.1 ICHx and Integrated LAN Disable

Note: ICHx Integrated LAN Controller resides on the ICHx VccSus3_3 and VccSus1_8 power wells (typically referred to as “auxiliary” (“aux”) or “standby” supplies at the platform level).

The ICHx Integrated LAN’s LAN_RST# is the ICHx Resume-well input. It can be held low indefinitely to keep the ICHx Integrated LAN Controller in a reset state. The LAN Reset (LAN_RST#) signal must not be deasserted sooner than 10 ms after the Resume power supply reaches its nominal voltage. This ensures that the ICHx Integrated LAN Controller is initialized. Figure 1illustrates a possible solution for ICHx Integrated LAN disable.[1] Section 2.3.3 explains the remainder of the circuit."

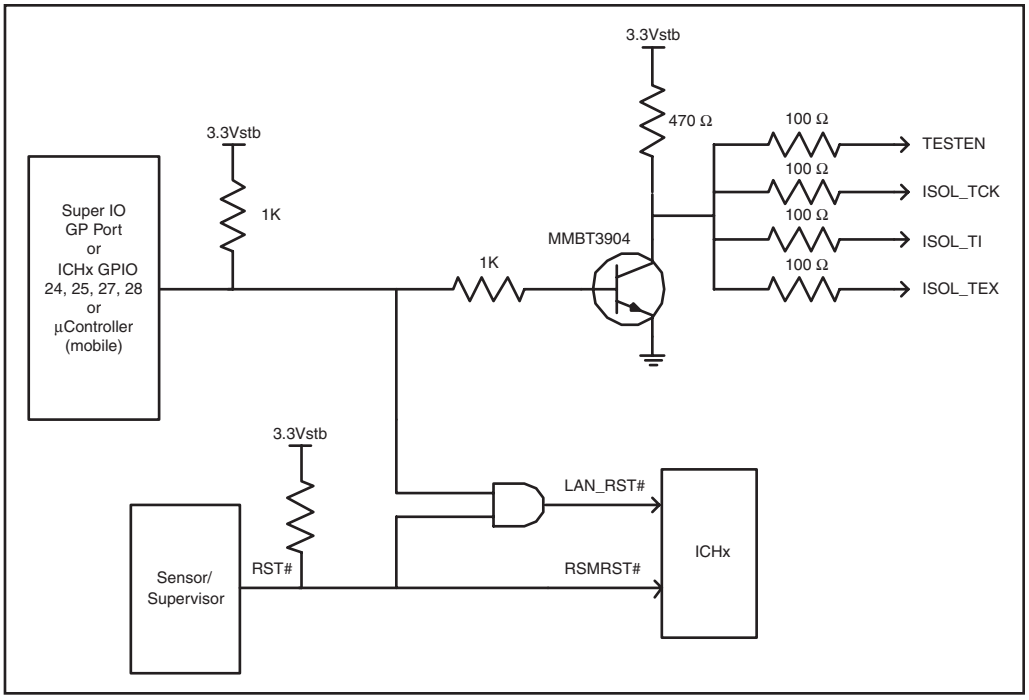

Figure 1. ICHx LAN Disable Circuitry

The 100 Ω resistors for the Test Mode signals are required for the Exclusive OR (XOR) Tree and Isolate Mode.

1. It is assumed that the sensor/supervisor device provides the required 10 ms. LAN reset

2.3.2 82562ET/EM PLC Device Disable for Lower Power Consumption

The configuration to place the LAN Controller device into various modes is outlined in the table below. The configuration for disabled mode (or powered-down mode) is also listed in the following table.

TESTEN[a]	ISOL_TCK[b]	ISOL_TI[c]	ISOL_EX[d]	Mode	Comments
0	0	0	0	Normal System Mode	The ISOL_TCK, ISOL_TI and ISOL_EX pins can remain floating.
0	1	1	1	Isolate Mode	The device is in tri-state mode and fully powered down.
1	0	0	0	XOR Tree	The XOR Tree is used for board testing and tri-state mode.
1	1	1	1	Power-down Mode	The device is in tri-state mode and fully powered down.

a. Test Enable signal
b. Test Clock signal
c. Test Input signal
d. Test Execute Command signal

2.3.3 Recommended ICHx Resume-well GPIO Control Methods for LAN Disable

A Super I/O GPIO, ICHx Resume-well GPIO, or micro-controller output (Mobile) is used to control the ICHx LAN_RST# signal as well as the LAN Controller test pins. After Resume-well Reset, the GPIO signals transition high (default). The Resume-well GPIOs hold their state while the Resume Power is valid. When the Resume-well has power and while the Resume Reset (RSMRST#) signal is still low, the Resume-well GPIOs will be floated. A 1K pull-up resistor is required on the chosen GPIO to ensure that it is held high until actively driven by the ICHx. Also, an inverter is required on the signal before it is routed to the PLC. The NPN transistor circuit provides inversion.

Notes:

1. ICHx Resume-well GPIOs are GPIO 24, GPIO 25, GPIO 27, and GPIO 28.
2. If LAN Controller is disabled during powerup, a test mode may be engaged.
3. ICH RSMRST# must be held low for at least 10ms after resume power supply reaches its nominal state.

The 82562xx PLC device must be enabled during power up. The circuit in Figure 1meets this need while providing the glue logic to disable the PLC device from BIOS as described earlier.