82559ER Fast Ethernet PCI Controller

Stepping Information

October 2004

Revision 1.1

Notice: The 82559ER Fast Ethernet PCI Controller may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

82559ER Stepping Information

Contents

Revision History

Date	Version	Description
Oct. 2004	1.1	Removed Intel Confidential status. Removed references to A3 stepping, which does not exist.
Apr. 2000	1.0	First initial release (Intel Confidential - Controlled Access)

Preface

This document is an update to the specifications contained in the Intel® 82559ER Fast Ethernet PCI Controller Data Sheet, and contains issues affecting all design using the 82559ER device.

This document is intended for hardware system manufacturers and software developers of applications, operating systems or tools. It contains Specification Changes, Errata, Specification Clarifications, and Document Changes.

All changes, errata, and clarifications described in this document will be incorporated into the next release of the 82559ER Fast Ethernet PCI Controller Data Sheet.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the 82559ER's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Identification Information

82559ER Component Marking Identification

Device	Stepping	Top Marking	Q-specification	MM Number	Notes
82559ER	A2	GD82559ER	STD	MM824184	Tape and reel
82559ER	A2	GD82559ER	Q409	MM822051	Tray
82559ER	A2	GD82559ER	SL3OG	MM825111	Tray
82559ER	A2	GD82559ER	SL3RB	MM825605	Extended temperature tape and reel

FFFFFFFF FPO numbers

82559ER Component Programming Interface Identification

Device	Stepping	Vendor ID	Device ID	Revision Number
82559ER	A2	8086h	1209h	09h

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82559ER steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes used in summary table:

X:	Specification Change, Erratum, or Specification Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This Item is either new or modified from the previous version of the document.

No.	A0	A2					Plans	SPECIFICATION CHANGES	Page
1		X					SDM1.2	Unsupported End of List Bit in High Priority Queues	5
No.	**A0**	**A2**					**Plans**	**ERRATA**	**Page**
1	X						Fix	False Power Management Event Indication on Power Cycle	6
2	X						Fix	Programmable Filter Corruption	6
No.	**A0**	**A2**					**Plans**	**SPECIFICATION CLARIFICATIONS**	**Page**
1		X					EDS 2.1	Link Loss Deep Power Down Noise Sensitivity	8
2		X					EDS 2.1	PCI Buffer Leakage When the Voltage Input/Output Pin (VIO) Not Powered	8

No.	A0	A2					Plans	DOCUMENTATION CHANGES	Page
1							AP-392 1.3	82559 LAN on Motherboard Design Guide	9
2							SDM 1.3	Software Developer's Manual	9

NOTE: The table uses the following abbreviations for listed documents.
DS: Data Sheet
SDM: Software Developer's Manual
EDS: External Data Specification
AP: Application Note

Specification Changes

1. Unsupported End of List Bit in High Priority Queues

Explanation: If High Priority Queue (HPQ) is used, the End of List (EL) bit in the command word of an HPQ or Low Priority Queue (LPQ) is not supported as an identification for the end of the Command Block List (CBL). Software drivers should only use the Start (S) bit in the header to identify the end of a CBL in a HPQ.

Implication: This change affects drivers that add support for multiple priority queues.

Status: The appropriate definition changes were made to all relative 82559ER documents.

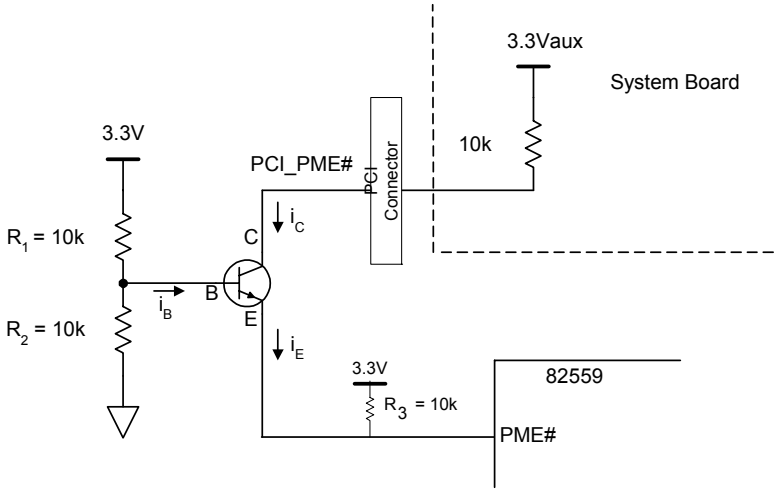
Errata

1. False Power Management Event Indication on Power Cycle

Problem: During power cycle events, the electrostatic discharge (ESD) elements internal to the 82559ER may falsely clamp the Power Management Event (PME) output signal to approximately 1.5 volts for 100 ms to 150 ms during initial power up. This can cause wake-up events to be recognized by the system if power management events are enabled in the system chipset. This may result in a problem for mobile environments since the false clamping can cause a suspended system to wake up when the power to the LAN device is transitioned.

Implication: The implications of this anomaly depend on the target system configuration. In desktop and server systems, the impact is limited to a false wake-up event occurring when a new card is installed. In mobile systems where the LAN power is transitioned more frequently, the PME signal should be disabled during transitions.

Workaround: False PME indications can be avoided by disabling the recognition of a PME before removing or restoring power to the 82559ER. If a hardware solution is required, the following isolation circuit has been proven to be effective. The circuit requires the PCI PME signal (PCI_PME#) to be isolated from the 82559ER PME signal (PME#). The system does not see the 1.5 voltage level drop caused by the 82559ER's power transition.



Status: This anomaly is under evaluation for resolution in future steppings of the 82559ER.

2. Programmable Filter Corruption

Problem: The first nine Dwords of the 16 Dwords of the programmable filter storage are shared with the transmit counters. The transmit counters are used by the 82559ER if Total Cost of Ownership (TCO) frames are sent from the System Management Bus (SMB) in a low power state. The filters can be corrupted due to the transmit counters update process as transmissions are completed.

Implication: Filters placed in the first nine Dwords of the programmable filters may be corrupted during TCO transmission. Interesting packets and power management event indication signals for these filters

may not occur. This issue does not affect the standard Advanced Configuration and Power Interface (ACPI) and Advance Power Management (APM) filters.

Workaround: If programmable filters are used, the construct of the Load Programmable Filter Command should be structured in such a way that the first nine Dwords of the filters are dummy filters. This structure should be followed with the next seven Dwords of real filter data.

Status: This anomaly is under evaluation for resolution in future steppings of the 82559ER.

Specification Clarifications

1. Link Loss Deep Power Down Noise Sensitivity

Clarification: The 82559ER supports a Deep Power Down on link loss feature. This feature enables the 82559ER to shut down when cable or activity from its link partner is present. If this feature is enabled, a powered down 82559ER physical layer (PHY) unit can be turned on by excessive noise. The thresholds on the 82559ER were chosen to work with existing devices on the market, with the goal of enabling the PHY over disabling the PHY in ambiguous situations.

Implication: The 82559ER may not be able to remain in the deep power down mode in noisy environments. This is not a serious concern because of the 82559ER's general low power consumption and its ability to shut down all but the PHY in this situation. Several changes can be made to the line interface to limit noise. These changes are only required on the receive pair of the device. This includes adding a capacitor between receive differential pair (RDP and RDN). Additional capacitance between the receive pair helps filter the differential noise but may have a negative impact on the receive performance and on receive return loss. A capacitor value above 15 pF may impact performance and should be disconnected after link is achieved.

2. PCI Buffer Leakage When the Voltage Input/Output Pin (VIO) Not Powered

Clarification: When the system is in a Suspend state (Voltage Input/Output pin equals 0 volts and power equals 3.3 volts), the 82559ER PCI I/O buffers can rise to about 700 mV causing a leakage current to flow into the Voltage Input/Output (VIO) pin. The resistor value greater than 10 KΩ is recommended in some of the application notes relating to 82559ER based designs. In 82559ER designs it is recommended that the VIO pin is pulled to the 3.3 V rail used by the device or a +5 V rail that is active when the 82559ER is powered (for example, +5 $V_{auxiliary}$).

Implication: The 82559ER VIO pin should be active when the device is active. This provides the lowest power consumption in suspend states.

Documentation Changes

1. 82559 LAN on Motherboard Design Guide

Document Title: Intel® 82559 LAN on Motherboard (LOM) Design Guide Application Note (AP-392)

Previous Revision: Revision 1.2

November 1998

Current Revision: Revision 1.3

September 1999

Changes: The application note (AP-392) was updated to the new recommendation for the PCI Reset signal to be tied to the 82559ER's Isolate pin. This change was made to maintain the proper relationship between the Isolate and Reset signals on the 82559ER. It was always recommended that the Isolate signal is not asserted following the assertion of the Reset signal and to ensure that the isolate event precedes a reset event. This has proven to be a difficult task in actual application; therefore, the recommendation was changed to simplify board design.

Impact: Operational designs that meet previous recommendations do not require any changes. The new recommendations provide a simpler solution for new board designs.

2. Software Developer's Manual

Document Title: Intel® 10/100 Mbit Ethernet Family Software Developer's Manual

Previous Revision: Revision 1.2

November 1998

Current Revision: Revision 1.3

August 1999

Changes: Software must issue a Port Reset command following a power state transition to the D0 state from the D1 or D2 states. This is required to clear the wake-up filters that are automatically cleared on the normal D3 state to D0 state change.

Impact: A corruption of the PCI Direct Memory Address (DMA) in the 82559ER may occur if the wake-up filters are still active following a transition.

Changes: The Link Status Indication bit in the Power Management Driver Register (PMDR) to a reserved bit (0).

Impact: The 82559ER will still wake-up on a Link Status change, but this bit cannot be used to poll for link status as a cause for the wake-up.

Changes: EEPROM Word Dh, bit 15 changes to a reserved bit (0).

Impact: This bit has always been defined as equal to 0 for all configurations. The change is only limited to calling it out as reserved in this description.

Changes: When High Priority Queue (HPQ) is used, The End of List (EL) bit is not allowed for both HPQ and Low Priority Queue (LPQ). Software should only use the Start (S) bit to identify the end of a Command Block List (CBL) in a HPQ.

Impact: This change does not effect existing drivers. However, drivers that add support for multiple priority queues will be affected.