82551QM Fast Ethernet Multifunction PCI/CardBus Controller

Stepping Information

July 2005

Revision 1.3

Notice: The 82551QM Fast Ethernet Controller may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this document.

Contents

Revision History

Date	Version	Description
Dec. 2001	1.0	Initial release. (Intel Secret)
Mar. 2003	1.1	• Added Errata 4, “MDI/MDI-X Feature Not Supported”. • Added Document Change 1, “82551QM Fast Ethernet PCI/CardBus Controller Datasheet”.
Aug. 2004	1.2	Removed Errata 4, “MDI/MDI-X Feature Not Supported”. This feature is now supported. Removed Documentation Changes section.
July 2005	1.3	Deleted Erratum #4.

Preface

This document is an update to the specifications contained in the 82551QM Fast Ethernet Multifunction PCI/CardBus Controller Datasheet, and contains issues affecting all design using the 82551QM device.

This document is intended for hardware system manufacturers and software developers of applications, operating systems or tools. It contains Specification Changes, Errata, Specification Clarifications, and Document Changes.

All changes, errata, and clarifications described in this document will be incorporated into the next release of the 82551QM datasheet.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the 82551QM’s behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification’s impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Product Code

The product ordering code for the 82551QM is: GD82551QM.

Identification Information

82551QM Component Marking Identification

The component marking identification and top marking diagram will be included in a future revision of this document.

Device	Stepping	Top Marking	Q-specification	MM Number	Notes
82551QM	A-1	82551QM	Q506ES	843565	

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82551QM steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes used in summary table:

X:	Specification Change, Erratum, or Specification Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This Item is either new or modified from the previous version of the document.

No.	A-0	A-1	Plans	SPECIFICATION CHANGES	Page
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NOTE: The table uses the following abbreviations for listed documents.
DS: Data Sheet
SDM: Software Developer's Manual
EDS: External Data Specification
AP: Application Note

Specification Changes

1. Unsupported End of List (EL) Bit in High Priority Queue

Explanation: If High Priority Queue (HPQ) is used, the End of List (EL) bit in the command word of an HPQ or Low Priority Queue (LPQ) is not supported as an identification for the end of the Command Block List (CBL). Software drivers should only use the Start (S) bit in the header to identify the end of a CBL in a HPQ.

Implication: This change affects only software drivers that add support for multiple priority queues. It does not affect existing drivers.

Status: The appropriate definition changes will be made to all relative documents.

Errata

1. Lost Wake-up Packets with Dump Wake-up Packet Command

Problem: Wake-up packets can be lost if the Dump Wake-up Packet command is used.

Implication: In the Dx state, the 82551QM uses internal memory space to store incoming packets for filtering. These packet types include wake-up, TCO, and ARP. When ARP and TCO filters are enabled, incoming packets are not stopped when a wake-up packet is received. The wake-up packet is written over and lost. Therefore, the dumped packet that the driver reads is not necessarily the one that woke the system.

Workaround: A workaround does not exist at this time.

Status: There are no plans to fix this erratum.

2. Incorrect CIS Read Accesses After Power Up

Problem: When the 82551QM is configured for CardBus operation, it assumes that any Card Information Structure (CIS) read access from software waits one millisecond after the Reset signal is de-asserted. This allows EEPROM accesses to complete before CIS transactions are initiated. An EEPROM read before 1 ms may cause incorrect CIS transactions.

Implication: An EEPROM read performed prior to 1 ms after the Reset signal is de-asserted can cause incorrect CIS transactions.

Workaround: CIS access from PCI should be restricted to start only 1 ms after the Reset signal is de-asserted.

Status: There are no plans to fix this erratum at this time.

3. Link Loss Deep Power Down Noise Sensitivity

Clarification: The 82551QM supports Deep Power Down on link loss. This feature enables the 82551QM to shut down when cable or activity from its link partner is present. If this feature is enabled, the powered down 82551QM physical layer (PHY) unit can be turned on by excessive noise. The 82551QM threshold values were chosen to work with existing devices on the market, with the goal of enabling the PHY unit over disabling the PHY in ambiguous situations.

Implication: The 82551QM may not be able to remain in the deep power down mode in noisy environments. This is not a serious concern because of the 82551QM's general low power consumption and its ability to shut down all but the PHY in this situation.

Workaround: Several changes can be made to the line interface to limit noise. These changes are only required on the receive differential pair of the device. This includes adding a capacitance between the receive pair (RDP and RDN). Additional capacitance between the receive pair helps filter the differential noise but may have a negative impact on the receive performance and on receive return loss. A capacitor value above 15 pF may impact performance and should be disconnected after link is achieved.

Status: There are no plans to fix this erratum at this time.

4. (Deleted)

Specification Clarifications

1. 82551QM Initialization During System Management Bus (SMB) Access

Clarification: Initialization or reset sequences during the reception of packets destined for the System Management Bus (SMB) can cause the 82551QM to drop fragments. This may cause a corrupted sequence and, depending when the reset occurred during packet reception, lost SMB fragments.

Implication: The SMB master might observe receive packets on the SMB with missing fragments in the sequence. If a packet was received during the reset, then the first transaction to the 82551QM may be ignored. Subsequent accesses will continue to operate properly. The management controller should verify the completion of the incoming packet stream on the SMB to insure that the full sequence is received. The easiest method to perform this check is to verify that a SMB message was received with first, middle, and last segment markers set in order. When the 82551QM is accessed across the SMB after a reset event, a second attempt may be required if the first access has timed out.

2. PCI Buffer Leakage when the Voltage Input/Output (VIO) Pin Not Powered

Clarification: When the system is in a suspended state (Voltage Input/Output [VIO] pin equals 0 volts and power equals 3.3 volts), the 82551QM PCI I/O buffers can rise to about 700 mV causing a leakage current to flow into the VIO pin. A resistor value greater than 100 KΩ is recommended in some of the application notes relating to 82551QM based designs. In 82551QM designs, it is also recommended that the VIO pin is pulled to the 5 V supply in a 5 V PCI signaling environment and a 3.3 V supply in 3.3 V signaling environment. If an auxiliary power supply (standby power) is available, the VIO should be connected to it.

Implication: The 82551QM VIO pin should be active whenever the device is active. This provides the lowest power consumption in suspended states.

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