82558 to 82559ER Migration for Embedded Applications

Application Note (AP-407)

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Contents

Appendices

1.0 Introduction

As the migration to smaller geometries continues in the semiconductor industry, the size of integrated circuit packaging required for silicon components has also become smaller.

The Intel® 82559ER represents the latest offering in its integrated Media Access Controller (MAC) and Physical Layer interface (PHY) for 10/100 Mbps Ethernet component family. At 15 mm per side, it is one of the smallest parts to perform this function in the industry.

The 82559ER succeeds Intel's 82558 integrated MAC/PHY for embedded designs.

This application note is intended for those designers that have the need to move a design that was originally done using the 82558 integrated MAC/PHY controller to the 82559ER.

The scope of this application note covers:

- 82558 and 82559ER basic differences
- 82558 and 82559ER pinouts
- Magnetic (transformer) circuit differences
- Layout guidelines
- EEPROM definitions

1.1 Terminology

For the purposes of this document, the following terms will be defined and used as follows:

IEEE:	Institute of Electrical and Electronic Engineers. The IEEE is a governing body for Ethernet specifications with respect to the Physical and Data Link Layers of the International Standards Organization (ISO) seven layer Open System Interconnect (OSI) model.
LAN Controller:	The Intel 82558 and 82559ER are Local Area Network (LAN) controllers.
Magnetics:	The encapsulated transformer that is used to electrically isolate the 82558 or 82559ER from the RJ45 connector, which is connected to the Ethernet media (for example, Category 3 or Category 5 cable).
RJ45 connector:	An eight-pin connector specified by the IEEE for twisted pair Ethernet cable connections.
EEPROM:	Electrically Erasable Programmable Read Only Memory. The EEPROM is a memory device used with an Intel LAN controller. Immediately after Power On Reset (POR), the LAN controller attempts to read from configuration values from the EEPROM. The EEPROM is used in conjunction with Intel's LAN controllers must support the MicroWire* interface.

1.2 Reference Documents

- 82559 Fast Ethernet Multifunction PCI/CardBus Controller Datasheet, Intel Corporation.
- 82559 LAN on Motherboard Design Guide Application Note (AP-392), Intel Corporation.

- 8255X EEPROM Map and Programming Information (AP-394), Intel Corporation.
- 82558 Fast Ethernet PCI Bus Controller with Integrated PHY Datasheet, Intel Corporation.
- 82558 LAN on Motherboard Design Guide Application Note (AP-383), Intel Corporation.
- 82557 C-step and 82558 Based Products EEPROM Address Map and Programming Information Application Note (AP-382), Intel Corporation.
- 82558 Test Access Port Application Note (AP-389), Intel Corporation.
- LAN on Motherboard (LOM) Design Guide Application Note (AP-391), Intel Corporation.

2.0 82558 and 82559ER Basic Differences

The primary difference between the 82558 and the 82559ER are outlined in Table 1.

Table 1. 82558 and 82559ER Differences

Parameter	82558	82559ER
Package	208 SQFP	196 BGA
Package Size	35 mm x 35 mm	15 mm x 15 mm
Pin Spacing	1.25 mm	1 mm
PCI Voltage	5 V	3.3 V or 5 V
Power Supply	50 V DC	33 V DC
Maximum Current	470 mA	175 mA
Crystal or Oscillator Pin Voltage	5 V	3.3 V
Flash Memory Size	64 Kbyte	128 Kbyte
EEPROM Size	64 x 16 bits	64 or 256 x 16 bits
Device ID	1229	1209
PHY-based Flow Control support	Yes	No
Clockrun Protocol support	No	Yes
Wake on LAN support	Yes	No
Power Management Event support	Yes	Yes
ACPI Power State support	Yes	Yes
PORT Dump Wake-up support	No	Yes

Note: The 82558 is a 5 V, 208-pin Shrink Quad Flat Pack device versus the 82559ER that is a 3.3 V device (with 5 V tolerance on the PCI interface only), 196-pin Ball Grid Array.

3.0 Serial EEPROM

The serial EEPROM provides storage for initialization. Both the 82558 and the 82559ER can be interfaced to a serial EEPROM that consist of the following signals:

- EEPROM Data Input (EEDI)
  The EEDI pin acts as the serial input data pin from the EEPROM data output signal.
- EEPROM Data Output (EEDO)
  The EEDO pin acts as the serial output data pin to the EEPROM data input signal.
- EEPROM Serial Clock (EESK)
  The EESK pin acts as the serial clock output to the EEPROM.
- EEPROM Chip Select (EECS)
  The EECS pin is used to assert chip select to the serial EEPROM.

While the EEPROM is not necessary for either the 82558 or the 82559ER to function, there are certain operations that can only be controlled with the use of the serial EEPROM.

For example, the ability to disable the Base Address Register for the Flash device is controlled through the serial EEPROM. This cannot be done without the EEPROM. Both the 82558 and 82559ER have the ability to program the EEPROM by writing to the Management Data Interface (MDI) register.

Both the 82558 and 82559ER use the 93C46 serial EEPROM. Although the 93C66 can be used, it does not introduce any added benefits from its usage. Several vendors offer the 93C46:

- Atmel
- Xicor
- Microchip
- Hyundia
- National Semiconductor.

Note: The 82559ER requires a 3.3 V part while the 82558 requires a 5 V version of the 93C64.

The 82558 and 82559ER attempt to read the EEPROM upon the de-assertion of the PCI Reset signal. An internal state machine executes the following sequence of events:

1. Determines if a device is attached.
2. Reads the word at address 0A (hexadecimal).
3. Verifies that bits 15 and 14 of word A contain a valid configuration (01b).
   If a valid configuration is present, the remaining bits are read and loaded into the controller; otherwise, default values are used.

However, the bit definitions between the two components differ. The differences are illustrated in the following two subsections. More details relating to the serial EEPROM can be found in the following application notes: 82557 C-Step and 82558 Based Products EEPROM Map and Programming Information (AP-382) and the 8255X EEPROM Map and Programming Information (AP-394).

3.1 The 82559ER Serial EEPROM

A 3.3 V EEPROM (93C64) must be used with the 82559ER. Timing specifications from the EEPROM device datasheet should be taken into consideration for compatibility with the 82559ER.

Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	Sig (01b)		ID	0b	BD	Rev ID			ALT ID	DPD	0000b				STB Ena	RSV

Note: Bits 12 and 5:3 are reserved and should be set to 0.

Table 2. 82559ER EEPROM Word A Field Descriptions

Bits	Name	Description
15:14	Signature	The Signature field is a signature of 01b, indicating to the 82559 that there is a valid EEPROM present. If the Signature field is not 01b, the other bits are ignored and the default values are used.
13	ID	The ID bit indicates how the Subsystem ID and Subsystem Vendor ID fields are used. Default value is 0b. (Further details on this bit can be obtained in the 82559 Fast Ethernet Multifunction PCI/CardBus Datasheet.)
12	Reserved	This bit is reserved and should be set to 0b.
11	Boot Disable	The Boot Disable bit disables the Expansion ROM Base Address Register (PCI Configuration space, offset 30 hexadecimal) when it is set. Default value is 0b.
10:8	Revision ID	These three bits are used as the three least significant bits of the device revision. The default value depends on the silicon revision (for example, the 82559 C-Step's Revision ID is 09h).
7	Reserved	This bit is reserved and should be set to 1b.
6	Deep Power Down	This bit either enables or disables Deep Power Down in the D2 or D3 states when PME is disabled: '0' Deep Power Down is enabled in D3 state if PME-Disabled '1' Deep Power Down disabled in D3 state when PME-Disabled.
5:2	Reserved	These are reserved and should be set to 0000b.
1	Standby Enable	The Standby Enable bit enables the 82559 to enter standby mode. When this bit equals 1b, the 82559 is able to recognize an idle state and can enter standby mode (some internal clocks are stopped for power saving purposes). The 82559 does not require a PCI clock signal in standby mode. If this bit equals 0b, the idle recognition circuit is disabled and the 82559 always remains in an active state. Thus, the 82559 will always request PCI CLK using the Clockrun mechanism.
0	Reserved	This bit is reserved and should be set to 0b.

Note: Write timing specifications are critical and not all manufacturers timing specifications are exactly the same.

3.2 The 82558 Serial EEPROM

A 5 V EEPROM (93C64) must be used with the 82558. Timing specifications from the EEPROM device datasheet should be taken into consideration for compatibility with the 82559ER.

Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	Sig (01b)		ID	0b	BD	Rev ID			PM	0b	WOL	00b		Clk En	PHY Address	

Note: Bits 12, 6, and 4:3 are reserved in the 82558 EEPROM and should be set to 0.

Table 3. 82558 EEPROM Word A Field Descriptions

Bits	Name	Description
15:14	Signature	The Signature field is a signature of 01b, indicating to the 82558 that there is a valid EEPROM present. If the Sig field is not 01b, the other bits are ignored and the default values are used.
13	ID	The ID bit indicates how the Subsystem ID and Subsystem Vendor ID fields are used. Default value is 0b.
12	Reserved	This bit is reserved and should be set to 0b.
11	Boot Disable	The Boot Disable bit disables the Expansion ROM Base Address Register (offset 30 hexadecimal) when it is set. Default value is 0b.
10:8	Revision ID	These three bits are used as the three least significant bits of the device revision. The default value depends on the silicon revision.
7	Power Management	The Power Management bit enables the 82558 whether to activate the power management abilities. If this bit is set, the 82558 will set the Cap_Ptr register to zero indicating no PCI compliant power management capabilities. Default value is 0b.
6	Reserved	This bit is reserved and should be set to 0b.
5	Wake on LAN	The WOL bit is sets the 82558 into WOL mode. When in this mode the 82558 reads three additional words from the EEPROM from word addresses 0h, 1h, and 2h. These words are expected to hold the MAC Individual Address. After reading these words the 82558 wakes the system by asserting PME# when a wake-up packet is received. Default value is 0b.
4:3	Reserved	These bits should be set to 000b.
2	Clock Enable	The Clock Enable bit enables (0) or disables (1) the 25 MHz clock output on the Clock Out (CLKOUT) signal (pin 27). The default value is 0.
1:0	PHY Address	These two bits are used as PHY address whenever a valid EEPROM exists; otherwise, the default value of 1h is used.

Note: Write timing specifications are critical and not all manufacturers timing specifications are exactly the same.

4.0 82559ER Board Design Considerations

4.1 Clock Source

The 82559ER can operate from either its internal oscillator using a 25 MHz crystal or an external oscillator as a 25 MHz clock source. If a crystal is used, then it should be connected across the X1 and X2 input pins. If an external oscillator is used, then it can be connected directly to the X1 input, with X2 left unconnected. In both cases the clock should be accurate within 25 ppm. The 82559ER can also provide its internal clock as an output on the CLK25 pin (pin N9, which is multiplexed with FLA[16]). The clock out function is enabled by asserting the CLKEN pin during PCI reset. The CLKEN pin is multiplexed with FLA[7].

A sampling of crystals that meet the specifications outlined is listed below:

Manufacturer	Manufacturer's Part Number
Raltron	TT-SMDC-25.00-20-T
Epson-Seiko	MA-406-25.000 @ 20%
Epson-Seiko	MA-406-25.000M-20PF

4.2 LED Indicators

The 82559ER provides three indication LED outputs:

- Link (LILED)
- Activity (ACTLED)
- Speed (SPEEDLED)

The 82559ER can sink up to 10 mA of current in the LEDs.

4.3 Magnetics

4.3.1 Magnetics Selection

One of the most critical component choices in a Fast Ethernet design is the magnetics module. The module has a critical effect on overall IEEE and emissions compliance. The device selected should meet the performance required for a design. Occasionally, components that meet basic specifications may cause the system (LOM, adapter, repeater, etc.) to fail because of unintentional interactions with board effects. Examples of these phenomena could be an unexpected series or parallel capacitance values or unexpected series inductance values within the magnetics module. This could cause the overall design to fail certain IEEE specifications. Qualifying a new magnetics module can help to alleviate these sorts of issues. The three-step process outlined below is recommended when evaluating suppliers:

1. Verify vendor's specification.

   The component should have more margins than the system specification. For example, "Does the module have a minimum of 400 µH of open circuit inductance (OCL) with 8 mA of DC bias?".

2. Check module's electrical qualifications.

   The electrical specifications of the module should be verified by performing stand-alone electrical qualification. Several modules should be tested (not in circuit) with two goals in mind:

   a. Does the component meet the published specifications?

   b. Does the vendor's published data correlate to the measured data?

3. Perform IEEE conformance tests.

   System level IEEE PHY conformance and EMC (FCC and EN) testing should be done to verify that the system meets all electrical requirements with the new component.

A sampling of modules that meet the specifications outlined is listed below:

Manufacturer	Manufacturer's Part Number
Pulse Engineering	H1012T
Bel Fuse	S558-5999-46
Delta Electronics	LF8200M

4.3.2 82558 and 82559ER Magnetic Circuit Differences

The most noticeable difference in external component connections between the 82558 and the 82559ER is how the component drives the magnetic device. Improvements made in the 82559ER transmit differential pair (TDP/TDN) circuitry require a change in the connection to the magnetics. The following subsections describe the differences in the magnetic interfaces.

However, the connection from the magnetic device to the RJ45 connector is the same for both the 82558 and 82559ER.

4.3.2.1 82559ER Magnetic Interface

The reference design in Appendix A illustrates the interface between the 82559ER and the magnetic device. The following should be noted:

1. The magnetics center tap on the transmit side is not connected to V_{CC} as in an 82558 design.
2. The pull-up resistors on the transmit differential pins (TDP and TDN) of the 82558 are not required for an 82559ER design.
3. A single 100 Ω termination resistor may be used between the transmit differential pair and one between the receive differential pair.
4. A single 100 Ω to 120 Ω may be used between the receive differential pair (RDP and RDN) of the 82559ER. The value used depends on the trace impedance of the printed circuit board.
5. A 0.1 mF capacitor on the center tap of the receive pair winding is required.
6. The capacitor that connects the junction of the two 49.1 Ω resistors on the receive differential pair (RDP and RDN) to ground in the 82558 design must be removed.
7. The 1500 pF capacitor (C5 in the reference design) helps eliminate ESD.
8. Although it is typically not required, additional capacitance may be required on the center tap of the transmit pair winding for FCC conformance. The value can range from 8 pF to 22 pF. However, it should be noted that the additional capacitance can lead to a trade-off between overshoot and return loss.

4.3.2.2 82558 Magnetic Interface

The reference design in Appendix A illustrates the interface between the 82558 and the magnetics module. The following should be noted:

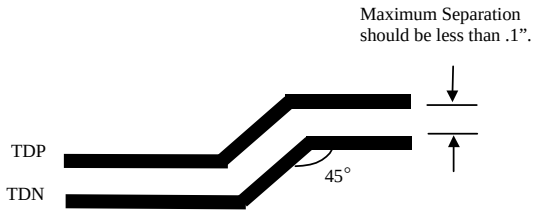
1. The magnetics center tap on the transmit side is connected to V_{CC}.
2. Parallel capacitors (C1 and C2 in the reference design) on the center tap of the transmit pair winding are required.
3. Identical resistance on the transmit differential and receive differential pairs is needed.
4. Additional capacitance is needed in the receive differential pair circuitry (C4 and C5 in the 82558 reference design).
5. A connection does not exist between on the transformer's center tap on the Receive Pair that interface

Note: Some components shown are not necessary for operation but may be required under special circumstances. For example, capacitance between the transmit differential pair (TDP and TDN) is not required but may be needed.

4.4 Trace Routing

Trace routing considerations for final layout are described in the LAN On Motherboard (LOM) Design Guide Application Note (AP-391). Critical layout issues are covered in the following section for completeness. Critical signal traces should be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals, including those propagated through power and ground planes. Capacitive loading, which is caused by the signal trace, can also be reduced by keeping the traces as short as possible. Maximum separation between differential pairs should be no more than one tenth of an inch as illustrated in the figure below.

Figure 1. Measuring Maximum Separation



4.5 Signal Terminations

49.9 Ω (1%) resistors are used to terminate the transmit differential (TDP/TDN) and receive differential (RDP/RDN) pairs. They should be placed as close to the 82559ER as possible.

Note: It is permissible to use a single 100 Ω (1%) resistor in place of the 49.9 (1%) resistors.

4.5.1 Termination Plane

Resistors are used to terminate noise from the unused inputs of both the RJ45 connector and the magnetics module to the termination plane. The netname TERMPLANE (for termination plane) is provided as a guide to the termination plane. A termplane is a plane fabricated into the printed circuit board (PCB) substrate. This plane, which has no DC termination, acts like a capacitive path for the coupled noise.

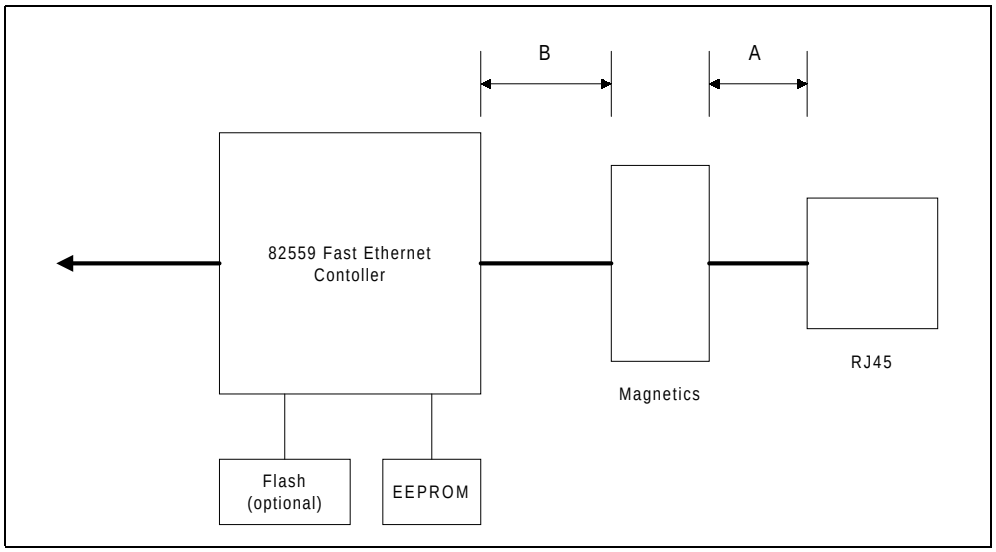
4.5.2 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of cross-talk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for additional capacitance, which may be required due to failure of electrical fast transient testing.

4.6 Critical Dimensions

There are two critical dimensions that must be considered during the layout phase of an 82559ER LOM implementation. These dimensions are identified in Figure 2 as A and B:

Figure 2. Critical Dimensions for Component Placement



4.6.1 Distance A: Magnetics to RJ45 (Priority 1)

The distance labeled “A” in Figure 2 should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

1. Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
2. Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit.

If the 82559ER must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping distance A as short as possible should be a priority.

4.6.2 Distance B: PHY to Magnetics (Priority 2)

Distance B from Figure 2 should also be designed to extend less than one inch between devices. The high speed nature of the signals propagating through these traces requires that the distance between these components are closely observed. In general, any section of traces that is intended for use with high speed signals should observe proper termination practices.

Proper termination of signals can reduce reflections caused by impedance mismatches between devices and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value.

5.0 Power Supply Requirements

WOL designs require a segmented power supply. The auxiliary power supply (+3.3VSB) is used to provide the trickle power necessary to keep key components operational in WOL mode.

5.1 +3.3VSB Power Requirement

In designs that utilize 3.3VSB, the 82559ER will operate from this supply in all operational states. Therefore, the +3.3VSB must be capable of supplying 175 mA of current (worst case requirements for the 82559ER).

5.2 +3.3VSB Power Recommendation

Ideally the power supply will provide an AUX_GOOD signal. The AUX_GOOD signal indicates that the auxiliary power supply is ready to provide stable power and is similar to the PWR_GOOD signal on many of today's common power supplies.

Note: The AUX_GOOD signal from the power supply is the same as the ALTRST# signal of the 82559ER.

6.0 Signal Descriptions

6.1 Signal Type Definitions

Type	Name	Description
IN	Input	The input pin is a standard input only signal.
OUT	Output	The output pin is a Totem Pole Output pin and is a standard active driver.
T/S	Tri-State	The tri-state pin is a bidirectional, input/output pin.
S/T/S	Sustained Tri-State	The sustained tri-state pin is an active low tri-state signal owned and driven by one agent at a time. The agent asserting the S/T/S pin low must drive it high at least one clock cycle before floating the pin. A new agent can only assert an S/T/S signal low one clock cycle after it has been tri-stated by the previous owner.
O/D	Open Drain	The open drain pin allows multiple devices to share this signal as a wired-OR.
A/I	Analog Input	The analog input pin is used for analog input signals.
A/O	Analog Output	The analog output pin is used for analog output signals.
B	Bias	The bias pin is an input bias.

6.2 PCI Bus Interface Signals

6.2.1 Address and Data Signals

Symbol	Type	Name and Function
AD[31:0]	T/S	**Address and Data.** The address and data lines are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. During the address phase, the address and data lines contain the 32-bit physical address. For I/O, this is a byte address; for configuration and memory, it is a Dword address. The 82559 uses little-endian byte ordering (in other words, AD[31:24] contain the most significant byte and AD[7:0] contain the least significant byte). During the data phases, the address and data lines contain data.
C/BE[3:0]#	T/S	**Command and Byte Enable.** The bus command and byte enable signals are multiplexed on the same PCI pins. During the address phase, the C/BE# lines define the bus command. During the data phase, the C/BE# lines are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
PAR	T/S	**Parity.** Parity is even across AD[31:0] and C/BE[3:0]# lines. It is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction.Once PAR is valid, it remains valid until one clock after the completion of the current data phase. The master drives PAR for address and write data phases; and the target, for read data phases.

6.2.2 Interface Control Signals

Symbol	Type	Name and Function
FRAME#	S/T/S	**Cycle Frame.** The cycle frame signal is driven by the current master to indicate the beginning and duration of a transaction. FRAME# is asserted to indicate the start of a transaction and de-asserted during the final data phase.
IRDY#	S/T/S	**Initiator Ready.** The initiator ready signal indicates the bus master's ability to complete the current data phase and is used in conjunction with the target ready (TRDY#) signal. A data phase is completed on any clock cycle where both IRDY# and TRDY# are sampled asserted (low) simultaneously.
TRDY#	S/T/S	**Target Ready.** The target ready signal indicates the selected device's ability to complete the current data phase and is used in conjunction with the initiator ready (IRDY#) signal. A data phase is completed on any clock cycle where both IRDY# and TRDY# are sampled asserted (low) simultaneously.
STOP#	S/T/S	**Stop.** The stop signal is driven by the target to indicate to the initiator that it wishes to stop the current transaction. As a bus slave, STOP# is driven by the 82559 to inform the bus master to stop the current transaction. As a bus master, STOP# is received by the 82559 to stop the current transaction.
IDSEL	IN	**Initialization Device Select.** The initialization device select signal is used by the 82559 as a chip select during PCI configuration read and write transactions. This signal is provided by the host in PCI systems.
DEVSEL#	S/T/S	**Device Select.** The device select signal is asserted by the target once it has detected its address. As a bus master, the DEVSEL# is an input signal to the 82559 indicating whether any device on the bus has been selected. As a bus slave, the 82559 asserts DEVSEL# to indicate that it has decoded its address as the target of the current transaction.
REQ#	T/S	**Request.** The request signal indicates to the bus arbiter that the 82559 desires use of the bus. This is a point-to-point signal and every bus master has its own REQ#.
GNT#	IN	**Grant.** The grant signal is asserted by the bus arbiter and indicates to the 82559 that access to the bus has been granted. This is a point-to-point signal and every master has its own GNT#.
INTA#	O/D	**Interrupt A.** The interrupt A signal is used to request an interrupt by the 82559. This is an active low, level triggered interrupt signal.
SERR#	O/D	**System Error.** The system error signal is used to report address parity errors. When an error is detected, SERR# is driven low for a single PCI clock.
PERR#	S/T/S	**Parity Error.** The parity error signal is used to report data parity errors during all PCI transactions except a Special Cycle. The parity error pin is asserted two clock cycles after the error was detected by the device receiving data. The minimum duration of PERR# is one clock for each data phase where an error is detected. A device cannot report a parity error until it has claimed the access by asserting DEVSEL# and completed a data phase.

6.2.3 System and Power Management Signals

Symbol	Type	Name and Function
CLK	IN	**Clock.** The Clock signal provides the timing for all PCI transactions and is an input signal to every PCI device. The 82559 requires a PCI Clock signal (frequency greater than or equal to 16 MHz) for nominal operation. The 82559 supports Clock signal suspension using the Clockrun protocol.
CLKRUN#	IN/OUT O/D	**Clockrun.** The Clockrun signal is used by the system to pause or slow down the PCI Clock signal. It is used by the 82559 to enable or disable suspension of the PCI Clock signal or restart of the PCI clock. When the Clockrun signal is not used, this pin should be connected to an external pull-down resistor.
RST#	IN	**Reset.** The PCI Reset signal is used to place PCI registers, sequencers, and signals into a consistent state. When RST# is asserted, all PCI output signals will be tri-stated.
PME# (PCI)	O/D	**Power Management Event.** The Power Management Event signal indicates that a power management event has occurred in a PCI bus system.
ISOLATE#	IN	**Isolate.** The Isolate signal is used to isolate the 82559 from the PCI bus. When Isolate is active (low), the 82559 does not drive its PCI outputs (except PME#) or sample its PCI inputs (including CLK and RST#). If the 82559 is not powered by an auxiliary power source, The ISOLATE# pin should not be connected.
ALTRST#	IN	**Alternate Reset.** The Alternate Reset signal is used to reset the 82559 on power-up. In systems that support an auxiliary power supply, ALTRST# should be connected to a power-up detection circuit. Otherwise, ALTRST# should be tied to Vcc.
VIO	B IN	**Voltage Input/Output.** The VIO pin is a voltage bias pin. It should be connected to +5 volts in a 5 V system and +3.3 volts in a 3.3 V system (in other words, the VIO pin should be connected to the voltage that the PCI interface operates at).

6.3 Local Memory Interface Signals

Symbol	Type	Name and Function
FLD[7:0]	T/S	**Flash Data Input/Output.** These pins are used for Flash data interface.
FLA[16]/ CLK25	OUT	**Flash Address[16]/25 MHz Clock.** This multiplexed pin is controlled by the status of the Flash Address[7] (FLA[7]) pin. If FLA[7] is left floating, this pin is used as FLA[16]; otherwise, if FLA[7] is connected to a pull-up resistor, this pin is used as a 25 MHz clock.
FLA[15]/ EESK	OUT	**Flash Address[15]/EEPROM Data Output.** During Flash accesses, this multiplexed pin acts as the Flash Address [15] output signal. During EEPROM accesses, it acts as the serial shift clock output to the EEPROM.
FLA[14]/ EEDO	IN/OUT	**Flash Address[14]/EEPROM Data Output.** During Flash accesses, this multiplexed pin acts as the Flash Address [14] output signal. During EEPROM accesses, it acts as serial input data to the EEPROM Data Output signal.

Symbol	Type	Name and Function
FLA[13]/ EEDI	OUT	**Flash Address[13]/EEPROM Data Input.** During Flash accesses, this multiplexed pin acts as the Flash Address [13] output signal. During EEPROM accesses, it acts as serial output data to the EEPROM Data Input signal.
FLA[12:8]	OUT	**Flash Address[12].** These pins act as the Flash Address[12:8] output signals.
FLA[7]/ CLKEN	T/S	**Flash Address[7]/Clock Enable.** This is a multiplexed pin and acts as the Flash Address[7] output signal during nominal operation. When the PCI RST# signal is active, this pin acts as input control over the FLA[16]/CLK25 output signal. If the FLA[7]/CLKEN pin is connected to a pull-up resistor (3.3 KW), a 25 MHz clock signal is provided on the FLA[16]/CLK25 output; otherwise, it is used as FLA[16] output.
FLA[6:2]	OUT	**Flash Address[6:2].** These pins are used as Flash address outputs to support 128 Kbyte Flash addressing.
FLA[1]/ AUXPWR	T/S	**Flash Address[1]/Auxiliary Power.** This multiplexed pin acts as the Flash Address[1] output signal during nominal operation. When RST is active (low), it acts as the power supply indicator. If the 82559 is fed PCI power, this pin should be connected to a pull-down resistor; if fed by auxiliary power, a pull-up resistor.
FLA[0]/ PCIMODE#	T/S	**Flash Address [0]/PCI Mode.** This multiplexed pin acts as the Flash Address[0] output signal during nominal operation. When RST# is active (low), it acts as the input system type.
EECS	OUT	**EEPROM Chip Select.** The EEPROM Chip Select signal is used to assert chip select to the serial EEPROM.
FLCS#	OUT	**Flash Chip Select.** The Flash Chip Select signal is active during Flash.
FLOE#	OUT	**Flash Output Enable.** This pin provides an active low output enable control to the Flash.
FLWE#	OUT	**Flash Write Enable.** This pin provides an active low write enable control to the Flash.

6.4 Testability Port Signals

Symbol	Type	Name and Function
TEST	IN	**Test.** If this input pin is high, the 82559 will enable the test port. During nominal operation this pin should be connected to a pull-down resistor.
TCK	IN	**Testability Port Clock.** This pin is used for the Testability Port Clock signal.
TI	IN	**Testability Port Data Input.** This pin is used for the Testability Port Data Input signal.
TEXEC	IN	**Testability Port Execute Enable.** This pin is used for the Testability Port Execute Enable signal.
TO	OUT	**Testability Port Data Output.** This pin is used for the Testability Port Data Output signal.

6.5 PHY Signals

Symbol	Type	Name and Function
X1	A/I	**Crystal Input One.** X1 and X2 can be driven by an external 3.3 V 25 MHz crystal. Otherwise, X1 may be driven by an external metal-oxide semiconductor (MOS) level 25 MHz oscillator when X2 is left floating.
X2	A/O	**Crystal Input Two.** X1 and X2 can be driven by an external 3.3 V 25 MHz crystal. Otherwise, X1 may be driven by an external MOS level 25 MHz oscillator when X2 is left floating.
TDP TDN	A/O	**Analog Twisted Pair Ethernet Transmit Differential Pair.** These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface directly with an isolation transformer.
RDP RDN	A/I	**Analog Twisted Pair Ethernet Receive Differential Pair.** These pins receive the serial bit stream from the isolation transformer. The bit stream can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation.
ACTLED#	OUT	**Activity LED.** The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off.
LILED#	OUT	**Link Integrity LED.** The Link Integrity LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if link is invalid, the LED is off.
SPEEDLED#	OUT	**Speed LED.** The Speed LED pin indicates the speed. The speed LED will be on at 100 Mbps and off at 10 Mbps.
RBIAS100	B	**Reference Bias Resistor (100 Mbps).** This pin should be connected to a 600 Ω pull-down resistor.[a]
RBIAS10	B	**Reference Bias Resistor (10 Mbps).** This pin should be connected to a 575 Ω pull-down resistor.[b]
VREF	B	**Voltage Reference.** This pin is connected to a 1.25 V ± 1% external voltage reference generator. To use the internal voltage reference source, this pin should be left floating.

a. 600 Ω for RBIAS100 is only a recommended value and should be fine tuned for various designs.
b. 575 Ω for RBIAS10 is only a recommended value and should be fine tuned for various designs.

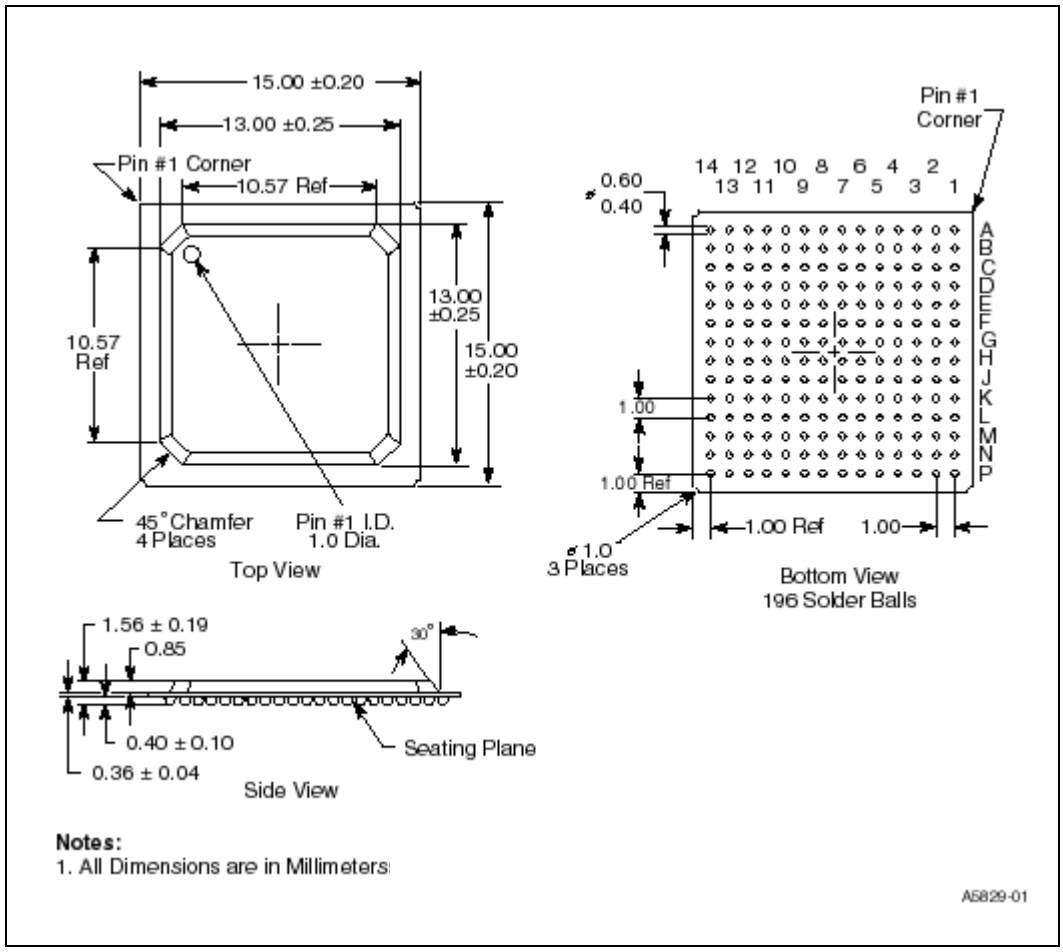
7.0 Package and Pinout Information

7.1 Package Information

7.1.1 82559ER Package Information

The 82559ER is a 196-pin Ball Grid Array (BGA) package. Package dimensions are shown in Figure 3. More information on Intel device packaging is available in the Intel Packaging Handbook, which is available from the Intel Literature Center or your local Intel sales office.

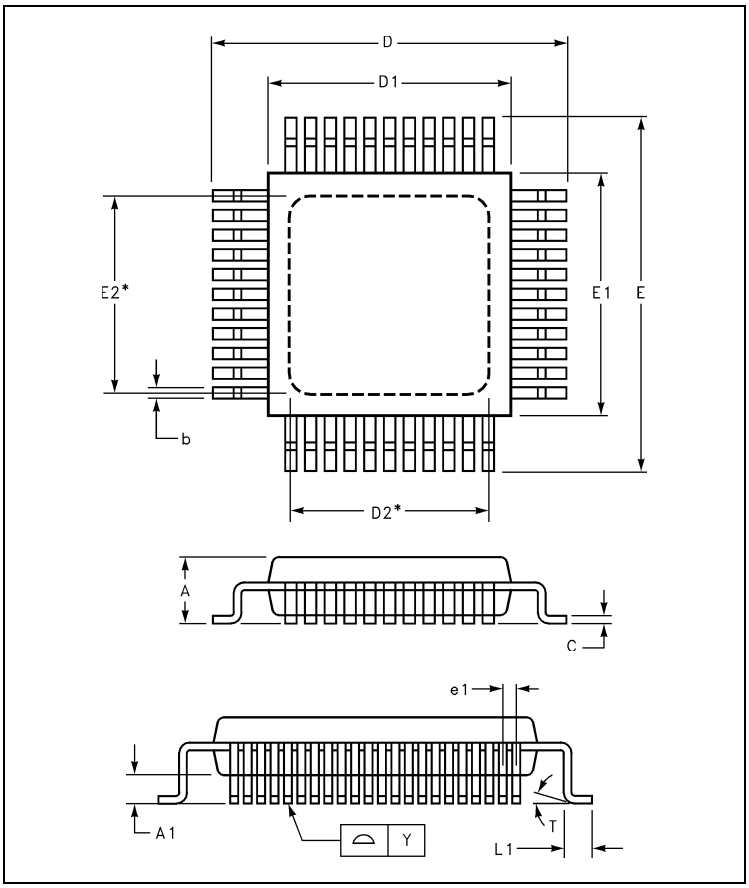
Figure 3. Dimension Diagram for the 82559ER 196-pin BGA



7.1.2 82558 Package Information

The 82558 is a 208-pin Shrink Quad Plat Pack (SQFP) device. Package dimensions are shown Figure 4. More information on Intel device packaging is available in the Intel Packaging Handbook, which is available from the Intel Literature Center or your local Intel sales office.

Figure 4. Dimension Diagram for the 82558 SQFP



NOTE: The distances labeled D2 and E2 refer to the measurement of the heatslug. They do not refer to the end-to-end pin distance.

Table 4. Dimensions for the 208-pin SQFP

Symbol	Description	Min	Max
A	Overall Height	3.25	3.75
A1	Stand Off	0	0.30
b	Lead Width	0.14	0.26
c	Lead Thickness	0.150	0.188
D	Terminal Dimension	30.2	31.0
D1	Package Body	27.9	28.1
E	Terminal Dimension	30.2	31.0

Table 4. Dimensions for the 208-pin SQFP

Symbol	Description	Min	Max
E1	Package Body	27.9	28.1
e1	Lead Pitch	0.40	0.60
L1	Foot Length	0.30	0.70
T	Lead Angle	0.0°	10.0°
Y	Coplanarity	0.1	0.1
D2/E2	Heatslug	21	21

7.2 Pinout Information

7.2.1 82559ER Pinout Information

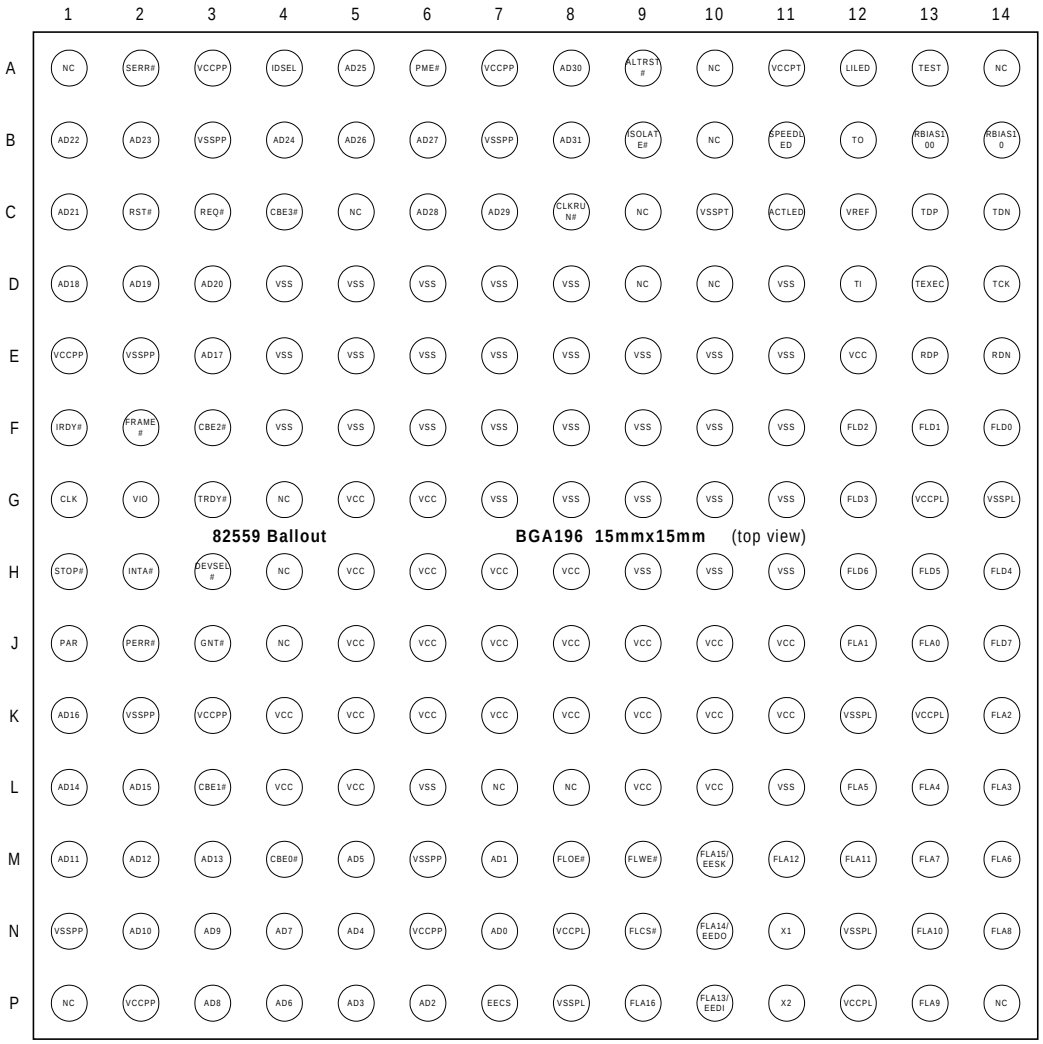
Table 5. 82559ER Pin Assignments

Pin	Name	Pin	Name	Pin	Name
A1	NC	A2	SERR#	A3	VCCPP
A4	IDSEL	A5	AD25	A6	PME#
A7	VCCPP	A8	AD30	A9	ALTRST#
A10	NC	A11	VCCPT	A12	LILED
A13	TEST	A14	NC		
B1	AD22	B2	AD23	B3	VSSPP
B4	AD24	B5	AD26	B6	AD27
B7	VSSPP	B8	AD31	B9	ISOLATE#
B10	NC	B11	SPEEDLED	B12	TO
B13	RBIAS100	B14	RBIAS10		
C1	AD21	C2	RST#	C3	REQ#
C4	C/BE3#	C5	NC	C6	AD28
C7	AD29	C8	CLKRUN#	C9	NC
C10	VSSPT	C11	ACTLED	C12	VREF
C13	TDP	C14	TDN		
D1	AD18	D2	AD19	D3	AD20
D4	VSS	D5	VSS	D6	VSS
D7	VSS	D8	VSS	D9	NC
D10	NC	D11	VSS	D12	TI
D13	TEXEC	D14	TCK		
E1	VCCPP	E2	VSSPP	E3	AD17
E4	VSS	E5	VSS	E6	VSS
E7	VSS	E8	VSS	E9	VSS
E10	VSS	E11	VSS	E12	VCC
E13	RDP	E14	RDN		
F1	IRDY#	F2	FRAME#	F3	C/BE2#
F4	VSS	F5	VSS	F6	VSS
F7	VSS	F8	VSS	F9	VSS
F10	VSS	F11	VSS	F12	FLD2
F13	FLD1	F14	FLD0		
G1	CLK	G2	VIO	G3	TRDY#
G4	NC	G5	VCC	G6	VCC
G7	VSS	G8	VSS	G9	VSS
G10	VSS	G11	VSS	G12	FLD3

Table 5. 82559ER Pin Assignments

Pin	Name	Pin	Name	Pin	Name
G13	VCCPL	G14	VSSPL		
H1	STOP#	H2	INTA#	H3	DEVSEL#
H4	NC	H5	VCC	H6	VCC
H7	VCC	H8	VCC	H9	VSS
H10	VSS	H11	VSS	H12	FLD6
H13	FLD5	H14	FLD4		
J1	PAR	J2	PERR#	J3	GNT#
J4	NC	J5	VCC	J6	VCC
J7	VCC	J8	VCC	J9	VCC
J10	VCC	J11	VCC	J12	FLA1
J13	FLA0	J14	FLD7		
K1	AD16	K2	VSSPP	K3	VCCPP
K4	VCC	K5	VCC	K6	VCC
K7	VCC	K8	VCC	K9	VCC
K10	VCC	K11	VCC	K12	VSSPL
K13	VCCPL	K14	FLA2		
L1	AD14	L2	AD15	L3	C/BE#1
L4	VCC	L5	VCC	L6	VSS
L7	NC	L8	NC	L9	VCC
L10	VCC	L11	VSS	L12	FLA5
L13	FLA4	L14	FLA3		
M1	AD11	M2	AD12	M3	AD13
M4	C/BE0#	M5	AD5	M6	VSSPP
M7	AD1	M8	FLOE#	M9	FLWE#
M10	FLA15/EESK	M11	FLA12	M12	FLA11
M13	FLA7	M14	FLA6		
N1	VSSPP	N2	AD10	N3	AD9
N4	AD7	N5	AD4	N6	VCCPP
N7	AD0	N8	VCCPL	N9	FLCS#
N10	FLA14/EEDO	N11	X1	N12	VSSPL
N13	FLA10	N14	FLA8/IOCHRDY		
P1	NC	P2	VCCPP	P3	AD8
P4	AD6	P5	AD3	P6	AD2
P7	EECS	P8	VSSPL	P9	FLA16
P10	FLA13/EEDI	P11	X2	P12	VCCPL
P13	FLA9	P14	NC		

Figure 5. 82559ER Ball Identification Diagram



7.2.2 82558 Pinout Information

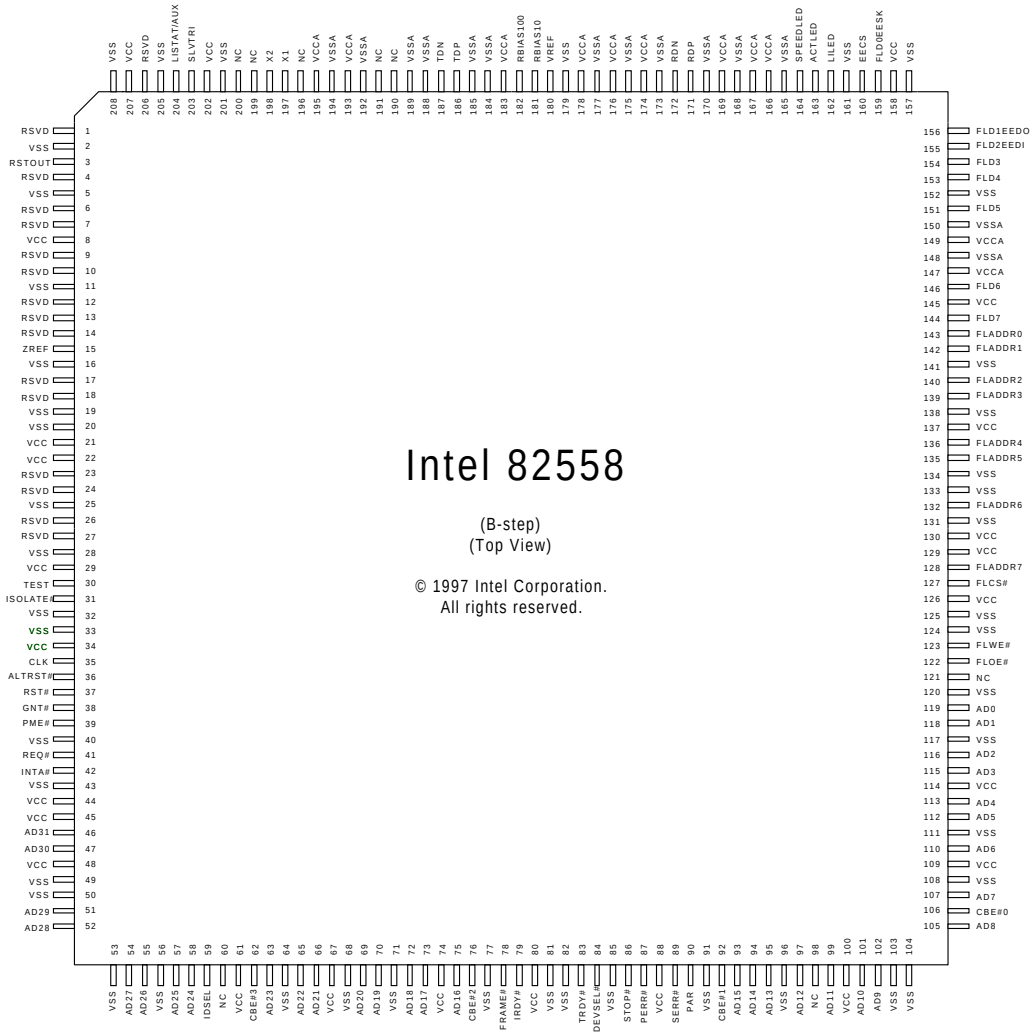
Table 6. 82558 Pin Assignments

Pin	Name	Pin	Name	Pin	Name
1	RSVD	2	VSS	3	RSTOUT
4	RSVD	5	VSS	6	RSVD
7	RSVD	8	VCC	9	RSVD
10	RSVD	11	VSS	12	RSVD
13	RSVD	14	RSVD	15	ZREF
16	VSS	17	RSVD	18	RSVD
19	VSS	20	VSS	21	VCC
22	VCC	23	RSVD	24	RSVD
25	VSS	26	RSVD	27	CLKOUT
28	VSS	29	VCC	30	TEST
31	ISOLATE#	32	VSS	33	VSS
34	VCC	35	CLK	36	ALTRST#
37	RST#	38	GNT#	39	PME#
40	VSS	41	REQ#	42	INTA#
43	VSS	44	VCC	45	VCC
46	AD31	47	AD30	48	VCC
49	VSS	50	VSS	51	AD29
52	AD28	53	VSS	54	AD27
55	AD26	56	VSS	57	AD25
58	AD24	59	IDSEL	60	NC
61	VCC	62	CBE3#	63	AD23
64	VSS	65	AD22	66	AD21
67	VCC	68	VSS	69	AD20
70	AD19	71	VSS	72	AD18
73	AD17	74	VCC	75	AD16
76	CBE2#	77	VSS	78	FRAME#
79	IRDY#	80	VCC	81	VSS
82	VSS	83	TRDY#	84	DEVSEL#
85	VSS	86	TOP#	87	PERR#
88	VCC	89	SERR#	90	PAR
91	VSS	92	CBE1#	93	AD15
94	AD14	95	AD13	96	VSS
97	AD12	98	NC	99	AD11
100	VCC	101	AD10	102	AD9
103	VSS	104	VSS	105	AD8
106	CBE0#	107	AD7	108	VSS

Table 6. 82558 Pin Assignments

Pin	Name	Pin	Name	Pin	Name
109	VCC	110	AD6	111	VSS
112	AD5	113	AD4	114	VCC
115	AD3	116	AD2	117	VSS
118	AD1	119	AD0	120	VSS
121	NC	122	FLOE#	123	FLWE#
124	VSS	125	VSS	126	VCC
127	FLCS#	128	FLADDR7	129	VCC
130	VCC	131	VSS	132	FLADDR6
133	VSS	134	VSS	135	FLADDR5
136	FLADDR4	137	VCC	138	VSS
139	FLADDR3	140	FLADDR2	141	VSS
142	FLADDR1	143	FLADDR0	144	FLD7
145	VCC	146	FLD6	147	VCCA
148	VSSA	149	VCCA	150	VSSA
151	FLD5	152	VSS	153	FLD4
154	FLD3	155	FLD2/EEDI	156	FLD1/EEDO
157	VSS	158	VCC	159	FLD0/EESK
160	EECS	161	VSS	162	LILED
163	ACTLED	164	SPEEDLED	165	VSSA
166	VCCA	167	VCCA	168	VSSA
169	VCCA	170	VSSA	171	RDP
172	RDN	173	VSSA	174	VCCA
175	VSSA	176	VCCA	177	VSSA
178	VCCA	179	VSS	180	VREF
181	RBIAS10	182	RBIAS100	183	VCCA
184	VSSA	185	VSSA	186	TDP
187	TDN	188	VSSA	189	VSSA
190	NC	191	NC	192	VSSA
193	VCCA	194	VSSA	195	VCCA
196	NC	197	X1	198	X2
199	NC	200	NC	201	VSS
202	VCC	203	SLVTRI	204	LISTAT/AUX
205	VSS	206	RSVD	207	VCC
208	VSS				

Figure 6. 82558 Pin Identification Diagram



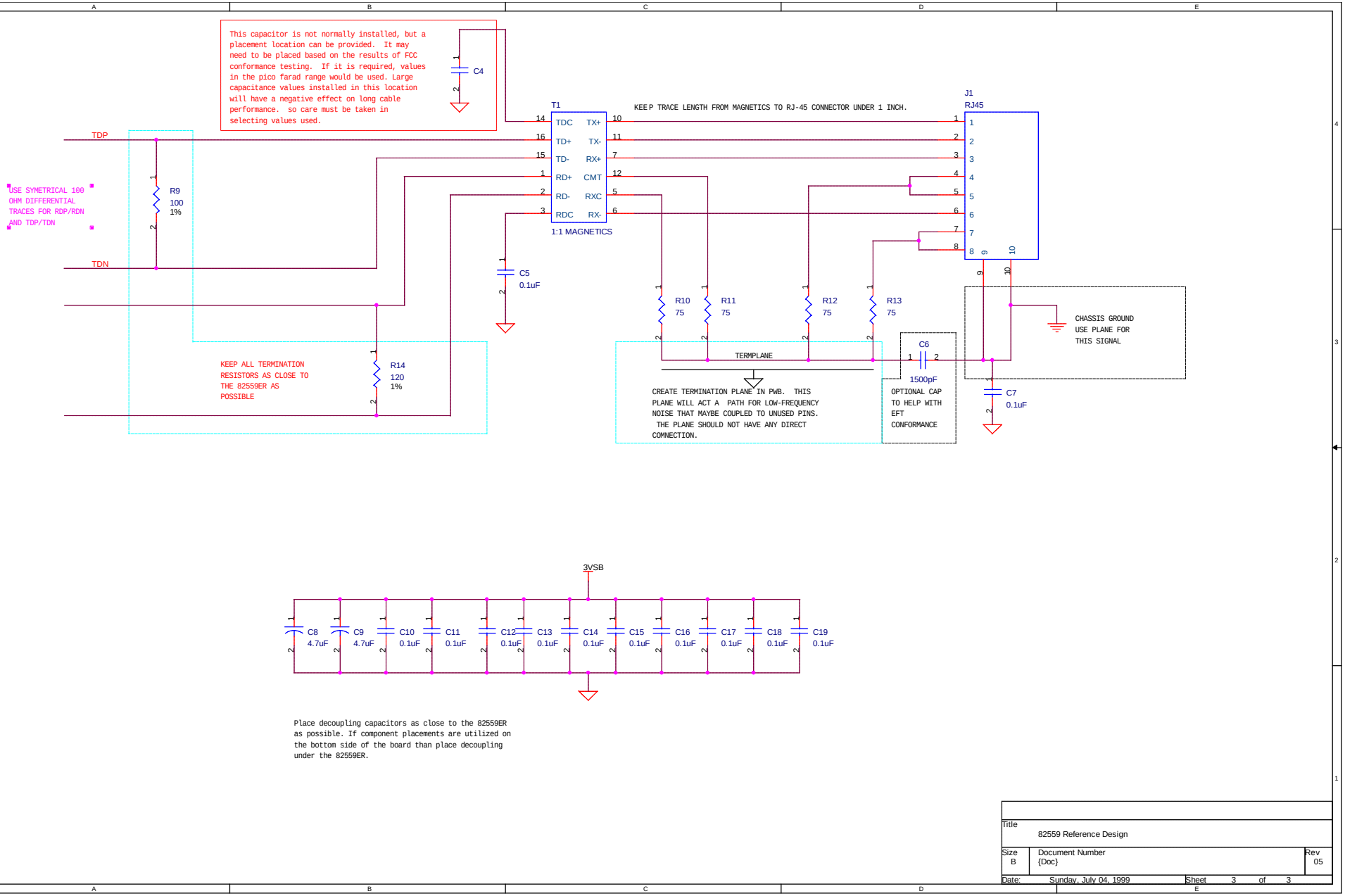
8.0 82559ER Bill of Materials

The following table is a bill of materials list for an 82559ER design.

Part	Part Number	Quantity	Reference Designator
22 pF Capacitor	C603C220J5GAC-T/R Kemet	2	C1, C2
0.1 uF Capacitor	0603YC104KAT$A AVX	3	C3, C5, C7
8.2 pF Capacitor		1	C4
1500 pF Capacitor		1	C6
LED		2	D1, D2
RJ45 connector	78186-003 Berg	1	J1
62 KΩ Resistor		3	R1, R2, R8
330 Ω Resistor	MCR03EZ$J#331 Rohm	2	R3, R4
549 Ω Resistor	ERJ3EKF5490FT Panasonic	1	R7
619 Ω Resistor	ERJ3EKF6190V Panasonic	1	R8
100 Ω Resistor	ERJ3EKF1000V Panasonic	2	R9, R14
75 Ω Resistor	EXB38V750JV Panasonic	4	R10, R11, R12, R13
1:1 Magnetics	H1112T Pulse Engineering	1	T1
82559ER	Intel	1	U1
93C46 EEPROM	AT92C46A-10SC2.7 Atmel	1	U2
PLCC Socket	821977-1 AMP	1	U3
25 MHz Crystal	TT-SMDC-25.000-20T Raltron	1	Y1

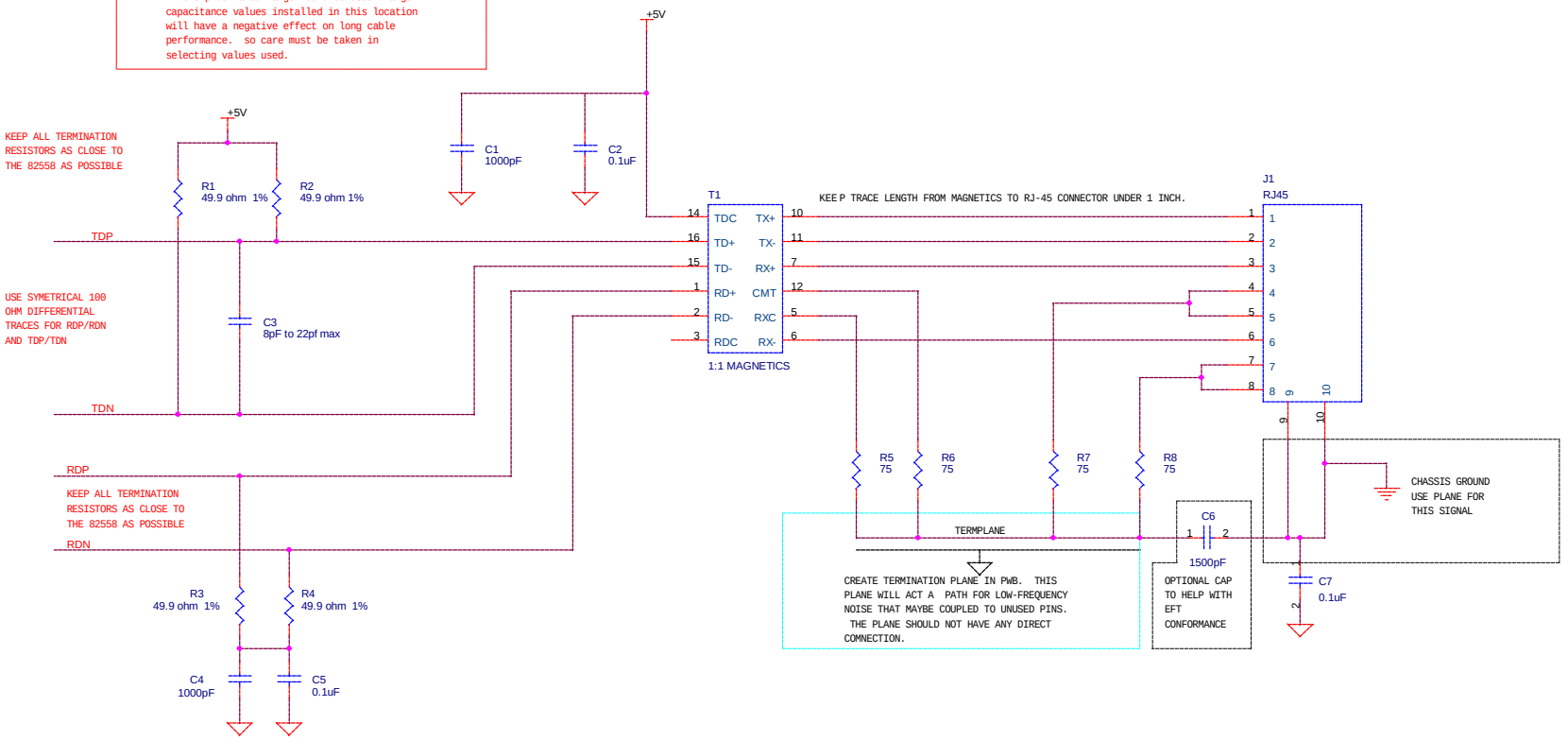
Appendix A: Reference Designs

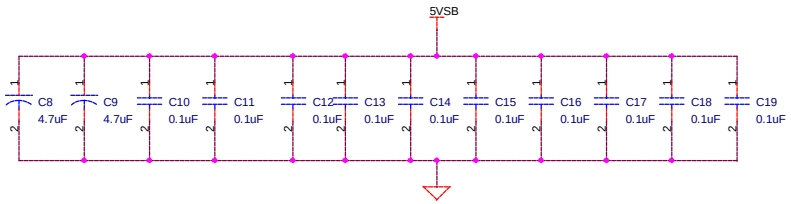
The following pages illustrate the differences of the magnetic interfaces between an 82559ER design and an 82558 design, respectively.



Title	82559 Reference Design	
Size B	Document Number {Doc}	Rev 05
Date: Sunday, July 04, 1999	Sheet 3 of 3	

Capacitor C3 is not normally installed, but a placement location should be provided. It may need to be placed based on the results of FCC conformance testing. If it is required, values in the pico farad range would be used. Large capacitance values installed in this location will have a negative effect on long cable performance. so care must be taken in selecting values used.





Place decoupling capacitors as close to the 82558 as possible. If component placements are utilized on the bottom side of the board than place decoupling under the 82558.

Title: S82558 Magnetic Interface		
Size: B	Document Number: {Doc}	Rev: 05
Date: Monday, July 19, 1999	Sheet 1 of 1	