82559ER EEPROM Map and Programming Information

Application Note (AP-406)

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Revision History

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July 1999	0.6	Initial release

Contents

1. Introduction and Scope

This document describes the EEPROM map and contents for products based upon the Intel 82559ER Fast Ethernet* controllers.

Part of the EEPROM is used for hardware configuration, while part of the EEPROM space is read by Intel-supplied drivers and other configuration software to determine and configure features specific to that design. For compatibility, Intel does not create separate drivers for the 82559ER controllers.

1.1 EEPROM Device and Interface

The serial EEPROM stores configuration data for the controller. The EEPROM is a 3.3 volt 9346 or 9366 Microwire* device. The 82559ER supports 64-word sized EEPROMs,

In PCI designs that do not use TCO functionality, the controller only requires an EEPROM that contains 64 registers of 16 bits per register. The 82559ER auto-detects the EEPROM size via a dummy zero mechanism following reset.

All accesses, read and write, are preceded by a command instruction to the EEPROM. The command instructions begin with a logical one as a start bit, two opcode bits (read, write, erase, etc.), and six bits of address. The address field is six bits for a 64 register EEPROM. The end of the address field is indicated by a dummy zero bit from the EEPROM. This indicates that the entire address field has been transferred to the EEPROM. A command is issued by asserting the EEPROM Chip Select (EECS) signal from the controller and clocking the data out of the EEPROM Data Input (EEDI) pin into the EEPROM on its data input pin relative to the EEPROM Shift Clock (EESK) controller output. The EECS signal is de-asserted after completion of the EEPROM cycle (command, address and data).

In designs employing 64-register EEPROM, the EEPROM read is approximately 6,000 clock cycles long (180 microseconds at 33 MHz). The system is required to provide a valid clock on the CLK pin for this time period after the de-assertion of RST#, even if the ISOLATE# pin is asserted (the CLK input is not isolated until the EEPROM accesses are complete).

The 82559ER performs an automatic read of three registers from the EEPROM after the de-assertion of reset. The 82559ER provides a sequence of $110A_5A_4A_3A_2A_1A_0b$ (start bit, read opcode, address) and read the 16 bits of data that follow the dummy zero, assuming the most significant bit first. The process is then repeated the for the next two addresses.

1.2 EEPROM Programming Procedure Overview

A device based on the 82559ER EEPROM can be programmed in-line at a Final Acceptance Test (FAT) station. This allows the use of a surface mount technology (SMT) EEPROM, which is otherwise difficult to handle with off-line automated programming equipment. The Bill of Materials (BOM) for an 82559-based solution requires a blank EEPROM (type 93C66 for TCO-enabled systems, type 93C46 otherwise). For the 82559, the image programmed into the EEPROM is specified by two controlled documents:

1. The 82559ER EEPROM Map and Programming Information (AP-406) application note (this document).

2. A program file that is unique for each printed board assembly (PBA) and contains the default EEPROM values for that particular PBA.

Note: *This file can be created in a simple text editor and follows the format shown in Appendix A of Application Note 394. Appendix A provides an example of an EEPROM map for a 82559-based design.*

EEPROMs may be pre-programmed prior to soldering it onto a board. Some LAN On Motherboard (LOM) designers may prefer this method over in-line programming.

The EEPROM image consists of two types of data: static data, which is fully described by this document, and dynamic (or serialized) data, which varies for each unit programmed. The dynamic data consists of the product's Ethernet Individual Address (IA) and the EEPROM checksum. In TCO systems, the heartbeat packet, SMBus address and heartbeat packet pointer are also dynamic data.

1.3 EEUPDATE Utility

Intel has created a DOS utility that meets the two basic requirements for an in-circuit programming utility. First, the utility can be used to update EEPROM images as part of an end-of-line production tool. Secondly, it can be used as a standalone development tool. The tool uses the two basic data files outlined in the following section (static data file, and IA address file).

The EEUPDATE utility is flexible and can be used to update the entire EEPROM image or to update only the IA address of the card. This utility is only available to OEM customers.

1.3.1 Command Line Parameters

The DOS command format is as follows:

EEUPDATE Parameter_ 1 Parameter_2
where:

- Parameter _1 = filename or /D
- Parameter_2 = filename or /A

Parameter 1 in this example case is file1.eep, which contains the complete EEPROM image in a specific format and is used to update the complete EEPROM. All comments in the ".eep" file must be preceded by a semicolon (;). The file names given here are only examples. Parameter 1 can also be a switch: /D. The switch /D implies, do not update the complete EEPROM image.

Parameter 2 in this example case is file2.dat, which contains a list of IA addresses. The EEUPDATE utility picks up the first unused address from this file and uses it to update the EEPROM. An address is marked as used by following the address with a date stamp. When the utility uses a specific address, it updates that address as used in a log file called eelog.dat. This file should then be used as the dat file for the next update. The Parameter 2 can also be /A, which implies, do not update the IA address.

2. 82559ER EEPROM Format and Contents

Table 1 shows the EEPROM map for the 82559ER. Each word listed is described in detail in following paragraphs.

Table 1. 82559ER EEPROM Address Map

E2P Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	IA byte 1								IA byte 0							
01	IA byte 3								IA byte 2							
02	IA byte 5								IA byte 4							
0A	SIG			ID	0	BD	Rev ID		1	Deep D PME	OL 0	0	0	0	ST B Ena	0
0B	Subsystem ID															
0C	Subsystem Vendor ID															

Words 00h through 02h are used by the hardware and are common to all controllers.

2.1 Ethernet Individual Address (Words 00-02h)

Ethernet Individual Address (IA) is a six-byte field that must be unique for each adapter card or board and unique for each copy of the EEPROM image. The first three bytes are vendor specific. The last three bytes must be unique for each copy of the EEPROM. It is anticipated that OEM versions of the product may be required to have non-Intel ID's in the first three byte positions. The Intel default is shown in the following table. Notice that the Ethernet Individual address is byte-swapped, as indicated next.

		Individual Address Byte / Value					
		Word 00		Word 01		Word 02	
Manufacturer	MAC Address	Byte 1	Byte 0	Byte 1	Byte 0	Byte 1	Byte 0
Intel	00AA00xxyyzz	AA	00	xx	00	zz	yy
Intel	00A0C9xxyyzz	A0	00	xx	C9	zz	yy
Intel	009027xxyyzz	90	00	xx	27	zz	yy

Note: The Individual Address (IA) bytes read from the EEPROM is used by the 82559ER until an IA Setup command is issued by software. The IA defined by the IA Setup command overrides the IA read from the EEPROM.

2.2 82559ER Product Identification

2.2.1 EEPROM ID (Word 0Ah)

The 82559ER Ethernet controller reads this register to obtain basic power-on configuration information. The format for this word has evolved substantially from controller to controller; this section applies only to the 82559ER.

The signature bits (15-14) of this word are used to indicate the validity of this word. If the signature bits are set to 01b, then the word is valid and the remaining contents of the word are used to determine configuration information. If the signature bits are not 01b, then the remainder of this word is ignored and the controller uses default values for its configuration.

Word A is the only section of the EEPROM map that affects the basic functionality of the 82559ER. Although other fields within the EEPROM are loaded into the controller, their impact is limited to loading values such as the IA address. Figure 1 shows the format of word 0Ah for the 82559ER.

15-14	13	12	11	10-8	7	6	5	4	3	2	1	0
SIG	ID	0	BD	Alt Rev ID	1	DDPD	0	IALED	0	0	STB Ena	0

Figure 1. 82559ER EEPROM ID Word 0Ah

These bits and their functions are described next.

2.2.2 82559ER Product Identification (Words 0B-0Ch)

Bit	Field Name	82559ER Word 0Ah Description
15:14	SIG	If the SIG field is 01b, then the remainder of the word is read to determine the basic functionality of the 82559. If the SIG is not loaded with 01b, then the remainder of the word is ignored and default configuration values are used for the parameters that are otherwise configured by word. 0Ah The default configuration values are: • Standby mode is disabled • Deep power down is enabled • Boot ROM enabled, boot expansion ROM base address register disabled. The Subsystem ID and System Vendor ID are both set to 0.
13	ID	This ID bit indicates how the Subsystem ID and Subsystem Vendor ID will be used. If the controller detects the presence of an EEPROM (as indicated by a value of 01b in bits 15 and 14), then bit 13, if set (1) causes the values stored in EEPROM, words 0Bh (Subsystem ID) and 0Ch (Subsystem Vendor ID), to be loaded into the Device ID and Vendor ID fields, respectively, in the PCI Configuration space. If bit 13 is clear (0), then the Device ID and Vendor ID fields in PCI Configuration space remain at the default values. See Section 2.2.2.
12	RSVD	This bit is reserved in the 82559ER. This bit cannot be reassigned to any other function.
11	BD	The Boot Disable bit disables the Expansion ROM Base Address Register (PCI Configuration space, offset 30H) when it is set. Default value is 0b. If the Boot Disable bit is set to '1', the 82559ER will not request an expansion ROM window.
10:8	Alt Rev ID	These three bits are used as the three least significant bits of the device revision, if bits 15, 14, and 13 equal 011b and the ID is set as described in Section 2.2.2, "82559ER Product Identification (Words 0B-0Ch)" on page 5. The default value depends on the silicon revision. These are the three LS bits of the 82559's rev ID field in the Ethernet PCI config space (the default rev ID of the 82559ER is 8 h). Note that the rev ID field in the EEPROM is active only if the ID field (bit 13) is also set.
7	PM	The Power Management bit reserved and should always '1' in the 82559ER (always enabled).
6	DDPD	For the 82559, this is the "Disable Deep Power Down while PME is disabled" bit. 0 - Deep Power Down is enabled in D3 state while PMEdisabled. 1 - Deep Power Down disabled in D3 state while PMEdisabled.
5	RSVD	This bit is reserved in the 82559ER and cannot be reassigned.
4	IA LED	IA LED controls the ACT LED functionality at WOL mode: '0' During WOL mode, the ACT LED is activated by a transmission and reception of broadcast and Individual Address match packets. 1' During WOL mode, the ACT LED is activated by a transmission and reception of Individual Address match packets only.
3	RSVD	This bit is reserved in the 82559ER and cannot be reassigned.
2	RSVD	This bit is reserved in the 82559ER and cannot be reassigned.
1	STB Ena	The Standby Enable bit enables the 82559ER to enter standby mode. When this bit equals 1b, the 82559ER is able to recognize an idle state and can enter standby mode (some internal clocks are stopped for power saving purposes). The 82559ER does not require a PCI clock signal in standby mode. If this bit equals 0b, the idle recognition circuit is disabled and the 82559ER always remains in an active state. Thus, the 82559ERalways requests PCI CLK using the Clockrun mechanism.
0	RSVD	This bit is reserved in the 82559ER and cannot be reassigned.

To support OEM branded products, the following optional fields provide additional information for the identification of the vendor and product. These optional fields have been implemented if they contain a value other than 0000h or FFFFh.

The 82559ER implements the Subsystem ID and Subsystem Vendor ID fields and reads the information from these locations in the EEPROM and uses it according to the PCI Specification, Revision 2.1. The Subsystem Vendor ID field identifies the vendor of an 82559-based solution. The Subsystem Vendor ID values are based upon the vendor's PCI Vendor ID and is controlled by the PCI Special Interest Group (SIG). The Subsystem ID field identifies the 82559-based specific solution implemented by the vendor indicated in the Subsystem Vendor ID field.

The 82559ER provides support for configurable Subsystem Vendor ID and Subsystem ID fields. After hardware reset is deasserted, the 82559ER automatically reads EEPROM words 0Ah through 0Ch. The first of these 16-bit values is used for controlling various 82559ER functions. The second is the Subsystem ID value, and the third is the Subsystem Vendor ID value. Again, the default values for the Subsystem ID and Subsystem Vendor ID are 0000h and 0000h, respectively.

The 82559ER checks bit numbers 15, 14, and 13 in the EEPROM, word 0Ah and behaves as described next.

Bits 15, 14 of Word 0Ah	Bit 13 of Word 0Ah	PCI Space Device ID	PCI Space Vendor ID	Revision ID	Subsystem ID	Subsystem Vendor ID
11, 10, 00	Don't care	1209h	8086h	Default	0000h	0000h
01	0	1209h	8086h	Default	Word 0Bh	Word 0Ch
01	1	value of word 0Bh	value of word 0Ch	Bits 10 -8 of word 0Ah	Word 0Bh	Word 0Ch

Note: The Revision ID is subject to change according to the silicon stepping.

The above table indicates that if the controller detects the presence of an EEPROM (as indicated by a value of 01b in bits 15 and 14), then bit 13, if set (1) causes the values stored in EEPROM, words 0Bh (Subsystem ID) and 0Ch (Subsystem Vendor ID), to be loaded into the Device ID and Vendor ID fields, respectively, in the PCI Configuration space. If bit 13 is clear (0), then the Device ID and Vendor ID fields in PCI Configuration space remain at the default values.

Between the deassertion of reset and the completion of the automatic EEPROM read, the 82559ER does not respond to any PCI configuration cycles. If the 82559ER happens to be accessed during this time, it retries the access.

2.2.3 Subsystem ID (Word 0Bh)

This one word (16 bit) field identifies the product number for the vendor. Intel generates this number for products that Intel creates. For OEM products, this number must be supplied and controlled by the OEM to avoid duplication of part numbers with the same Vendor ID number. Subsystem IDs for 82559-based Intel products are shown in the following table.

2.2.4 Subsystem Vendor ID (Word 0Ch)

This one word (16 bit) field identifies the OEM vendor. The code used for a particular vendor is the same code assigned as the Vendor ID by the PCI SIG.