21145 Phoneline/Ethernet LAN Controller

Hardware Reference Manual

April 1999

Order Number: 278211-001

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Introduction 1

This chapter provides a general description of the 21145 Phoneline/Ethernet LAN Controller, its features, and an overview of the hardware.

1.1 Purpose and Audience

This manual describes the operation of the 21145 Phoneline/Ethernet LAN Controller (also referred to as the 21145). This manual is for hardware and software designers who use the 21145.

There are two versions of the 21145: a 176-pin device and a 144-pin device (see the *21145 Phoneline/Ethernet LAN Controller Datasheet* for more details). Except for the modem and expansion ROM interfaces (see Section 1.6), the devices are identical. This document describes both, except when specifically noted otherwise.

1.2 Manual Organization

This manual contains the following chapters and appendices (an index is also included):

- This chapter, "Introduction", includes a general description of the 21145. It also provides an overview of the 21145 hardware components.
- Chapter 2, "Host Communication", describes how the 21145 communicates with the host by using descriptor lists and data buffers. It also describes the transmit and receive processes.
- Chapter 3, "Host Bus Operation", provides a description of the read, write, and termination cycles.
- Chapter 4, "Network Interface Operation", describes the MII and 10BASE-T ports. It includes a complete description of media access control (MAC) operations. It also provides detailed transmit and receive operation information.
- Chapter 5, "Modem Interface", describes the modem connections and the 21145 PCI/CardBus interface.
- Chapter 6, "Power-Management and Power-Saving Support", describes power-management features and associated specifications.
- Chapter 7, "External Ports", describes the interface and operation of the MicroWire* serial ROM, the boot ROM, the general-purpose port, and the network activity LEDs.
- Chapter 8, "Registers", provides a complete bit description of the 21145 command and status registers (CSRs) and the configuration registers.
- Appendix A, "DNA CSMA/CD Counters and Events Support", describes features that support the driver in implementing and reporting the specified counters and events.
- Appendix B, "Hash C Routine", provides an example of a C routine that generates a hash index for a given Ethernet address.
- Appendix C, "Port Selection Procedure", provides information about selecting the MII, 10BASE-T, and HomePNA* ports.

- Appendix D, “General-Purpose Port and LED Programming”, contains information about general-purpose port and LED programming.
- Appendix E, “Filtering Setup Frame Buffer Examples”, provides examples of perfect and imperfect filtering setup frame buffers.
- Appendix F, “Wake-Up Frame Filter Register Block Programming Examples”, provides examples of wake-up frame patterns and how the wake-up frame filter register block should be programmed.
- Appendix G, “The HomePNA PHY Register Interface”, describes how to access the HomePNA PHYs internal registers.
- Appendix H, “HomePNA Telephone Line Interface”, describes the 21145’s interface to the physical telephone line.
- Appendix I, “Magic Packet Format”, describes the Magic Packet* format used by the 21145.

1.3 Document Conventions

Some tables use the values 1, 0, and X. An X signifies a don’t care (1 or 0) convention, which can be determined by the system designer. Hexadecimal numbers have an ‘H’ suffix, and binary numbers a ‘b’ suffix; all other numbers are decimal, unless clearly identified by the context.

All shaded bits in the figures are reserved. All reserved fields within non-reserved locations must be written by software as 0, and must be masked off when read; reserved register and memory locations must not be written to. Otherwise, unpredictable results will occur.

1.4 General Description

The 21145 is an Ethernet/HomePNA LAN controller for both 100 Mb/s and 10 Mb/s data rates that integrates a HomePNA PHY for 1 Mb/s data rate home networking on telephone lines. The 21145 provides a direct interface to the Peripheral Component Interconnect (PCI) local bus or to a CardBus. The 21145 interfaces to the host processor by using on-chip command and status registers (CSRs) and a shared host memory area, set up mainly during initialization. This minimizes processor involvement in the 21145 operation during normal reception and transmission.

The 21145 also incorporates a modem interface (176-pin device only), and can operate with a wide range of ISA-bus modem chipsets available in the marketplace.

The 21145 is optimized for low power PCI/CardBus based systems and supports a power-management mechanism, based upon the OnNow architecture which is required for PC 97, PC 98 and PC 99.

Large FIFOs allow the 21145 to efficiently operate in systems with longer latency periods. Bus traffic is also minimized by filtering out received runt frames and by automatically retransmitting collided frames without a repeated fetch from the host memory. The 21145 also provides an expansion ROM interface (176-pin device only) for uses such as boot ROMs.

The 21145 provides the following network interfaces:

- 10BASE-T 10 Mb/s port
- HomePNA port
- A media-independent/symbol interface (MII/SYM) 10/100 Mb/s port

The 10BASE-T port provides a direct Ethernet connection to the twisted-pair (TP) interface. The HomePNA port provides a direct interface to a residential telephone line at a rate of 1 Mb/s.

The MII/SYM port supports two operational modes:

- MII mode—A full implementation of the MII standard
- SYM mode—Symbol interface to an external 100 Mb/s front-end decoder (ENDEC). In this mode the 21145 uses an on-chip physical coding sublayer (PCS) and a scrambler/descrambler circuit to enable a low-cost 100BASE-T implementation.

The 21145 is capable of functioning in a full-duplex environment for the MII/SYM and 10BASE-T ports.

1.5 Features

The 21145 has the following features:

Host Interface Features:

- Includes a powerful onchip direct memory access (DMA) with programmable burst size, providing low CPU utilization.
- Supports early interrupt on transmit and receive.
- Supports interrupt mitigation on transmit and receive.
- Supports big or little endian byte ordering for buffers and descriptors.
- Implements intelligent arbitration between DMA channels to minimize underflow and overflow.
- Contains large independent receive and transmit FIFOs.

Network Side Features:

- Supports three network ports: 10BASE-T (10 Mb/s), HomePNA (1 Mb/s), and MII/SYM (10/100 Mb/s).
- Contains a variety of flexible address filtering modes.
- Contains on-chip PCS and scrambler/descrambler for 100BASE-TX.
- Implements signal-detect filtering to avoid false detection of link with 100BASE-TX symbol interfaces.
- Enables automatic detection and correction of 10BASE-T receive polarity.
- Contains on-chip integrated 10BASE-T transceiver.
- Supports autodetection between 10BASE-T, HomePNA, and MII/SYM ports.
- Supports IEEE 802.3 Auto-Negotiation algorithm of full-duplex and half-duplex operation for 10 Mb/s and 100 Mb/s (NWAY).

- Offers a patented solution to the Ethernet capture-effect problem.
- Supports full-duplex operation on both MII/SYM and 10BASE-T ports.
- Provides internal or external loopback capability on all network ports.
- Supports IEEE 802.3 and ANSI 8802-3 Ethernet standards.

HomePNA Features:

- Compliant with the *Home Phoneline Networking Alliance* (HomePNA) specification effort.
- Integrates a HomePNA PHY for 1 Mb/s Ethernet-like home networking on residential telephone lines.
- Provides automatic support for dual HomePNA data transfer rates and dual transmission power levels.
- Generates an interrupt upon HomePNA PHY interrupt.
- Provides a software interface to the HomePNA PHY internal registers.
- Supports ACPI and OnNow on the HomePNA port (except for the link-change event).

Modem Interface (176-pin 21145 only):

- Supports a glueless modem interface port for standard ISA modem chipsets.
- Modem is accessed as a second PCI function with its own PCI configuration space.
- Internal modem registers mapped to PCI Memory or I/O space.
- Supports ACPI power management for modem, including wakeup.

PCI and CardBus Features:

- Supports *PCI Local Bus Specification*, Revision 2.1.
- Supports PCI and CardBus interfaces for network and modem access.
- Supports PCI/CardBus clock control through clkrun.
- Supports CardBus cstschg pin and Status Changed registers.
- Supports automatic loading of subvendor ID and CardBus card information structure (CIS) pointer from serial ROM to configuration registers.
- Supports storage of CardBus card information structure (CIS) in the serial ROM or the expansion ROM.
- Supports the advanced PCI/CardBus read multiple, read line, and write and invalidate commands.
- Supports an unlimited PCI/CardBus burst.
- Supports PCI/CardBus clock speed frequency from DC to 33 MHz; network operation with PCI clock from 20 MHz to 33 MHz.

Power Management and Power Savings:

- Fully compliant with the *Network Device Class Power Management Specification*, Revision 1.0, and the *Communication Device Class Power management Specification*, under the OnNow Architecture for Microsoft's *PC 97 Hardware Design Guide*, *PC 98 Hardware Design Guide and PC 99 Hardware Design Guide.*

- Supports all wake-up events defined in the *Network Device Class Power Management Specification*, Revision 1.0 and the *Communication Device Class Power management Specification* including:
  - — Pattern matching
  - — Link change (except on HomePNA port)
  - — Magic Packet
  - — Phone ring indication on modem port (176-pin device only)
- Fully compliant with the *Advanced Configuration and Power Interface* (ACPI) *Specification*, Revision 1.0.
- Fully compliant with the *PCI Bus Power Management Interface Specification*, Revision 1.0.
- Implements device power management with two power saving modes (Snooze and Sleep). Meets the CardBus power-up current restriction of 70 mA by powering up in Sleep mode.
- Implements low-power, 3.3 V CMOS technology.

Other Features:

- Provides MicroWire interface for serial ROM (1 K and 4 K EEPROM).
- Provides an expansion ROM interface up to 256 KB (176-pin device only).
- Provides LED indications for various network activity.
- Contains a 4-bit, general-purpose programmable register and corresponding I/O pins with the ability to generate interrupts from two general-purpose pins.

1.6 Microarchitecture

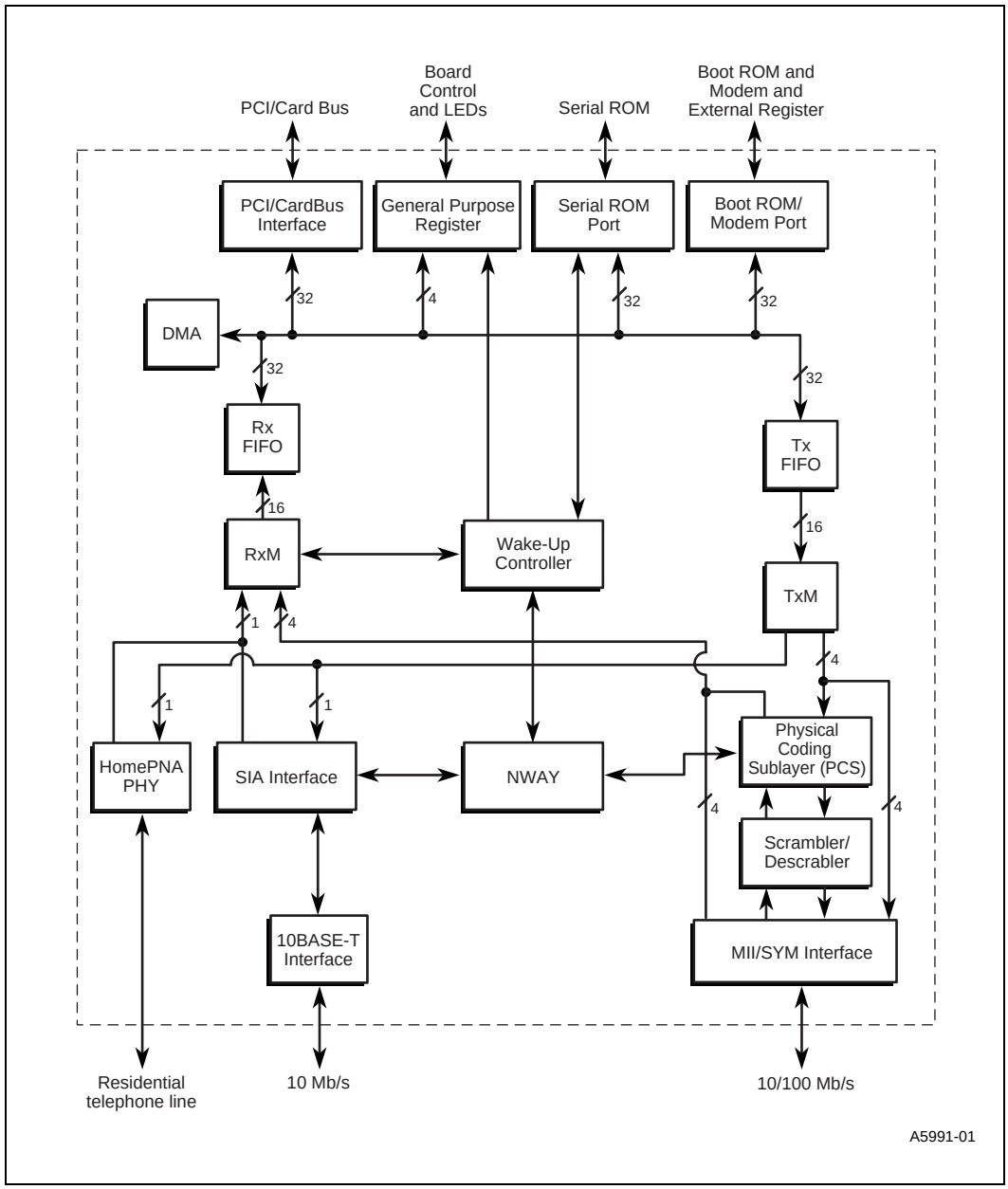
The following list describes the 21145 hardware components, and Figure 1-1 shows a block diagram of the 21145:

- PCI/CardBus interface—Includes all interface functions to the PCI and CardBus bus. Handles all interconnect control signals, and executes DMA and I/O transactions.
- Expansion ROM (176-pin device only)—Provides an interface to perform read and write operations to the expansion ROM. Supports accesses to bytes or longwords (32-bit). Provides the ability to connect an external 8-bit register to the expansion ROM port.
- Modem port (176-pin device only)—Provides an interface to perform byte read and write operations to ISA compliant modem chipsets.
- Serial ROM port—Provides a direct interface to a MicroWire ROM for storage of the Ethernet address and system parameters.
- General-purpose register—Enables software use for input or output functions and LEDs.
- DMA—Contains independent receive and transmit controllers. Handles data transfers between CPU memory and on-chip memory.
- FIFOs—Contains independent FIFOs for receive and transmit. Supports automatic packet deletion on receive (runt packets or after a collision) and packet retransmission after a collision on transmit.

- RxM—Handles all CSMA/CD[1] MAC[2] receive operations, and transfers the network data from the PHY to the receive FIFO.
- TxM—Handles all CSMA/CD MAC transmit operations, and transfers data from transmit FIFO to the 10Base-T, HomePNA, or MII/SYM ports for transmission.
- SIA interface—Performs 10 Mb/s physical layer network operations; implements the HomePNA and 10BASE-T functions, including the Manchester encoder and decoder functions.
- NWAY—Implements the IEEE 802.3 Auto-Negotiation algorithm.
- Physical coding sublayer—Implements the encoding and decoding sublayer of the 100BASE-TX (CAT5) specification, including the squelch feature.
- HomePNA PHY—Implements the HomePNA telephone network interface.
- Scrambler/descrambler—Implements the twisted-pair physical layer medium dependent (TP-PMD) scrambler/descrambler scheme for 100BASE-TX.
- Three network interfaces—A HomePNA interface, a 10BASE-T interface, and an MII/SYM interface provide a full MII signal interface and direct interface to the 100 Mb/s PHY for CAT5.
- Wake-up-controller—Enables power-management control compliant with the ACPI.

1. Carrier-sense multiple access with collision detection.
2. Media access control.

Figure 1-1. 21145 Block Diagram



Host Communication 2

This chapter describes descriptor lists and data buffers, which are collectively called the host communication area, that manage the actions and status related to buffer management. Commands and signals that control the functional operation, receive and transmit processes, interrupt handling, and the initialization sequence of the 21145 are also described.

Note: All shaded bits in the figures in this chapter are reserved and should be written by the driver as zero.

2.1 Data Communication

The 21145 and the driver communicate through the two following data structures:

- Control and status registers (CSRs), described in Chapter 8.
- Descriptor lists and data buffers, described in this chapter.

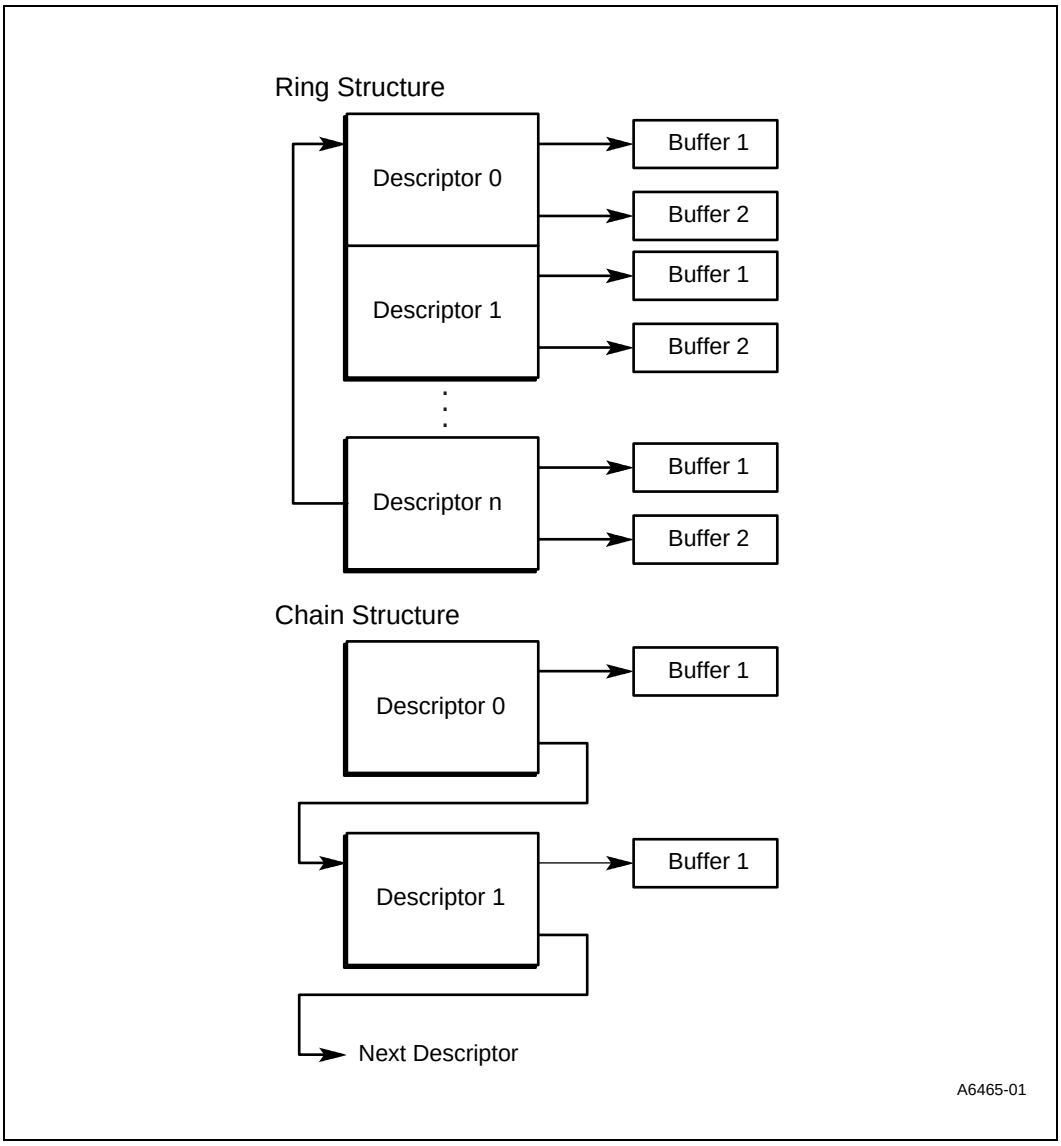
2.2 Descriptor Lists and Data Buffers

The 21145 transfers received data frames to the receive buffers in host memory and transmits data from the transmit buffers in host memory. Descriptors that reside in the host memory act as pointers to these buffers.

There are two descriptor lists, one for receive and one for transmit. The base address of each list is written into CSR3 and CSR4, respectively. A descriptor list is forward linked (either implicitly or explicitly). The last descriptor may point back to the first entry to create a ring structure. Explicit chaining of descriptors is accomplished by setting the second address chained in both the receive and transmit descriptors RDES1<24> and TDES1<24>. The descriptor lists reside in the host *physical* memory address space. Each descriptor can point to a maximum of two buffers. This enables two buffers to be used, physically addressed, and not contiguous in memory (Figure 2-1).

A data buffer consists of either an entire frame or part of a frame, but it cannot exceed a single frame. Buffers contain only data; buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. Data chaining can be enabled or disabled. Data buffers reside in host *physical* memory space.

Figure 2-1. Descriptor Ring and Chain Structure Examples



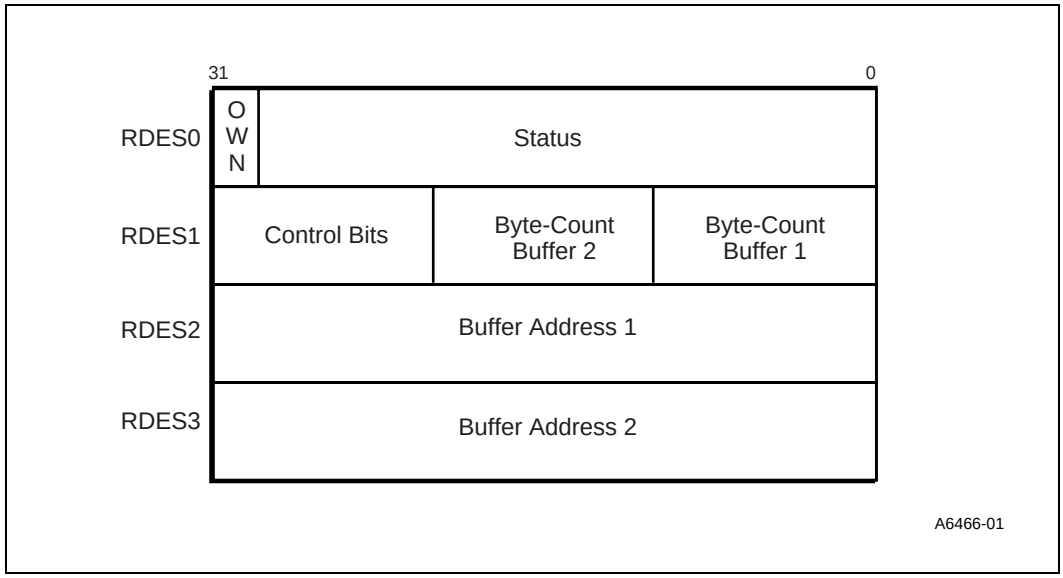
2.2.1 Receive Descriptors

Figure 2-2 shows the receive descriptor format.

Note: Descriptors and receive buffers addresses must be longword aligned.

Providing two buffers, two byte-count buffers, and two address pointers in each descriptor enables the adapter port to be compatible with various types of memory-management schemes.

Figure 2-2. Receive Descriptor Format



2.2.1.1 Receive Descriptor 0 (RDES0)

RDES0 contains the received frame status, the frame length, and the descriptor ownership information. Figure 2-3 shows the RDES0 bit fields.

Figure 2-3. RDES0 Bit Fields

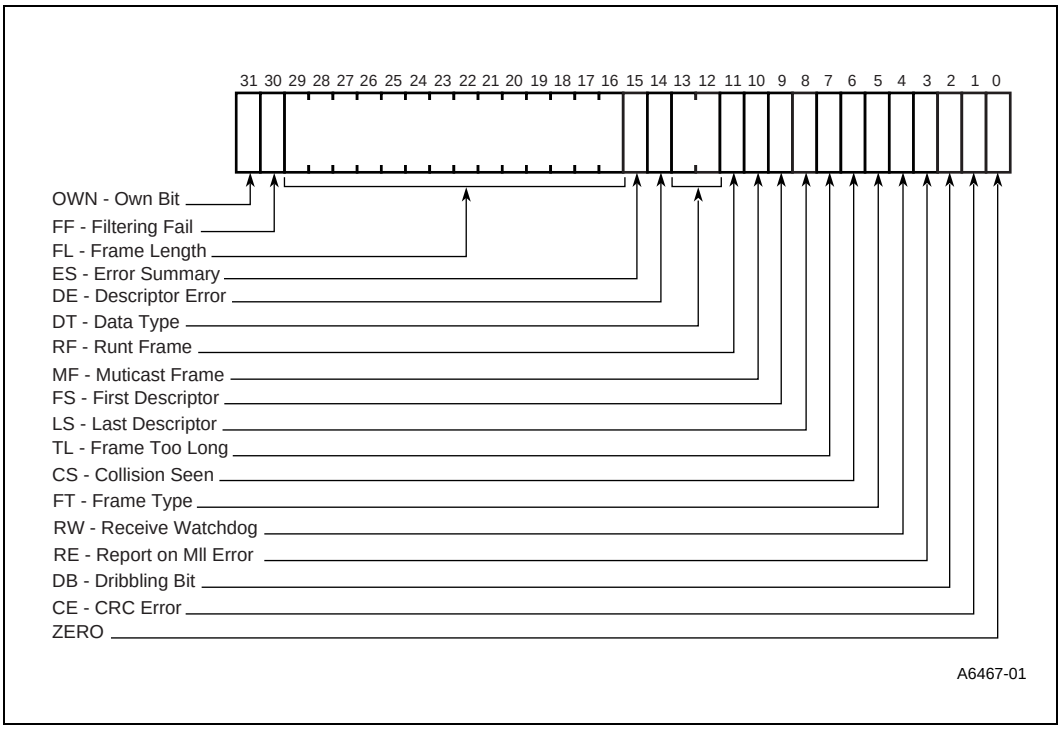


Table 2-1 describes the RDES0 bit fields.

Table 2-1. RDES0 Bit Fields Description (Sheet 1 of 3)

Field	Description
31	OWN—Own Bit When set, indicates that the descriptor is owned by the 21145. When reset, indicates that the descriptor is owned by the host. The 21145 clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
30	FF—Filtering Fail When set, indicates that the frame failed the address recognition filtering. This bit can be set only when receive all (CSR6<30>) is set. Otherwise, this bit is reset. This bit is valid only when last descriptor (RDES0<8>) is set and when the received frame is 64 bytes or longer.
29:16	FL—Frame Length Indicates the length, in bytes, of the received frame that was transferred into host memory, including the cyclic redundancy check (CRC). Normally, this is also the length in bytes of the frame received from the network. In the case of receive timeout, the length of the frame on the network is longer. This field is valid only when last descriptor (RDES0<8>) is set and descriptor error (RDES0<14>) is reset.

Table 2-1. RDES0 Bit Fields Description (Sheet 2 of 3)

Field	Description
15	ES—Error Summary Indicates the logical OR of the following RDES0 bits: RDES0<1>—CRC error RDES0<6>—Collision seen RDES0<7>—Frame too long RDES0<11>—Runt frame RDES0<14>—Descriptor error This bit is valid only when last descriptor (RDES0<8>) is set.
14	DE—Descriptor Error When set, indicates a frame truncation caused by a frame that does not fit within the current descriptor buffers, and that the 21145 does not own the next descriptor. The frame is truncated. This bit is valid only when last descriptor (RDES0<8>) is set.
13:12	DT—Data Type Indicates the type of frame the buffer contains: 00—Serial received frame. 01—Internal loopback frame. 10—External loopback frame or serial received frame. The 21145 does not differentiate between loopback and serial received frames; therefore, this information is global and reflects only the operating mode (CSR6<11:10>). 11—Reserved. This field is valid only when last descriptor (RDES0<8>) is set.
11	RF—Runt Frame When set, indicates that this frame was damaged by a collision or premature termination before the collision window had passed. Runt frames are passed on to the host only if the pass bad frames bit (CSR6<3>) is set. This bit is valid only when last descriptor (RDES0<8>) is set.
10	MF—Multicast Frame When set, indicates that this frame has a multicast address. This bit is valid only when last descriptor (RDES0<8>) is set.
9	FS—First Descriptor When set, indicates that this descriptor contains the first buffer of a frame. If the buffer size of the first buffer is 0, the second buffer contains the beginning of the frame. If the buffer size of the second buffer is also 0, the second descriptor contains the beginning of the frame.
8	LS—Last Descriptor When set, indicates that the buffers pointed to by this descriptor are the last buffers of the frame.
7	TL—Frame Too Long When set, indicates that the frame length exceeds the maximum Ethernet-specified size of 1518 bytes. This bit is valid only when last descriptor (RDES0<8>) is set. **Note:** Frame too long is only a frame length indication and does not cause any frame truncation.
6	CS—Collision Seen When set, indicates that the frame was damaged by a collision that occurred after the 64 bytes following the start frame delimiter (SFD). This is a late collision. This bit is valid only when last descriptor (RDES0<8>) is set.

Table 2-1. RDES0 Bit Fields Description (Sheet 3 of 3)

Field	Description
5	FT—Frame Type When set, indicates that the frame is an Ethernet-type frame (frame length field is greater than 1500 bytes). When clear, indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames of less than 14 bytes. This bit is valid only when last descriptor (RDES0<8>) is set.
4	RW—Receive Watchdog When set, indicates that the receive watchdog timer expired while receiving this frame. If the device is in the Snooze power saving mode, the frame was longer than 1792 to 2304 bytes; otherwise, the frame was longer than 2048 to 2560 bytes. Receive watchdog timeout (CSR5<9>) is also set. When RDES0<4> is set, the frame length field in RDES0<29:16> is not valid. This bit is valid only when last descriptor (RDES0<8>) is set, and should be ignored in HomePNA mode.
3	RE—Report on MII Error When set, indicates that a receive error in the physical layer was reported during the frame reception. This bit is valid only if the packet was received on the MII/SYM port and when last descriptor (RDES0<8>) is set.
2	DB—Dribbling Bit When set, indicates that the frame contained a noninteger multiple of 8 bits. This error is reported only if the number of dribbling bits in the last byte is 4 in MII operating mode, or at least 3 in 10 Mb/s serial operating mode. This bit is not valid if collision seen (RDES0<6>) is set. If set, and the CRC error (RDES0<1>) is reset, then the packet is valid. This bit is valid only when last descriptor (RDES0<8>) is set. This bit is not valid in HomePNA mode.
1	CE—CRC Error When set, indicates that a cyclic redundancy check (CRC) error occurred on the received frame. This bit is also set when the mii_err pin is asserted during the reception of a receive packet even though the CRC may be correct. This bit is not valid if one of the following conditions exist: –The received frame is a runt frame –A collision occurred while the packet was being received –A watchdog timeout occurred while the packet was being received This bit is valid only when last descriptor (RDES0<8>) is set.
0	ZERO This bit is always zero for a packet with legal length.

2.2.1.2 Receive Descriptor 1 (RDES1)

Figure 2-4 shows the RDES1 bit fields.

Figure 2-4. RDES1 Bit Fields

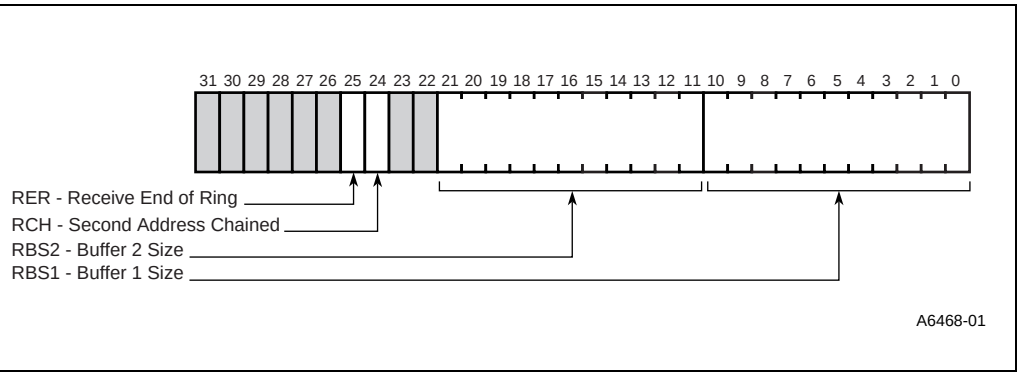


Table 2-2 describes the RDES1 bit fields.

Table 2-2. RDES1 Bit Fields Description

Field	Description
25	RER—Receive End of Ring When set, indicates that the descriptor list reached its final descriptor. The 21145 returns to the base address of the list (Section 8.3.2.7), creating a descriptor ring.
24	RCH—Second Address Chained When set, indicates that the second address in the descriptor is the next descriptor address, rather than the second buffer address. RDES1<25> takes precedence over RDES1<24>.
21:11	RBS2—Buffer 2 Size Indicates the size, in bytes, of the second data buffer. If this field is 0, the 21145 ignores this buffer and fetches the next descriptor. The buffer size must be a multiple of 4. This field is not valid if RDES1<24> is set.
10:0	RBS1—Buffer 1 Size Indicates the size, in bytes, of the first data buffer. If this field is 0, the 21145 ignores this buffer and uses buffer 2. The buffer size must be a multiple of 4.

2.2.1.3 Receive Descriptor 2 (RDES2)

Figure 2-5 shows the RDES2 bit field.

Figure 2-5. RDES2 Bit Field

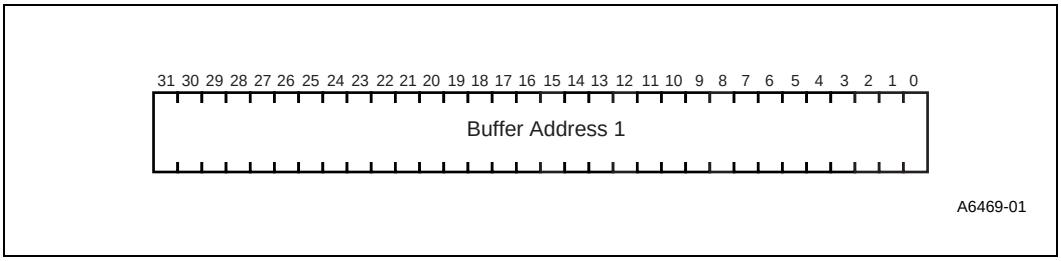


Table 2-3 describes the RDES2 bit field.

Table 2-3. RDES2 Bit Field Description

Field	Description
31:0	Buffer Address 1 Indicates the physical address of buffer 1. The buffer must be longword aligned (RDES2<1:0> = 00).

2.2.1.4 Receive Descriptor 3 (RDES3)

Figure 2-6 shows the RDES3 bit field.

Figure 2-6. RDES3 Bit Field

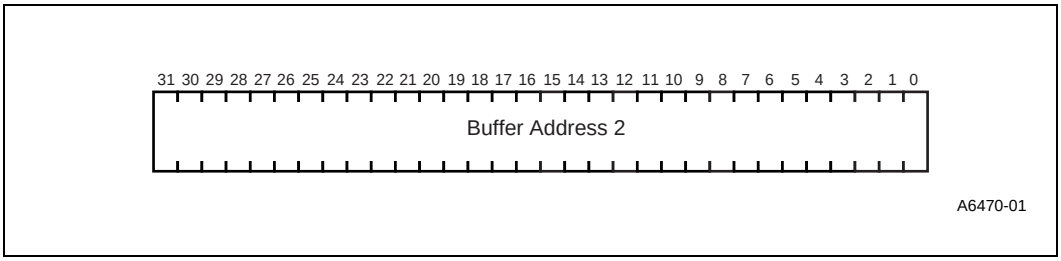


Table 2-4 describes the RDES3 bit field.

Table 2-4. RDES3 Bit Field Description

Field	Description
31:0	Buffer Address 2 If the RCH field (RDES1<24>) is set, this field is physical address of buffer 2; The buffer must be longword aligned (RDES3<1:0> = 00).Otherwise, this field points to the next descriptor.

2.2.1.5 Receive Descriptor Status Validity

Table 2-5 lists the validity of the receive descriptor status bits in relation to the reception completion status.

Table 2-5. Receive Descriptor Status Validity

Reception	Receive Status Report							
Status	**RF**	**CS**	**FT**	**FF**	**DB**	**CE**	**RE**	**(ES, DE, DT, FS, LS, FL)**
Collision after 512 bits	0	1	V	V	NV	NV	V	V
Runt frame	1	0	V	NV	V	NV	V	V
Runt frame less than 14 bytes	1	0	NV	NV	V	NV	V	V
Watchdog timeout	0	V	V	V	V	NV	V	V

List of table abbreviations

RF—Runt frame (RDES0<11>)
CS—Collision seen (RDES0<6>)
FT—Frame type (RDES0<5>)
FF—Filtering fail (RDES0<30>)
DB—Dribbling bit (RDES0<2>)
CE—CRC error (RDES0<1>)
RE—Report on MII error (RDES0<3>)
ES—Error summary (RDES0<15>)

DE—Descriptor error (RDES0<14>)
DT—Data type (RDES0<13:12>)
FS—First descriptor (RDES0<9>)
LS—Last descriptor (RDES0<8>)
FL—Frame length (RDES0<30:16>)
V—Valid
NV—Not valid

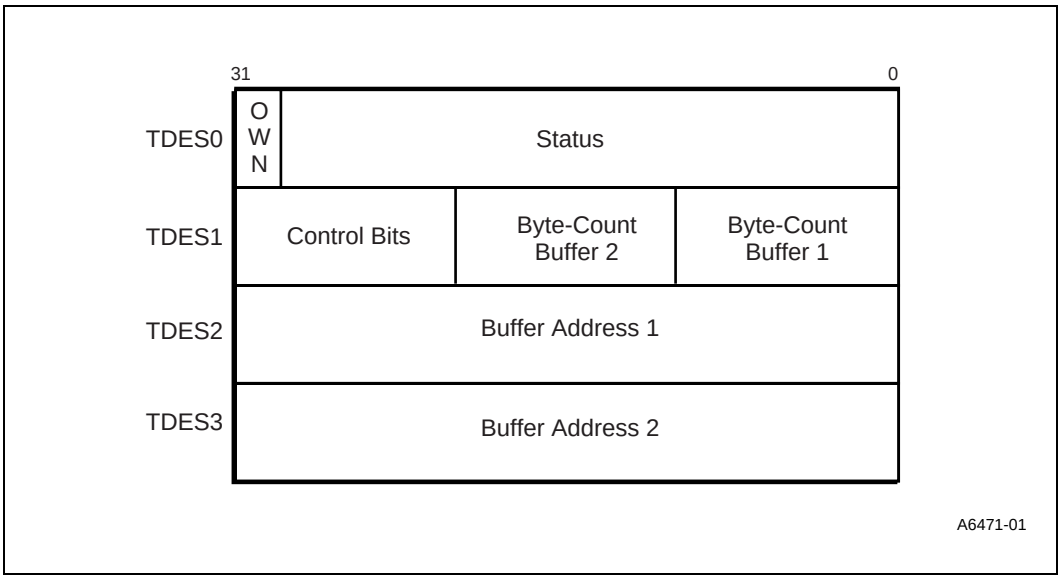
2.2.2 Transmit Descriptors

Figure 2-7 shows the transmit descriptor format.

Note: Descriptor addresses must be longword aligned.

Providing two buffers, two byte-count buffers, and two address pointers in each descriptor enables the adapter port to be compatible with various types of memory-management schemes.

Figure 2-7. Transmit Descriptor Format



2.2.2.1 Transmit Descriptor 0 (TDES0)

TDES0 contains transmitted frame status and descriptor ownership information. Figure 2-8 shows the TDES0 bit fields.

Figure 2-8. TDES0 Bit Fields

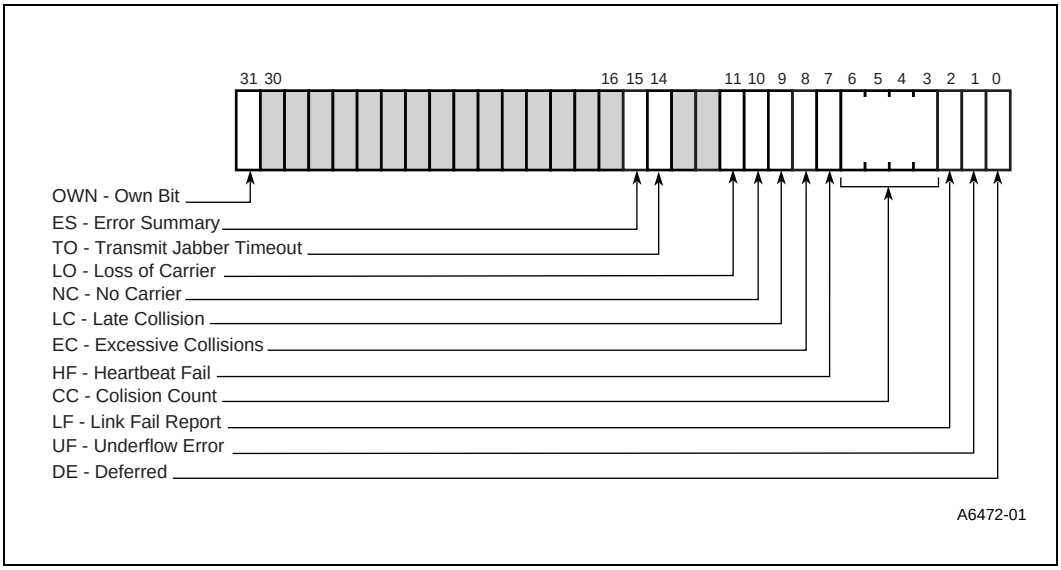


Table 2-6 describes the TDES0 bit fields.

Table 2-6. TDES0 Bit Fields Description (Sheet 1 of 2)

Field	Description
31	OWN—Own Bit When set, indicates that the descriptor is owned by the 21145. When cleared, indicates that the descriptor is owned by the host. The 21145 clears this bit either when it completes the frame transmission or when the buffers allocated in the descriptor are empty. The ownership bit of the first descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between the 21145 fetching a descriptor and the driver setting an ownership bit.
15	ES—Error Summary Indicates the logical OR of the following bits: TDES0<1>—Underflow error TDES0<2>—Link Fail Report TDES0<8>—Excessive collisions TDES0<9>—Late collision TDES0<10>—No carrier TDES0<11>—Loss of carrier TDES0<14>—Transmit jabber timeout summary The error summary bit may be set despite the fact that none of the above bits are set. When this happens, no error has occurred and the ES indication should be ignored.
14	TO—Transmit Jabber Timeout When set, indicates that the transmit jabber timer timed out and that the 21145 transmitter was still active. The transmit jabber timeout interrupt CSR5<3> is set. The transmission process is *aborted* and placed in the STOPPED state. When TDES0<14> is set, any Heartbeat Fail (TDES0<7>) or Late Collision (TDES0<9>) indication is not valid.
11	LO—Loss of Carrier When set, indicates loss of carrier during transmission. Not valid in internal loopback mode (CSR6<11:10>=01).
10	NC—No Carrier When set, indicates that the carrier signal from the transceiver was not present during transmission. Not valid in internal loopback mode (CSR6<11:10>=01).
9	LC—Late Collision When set, indicates that the frame transmission was aborted due to collision occurring after the collision window of 64 bytes. Not valid if Underflow Error (TDES0<1>) or Transmit Jabber Timeout (TDES0<14>) are set.
8	EC—Excessive Collisions When set, indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current frame.
7	HF—Heartbeat Fail This bit is effective only in 10BASE-T operating mode. When set, this bit indicates a heartbeat collision check failure (the transceiver failed to return a collision pulse as a check after the transmission). For transceivers that do not support heartbeat collision check, heartbeat fail is set but is not valid. This bit is not valid if Underflow Error (TDES0<1>) is set. On the second transmission attempt, after the first transmission was aborted due to a collision, the 21145 does not check Heartbeat Fail (TDES0<7>) and is reset.

Table 2-6. TDES0 Bit Fields Description (Sheet 2 of 2)

Field	Description
6:3	CC—Collision Count This 4-bit counter indicates the number of collisions that occurred before the frame was transmitted. Not valid when the Excessive Collisions bit (TDES0<8>) is also set.
2	LF—Link Fail Report When set, indicates the link was down when packet transmission completed, so the packet was not received by the link partner. If the link was down at some stage during packet transmission, but returned by the time packet transmission was done, this bit will not be set, although the packet may not have been received. This bit is only valid in 10BASE-T mode (CSR6<18> = 0, CSR13<3> = 0) and 100 Mb/s SYM mode (CSR6<18> = 1, CSR6<23> = 1).
1	UF—Underflow Error When set, indicates that the transmitter aborted the message because data arrived late from memory. Underflow Error indicates that the 21145 encountered an empty transmit FIFO while transmitting a frame. The transmission process enters the suspended state and sets both Transmit Underflow (CSR5<5>) and Transmit Interrupt (CSR5<0>).
0	DE—Deferred When set, indicates that the 21145 had to defer while ready to transmit a frame because the carrier was asserted.

2.2.2.2 Transmit Descriptor 1 (TDES1)

Figure 2-9 shows the TDES1 bit fields.

Figure 2-9. TDES1 Bit Fields

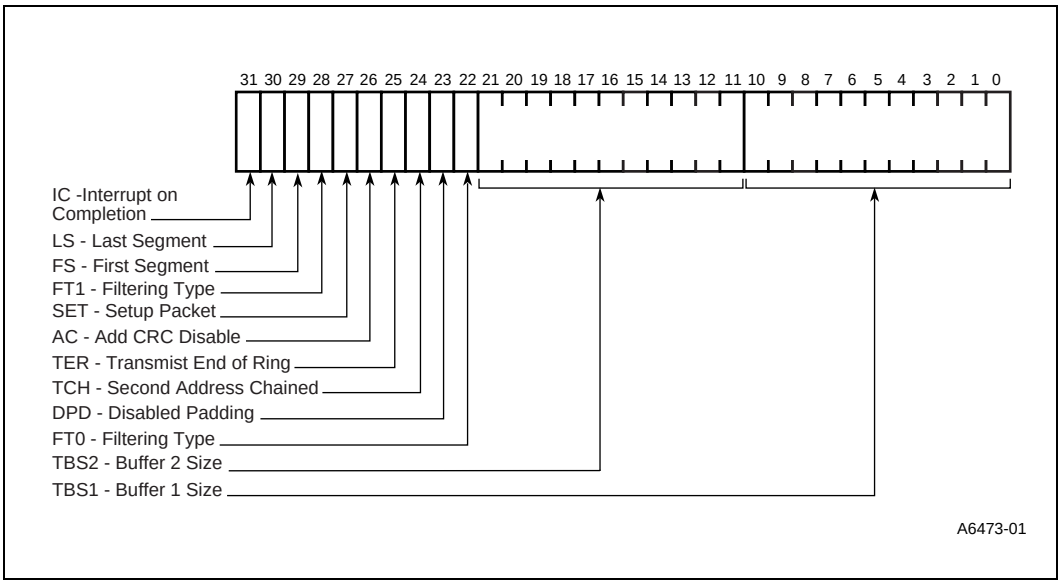


Table 2-7 describes the TDES1 bit fields.

Table 2-7. TDES1 Bit Fields Description

Field	Description
31	IC—Interrupt on Completion When set, the 21145 sets transmit interrupt (CSR5<0>) after the present frame has been transmitted. It is valid only when last segment (TDES1<30>) is set or when it is a setup packet.
30	LS—Last Segment When set, indicates that the buffer contains the last segment of a frame. If a frame is both the first and last segment, then both LS and FS should be set.
29	FS—First Segment When set, indicates that the buffer contains the first segment of a frame. If a frame is both the first and last segment, then both LS and FS should be set.
28	FT1—Filtering Type This bit is valid only when setup packet (TDES1<27>) is set. Table 2-8 lists the filtering types.
27	SET—Setup Packet When set, indicates that the current descriptor is a setup frame descriptor (Section 2.2.3).
26	AC—Add CRC Disable When set, the 21145 does not append the cyclic redundancy check (CRC) to the end of the transmitted frame. This field is valid only when first segment (TDES1<29>) is set.
25	TER—Transmit End of Ring When set, indicates that the descriptor pointer has reached its final descriptor. The 21145 returns to the root address of the list. This creates a descriptor ring.
24	TCH—Second Address Chained When set, indicates that the second address in the descriptor is the next descriptor address, rather than the second buffer address. Transmit end of ring (TDES1<25>) takes precedence over second address chained (TDES1<24>).
23	DPD—Disabled Padding When set, the 21145 does not automatically add a padding field, to a packet shorter than 64 bytes. When reset, the 21145 automatically adds a padding field and also a CRC field to a packet shorter than 64 bytes. The CRC field is added despite the state of the add CRC disable (TDES1<26>) flag.
22	FT0—Filtering Type This bit is valid only when setup packet (TDES1<27>) is set. Table 2-8 lists the filtering types.
21:11	TBS2—Buffer 2 Size Indicates the size, in bytes, of the second data buffer. If this field is 0, the 21145 ignores this buffer and fetches the next descriptor. This field is not valid if second address chained (TDES1<24>) is set.
10:0	TBS1—Buffer 1 Size Indicates the size, in bytes, of the first data buffer. If this field is 0, the 21145 ignores this buffer and uses buffer 2.

Table 2-8 lists the filtering types.

Table 2-8. Filtering Type

FT1	FT0	Description
0	0	Perfect Filtering The 21145 interprets the descriptor buffer as a setup perfect table of 16 addresses, and sets the 21145 filtering mode to perfect filtering.
0	1	Hash Filtering The 21145 interprets the descriptor buffer as a setup hash table of 512-bit-plus-one perfect address. If an incoming receive packet destination address is a multicast address, the 21145 executes an imperfect address filtering compared with the hash table. However, if the incoming receive packet destination address is a physical address, the 21145 executes a perfect filtering compared with the perfect address.
1	0	Inverse Filtering The 21145 interprets the descriptor buffer as a setup perfect table of 16 addresses and sets the 21145 filtering mode to inverse filtering. The 21145 receives the incoming frames with destination addresses not matching the perfect addresses and rejects the frames with destination addresses matching one of the perfect addresses.
1	1	Hash-Only Filtering The 21145 interprets the descriptor buffer as a setup 512-bit hash table. If an incoming receive packet destination address is multicast or physical, the 21145 executes an imperfect address filtering against the hash table.

2.2.2.3 Transmit Descriptor 2 (TDES2)

Figure 2-10 shows the TDES2 bit field.

Figure 2-10. TDES2 Bit Field

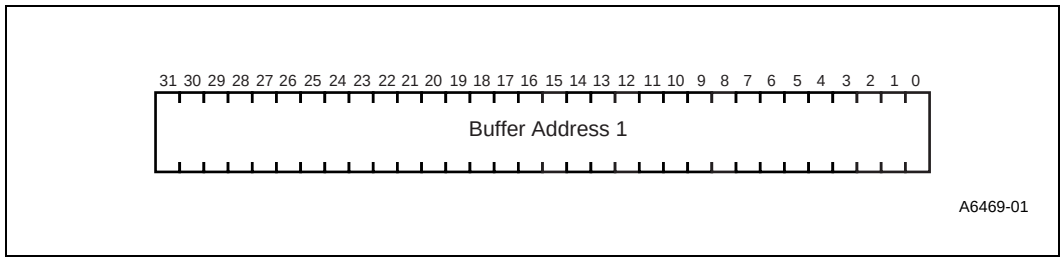


Table 2-9 describes the TDES2 bit field.

Table 2-9. TDES2 Bit Field Description

Field	Description
31:0	Buffer Address 1 Physical address of buffer 1. There are no limitations on the buffer address alignment.

2.2.2.4 Transmit Descriptor 3 (TDES3)

Figure 2-11 shows the TDES3 bit field.

Figure 2-11. TDES3 Bit Field

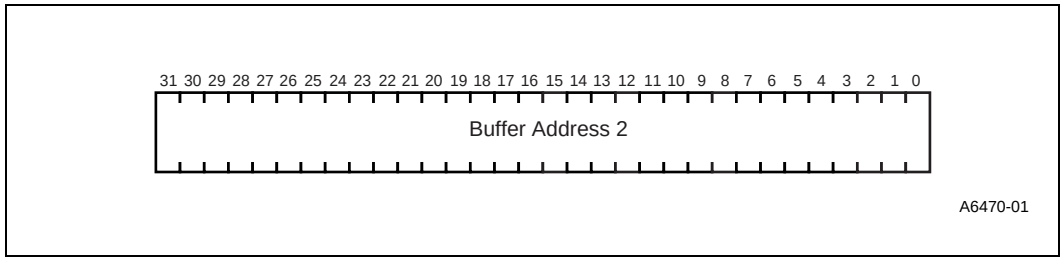


Table 2-10 describes the TDES3 bit field.

Table 2-10. TDES3 Bit Field Description

Field	Description
31:0	Buffer Address 2 If the TCH field (TDES1<24>) is set, this field is physical address of buffer 2; there are no limitations on the buffer address alignment. Otherwise, this field points to the next descriptor.

2.2.2.5 Transmit Descriptor Status Validity

Table 2-11 lists the validity of the transmit descriptor status bits during transmission completion status.

Table 2-11. Transmit Descriptor Status Validity

	Transmit Status Report								
Network error	**LO**	**NC**	**LC**	**EC**	**HF**	**CC**	**TO**	**UF**	**DE**
Underflow	V	V	NV	V	V	V	V	V	V
Excessive collisions	V	V	V	V	V	NV	V	V	V
Watchdog timeout	NV	V	NV	NV	NV	V	V	V	V
Internal loopback	NV	NV	V	V	NV	V	V	V	V
Transmit Jabber	V	V	NV	V	NV	V	V	V	V

List of table abbreviations

LO—Loss of carrier (TDES0<11>)
NC—No carrier (TDES0<10>)
LC—Late collision (TDES0<9>)
EC—Excessive collisions (TDES0<8>)
HF—Heartbeat fail (TDES0<7>)
CC—Collision count (TDES0<6:3>)
TO—Transmit jabber timeout (TDES0<14>)
UF—Underflow error (TDES0<1>)
DE—Deferred (TDES0<0>)
V—Valid
NV—Not valid

2.2.3 Setup Frame

A setup frame defines the 21145 Ethernet addresses that are used to filter all incoming frames. For a description of the various filtering groups, see Section 4.4.2. The setup frame is *never* transmitted on the wire nor is it looped back to the receive list. When processing the setup frame, the receiver logic temporarily disengages from the wire. The setup frame size must be *exactly* 192 bytes.

Note: The setup frame must be allocated in a single buffer that is longword aligned. First segment (TDES1<29>) and last segment (TDES1<30>) must both be 0.

When the setup frame load is completed, the 21145 closes the setup frame descriptor by clearing its ownership bit and by setting all other bits to 1.

2.2.3.1 First Setup Frame

A setup frame must be processed before the reception process is started, except when it operates in promiscuous filtering mode.

2.2.3.2 Subsequent Setup Frames

Subsequent setup frames may be queued to the 21145 despite the receive process state. To ensure correct setup frame processing, these packets must be queued at the beginning of the transmit descriptor's ring or following a descriptor with a zero-length buffer. A descriptor with a zero-length buffer should contain the following information:

TDES0<31> = 1 (Adapter-owned descriptor)
TDES1<30> = 0 (Last segment bit 0)
TDES1<29> = 0 (First segment bit 0)
TDES1<21:11> = 0 (Transmit buffer 2 empty)
TDES1<10:0> = 0 (Transmit buffer 1 empty)

Setup packet (TDES1<27>) may also be set. If so, the address filtering bits (TDES1<22> and TDES1<28>) should be the same as in the previous packet. For setup frame processing, the transmission process must be running. The setup frame is processed after all preceding frames have been transmitted and the current frame reception, if any, is completed.

The setup frame does not affect the reception process state, but during setup frame processing, the 21145 is disengaged from the Ethernet wire.

2.2.3.3 Perfect Filtering Setup Frame Buffer

This section describes how the 21145 interprets a setup frame buffer in perfect filtering mode (CSR6<0> = 0).

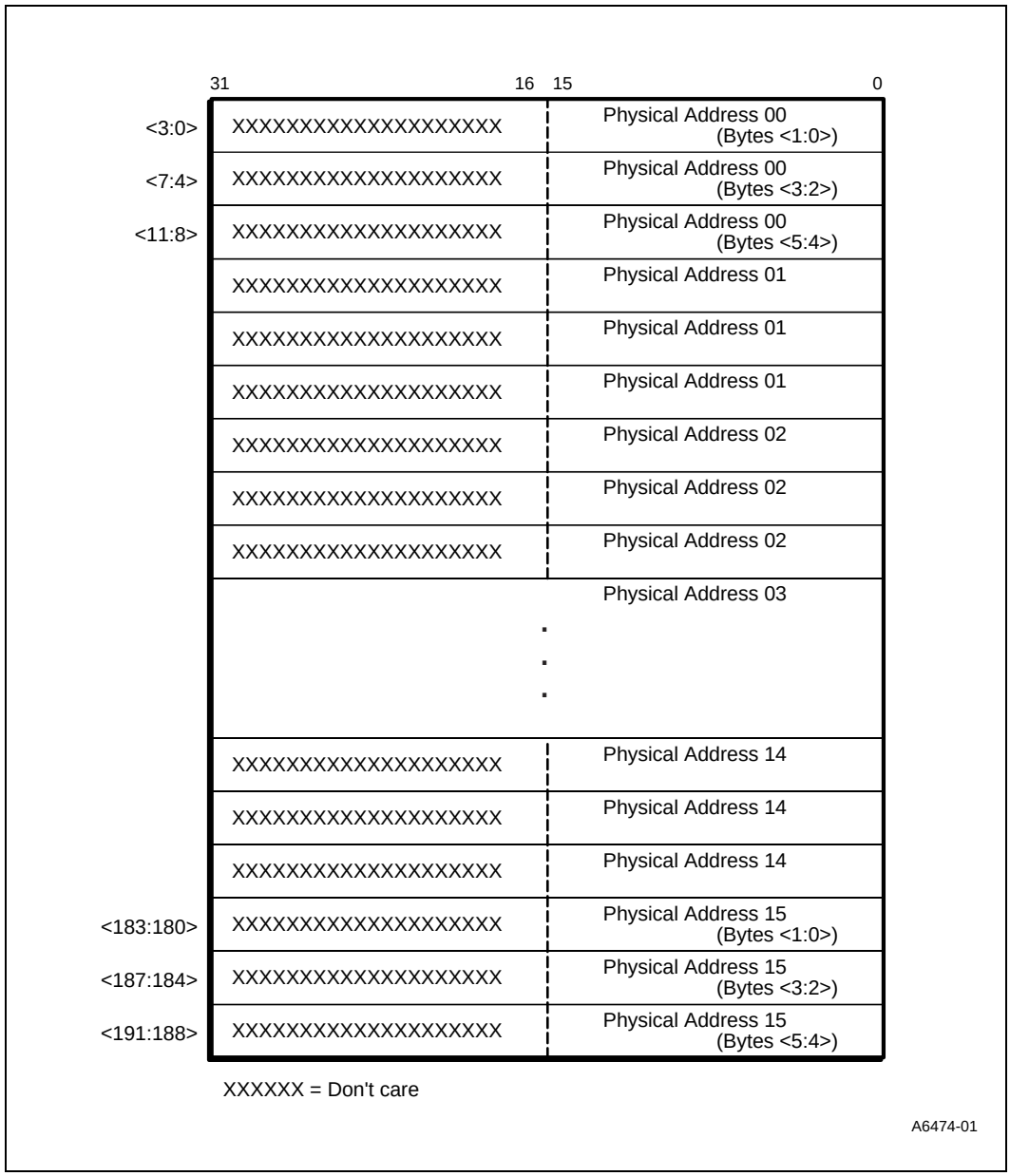
The 21145 can store 16 destination addresses (full 48-bit Ethernet addresses). The 21145 compares the addresses of any incoming frame to these addresses, and also tests the status of the inverse filtering (CSR6<4>). It rejects addresses that:

- Do not match if inverse filtering (CSR6<4>) is reset.
- Match if inverse filtering is set.

The setup frame must *always* supply all 16 addresses. Any mix of physical and multicast addresses can be used. Unused addresses should duplicate one of the valid addresses.

Figure 2-12 shows the perfect filtering setup frame buffer format of the addresses.

Figure 2-12. Perfect Filtering Setup Frame Buffer Format

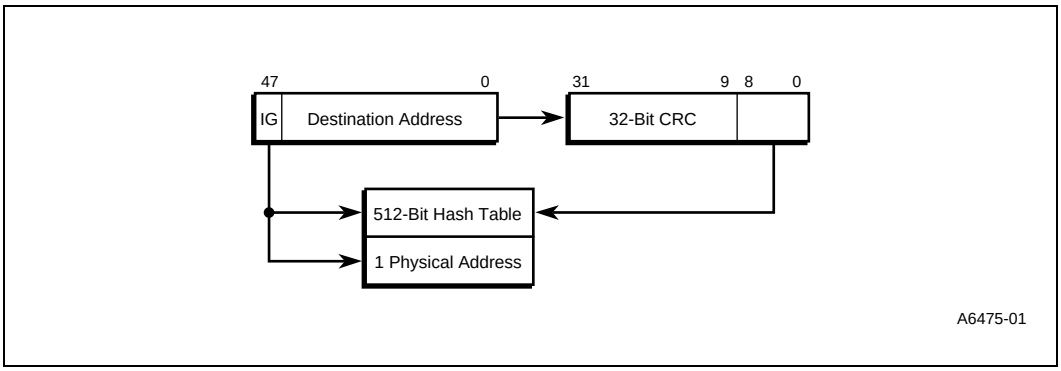


The low-order bit of the low-order bytes is the multicast bit of the address.

2.2.3.4 Imperfect Filtering Setup Frame Buffer

This section describes how the 21145 interprets a setup frame buffer in imperfect filtering mode (CSR6<0> is set). Figure 2-13 shows imperfect filtering.

Figure 2-13. Imperfect Filtering



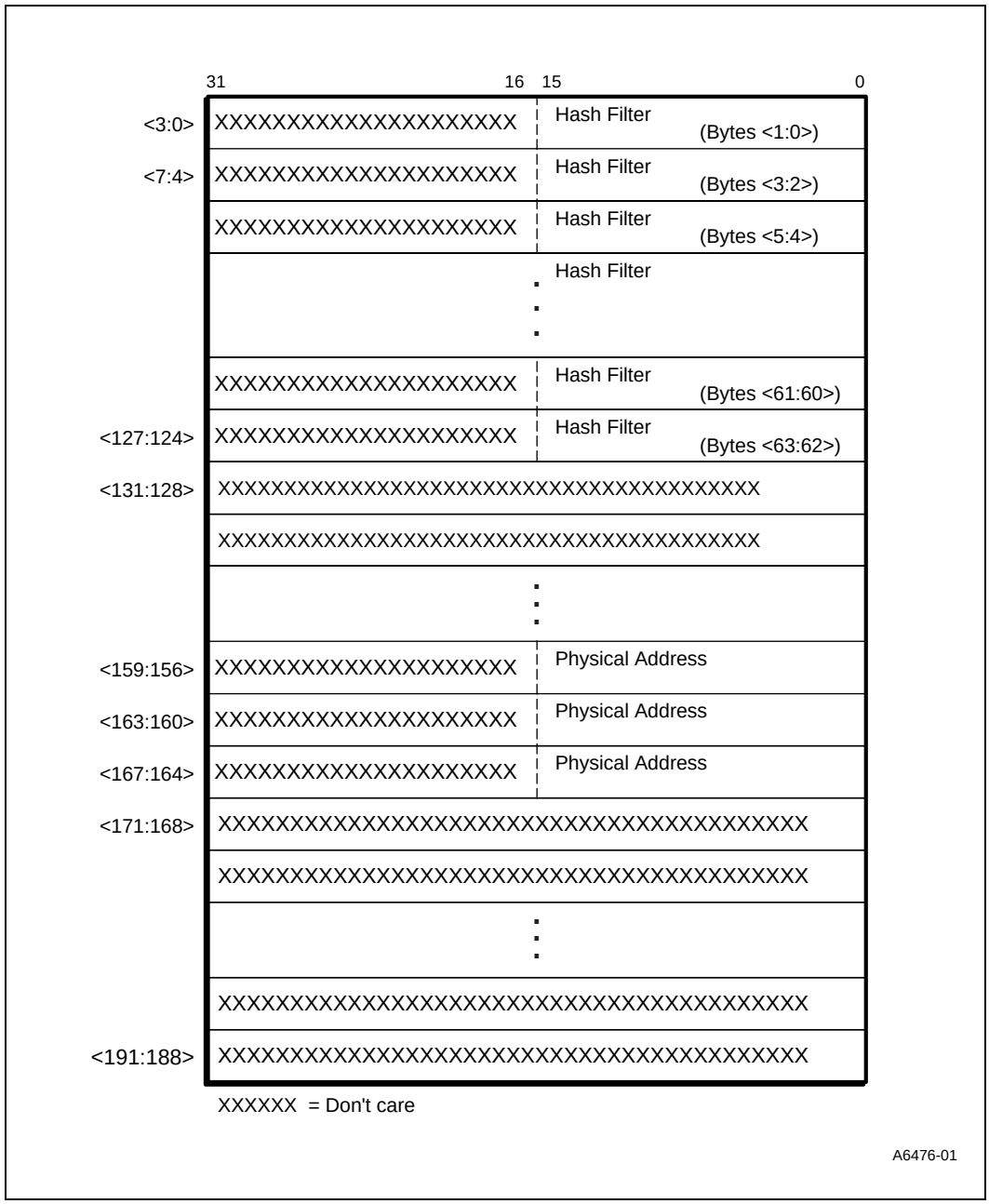
The 21145 can store 512 bits serving as hash bucket heads, and one *physical* 48-bit Ethernet address. Incoming frames with multicast destination addresses are subjected to imperfect filtering. Frames with physical destination addresses are checked against the single physical address.

For any incoming frame with a multicast destination address, the 21145 applies the standard Ethernet cyclic redundancy check (CRC) function to the first 6 bytes containing the destination address, then it uses the most significant 9 bits of the result as a bit index into the table. If the indexed bit is set, the frame is accepted. If the bit is cleared, the frame is rejected. (Appendix C provides an example of a hash index for a given Ethernet address.)

This filtering mode is called imperfect because multicast frames not addressed to this station may slip through, but it still decreases the number of frames that the host can receive. Imperfect filtering can only be used in the D0 power state.

Figure 2-14 shows the format for the hash table and the physical address.

Figure 2-14. Imperfect Filtering Setup Frame Buffer Format



Bits are sequentially numbered from right to left and down the hash table. For example, if the CRC (destination address) <8:0> = 33, the 21145 examines bit 1 in the third longword.

2.3 Functional Description

This section describes the reset commands, interrupt handling, and startup. It also describes the transmit and receive processes.

The functional operation of the 21145 is controlled by the driver interface located in the host communication area. The driver interface activity is controlled by control and status registers (CSRs), descriptor lists, and data buffers.

Descriptor lists and data buffers, collectively referred to as the host communication area, reside in host memory. These data structures process the actions and status related to buffer management. The 21145 transfers frame data to and from the receive and transmit buffers in host memory. Descriptors resident in the host memory point to these buffers.

2.3.1 Reset Commands

The following two commands are available to reset the 21145 hardware and software:

- Assert rst_l, to initiate a hardware reset.
- Assert CSR0<0>, to initiate a software reset.

For a proper hardware reset, both pci_clk and xtal1 clocks should be active. Note that after a hardware reset, the mode is set to 10BASE-T. For a proper software reset, both pci_clk and the correct serial clock (for example, mii_tclk when in MII mode or xtal1 when in either 10BASE-T or HomePNA mode) should be active. For both the hardware and software reset commands, the 21145 *aborts* all processing and starts the reset sequence. The 21145 initializes all internal states and registers.

Note: No internal states are retained, no descriptors are owned, and all the host-visible registers are set to the reset values. However, a software reset command has no effect on the configuration registers or on CSR6<18> port select.

The 21145 does not explicitly disown any owned descriptor; descriptor-owned bits can be left in a state indicating 21145 ownership. Section 2.2.1.1 and Section 2.2.2.1 provide a detailed description of own bits.

After either a hardware or software reset command, the first bus transaction to the 21145 should not be initiated for at least 50 PCI clock cycles. When the reset sequence completes, the 21145 can accept host commands. The receive and transmit processes are placed in the stopped state (Table 2-13 and Table 2-14). It is permissible to issue successive reset commands (hardware or software).

2.3.2 DMA Arbitration Scheme

The DMA arbitration scheme is used by the 21145 to grant precedence to the receive process instead of the transmit process (CSR0<1>). The technical expressions used in this table are described in the following list:

- *Txreq*—Specifies a DMA request for the transmit process to:
  - — Fetch descriptor.
  - — Close descriptor.
  - — Process setup packet.
  - — Transfer data from the host buffer to the transmit FIFO when there is sufficient space in the transmit FIFO for a full data burst.
- *Rxreq*—Specifies a DMA request for the receive process to:
  - — Fetch descriptor.
  - — Close descriptor.
  - — Transfer data from the receive FIFO to the host buffer when the receive FIFO contains sufficient data for a full data burst or contains the end of the packet.
- *TxEN*—Specifies that the 21145 is currently transmitting.
- *RxF<thrx*—Specifies that the amount of free bytes left in the receive FIFO is less than an internal threshold.
- *TxF<thtx*—Specifies that the amount of bytes in the transmit FIFO is less than an internal threshold.

Table 2-12 lists a description of the arbitration scheme.

Table 2-12. Arbitration Scheme

Txreq	Rxreq	TxEN	RxF<thrx	TxF<thtx	Chosen Process
0	0	0	—	—	—
0	0	1	—	—	—
0	1	0	—	—	Receive process
0	1	1	—	—	Receive process
1	0	0	—	—	Transmit process
1	0	1	—	—	Transmit process
1	1	0	—	—	Receive process
1	1	1	0	0	Transmit process
1	1	1	0	1	Transmit process
1	1	1	1	0	Receive process
1	1	1	1	1	Transmit process[1]

NOTE:
1. The transmit process choice is true only when working in half-duplex mode. When working in full-duplex mode, a round-robin arbitration scheme will be applied.

In addition to the arbitration scheme listed in Table 2-12, two other factors must be considered:

- The transmit process obtains a window for one burst between two consecutive receive packets.
- The receive process obtains a window for one burst between two consecutive transmit packets.

2.3.3 Interrupts

Interrupts can be generated as a result of various events. CSR5 contains all the status bits that might cause an interrupt. CSR7 contains an enable bit for each of the events that can cause an interrupt. An event will cause an interrupt only if it is enabled in CSR7.

The interrupts are divided into two groups: the normal interrupts and the abnormal interrupts. Each of these groups has a summary bit in CSR5, indicating that one of the events under the group has caused an interrupt. The 21145 asserts the int_l pin when at least one of the interrupt summary bits is set.

The following list contains the events that belong to the *normal* interrupts group:

CSR5<0>—Transmit interrupt
CSR5<2>—Transmit buffer unavailable
CSR5<6>—Receive interrupt
CSR5<11>—General-purpose timer expired
CSR5<14>—Early receive interrupt

The following list contains the events that belong to the *abnormal* interrupts group:

CSR5<1>—Transmit process stopped
CSR5<3>—Transmit jabber timeout
CSR5<4>—Link pass or autonegotiation completed
CSR5<5>—Transmit underflow
CSR5<7>—Receive buffer unavailable
CSR5<8>—Receive process stopped
CSR5<9>—Receive watchdog timeout
CSR5<10>—Early transmit interrupt
CSR5<12>—Link fail
CSR5<13>—Fatal bus error
CSR5<26>—General-purpose port interrupt
CSR5<27>—Link changed
CSR5<28>—HomePNA interrupt

Interrupt bits are cleared by writing a 1 to the bit position. When all enabled bits in one of the interrupt groups are cleared, the corresponding summary bit is cleared. If both summary bits are cleared, the 21145 deasserts the int_l pin.

Interrupts are not queued, and if the interrupting event recurs *before* the driver has responded to it, no additional interrupts are generated. For example, receive interrupt (CSR5<6>) indicates that one or more received frames were delivered to host memory. The driver must scan *all* descriptors, from the last recorded position to the first one owned by the 21145.

An interrupt is generated only *once* for simultaneous, multiple interrupting events. The driver must scan CSR5 for the interrupt cause or causes. The interrupt is not generated *again*, unless a new interrupting event occurs after the driver has cleared the appropriate CSR5 bits.

For example, transmit interrupt (CSR5<0>) and receive interrupt (CSR5<6>) are set simultaneously. The host acknowledges the interrupt, and the driver begins executing by reading CSR5. Next, receive buffer unavailable (CSR5<7>) is set. The driver writes back its copy of CSR5, clearing transmit interrupt and receive interrupt. The interrupt line is deasserted for at least one cycle and then asserted again with receive buffer unavailable.

2.3.3.1 Receive and Transmit Interrupt Mitigation

The interrupt mitigation timers and counters allow the software driver to reduce the number of transmit interrupts (CSR5<0>) and receive interrupts (CSR5<6>). This lowers CPU utilization for servicing a large number of interrupts.

The adapter has two counters for counting the received and transmitted packets, and two associated timers. The mitigation mechanism is similar for both receive and transmit interrupts.

Both counters and timers are programmed by writing to CSR11. Programming the counter to zero disables the counter effect on the interrupt mitigation mechanism. Programming the timer to zero disables the timer effect on the interrupt mitigation mechanism.

The counter defines the maximum number of received or transmit interrupts that can be pending before an interrupt is generated. The timer defines the maximum delay an interrupt can be pending before the interrupt is generated.

The timer and counter combination allows for the batching of several packets into a single interrupt with a limit for how long it can be pending. This single interrupt prevents throughput from being impeded in heavy traffic, while the time limit prevents resources from being held for too long in low traffic.

In interrupt mitigation mode, instead of immediately generating a receive or transmit interrupt, the adapter decrements the associated interrupt counter and starts the associated timer if it is not already started. The pending interrupt(s) is (are) generated when either the counter or the timer expires. Both counter and timer are then reloaded.

When the receive or the transmit process moves to the suspended or stopped state, any pending interrupt(s) are immediately generated.

This mechanism allows for reducing the number of interrupts without turning to the classic interrupt mode or polling mode where the CPU spends cycles on polling the interrupt status regardless of the traffic. This mechanism is also more efficient than the fixed interrupt rate interrupt scheme that generates the same rate of interrupts regardless of the traffic.

2.3.4 Initialization Procedure

The following sequence of checks and commands must be performed by the driver to prepare the 21145 for operation:

1. Wait 50 PCI clock cycles for the 21145 to complete its reset sequence.
2. Update configuration registers (Section 3.1):
   a. Read the configuration ID and revision registers to identify the 21145 and its revision.
   b. Write the configuration interrupt register (if interrupt mapping is necessary).
   c. Write the configuration base address registers to map the 21145 I/O or memory address space into the appropriate processor address space.

d. Write the configuration command register.

e. Write the configuration latency timer to match the system latency guidelines.

3. Write the configuration device and driver area register (CFDD) to move the 21145 out of Sleep mode.
4. Write CSR0 to set global host bus operating parameters (Section 8.3.2.1).
5. Write CSR7 to mask unnecessary (depending on the particular application) interrupt causes.
6. The driver must create the transmit and receive descriptor lists. Then, it writes to both CSR3 and CSR4, providing the 21145 with the starting address of each list (Section 8.3.2.7). The first descriptor on the transmit list may contain a setup frame (Section 2.2.3).

Caution: If address filtering (either perfect or imperfect) is desired, the receive process should only be started after the setup frame has been processed (Section 2.2.3).

7. Set jabber timers and initial SIA settings by writing to CSR13 (Section 8.3.2.16), CSR14 (Section 8.3.2.17), and CSR15 (Section 8.3.2.18) also, refer to Appendix C
8. Write CSR6 (Section 8.3.2.9) to set global serial parameters and to start both the receive and transmit processes. The receive and transmit processes enter the running state and attempt to acquire descriptors from the respective descriptor lists. Then the receive and transmit processes begin processing incoming and outgoing frames. The receive and transmit processes are independent of each other and can be started and stopped separately.

2.3.5 Receive Process

While in the running state, the receive process polls the receive descriptor list, attempting to acquire free descriptors. Incoming frames are processed and placed in acquired descriptors' data buffers. Status information is written to RDES0 of the last receive descriptor of the frame.

2.3.5.1 Descriptor Acquisition

The 21145 always attempts to acquire an extra descriptor in anticipation of incoming frames. Descriptor acquisition is attempted if any of the following conditions are satisfied:

- When start/stop receive (CSR6<1>) is set immediately after being placed in the running state.
- When the 21145 begins writing frame data to a data buffer pointed to by the current descriptor, and the buffer ends before the frame ends.
- When the 21145 completes the reception of a frame, and the current receive descriptor has been closed.
- When the receive process is suspended because of a host-owned buffer (RDES0<31>=0), and a new frame is received.
- When receive poll demand is issued (Section 8.3.2.5).

2.3.5.2 Frame Processing

As incoming frames arrive, the 21145 recovers the incoming data and clock pulses, and then sends them to the receive engine. The receive engine strips the preamble bits and stores the frame data in the receive FIFO. Concurrently, the receive section performs address filtering depending on the results of inverse filtering (CSR6<6>), hash/perfect receive filtering mode (CSR6<0>), and hash-only receive filtering mode (CSR6<2>), and also its internal filtering table. If the frame fails the address filtering, it is ignored and purged from the FIFO. Frames that are shorter than 64 bytes, because of collision or premature termination, are also ignored and purged from the FIFO (unless pass bad frames bit CSR6<3> is set).

After 64 bytes have been received, the 21145 requests the PCI bus to begin transferring the frame data to the buffer pointed to by the current descriptor. While waiting for the PCI bus, the 21145 continues to receive and store the data in the FIFO. After receiving the PCI bus, the 21145 sets first descriptor (RDES0<9>), to delimit the frame. Then, the descriptors are released when the OWN (RDES0<31>) bit is reset to 0, either as the data buffers fill up or as the last segment of a frame is transferred to a buffer. If a frame is contained in a single descriptor, both last descriptor (RDES0<8>) and first descriptor (RDES0<9>) are set.

The 21145 fetches the next descriptor, sets last descriptor (RDES0<8>), and releases the RDES0 status bits in the last frame descriptor. Then the 21145 sets receive interrupt (CSR5<6>). The same process repeats unless the 21145 encounters a descriptor flagged as being owned by the host. If this occurs, the receive process sets receive buffer unavailable (CSR5<7>) and then enters the suspended state. The position in the receive list is retained.

2.3.5.3 Receive Process Suspended

If a receive frame arrives while the receive process is suspended, the 21145 refetches the current descriptor in host memory. If the descriptor is now owned by the 21145, the receive process reenters the running state and starts the frame reception. If the descriptor is still owned by the host, the 21145 discards the current frame in the receive FIFO and increments the missed frames counter (CSR8<15:0>). If more than one frame is stored in the receive FIFO, the process repeats.

2.3.5.4 Stopping the Receive Process

To stop the receive process, the following sequence should be used:

1. Set CSR6<1>=0
2. Poll on CSR5 until CSR5<19:17>=000b

2.3.5.5 Receive Process State Transitions

Table 2-13 lists the receive process state transitions and the resulting actions.

Table 2-13. Receive Process State Transitions

From State	Event	To State	Action
Stopped	Start receive command.	Running	Receive polling begins from last list position or from the list head, if this is the first start receive command issued, or if the receive descriptor list address (CSR3) was modified by the driver.
Running	The 21145 attempts to acquire a descriptor owned by the host.	Suspended	Receive buffer unavailable (CSR5<7>) sets when the last acquired descriptor buffer is consumed. The position in the list is retained.
Running	Stop receive command.	Stopped	Receive process is stopped after the current frame, if any, is completely transferred to data buffers. Receive process stopped (CSR5<8>) is set. The position in the list is retained.
Running	Memory or host bus parity error encountered.	Running	The 21145 operation is stopped and fatal bus error (CSR5<13>) sets. The 21145 remains in the running state. A software reset must be issued to release the 21145.
Running	Reset command.	Stopped	Receive capability is cut off.
Suspended	Receive poll demand or incoming frame and available descriptor.	Running	Receive polling resumes from last list position.
Suspended	Stop receive command.	Stopped	Receive process stopped (CSR5<8>) is set.
Suspended	Reset command.	Stopped	None.

2.3.6 Transmit Process

While in the running state, the transmit process polls the transmit descriptor list for frames requiring transmission. After polling starts, it continues in either sequential descriptor ring order or chained order. When it completes frame transmission, status information is written into transmit descriptor 0 (TDES0). If the 21145 detects a descriptor flagged as owned by the host, or if an error condition occurs, the transmit process is suspended and both transmit buffer unavailable (CSR5<2>) and normal interrupt summary (CSR5<16>) are set.

Transmit interrupt (CSR5<0>) is set after completing transmission of a frame that has interrupt on completion (TDES1<31>) set in its last descriptor. When this occurs, the transmission process continues to run.

While in the running state, the transmit process can simultaneously acquire two frames. As the transmit process completes copying the first frame, it immediately polls the transmit descriptor list for the second frame. If the second frame is valid, the transmit process copies the frame before writing the status information of the first frame.

2.3.6.1 Frame Processing

Frames can be data-chained and span several buffers. Frames must be delimited by the first descriptor (TDES1<29>) and the last descriptor (TDES1<30>), respectively.

As the transmit process starts execution, the first descriptor must have TDES1<29> set. When this occurs, frame data transfers from the host buffer to the internal FIFO. Concurrently, if the current frame has the last descriptor TDES1<30> clear, the transmit process attempts to acquire the next descriptor. The transmit process expects this descriptor to have TDES1<29> clear. If TDES1<30> is clear, it indicates an intermediary buffer. If TDES1<30> is set, it indicates the last buffer of the frame.

After the last buffer of the frame has been transmitted, the 21145 writes back the final status information to the transmit descriptor 0 (TDES0) word of the descriptor that has the last segment set in transmit descriptor 1 TDES1<30>). At this time, if interrupt on completion (TDES1<31>) was set, the transmit interrupt (CSR5<0>) is set, the next descriptor is fetched, and the process repeats.

Actual frame transmission begins after the internal FIFO has reached either a programmable threshold CSR6<15:14> (Table 8-61), or a full frame is contained in the FIFO. There is also an option for store and forward mode CSR6<21>, (Table 8-61). Descriptors are released (OWN bit TDES0<31> clears) when the 21145 completes the packet transmission.

2.3.6.2 Transmit Polling Suspended

Transmit polling can be suspended by either of the following conditions:

- The 21145 detects a descriptor owned by the host (TDES0<31>=0). To resume, the driver must give descriptor ownership to the 21145 and then issue a poll demand command.
- A frame transmission is aborted when a locally induced error is detected. The appropriate transmit descriptor 0 (TDES0) bit is set.

If either of the previous two conditions occur, both abnormal interrupt summary (CSR5<15>) and transmit interrupt (CSR5<0>) are set, and the information is written to transmit descriptor 0, causing the suspension.

In both of the cases previously described, the position in the transmit list is retained. The retained position is that of the *descriptor following the last descriptor closed* (set to host ownership) by the 21145.

Note: The 21145 *does not* automatically poll the transmit descriptor list. The driver *must* explicitly issue a transmit poll demand command after rectifying the suspension cause, unless the transmit automatic polling (CSR0<19:17>) field is nonzero. In case of suspension as a result of underflow, the 21145 does not automatically poll the descriptors list even if CSR0<19:17> is nonzero.

2.3.6.3 Stopping the Transmit Process

To stop the transmit process, the following sequence should be used:

1. Set CSR6<13>=0
2. Poll on CSR5 until CSR5<22:20>=000b
3. In HomePNA mode, wait an additional 200µs

2.3.6.4 Transmit Process State Transitions

Table 2-14 lists the transmit process state transitions and the resulting actions.

Table 2-14. Transmit Process State Transitions

From State	Event	To State	Action
Stopped	Start transmit command.	Running	Transmit polling begins from one of the following positions: • The last list position. • The head of the list, if this is the first start command issued after CSR4 was initialized or modified.
Running	The 21145 attempts acquisition of a descriptor owned by the host.	Suspended	Transmit buffer unavailable. (CSR5<2>) is set.
Running	Frame transmission aborts because a locally induced underflow error (TDES0<1>) is detected (Section 2.2.2.1).	Suspended	The following bits are set: TDES0<1>—Underflow error CSR5<5>—Transmit underflow CSR5<15>—Abnormal interrupt summary
Running	Stop transmit command.	Stopped	Transmit process is stopped after the current frame, if any, is transmitted.
Running	Frame transmission aborts because a transmit jabber timeout (TDES0<14>) was detected (Section 2.2.2.1).	Stopped	The following bits are set: • TDES0<14>— Transmit jabber timeout • CSR5<1>—Transmit process stopped • CSR5<3>—Transmit jabber timeout • CSR5<15>—Abnormal interrupt summary
Running	Parity error detected by memory or host bus.	Running	Transmission is cut off and fatal bus error (CSR5<13>) is set. The 21145 remains in the running state. If a software reset occurs, normal operation continues.
Running	Reset command.	Stopped	Transmission is cut off. If CSR4 was not changed, the position in the list is retained. If CSR4 was changed, the next descriptor address is fetched from the header list (CSR4) when the poll demand command is issued. Transmit process stopped (CSR5<1>) is set.
Suspended	Transmit poll demand command issued.	Running	Transmit polling resumes from the last list position.
Suspended	Stop transmit command.	Stopped	Transmit process stopped (CSR5<1>) is set.
Suspended	Reset command.	Stopped	None.

2.3.7 Card Information Structure

The Card Information Structure (CIS), also known as tuples, is used in CardBus applications to store card information. This information is a structure of bytes used by the system software.

The 21145 supports two ways of storing the CIS data:

- External expansion ROM
- Serial ROM

Storing the CIS data in the serial ROM eliminates the need for an external expansion ROM and latches in CardBus applications.

The CIS pointer register is located in the PCI configuration space (CCIS). Its format is defined in the CardBus specification.

For more information about how to set the CIS pointer, see Appendix C of the *21X4 Serial ROM Format* available from the Intel Developer's Website (http://developer.intel.com/).

Host Bus Operation 3

This chapter describes the commands and operations of read and write cycles for a bus slave and a bus master. It also explains the initiation of termination cycles by the bus master or bus slave.

3.1 Overview

The peripheral component interconnect (PCI) is the physical interconnection used between highly integrated peripheral controller components and the host system. The 21145 uses the PCI bus to communicate with the host CPU and memory.

The 21145 is directly compatible with the *PCI Local Bus Specification*, Revision 2.1. The 21145 supports a subset of the PCI-bus cycles (transactions). When communicating with the host, the 21145 operates as a bus slave; when communicating with the memory, as a bus master.

All signals are sampled on the rising edge of the clock. Each signal has a setup and hold aperture with respect to the rising clock edge. Refer to the *21145 Phoneline/Ethernet LAN Controller Datasheet* for detailed timing information.

Note: The term clock cycle, as used in this chapter, refers to the PCI bus clock period specification.

3.2 Bus Commands

Table 3-1 lists the bus commands.

Table 3-1. Bus Commands

c_be_l<3:0>	Command	Type of Support
0000	Interrupt acknowledge	Not supported
0001	Special cycle	Not supported
0010	I/O read	Supported as target
0011	I/O write	Supported as target
0100	Reserved	—
0101	Reserved	—
0110	Memory read	Supported as master and target
0111	Memory write	Supported as master and target
1000	Reserved	—
1001	Reserved	—
1010	Configuration read	Supported as target
1011	Configuration write	Supported as target
1100	Memory read multiple	Supported as master and target[1, 2]
1101	Dual-address cycle	Not supported
1110	Memory read line	Supported as master and target[1, 2]
1111	Memory write and invalidate	Supported as master and target[1, 2]

1. Master support for this command is controlled by CSR0.
2. As PCI target, the 21145 will respond with a single 32-bit transfer. The second cycle of any multiple read or write command will cause a PCI disconnect termination. See Section 3.5.

3.3 Bus Slave Operation

All host accesses to CSRs and configuration registers in the 21145 are executed with the 21145 acting as the slave. The bus slave responds to the following operations:

- I/O read
- I/O write
- Configuration read
- Configuration write
- Memory read
- Memory write
- Memory write invalidate
- Memory read line
- Memory read multiple

Note: If the 21145 is targeted for a burst I/O or memory operation, it responds with a retry on the second data transaction.

3.3.1 Slave Read Cycle (I/O or Memory Target)

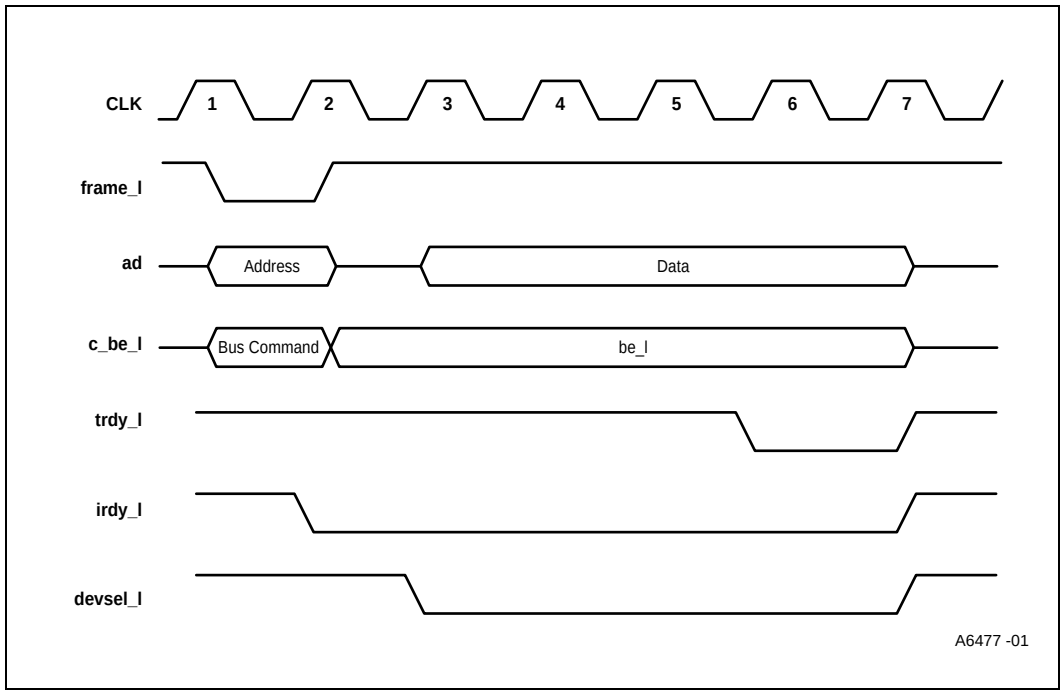
Figure 3-1 shows a typical slave read cycle. The 21145 I/O read cycle is executed as follows:

1. The host initiates the slave read cycle by asserting the frame_l signal, driving the address on the ad lines and driving the bus command (slave read operation) on the c_be_l lines.
2. The 21145 samples the address and the bus command on the next clock edge.
3. The host deasserts frame_l signal and asserts irdy_l signal.
4. The 21145 asserts devsel_l, and, at the next cycle, drives the data on the ad lines.
5. The read transaction completes when both irdy_l and trdy_l are asserted by the host and the 21145, respectively, on the same clock edge.

   The 21145 ignores c_be_l when used as Byte Enable, and acts as if it were 0000 (longword access).

   If the c_be_l lines are 1111, the ad bus read is 00000000H with correct parity.
6. The host and the 21145 terminates the cycle by deasserting irdy_l and trdy_l, respectively.

Figure 3-1. Slave Read Cycle



3.3.2 Slave Write Cycle (I/O or Memory Target)

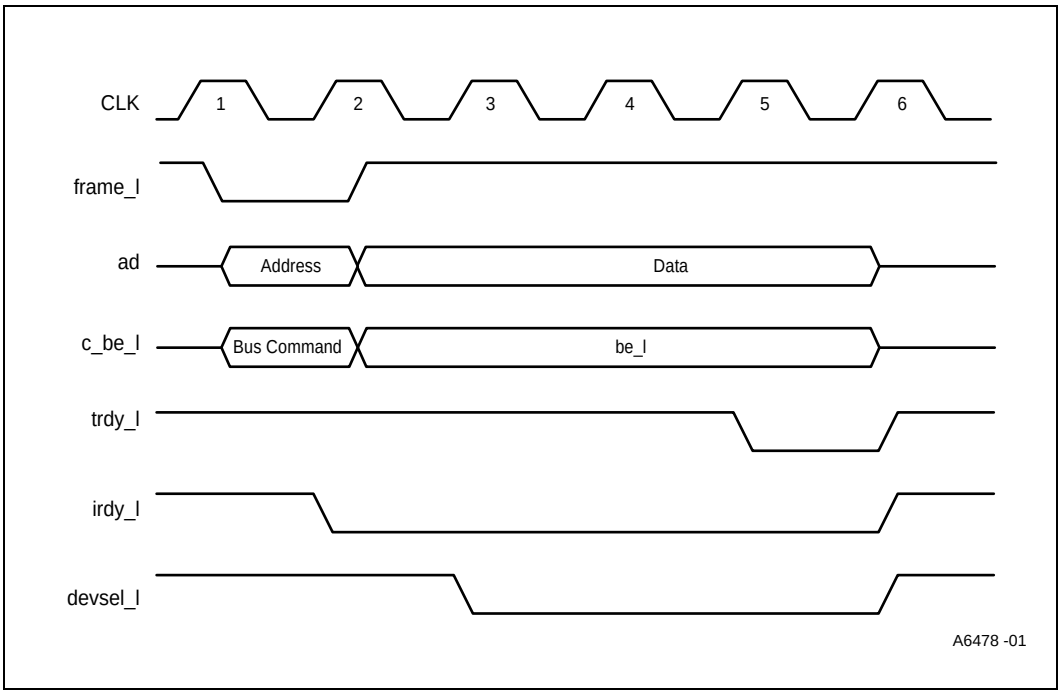
Figure 3-2 shows a typical slave write cycle. The 21145 slave write cycle is executed as follows:

1. The host initiates the slave write cycle by asserting the frame_l signal, driving both the address on the ad lines and the bus command (slave write operation) on the c_be_l lines.
2. The 21145 samples the address and the bus command on the next clock edge.
3. The host deasserts frame_l and drives the data on the ad lines along with irdy_l.
4. The 21145 samples the data, and also asserts both devsel_l and trdy_l.
5. The host and the 21145 complete the write transaction by asserting both irdy_l and trdy_l, respectively, on the same clock edge.

   The 21145 ignores c_be_l when used as Byte Enable, and acts as if it were 0000 (longword access).

   If the c_be_l lines are 1111, the write transaction completes normally on the bus, but the write transaction to the CSR is not executed.
6. The host and the 21145 terminate the cycle by deasserting irdy_l and trdy_l, respectively.

Figure 3-2. Slave Write Cycle



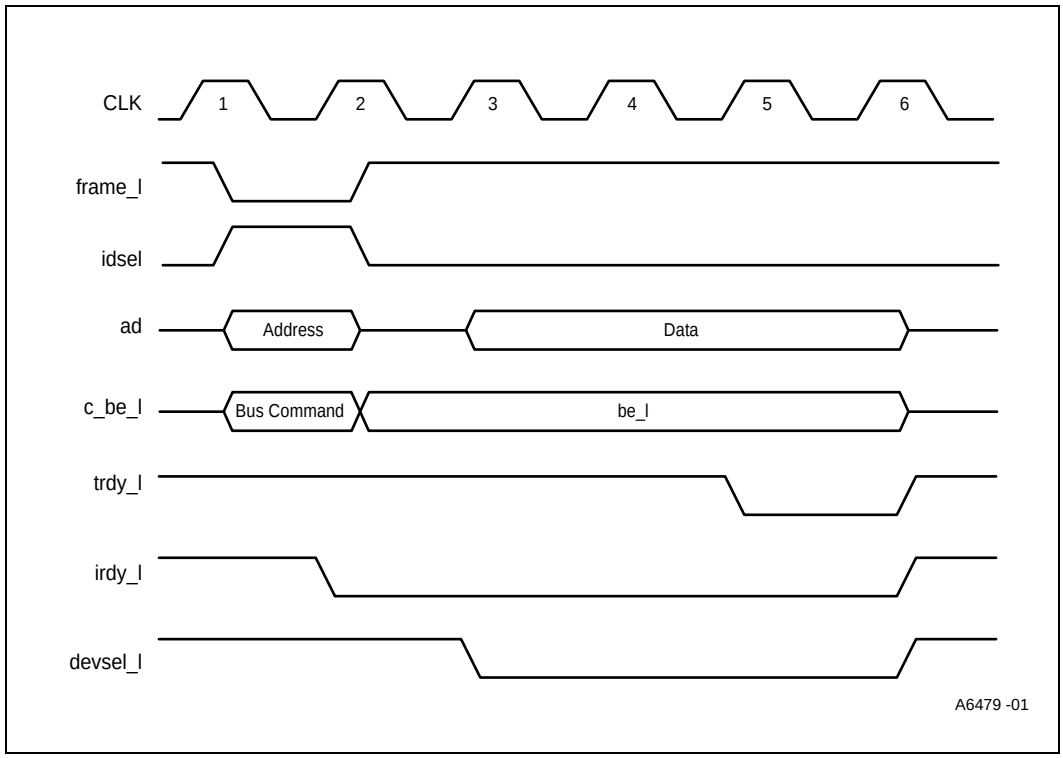
3.3.3 Configuration Read and Write Cycles

The 21145 provides a way for software to analyze and configure the system before defining any address assignments or mapping. The 21145 provides 256 bytes of configuration registers. Chapter 8 describes these registers.

Note: Configuration space accesses support the Byte Enable mask for writes only.

Figure 3-3 shows a configuration read cycle. The host selects the 21145 by asserting idsel. The 21145 responds by asserting devsel_l. The remainder of the read cycle is similar to the slave read cycle (Section 3.3.1).

Figure 3-3. Configuration Read Cycle



3.4 Bus Master Operation

All memory accesses are completed with the 21145 as the master on the PCI bus. The bus master can perform the following operations:

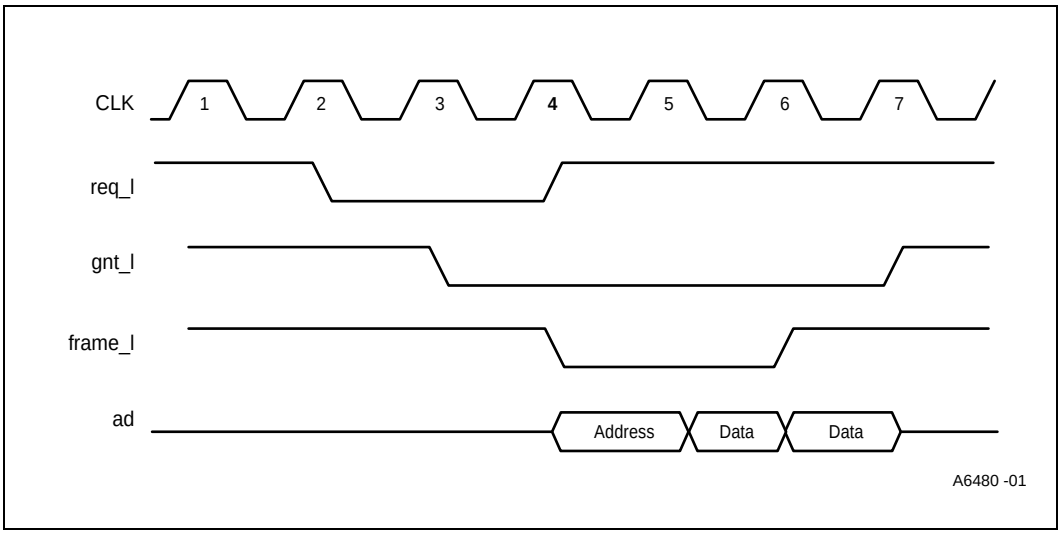
- Bus arbitration
- Memory read cycle
- Memory write cycle
- Termination cycles

3.4.1 Bus Arbitration

The 21145 uses the PCI central arbitration mechanism with its unique request (req_l) and grant (gnt_l) signals. Figure 3-4 shows the bus arbitration mechanism. The 21145 bus arbitration is executed as follows:

1. The 21145 requests the bus by asserting req_l.
2. The arbiter, in response, asserts gnt_l (gnt_l can be deasserted on any clock).
3. The 21145 ensures that its gnt_l is asserted on the clock edge that it wants to drive frame_l. (If gnt_l is deasserted, the 21145 does not proceed.)
4. The 21145 deasserts req_l on the cycle that it asserts frame_l.

Figure 3-4. Bus Arbitration



The 21145 uses gnt_l according to the following rules:

- If gnt_l is deasserted together with the assertion of frame_l, the 21145 continues its bus transaction.
- If gnt_l is asserted while frame_l remains deasserted, the arbiter can deassert gnt_l at any time. The 21145 does not assert frame_l until it is granted again.

3.4.2 Memory Read Cycle

The memory read cycle is executed when the 21145 performs one of the following operations:

- Memory read
- Memory read multiple
- Memory read line

The 21145 chooses one of these commands for a memory read cycle according to the conditions described in the read line enable (CSR0<23>) bit and the read multiple enable (CSR0<21>) bit descriptions.

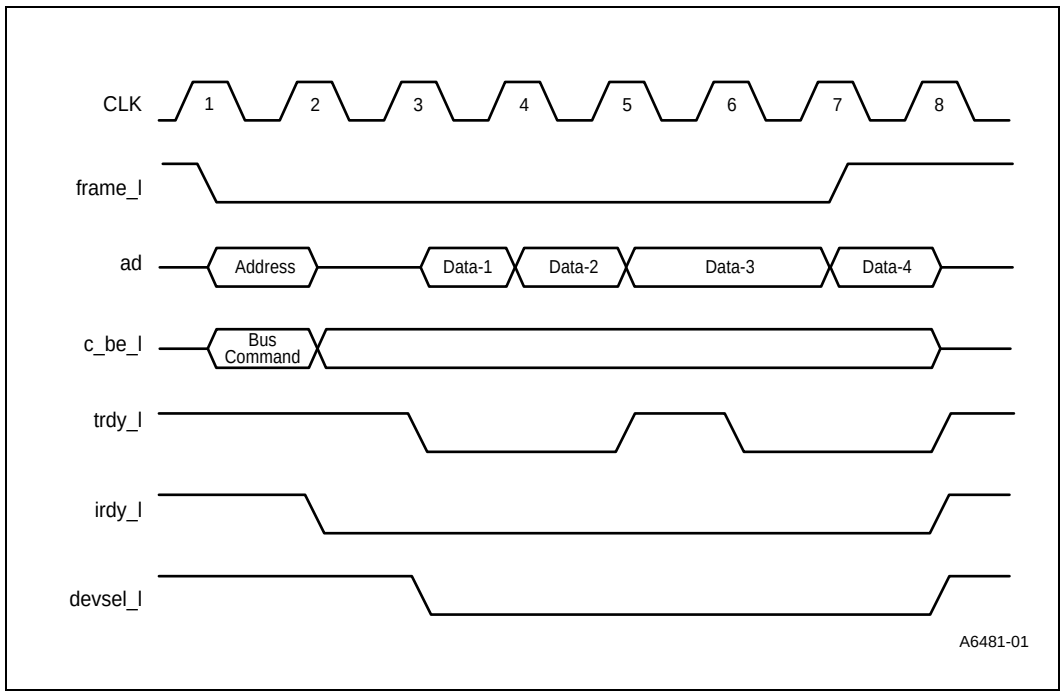
The memory read cycle is executed as follows:

1. The 21145 initiates the memory read cycle by asserting frame_l. It also drives the address on the ad lines and the appropriate bus command (memory read, memory read multiple, or memory read line) on the c_be_l lines.
2. The memory controller samples the address and the bus command on the next clock edge.
3. The 21145 asserts irdy_l until the end of the read transaction.
4. During the data transfer cycles, c_be_l indicates which byte lines are involved in each cycle. The 21145 drives 0000 on the c_be_l lines (longword access).
5. The memory controller drives the data on the ad lines and asserts trdy_l.
6. The 21145 samples the data on each rising clock edge when both irdy_l and trdy_l are asserted.

7. The previous two steps can be repeated a number of times.
8. The cycle is terminated when frame_l is deasserted by the 21145.
9. Signal irdy_l is deasserted by the 21145 and trdy_l is deasserted by the memory controller.

Figure 3-5 shows the memory read cycle.

Figure 3-5. Memory Read Cycle



3.4.3 Memory Write Cycle

The memory write cycle is executed when the 21145 performs one of the following operations:

- Memory write
- Memory write and invalidate

The 21145 chooses one of these commands for a memory write cycle according to the conditions described in the memory write and invalidate enable (CSR0<24>) bit description.

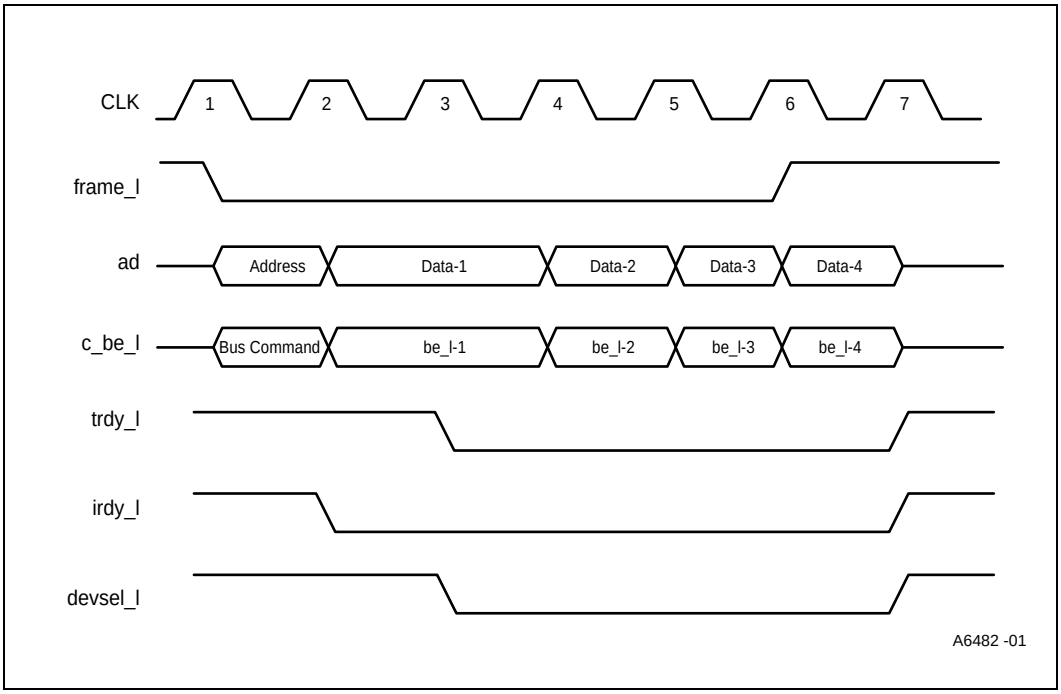
The memory write cycle is executed as follows:

1. The 21145 initiates the memory write cycle by asserting frame_l. It also drives the address on the ad lines and the appropriate bus command (memory write or memory write and invalidate) on the c_be_l lines.
2. The 21145 asserts irdy_l until the end of the transaction and drives the data on the ad lines.
3. The memory controller samples the address and the bus command on the next clock edge and asserts devsel_l.
4. During the data transfer cycles, the c_be_l lines indicate which byte lines are involved in each cycle. The 21145 drives 0000 on the c_be_l lines (longword access).

5. The memory controller samples the data and asserts trdy_l. Each data cycle is completed on the rising clock edge when both irdy_l and trdy_l are asserted.
6. The previous two steps can be repeated a number of times.
7. The 21145 terminates the cycle by deasserting frame_l.
8. The 21145 deasserts irdy_l and the memory controller deasserts trdy_l.

Figure 3-6 shows the memory write cycle.

Figure 3-6. Memory Write Cycle



3.5 Termination Cycles

Termination cycles can be initiated during either slave or master cycles.

3.5.1 Slave-Initiated Termination

A slave-initiated termination can occur when the 21145 operates as a slave device on the PCI bus. A slave can initiate the following types of terminations:

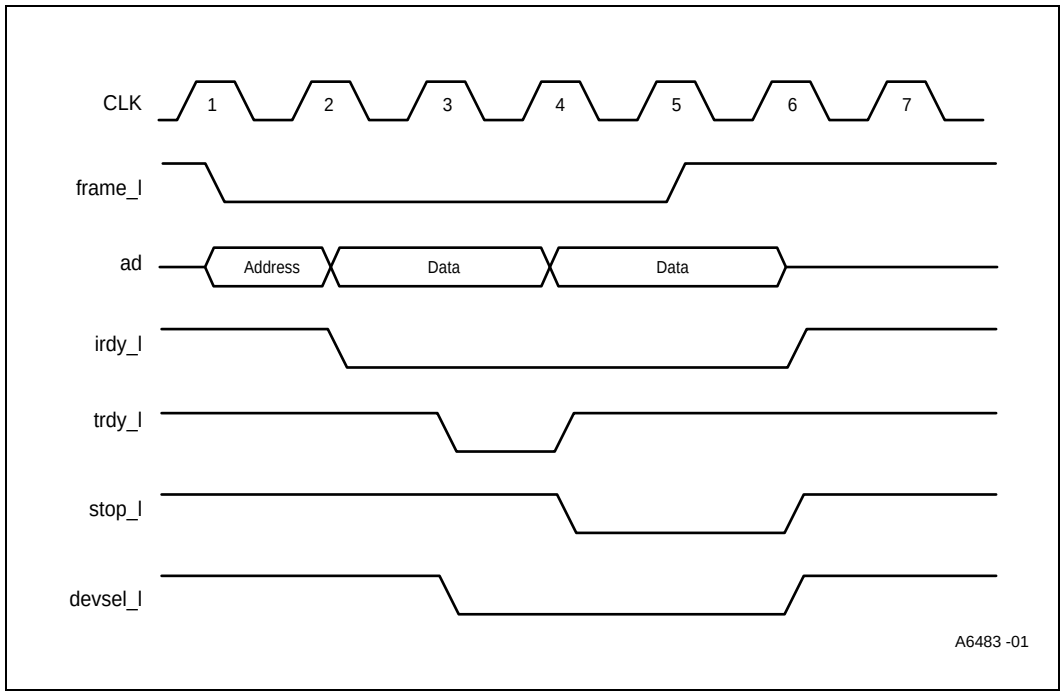
- Disconnect
- Retry

3.5.1.1 Disconnect Termination

The 21145 initiates disconnect termination in slave mode when it is accessed by the host with I/O or memory burst cycles. The 21145 asserts stop_l to request the host to terminate the transaction. After stop_l is asserted, it remains asserted until frame_l is deasserted.

Figure 3-7 shows the disconnected device (the host) releasing the bus. The host retries the last data transaction after acquiring the bus in a different arbitration.

Figure 3-7. 21145-Initiated Disconnect Cycle



3.5.1.2 Retry Termination

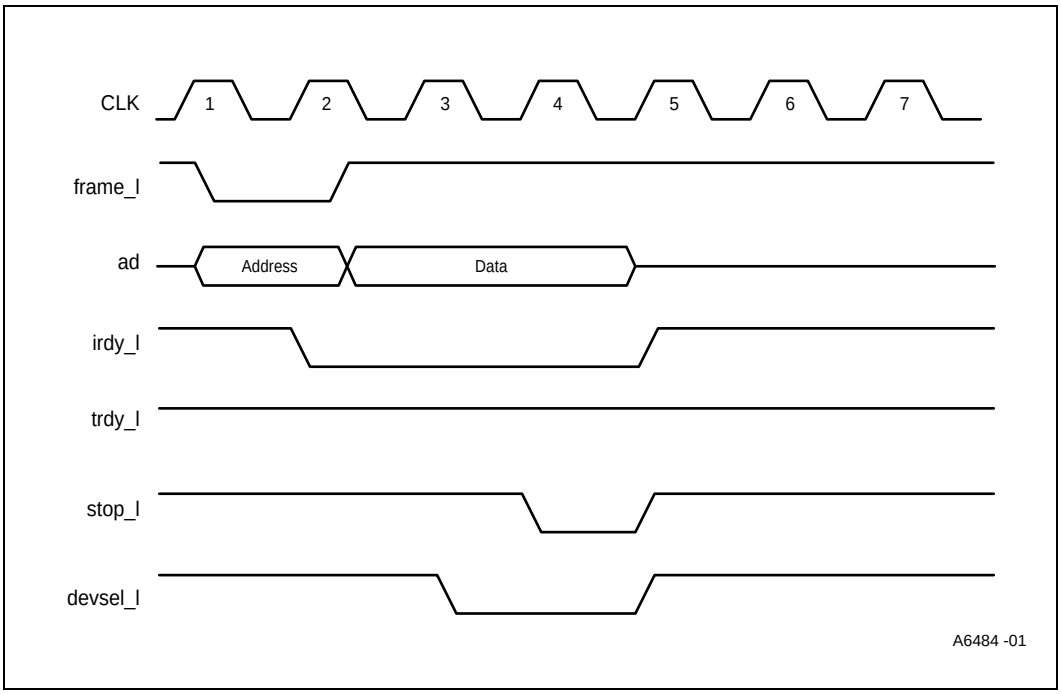
The 21145 initiates retry termination in slave mode when one of the following transactions occur:

- The 21145 registers CSR9 and CSR10 are accessed by the host, while the 21145 is still handling either a previous expansion ROM or serial ROM access.
- The 21145 configuration registers CSID and CCIS are accessed by the host, before their contents are loaded from the serial ROM.

The 21145 does not assert trdy_l in response to these host accesses. It asserts stop_l requesting that the host terminate the transaction. Signal stop_l remains asserted until irdy_l is deasserted.

Figure 3-8 shows the retried device (the host) releasing the bus. The host retries the last data transaction after acquiring the bus in a different arbitration.

Figure 3-8. 21145-Initiated Retry Cycle



3.5.2 Master-Initiated Termination

A master-initiated termination can occur when the 21145 operates as a master device on the PCI bus. Terminations can be issued by either the 21145 or the memory controller.

The 21145 can perform the following terminations:

- Normal completion
- Timeout
- Master abort

The memory-controller can perform the following terminations (target):

- Target abort
- Target disconnect
- Target retry

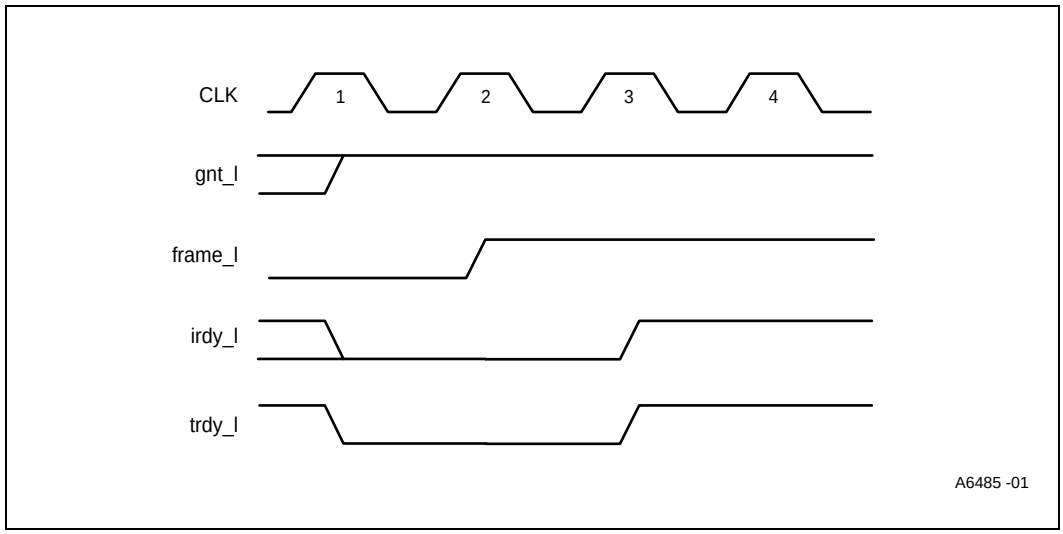
3.5.2.1 21145-Initiated Termination

A 21145-initiated termination occurs when frame_l is deasserted and irdy_l is asserted. This indicates to the memory controller that the final data phase is in progress. The final data transfer occurs when both irdy_l and trdy_l assert. The transaction completes when both frame_l and irdy_l deassert. This is an idle bus condition.

Normal Completion

Figure 3-9 shows a normal completion cycle termination. This indicates that the 21145 successfully completed its intended transaction.

Figure 3-9. Normal Completion



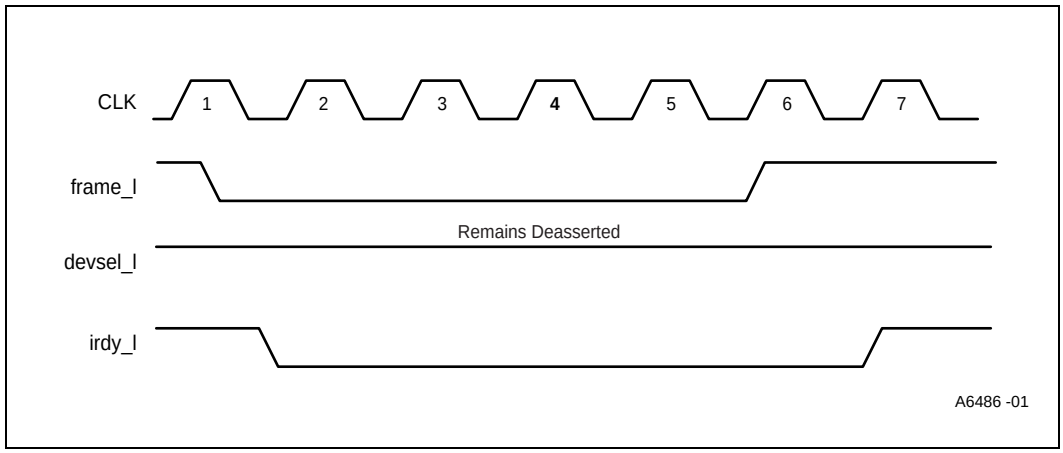
Timeout

A timeout cycle termination occurs when the gnt_l line has been deasserted by the arbiter and the 21145 internal latency timer has expired. However, the intended transaction has not completed. A maximum of two additional data phases are permitted and then the 21145 performs a normal transaction completion.

Master Abort

If the target does not assert devsel_l within five cycles from the assertion of frame_l, the 21145 performs a normal completion. It then releases the bus and asserts both master abort (CFCS<29>) and fatal bus error (CSR5<13>). Figure 3-10 shows the 21145 master abort termination.

Figure 3-10. Master Abort



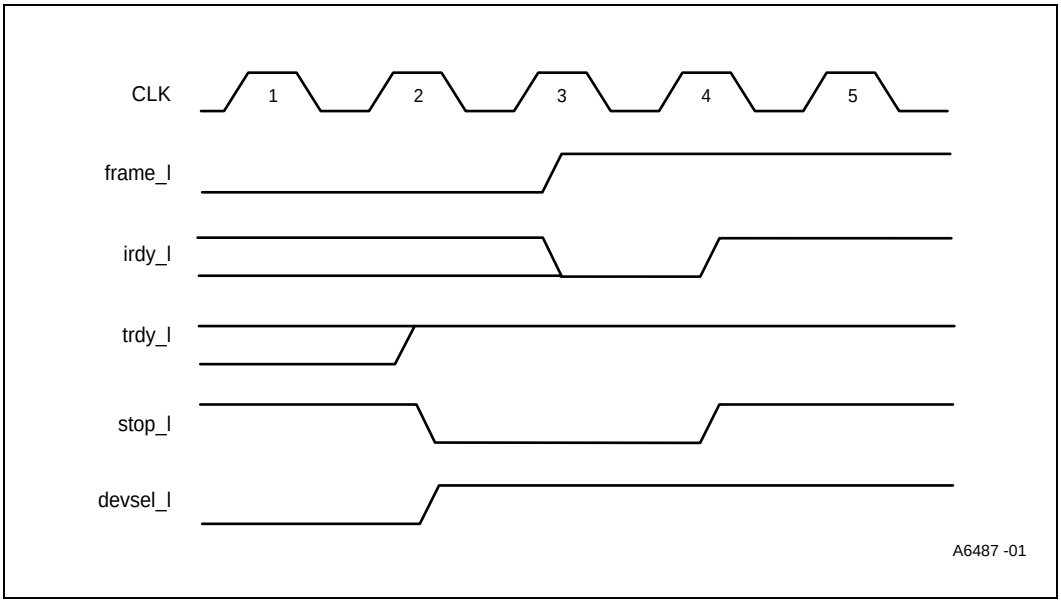
3.5.2.2 Memory-Controller-Initiated Termination

The memory controller or target can initiate certain terminations when the 21145 is the bus master.

Target Abort

The 21145 aborts the bus transaction when the target asserts stop_l and deasserts devsel_l. This indicates that the target wants the transaction to be aborted. The 21145 releases the bus and asserts both received target abort (CFCS<28>) and fatal bus error (CSR5<15>). Figure 3-11 shows the 21145 target abort.

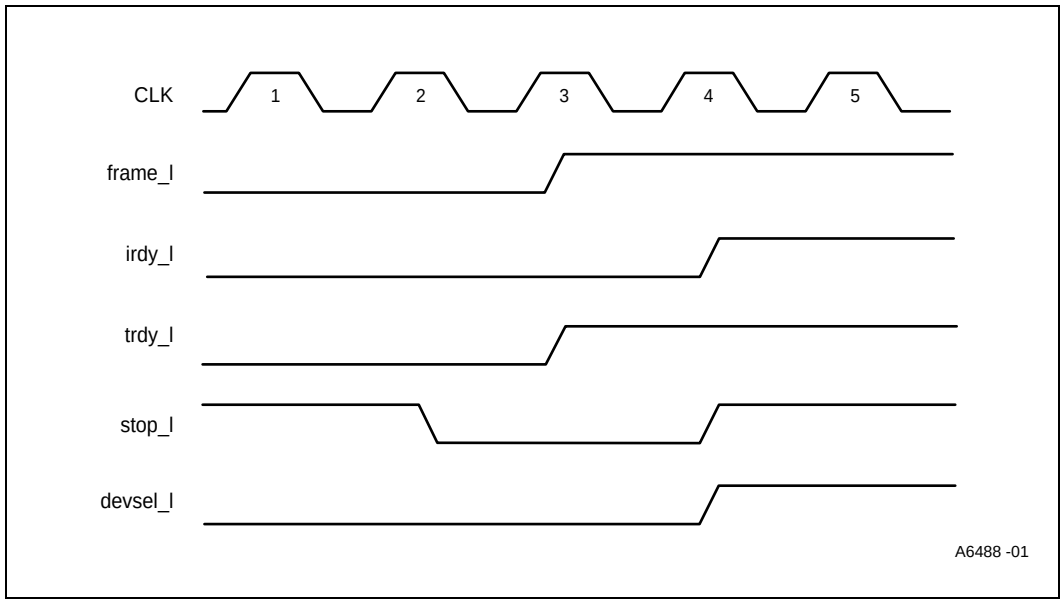
Figure 3-11. Target Abort



Target Disconnect Termination

The 21145 terminates the bus transaction when the target asserts stop_l, which remains asserted until frame_l is deasserted. The 21145 releases the bus. Then, it retries at least the last data transaction after regaining the bus in another arbitration. Figure 3-12 shows the 21145 target disconnect.

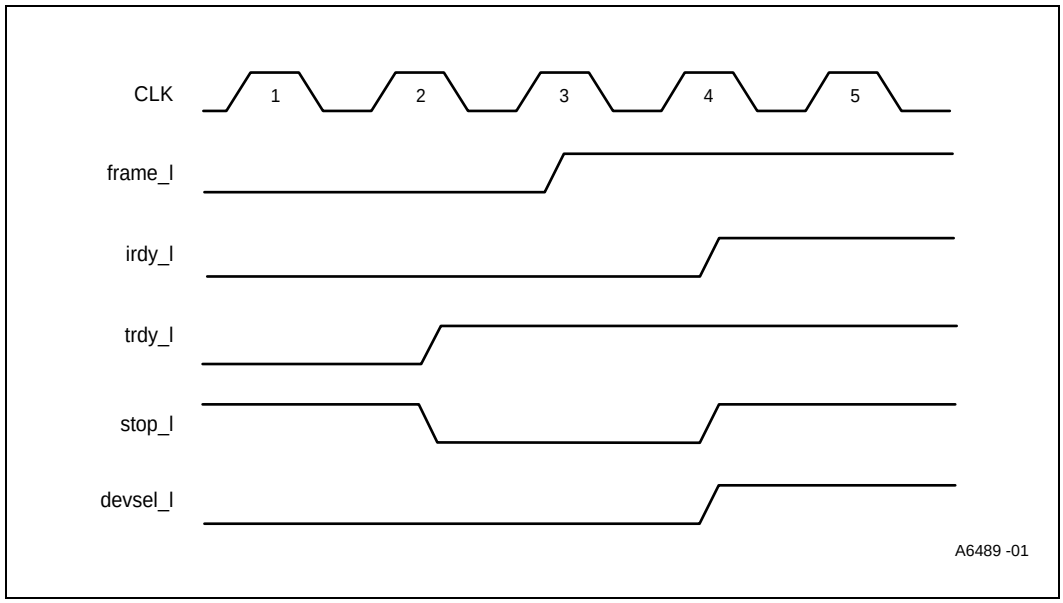
Figure 3-12. Target Disconnect



Target Retry

The 21145 retries the bus transaction when the target asserts stop_l and deasserts trdy_l; stop_l remains asserted until frame_l is deasserted. The 21145 releases the bus. Then, it retries at least the last two data transactions after regaining the bus in another arbitration. Figure 3-13 shows the 21145 target retry.

Figure 3-13. Target Retry

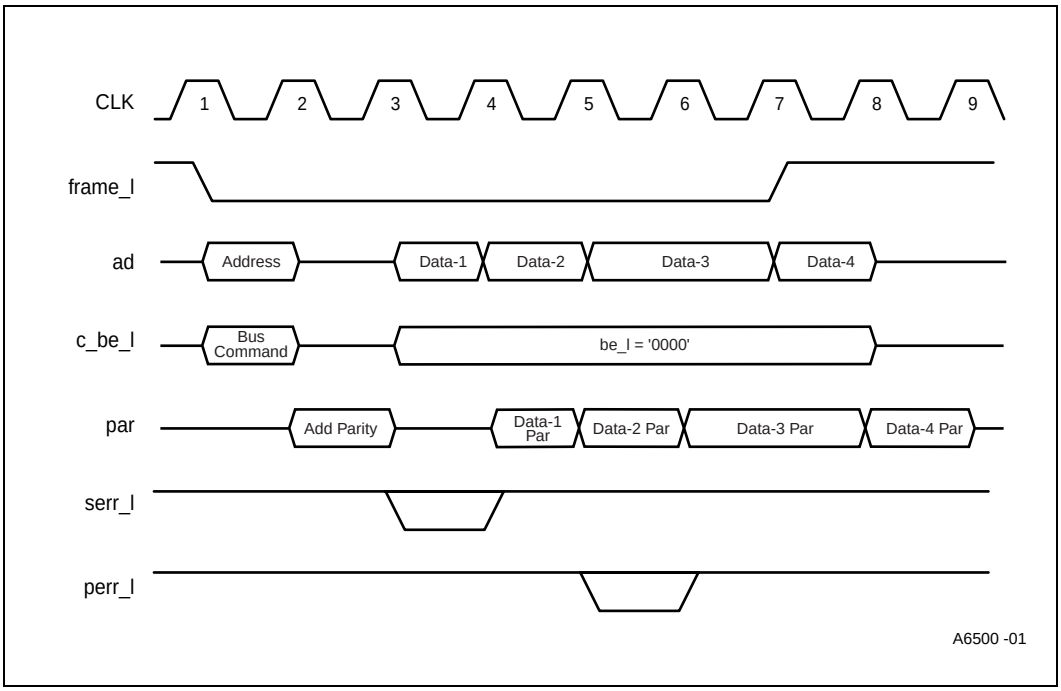


3.6 Parity

The 21145 supports parity generation on all address, data, and command bits. Parity is always checked and generated on the 32-bit address and data bus (ad) as well as on the four command (c_be_l) lines. The 21145 always transfers stable values (1 or 0) on all the ad and c_be_l lines. If a data parity error is detected or perr_l is asserted when the 21145 is a bus master, the 21145 asserts data parity report (CFCS<24>) and fatal bus error (CSR5<13>).

Figure 3-14 shows an example of parity generation on a memory write burst transaction. Note that valid parity is generated one cycle after the address and data segments were generated on the bus. One cycle after the assertion of the address parity, serr_l is asserted for one cycle because of an address parity error during slave operation. One cycle after the assertion of the data parity, perr_l is asserted because of a parity data error in either slave write or master read operations.

Figure 3-14. Parity Operation



3.7 Parking

Parking in the PCI bus allows the central arbiter to pause any selected agent. The 21145 enters the parking state when the arbiter asserts its gnt_l line while the bus is idle.

3.8 PCI/CardBus Clock Control through Clkrun

In order to reduce power consumption during idle time, a PCI/CardBus system can dynamically control the bus clock using the clkrun_l line. The host asserts this line to indicate normal operation of the system clock. It may deassert this line to indicate to devices connected to the bus that the clock is going to be stopped or slowed down to a nonoperational frequency. A device connected to the bus may reject the request to stop the clock by asserting clkrun_l line.

The 21145 requests that the system clock be maintained when one or more of the following conditions is true:

- PCI slave or master access is in progress
- Serial ROM interface is active
- Expansion ROM port is active
- Transmit is in progress
- Receive is in progress
- Carrier is sensed
- Link pass or link fail interrupt is pending
- Hardware or software reset is in progress
- The 21145 is set to normal mode and is not in D2 or D3
- Func0_HwOptions<4> (EnableCLKRUN) in the serial ROM is cleared
- Receive interrupt is pending for timer expiration in the interrupt mitigation mechanism
- Modem interrupt is pending (176-pin device only).
- The mdm_rst pin is asserted (176-pin device only)

The 21145 requests that the system clock be restored, when one or more of the following events occur:

- PCI slave access
- Carrier is sensed on the LAN
- Power-management event was detected
- Link change event was detected
- Autonegotiation is completed
- A modem interrupt is pending (176-pin device only).

Figure 3-15 shows the PCI/CardBus clock restart or speed-up timing characteristics.

Figure 3-15. PCI/CardBus Clock—Restart or Speed-Up

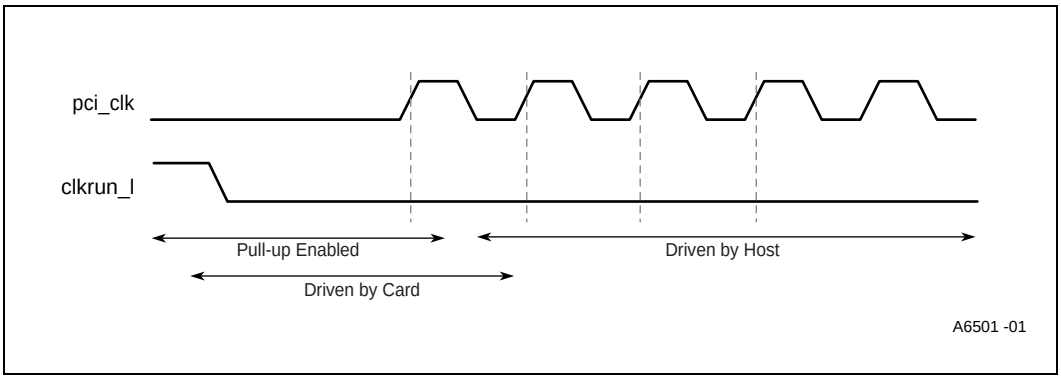
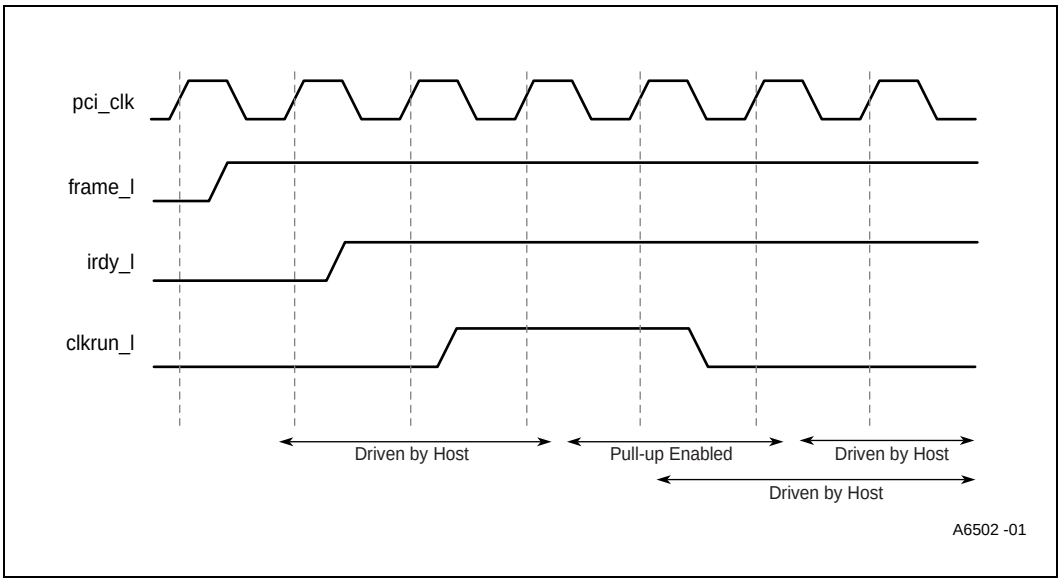


Figure 3-16 shows the maintaining PCI/CardBus clock timing characteristics.

Figure 3-16. PCI/CardBus Clock—Maintaining Speed



While the PCI/CardBus clock is stopped through clkrun, interrupts from the general-purpose port are not issued.

Network Interface Operation 4

This chapter describes the operation of the MII/SYM port, the 10BASE-T port, and the HomePNA port. It also describes media access control (MAC), loopback, and full-duplex operations. Appendix C and Table 8-86 through Table 8-90 describe the port selection procedure.

For operation, the 21145 must be provided with a 20 MHz signal.

4.1 MII/SYM Port

This section provides a description of the 100BASE-T terminology, the interface, the signals used, and the operating modes.

4.1.1 100BASE-T Terminology

This subsection provides a description of the 100BASE-T terminology used for the MII/SYM port. A list of these terms follows:

- Media-independent interface (MII) is defined between the media access control (MAC) sublayer and the physical layer protocol (PHY) layer.
- Physical coding sublayer (PCS) is a sublayer within the PHY defined by 100BASE-T. The PCS implements the higher level functions of the PHY.
- 100BASE-T is a generic term that refers to all members in the IEEE 802.3 family of 100 Mb/s carrier-sense multiple access with collision detection (CSMA/CD) standards.
- 100BASE-T4 is the standard IEEE 802.3 for 100 Mb/s, using unshielded twisted-pair (UTP) category 3 (CAT3) cables.
- 100BASE-X refers to all members of the IEEE 802.3 family contained in the 100 Mb/s CSMA/CD standard. It implements a specific physical medium attachment (PMA) and PCS. Members of this family include 100BASE-TX and 100BASE-FX.
- 100BASE-TX refers to the IEEE 802.3 PHY layer, which includes the 100BASE-X PCS and PMA together with the physical layer medium dependent (PMD). It uses UTP category 5 (CAT5) cables and STP cables.
- 100BASE-FX refers to the IEEE 802.3 PHY layer, which includes the 100BASE-X PCS and PMA together with the PMD. It uses multimode fiber.

4.1.2 Interface Description

The MII port is an IEEE 802.3 compliant interface that provides a simple, inexpensive, and easily implemented interconnection between the MAC sublayer and PHY layer. It also interconnects the PHY layer devices and station management (STA) entities. This interface has the following characteristics:

- Supports both 100 Mb/s and 10 Mb/s data rates
- Contains data and delimiters that are synchronous to clock references
- Provides independent, 4-bit-wide transmit and receive data paths

- Uses TTL signal levels, compatible with both TTL and CMOS logic types
- Provides a simple management interface

4.1.2.1 Signal Standards

Table 4-1 provides the standards that reference the MII/SYM port signal names with the appropriate IEEE 802.3 signal names.

Table 4-1. IEEE 802.3 and MII/SYM Signals

MII/SYM Signals	IEEE 802.3 Signals	Purpose
mii_clsn	COL	Collision detect is asserted by the PHY layer when it detects a collision on the medium. It remains asserted while this condition persists. For the 10 Mb/s implementation, collision is derived from the signal quality error of the PMA. For the 100 Mb/s implementation, collision is defined for each PHY layer separately.
mii_crs	CRS	Carrier sense is asserted by the PHY layer when either the transmit or receive medium is active (not idle).
mii_dv	RX_DV	Receive data valid is asserted by the PHY layer when the first received preamble nibble is driven over the MII/SYM and remains asserted for the remainder of the frame.
mii_rx_err	RX_ERR	Receive error is asserted by the PHY layer to indicate either a coding error or any other type of error that the MAC cannot detect was received. This error was detected on the frame currently being received and transferred over the MII/SYM.
mii_mdc	MDC	Management data clock is the clock reference for the mii_mdio signal.
mii_mdio	MDIO	Management data input/output is used to transfer control signals between the 21145 and the MII PHY. The 21145 is capable of initiating the transfer of control signals to and from the PHY device by using this line.
mii/sym_rclk	RX_CLK	Receive clock synchronizes all receive signals.
mii/sym_rxd<3:0>	RXD<3:0>	These lines provide receive data.
mii/sym_tclk	TX_CLK	Transmit clock synchronizes all transmit signals.
mii/sym_txd<3:0>	TXD<3:0>	These lines provide transmit data.
mii_txen	TX_EN	Transmit enable is asserted by the MAC sublayer when the first transmit preamble nibble is driven over the MII/SYM and remains asserted for the remainder of the frame.
Note: The remaining three signals are activated when the MII/SYM port uses the 21145 PCS function for 100Base-TX or 100Base-FX operation.		
sd	—	Signal detect indication is supplied by an external PMD device.
sym_rxd<4>	—	This line is used for receive data.
sym_txd<4>	—	This line is used for transmit data.

4.1.2.2 Operating Modes

The 21145 implements the MII/SYM port signals (Table 4-1) to support the following operating modes:

- **MII 100 Mb/s mode**—The 21145 implements the MII with a data rate of 100 Mb/s and both the receive clock (mii/sym_rclk) and the transmit clock (mii/sym_tclk) operate at 25 MHz. In this mode, the 21145 can be used with any device that implements the 100BASE-T PHY layer (for example, 100BASE-TX, 100BASE-FX, or 100BASE-T4) and an MII.
- **MII 10 Mb/s mode**—The 21145 implements the MII with a data rate of 10 Mb/s and both the receive clock mii/sym_rclk and the transmit clock mii/sym_tclk operate at 2.5 MHz. In this mode, the 21145 can be used with any device that implements the 10 Mb/s PHY layer and an MII.
- **100BASE-TX mode**—The 21145 implements certain functions of the PCS for STP PMD and UTP CAT5 PMD. The receive symbols are 5 bits wide and are transferred over the mii/sym_rxd<3:0> and sym_rxd<4> lines. The transmit symbols are also 5 bits wide and are transferred over the mii/sym_txd<3:0> and sym_txd<4> lines. The 21145 implements the following functions:
  - 4-bit and 5-bit decoding and encoding
  - Start-of-stream delimiter (SSD) and end-of-stream delimiter (ESD) detection and generation
  - Bit alignment
  - Carrier detect
  - Collision detect
  - Symbol error detection
  - Scrambling and descrambling
  - Link timer
- **100BASE-FX mode**—The 21145 implements certain functions of the PCS sublayer for multimode fiber. The receive symbols are 5 bits wide and are transferred over the mii/sym_rxd<3:0> and sym_rxd<4> lines. The transmit symbols are also 5 bits wide and are transferred over the mii/sym_txd<3:0> and sym_txd<4> lines. The 21145 implements the following functions:
  - 4-bit and 5-bit decoding and encoding
  - SSD and ESD detection and generation
  - Bit alignment
  - Carrier detect
  - Collision detect
  - Symbol error detection
  - Link timer

This mode enables a direct interface with existing FDDI TP-PMD devices that implement the physical functions.

Note: The SSD detection logic compares the incoming data to JK and not to IJK (this complies with IEEE 802.3, draft number 2).

4.2 10BASE-T Port

The 10BASE-T protocol includes the following functions:

- Supports data driver and is receiver compatible with 10BASE-T specifications
- Implements Manchester decoder for incoming data
- Implements Manchester encoder for outgoing data
- Contains on-chip, 20 MHz crystal oscillator circuitry
- Enables watchdog timers on incoming and outgoing data
- Contains 10BASE-T enhanced features that include:
  - — Smart squelch, rejecting noise detected by the 10BASE-T receiver interface
  - — Combined autopolarity and link test detection, presenting a robust algorithm for detection of both wire failure and switching of wires. Polarity correction is automatically done, while wire failure is reported to higher layers.

4.2.1 Manchester Decoder

The Manchester decoder is a phase-locked loop decoder that provides received clocks and data to the media access control (MAC) interface (Section 4.4).

4.2.2 Manchester Encoder

The Manchester encoder receives clocked data from the transmit engine and uses the 20 MHz clock to provide Manchester encoded data. The encoder provides the transition to idle for the TP drivers.

4.2.3 Oscillator Circuitry

The 21145 supports two options for generating internal 10 MHz clock required by the internal circuitry.

1. An external parallel resonant crystal connected between xtal1 and xtal2 to drive the 21145-integrated oscillator circuitry.
2. An external clock generator module connected to xtal1; xtal2 remains unconnected.

For circuitry characteristics, see the *21145 Phoneline/Ethernet LAN Controller Datasheet*.

4.2.4 Smart Squelch

The 21145 implements an intelligent squelch on its TP receiver to ensure that impulse noise detected on the receive inputs is not mistaken for valid signals. The squelch circuitry employs a combination of both amplitude and timing measurements to determine the validity of data received on the TP inputs.

The squelch circuit allows only valid differential receive data to pass through to the Manchester decoder provided that the following two conditions are satisfied:

1. The input amplitude is greater than the minimum signal threshold level.
2. A specific pulse sequence is received.

Satisfying these two conditions ensures that a good signal-to-noise ratio is maintained while the signal pair is active, and it prevents system noise from causing false squelch deactivation.

The line squelch quickly activates and deactivates within the specified time intervals, when the input squelch threshold is exceeded and a specific pulse sequence of proper polarity is detected.

The squelch circuitry rejects system noise by ignoring received pulses that are less than the required fixed time width. It also rejects pulses that are greater than the expected signal duration.

4.2.5 Autopolarity Detector

The autopolarity detector (CSR14<13>) provides a method of detecting receive wire polarity by switching the polarity of the data going into the MAC layer accordingly. To detect polarity, the 21145 uses the link test pulse and the end-of-frame delimiter in an algorithm integrated into the link integrity test, as specified in the IEEE 802.3 10BASE-T supplement.

4.2.6 10BASE-T Link Integrity Test

Before transmitting on an Ethernet CSMA/CD network, each device has to check the reliability of its receive lines. In the twisted-pair (TP) case, link pulses are sent every 8 ms to 24 ms at the interval between two transmissions.

The 21145 monitors the received link pulses and end-of-frame delimiters to be spaced and electrically shaped as specified in the IEEE 802.3 10BASE-T supplement. Accordingly, the 21145 implements the Link Integrity Test.

After a software or hardware reset, the 21145 wakes up in the link fail state. In this state, only link pulses are sent onto the transmit lines. Upon detection of the required line activity, and autonegotiation completion (if enabled), the 21145 enters the link pass state enabling the receive and transmit paths.

A broken or noisy wire can bring the 21145 back to the link fail state. It will then report the wire failure by generating a link fail interrupt to the host and will immediately stop the receive and transmit paths. These paths will not be enabled again until the Link Integrity Test ends successfully.

4.3 HomePNA Port

The HomePNA port interfaces the 21145’s IEEE 802.3 MAC to the 21145's integrated HomePNA PHY, providing CSMA/CD networking on residential telephone line media. For detailed information on HomePNA refer to the *Home Phoneline Networking Alliance PHY Specification* available from the Home Phoneline Network Alliance website *(*http://www.homepna.org/).

HomePNA PHY Functions:

- Includes Analog Front End to interface telephone line (via RJ11 jack); the integrated envelope detector may be bypassed to connect to an external one.
- Implements symbol decoding for incoming data using HomePNA modulation.
- Implements symbol encoding for outgoing data using HomePNA modulation.
- Strips off Ethernet MAC preamble and Start Frame Delimiter (SFD) and replaces them with HomePNA header on transmitted packets.

- Strips off the HomePNA header and replaces it with Ethernet MAC preamble and Start Frame Delimiter on received packets.
- Uses a modulation frequency of 7.5 MHz.
- Provides telephone line noise filtering.

Programmable Parameters:

- Provides PHY transmission power level control.
- Offers speed control (1 Mb/s or 0.7 Mb/s).
- Noise filtering.

In-Band Control Features:

- Provides receiver automatic adjustment to one of two speeds.
- Supports two transmit power levels and two transmit speeds remotely set by master HomePNA station.
- Supports the PCOM field.

4.4 Media Access Control Operation

The 21145 supports a full implementation of the MAC sublayer of IEEE 802.3. It can operate in half-duplex mode, full-duplex mode, and loopback mode.

All Ethernet MAC frame information in this section also applies to HomePNA, unless noted otherwise; note that there are no Link Pulses and no Full-Duplex Mode on the HomePNA medium.

4.4.1 MAC Frame Format

The 21145 handles IEEE 802.3 and Ethernet MAC frames. While operating in either the 100BASE-FX mode or 100BASE-TX mode, the 21145 encapsulates the frames it transmits according to the IEEE 802.3, clause 24. Receive frames are decapsulated according to the IEEE 802.3, clause 24.

While operating in HomePNA mode, the 21145 encapsulates transmitted frames and decapsulates received frames according to the *Home Phoneline Networking Alliance PHY Specification*.

4.4.1.1 Ethernet/IEEE 802.3 and HomePNA Frames

CSMA/CD is the generic name for the network type. A CSMA/CD frame has a minimum length of 64 bytes and a maximum length of 1518 bytes, exclusive of the preamble and the start frame delimiter.

A CSMA/CD frame consists of the following parts:

- Preamble
- Start frame delimiter (SFD)
- Two address fields
- Type or length field

- Data field
- Frame check sequence (CRC value)

In HomePNA, the preamble and SFD are as specified in the *Home Phoneline Networking Alliance PHY Specification.*

4.4.1.2 CSMA/CD Frame Format Description

Figure 4-1 shows the CSMA/CD frame format.

Figure 4-1. CSMDA/CD Frame Format

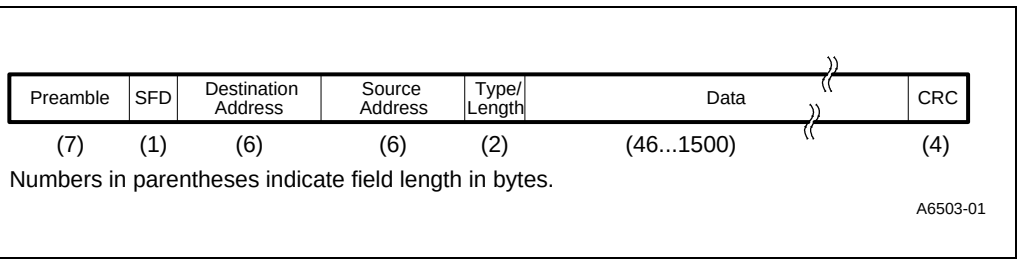


Table 4-2 describes the CSMA/CD frame format.

Table 4-2. CSMDA/CD Frame Format

Field	Description
Preamble	A 7-byte field of 56 alternating 1s and 0s, beginning with a 0.
SFD—Start frame delimiter	A 1-byte field that contains the value 10101011; the most significant bit is transmitted and received first.
Destination address	A 6-byte field that contains either a specific station address, the broadcast address, or a multicast (logical) address where this frame is directed.
Source address	A 6-byte field that contains the specific station address where this frame originated.
Type/length	A field value greater than 1500 is interpreted as an Ethernet type field, which defines the type of protocol of the frame. A field smaller than or equal to 1500 (05-DCH) is interpreted as an IEEE 802.3 length field, which indicates the number of data bytes in the frame.
Data	A data field consists of 46 bytes to 1500 bytes of information that is fully transparent because any arbitrary sequence of bits can occur. A data field shorter than 46 bytes, which is specified by the length field, is allowed. Unless padding is disabled (TDES1<23>), it is added by the 21145 when transmitting to fill the data field up to 46 bytes.
CRC	A frame check sequence is a 32-bit cyclic redundancy check (CRC) value that is computed as a function of the destination address field, source address field, type field, and data field. The FCS is appended to each transmitted frame, and is used at reception to determine if the received frame is valid.

Table 4-3 lists the possible values for the frame format. The values are expressed in hexadecimal notation and the 2-byte field is displayed with a hyphen separating the 2 bytes. The byte on the left of the hyphen is the most significant byte and is transmitted first.

Table 4-3. Frame Format Table

Frame Format	Length or Type	Hexadecimal Value
IEEE 802.3	Length field	00-00 to 05-DC
Ethernet	Type field	05-DD to FF-FF

The CRC polynomial, as specified in the Ethernet specification, is as follows:

$$FCS(X) = X^{31} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X^{1} + 1$$

The 32 bits of the CRC value are placed in the FCS field so that the X^{31} term is the right-most bit of the first octet, and the X^{0} term is the left-most bit of the last octet. The bits of the CRC are thus transmitted in the order X^{31}, X^{30}, ... , X^{1}, X^{0}.

4.4.2 MAC Reception Addressing

The 21145 can be set up to recognize any one of the MAC receive address groups described in Table 4-4. Each group is separate and distinct from the other groups.

Table 4-4. MAC Receive Address Groups (Sheet 1 of 2)

Group	Description
1	16-address perfect filtering The 21145 provides support for the perfect filtering of up to 16 Ethernet physical or multicast addresses. Any mix of addresses can be used for this perfect filter function of the 21145. The 16 addresses are issued in setup frames to the 21145.
2	One physical address, unlimited multicast addresses imperfect filtering The 21145 provides support for one, single physical address to be perfectly filtered with an unlimited number of multicast addresses to be imperfectly filtered. This case supports the needs of applications that require one, single physical address to be filtered as the station address, while enabling reception of more than 16 multicast addresses, without suffering the overhead of pass-all-multicast mode. The single physical address, for perfect filtering, and a 512-bit mask, for imperfect filtering using a hash algorithm, are issued in a setup frame to the 21145. When hash hits are detected, the 21145 delivers the received frame (Section 4.2.3). Note that imperfect filtering can only be used in the D0 power state.
3	Unlimited physical addresses, unlimited multicast addresses imperfect filtering The 21145 provides support for unlimited physical addresses to be imperfectly filtered with an unlimited number of multicast addresses to be imperfectly filtered as well. This case supports applications that require more than one physical address to be filtered as the station address, while enabling the reception of more than 16 multicast addresses, without suffering the overhead of pass-all-multicast mode. A 512-bit mask, for imperfect filtering using a hash algorithm, is issued in a setup frame to the 21145. When hash hits are detected, the 21145 delivers the received frame (Section 4.2.3). Note that imperfect filtering is only available in the D0 power state.

Table 4-4. MAC Receive Address Groups (Sheet 2 of 2)

Group	Description
4	Promiscuous Ethernet reception The 21145 provides support for reception of all frames on the network regardless of their destination. This function is controlled by a CSR bit. This group is typically used for network monitoring.
5	16-address perfect filtering and reception of all multicast Ethernet addresses This group augments the receive address Group 1 and also receives all frames on the Ethernet with a multicast address.
6	16-address inverse filtering In this mode, the 21145 applies the reverse filter of Group 1. The 21145 provides support for the rejection of up to 16 Ethernet physical or multicast addresses. Any mix of addresses may be used for this filter function of the 21145. The 16 addresses are issued in setup frames to the 21145. This mode can only be used in the D0 power state.

4.4.3 Detailed Transmit Operation

This section describes the transmit operation in detail, as supported by the 21145. This description includes the specific control register definitions, setup frame definitions, and a mechanism used by the host processor software to manipulate the transmit list (that is, the descriptors and buffers that can be found in Section 4.2).

4.4.3.1 Transmit Initiation

The host CPU initiates a transmit by storing the entire information content of the frame to be transmitted in one or more buffers in host memory. The host processor software prepares a companion transmit descriptor, also in host memory, for the transmit buffer and signals the 21145 to take it. After the 21145 has been notified of this transmit list, the 21145 starts to move the data bytes from the host memory to the internal transmit FIFO.

When the transmit FIFO is adequately filled to the programmed threshold level, or when there is a full frame buffered into the transmit FIFO, the 21145 begins to encapsulate the frame.

The threshold level can be programmed with various quantities (Table 8-61). The lower threshold is for low bus latency systems and the high threshold is for high bus latency systems.

The transmit encapsulation is performed by the transmit state machine, which delays the actual transmission of the data onto the network until the network has been idle for a minimum interpacket gap (IPG) time.

4.4.3.2 Frame Encapsulation

The transmit data frame encapsulation stream consists of appending the 56 preamble bits together with the SFD to the basic frame beginning and the FCS (for example, CRC), to the basic frame end.

The basic frame read from the host memory includes the destination address field, the source address field, the type/length field, and the data field. If the data field length is less than 46 bytes, and padding (TDES1<23>) is enabled, the 21145 pads the basic frame with the pattern 00 for up to 46 bytes before appending the FCS field to the end.

While operating either in 100BASE-FX mode or 100BASE-TX mode, the 21145 encapsulates the frames it transmits according to IEEE 802.3, clause 24 and the receive frames are decapsulated as defined in IEEE 802.3, clause 24.

The changes between a MAC frame (Section 4.4.1) and the encapsulation used when operating either in 100BASE-TX or 100BASE-FX modes are listed as follows:

1. The first byte of the preamble in the MAC frame is replaced with the JK symbol pair.
2. After the FCS byte of the MAC frame, the TR symbol pair is inserted.

4.4.3.3 Initial Deferral

The 21145 constantly monitors the line and can initiate a transmission any time the host CPU requests it. Actual transmission of the data onto the network occurs only if the network has been idle for a 96-bit time period, and any backoff time requirements have been satisfied.

The IPG time is divided into two parts: IPS1 and IPS2.

1. IPS1 time (60-bit times): the 21145 monitors the network for an idle state. If a carrier is sensed on the serial line during this time, the 21145 defers and waits until the line is idle again before restarting the IPS1 time count.
2. IPS2 time (36-bit times): the 21145 continues to count time even though a carrier has been sensed on the network, and thus forces collisions on the network. This enables all network stations to have access to the serial line.

4.4.3.4 Collision

A collision occurs when concurrent transmissions from two or more Ethernet nodes take place. When the 21145 detects a collision while transmitting, it halts the transmission of the data, and instead, transmits a jam pattern. At the end of the jam transmission, the 21145 begins the backoff wait period.

If the collision was detected during the preamble transmission, the jam pattern is transmitted after completing the preamble (if the 21145 is in 100BASE-FX or 100BASE-TX operating modes, this includes the JK symbol pair as described in Section 4.4.4.2.2). This action results in a minimum 96-bit fragment.

The 21145 scheduling of retransmission is determined by a controlled randomization process called truncated binary exponential backoff. The delay is an integer multiple of slot times. The number of slot times of delay before the *n*th retransmission attempt is chosen as a uniformly distributed random integer r in the range:

$0 \leq r < 2^k$

$k = \min(n, N)$ and $N = 10$

When 16 attempts have been made at transmission and all have been terminated by a collision, the 21145 sets an error status bit in the descriptor (TDES0<8>) and, if enabled, issues a normal transmit termination (CSR5<0>) interrupt to the host.

Note: The jam pattern is a fixed pattern that is not compared with the actual frame CRC. This has the very low probability (0.5^{32}) of having a jam pattern equal to the CRC.

4.4.3.5 Terminating Transmission

A specific frame transmission is terminated by any of the following conditions:

- Normal—The frame has been transmitted successfully. When the last byte is serialized, the pad and CRC are optionally appended and transmitted, thus concluding frame transmission.
- Underflow—Transmit data is not ready when needed for transmission. The underflow status bits (TDES0<1> and CSR5<5>) are set, and the packet is terminated on the network with a bad CRC.
- Excessive collisions—If a collision occurs for the 15th consecutive retransmission attempt of the same frame, TDES0<8> is set.
- Jabber timer expired—If the timer expires (TDES0<14> sets) while transmission continues, the programmed interval transmission is cut off.
- Memory error—This generic error indicates either a host bus timeout or a host memory error.
- Late collision—If a collision occurs after the collision window (transmitting at least 64 bytes), transmission is cut off and TDES0<9> sets.

At the completion of every frame transmission, status information about the frame is written into the transmit descriptor. Status information is written into CSR5 if an error occurs during the operation of the transmit machine itself. If a normal interrupt summary (CSR7<16>) is enabled, the 21145 issues a normal transmit termination interrupt (CSR5<0>) to the host.

4.4.3.6 Transmit Parameter Values

Table 4-5 lists the transmit parameter values for both the 10 Mb/s and 100 Mb/s serial bit rates.

Table 4-5. Transmit Parameter Values

Parameter	Condition	Value
Defer time	IPS1+IPS2=96-bit time period	—
IPS1	—	60-bit time period
IPS2	—	36-bit time period
Slot time interval	—	512-bit time period
Network acquisition time	—	512-bit time period
Transmission attempts	—	16
Backoff limit	—	10
Jabber timer	Default	16,000-bit to 20,000-bit time period
Jabber timer	Programmable range	26,000-bit to 32,000-bit time period

4.4.4 Detailed Receive Operation

This section describes the detailed receive operation as supported by the 21145. This description includes the specific control register definitions, setup frame definitions, and a mechanism used by the host processor software to manipulate the receive list (that is, the descriptors and buffers that can be found in Section 4.2).

4.4.4.1 Receive Initiation

The 21145 continuously monitors the network when reception is enabled. When activity is recognized, it starts to process the incoming data. After detecting receive activity on the line, the 21145 starts to process the preamble bytes based on the mode of operation.

4.4.4.2 Preamble Processing

Preamble processing varies depending on the 21145 operating mode. The next two subsections describe how this processing is handled.

4.4.4.2.1 MII/SYM and 10BASE-T Mode Preambles

In MII/SYM and 10BASE-T, the preamble, as defined by Ethernet, can be up to 64 bits (8 bytes) long.

The 21145 allows any arbitrary preamble length. However, depending on the mode, there is a minimum preamble length.

- In MII/SYM mode, at least 8 bits are required to recognize a preamble.
- In 10BASE-T, at least 16 bits are required to recognize a preamble.
- While in Snooze mode, at least 20 bits are required to recognize a preamble. This is true for MII/SYM and 10BASE-T. Some PHY devices do not provide 20 bits of preamble to the MAC, so if Snooze mode is to be used, it must be verified that the PHY device used provides at least 20 bits to the 21145.

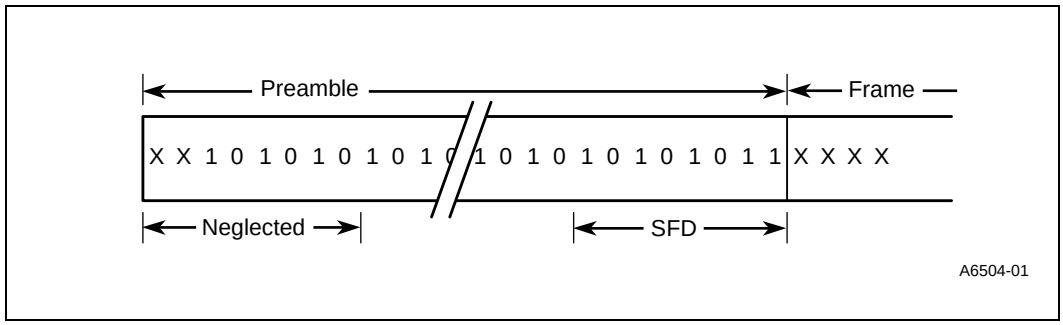
Recognition occurs as follows:

- In MII/SYM mode, the 21145 checks for the start frame delimiter (SFD) byte content of 10101011.
- In 10BASE-T:
  - The first 8 preamble bits are ignored.
  - The 21145 checks for the start frame delimiter (SFD) byte content of 10101011.

While checking for SFD, if the 21145 receives an 11b (before receiving 14 bits in 10BASE-T or 6 bits in MII/SYM mode) or a 00b (everywhere), the reception of the current frame is aborted. The frame is not received, and the 21145 waits until the network activity stops (Section 4.4.4.1) before monitoring the network activity for a new preamble.

Figure 4-2 shows the preamble recognition sequence bit fields.

Figure 4-2. Preamble Recognition Sequence in 10BASE-T



4.4.4.2.2 100BASE-TX or 100BASE-FX Mode Preambles

When operating in either 100BASE-TX or 100BASE-FX mode, the 21145 expects the frame to start with the symbol pair JK followed by the preamble, as specified in Section 4.4.4.2.1. If a JK symbol pair is not detected, the reception of the current frame is aborted (not received), and the 21145 waits until the network activity stops before monitoring the network activity for a new preamble.

4.4.4.3 Address Matching

Ethernet addresses consist of two 6-byte fields: one field for the destination address and one for the source address. The first bit of the destination address signifies whether it is a physical address or a multicast address as listed in Table 4-6.

Table 4-6. Destination Address Bit 1

Bit 1	Address
0	Station address (physical)
1	Multicast address

The 21145 filters the frame based on the Ethernet receive address group filtering mode that has been enabled (Section 4.4.2).

If the frame address passes the filter, the 21145 removes the preamble and delivers the frame to the host processor memory. If, however, the address does not pass the filter when the mismatch is recognized, the 21145 terminates its reception. In this case, no data is sent to the host memory nor is any receive buffer consumed.

If receive all (CSR6<30>) is set, the 21145 receives all incoming packets, regardless of the destination address. The address recognition status is posted in RDES0<30>.

4.4.4.4 Frame Decapsulation

The 21145 checks the CRC bytes of all received frames before releasing them to the host processor. When operating in either 100BASE-TX or 100BASE-FX mode, the 21145 also checks that the frame ends with the TR symbol pair; if not, the 21145 reports a CRC error in the packet reception status.

4.4.4.5 Terminating Reception

Reception of a specific frame is terminated when any of the following conditions occur:

- Normal termination—The network activity (Section 4.4.4.1) stops for the various operating modes.
- Overflow—The receive DMA cannot empty the receive FIFO into host processor memory as rapidly as it is filled, and an error occurs as frame data is lost.
- Watchdog timer expired—If the timer expires (CSR5<9> and RDES0<4> both set) while reception is still in process.
- Collision—If a late collision occurs after the reception of 64 bytes of the packet, the collision seen status bit RDES0<6> is set.

4.4.4.6 Frame Reception Status

When reception terminates, the 21145 determines the status of the received frame and loads it into the receive status word in the buffer descriptor. An interrupt is issued if enabled. The 21145 may report the following conditions at the end of frame reception:

- CRC error—The 32-bit CRC transmitted with the frame did not match the CRC calculated upon reception. The CRC check is always executed and is independent of any other errors. In addition, the 21145 reports a CRC error in any of the following cases:
  - — The mii_err signal asserts during frame reception over the MII when operating in one of the MII operating modes.
  - — The 21145 is operating in either the 100BASE-TX or 100BASE-FX mode and one of the following events occur:
    * An invalid symbol is received in the middle of the frame.
    * The frame does not end with the symbol T followed by the symbol R.
- Dribbling bits error—This indicates the frame did not end on a byte boundary. The 21145 signals a dribbling bits error only if the number of dribbling bits in the last byte is 4 in MII operating mode, or at least 3 in 10BASE-T serial operating mode. Only *whole bytes* are run through the CRC check. This means that although up to 7 dribbling bits may have occurred and a framing error was signaled, the frame might nevertheless have been received correctly. This condition must be ignored in HomePNA mode.
- Alignment error—A CRC error and a dribbling bit error occur together. This means that the frame did not contain an integral number of bytes and the CRC check failed.
- Frame too short (runt frame)—A frame containing less than 64 bytes was received (including CRC). Reception of runt frames is optionally selectable. The 21145 defaults to inhibit reception of runts.
- Frame too long—A frame containing more than 1518 bytes (including CRC) was received. Reception of frames too long completes with an error indication.
- Collision seen—A frame collision occurred after the 64 bytes following the Start Frame Delimiter (SFD) were received. Reception of such frames is completed and an error bit is set in the descriptor.
- Descriptor error—An error was found in one of the receive descriptors, which disabled the correct reception of an incoming frame.

4.5 Network Port Autosensing

The 21145 can sense the HomePNA and 10BASE-T ports at the same time. In addition, while the HomePNA port is used for transmission, it can also send the 10BASE-T link pulses onto the TP wires. These features, along with reported status bits and interrupts, together with indications taken from the MII/SYM PHY port, allow the driver to choose between the three ports for network connection without any network configuration information.

To implement the autosensing algorithm, the driver can use the following hardware support provided by the 21145 (a detailed description of these bits is provided in Chapter 8):

- Interrupts
  - — Link pass CSR5<4>
  - — Link fail CSR5<12>
  - — General Purpose Timer expired CSR5<11>
- CSRs
  - — Autosensing enable bit CSR14<15>
  - — Activity sensed on the HomePNA port CSR12<8>
  - — Activity sensed on the 10BASE-T port CSR12<9>
  - — Activity sensed on the MII port CSR12<0>
  - — General-purpose timer (CSR11)

Additional information about the MII port activity can be taken from the 100BASE-T PHY chip located on the board through the MII management port (mii_mdc and mii_mdio).

Selecting one of the network ports requires programming of CSR6, CSR13, CSR14, and CSR15. Table 8-89 and Table 8-90 provide the programming values for enabling autosensing. To change the selection, start by resetting the SIA using CSR13.

4.6 Loopback Operations

The 21145 supports two loopback modes: internal loopback and external loopback. Both internal and external loopback require external clock activity (mii_tclk in MII mode and xtal1 in 10BASE-T).

4.6.1 Internal Loopback Mode

Internal loopback mode is normally used to verify that the internal logic operations function correctly. Internal loopback mode is enabled according to CSR6<11:10>. Internal loopback mode includes all the internal functions. In loopback mode, the 21145 disengages from the Ethernet.

Internal loopback mode also supports the following modes of operation:

1. Media access control (MAC) internal loopback mode in which transmit packets are looped back at the MAC level and the 21145 disengages the SIA. The loopback data rate is 10 Mb/s, or 10/100 Mb/s in MII/SYM mode.
2. 10BASE-T internal loopback mode in which transmit packets from the encoder output are selected and looped back to the decoder input. The loopback data rate is 10 Mb/s.

4.6.2 External Loopback Mode

External loopback mode is normally used to verify that the logic operations up to the Ethernet cable function correctly. In external loopback mode, the 21145 takes frames from the transmit list and transmits them on the Ethernet wire. Concurrently, the 21145 listens to the line that carries its own transmissions and places incoming frames in the receive list.

Caution: In external loopback mode, when transmitted frames are placed on the Ethernet wire, the 21145 does not check the origin of any incoming frames. It is possible for frames not originating from the 21145 to enter the receive buffers.

Note: External loopback mode cannot be used on the HomePNA port.

External loopback mode also supports the following modes of operation:

- 10BASE-T external loopback mode transmits packets using twisted-pair wires. Concurrently, the 21145 disables the internal collision detector and thus listens to the line that carries its own transmission. The board designer must use an external shunt to connect the transmit line with the receive line.
- MII/SYM external loopback mode transmits packets using the MII/SYM interface to check the MII/SYM integrity.

4.6.3 Driver Entering Loopback Mode

To enter a specific loopback mode, the driver must take the following actions:

Note: All address filtering and validity checking rules apply in all loopback modes.

1. Stop the receive and transmit processes by writing 0 to both the start/stop receive (CSR6<1>) and the start/stop transmit (CSR6<13>) fields. The driver must wait for any previously scheduled frame activity to cease by polling the transmit process state (<22:20>) and the receive process state (<19:17>) fields in CSR5.
2. Prepare the appropriate transmit and receive descriptor lists in host memory. These lists can follow the existing lists at the point of suspension or be new lists identified to the 21145 by the receive list base address in CSR3 and by the transmit list address in CSR4.
3. Stop the SIA by setting CSR13 to a value of 00000000H.
4. In 10BASE-T/HomePNA mode, program CSR13, CSR14, and CSR15 to the desired SIA operation mode according to Table 8-86 toTable 8-90.
5. Wait at least 5 µs.
6. Select the desired loopback mode according to Table 8-86 to Table 8-90.
7. Use start commands to place both the transmit and receive processes into the running state.
8. As in normal processing, execute any 21145 interrupts.

4.6.4 Driver Restoring Normal Operation

To restore normal operation, the driver must execute the following procedure:

1. Stop both the receive and transmit processes. The driver must wait for any previously scheduled frame activity to cease by polling both the transmit (CSR5<22:20>) and receive process state (CSR5<19:17>) fields in CSR5.
2. Prepare appropriate transmit and receive descriptor lists in host memory. These lists can either follow the existing lists at the point of suspension or be new lists that have to be identified to the 21145 by the receive list base address in CSR3 and the transmit list base address in CSR4.
3. Stop the SIA by setting CSR13 to a value of 00000000H.
4. In 10BASE-T/HomePNA mode, program CSR13, CSR14, and CSR15 to the desired SIA operation mode according to Table 8-86 to Table 8-90.
5. Wait at least 5 µs.
6. Select normal mode operation according to Table 8-86 to Table 8-90.
7. Use start commands to place both the transmit and receive processes into the running state.
8. Resume normal processing. Execute any 21145 interrupts.

4.7 Full-Duplex Operation

The 21145 activates the transmit and receive processes simultaneously. It also supports receive back-to-back packets with an interpacket gap (IPG) of 96-bit times in parallel with transmit back-to-back packets with an IPG of 96-bit times.

The 21145 implements a programmable full-duplex operating mode (CSR6<9>) bit that commands the MAC to ignore both the carrier and the collision detect signal. In 10BASE-T mode, when the autonegotiation algorithm is used (CSR14<7>), the 21145 operates in full-duplex mode only if the negotiation results allow it. For additional information about programming full-duplex operation with autonegotiation, refer to Section 4.8.

The driver must take the following actions to enter full-duplex operation.

1. Stop the receive and transmit processes by writing 0 to CSR6<1> and CSR6<13> fields, respectively. The driver must wait for any previously scheduled frame activity to cease by polling the transmit process state (<22:20>) and receive process state (<19:17>) fields in CSR5.
2. Reset the SIA by writing 0 to CSR13.
3. Prepare appropriate transmit and receive descriptor lists in host memory. These lists can use the existing lists at the point of suspension, or can create new lists that must be identified to the 21145 by referencing the receive list base address in CSR3 and the transmit list base address in CSR4.
4. Set full-duplex mode (CSR6<9>).
5. In 10BASE-T mode set CSR13 through CSR15, using Table 8-100 as a reference.
6. In 10BASE-T mode, wait for the link pass interrupt.
7. Place the transmit and receive processes in the running state by using the start commands.
8. Resume normal processing. Execute any 21145 interrupts.

4.8 Autonegotiation

The IEEE 802.3 10BASE-T autonegotiation algorithm allows a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment. Similarly, a device can detect corresponding enhanced operation modes that the other device may be advertising. The algorithm builds upon the existing 10BASE-T link pulse scheme and is based on data exchange in the physical layer between two nodes.

The 21145 implements this algorithm for 10BASE-T and 100BASE-TX half-duplex and full-duplex mode autonegotiation and 100BASE-T4 mode autonegotiation. The whole negotiation is done by the 21145 without software involvement. At the end of the negotiation, the software should set the operating mode according to Table 4-7. The HomePNA medium does not support link pulses, therefore there is no Autonegotiation on the HomePNA port.

Table 4-7. Autonegotiation Modes Selection

CSR12<25:21>[1]	CSR14<18:16>[2]	CSR14<6>[2]	CSR6<9>[2]	Selected Mode
X1XXX[3]	X1X	X	X	100BASE-TX FD[4]
XX1XX	001	X	X	100BASE-TX HD[5]
001XX	XX1	X	X	100BASE-TX HD
XXX1X	000	X	1	10BASE-T FD
0001X	XXX	X	1	10BASE-T FD
XXXX1	000	1	0	10BASE-T HD
00001	XXX	1	X	10BASE-T HD
1XXXX	10X	X	X	T4
10XXX	1XX	X	X	T4
All other cases				No common mode

NOTES:
1. Link partner's link code word.
2. 21145 advertisement.
3. Binary representation.
4. Full-duplex.
5. Half-duplex

If the selected mode at the end of negotiation is 10BASE-T, the receive and transmit paths are only enabled if the link integrity test passed successfully within 1 second. Otherwise, the autonegotiation process automatically starts again.

If the selected mode at the end of negotiation is 100BASE-TX, the driver should configure the 21145 to select the MII/SYM port (for more information, see Table 8-96). The receive and transmit paths are only enabled if the 100BASE-TX link integrity test passed successfully within 1 second. Otherwise, the autonegotiation process starts again.

In addition, when there is no common mode of operation between the two link partners, the autonegotiation process automatically starts once again within 1 second after negotiation has completed.

To enable the autonegotiation mechanism, CSR14<7> (autonegotiation enable) must be set. Table 8-100 shows the programming of the SIA with autonegotiation enabled.

Before enabling its receive or transmit paths, or after the link integrity test has failed, the 21145 starts an autonegotiation sequence with its link partner. The 21145 stops sending its link pulses for at least 1 second and moves its link partner into the link fail state, forcing it to renegotiate.

An autonegotiation completed interrupt, together with CSR12<14:12> read as 101, indicates the end of the negotiation. The driver then reads CSR12 to get the link test status, and the driver also has the ability to restart the negotiation by setting the CSR12<14:12> field to a value of 001.

4.9 Capture Effect–A Value-Added Feature

As a value-added feature, the 21145 provides a complete solution to an Ethernet and IEEE 802.3 problem referred to as capture effect. This solution is not part of the IEEE 802.3 standard. A device implementing this feature deviates from the IEEE 802.3 standard backoff algorithm. Therefore, this feature is optional and can be enabled or disabled using the CSR6<17> control bit.

4.9.1 What Is Capture Effect?

Consider two stations on the line, station A and station B. Each station has a significant amount of data ready to transmit. Each station is able to satisfy the minimum IPG rules (both from transmit-to-transmit and from receive-to-transmit operations). Table 4-8 shows the capture-effect sequence. The following steps show how station A captures the line:

1. Station A (with data A1) and station B (with data B1) both attempt to transmit simultaneously within a slot time of 51.2 µs. Each station has an initial collision count set to 0.
2. The stations experience a collision. Both stations increment their collision count to 1.
3. Each station picks a backoff time value that is uniformly distributed from 0 to (2*n*)–1 slots. In this example, station B selects a backoff of 1 (a 50% probability), and station A selects a backoff of 0.
4. Station A successfully transmits its A1 data packet. Station B waits for data A1 to be transmitted before attempting to retransmit data B1.
5. Collision count at station B remains at 1, while collision count at station A is reset to 0.
6. If station A has another packet (data A2) ready to transmit while station B still wants to transmit its packet (data B1), the stations both contend for the line again.
7. If these stations collide, the backoff value available for station A is 0 or 1 slots. The backoff value available for station B is 0, 1, 2, or 3 slots because the collision count is now at 2 (station A's collision count is at 1). Station A is more likely to succeed and transmit data A2, while data B1 from station B begins the deferral of completing its backoff interval.
8. It is possible, with this type of behavior between stations, that in the 2-node Ethernet, a station can capture the channel for an unfair amount of time. One station can transmit a significant number of packets back to back, while the other station continues to backoff further and further.
9. This process could continue until station B reaches the maximum number of collisions, 16, while attempting to transmit data B1. At this time, station B would abort data B1. If station B had another packet (data B2), station B would access the line and transmit data B2.

Note: If station A completes the transmitting of a stream of packets during this type of capture, and station B is still in backoff, potentially for a long time, the line is idle for this period of time.

Table 4-8. Capture-Effect Sequence

Station A	Line	Station B	Collision A	Count B
Transmit packet A1	Collision	Transmit packet B1	0	0
Backoff 0, 1	—	Backoff 0, 1	1	1
Transmit packet A1	Packet A1	Backoff	0	1
Transmit packet A2	Collision	Transmit packet B1	0	1
Backoff 0, 1	—	Backoff 0, 1, 2, 3	1	2
Transmit packet A2	Packet A2	Backoff	0	2
Transmit packet A3	Collision	Transmit packet B1	0	2
Backoff 0, 1	—	Backoff 0, 1, 2, ... 7	1	3

4.9.2 Resolving Capture Effect

The 21145 generally resolves the capture effect by having the station use, after a successful transmission of a frame by a station, a 2–0 backoff algorithm on the next transmit frame. If the station senses a frame on the network before it attempts to transmit the next frame, regardless of whether the sensed frame destination address matches the station's source address, the station returns to use the standard truncated binary exponential backoff algorithm (Section 4.4.3.4).

When the station executes the 2–0 backoff algorithm, it always waits for a 2-slot period on the first collision, and for a 0-slot period on the second collision. For retransmission attempts greater than 2, it uses the standard truncated, binary exponential backoff algorithm.

Table 4-9 summarizes the 2–0 backoff algorithm.

Table 4-9. 2–0 Backoff Algorithm

Retransmission Attempts	Backoff Period (Number of Slot Times)
$n = 1$	Backoff = 2 slots
$n = 2$	Backoff = 0 slots
$n = 3$ to 15	Backoff = $0 \leq r < 2^k$ (k = min(n, N) and N = 10) (r = uniformly distributed random integer)

4.9.3 Enhanced Resolution for Capture Effect

The 21145 offers an enhanced resolution for capture effect. The enhancement is made by incorporating a stopped backoff algorithm (with the 2–0 backoff algorithm) to reduce collision while maintaining the key properties of the 2–0 backoff algorithm.

When the enhanced resolution for the capture effect bit is set (CSR6<31>), the 21145 activates the stopped backoff algorithm as follows: in a back-to-back transmit, while in backoff after the first collision (n=1, where n is the retransmission attempts), the 21145 stops its backoff timer for the duration when the channel is busy. It continues its backoff timer when the channel is idle. For any other collision cases, the backoff timer is not stopped.

4.10 Jabber and Watchdog Timers

The jabber timer monitors the time of each packet transmission. The watchdog timer monitors the time of each packet reception. If a single packet transmission or reception exceeds a programmable value (Section 8.3.2.18), the jabber and watchdog circuitry automatically disables both the transmit and receive path. The transmit jabber timer provides the jabber function by cutting off transmission and asserting the collision signal to the MAC.

The packet descriptor closes with both transmit jabber timeout (TDES0<14>) and late collision (TDES0<9>) setting if the jabber timer expires on a transmit packet.

The receive watchdog provides the watchdog function by cutting off reception. The packet descriptor closes with the receive watchdog bit (RDES0<4>) set.

The watchdog timer must not be used in HomePNA mode.

Modem Interface 5

5.1 PCI/CardBus Function for Modem and Modem Interface

The 21145 (176-pin device only) provides an interface to ISA compliant modem chipsets. This allows byte read and write operations to the modem's internal registers via PCI accesses. The 21145 implements a PCI/CardBus modem function, separate from the Ethernet function. It serves as a bridge from PCI to ISA, enabling a connection for a non-PCI/CardBus modem chipset to a PCI/CardBus system, using the 21145's PCI/CardBus interface. For the modem PCI/CardBus function, the 21145 implements the PCI/CardBus configuration registers (including the PCI/CardBus power management interface), and the CardBus Status Changed registers. The modem function is enabled when Func1_HwOptions<0> bit in the serial ROM is set. When this bit is clear, the modem function is disabled.

The modem interface and PCI function support:

- Byte access to the modem's internal registers
- I/O or memory mapped registers
- Modem-generated interrupts
- Wakeup on modem ring
- ACPI/OnNow power management

The modem interface consists of the pins listed and described in Table 5-1:

Table 5-1. Modem Interface Pins (Sheet 1 of 2)

Signal	Type	Description
mdm_a<4:0>	O	Modem address lines. Address lines that are not needed in order to access the modem should be left unconnected. For example, if the modem chipset has only 8 registers, mdm_a<4:3> should be left unconnected.
mdm_chip_sel	O	Modem chip select. This pin is active low.
mdm_wr	I/O	When accessing the modem chipset (mdm_chip_sel is asserted), this pin is used as the modem write line and is active low.
mdm_rd	O	When accessing the modem chipset (mdm_chip_sel is asserted), this pin is used as the modem read line and is active low.
mdm<7:0>	I/O	When accessing the modem chipset (mdm_chip_sel is asserted), these pins are used as the modem data lines bits 7 through 0.
mdm_int	I	Modem interrupt line. When asserted, the 21145 asserts the int_l pin. This pin is active high. It must be connected to a pull-down resistor.
mdm_pwr_down	O	Modem power down. This pin is asserted when the modem function is in D3 power state. It is intended to control the modem chipset's power management. The polarity of this pin is determined by the Func1_HwOptions<5> bit in the serial ROM.

Table 5-1. Modem Interface Pins (Sheet 2 of 2)

Signal	Type	Description
mdm_ring_ind	I	Modem ring indicator. The assertion of this pin affects the assertion of the wake pin. The polarity of this pin is determined by the Func1_HwOptions<4> bit in the serial ROM. This pin must not be left floating.
mdm_rst	O	Modem reset. This pin is asserted for at least 15 µs upon hardware reset (rst_l pin asserted) and when the modem function moves from D3 to the D0 power state.
mdm_spkr_en	O	Modem speaker enable. This pin reflects the Audio enable bits of the modem function Status Changed registers. If the Func1_HwOptions<7> bit in the serial ROM is set, the value of the FEMR<6> is driven on the MDM_SPKR_EN pin. If the Func1_HwOptions<7> is cleared, the value of FEMR<5> is driven on the MDM_SPKR_EN pin.

During PCI/CardBus access to the modem, the 21145 operates as a bus slave. The modem may be accessed only by byte access, reading or writing one byte at a time. Only one bit in c_be_l<3:0> may be asserted during a given access. A PCI/CardBus access to the modem causes the 21145 to issue a read/write access to the modem chipset.

5.2 Modem Write Access

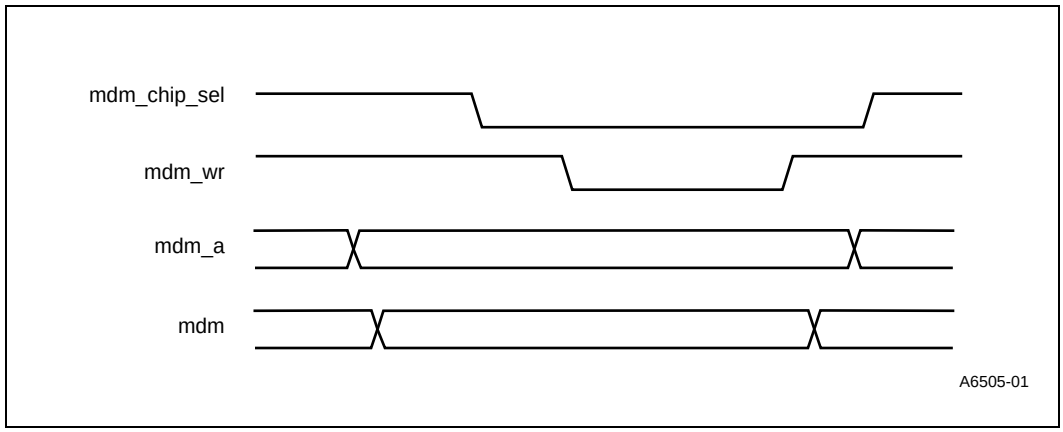
A write access to the modem chipset is executed as follows:

1. The host initiates a write cycle on the PCI/CardBus bus and writes the data to the 21145.
2. The 21145 drives the address on the mdm_a<4:0> lines.
3. The 21145 drives the data on the mdm<7:0> lines.
4. The 21145 asserts the mdm_chip_sel line.
5. The 21145 asserts the mdm_wr line.
6. The 21145 deasserts the mdm_wr line.
7. The 21145 deasserts the mdm_chip_sel line.

Note: There must be a delay of at least 20 PCI cycles between any write to a modem register, and a write to CSR9.

Figure 5-1 shows a write access to the modem chipset.

Figure 5-1. Write Access Timing



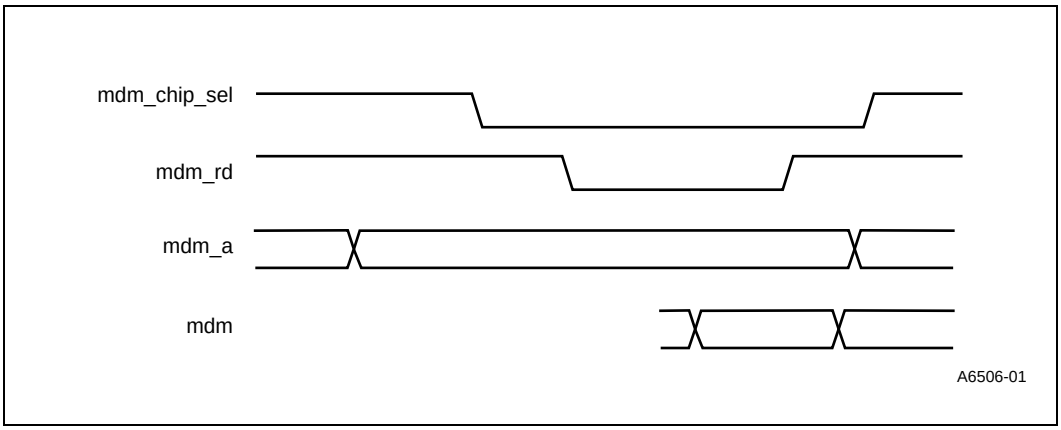
5.3 Modem Read Access

A read access to the modem chipset is executed as follows:

1. The host initiates a read cycle on the PCI/CardBus bus.
2. The 21145 drives the address on the mdm_a<4:0> lines.
3. The 21145 asserts the mdm_chip_sel line.
4. The 21145 asserts the mdm_rd line.
5. The modem chipset drives the data on the mdm<7:0>.
6. The 21145 samples the data on the mdm<7:0> lines.
7. The 21145 deasserts the mdm_rd line.
8. The 21145 deasserts the mdm_chip_sel line.
9. The 21145 drives the data on the mdm lines.

While the 21145 waits for the data to be driven on mdm<7:0> lines by the modem chipset, it inserts wait states on the PCI/CardBus bus. Figure 5-2 shows a read access to the modem chipset.

Figure 5-2. Read Access Timing



Power-Management and Power-Saving Support 6

This chapter provides an overview of the various power-management specifications and describes the power-management mechanisms supported by the 21145. This chapter also describes the various power-saving modes of the 21145. Throughout this document, the term *power management* is used for mechanisms to control the entire system's power state, while the term *power saving* is used for mechanisms to control the power consumption of the 21145 device itself.

6.1 Overview

The 21145 supports a power management mechanism based upon the OnNow initiative and the ACPI specification, for both the Ethernet function and the Modem function (176-pin device only). The 21145 is fully compliant with the *Network Device Class Specifications* Revision 1.0 and the *Communication Device Class Power Management Specification,* under the OnNow Architecture for Microsoft's *PC 97 Design Guide, PC98 Design Guide,* and the *PC99 Design Guide*. The 21145 supports all the network device class and communication requirements of the *PC97 Design Guide*, *PC 98 Design Guide* and the *PC 99 Design Guide.*

Fully compliant wit the *PCI Bus Power Management Interface Specification* Revision 1.0, and the *Advanced Configuration and Power Interface* (*ACPI) Specification Revision 1.0.*

In addition to the power-management support, the 21145 provides two power-saving modes: sleep mode and snooze mode. In sleep mode, the 21145 consumes minimal power, but most of its functions are not operating. Snooze mode is a dynamic mode in which the device consumes minimal power while in an idle state, and more power when it is active. The 21145 also supports the PCI/CardBus clkrun mechanism for power savings.

6.2 OnNow and ACPI Power-Management Mechanism

This section describes the specifications supported by the OnNow initiative and the ACPI specification.

6.2.1 Advanced Configuration and Power Interface (ACPI) Specification

The ACPI specification defines a flexible and abstract hardware interface that enables a wide variety of PC systems to implement power-management and thermal-management functions.

The ACPI specification defines power states for each component of the system (system, buses, devices, and so on).

6.2.1.1 PCI Power Management

The *PCI Power Management Interface* specification is a part of the ACPI Specification. This specification defines the behavior and requirements of the PCI bus and each PCI device when put in one of the power-management states defined by the ACPI specification.

Table 6-1 defines each of the power states for a PCI function:

Table 6-1. Power State Definitions

State	Definition
D0 - Fully On	This state is assumed to be the highest level of power consumption. In this state, the device is completely active and responsive, and is expected to remember all preserved context continuously.
D1	This state operates as a light sleep state. In this state, the PCI clock is running.
D2	This state operates as a deeper sleep state than the D1 state. In this state, the PCI clock can be stopped.
$D3_{hot}$	In this state, system power is supplied to the device, but the PCI clock can be stopped. The only context a PCI function in this state should maintain is the power management event (PME) context.
$D3_{cold}$	In this state, system power is removed from the device. The device context is lost. Functions that support power management events in the $D3_{cold}$ state must preserve their PME context when transitioning from the $D3_{cold}$ to the D0 state. Such functions require an auxiliary power source other than the normal Vcc power plane.

The *PCI Bus Power Management Interface Specification* defines how the power-management (wake-up) events are reported by a PCI function. It defines a new power management register block in the PCI configuration space and a new active-low PCI pin (PME#) to notify the system of a power management event. These registers are used by the software to put the device in a power state, and by the PCI function to report the power-management events.

6.2.2 Network and Communication Device Class Power Management Specification

OnNow is a term for a PC that is always powered-up, that appears off, but is capable of responding to users or other requests. OnNow defines the power-management requirements for each device class. The *Network Device Class Power Management Specification* defines the power-management requirements of a network device. The *Communication Device Class Power Management Specification* defines the power-management requirements of a communication device and specifically of a modem device.

The *Network Device Class Power Management Specification* defines the following wake-up events:

- Detection of change in the network link state
- Reception of a network wake-up frame
- Reception of a Magic Packet

A network wake-up frame is typically a frame that is sent by existing network protocols, such as ARP requests or IP frames addressed to the machine. Before putting the network adapter into the wake-up state, the system passes to the adapter's driver a list of sample frames and corresponding byte masks. Each sample frame is a template the 21145 will use to perform frame filtering to wake up the system via the gep2/pme/cstschg pin. Each byte mask defines which bytes of the incoming frames should be compared with the corresponding sample frame in order to determine whether or not to accept an incoming frame as a wake-up event.

The *Communication Device Class Power Management Specification* defines the wake-up event for a modem device, which is the phone ring indication.

6.2.3 The 21145 Support for OnNow and ACPI

The 21145 supports all three wake-up events defined in the *Network Device Class Power Management Specification* and the wake-up event defined by the *Communication Device Class Power Management Specification*.

Upon a wake-up event, the 21145 asserts its gep<2>/rcv_match/wake pin if either CPMC<8> or FEMR<4> of the function (Ethernet or Modem) that identified the wake-up event is set. Func0_HwOptions<9> bit in the serial ROM defines the polarity of the gep<2>/rcv_match/wake pin.

For each of the functions, the 21145 implements the new power-management register block within the PCI configuration registers as defined by the *PCI Bus Power Management Interface Specification*. This block contains the power-management capabilities of the function and the power-management control and status. For the register block definitions, see Chapter 8.

6.2.3.1 Ethernet Function Power Management

When the 21145 Ethernet function is put in the D1, D2, or D3 power state, it reads the Magic block information from the serial ROM. The Magic block contains information regarding the Magic Packet IEEE address, password, and the network ports that are connected to the 21145. The 21145 uses the information read from the serial ROM only if the CRC is valid. If the 21145 Ethernet function is put in the present power state when the link is down, or if the link fails while the 21145 Ethernet function is already in the D1, D2, or D3 power states, the 21145 starts autosensing and autonegotiations according to the algorithm below. The 21145 Ethernet function can be instructed to generate a wake-up event upon changes in the link status according to Table 6-2. When the link is valid, the 21145 Ethernet function can be instructed to generate wake-up events upon reception of a Magic Packet or a wake-up frame, according to Table 6-2.

Network Link Establishment Algorithm for Low Power States

1. Read serial ROM.
2. If selected port is 10-BASE-T and there is a link, or Symbol port and there is a symbol link, link is already established.
3. Otherwise, look for a link in following order:
   a. If Serial ROM defines an MII port and there is an MII link, then select MII port.
   b. If Serial ROM defines HomePNA port and there is no symbol port nor TP port defined, then select HomePNA port.
   c. Otherwise select HomePNA port and start autonegotiation.
4. Once a link is found using autonegotiation, select port with link.

Virtually-Connected Network Packet Filters

In order to stay “virtually connected” to the network while in low-power state, the 21145 monitors the network and wakes the system up on certain protocol-specific frames. The wake-up patterns are provided by software before the 21145 Ethernet function is put in low-power state.

The 21145 wake-up filter supports four programmable filters that allow support of many different receive packet patterns. Specifically, these filters allow support of both IP and IPX protocols, currently the only two protocols targeted to be power manageable. Each filter relates to 31 contiguous bytes in the wake-up frames.

When a frame is received from the network, the 21145 examines its content to determine whether the pattern matches to a wake-up frame. The 21145 first checks the frame’s destination address. Only frames that passed the 21145 perfect address filtering, and that are legal-sized Ethernet frames, can be accepted as wake-up frames. Each of the four pattern filters can be applied to either unicast frames or multicast frames. To know which bytes of the frame should be checked, in addition to the frame’s destination address, the 21145 uses a programmable byte mask and a programmable pattern offset for each of the four supported filters. The pattern's offset defines the location of the first byte that should be checked in the frame. Since the destination address is checked by the 21145 address filtering, the pattern offset is always greater than 12. The byte mask is a 31-bit field that specifies for each of the 31 contiguous bytes with the frame, beginning in the pattern offset, whether or not it should be checked. If bit *j* in the byte mask is set, byte *offset* + *j* in the frame is checked.

The 21145 implements imperfect pattern matching by calculating a CRC-16 on all bytes of the received frames that were specified by the pattern’s offset and the byte mask and comparing it to a programmable precalculated CRC value. The CRC calculation uses the following polynomial:

$$G(x) = x^{16} + x^{15} + x^2 + 1$$

To support wake-up patterns longer than 31 contiguous bytes, or to increase the selectivity of the filter, the 21145 provides the add-previous command. When the add-previous bit is set, the 21145 performs a logical AND between the current entry matching signal and the matching signal of the previous filter entry (including if the previous filter entry was disabled).

The 21145 also implements a global unicast (CSR2-PM<9>) filter. All unicast frames that pass the 21145 address filtering are identified as wake-up frames by the global unicast filter. The global unicast filter functions as the first filter for the add-previous command. If the add-previous command for filter 0 is set, the 21145 performs a logical *AND* between the global unicast matching signal and the filter 0 matching signal.

The 21145 also supports an inverse-mode command. When the inverse-mode bit is set, the 21145 uses its matching signal as a rejection signal, meaning that if a frame does not match this pattern, a wake-up event is generated. In the opposite case, if a frame does match the pattern, a wake-up event is not generated.

Note: Since the 21145 implements imperfect filtering, a CRC value can be matched by more than one pattern. Thus, the inverse-mode command should be used carefully in order to prevent situations in which the group of patterns matched by the CRC contains frames that should also wake up the system.

The 21145 filter includes support for VLAN frames. A VLAN frame is identified if the type field has the VLAN type value. A VLAN frame is identical to a non-VLAN frame, except for the 4-byte VLAN header inserted between the source address field and the length/type field. If the 21145 has identified an incoming frame as a VLAN frame, it ignores the VLAN header by automatically incrementing the filter’s pattern offset by four bytes for this frame.

The pattern matching parameters including the VLAN parameters can be programmed by writing to CSR1-PM and CSR2-PM.

Table 6-2 shows the power-management event capabilities of the 21145 Ethernet function.

Table 6-2. Ethernet Function Power Management Event Capabilities

Power State	Link Changed	Magic Packet	Wake-up Frame
D0[1]	—	—	—
D1	Yes	Yes	Yes
D2	Yes	Yes	Yes
D3	Yes[2]	Yes	Yes
Write access rules	—	—	—

1. Link changes in the D0 power state are indicated by the software. Magic Packets and wake-up frames are not applicable in the D0 power state.
2. In the D3 state, only link-pass will cause the 21145 to generate a wake-up event.

6.2.3.2 Ethernet Function Software Procedure for Power State Transitions

Table 6-3 describes the operations expected from the 21145 Ethernet driver when the 21145 Ethernet function is switched between power states.

In the D1, D2 and D3 states the 21145 may be programmed to generate a power management event on link changes. If the ability to automatically change between network ports while in the low-power states is desired, and both the HomePNA port and the internal 10BASE-T port are used, then autonegotiation must be enabled (via CSR14<7>) prior to placing the device in a low-power state. Otherwise, the device may report a false PME, possibly waking up the system, immediately after being placed in the low-power state.

Table 6-3. Driver Procedure Upon Moving Between Power States (Sheet 1 of 2)

From State...	To State...	Procedure
D0	D1/D2/D3	1. If the address filtering required for wake-up frames is different from what is required in D0, load the 21145 address recognition RAM with the wake-up pattern's address. 2. Stop the receive and transmit processes by writing to CSR6. 3. Verify that the receive and transmit processes have stopped by polling CSR5. 4. If the selected port is HomePNA, set the enable link integrity test bit (CSR14<12>) if it has not already been set. 5. If the MII management clock bit (CSR9<16>) is set, clear this bit. 6. Set the Enable OnNow Registers bit in CSR0. 7. Load the wake-up frame filter register block by writing to CSR1-PM. 8. Program the requested wake-up events and VLAN parameters and clear the wake-up events bits by writing to CSR2-PM. 9. Clear the Enable OnNow Registers bit in CSR0. The 21145 Ethernet function is now ready to be put in the new power state.

Table 6-3. Driver Procedure Upon Moving Between Power States (Sheet 2 of 2)

From State...	To State...	Procedure
D1/D2	D0	After the 21145 Ethernet function is put in D0, the software has to: 1. Reload the 21145 address recognition RAM if the address filtering requirements in D0 are different from what is required for wake-up frames. 2. Wait 1ms. 3. Start the receive and transmit processes by writing to CSR6. 4. In HomePNA mode, wait an additional 200 ms before attempting transmission.
D3	D0	After the 21145 Ethernet function is put in D0, the software has to:[1] 1. Reinitialize the 21145 including media sensing. 2. Wait 1ms 3. Start the receive and transmit processes by writing to CSR6. 4. In HomePNA mode, wait an additional 200 ms before attempting transmission.

1. The device experiences a hardware reset upon this transition.

6.2.3.3 Modem Function Power Management

The modem function supports the D0, D2, and D3 power states, as defined in the *Communication Device Class Power Management Specification.* For the modem function, the 21145 uses the modem chipset phone ring indication as a wake-up event. This is supported in the D2 and D3 power states.

6.3 Power-Saving Modes

The 21145 incorporates two different power-saving modes: sleep mode and snooze mode. Setting the Func0_HwOptions<4> (EnableCLKRUN) bit in the serial ROM provides further reduction in power consumption in the sleep and snooze modes. The following subsections describe these power-saving modes.

6.3.1 Sleep Mode

Sleep mode can be activated when the 21145 is not being used (for example, not connected to the network) and it is important to reduce its power dissipation. While in sleep mode, most of the internal logic is disabled. This includes the DMA machine, FIFOs, RxM, TxM, SIA, twisted-pair interface, HomePNA interface, and the general-purpose timer. The PCI section is not affected and access to the 21145 configuration registers remains possible. Access to the 21145 CSRs is not allowed.

To enter sleep mode, the driver must take the following actions:

1. Stop the receive and transmit processes by writing 0 to the CSR6<1> and CSR6<13> fields, respectively. The driver must wait for any previously scheduled frame activity to cease. This is done by polling the transmit process state (CSR5<22:20>) and the receive process state (CSR5<19:17>).
2. In 10BASE-T or HomePNA mode, reset the SIA by writing 0 to CSR13<0>.
3. Set the CFDD<31> bit.

To exit sleep mode, the driver must take the following actions:

1. Clear the CFDD<31> bit.
2. Wait 10 ms.
3. In 10BASE-T or HomePNA mode, start the SIA by writing 1 to CSR13<0>.
4. Wait at least 5 µs.
5. Start the receive and transmit processes by writing 1 to the CSR6<1> and CSR6<13> fields, respectively.

The 21145 powers up in sleep mode. Sleep mode must be exited before initialization of the 21145.

6.3.2 Snooze Mode

Snooze mode is a dynamic power-saving mode. When the snooze mode bit (CFDD<30>) is set, the 21145 reduces its power dissipation unless one or more of the following conditions is true:

- PCI slave or master access is conducted.
- Transmit process is in the running state.
- Receive process is in the running state but not waiting for a packet.
- Receive FIFO is not empty.
- MAC receive engine is not idle.
- Carrier is sensed.
- General-purpose port interrupt occurred.
- Link pass or link fail occurred.
- Receive interrupt is pending for timer expiration in the interrupt mitigation mechanism.
- Modem interrupt is pending (176-pin device only).
- The mdm_rst pin is asserted (176-pin device only).

When none of these conditions is true, the 21145 disables all its internal logic except for the PCI interface (not including the Manchester decoder that uses the 100-MHz phases). The device automatically and immediately reenables all its logic when at least one of the following occurs:

- PCI slave access is conducted.
- General-purpose port interrupt occurred.
- Carrier is sensed.
- Link pass or link fail occurred.
- Modem interrupt is pending (176-pin device only).

This results in the 21145 dynamically getting into and out of low-power mode, and overall power dissipation is reduced.

Note: The general-purpose timer and the automatic poll demand functions cannot be used in snooze mode.

6.4 Power-Management and Power-Saving Modes

The power-management and power-saving features of the 21145 are two independent mechanisms that can operate simultaneously. For example, the 21145 can be programmed to operate in the snooze power-saving mode and still operate in an OnNow power-management machine that generates wake-up events. Intel recommends putting the 21145 in the sleep power-saving mode when the 21145 is not expected to be used (for example, no packets are expected to be received or transmitted from the Ethernet or the modem).

To reduce power consumption, when the 21145 is expected to operate, Intel recommends putting the 21145 into the snooze power-saving mode. For a further reduction in power consumption, while the 21145 is in the sleep or the snooze power-saving mode, Intel recommends setting the Func0_HwOptions<4> (EnableCLKRUN) bit in the serial ROM.

External Ports 7

This chapter describes the interface and operation of the expansion ROM, the MicroWire serial ROM, the general-purpose port, and the network activity LEDs. This chapter also describes how to connect an external register to the expansion ROM port.

7.1 Overview

The 21145 (176-pin device only) provides an expansion ROM interface that may be optionally used on the adapter. The expansion ROM may contain code that can be executed for device-specific initialization and, possibly, a system boot function. During machine boot, the BIOS looks for bootable devices by searching a specific signature (55AA). Once found, the BIOS copies the code from the boot ROM to a shadow RAM in the host memory and executes the code from the RAM. Refer to *PCI BIOS Specification*, Revision 2.1.

The expansion ROM interface supports:

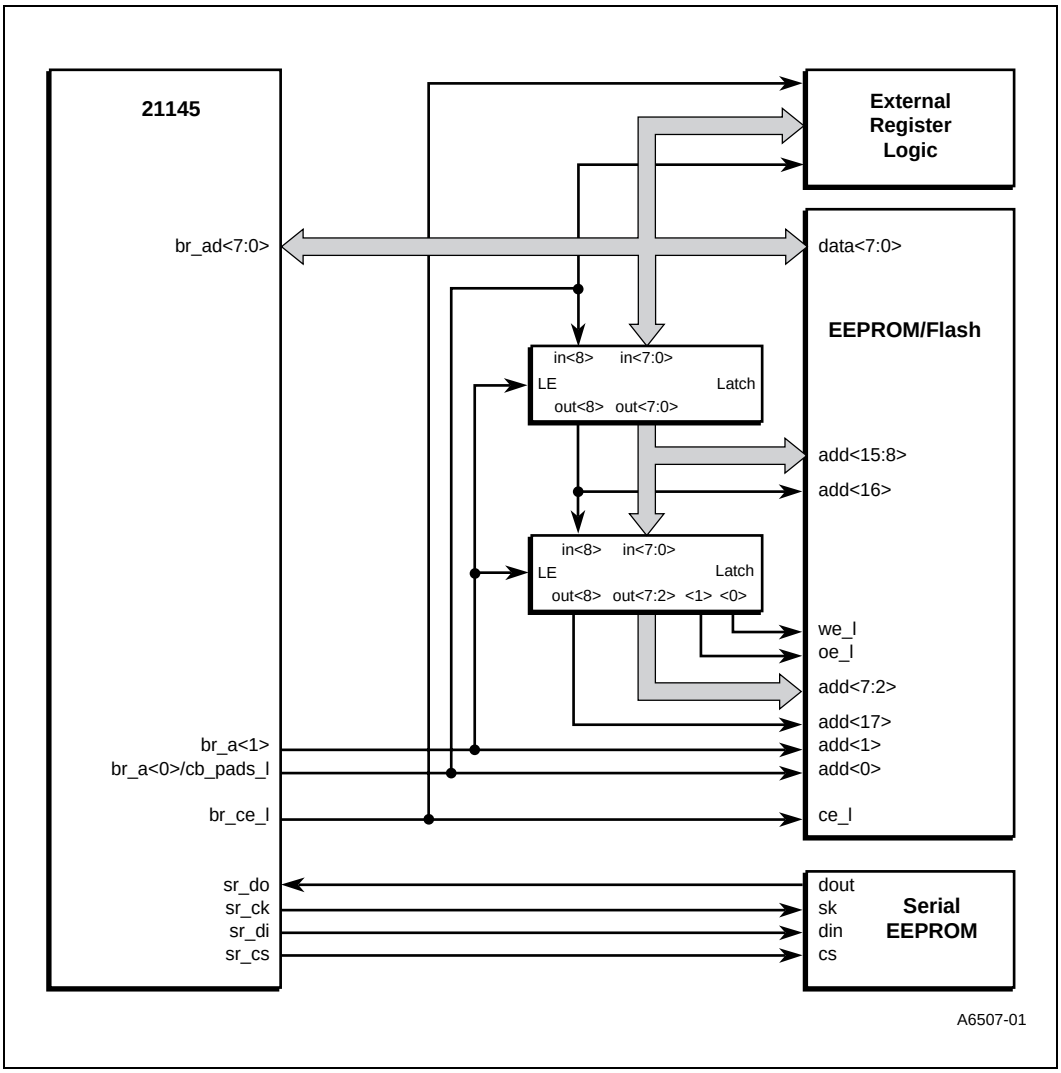
- 5 V or 12 V flash memory for code upgrade
- 240 ns EEPROM or faster
- Up to 256 KB address space

The 21145 provides a software-controlled, serial port interface suitable for MicroWire and other common serial ROM devices. The serial ROM contains the IEEE address and, optionally, other system parameters.

7.2 Expansion ROM and Serial ROM Connection

Figure 7-1 shows the connection of a 256 KB expansion ROM and the serial ROM. The two 9-bit edge trigger latches are used to latch the expansion ROM addresses <17:2> and the oe_l and we_l control signals.

Figure 7-1. Expansion ROM, Serial ROM, and External Register Connection



7.2.1 Expansion ROM Size

The 21145 supports several expansion ROM sizes. The size is specified in the Func0_HwOptions<1:0> field in the Serial ROM, as listed in Table 7-1.

Table 7-1. Expansion ROM Size

Size	Func0_HwOptions<1:0>
4 Kbyte	11
16 Kbyte	10
64 Kbyte	01
256 KByte	00

The 21145 divides the expansion ROM by two, and uses the first half of the expansion ROM for the Ethernet function and the second half for the modem function.

7.3 Expansion ROM Operations

Access to the Expansion ROM is done in two ways:

- Byte access (read/write) by using CSR9 and CSR10 (for manufacturing purposes).
- Dword (32-bit) read access from the PCI expansion ROM address space.

The following sections describe these accesses when two latches are connected to the expansion ROM. For each access, the expansion ROM must be set to the desired mode (read or write) prior to the actual access for the read or write transaction. For additional information about how this is done, refer to the specific ROM device documentation.

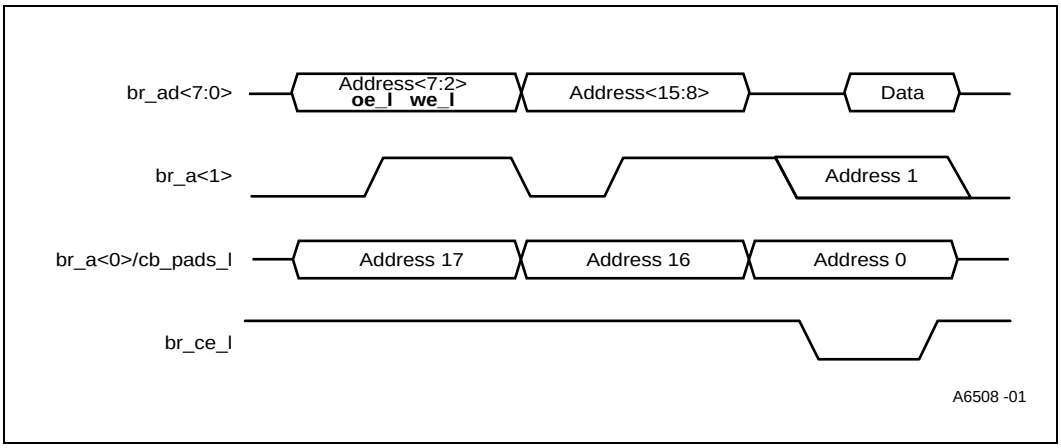
Any mixture between byte access and Dword access is allowed, providing that byte access followed by Dword access will be separated by at least 20 PCI clock cycles. Byte access is not allowed during normal operation. It is typically used for programming the expansion ROM.

7.3.1 Byte Read

Figure 7-2 shows the 21145 byte read cycle. It is executed as follows:

1. The host initiates a byte read cycle to the expansion ROM by writing the expansion ROM offset to CSR10 and by setting a read command in CSR9 (CSR9<14>) and CSR9<12> = 1.
2. The 21145 drives the expansion ROM address bits <7:2> and the signals oe_l and we_l on the br_ad lines, drives address bit 17 on the br_a<0>/cb_pads_l line, and sets br_a<1>. Signal br_a<1> is used as a latch enable to latch the address, oe_l, and we_l in the upper edge trigger latch.
3. The 21145 clears br_a<1>.
4. The 21145 drives the expansion ROM address bits <15:8> on the br_ad lines, drives address bit 16 on the br_a<0>/cb_pads_l line, and sets br_a<1>. Address bits <16:8> are latched in the upper edge trigger latch while the previous address bits (17, <7:2>) and the control signals (oe_l and we_l) are latched in the lower edge trigger latch.
5. The 21145 drives address bits <1:0> on br_a<1> and br_a<0>/cb_pads_l, respectively, and asserts the br_ce_l pin.
6. In response, the expansion ROM drives the data on the br_ad lines.
7. The 21145 terminates the byte read cycle by sampling the data, by placing it in CSR9<7:0>, and by deasserting the br_ce_l signal.
8. The driver can read the data from CSR9 after at least 20 PCI clock cycles passed since this CSR was previously written. Note that the results of trying to read the data earlier are UNPREDICTABLE.

Figure 7-2. Expansion ROM Byte Read Cycle



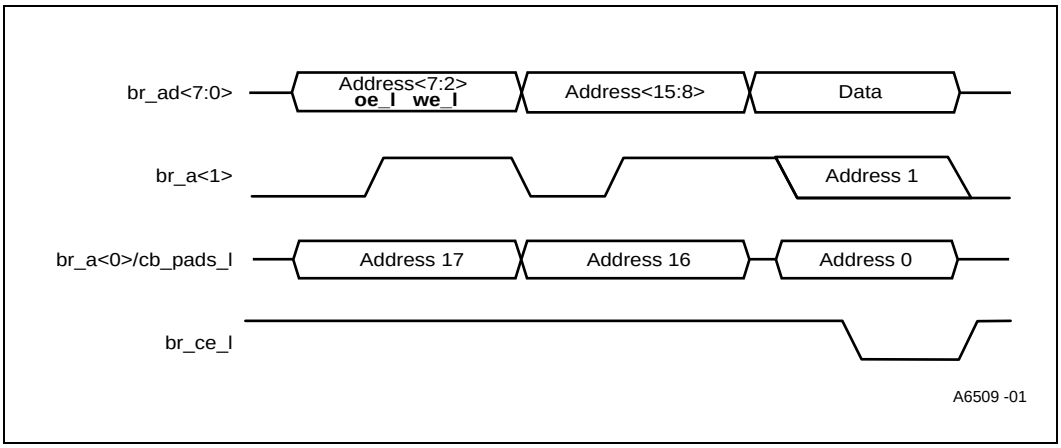
7.3.2 Byte Write

Before performing a write operation, all the expansion ROM entries must be 1. This is achieved by using the erase command.

Figure 7-3 shows the 21145 byte write cycle. It is executed as follows:

1. The host initiates a byte write cycle to the expansion ROM by writing the expansion ROM offset to CSR10, setting a write command in CSR9 (CSR9<13> and CSR9<12> = 1), and by writing the data to CSR9<7:0>.
2. The 21145 drives the expansion ROM address bits <7:2> and the signals oe_l and we_l on the br_ad lines, drives address bit 17 on the br_a<0>/cb_pads_l line, and sets br_a<1>. Signal br_a<1> is used as a latch enable to latch the address, oe_l, and we_l in the upper edge trigger latch.
3. The 21145 clears br_a<1>.
4. The 21145 drives the expansion ROM address bits <15:8> on the br_ad lines, drives address bit 16 on the br_a<0>/cb_pads_l line, and sets br_a<1>. Address bits <16:8> are latched in the upper edge trigger latch while the previous address bits (<17>, <7:2>) and the control signals (oe_l and we_l) are latched in the lower edge trigger latch.
5. The 21145 drives address bits <1:0> on br_a<1> and br_a<0>/cb_pads_l, respectively; drives the data on the br_ad lines; and asserts the br_ce_l pin.
6. The expansion ROM samples the data.
7. The 21145 terminates the byte write cycle by deasserting the br_ce_l signal.

Figure 7-3. Expansion ROM Byte Write Cycle



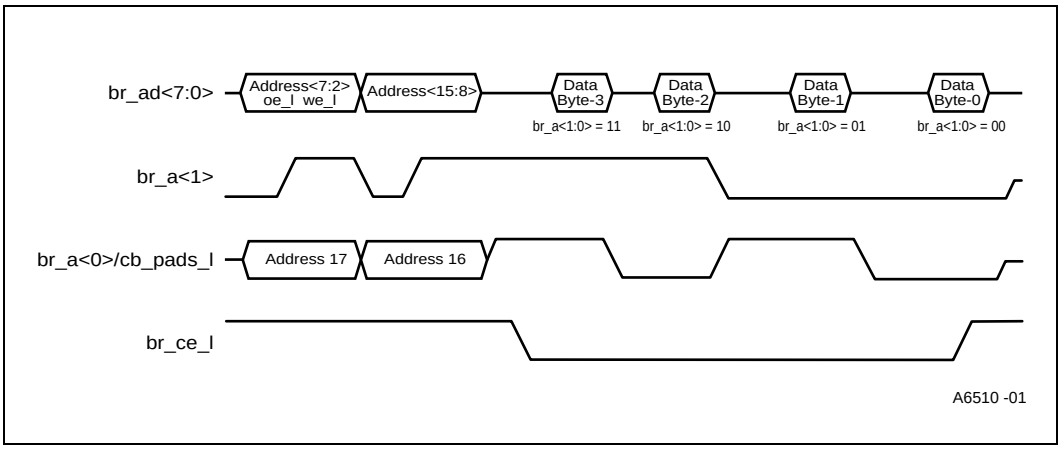
7.3.3 Dword Read

Figure 7-4 shows the Dword read cycle. The host initiates a Dword read cycle by executing a typical read cycle to the expansion ROM address space. The ad lines contain the expansion ROM address (base address and offset). Prior to the assertion of the trdy_l signal, the 21145 takes the following steps:

1. The 21145 drives the expansion ROM address bits <7:2> and the control signals oe_l and we_l on the br_ad lines, drives address bit 17 on the br_a<0>/cb_pads_l line, and sets br_a<1>. Signal br_a<1> is used as a latch enable to latch the address, oe_l, and we_l in the upper edge trigger latch.
2. The 21145 clears br_a<1>.
3. The 21145 drives the expansion ROM address bits <15:8> on the br_ad lines, drives address bit 16 on the br_ad<0> line, and sets br_a<1>. Address bits <16:8> are latched in the upper edge trigger latch while the previous address bits (17, <7:2>) and the control signals oe_l and we_l are latched in the lower edge trigger latch.
4. The 21145 remains br_a<1> high, drives br_a<0>/cb_pads_l to high, and asserts the br_ce_l pin.
5. In response, the expansion ROM drives the data on the br_ad lines (byte 3).
6. The 21145 samples the data (byte 3).
7. The 21145 remains br_a<1> high, drives br_a<0>/cb_pads_l to low, and asserts the br_ce_l pin.
8. In response, the expansion ROM drives the data on the br_ad lines (byte 2).
9. The 21145 samples the data (byte 2).
10. The 21145 drives br_a<1> to low, drives br_a<0>/cb_pads_l high, and asserts the br_ce_l pin.
11. In response, the expansion ROM drives the data on the br_ad lines (byte 1).
12. The 21145 samples the data (byte 1).
13. The 21145 remains br_a<1> low, drives br_a<0>/cb_pads_l to low, and asserts the br_ce_l pin.
14. In response, the expansion ROM drives the data on the br_ad lines (byte 0).
15. The 21145 samples the data and deasserts the br_ce_l signal.

16. The 21145 assembles the 4 bytes, drives the data on the ad lines, and asserts trdy_l.

Figure 7-4. Expansion ROM Dword Read Cycle



7.4 Serial ROM

There are four serial ROM interface pins (Table 8-81):

- Serial ROM data out (sr_do)
- Serial ROM data in (sr_di)
- Serial ROM clock (sr_ck)
- Serial ROM chip select (sr_cs)

The 21145 supports two sizes of serial ROM, 1 Kb and 4 Kb.

The serial ROM has three types of information:

- Information that is used by the 21145
- Information that can be used by the 21145 driver
- CIS data

The information that is used by the 21145 is located in the ID block and the Magic block. These blocks are automatically read by the 21145 without software involvement. The ID block is read upon a hardware reset or when the 21145 transitions from the D3 power state to the D0 power state. The Magic block is read when the 21145 transitions from the D0 power state to any other power state. The ID block is located at the lowest addresses of the serial ROM, beginning in address 0; the Magic block is located at the higher addresses of the serial ROM.

The space in the serial ROM that is between the ID block and the Magic block can be used for driver information and for CIS data. When using the Intel drivers, the area that is immediately after the ID block is used by the driver.

The 21145 driver accesses the serial ROM through CSR9. The access sequences and timing are handled by the software. The serial ROM operations in this method can be read, write, or erase. The read and write operations in this method are described in Section 7.4.1 and Section 7.4.2. The erase operation is handled similarly to the read and write operations.

The serial ROM is mapped into the memory space beginning at offset 200H from the CBMA register. This feature allows the system software to read the CIS data in a simple memory read operation. For example, when a memory read access to address CBMA + 200H is performed, the 21145 returns the data located in address 0 of the serial ROM. This method can be used only if the CIS data is located in the serial ROM (CCIS<2:0>=2). Write and erase operations are not supported in this method.

Access to the serial ROM through memory read is not allowed while an access to the serial ROM through CSR9 is ongoing.

For more information about the serial ROM format including the ID and Magic block, see the *21X4 Serial ROM Format* specification available from the Intel Developer's website located at http://developer.intel.com/.

7.4.1 Read Operation

Read operations consist of three phases:

1. Command phase—3 bits (110b)
2. Address phase—6 bits for 256-bit to 1 Kb ROMs, 8 bits for 2 Kb to 4 Kb ROMs.
3. Data phase—16 bits

Figure 7-5 and Figure 7-6 show a typical read cycle that describes the action steps that need to be taken by the driver to execute a read cycle. The timing (listed on the right side of the figures) specifies the minimum time that the driver must wait before advancing to the next action.

During both the address phase in Figure 7-5 and the data phase in Figure 7-6, 1 bit is handled during each phase cycle. Therefore, the address phase should be repeated 6 or 8 times depending on the address length and the data phase should be repeated 16 times. Note that the value DX is the current data bit.

Figure 7-5. Read Cycle (Page 1 of 2)

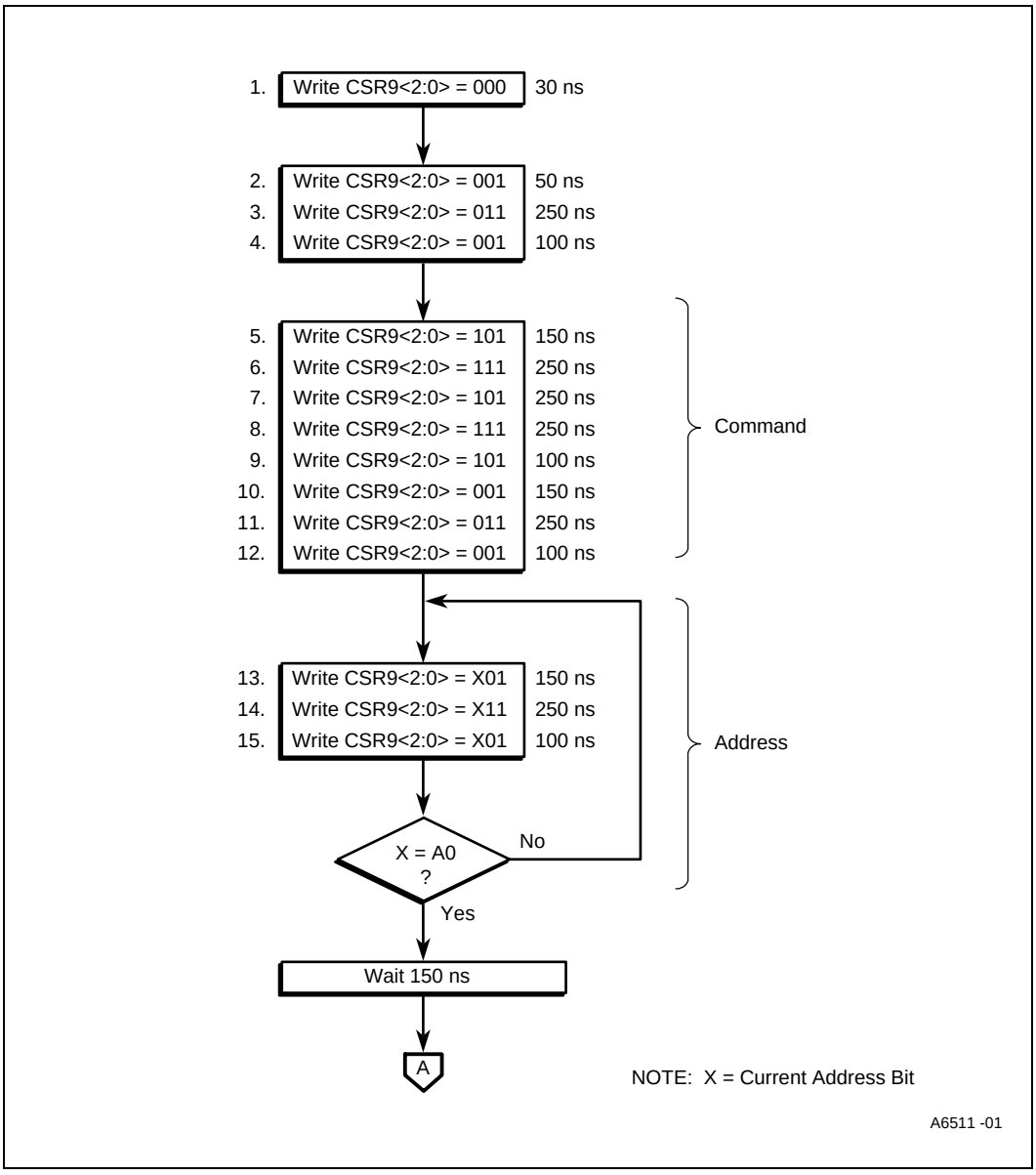


Figure 7-6. Read Cycle (Page 2 of 2)

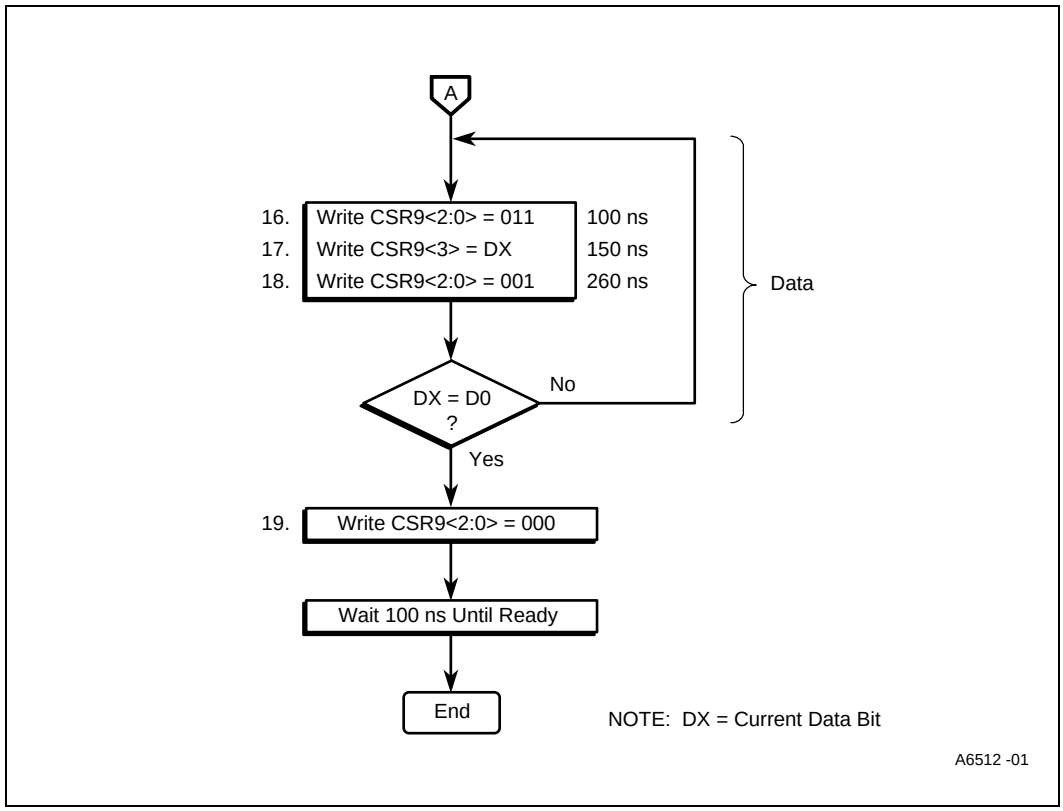
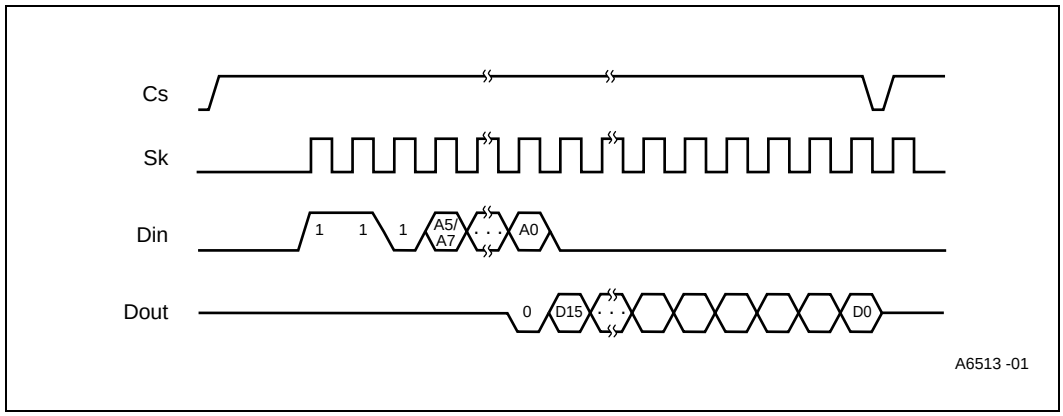


Figure 7-7 shows the read operation timing of the address and data.

Figure 7-7. Read Operation



7.4.2 Write Operation

Write operations consist of three phases:

1. Command phase—3 bits (101b)
2. Address phase—6 bits for 256-bit to 1Kb ROMs, 8 bits for 2Kb to 4Kb ROMs.
3. Data phase—16 bits

Figure 7-8 and Figure 7-9 show a typical write cycle that describes the action steps that need to be taken by the driver to execute a write cycle. The timing (listed on the right side of the figures) specifies the minimum time that the driver must wait before advancing to the next action.

During both the address phase in Figure 7-8 and the data phase in Figure 7-9, 1 bit is handled during each phase cycle. Therefore, the address phase should be repeated 6 or 8 times depending on the address length and the data phase should be repeated 16 times.

Figure 7-8. Write Cycle (Page 1 of 2)

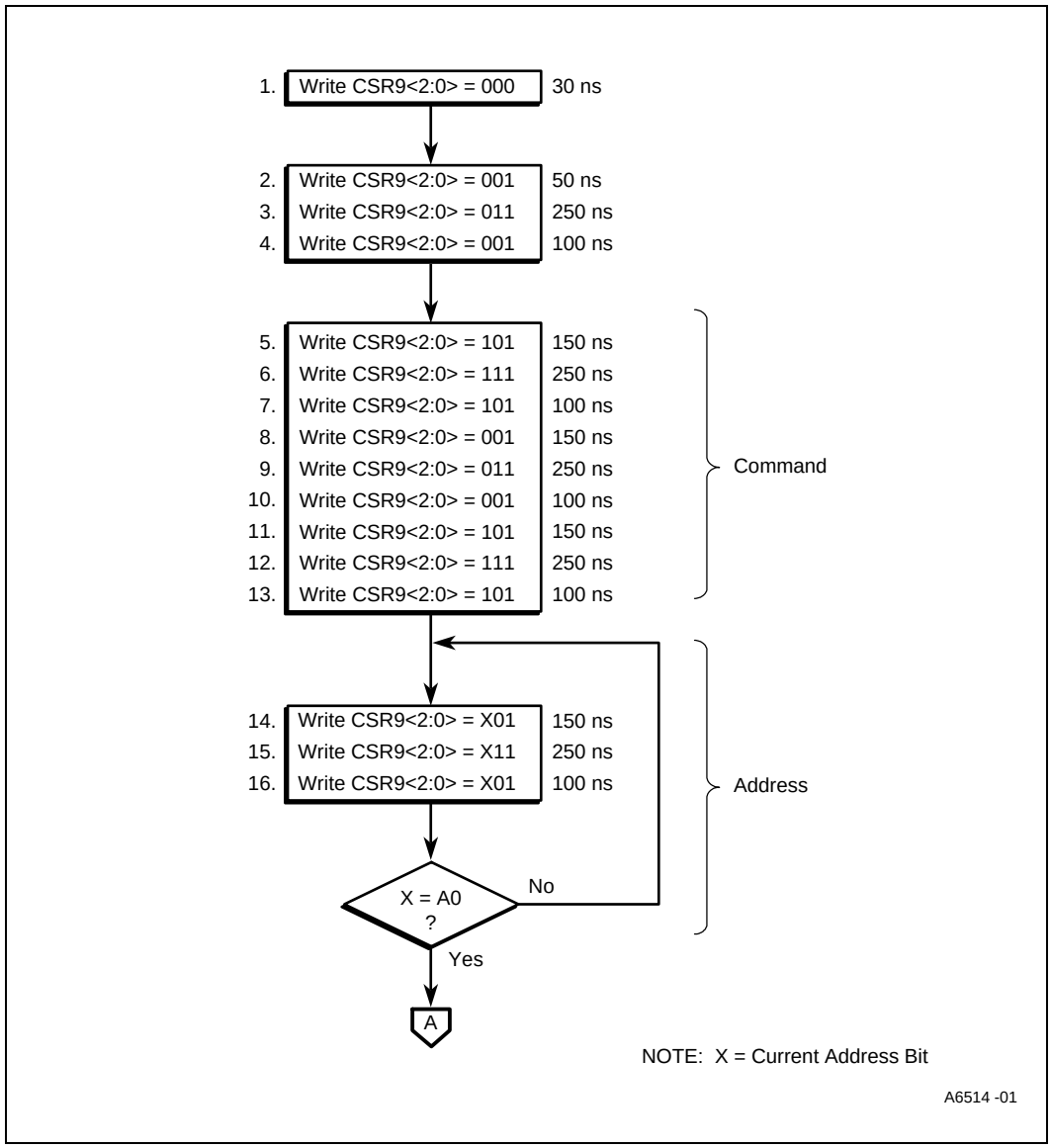


Figure 7-9. Write Cycle (Page 2 of 2)

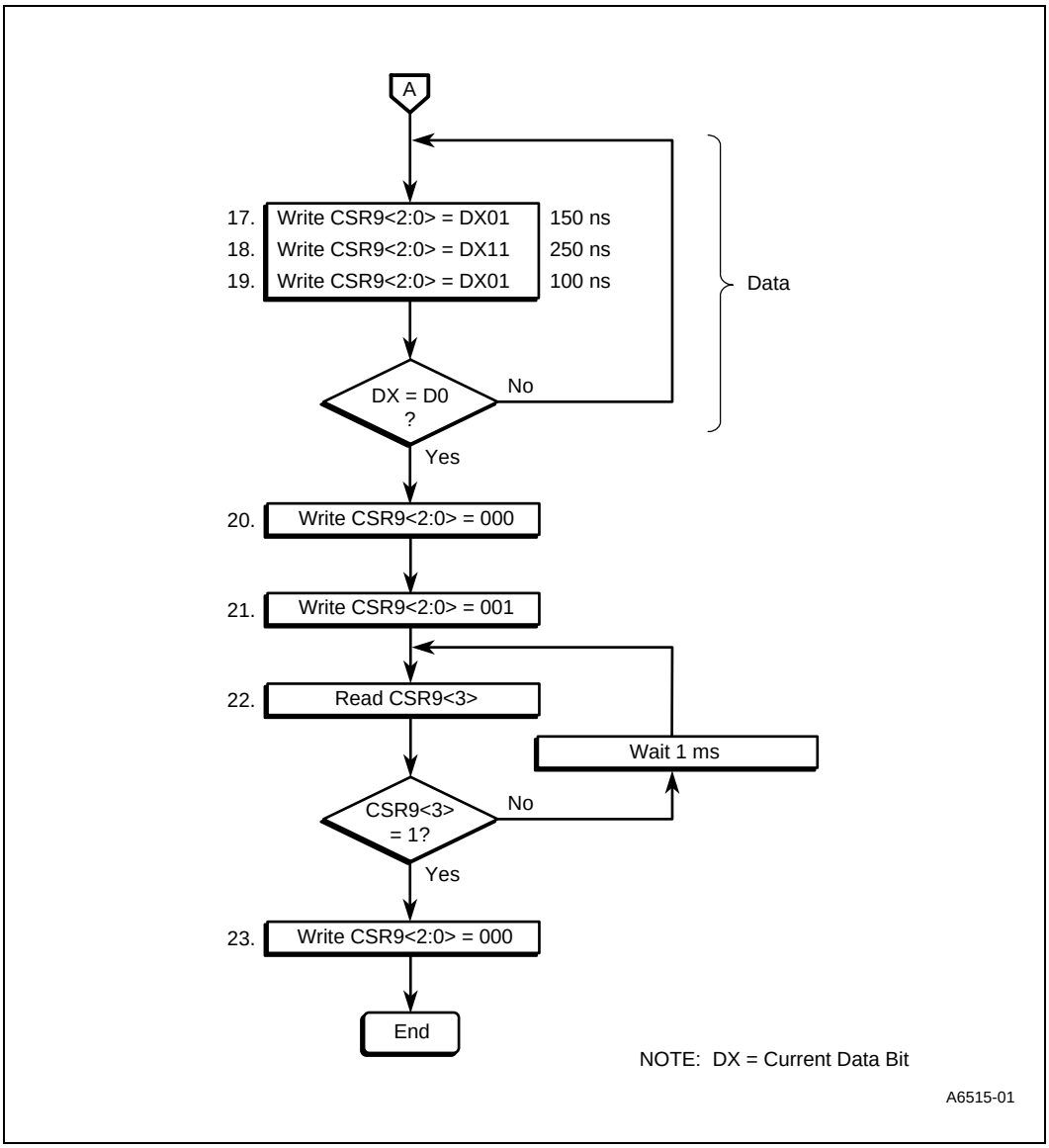
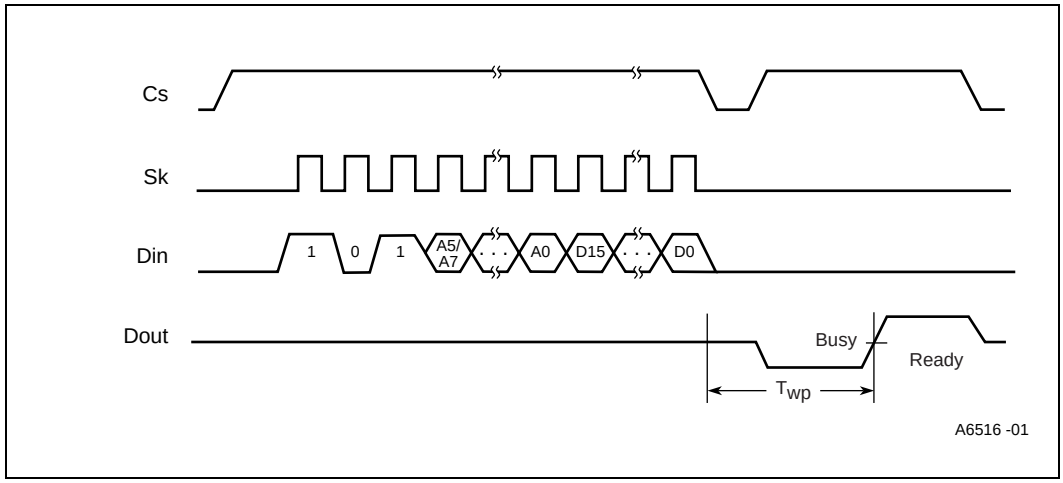


Figure 7-10 shows the write operation timing of the address and data. The time period indicated by Twp is the actual write cycle time.

Figure 7-10. Write Operation



7.5 External Register Operation

The 21145 provides the ability to connect an external 8-bit register to the expansion ROM port. Figure 7-1 illustrates the signals for this connection.

Note: CSR10 must be 0 before any external register access is done.

To read from the external register, the driver should set the read command (CSR9<14>) and select the external register (CSR9<10> =1). The 21145 performs the same steps as described in Section 7.3.1. The only differences are that now the 21145 drives 1 on both the we_l and oe_l expansion ROM inputs and drives 0 on br_a<0>/cb_pads_l. This, together with the assertion of br_ce_l, performs the actual read operation. The data is sampled by the 21145 and is placed in CSR9<7:0>.

Note: Consecutive accesses to the external register should be separated by at least 20 PCI clock cycles. Accessing the serial ROM after access to the external register can be done only after at least 20 PCI clock cycles.

To write to the external register, the driver should set the write command (CSR9<13>), select the external register (CSR9<10>=1), and write the data to CSR9<7:0>. The 21145 performs the same steps as described in Section 7.3.2. The only differences are that now the 21145 drives 1 on both the we_l and oe_l expansion ROM inputs and drives 1 on br_a<0>/cb_pads_l. This, together with the assertion of br_ce_l, performs the actual write operation.

7.6 General-Purpose Port and LEDs

The 21145 contains a 4-bit port (gep<3:0>) that can be used as either as a general-purpose port or for network event LEDs. Each of the four pins can be programmed to be either a general-purpose port pin or for an LED/control pin. Each general-purpose port pin can be programmed to be either an input pin or an output pin. When programmed as an input pin, gep<1:0> can generate an interrupt when the pin changes its state either from 1 to 0 or 0 to 1. Refer to Section 8.3.2.18 (CSR15<30:16>) for a detailed programming description. Table 7-2 provides a description of the pin connections for 10BASE2 mode selection and LED indicators.

Table 7-2. Mode Selection and LED Indicator Pin Descriptions

Signal	Pin Number, 176-pin device	Pin Number, 144-pin device	Description
activ	124	101	This pin provides the receive and transmit activity indication. A stretcher circuit implemented on this pin enables a direct connection of the pin to the LED.
rcv_match	125	102	A receive packet passed address recognition.
link	126	103	Link and activity indications. This pin provides link indication for the 10BASE-T or 100BASE-TX SYM ports. It can also provide combined link and activity indications. If the MiscHwOptions<0> bit in the serial ROM is cleared, this pin provides only the link indication. If the MiscHwOptions<0> bit in the serial ROM is set, this pin provides both the link and activity indications. In this mode, an LED connected to this pin remains lit when a link is present and there is no activity, and blinks when activity is present.

Registers 8

This chapter describes the 21145's PCI configuration registers, CardBus Status Changed registers, command and status registers (CSRs) and HomePNA PHY internal registers. The 21145 implements separate PCI Ethernet and Modem functions (176-pin 21145 only). The two functions have separate PCI Configuration Spaces and sets of CardBus Status Changed registers. The Ethernet function is described in Section 8.1 to Section 8.3, and the Modem function in Section 8.6 to Section 8.8. The HomePNA PHY's registers are described in Section 8.5.

For both functions, the configuration registers are located in the configuration space and are accessed through configuration accesses. The configuration registers are used for initialization and configuration, and accessed by system software.

The Ethernet function's CSRs are 21145 specific. These registers can be mapped to either the host I/O address space or the host memory address space. The CSRs are accessed by the 21145 driver and are used for initialization, pointers, commands, and status reporting.

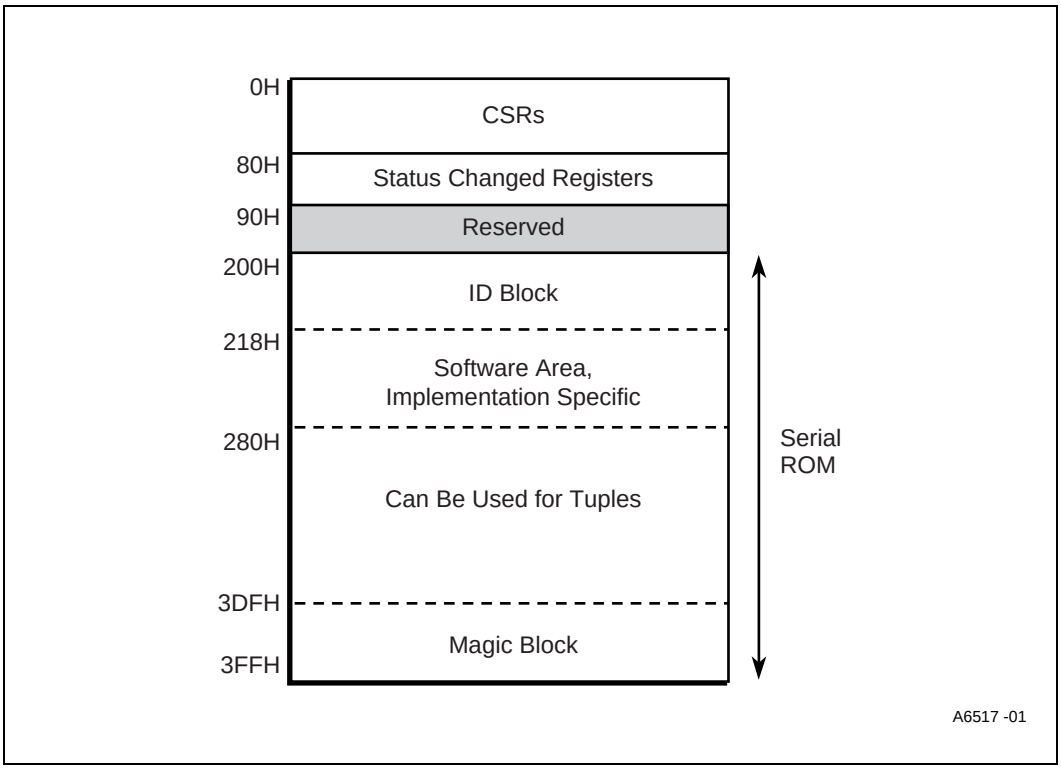
The CardBus Status Changed registers are standard registers that are defined in the PC Card Standard. These registers are located *only* in the host memory address space and are used for control and status in CardBus applications.

8.1 Ethernet Function Memory Map

The 21145 implements two base address registers that can map the 21145 structures to the I/O and the memory address spaces. The I/O base address register (CBIO) can map only the 21145 Ethernet Function CSRs. The memory base address register (CBMA) can map the 21145 Ethernet Function CSRs, the 4 CardBus Status Changed registers, and the serial ROM.

Figure 8-1 shows the Ethernet Function 21145 structures that are mapped into the host memory address space.

Figure 8-1. 21145 Ethernet Function Memory Map



This figure shows the case where the serial ROM size is 4 Kb when Intel drivers are used. In this case, the space that is between 218H and 280H is used by the 21145 drivers. For applications that are not using Intel drivers, the space that is between 218H and 3DFH can be used for tuples and for vendor-specific information. For information about the contents of the serial ROM, see the *21X4 Serial ROM Format* specification available from the Intel Developer's website located at http://developer.intel.com/.

8.2 Ethernet Function Configuration Operation

The 21145 allows full software-driven initialization and configuration. This permits the software to identify and query the 21145.

The 21145 Ethernet Function treats configuration space write operations to registers that are reserved as no-ops. That is, the access completes normally on the bus and the data is discarded.

A software reset (CSR0<0>) has no effect on the configuration registers. A hardware reset and exit from the D3 power state sets the configuration registers to their default values.

The 21145 supports byte, word, and longword accesses to configuration registers.

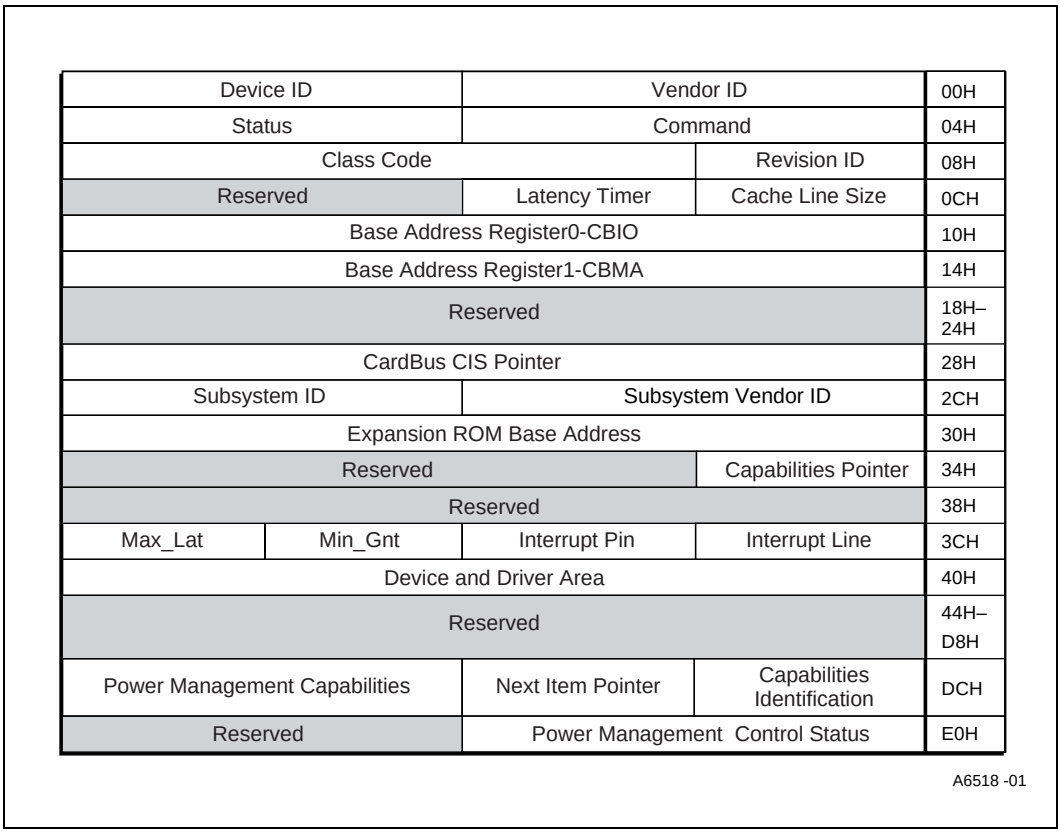
8.2.1 Ethernet Function Configuration Register Mapping

Table 8-1 lists the definitions and addresses for the Ethernet function configuration registers and Figure 8-2 shows the structure.

Table 8-1. Ethernet Function Configuration Registers Mapping

Configuration Register	Identifier	I/O Address Offset
Identification	CFID	00H
Command and status	CFCS	04H
Revision	CFRV	08H
Latency timer	CFLT	0CH
Base I/O address	CBIO	10H
Base memory address	CBMA	14H
Reserved	—	18H – 24H
Card information structure	CCIS	28H
Subsystem ID	CSID	2CH
Expansion ROM base address (176-pin 21145 only)	CBER	30H
Capabilities Pointer	CCAP	34H
Reserved	—	38H
Interrupt	CFIT	3CH
Device and Driver area	CFDD	40H
Reserved	—	44H – D8H
Capability ID	CCID	DCH
Power Management Control and Status	CPMC	E0H

Figure 8-2. Configuration Register Structure



8.2.2 Standard Ethernet Function Configuration Registers

The 21145 Ethernet function implements 13 standard PCI configuration registers. These registers are described in the following subsections.

8.2.2.1 Ethernet Function Configuration ID Register (CFID–Offset 00H)

The CFID register identifies the 21145 Ethernet Function. Figure 8-3 shows the CFID register bit fields and Table 8-2 describes the bit fields.

Figure 8-3. CFID Register Bit Fields

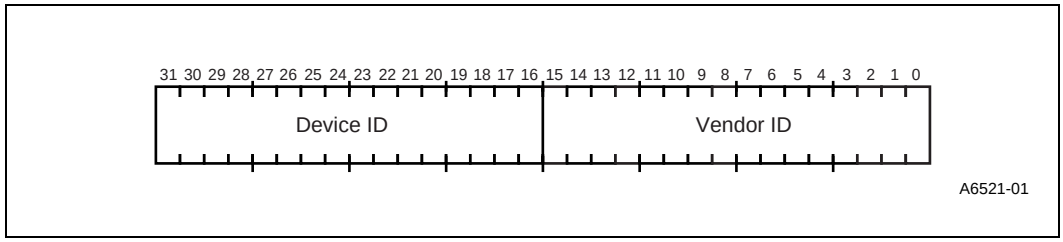


Table 8-2. CFID Register Bit Fields Description

Field	Description
31:16	Device ID Provides the unique 21145 Ethernet Function ID number (0039H).
15:0	Vendor ID Specifies the manufacturer ID of the 21145 (8086H).

Table 8-3 lists the access rules for the CFID register.

Table 8-3. CFID Register Access Rules

Category	Description
Value after hardware reset	00398086H
Read access rules	—
Write access rules	Writing has no effect.

8.2.2.2 Command and Status Configuration Register (CFCS–Offset 04H)

The CFCS register is divided into two sections: a command register (CFCS<15:0>) and a status register (CFCS<31:16>).

The command register provides control of the 21145's ability to generate and respond to PCI cycles. When 0 is written to this register, the 21145 logically disconnects from the PCI bus for all accesses except configuration accesses.

The status register records status information for the PCI bus-related events. The CFCS status bits are not cleared when they are read. Writing 1 to these bits clears them; writing 0 has no effect. If the CFCS is addressed by the host before these bits are loaded from the serial ROM, the 21145 responds with a retry termination on the PCI bus.

Figure 8-4 shows the CFCS register bit fields.

Figure 8-4. CFCS Register Bit Fields

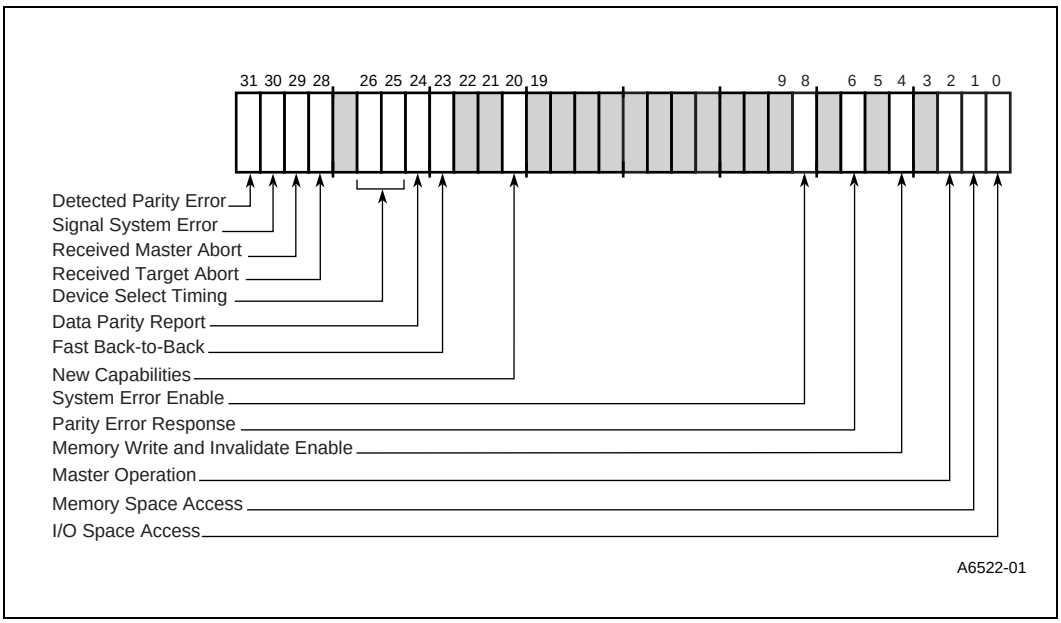


Table 8-4 describes the CFCS register bit fields.

Table 8-4. CFCS Register Bit Fields Description

Field	Bit Type	Description
31	Status	Detected Parity Error When set, indicates that the 21145 detected a parity error, even if parity error handling is disabled in parity error response (CFCS<6>).
30	Status	Signal System Error When set, indicates that the 21145 asserted the system error serr_l pin.
29	Status	Received Master Abort When set, indicates that the 21145 terminated a master transaction with master abort.
28	Status	Received Target Abort When set, indicates the 21145 master transaction was terminated due to a target abort.
26:25	Status	Device Select Timing Indicates the timing of the assertion of device select (devsel_l). These bits are fixed at 01, which indicates a medium assertion of devsel_l.
24	Status	Data Parity Report This bit sets when all of the following conditions are met: • 21145 asserts parity error perr_l or it senses the assertion of perr_l by another device. • 21145 operates as a bus master for the operation that caused the error. • Parity error response (CFCS<6>) is set.
23	Status	Fast Back-to-Back Always set by the 21145. This indicates that the 21145 is capable of accepting fast back-to-back transactions that are not sent to the same bus device.
20	Status	New Capabilities Indicates whether or not the 21145 implements a list of new capabilities. When set, this bit indicates the presence of New Capabilities. When cleared, New Capabilities are not implemented. The value of this bit is loaded from Func0_HwOptions<3> bit (PME_Enable) in the serial ROM.
8	Command	System Error Enable When set, the 21145 asserts system error (serr_l) when it detects a parity error on the address phase (ad<31:0> and c_be_l<3:0>).
6	Command	Parity Error Response When set, the 21145 asserts fatal bus error (CSR5<13>) after it detects a parity error. When reset, any detected parity error is ignored and 21145 continues normal operation. Parity checking is disabled after a hardware reset.
4	Command	Memory Write and Invalidate Enable When set, the 21145 is allowed to generate the memory write and invalidate command. When reset, the 21145 capability to generate the memory write and invalidate command is disabled.
2	Command	Master Operation When set, the 21145 is capable of acting as a bus master. When reset, the 21145 capability to generate PCI accesses is disabled. For normal 21145 operation, this bit must be set.
1	Command	Memory Space Access When set, the 21145 responds to memory space accesses. When reset, the 21145 does not respond to memory space accesses.
0	Command	I/O Space Access When set, the 21145 responds to I/O space accesses. When reset, the 21145 does not respond to I/O space accesses.

Table 8-5 lists the access rules for the CFCS register.

Table 8-5. CFCS Register Access Rules

Category	Description
Value after hardware reset	02800000H
Read access rules	—
Write access rules	—

8.2.2.3 Configuration Revision Register (CFRV–Offset 08H)

The CFRV register contains the 21145 revision number. Figure 8-5 shows the CFRV register bit fields and Table 8-6 describes the bit fields.

Figure 8-5. 21145 CFRV Register Bit Fields

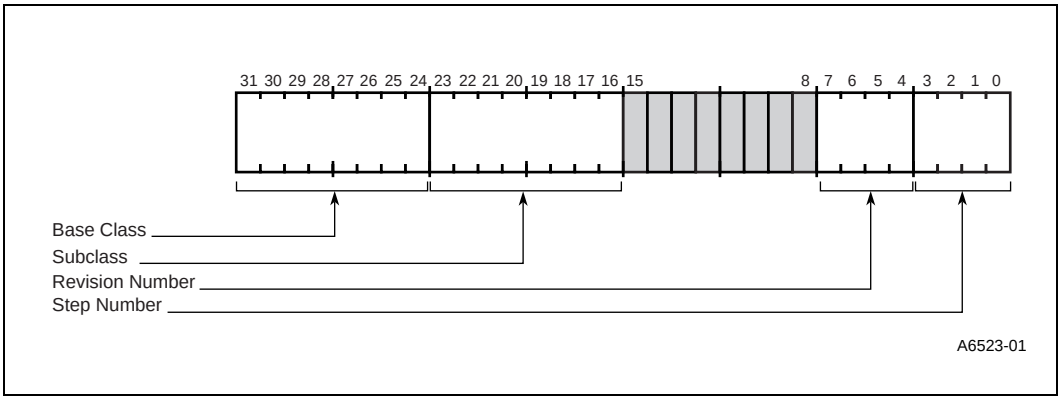


Table 8-6. CFRV Register Bit Fields Description

Field	Description
31:24	Base Class Indicates a network controller and is equal to 2H.
23:16	Subclass Indicates a fast Ethernet controller and is equal to 0H.
7:4	Revision Number Indicates the 21145 Ethernet function revision number.
3:0	Step Number Indicates the 21145 Ethernet function step number within the current revision.

Table 8-7 lists the revision and step numbers for each variant of the device.

Table 8-7. 21145 Ethernet Function Revision and Step Number

Device	Revision Number	Step Number
21145, 144-pin, B0 stepping (DC1116, order no. DE-NH978-TA)	1	1
21145, 176-pin, B0 stepping (DC1116, order no. DE-NH978-AA)	1	9

Table 8-8 lists the access rules for the CFRV register.

Table 8-8. CFRV Register Access Rules

Category	Description
Value after hardware reset	02000019H for 176-pin 02000011H for 144-pin
Read access rules	—
Write access rules	Writing has no effect.

8.2.2.4 Configuration Latency Timer Register (CFLT–Offset 0CH)

This register determines whether the 21145 Modem function is enabled (176-pin device only) and configures the cache line size field and the 21145 latency timer. Figure 8-6 shows the CFLT bit field and Table 8-9 describes the CFLT bit field.

Figure 8-6. CFLT Configuration Latency Timer Register

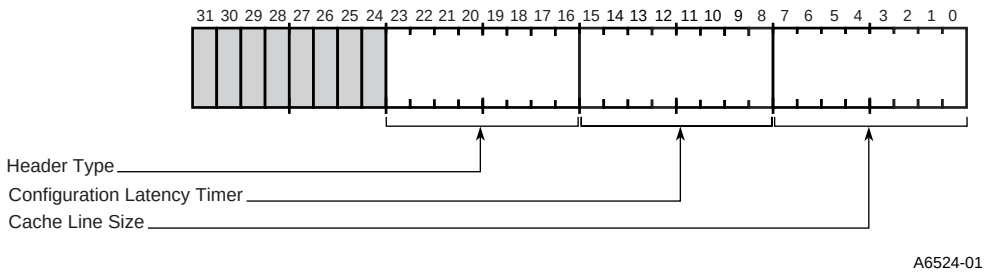


Table 8-9. CFLT Register Bit Fields Description

Field	Description
23:16	Header Type Specifies whether 21145 Modem function is enabled. Value: 80H if function is enabled, 00H if disabled.
15:8	Configuration Latency Timer Specifies, in units of PCI bus clocks, the value of the latency timer of the 21145. When the 21145 asserts frame_l, it enables its latency timer to count. If the 21145 deasserts frame_l prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the 21145 initiates transaction termination as soon as its gnt_l is deasserted.
7:0	Cache Line Size Specifies, in units of 32-bit words, the system cache line size. The 21145 supports cache line sizes of 8, 16 and 32 longwords. If an attempt is made to write an unsupported value to this register, the 21145 behaves as if a value of zero was written. If any extended PCI command is used, the driver should use the value of the cache line size to program the cache alignment bits (CSR0<15:14>).

Table 8-10 lists the access rules for the CFLT register.

Table 8-10. CFLT Access Rules

Category	Description
Value after hardware reset	0H
Read access rules	—
Write access rules	—

8.2.2.5 Configuration Base I/O Address Register (CBIO–Offset 10H)

The CBIO register specifies the base I/O address for accessing the 21145 Ethernet Function CSRs (CSR0–15, CSR1-PM and CSR2-PM). For example, if the CBIO register is programmed to 1000H, the I/O address of CSR15 is equal to CBIO + CSR15-offset for a value of 1078H (Table 8-31).

This register must be initialized prior to accessing any Ethernet CSR with I/O access.

Figure 8-7 shows the CBIO register bit fields and Table 8-11 describes the bit fields.

Figure 8-7. CBIO Register Bit Fields

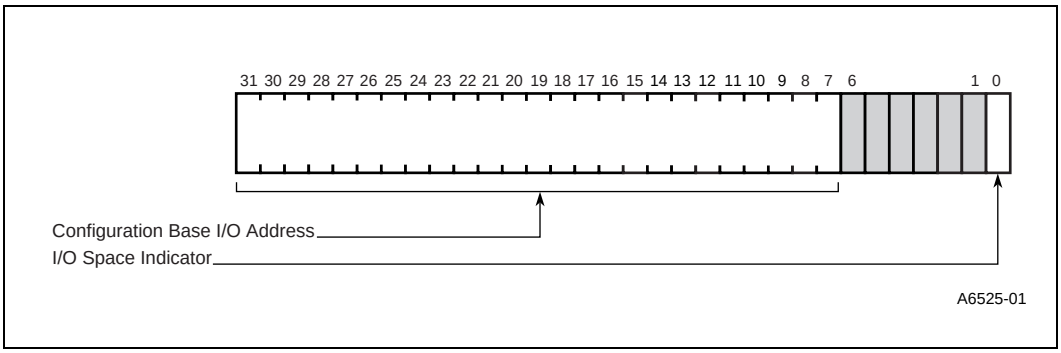


Table 8-11. CBIO Register Bit Fields Description

Field	Description
31:7	Configuration Base I/O Address Defines the base address assigned for mapping the 21145 Ethernet Function CSRs.
6:1	This field value is 0 when read.
0	I/O Space Indicator Determines that the register maps into the I/O space. The value in this field is 1. This is a read-only field.

Table 8-12 lists the access rules for the CBIO register.

Table 8-12. CBIO Register Access Rules

Category	Description
Value after hardware reset	Undefined
Read access rules	—
Write access rules	—

8.2.2.6 Configuration Base Memory Address Register (CBMA–Offset 14H)

The CBMA register specifies the base memory address for memory accesses to the 21145 Ethernet Function structures. The CBMA maps 18 21145-specific CSRs, 4 CardBus Status Changed registers, and the serial ROM.

This register must be initialized prior to accessing any CSR with memory access.

Figure 8-8 shows the CBMA register bit fields and Table 8-13 describes the bit fields.

Figure 8-8. CBMA Register Bit Fields

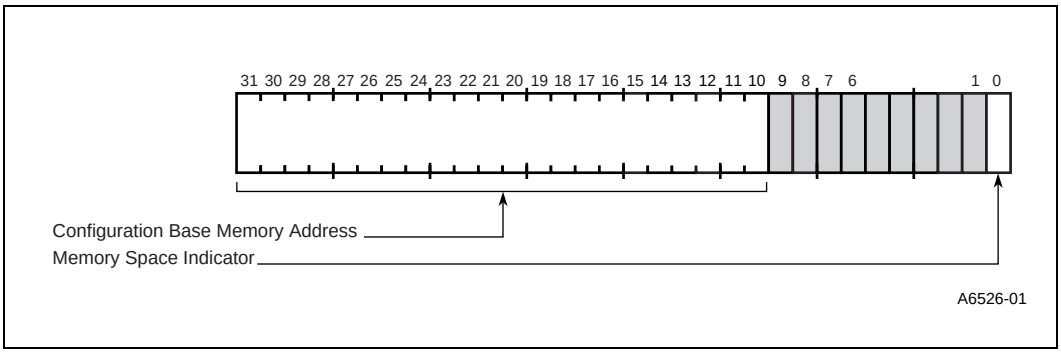


Table 8-13. CBMA Register Bit Fields Description

Field	Description
31:10	Configuration Base Memory Address Defines the base address assigned for mapping the 21145 CSRs.
9:1	This field value is 0 when read.
0	Memory Space Indicator Determines that the register maps into the memory space. The value in this field is 0. This is a read-only field.

Table 8-14 lists the access rules for the CBMA register.

Table 8-14. CBMA Register Access Rules

Category	Description
Value after hardware reset	Undefined
Read access rules	—
Write access rules	—

8.2.2.7 Configuration Card Information Structure Register (CCIS–Offset 28H)

The CCIS register is a read-only 32-bit register. This register points to one of the possible address spaces where the card information structure (CIS) begins. The pointer is used in a CardBus PC Card environment. The content of the CCIS is loaded from the serial ROM after a hardware reset. If the CCIS is accessed by the host before its content is loaded from the serial ROM, the 21145 responds with retry termination on the PCI bus. A value of 0 in this register indicates that CIS is not supported.

Figure 8-9 shows the CCIS register bit fields and Table 8-15 describes the bit fields.

Figure 8-9. CCIS Register Bit Fields

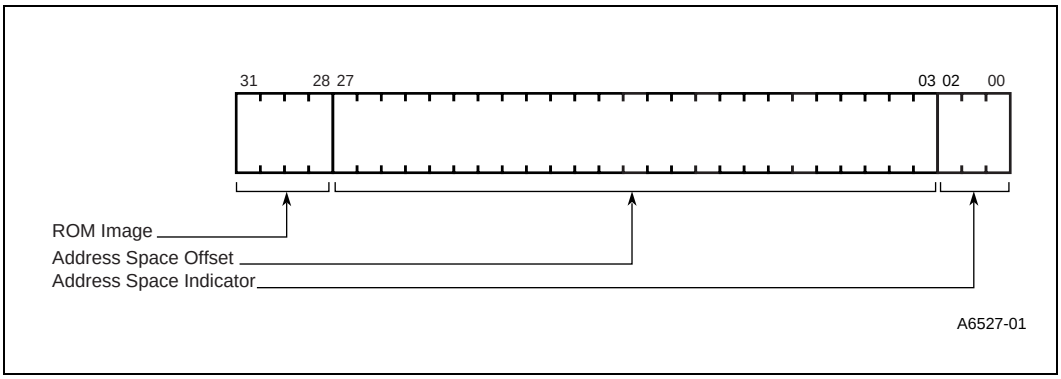


Table 8-15. CCIS Register Bit Fields Description

Field	Description
31:28	ROM Image The 4-bit ROM image field value when the CIS resides in an expansion ROM.
27:3	Address Space Offset This field contains the address offset within the address space indicated by the address space indicator field (CCIS<2:0>).
2:0	Address Space Indicator This field indicates the location of the CIS base address. The 21145 supports the value of 2, indicating that the CIS is stored in the serial ROM, and 7, indicating that the CIS is stored in the expansion ROM. Any value other than 2 or 7 may lead to unpredictable behavior.

Table 8-16 lists the access rules for the CCIS register.

Table 8-16. CCIS Register Access Rules

Category	Description
Value after hardware reset	Read from serial ROM.
Read access rules	—
Write access rules	Write has no effect on 21145.

8.2.2.8 Subsystem ID Register (CSID–Offset 2CH)

The CSID register is a read-only 32-bit register. The content of the CSID is loaded from the serial ROM after a hardware reset. If the CSID is accessed by the host before its content is loaded from the serial ROM, the 21145 responds with retry termination on the PCI bus. The value is 0 if the serial ROM data integrity check fails.

Figure 8-10 shows the CSID register bit fields and Table 8-17 describes the bit fields.

Figure 8-10. CSID Register Bit Fields

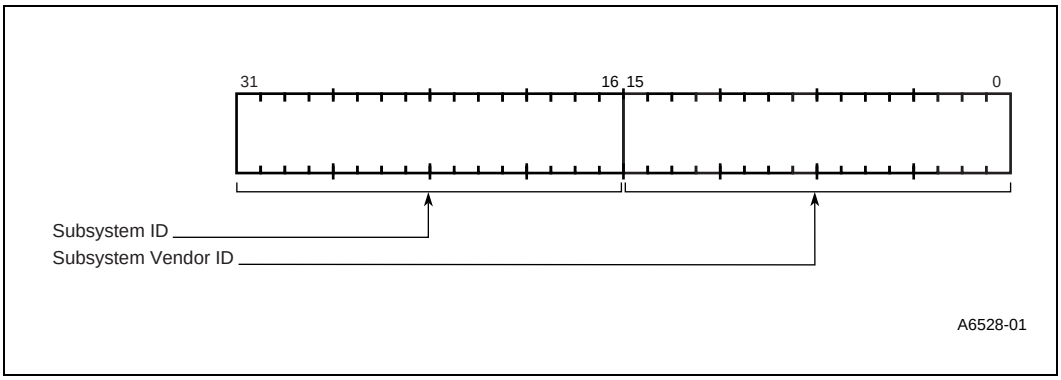


Table 8-17. CSID Register Bit Fields Description

Field	Description
31:16	Subsystem ID A 16-bit field containing the Ethernet Function's subsystem ID.
15:0	Subsystem Vendor ID A 16-bit field containing the Ethernet Function's subsystem vendor ID.

Table 8-18 lists the access rules for the CSID register.

Table 8-18. CSID Register Access Rules

Category	Description
Value after hardware reset	Read from serial ROM.
Read access rules	—
Write access rules	Write has no effect on 21145.

8.2.2.9 Expansion ROM Base Address Register (CBER–Offset 30H)

This register is valid for the 176-pin 21145 only. The CBER register specifies the expansion ROM base address and provides information about the expansion ROM size. This register must be initialized prior to accessing the expansion ROM with longword access (see Section 7.3).

Figure 8-11 shows the CBER register bit fields and Table 8-19 describes the bit fields.

Figure 8-11. CBER Register Bit Fields

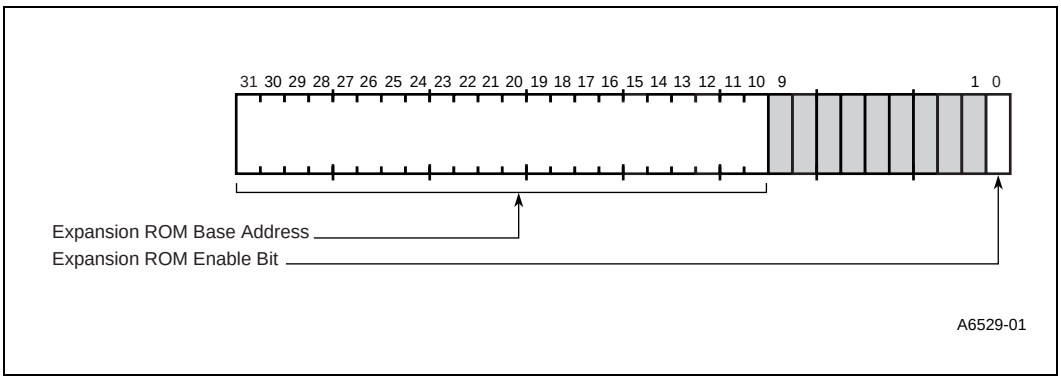


Table 8-19. CBER Register Bit Fields Description

Field	Description
31:10	Expansion ROM Base Address Defines the base address assigned for mapping the expansion ROM. It also provides information about the expansion ROM size. CBER<17:10> are hardwired to 0, indicating that the expansion ROM size is up to 256KB.
9:1	This field value is 0 when read.
0	Expansion ROM Enable Bit The 21145 responds to its expansion ROM accesses only if the memory space access bit (CFCS<1>) and the expansion ROM enable bit are both set to 1.

Table 8-20 lists the access rules for the CBER register.

Table 8-20. CBER Register Access Rules

Category	Description
Value after hardware reset	XXXX0000H
Read access rules	—
Write access rules	—

8.2.2.10 Capabilities Pointer (CCAP–Offset 34H)

The CCAP register has a pointer to the power-management register block in the PCI configuration space. This pointer is valid only if the new capabilities bit in CFCS is set.

Figure 8-12 shows the CCAP register bit fields and Table 8-21 describes the bit fields.

Figure 8-12. CCAP Register Bit Fields

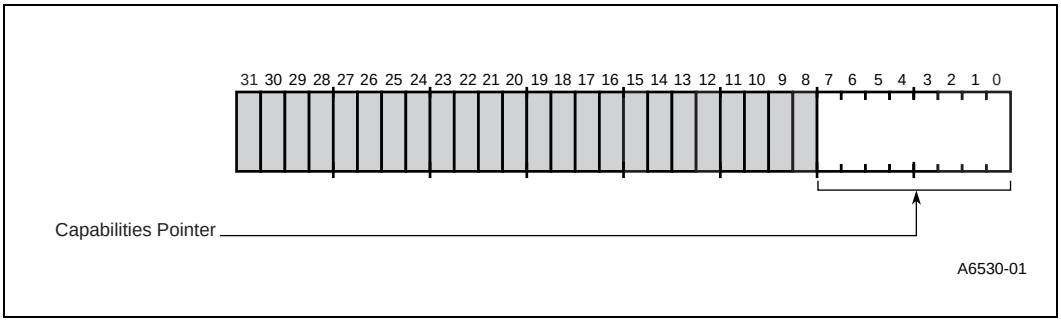


Table 8-21. CCAP Register Bit Fields Description

Field	Description
7:0	Capabilities Pointer Points to the location of the power-management register block in the PCI configuration space. The value of this field is determined by Func0_HwOptions<3> bit (PME_Enable**)** in the serial ROM. If this bit is set, the value of this field is DCH; otherwise, this field is read as 00H.

Table 8-22 lists the access rules for the CCAP register.

Table 8-22. CCAP Register Access Rules

Category	Description
Value after hardware reset	000000DCH or 00000000H[1]
Read access rules	—
Write access rules	—

NOTE:
1. According to Func0_HwOptions<3> (PME_Enable) in the serial ROM.

8.2.2.11 Configuration Interrupt Register (CFIT–Offset 3CH)

The CFIT register is divided into two sections: the interrupt line and the interrupt pin. CFIT configures both the system's interrupt line and the 21145 interrupt pin connection. Figure 8-13 shows the CFIT register bit fields.

Figure 8-13. CFIT Register Bit Fields

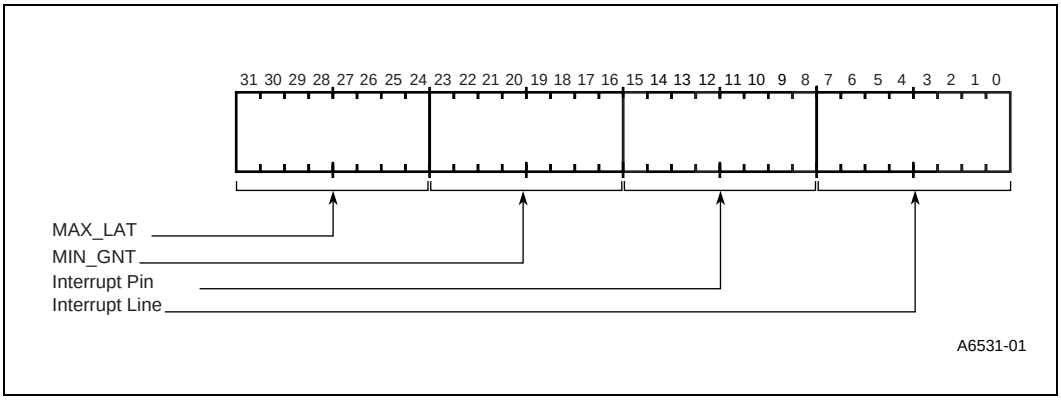


Table 8-23 describes the CFIT register bit fields.

Table 8-23. CFIT Register Bit Fields Description

Field	Description
31:24	MAX_LAT This field indicates how often the device needs to gain access to the PCI bus. Time unit is equal to 0.25 µs, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 28H (10 µs).
23:16	MIN_GNT This field indicates the burst period length that the device needs. Time unit is equal to 0.25 µs, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 14H (5 µs).
15:8	Interrupt Pin Indicates which interrupt pin the 21145 uses. The 21145 uses INTA# and the read value is 01H.
7:0	Interrupt Line Provides interrupt line routing information. The basic input/output system (BIOS) writes the routing information into this field when it initializes and configures the system. The value in this field indicates which input of the system interrupt controller is connected to the 21145's interrupt pin. The driver can use this information to determine priority and vector information. Values in this field are system architecture specific.

Table 8-24 lists the access rules for the CFIT register.

Table 8-24. CFIT Register Access Rules

Category	Description
Value after hardware reset	281401XXH
Read access rules	—
Write access rules	—

8.2.2.12 Capability ID Register (CCID–Offset DCH)

The CCID register is a read-only register that provides information on the 21145 Ethernet Function power-management capabilities. Figure 8-14 shows the CCID register.

Figure 8-14. CCID Register Bit Fields

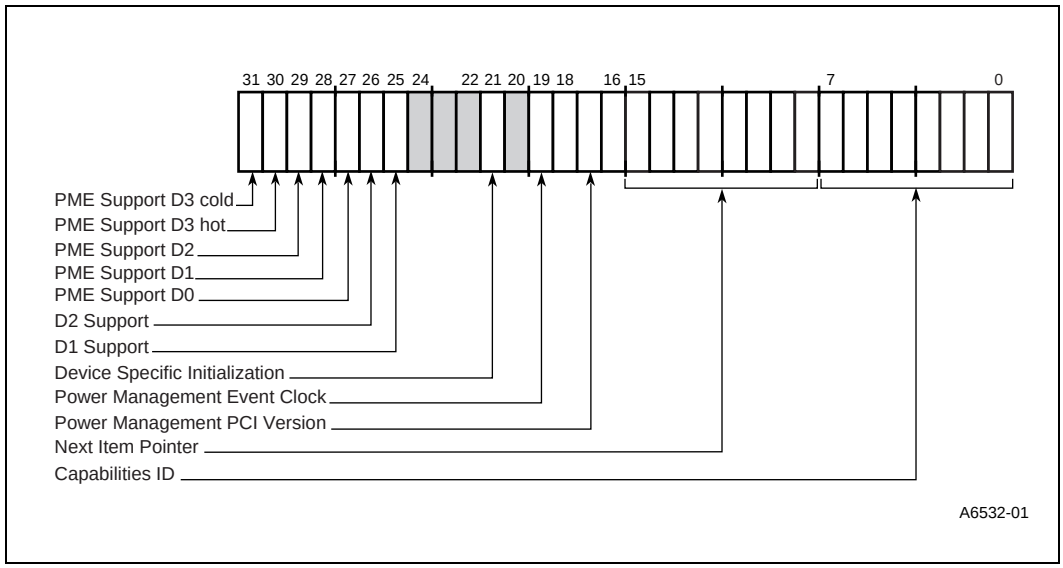


Table 8-25 describes the CCID register bit fields.

Table 8-25. CCID Register Bit Fields Description (Sheet 1 of 2)

Field	Description
31	PME Support $D3_{cold}$ If this bit is set, the 21145 asserts PME in $D3_{cold}$ power state. Otherwise, the 21145 does not assert PME in $D3_{cold}$. The value of this bit is loaded from Func0_HwOptions<6> bit in the serial ROM.
30	PME Support $D3_{hot}$ The value of this field is 1, indicating that the 21145 may assert PME in $D3_{hot}$ power state.
29	PME Support D2 The value of this field is 1, indicating that the 21145 may assert PME in D2 power state.
28	PME Support D1 The value of this field is 1, indicating that the 21145 may assert PME in D1 power state.
27	PME Support D0 The value of this field is 0, indicating that the 21145 does not assert PME in D0 power state.
26	D2 Support The value of this field is 1, indicating that the 21145 supports the D2 power state.
25	D1 Support The value of this field is 1, indicating that the 21145 supports the D1 power state.

Table 8-25. CCID Register Bit Fields Description (Sheet 2 of 2)

Field	Description
21	Device Specific Initialization The value of this field is 0, indicating that the 21145 does not require a special initialization code sequence in order to be configured correctly.
19	Power Management Event Clock The value of this field is 0, indicating that the 21145 does not rely on the presence of the CardBus clock in order to generate a PME.
18:16	Power Management PCI Version The value of this field is 001BH, indicating that the 21145 complies with the *PCI Bus Power Management Interface Specification,* Revision 1.0.
15:8	Next Item Pointer Points to the location of the next block of the capability list in the PCI Configuration Space. The value of this field is 00H, indicating that this is the last item of the Capability linked list.
7:0	Capabilities ID PCI Power Management Registers ID. The value of this field is 01h, indicating that this is the power-management register block.

Table 8-26 lists the access rules for the CCID register.

Table 8-26. CCID Register Access Rules

Category	Description
Value after reset	F6010001H[1]
Read access rules	—
Write access rules	Write has no effect on 21145.

NOTE:
1. According to Func0_HwOptions<6> (OnNowD3ColdCap) in the serial ROM.

8.2.2.13 Power-Management Control and Status Register (CPMC–Offset E0H)

The CPMC register is used to manage the 21145 Ethernet Function device power state, and to enable and monitor the 21145 power-management events.

Figure 8-15 shows the CPMC register.

Figure 8-15. CPMC Register Bit Fields

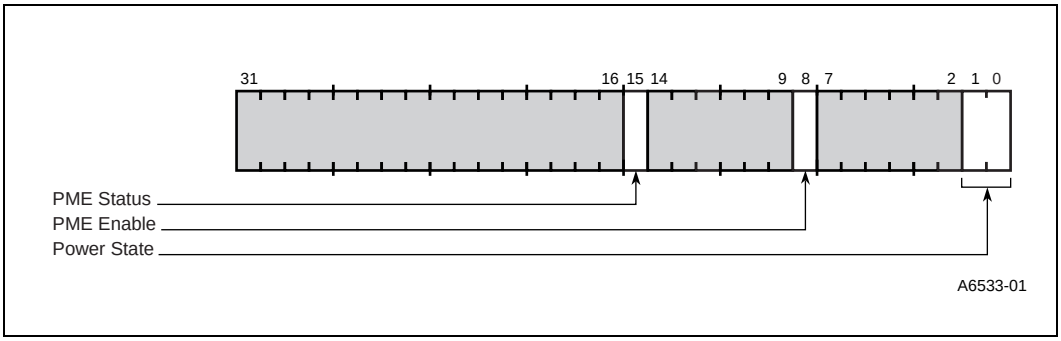


Table 8-27 describes the CPMC register bit fields.

Table 8-27. CPMC Register Bit Fields Description

Field	Description
15	PME_Status This bit indicates that the 21145 has detected a power-management event. If bit PME_Enable is set, the 21145 also asserts the gep<2>/rcv_match/wake pin. This bit may be cleared by writing 1 to it after the 21145 is placed in the D0 power state. When this bit is cleared, the 21145 deasserts the gep<2>/rcv_match/wake pin. Note: This bit is affected by General Enable bit of the Function Event Register (Function Event Register<4>); see Section 8.4.1. It is not modified by either hardware or software reset.
8	PME_Enable If this bit is set, the 21145 can assert the gep<2>/rcv_match/wake pin. Otherwise, assertion of the gep<2>/rcv_match/wake pin by the 21145 is disabled. This bit is cleared on power-up reset only and is not modified by either hardware or software reset.
1:0	Power State This field is used to set the current power state of the 21145 and to determine its power state. The definitions of the field values are: 0 - D0 1 - D1 2 - D2 3 - D3 This field gets a value of 0 after power-up. After this field is changed, at least 200 µs must elapse before it can be changed again.

Table 8-28 lists the access rules for the CPMC register.

Table 8-28. CPMC Register Access Rules

Category	Description
Value after reset	0000000XH
Read access rules	—
Write access rules	—

8.2.3 21145-Specific Configuration Registers

The 21145 implements six 21145-specific configuration registers. These registers are described in the following subsections.

8.2.3.1 Configuration Device and Driver Area Register (CFDD–Offset 40H)

The CFDD register can be used to store driver-specific information and to control the 21145 power-saving mode.

Figure 8-16 shows the CFDD register bit fields.

Figure 8-16. CFDD Register Bit Fields

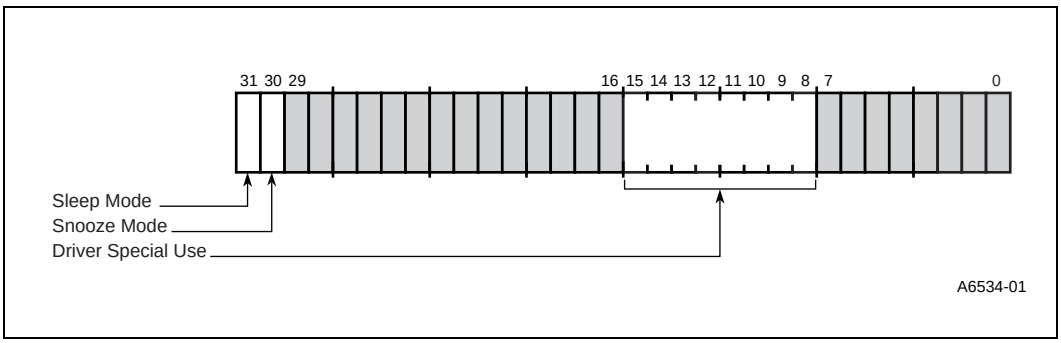


Table 8-29 describes the CFFD register bit.

Table 8-29. CFDD Register Bit Fields Description

Field	Description
31	Sleep Mode When this bit is set, the 21145 enters sleep mode and most of its internal clocks are disconnected. While in sleep mode, the 21145 must only be accessed through its configuration space. The 21145 also allows the clock to be stopped through clkrun while in sleep mode. The 21145 temporarily exits sleep mode upon hardware reset. When this bit is reset, a permanent exit from sleep mode is accomplished. Note that this bit must *not* be asserted together with bit 30 (snooze mode) in this register.
30	Snooze Mode When this bit is set, the 21145 enters snooze mode. In this mode, most of the clocks are disconnected when they are not needed. When the 21145 needs the clocks, it temporarily connects the clocks, until the event that caused the clocks to reconnect is completed. For more information, see Section 6.3.2. While in snooze mode, the 21145 allows the PCI/CardBus clock to be stopped through the CLKRUN mechanism, if it is not needed. When this bit is reset, the 21145 exits snooze mode. Note that this bit must *not* be asserted together with bit 31 (sleep mode) in this register.
15:8	Driver Special Use Specifies read and write fields for the driver's special use.

Table 8-30 lists the access rules for the CFDD register.

Table 8-30. CFDD Register Access Rules

Category	Description
Value after hardware reset	8000XX00H
Read access rules	—
Write access rules	—

8.3 Ethernet Function CSR Operation

The 21145 CSRs are mapped into the host I/O or the host memory address space. The CSRs are *quadword* aligned, 32 bits long, and must be accessed using *longword* instructions with quadword-aligned addresses only.

Note: All shaded bits in the figures are reserved. All reserved fields within non-reserved locations must be written by software as 0, and must be masked off when read; reserved register and memory locations must not be written to. Otherwise, unpredictable results will occur.

Retries on second data transactions occur in response to burst accesses.

CSRs are physically located in the chip. The host uses a single instruction to access a CSR.

All CSRs are set to default values by either a hardware or a software reset unless otherwise specified.

8.3.1 Control and Status Register Mapping

Table 8-31 lists the definitions and addresses for the CSR registers.

Table 8-31. CSR Mapping

Register	Meaning	Offset from CSR Base Address (CBIO and CBMA)
CSR0	Bus mode	00H
CSR1	Transmit poll demand	08H
CSR1-PM	Wake-up frame filter control	08H
CSR2	Receive poll demand	10H
CSR2-PM	Wake-up events control and status	10H
CSR3	Receive list base address	18H
CSR4	Transmit list base address	20H
CSR5	Status	28H
CSR6	Operation mode	30H
CSR7	Interrupt enable	38H
CSR8	Missed frames and overflow counter	40H
CSR9	Expansion ROM, serial ROM, and MII management	48H
CSR10	Expansion ROM programming address	50H
CSR11	General-purpose timer and interrupt mitigation control	58H
CSR12	SIA status	60H
CSR13	SIA connectivity	68H
CSR14	SIA transmit and receive	70H
CSR15	SIA and general-purpose port	78H

8.3.2 Ethernet Function Host CSRs

The 21145 implements 18 CSRs (CSR0 through CSR15, plus CSR1-PM and CSR2-PM), which can be accessed by the host.

8.3.2.1 Bus Mode Register (CSR0–Offset 00H)

CSR0 establishes the bus operating modes. Figure 8-17 shows the CSR0 bit fields.

Figure 8-17. CSR0 Bus Mode Register

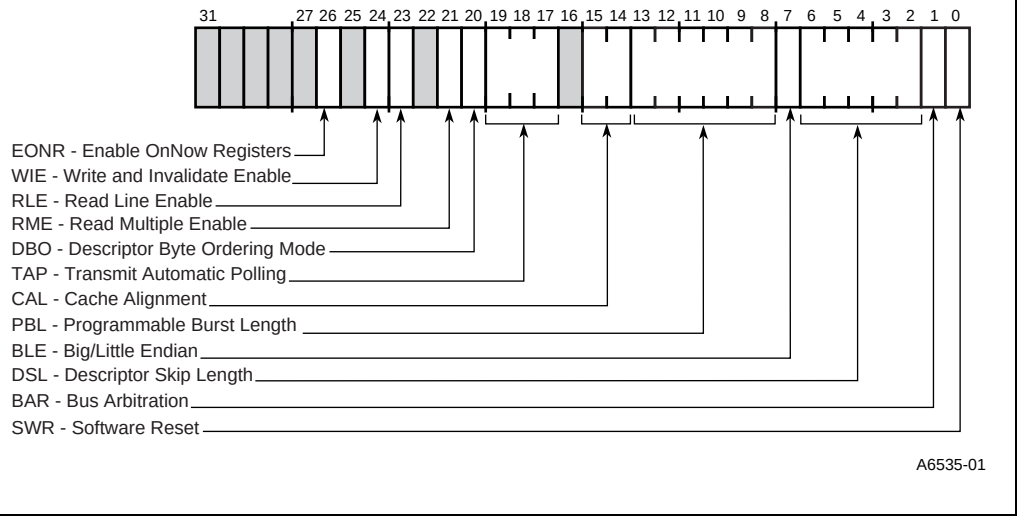


Table 8-32 describes the CSR0 bit fields.

Table 8-32. CSR0 Register Bit Fields Description (Sheet 1 of 2)

Field	Description
26	EONR—Enable OnNow Registers When set, CSR1-PM and CSR2-PM are accessible. When this bit is cleared, writing to these registers is interpreted as writing to CSR1 and CSR2 (receive/transmit poll demand). This bit is cleared upon hardware and software reset.
24	WIE—Write and Invalidate Enable When set, the 21145 supports the memory-write-and-invalidate command on the PCI bus. The 21145 uses the memory-write-and-invalidate command while writing full cache lines. While writing partial cache lines, the 21145 uses the memory-write command. Descriptors are also written using the memory-write command. When this field is reset, the memory-write command is used for write access. This bit is effective only if CFCS<4> is set.
23	RLE—Read Line Enable When set, the 21145 supports the memory-read-line command on the PCI bus. Read access instructions that reach the cache-line boundary use the memory-read-line command. Read access instructions that do not reach the cache-line boundary use the memory-read command. This field operates in conjunction with the read multiple enable (CSR0<21>) field.

Table 8-32. CSR0 Register Bit Fields Description (Sheet 2 of 2)

Field	Description
21	RME—Read Multiple Enable When set, the 21145 supports the memory-read-multiple command on the PCI bus. The 21145 uses the memory-read-multiple command while reading full cache lines. If the memory buffer is not cache aligned, the 21145 uses a memory-read command to read up to the cache line boundary. The 21145 then uses a memory-read-multiple command for reading an integer number of cache lines. If read line enable (CSR0<23>) is also set, the 21145 uses the memory-read-line command to align the memory buffer to the cache line. Read transactions that do not reach the cache line boundary use the memory-read command. The memory-read command is used to read descriptors.
20	DBO—Descriptor Byte Ordering Mode When set, the 21145 operates in big endian ordering mode for descriptors only. When reset, the 21145 operates in little endian mode.
19:17	TAP—Transmit Automatic Polling When set and the 21145 is in a suspended state because a transmit buffer is unavailable, the 21145 performs a transmit automatic poll demand (Table 8-33). This feature is not active in snooze mode.
15:14	CAL—Cache Alignment Programmable address boundaries for data burst stop (Table 8-35). If the buffer is not aligned, the 21145 executes the first transfer up to the address boundary. Then, all transfers are aligned to the specified boundary. When one or more of RLE, WIE or RME are set, this field should be equal to the system cache line size (CFLT<7:0>).
13:8	PBL—Programmable Burst Length Indicates the maximum number of longwords to be transferred in one DMA transaction. If reset, the 21145 burst is limited only by the amount of data stored in the receive FIFO (at least 16 longwords), or by the amount of free space in the transmit FIFO (at least 16 longwords) before issuing a bus request. When one or more of RLE, WIE or RME are set, the PBL should be greater than or equal to CAL(CSR0<15:14>). The PBL can be programmed with permissible values 0, 1, 2, 4, 8, 16, or 32. After reset, the PBL default value is 0.
7	BLE—Big/Little Endian When set, the 21145 operates in big endian byte ordering mode. When reset, the 21145 operates in little endian byte ordering mode. Big endian is only applicable for data buffers. For example, the byte order in little endian of a data buffer is 12345678H, with each digit representing a nibble. In big endian, the byte orientation is 78563412H.
6:2	DSL—Descriptor Skip Length Specifies the number of longwords to skip between two unchained descriptors. This is the size of the gap between the end of one descriptor and the beginning of the next.
1	BAR—Bus Arbitration Selects the internal bus arbitration between the receive and transmit processes. When set, a round-robin arbitration scheme is applied resulting in equal sharing between processes. When reset, the receive process has priority over the transmit process, unless the 21145 is currently transmitting (Section 2.3.5).
0	SWR—Software Reset When set, the 21145 resets all internal hardware with the exception of the configuration area; it does not change the port select setting (CSR6<18>).

Table 8-33 defines the transmit automatic polling bits and lists the automatic polling intervals for the different ports:

Table 8-33. Transmit Automatic Polling Intervals

	Polling Interval			
CSR0<19:17	10BASE-T	10 Mb/s MII	100 Mb/s MII/SYM	HomePNA[1]
000	TAP Disabled	TAP Disabled	TAP Disabled	
001	200 µs	800 µs	80 µs	200 µs – 200 ms
010	600 µs	2.4 ms	240 µs	600 µs – 600 ms
011	1.4 ms	5.6 ms	560 µs	1.4 ms – 200 ms
100	12.8 µs	51.2 µs	5.12 µs	12.8 µs – 12.8 ms
101	25.6 µs	102.4 µs	10.24 µs	25.6 µs – 25.6 ms
110	38.4 µs	153.6 µs	15.36 µs	38.4 µs – 38.4 ms
111	89.6 µs	358.4 µs	35.84 µs	89.6 µ – 89.6 ms

NOTE:
1. Note that in HomePNA, the interval varies between the values given.

Table 8-34 lists the access rules for the CSR0 register.

Table 8-34. CSR0 Access Rules

Category	Description
Value after reset	F8000000H
Read access rules	—
Write access rules	Before writing, the transmit and receive processes must be stopped; see Section 2.3.5.4 and Section 2.3.6.3. If one or both of the processes is not stopped, the result is **UNPREDICTABLE**.

Table 8-35 defines the cache address alignment bits.

Table 8-35. Cache Alignment Bits

CSR0<15:14>	Address Alignment
00	No cache alignment
01	8-longword boundary alignment
10	16-longword boundary alignment
11	32-longword boundary alignment

8.3.2.2 Transmit Poll Demand Register (CSR1–Offset 08H)

CSR1 is used by the driver to instruct the 21145 to poll the transmit descriptor list. Figure 8-18 shows the CSR1 register bit field and Table 8-36 describes the bit field.

Figure 8-18. CSR1 Register Bit Field

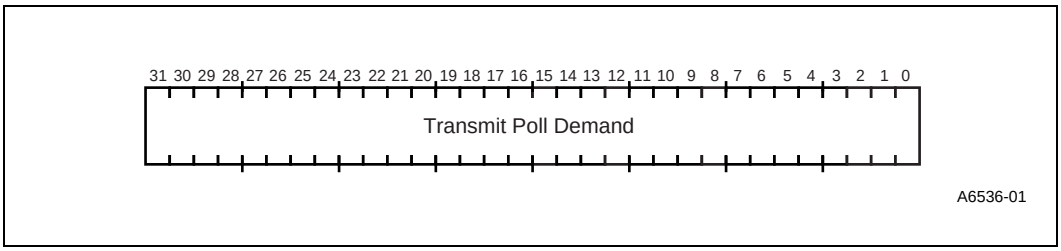


Table 8-36. CSR1 Register Bit Field Description

Field	Description
31:0	TPD–Transmit Poll Demand (Write Only) When written with any value, the 21145 checks for frames to be transmitted. If no descriptor is available, the transmit process returns to the suspended state and CSR5<2> is not asserted. If the descriptor is available, the transmit process resumes.

Table 8-37 lists the access rules for the CSR1 register.

Table 8-37. CSR1 Register Access Rules

Category	Description
Value after reset	FFFFFFFFH
Read access rules	—
Write access rules	This register can be written only when the CSR0<26> bit is cleared.

8.3.2.3 Wake-Up Frame Filter Register (CSR1-PM–Offset 08H)

This register is used for loading the wake-up frame filter register.

In order to load the wake-up frame filter register, CSR0<26> must be set and CSR1-PM must be written eight times.

The wake-up frame filter register is undefined after reset, except for the filter command that gets the value of 0. Figure 8-19 shows the CSR1-PM register bit field and Table 8-38 describes the bit field.

Figure 8-19. CSR1-PM Register Bit Field

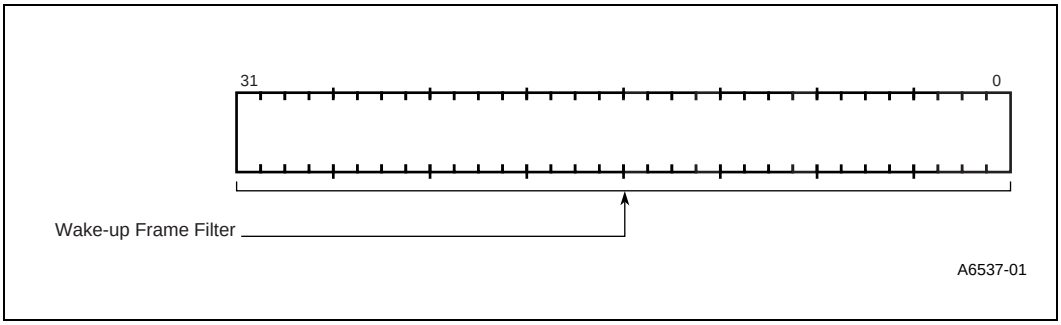


Table 8-38. CSR1-PM Register Bit Field Description

Field	Description
31:0	Wake-Up Frame Filter The first value written to this register, after CSR0<26> was set, is loaded by the 21145 to the first longword in the wake-up frame filter register (filter_0_byte_mask). The second value written to this register is loaded to the second longword in the wake-up frame filter register and so on.

Table 8-39 lists the access rules for the CSR1-PM register.

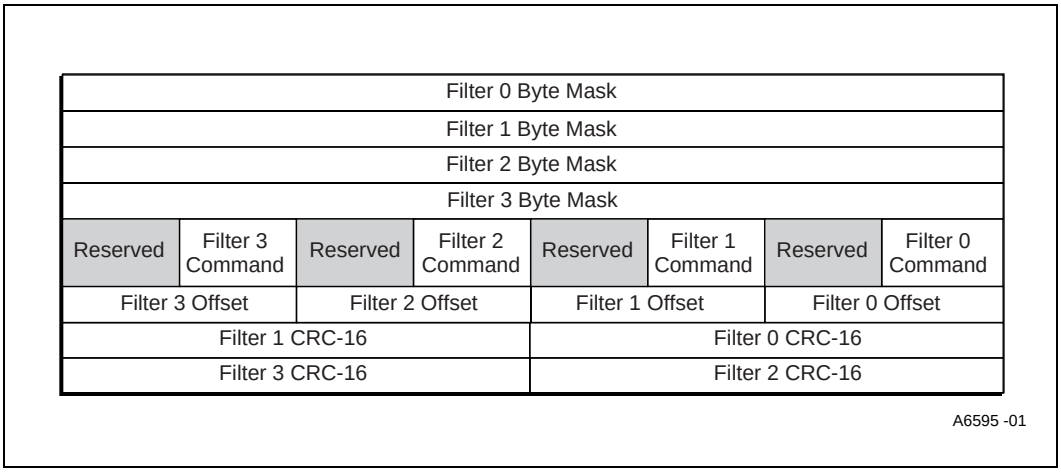
Table 8-39. CSR1-PM Register Access Rules

Category	Description
Value after reset	Undefined
Read access rules	This is a write-only register.
Write access rules	This register can be written only when the CSR0<26> bit is set.

8.3.2.4 Wake-Up Frame Filter Register

Figure 8-20 shows the wake-up frame filter register.

Figure 8-20. Wake-Up Frame Filter Register Structure



8.3.2.4.1 Filter i Byte Mask

This register defines which bytes of the incoming frames are examined by filter i in order to determine whether or not this is a wake-up frame. Figure 8-21 shows the filter i byte mask register and Table 8-40 describes the bit fields.

Figure 8-21. Filter i Byte Mask Bit Fields

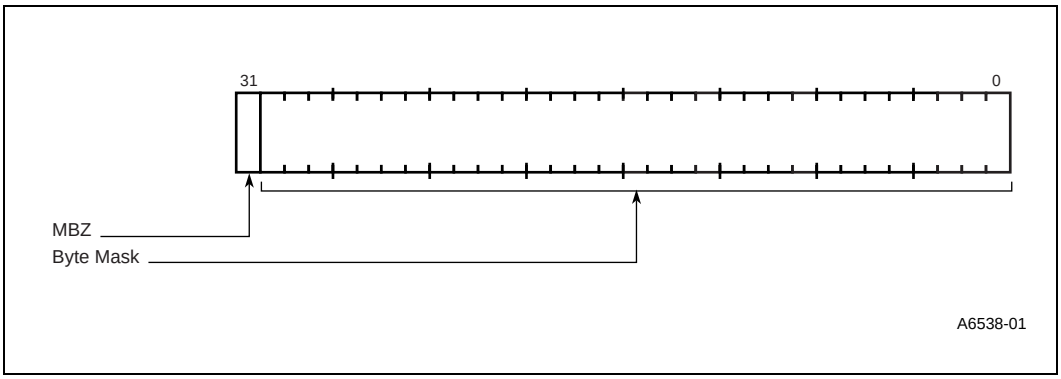


Table 8-40. Filter i Byte Mask Descriptions

Field	Description
31	MBZ This bit must be zero.
30:0	Byte Mask If bit number *j* of the byte mask is set, byte number *pattern-offset + j* of the incoming frame is processed by the CRC machine. Otherwise, byte *pattern-offset + j* is ignored. This field is not affected by either power-up, hardware, or software reset.

Table 8-41 lists the access rules for the filter i byte mask register.

Table 8-41. Filter i Byte Mask Register Access Rules

Category	Description
Value after reset	Undefined
Read access rules	This is a write-only register.
Write access rules	—

8.3.2.4.2 Filter i Command

This register controls the filter i operation. Figure 8-22 shows the filter i command register.

Figure 8-22. Filter i Command Bit Fields

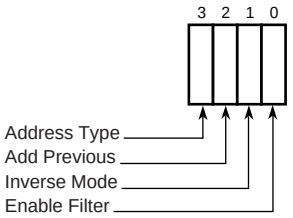


Table 8-42 describes the filter i command bit fields.

Table 8-42. Filter i Command Descriptions

Field	Description
3	Address Type Defines the destination address type of the pattern. When this bit is set, the pattern applies only to multicast frames. When this bit is cleared, the pattern applies only to unicast frames.
2	Add Previous When this bit is set, the 21145 performs a logical AND between the current filter matching signal and the matching signal of the previous filter. For the first filter, the 21145 chains the filter's matching signal with the result of the global unicast filter (CRS2-PM<9>).
1	Inverse Mode When this bit is set, the 21145 uses its match signal as a rejection signal. A frame that does not match this filter causes the 21145 to generate a power-management event.
0	Enable Filter When this bit is set, filter i is enabled, otherwise, filter i is disabled.

Table 8-43 lists the access rules for the filter i command register.

Table 8-43. Filter i Command Register Access Rules

Category	Description
Value after reset	00000000H
Read access rules	This is a write-only register.
Write access rules	—

8.3.2.4.3 Filter i Offset

This register defines the offset in the frame's destination address field from which the frames are examined by filter i. Figure 8-23 shows the filter i offset register and Table 8-44 describes the bit fields.

Figure 8-23. Filter i Offset Bit Fields

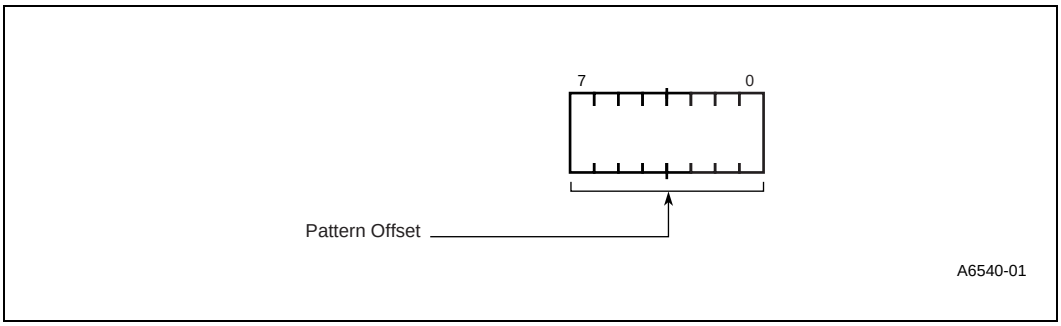


Table 8-44. Filter i Offset Descriptions

Field	Description
7:0	Pattern Offset The offset of the first byte in the frame that is examined by the 21145 in order to check if an incoming frame is a wake-up frame. Offset 0 is the first byte of the incoming frame's destination address. The minimum value allowed for this field is 12. This field is not affected by either power-up, hardware, or software reset.

Table 8-45 lists the access rules for the filter i offset register.

Table 8-45. Filter i Offset Register Access Rules

Category	Description
Value after reset	Undefined
Read access rules	This is a write-only register.
Write access rules	—

8.3.2.4.4 Filter i CRC-16

This register contains the CRC-16 result of a frame that should pass filter i. Figure 8-24 shows the filter i CRC-16 register and Table 8-46 describes the bit fields.

Figure 8-24. Filter i CRC-16 Bit Fields

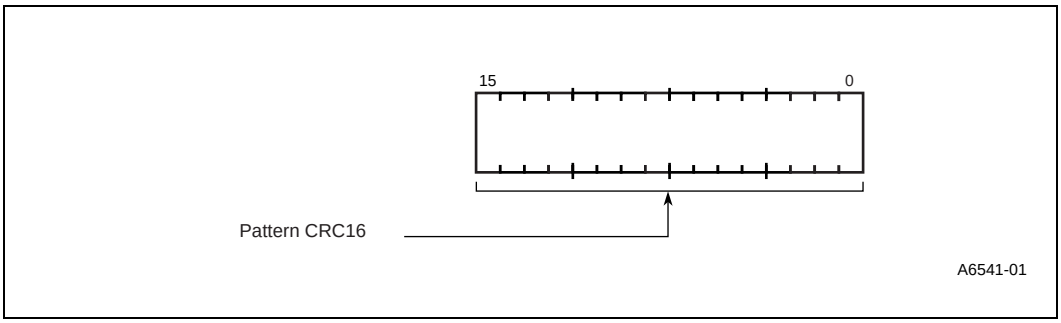


Table 8-46. Filter i CRC-16 Descriptions

Field	Description
15:0	Pattern CRC16 This field contains the 16-bit CRC value calculated from the pattern and the byte mask programmed to the wake-up filter register block. The 21145 compares the result of its CRC machine to this value in order to determine whether the frame is a wake-up frame. This field is not affected by either power-up, hardware, or software reset.

Table 8-47 lists the access rules for the filter i CRC-16 register.

Table 8-47. Filter i CRC-16 Register Access Rules

Category	Description
Value after reset	Undefined
Read access rules	This is a write-only register.
Write access rules	—

8.3.2.5 Receive Poll Demand Register (CSR2–Offset 10H)

CSR2 is used by the driver to instruct the 21145 to poll the receive descriptor list. Figure 8-25 shows the CSR2 bit field and Table 8-48 describes the bit field.

Figure 8-25. CSR2 Register Bit Field

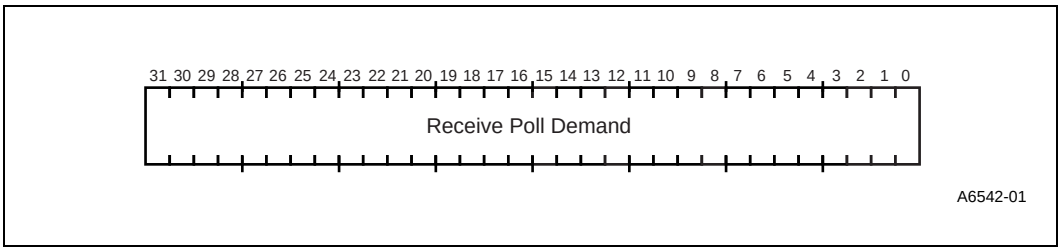


Table 8-48. CSR2 Register Bit Field Description

Field	Description
31:0	RPD–Receive Poll Demand (Write Only) When written with any value, the 21145 checks for receive descriptors to be acquired. If no descriptor is available, the receive process returns to the suspended state and CSR5<7> is set. If the descriptor is available, the receive process resumes.

Table 8-49 lists the access rules for the CSR2 register.

Table 8-49. CSR2 Register Access Rules

Category	Description
Value after reset	FFFFFFFFH
Read access rules	—
Write access rules	This register can be written only when the CSR0<26> bit is cleared.

8.3.2.6 Wake-Up Events Control and Status (CSR2-PM–Offset 10H)

This register is used for programming the requested wake-up events and the VLAN parameters, and monitoring the wake-up events.

In order to program the requested wake-up events and the VLAN parameters, CSR0<26> must be set. Figure 8-26 shows the CSR2-PM register bit field and Table 8-50 describes the bit field.

Figure 8-26. CSR2-PM Register Bit Field

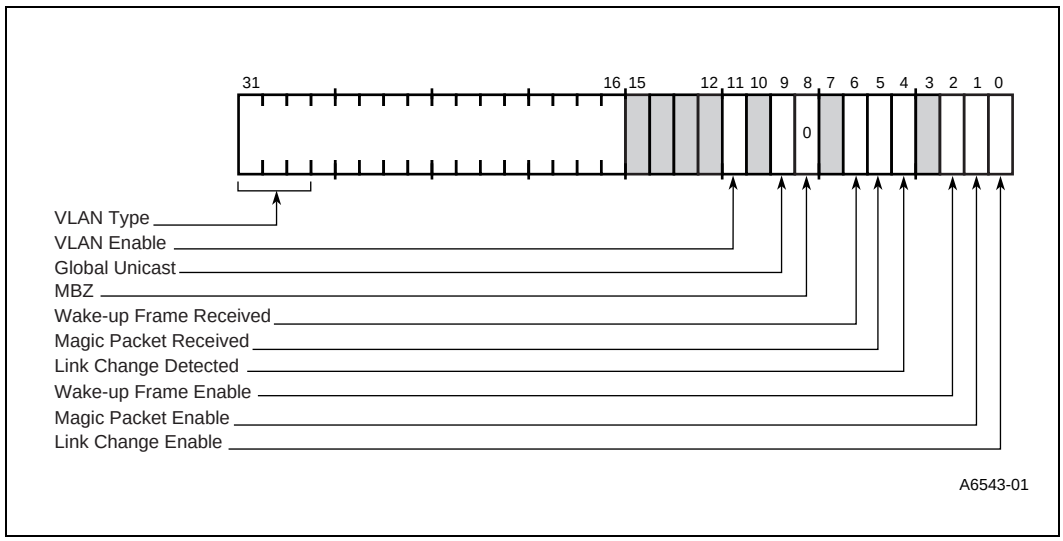


Table 8-50. CSR2-PM Register Bit Field Description

Field	Description
31:16	VLAN Type If VLAN Enable bit is set (CSR2-PM<11>), this field should be written with the VLAN type defined by the IEEE 802.1 standard.
11	VLAN Enable When set, enables the 21145's VLAN support. This field is reset upon hardware and software reset.
9	Global Unicast When set, enables any unicast packet filtered by the 21145 address recognition to be a wake-up frame.
8	MBZ This bit must be zero.
6	Wake-Up Frame Received If set, indicates that a power-management event was generated due to reception of a wake-up frame. This bit is cleared by write 1, or upon power-up reset. It is unaffected by either hardware or software reset.
5	Magic Packet Received If set, indicates that a power-management event was generated due to reception of a Magic Packet. This bit is cleared by write 1, or upon power-up reset. It is unaffected by either hardware or software reset.
4	Link Change Detected If set, indicates that a power-management event was generated due to link change. This bit is cleared by write 1, or upon power-up reset. It is unaffected by either hardware or software reset.
2	Wake-Up Frame Enable If set, enables generation of a power-management event due to reception of a wake-up frame.
1	Magic Packet Enable If set, enables generation of a power-management event due to Magic Packet reception
0	Link Change Enable If set, enables generation of a power-management event due to link change (not supported for the HomePNA port).

Table 8-51 lists the access rules for the CSR2-PM register.

Table 8-51. CSR2-PM Register Access Rules

Category	Description
Value after reset	Undefined
Read access rules	—
Write access rules	This register can be written only when the CSR0<26> bit is set.

8.3.2.7 Descriptor List Base Address Registers (CSR3–Offset 18H and CSR4–Offset 20H)

The CSR3 descriptor list base address register is used for receive buffer descriptors, and the CSR4 descriptor list base address register is used for transmit buffer descriptors. In both cases, the registers are used to point the 21145 to the start of the appropriate descriptor list.

Note: The descriptor lists reside in *physical* memory space and must be *longword* aligned. The 21145 behavior is **UNPREDICTABLE** when the lists are not longword aligned.

Figure 8-27 shows the CSR3 register bit field and Table 8-52 describes the bit field.

Writing to either CSR3 or CSR4 is permitted only when its respective process is in the stopped state. When stopped, the CSR3 and CSR4 registers must be written *before* the respective START command is given (Section 8.3.2.9).

Figure 8-27. CSR3 Register Bit Field

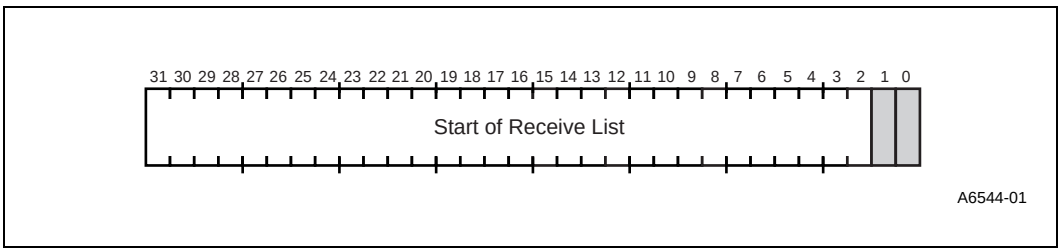


Table 8-52. CSR3 Register Bit Fields Description

Field	Description
31:2	Start of Receive List This field contains the base address of the first descriptor in the receive descriptor list.
1:0	Must be 00 for longword alignment.

Table 8-53 lists the access rules for the CSR3 register.

Table 8-53. CSR3 Register Access Rules

Category	Description
Value after reset	Undefined
Read access rules	—
Write access rules	Writing to this register is allowed only when the receive process is stopped.

Figure 8-28 shows the CSR4 register bit field and Table 8-54 describes the bit field.

Figure 8-28. CSR4 Register Bit Field

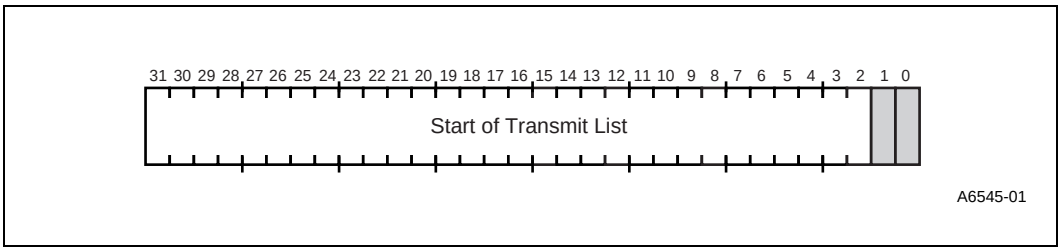


Table 8-54. CSR4 Register Bit Fields Description

Field	Description
31:2	Start of Transmit List This field contains the base address of the first descriptor in the transmit descriptor list.
1:0	Must be 00 for longword alignment.

Table 8-55 lists the access rules for the CSR4 register.

Table 8-55. CSR4 Register Access Rules

Category	Description
Value after reset	Undefined
Read access rules	—
Write access rules	Writing to this register is allowed only when the receive process is stopped.

8.3.2.8 Status Register (CSR5–Offset 28H)

The status register (CSR5) contains all the status bits that the 21145 reports to the host. CSR5 is usually read by the driver during interrupt service routine or polling. Most of the fields in this register cause the host to be interrupted. CSR5 bits are not cleared when read. Writing 1 to these bits clears them; writing 0 has no effect. Each field can be masked by setting the appropriate bit in CSR7 (see Section 8.3.2.10).

Figure 8-29 shows the CSR5 register bit fields.

Figure 8-29. CSR5 Register Bit Fields

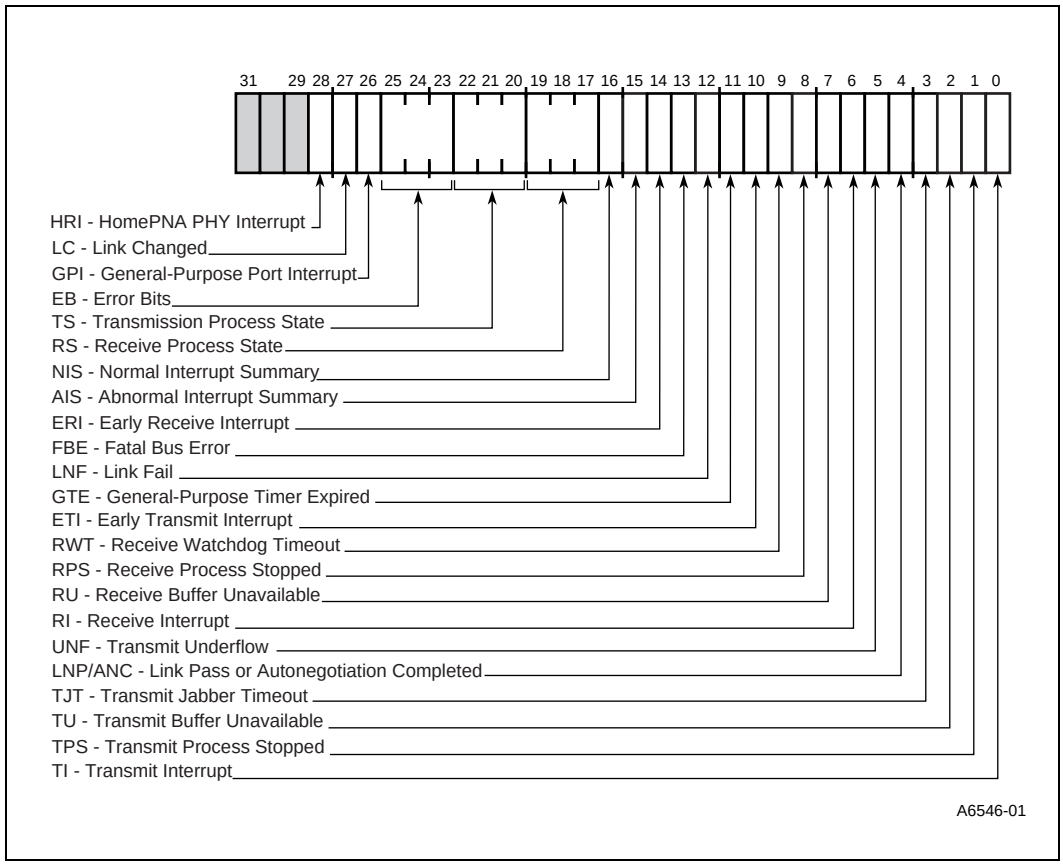


Table 8-56 describes the CSR5 register bit fields.

Table 8-56. CSR5 Register Bit Fields Description (Sheet 1 of 3)

Field	Description
28	HRI—HomePNA PHY Interrupt Indicates an interrupt event from the HomePNA PHY. For a description of the possible interrupt events, and to selectively mask which events cause the HRI bit to be set, see sections 8.5.3.3 and 8.5.3.4.
27	LC—Link Changed Indicates that the 100BASE-T link status has changed from link pass to link fail or from link fail to link pass. The new status can be read from CSR12<1>, 100BASE-T link status.
26	GPI—General-Purpose Port Interrupt Indicates an interrupt from the general-purpose port. The value of this bit is the logical *OR* of: CSR15<30>—Receive match interrupt CSR15<29>—General-purpose port interrupt 1 CSR15<28>—General-purpose port interrupt 0 Only unmasked bits affect the value of the general-purpose port CSR5<26> bit.
25:23	EB—Error Bits (Read Only) Indicates the type of error that caused bus error. Valid only when fatal bus error CSR5<13> is set (Table 8-57). This field does not generate an interrupt.
22:20	TS—Transmission Process State (Read Only) Indicates the state of the transmit process (Table 8-58). This field does not generate an interrupt.
19:17	RS—Receive Process State (Read Only) Indicates the state of the receive process (Table 8-59). This field does not generate an interrupt.
16	NIS—Normal Interrupt Summary Normal interrupt summary bit. Its value is the logical *OR* of: CSR5<0>—Transmit interrupt CSR5<2>—Transmit buffer unavailable CSR5<6>—Receive interrupt CSR5<11>—General-purpose timer and interrupt mitigation control CSR5<14>—Early receive interrupt Only unmasked bits affect the normal interrupt summary CSR5<16> bit.

Table 8-56. CSR5 Register Bit Fields Description (Sheet 2 of 3)

Field	Description
15	AIS—Abnormal Interrupt Summary Abnormal interrupt summary bits. Its value is the logical *OR* of: CSR5<1>—Transmit process stopped CSR5<3>—Transmit jabber timeout CSR5<4>—Link pass or autonegotiation completed CSR5<5>—Transmit underflow CSR5<7>—Receive buffer unavailable CSR5<8>—Receive process stopped CSR5<9>—Receive watchdog timeout CSR5<10>—Early transmit interrupt CSR5<12>—Link fail CSR5<13>—Fatal bus error CSR5<26>—General-purpose port interrupt CSR5<27>—Link changed CSR5<28>—HomePNA Interrupt Only unmasked bits affect the abnormal interrupt summary CSR5<15> bit. The transmit interrupt (CSR5<0>) automatically clears the early transmit interrupt (CSR5<10>). To keep the int_l pin asserted when there are early transmit interrupts with the transmit interrupt masked, the abnormal interrupt summary bit should remain set after the early transmit interrupt is cleared. To clear the abnormal interrupt summary bit in this case, the early transmit interrupt bit should be written with a value of 1.
14	ERI—Early Receive Interrupt Indicates that the 21145 has filled the first data buffer of the packet. Receive interrupt (CSR5<6>) automatically clears this bit.
13	FBE—Fatal Bus Error Indicates that a bus error occurred (Table 8-57). When this bit is set, the 21145 disables all of its bus access operations.
12	LNF—Link Fail Indicates a transition to the link fail state in the twisted-pair port. See link fail status CSR12<2>. This bit is valid only when CSR6<18>, Port Select, is reset; CSR14<8>, Receive Squelch Enable, is set; and CSR13<3>, 10BASE-T or HomePNA, is 0 (10BASE-T mode). Link pass CSR5<4> automatically clears this bit.
11	GTE—General-Purpose Timer Expired Indicates that the general-purpose timer (CSR11) counter has expired. This timer is mainly used by the software driver.
10	ETI—Early Transmit Interrupt Indicates that the packet to be transmitted was fully transferred into the chip's internal transmit FIFOs. Transmit interrupt (CSR5<0>) automatically clears this bit, but the abnormal interrupt summary bit remains set if ETI was enabled.
9	RWT—Receive Watchdog Timeout This bit reflects the line status and indicates that the receive watchdog timer has expired while another node is still active on the network. In case of overflow, the long packets may not be received.
8	RPS—Receive Process Stopped Asserts when the receive process enters the stopped state.

Table 8-56. CSR5 Register Bit Fields Description (Sheet 3 of 3)

Field	Description
7	RU—Receive Buffer Unavailable Indicates that the next descriptor in the receive list is owned by the host and cannot be acquired by the 21145. The reception process is suspended. To resume processing receive descriptors, the host should change the ownership of the descriptor and issue a receive poll demand command. If no receive poll demand is issued, the reception process resumes when the next recognized incoming frame is received. CSR5<7> is set only when the previous receive descriptor was owned by the 21145.
6	RI—Receive Interrupt Indicates the completion of a frame reception. Specific frame status information has been posted in the descriptor. The reception process remains in the running state.
5	UNF—Transmit Underflow Indicates that the transmit FIFO had an underflow condition during the packet transmission. The transmit process is placed in the suspended state and underflow error TDES0<1> is set.
4	LNP/ANC—Link Pass or Autonegotiation Completed When autonegotiation is not enabled (CSR14<7>=0), this bit indicates that the 10BASE-T Link Integrity Test has completed successfully, after the link was down. This bit is also set as a result of writing 0 to CSR14<12>, Link Test Enable. When autonegotiation is enabled (CSR14<7>=1), this bit indicates that the autonegotiation has completed (CSR12<14:12>=5H). CSR12 should then be read for a link status report. This bit is valid only when port select (CSR6<18>) is reset, and receive squelch enable (CSR14<8>) is set. Link fail interrupt (CSR5<12>) automatically clears this bit.
3	TJT—Transmit Jabber Timeout Indicates that the transmit jabber timer expired, meaning that the 21145 transmitter had been excessively active. The transmission process is *aborted* and placed in the stopped state. This event causes the transmit jabber timeout TDES0<14> flag to be set.
2	TU—Transmit Buffer Unavailable Indicates that the next descriptor on the transmit list is owned by the host and cannot be acquired by the 21145. The transmission process is suspended. Table 2-14 explains the transmit process state transitions. To resume processing transmit descriptors, the host should change the ownership bit of the descriptor and then issue a transmit poll demand command, unless transmit automatic polling (Table 8-33) is enabled.
1	TPS—Transmit Process Stopped Sets when the transmit process enters the stopped state.
0	TI—Transmit Interrupt Indicates that a frame transmission was completed and TDES1<31> is set in the first descriptor of the frame.

Table 8-57 lists the bit codes for the fatal bus error bits.

Table 8-57. Fatal Bus Error Bits

CSR5<25:23>	Error Type
000	Parity error[1]
001	Master abort
010	Target abort
011	Reserved
1xx	Reserved

NOTE:
1. The only way to recover from a parity error is by issuing a software reset (CSR0<0>=1).

Table 8-58 lists the bit codes for the transmit process state.

Table 8-58. Transmit Process State

CSR5<22:20>	Process State
000	Stopped—RESET command or STOP COMMAND issued, or transmit jabber expired
001	Running—Fetching transmit descriptor
010	Running—Waiting for end of transmission
011	Running—Reading buffer from memory and queuing the data into the transmit FIFO
100	Reserved
101	Running—Setup packet
110	Suspended—Transmit FIFO underflow, or an unavailable transmit descriptor
111	Running—Closing transmit descriptor

Table 8-59 lists the bit codes for the receive process state.

Table 8-59. Receive Process State

CSR5<19:17>	Process State
000	Stopped—RESET or STOP RECEIVE command issued
001	Running—Fetching receive descriptor
010	Running—Checking for end of receive packet before prefetch of next descriptor
011	Running—Waiting for receive packet
100	Suspended—Unavailable receive buffer
101	Running—Closing receive descriptor
110	Running—Flushing the current frame from the receive FIFO because of unavailable receive buffer
111	Running—Queuing the receive frame from the receive FIFO into the receive buffer

Table 8-60 lists the access rules for the CSR5 register.

Table 8-60. CSR5 Register Access Rules

Category	Description
Value after reset	E0000000H
Read access rules	—
Write access rules	CSR5 bits 0 through 16, bit 26, and bit 27 are cleared by writing 1. Writing 0 to these bits has no effect. CSR5 bits 17 through 25 are read-only bits.

8.3.2.9 Operation Mode Register (CSR6–Offset 30H)

The operation mode register (CSR6) establishes the receive and transmit operating modes and commands. CSR6 should be the last CSR to be written as part of initialization. Figure 8-30 shows the CSR6 register bit fields.

Figure 8-30. CSR6 Register Bit Fields

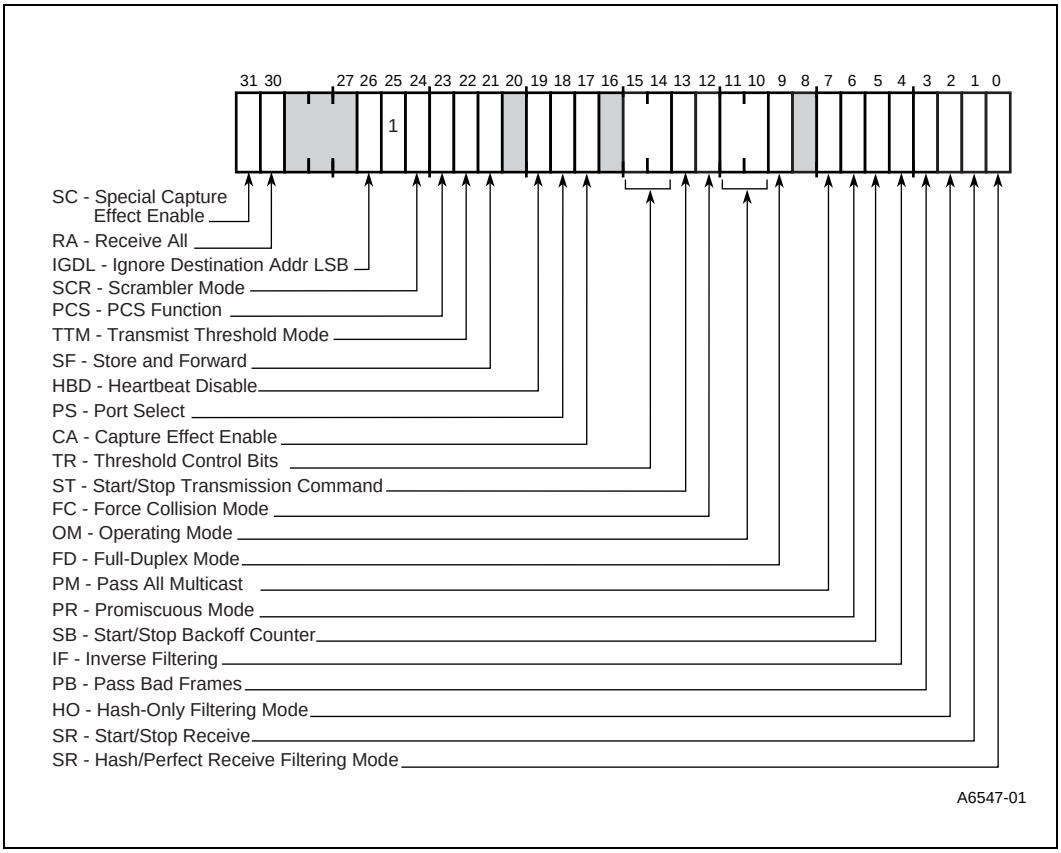


Table 8-61 describes the CSR6 register bit fields.

Table 8-61. CSR6 Register Bit Fields Description (Sheet 1 of 3)

Field	Description
31	SC—Special Capture Effect Enable When set, enables the enhanced resolution of capture effect on the network (Section 4.9.3). Intel recommends that this bit be set when CSR6<17> is set. When clear, the 21145 disables the enhanced resolution of capture effect on the network.
30	RA—Receive All When set, all incoming packets are received, regardless of the destination address. The address match is checked according to Table 8-65, and is reported in RDES0<30>.
26	IGDL—Ignore Destination Address LSB When set, the least significant bit of the destination address is ignored in the MAC's destination address filtering. This bit is meaningful only if the 21145 is programmed to do perfect address filtering. It is cleared upon hardware and software reset.
25	MBO—Must Be One This bit should always be programmed to one.
24	SCR—Scrambler Mode When set, the scrambler function is active and the MII/SYM port transmits and receives scrambled signals. This bit must be cleared when CSR6<23> bit is cleared. Changing this bit during operation may cause UNPREDICTABLE behavior.
23	PCS—PCS Function When set, the PCS functions are active and the MII/SYM port operates in symbol mode. The mii_rx_err/sel10_100 pin functions as the select 10/100 output pin. When reset, the PCS functions are not active, and the MII/SYM port operates in MII mode. The mii_rx_err/sel10_100 pin functions as the mii_rx_err input pin. Changing this bit during operation may cause UNPREDICTABLE behavior.
22	TTM—Transmit Threshold Mode Selects the transmit FIFO threshold to be either 10 Mb/s or 100 Mb/s (Table 8-62). When set, the threshold is 10 Mb/s. When reset, the threshold is 100 Mb/s. This bit can be changed only when the transmit process is in the stopped state.
21	SF—Store and Forward When set, transmission starts when a full packet resides in the FIFO. When this occurs, the threshold values specified in CSR6<15:14> are ignored. This bit can be changed only when the transmit process is in the stopped state.
19	HBD—Heartbeat Disable When set, the heartbeat signal quality (SQE) generator function is disabled. This bit should be set in the MII/SYM 100 Mb/s mode and HomePNA mode. In the MII 10 Mb/s mode this bit should be set according to the PHY device configuration.
18	PS—Port Select When reset, the 10BASE-T or HomePNA port is selected according to the CSR13<3> value. When set, the MII/SYM port is selected (Table 8-63). During a hardware reset, this bit automatically resets. A software reset does not affect this bit. In HomePNA mode, this bit can be changed only 200 µs after last change.
17	CA—Capture Effect Enable When set, enables the 21145 feature that solves the capture effect problem on the network (Section 4.9). When reset, this 21145 feature is disabled. In HomePNA or MII 10 Mb/s mode of operation, this bit is left cleared in filtering modes of Hash or Hash only mode

Table 8-61. CSR6 Register Bit Fields Description (Sheet 2 of 3)

Field	Description
15:14	TR—Threshold Control Bits Controls the selected threshold level for the 21145 transmit FIFO. The threshold value has a direct impact on the 21145 bus arbitration scheme (Section 2.3.2). Transmission starts when the frame size within the transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted. This bit can be changed only when the transmit process is in the stopped state.
13	ST—Start/Stop Transmission Command When set, the transmission process is placed in the running state, and the 21145 checks the transmit list at the *current* position for a frame to be transmitted. Descriptor acquisition is attempted either from the *current* position in the list, which is the transmit list base address set by CSR4, or from the position retained when the transmit process was previously stopped. If the current descriptor is not owned by the 21145, the transmission process enters the suspended state and transmit buffer unavailable (CSR5<2>) is set. The start transmission command is effective only when the transmission process is stopped. If the command is issued before setting CSR4, the 21145 behavior will be UNPREDICTABLE. When reset, the transmission process is placed in the stopped state after completing the transmission of the current frame. The next descriptor position in the transmit list is saved, and becomes the current position when transmission is restarted. The stop transmission command is effective only when the transmission process is in either the running or suspended state (Table 2-14). In HomePNA mode, the start command can only be issued at least 200 µs after the transmit process has stopped, see CSR5<1>.
12	FC—Force Collision Mode Allows the collision logic to be tested. Meaningful only in internal loopback mode. When set, a collision is forced during the next transmission attempt. This results in 16 transmission attempts with excessive collision reported in the transmit descriptor (TDES0<8>). In HomePNA mode, this bit can be changed only 200 µs after last change.
11:10	OM—Operating Mode Selects the 21145 loopback operation modes (Table 8-64). In HomePNA mode, this bit can be changed only 200 µs after last change.
9	FD—Full-Duplex Mode When autonegotiation is disabled (CSR14<7> = 0), this bit selects the 21145 half-duplex or full-duplex operation mode. A 0 selects half-duplex operation while a 1 selects full-duplex operation. When autonegotiation is enabled (CSR14<7> = 1) and the 21145 is operating in 10BASE-T mode (CSR6<18> = 0 and CSR13<3> = 0), this bit controls the advertisement of 10BASE-T full-duplex capability (bit 6) in the transmitted code word. The 21145 will operate in 10BASE-T full-duplex mode *only* if both link partners are advertising this bit set. This bit must be 0 in HomePNA mode (CSR6<18> = 0 and CSR13<3> = 1). Changing the full-duplex bit is permitted only if the transmit and receive processes are in the stopped state. While in full-duplex mode, heartbeat check is disabled, heartbeat fail (TDES0<7>) should be ignored, and internal loopback is not allowed. In HomePNA mode (CSR13<3> = 1 and CSR6<8> = 0), this bit should be set to 0.
7	PM—Pass All Multicast When set, indicates that all the incoming frames with a multicast destination address (first bit in the destination address field is 1) are received. Incoming frames with physical address destinations are filtered according to the CSR6<0> bit.
6	PR—Promiscuous Mode When set, indicates that any incoming valid frame is received, regardless of its destination address.

Table 8-61. CSR6 Register Bit Fields Description (Sheet 3 of 3)

Field	Description
5	SB—Start/Stop Backoff Counter When set, the internal backoff counter stops counting when any carrier activity is detected. The 21145 backoff counter resumes when the carrier drops. The earliest the 21145 starts its transmission after carrier deassertion is 9.6 µs for 10 Mb/s data rate, 0.96 µs for 100 Mb/s data rate, and 96 µs for HomePNA. This bit is effective only during the first seven retransmissions of a given packet. When reset, the internal backoff counter is not affected by the carrier activity.
4	IF—Inverse Filtering (Read Only) When set, the 21145 operates in an inverse filtering mode. This is valid only during perfect filtering mode (Table 8-65 and Table 2-8).
3	PB—Pass Bad Frames When set, the 21145 operates in pass bad frame mode. All incoming frames that passed the address filtering are received, including runt frames, collided fragments, or truncated frames caused by FIFO overflow. If any received bad frames are required, promiscuous mode (CSR6<6>) should be set to 1.
2	HO—Hash-Only Filtering Mode (Read Only) When set, and the 21145 is in the D0 power state, the device is in an imperfect address filtering mode for both physical and multicast addresses (Table 2-8).
1	SR—Start/Stop Receive When set, the receive process is placed in the running state. The 21145 attempts to acquire a descriptor from the receive list and processes incoming frames. Descriptor acquisition is attempted from the *current* position in the list, which is the address set by CSR3 or the position retained when the receive process was previously stopped. If no descriptor is owned by the 21145, the receive process enters the suspended state and receive buffer unavailable (CSR5<7>) is set. The start reception command is effective only when the reception process has stopped. If the command was issued before setting CSR3, the 21145 behavior is UNPREDICTABLE. When cleared, the receive process enters the stopped state after completing the reception of the current frame. The next descriptor position in the receive list is saved, and becomes the *current* position after the receive process is restarted. The stop reception command is effective only when the receive process is in running or suspended state (Table 2-13). In HomePNA mode, the start command can only be issued at least 200 µs after the receive process has stopped, see CSR5<8>.
0	HP—Hash/Perfect Receive Filtering Mode (Read Only) When reset, the 21145 does a perfect address filter of incoming frames according to the addresses specified in the setup frame (Table 2-8). When set, and the 21145 is in the D0 power state, the device does imperfect address filtering of multicast incoming frames according to the hash table specified in the setup frame. If CSR6<2> is set, then physical addresses are imperfect address filtered too. If CSR6<2> is reset, physical addresses are perfect address filtered, according to a single physical address, as specified in the setup frame.

Table 8-62 lists the threshold values in bytes.

Table 8-62. Transmit Threshold

CSR6<21>	CSR6<15:14>	CSR6<18> = 0 CSR6<22> = X	CSR6<18> = 1 CSR6<22> = 1	CSR6<18> = 1 CSR6<22> = 0
0	00	72	72	128
0	01	96	96	256
0	10	128	128	512
0	11	160	160	1024
1	XX	Store and forward	Store and forward	Store and forward

Table 8-63 lists the port and data rate selection.

Table 8-63. Port and Data Rate Selection

CSR6 <18>	CSR6 <22>	CSR6 <23>	CSR6 <24>	CSR13 <3>	Active Port	Data Rate	Function
0	0	X	X	1	HomePNA	1 Mb/s	HomePNA Interface
0	0	X	X	0	10BASE-T	10 Mb/s	10BASE-T interface
1	1	0	0	X	MII	10 Mb/s	MII with transmit FIFO thresholds appropriate for 10 Mb/s
1	0	0	0	X	MII/SYM	100 Mb/s	MII with transmit FIFO thresholds appropriate for 100 Mb/s
1	0	1	0	X	MII/SYM	100 Mb/s	PCS function for 100BASE-FX
1	0	1	1	X	MII/SYM	100 Mb/s	PCS and scrambler functions for 100BASE-TX

Table 8-64 selects the 21145 loopback operation modes.

Table 8-64. Loopback Operation Mode

CSR6<11:10>	Operation Mode
00	Normal
01	Internal loopback[1]
10	External loopback[2]

NOTES:
1. The selected port is placed in the internal loopback mode of operation. The PCS function (CSR6<23>) and the scrambler mode (CSR6<24>) are also tested. When the SYM port is in internal loopback mode, symbols appear on the network. When the MII port is in internal loopback mode, the signal mii_txen is disabled.
2. External loopback is not usable in HomePNA mode.

Table 8-65 lists the codes to determine the filtering mode.

Table 8-65. Filtering Mode

CSR6<7>	CSR6<6>	CSR6<4>	CSR6<2>	CSR6<0>	Filtering Mode
0	0	0	0	0	16 perfect filtering
0	0	0	0	1	512-bit hash + 1 perfect filtering. This mode is not available in the Ethernet function D1, D2 and D3 power states.
0	0	0	1	1	512-bit hash for multicast and physical addresses This mode is not available in the Ethernet function D1, D2 and D3 power states.
0	0	1	0	0	Inverse filtering
X	1	0	0	X	Promiscuous
0	1	0	1	1	Promiscuous
1	0	0	0	X	Pass all multicast
1	0	0	1	1	Pass all multicast

Note: When CSR6<30> is set (receive all mode), this table is used to generate the address match status reported in RDES0<30>.

Table 8-66 describes the only conditions that permit change to a field when modifying values to the CSR6 register.

Table 8-66. CSR6 Register Access Rules (Sheet 1 of 2)

Category	Description
Value after reset	32000040H
Read access rules	—
Write access rules	
* CSR6<22>	Receive and transmit processes stopped
* CSR6<21>	Receive and transmit processes stopped
* CSR6<17>	Receive and transmit processes stopped
* CSR6<16>	Receive and transmit processes stopped
* CSR6<15:14>	Transmit process stopped
* CSR6<12>	Receive and transmit processes stopped
* CSR6<11:10>	Receive and transmit processes stopped
* CSR6<9>	Receive and transmit processes stopped
* CSR6<8>	Transmit process stopped
* CSR6<5>	Receive and transmit processes stopped
* CSR6<3>	Receive process stopped
* Start_Transmit CSR6<13>=1	CSR4 initialized

Table 8-66. CSR6 Register Access Rules (Sheet 2 of 2)

Category	Description
* Stop_Transmit CSR6<13>=0	Transmit running or suspended
* Start_Receive CSR6<1>=1	CSR3 initialized
* Stop_Receive CSR6<1>=0	Receive running or suspended

8.3.2.10 Interrupt Enable Register (CSR7–Offset 38H)

The interrupt enable register (CSR7) enables the interrupts reported by CSR5 (Section 8.3.2.8). Setting a bit to 1 enables a corresponding interrupt. After a hardware or software reset, all interrupts are disabled. Figure 8-31 shows the CSR7 register bit fields.

Figure 8-31. CSR7 Register Bit Fields

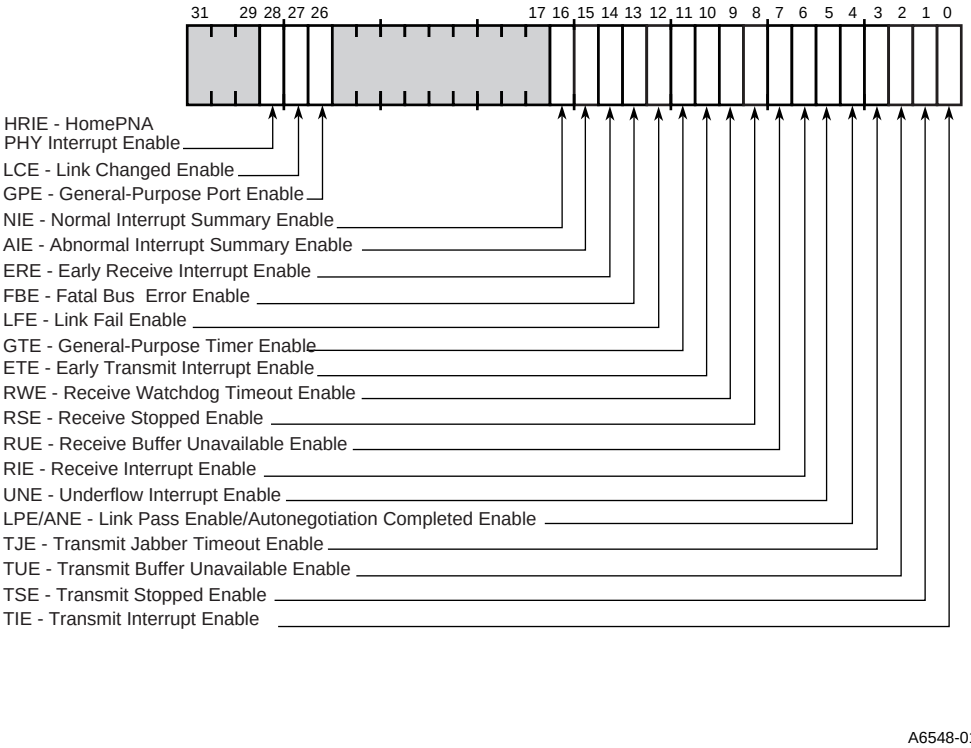


Table 8-67 describes the CSR7 register bit fields.

Table 8-67. CSR7 Register Bit Fields Description (Sheet 1 of 3)

Field	Description
28	HRIE—HomePNA PHY Interrupt Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the HomePNA PHY interrupt (CSR5<28>) is enabled. When this bit is reset, the HomePNA PHY interrupt (CSR5<28>) is disabled.
27	LCE—Link Changed Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the link changed interrupt (CSR5<27>) is enabled. When this bit is reset, the link changed interrupt (CSR5<27>) is disabled.
26	GPE—General-Purpose Port Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the general-purpose port interrupt (CSR5<26>) is enabled. When this bit is reset, the general-purpose port interrupt (CSR5<26>) is disabled.
16	NIE—Normal Interrupt Summary Enable When set, normal interrupt is enabled. When reset, no normal interrupt is enabled. This bit (CSR7<16>) enables the following bits: CSR5<0>—Transmit interrupt CSR5<2>—Transmit buffer unavailable CSR5<6>—Receive interrupt CSR5<11>—General-purpose timer expired CSR5<14>—Early receive interrupt
15	AIE—Abnormal Interrupt Summary Enable When set, abnormal interrupt is enabled. When reset, no abnormal interrupt is enabled. This bit (CSR7<15>) enables the following bits: CSR5<1>—Transmit process stopped CSR5<3>—Transmit jabber timeout CSR5<4>—Link pass or autonegotiation completed CSR5<5>—Transmit underflow CSR5<7>—Receive buffer unavailable CSR5<8>—Receive process stopped CSR5<9>—Receive watchdog timeout CSR5<10>—Early transmit interrupt CSR5<12>—Link fail CSR5<26>—General-purpose port interrupt CSR5<27>—Link changed CSR5<28>—HomePNA interrupt
14	ERE—Early Receive Interrupt Enable When this bit and the normal interrupt summary enable bit (CSR7<16>) are set, the early receive interrupt (CSR5<14>) is enabled. When this bit is reset, the early receive interrupt (CSR5<14>) is disabled.
13	FBE—Fatal Bus Error Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the fatal bus error interrupt (CSR5<13>) is enabled. When this bit is reset, the fatal bus error interrupt (CSR5<13>) is disabled.

Table 8-67. CSR7 Register Bit Fields Description (Sheet 2 of 3)

Field	Description
12	LFE—Link Fail Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the link fail interrupt (CSR5<12>) is enabled. When this bit is reset, the link fail interrupt (CSR5<12>) is disabled.
11	GTE—General-Purpose Timer and Interrupt Mitigation Control Enable When this bit and the normal interrupt summary enable bit (CSR7<16>) are set, the general-purpose timer and interrupt mitigation control expired interrupt (CSR5<11>) is enabled. When this bit is reset, the general-purpose timer and interrupt mitigation control expired interrupt (CSR5<11>) is disabled.
10	ETE—Early Transmit Interrupt Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the early transmit interrupt (CSR5<10>) is enabled. When this bit is reset, the early transmit interrupt (CSR5<10>) is disabled.
9	RWE—Receive Watchdog Timeout Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the receive watchdog timeout interrupt (CSR5<9>) is enabled. When this bit is reset, the receive watchdog timeout interrupt (CSR5<9>) is disabled.
8	RSE—Receive Stopped Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the receive stopped interrupt (CSR5<8>) is enabled. When this bit is reset, the receive stopped interrupt (CSR5<8>) is disabled.
7	RUE—Receive Buffer Unavailable Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the receive buffer unavailable interrupt (CSR5<7>) is enabled. When this bit is reset, the receive buffer unavailable interrupt (CSR5<7>) is disabled.
6	RIE—Receive Interrupt Enable When this bit and the normal interrupt summary enable bit (CSR7<16>) are set, the receive interrupt (CSR5<6>) is enabled. When this bit is reset, the receive interrupt (CSR5<6>) is disabled.
5	UNE—Underflow Interrupt Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the transmit underflow interrupt (CSR5<5>) is enabled. When this bit is reset, the transmit underflow bit (CSR5<5>) is disabled.
4	LPE/ANE—Link Pass Enable/Autonegotiation Completed Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the link pass/ autonegotiation completed interrupt (CSR5<4>) is enabled. When this bit is reset, the link pass/autonegotiation completed bit (CSR5<4>) is disabled.
3	TJE—Transmit Jabber Timeout Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the transmit jabber timeout interrupt (CSR5<3>) is enabled. When this bit is reset, the transmit jabber timeout interrupt (CSR5<3>) is disabled.

Table 8-67. CSR7 Register Bit Fields Description (Sheet 3 of 3)

Field	Description
2	TUE—Transmit Buffer Unavailable Enable When this bit and the normal interrupt summary enable bit (CSR7<16>) are set, the transmit buffer unavailable interrupt (CSR5<2>) is enabled. When this bit is reset, the transmit buffer unavailable interrupt (CSR5<2>) is disabled.
1	TSE—Transmit Stopped Enable When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the transmit process stopped interrupt (CSR5<1>) is enabled. When this bit is reset, the transmit process stopped interrupt (CSR5<1>) is disabled.
0	TIE—Transmit Interrupt Enable When this bit and the normal interrupt summary enable bit (CSR7<16>) are set, the transmit interrupt (CSR5<0>) is enabled. When this bit is reset, the transmit interrupt (CSR5<0>) is disabled.

Table 8-68 lists the access rules for the CSR7 register.

Table 8-68. CSR7 Register Access Rules

Category	Description
Value after reset	E3FE0000H
Read access rules	—
Write access rules	—

8.3.2.11 Missed Frames and Overflow Counter Register (CSR8–Offset 40H)

Figure 8-32 shows the CSR8 bit fields and Table 8-69 describes the bit fields.

Figure 8-32. CSR8 Missed Frames and Overflow Counter

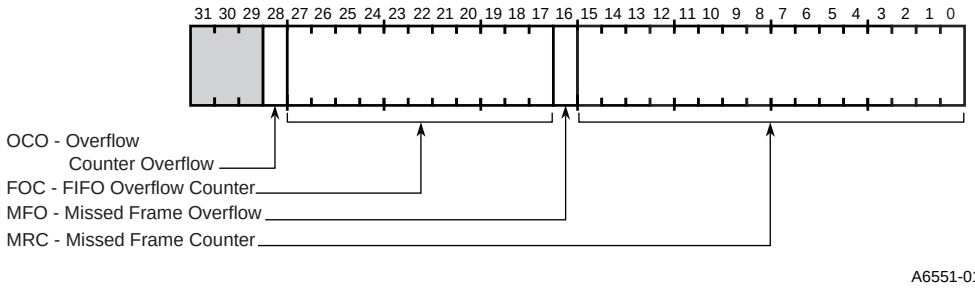


Table 8-69. CSR8 Register Bit Fields Description

Field	Description
28	OCO—Overflow Counter Overflow (Read Only) Sets when the FIFO overflow counter overflows; resets when CSR8 is read.
27:17	FOC—FIFO Overflow Counter (Read Only) Indicates the number of received frames discarded because of receive FIFO overflow. The counter clears when read. Packets longer than 4 KB are not counted.
16	MFO—Missed Frame Overflow (Read Only) Sets when the missed frame counter overflows; resets when CSR8 is read.
15:0	MFC—Missed Frame Counter (Read Only) Indicates the number of frames discarded because no host receive descriptors were available (CSR5<7>, RU – Receive Buffer Unavailable). The counter clears when read.

Table 8-70 lists the access rules for the CSR8 register.

Table 8-70. CSR8 Register Access Rules

Category	Description
Value after reset	E0000000H
Read access rules	—
Write access rules	This is a read-only register.

8.3.2.12 Expansion ROM, Serial ROM, MII Management and SPI Register (CSR9–Offset 48H)

The expansion ROM, serial ROM, MII management and SPI register (CSR9) provides an interface to the expansion ROM (176-pin 21145 only), serial ROM, MII management and HomePNA PHY internal registers. It selects the device and contains both the commands and data to be read from and stored in the expansion ROM and serial ROM. The MII management selects an operation mode for reading and writing the MII PHY registers through the MII management interface. The SPI is the interface to access the HomePNA PHY's internal registers.

Figure 8-33 shows the CSR9 register bit fields.

Figure 8-33. CSR9 Register Bit Fields

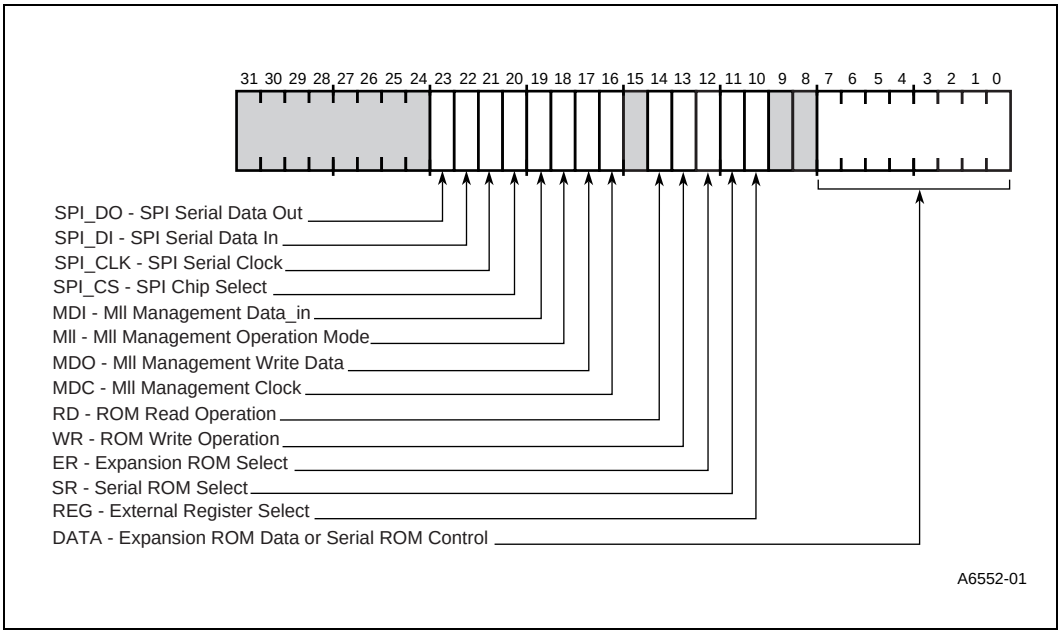


Table 8-71 describes the CSR9 register bit fields.

Table 8-71. CSR9 Register Bit Fields Description (Sheet 1 of 2)

Field	Description
23	SPI_DO – SPI Serial Data Out SPI_DO is the serial data output bit from the PHY. During a read cycle, data is shifted out from the PHY register into this bit. Data is clocked out by the falling edge of the serial clock.
22	SPI_DI – SPI Serial Data In SPI_DI is the serial data input bit to the PHY. All data, opcodes, byte addresses, and data to be written to the registers are inputted through this bit. Data is latched on the rising edge of the serial clock.
21	SPI_CLK – SPI Serial Clock The serial clock controls the serial interface timing for data input and output. Opcodes, addresses, or data present on the SPI_DI bit are sampled or latched on the rising edge of the SPI_CLK clock input, while data on the SPI_DO bit changes after the falling edge of the SPI_CLK clock input.

Table 8-71. CSR9 Register Bit Fields Description (Sheet 2 of 2)

Field	Description
20	SPI_CS – SPI Chip Select When SPI_CS bit is low, the SPI interface is deselected and the SPI_DO output bit is invalid. A low to high transition followed by a steady high on the SPI_CS bit enables a read or write function. Before any read or write operation, this bit should be set low to high and asserted high for the operation itself.
19	MDI—MII Management Data_In When reading the MII PHY registers, this bit samples the value driven by the PHY on the mii_mdio pin.
18	MII—MII Management Operation Mode Defines the operation mode (read or write) of the MII PHY registers. When set, the 21145 reads the MII PHY registers. The mii_mdio pin is sampled by the 21145 into the MII management data in (CSR9<19>) bit. When cleared, the 21145 writes to the MII PHY registers. The mii_mdio pin is driven by the 21145 with the MII management write data (CSR9<17>) bit.
17	MDO—MII Management Write Data When writing to the MII PHY device, the 21145 drives the value of this bit on the mii_mdio pin.
16	MDC—MII Management Clock The value of this bit is driven by the 21145 on the mii_mdc pin. This bit should be cleared at the end of each MII register access.
14	RD—ROM Read Operation Read control bit. When set, together with either CSR9<12>, CSR9<11>, or CSR9<10>, the 21145 performs read cycles from the selected target (expansion ROM, the serial ROM, or external register). Setting this bit together with CSR9<13> will cause UNPREDICTABLE behavior.
13	WR—ROM Write Operation Write control bit. When set, together with either CSR9<12>, CSR9<11>, or CSR9<10>, the 21145 performs write cycles to the selected target (expansion ROM, the serial ROM, or external register). Setting this bit together with CSR9<14> will cause UNPREDICTABLE behavior.
12	ER—Expansion ROM Select Valid only for the 176-pin 21145. When set, the 21145 selects the expansion ROM. Setting this bit together with CSR9<11> or CSR9<10> will cause UNPREDICTABLE behavior.
11	SR—Serial ROM Select When set, the 21145 selects the serial ROM. Setting this bit together with CSR9<12> or CSR9<10> will cause UNPREDICTABLE behavior.
10	REG—External Register Select When set, the 21145 selects an external register (Section 7.5). Setting this bit together with CSR9<12> or CSR9<11> will cause UNPREDICTABLE behavior.
7:0	DATA—Expansion ROM Data or Serial ROM Control If the expansion ROM is selected (176-pin 21145 only), this field contains the data to be read from and written to the expansion ROM. If the serial ROM is selected, CSR9<3:0> bits are connected to the serial ROM control pins as follows: Bit 3, Data Out—This bit samples the value driven by the serial ROM on the sr_do pin. Bit 2, Data In—The value of this bit is driven by the 21145 on the sr_di pin. Bit 1, Serial ROM Clock—The value of this bit is driven by the 21145 on the sr_ck pin. Bit 0, Serial ROM Chip Select—The value of this bit is driven by the 21145 on the sr_cs pin. If the external register is selected, this field contains the data to be read from and written to the external register. If CSR9<12> bit is set, this field is not affected by a software reset.

Table 8-72 lists the access rules for the CSR9 register.

Table 8-72. CSR9 Register Access Rules

Category	Description
Value after reset	FFX483FFH[1]
Read access rules	—
Write access rules	If the 21145 Modem Function is being used (176-pin 21145), there must be a delay of at least 20 PCI cycles between writing to any modem register and writing to CSR9.

NOTE:
1. CSR9<14:10> are not affected by software reset.

8.3.2.13 Expansion ROM Programming Address Register (CSR10–Offset 50H)

The expansion ROM programming address register (CSR10) contains the 18-bit expansion ROM address. This register is valid for the 176-pin 21145 only.

Figure 8-34 shows the CSR10 register bit field and Table 8-73 describes the bit field.

Figure 8-34. CSR10 Register Bit Field

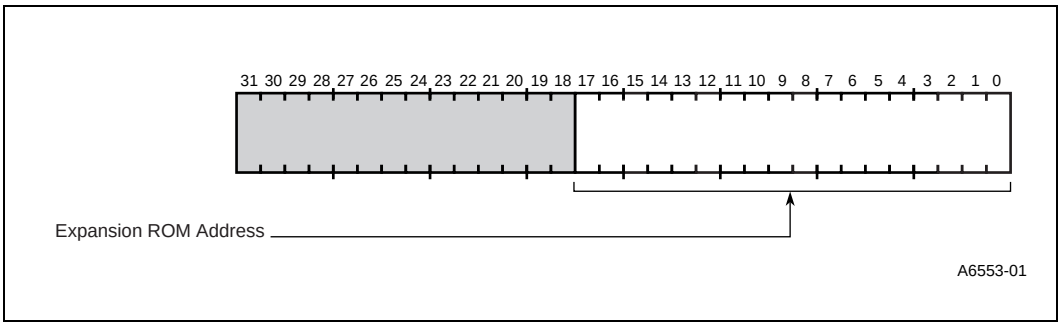


Table 8-73. CSR10 Register Bit Field Description

Field	Description
17:0	Expansion ROM Address Contains a pointer to the expansion ROM.

Table 8-74 lists the access rules for the CSR10 register.

Table 8-74. CSR10 Register Access Rules

Category	Description
Value after reset	Undefined
Read access rules	—
Write access rules	—

8.3.2.14 General-Purpose Timer and Interrupt Mitigation Control Register (CSR11–Offset 58H)

CSR11 controls the receive and transmit interrupt mitigation and contains a 16-bit general-purpose timer. The general-purpose timer is used mainly by the software driver for timing functions not supplied by the operating system. After this timer is loaded, it starts counting down. The expiration of the timer causes an interrupt in CSR5<11>. If the timer expires and the CON bit is set, the timer will load itself automatically with the last value loaded. The value that is read by the host in this register is the current count value. The timer reading accuracy is ±1 bit.

The timer operation is based on the existing serial clock. The cycle time of the timer depends on the port that is selected. The timer is not active in snooze mode (Section 6.3.2).

The interrupt mitigation mechanism allows the driver to reduce the number of receive and transmit interrupts, which reduces the CPU utilization for servicing a large number of interrupts. For more information about the interrupt mitigation mechanism, see Section 2.3.3.1.

In HomePNA mode, the cycle time is variable, so the general-purpose timer and mitigation mechanisms are not accurate in this mode.

Figure 8-35 shows the CSR11 register bit fields and Table 8-75 describes the bit fields.

Figure 8-35. CSR11 Register Bit Fields

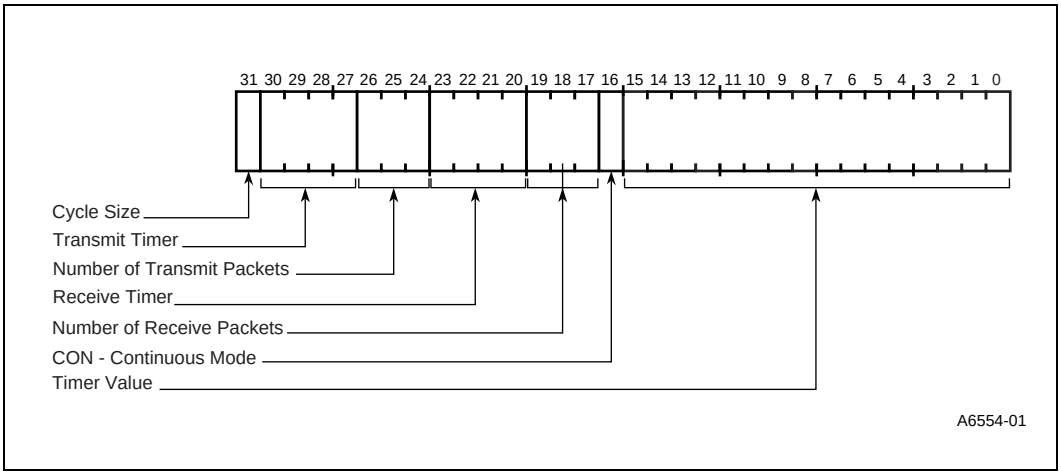


Table 8-75. CSR11 Register Bit Fields Description

Field	Description
31	Cycle Size This field controls the units for the transmit and receive timers. When set, the cycle size is: • 10BASE-T mode—12.8 µs • MII/SYM 100 Mb/s mode—5.12 µs • MII 10 Mb/s mode—51.2 µs • HomePNA mode—between 12.8 µs and 12.8 ms When cleared, the cycle size is: • 10BASE-T mode—204.8 µs • MII/SYM 100 Mb/s mode—81.92 µs • MII 10 Mb/s mode—819.2 µs • HomePNA mode—between 204.8 µs and 204.8 ms
30:27	Transmit Timer Indicates the time in units of “16 * Cycle Size” before issuing a transmit interrupt after packet transmission.
26:24	Number of Transmit Packets Indicates the number of transmit packets before issuing a transmit interrupt.
23:20	Receive Timer Indicates the time in units of “Cycle Size” before issuing a receive interrupt after packet reception.
19:17	Number of Receive Packets Indicates the number of receive packets before issuing a receive interrupt.
16	CON—Continuous Mode When set, the general-purpose timer is in continuous operating mode. When reset, the general-purpose timer is in one-shot operating mode.
15:0	Timer Value Contains the number of iterations of the general-purpose timer. Each iteration duration is the same as cycle duration when field <31> is cleared.

Table 8-76 lists the access rules for the CSR11 register.

Table 8-76. CSR11 Register Access Rules

Category	Description
Value after reset	00000000H
Read access rules	The values returned from this register’s fields are the current count values of the timers and counters.
Write access rules	—

8.3.2.15 SIA Status Register (CSR12–Offset 60H)

Figure 8-36 shows the CSR12 register bit fields.

Figure 8-36. CSR12 Register Bit Fields

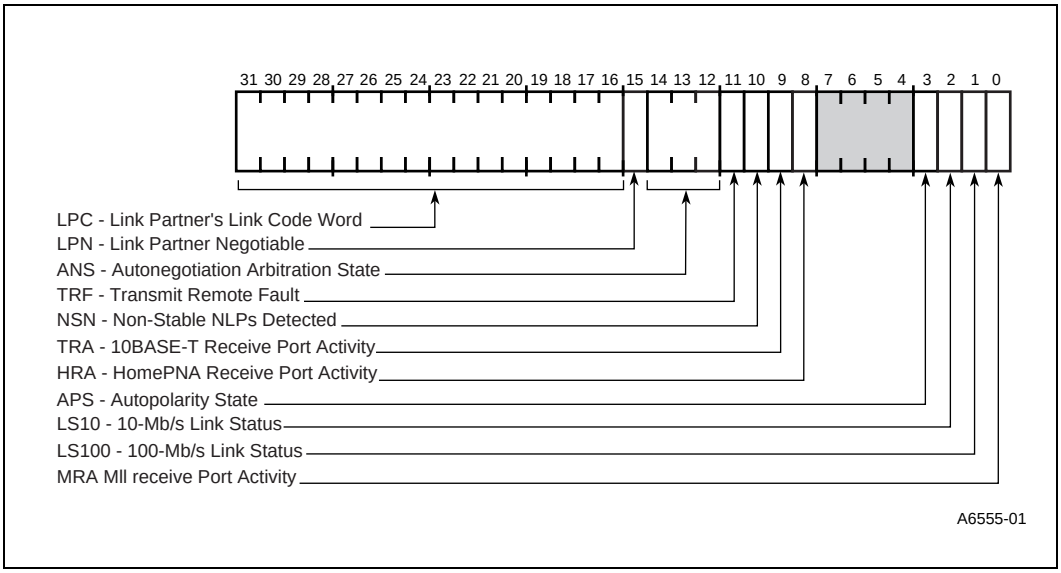


Table 8-77 describes the CSR12 register bit fields.

Table 8-77. CSR12 Register Bit Fields Description (Sheet 1 of 2)

Field	Description
31:16	LPC—Link Partner's Link Code Word These bits contain the link partner's link code word, where bit 16 is S0 (selector field bit 0) and bit 31 is NP (Next Page). Effective only when CSR12<15> is set.
15	LPN—Link Partner Negotiable This bit is set when the link partner is recognized to be a device that implements the autonegotiation algorithm. Effective only when CSR14<7> is set.
14:12	ANS—Autonegotiation Arbitration State The CSR12<14:12> bits reflect the current autonegotiation arbitration state as follows: 000—Autonegotiation disable 001—Transmit disable 010—Ability detect 011—Acknowledge detect 100—Complete acknowledge 101—FLP link good; autonegotiation complete 110—Link check When autonegotiation is completed, an ANC interrupt (CSR5<4>) is generated. These bits can also be used to restart the autonegotiation sequence. This is done by writing a pattern of 001 into this field, provided that autonegotiation enable (CSR14<7>) is set. Otherwise, these bits should be written as 0.
11	TRF—Transmit Remote Fault When set, the 21145 sets bit 13 (remote fault bit) in the transmitted link code words. This can be used to inform the link partner that some fault has occurred.

Table 8-77. CSR12 Register Bit Fields Description (Sheet 2 of 2)

Field	Description
10	NSN—Non-Stable NLPs Detected When set, indicates that the 10BASE-T normal link pulse (NLP) is not stable. The Link Integrity Test passed for a while, but failed later during negotiation. This means that NLPs were recognized on the line, but were not stable enough to cause autonegotiation completion. This bit is cleared by a read transaction. Effective only when CSR14<7> is set.
9	TRA—10BASE-T Receive Port Activity Sets when there is receive activity on the 10BASE-T port. This bit is valid only if port select CSR6<18> is reset. This bit is cleared by writing 1.
8	HRA—HomePNA Receive Port Activity Sets when there is receive activity on the HomePNA port. This bit is valid only if port select CSR6<18> is reset. This bit is cleared by writing 1.
3	APS—Autopolarity State When set, the 10BASE-T polarity is positive. When reset, the 10BASE-T polarity is negative. The received bit stream is inverted by the receiver. (Refer to autopolarity enable CSR14<13> and set polarity plus CSR14<14>).
2	LS10—10 Mb/s Link Status This bit continuously reflects the 10BASE-T link test status. When set, the 10BASE-T link test is in fail state. When reset, the 10BASE-T link test is in pass state. This bit is effective only in 10BASE-T mode, and only when CSR14<8>, Receive Squelch Enable, is set. During link fail, when in 10BASE-T mode, the 21145 does not transmit any packet to the media. A packet queued internally for transmission will not be processed and will be left pending. However, any queued packets in the transmit list can be closed by the 21145 with the following set: TDES0<2>—Link fail TDES0<10>—No carrier TDES0<11>—Loss of carrier During link fail, when in 10BASE-T mode, the 21145 does not receive any packet from the media. The 21145 moves from the link fail state to the link pass state when it receives a legal link pulse stream or two consecutive packets. These packets are discarded internally. When autonegotiation (CSR14<7>) is set, the LS10 bit is effective only if autonegotiation arbitration state (CSR12<14:12>) is 101 (autonegotiation completed).
1	LS100—100 Mb/s Link Status This bit continuously reflects the 100BASE-TX link test status. When set, the 100BASE-TX link test is in fail state. Any packets queued for transmission will be transmitted but not received by the link partner. When reset, the 100BASE-TX link test is in pass state. This status is derived from the sd pin and is effective only when CSR6<23> (PCS function) is set. This bit is effective regardless of the status of CSR6<18> (Port Select) and CSR14<7> (Autonegotiation Enable). When autonegotiation (CSR14<7>) is set, the LS100 bit is effective only if autonegotiation arbitration state (CSR12<14:12>) is 101 (autonegotiation completed).
0	MRA—MII Receive Port Activity This bit is set when there is receive activity on the MII port and the MII port is selected. This bit is cleared by writing 1.

Table 8-78 lists the access rules for the CSR12 register.

Table 8-78. CSR12 Register Access Rules

Category	Description
Value after reset	000000C6H
Read access rules	—
Write access rules	CSR12<0>, CSR12<8>, and CSR12<9> are cleared by writing 1. Writing 0 to these same bits has no effect. Writing to the remainder of the CSR12 bits (except bits 14:11) has no effect.

8.3.2.16 SIA Connectivity Register (CSR13–Offset 68H)

The SIA connectivity register (CSR13) contains the SIA connectivity control bits that permit the interconnection of different sections within the SIA. Figure 8-37 shows the CSR13 register bit fields, and Table 8-79 describes the bit fields.

Figure 8-37. CSR13 Register Bit Fields

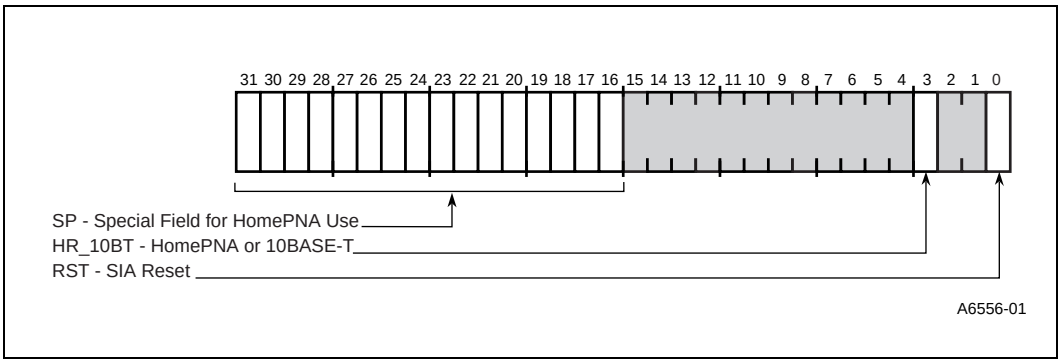


Table 8-79. CSR13 Register Bit Fields Description

Field	Description
31:16	SP—Special field for HomePNA use This field should be programmed according to Appendix C.4 only.
3	HR_10BT—HomePNA or 10BASE-T When reset, forces the 21145 to select the 10BASE-T interface. When set to 1, forces the 21145 to select the HomePNA interface.
0	RST—SIA Reset When reset, resets all the SIA functions and machines.

Table 8-80 lists the access rules for the CSR13 register.

Table 8-80. CSR13 Register Access Rules

Category	Description
Value after reset	00000000H
Read access rules	—
Write access rules	—

8.3.2.17 SIA Transmit and Receive Register (CSR14–Offset 70H)

The SIA transmit and receive register (CSR14) configures the SIA transmitter and receiver operating modes. Figure 8-38 shows the CSR14 register bit fields.

Figure 8-38. CSR14 Register Bit Fields

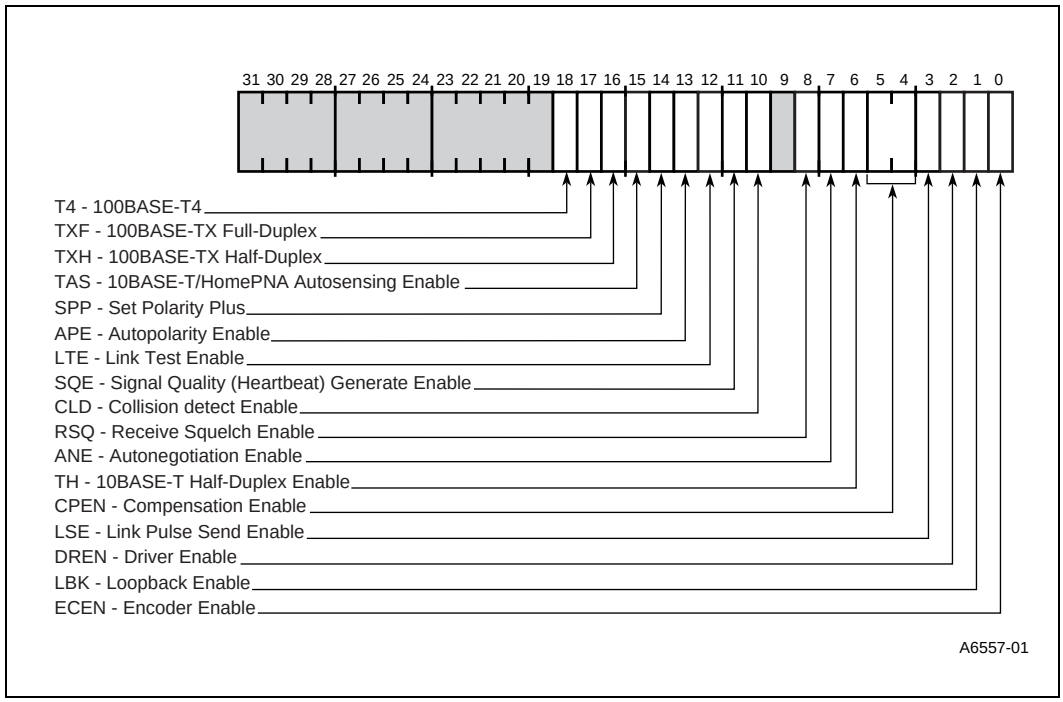


Table 8-81 describes the bit CSR14 register bit fields.

Table 8-81. CSR14 Register Bit Fields Description (Sheet 1 of 2)

Field	Description
18	T4—100BASE-T4 This bit controls the value of bit 9 in the transmitted auto-negotiation link code word. When set, the 21145 advertises its ability to work also in 100BASE-T4 mode. (Bit 9 in the auto-negotiation link code word is set.) When clear, the 21145 advertises that no 100BASE-T4 operation is allowed. (Bit 9 in the auto-negotiation link code word is cleared.) This bit is meaningful only if CSR14<7> is set.
17	TXF—100BASE-TX Full-Duplex This bit controls the value of bit 8 in the transmitted auto-negotiation link code word. When set, the 21145 advertises its ability to work also in 100BASE-TX full-duplex mode. (Bit 8 in the auto-negotiation link code word is set.) When clear, the 21145 advertises that no 100BASE-TX full-duplex operation is allowed. (Bit 8 in the auto-negotiation link code word is cleared.) This bit is meaningful only if CSR14<7> is set.
16	TXH—100BASE-TX Half-Duplex This bit controls the value of bit 7 in the transmitted auto-negotiation link code word. When set, the 21145 advertises its ability to work also in 100BASE-TX half-duplex mode. (Bit 7 in the auto-negotiation link code word is set.) When clear, the 21145 advertises that no 100BASE-TX half-duplex operation is allowed. (Bit 7 in the auto-negotiation link code word is clear.) This bit is meaningful only if CSR14<7> is set.
15	TAS—10BASE-T/HomePNA Autosensing Enable When set, the 21145 monitors its 10BASE-T and HomePNA ports. The selected port operation is not affected. See Section 4.5. When cleared, the 21145 monitors only the port that is selected for operation HomePNA or 10BASE-T according to CSR13<3>.
14	SPP—Set Polarity Plus When reset and autopolarity enable (CSR14<13>) is reset, the polarity of the incoming data is switched. This feature can be used by the driver to reverse polarity of incoming packets; otherwise, this bit should be set. This bit is valid only in 10BASE-T mode.
13	APE—Autopolarity Enable When set and link test enable CSR14<12> is also set, the autopolarity function logic is enabled (Section 4.2.5). When reset, the polarity is determined by set polarity plus (CSR14<14>). When link test enable (CSR14<12>) is reset, this bit (CSR14<13>) should be also reset. This bit is valid only in 10BASE-T mode.
12	LTE—Link Test Enable This bit is meaningful only for the 10BASE-T port. When set, the link test function logic is enabled. Resetting this bit forces the link test function to link pass state.
11	SQE—Signal Quality (Heartbeat) Generate Enable For 10BASE-T mode, SQE (CSR14<11>) should be set; otherwise, a heartbeat fail event (TDES0<7>) will occur. See also the description CSR6<19> in Section 8.3.2.9. For other modes, this bit should be cleared.
10	CLD—Collision Detect Enable When set, the collision detect logic is enabled.
8	RSQ—Receive Squelch Enable When set, the 10BASE-T receivers are active in accordance with the selected mode.

Table 8-81. CSR14 Register Bit Fields Description (Sheet 2 of 2)

Field	Description
7	ANE—Autonegotiation Enable When set, the 21145 performs an auto-negotiation with the link partner to determine the operation mode (Section 4.8). When reset, auto-negotiation is disabled. Auto-negotiation can be performed only when in 10BASE-T mode.
6	TH—10BASE-T Half-Duplex Enable This bit controls the value of bit 5 in the transmitted auto-negotiation link code word. When set, the 21145 advertises its ability to also work in 10BASE-T half-duplex mode. (Bit 5 in the auto-negotiation link code word is set.) When clear, the 21145 advertises that no 10BASE-T half-duplex operation is allowed. (Bit 5 in the auto-negotiation link code word is cleared.) 10BASE-T full-duplex ability advertisement (bit 6 in the transmitted auto-negotiation link code word) is controlled by CSR6<9> Full Duplex Mode. This bit is meaningful only if CSR14<7> is set.
5:4	CPEN—Compensation Enable Table 8-83 defines twisted-pair compensation behavior. These bits are valid only in 10BASE-T mode.
3	LSE—Link Pulse Send Enable This bit is meaningful only for the 10BASE-T port. When set, the link pulse generator is enabled.
2	DREN—Driver Enable When set, the transmit SIA driver is enabled for 10BASE-T operation. When reset, the transmit driver is disabled, preventing the data and link pulse transmission to the external wires.
1	LBK—Loopback Enable Enables loopback operation in SIA (see Table 8-86 to Table 8-90).
0	ECEN—Encoder Enable When set, the transmit data encoder is enabled, and the encoded data is transferred to the output drivers. When reset, the transmit data encoder is disabled, and the encoded data is blocked from propagating to the output drivers.

Table 8-82 lists the access rules for the CSR14 register.

Table 8-82. CSR14 Register Access Rules

Category	Description
Value after reset	FFFF7FFFH
Read access rules	—
Write access rules	—

Table 8-83 lists the compensation field (CSR14<5:4>) definitions.

Table 8-83. Twisted-Pair Compensation Behavior

CSR14<5:4> Value	Transmitter Output
00, 01	Compensation disabled mode—Twisted-pair driver does not compensate for 10 MHz versus 5 MHz media attenuation. (Differential voltages are bound between 1.5 V and 2.1 V.)
10	High power mode—Twisted-pair driver drives only high-differential voltage (between 2.2 V and 2.8 V).
11	Normal compensation mode—Driver compensates for 10 MHz versus 5 MHz media attenuation by driving high-differential voltage for transients and by driving low if the signal is stable for more than 50 ns.

8.3.2.18 SIA and General-Purpose Port Register (CSR15–Offset 78H)

Figure 8-39 shows the CSR15 register bit fields. CSR15 is divided into two sections: the SIA general register (CSR15<15:0>) and the general-purpose port register (CSR15<31:16>). Appendix D describes the general-purpose port programming procedures.

Figure 8-39. CSR15 Register Bit Fields

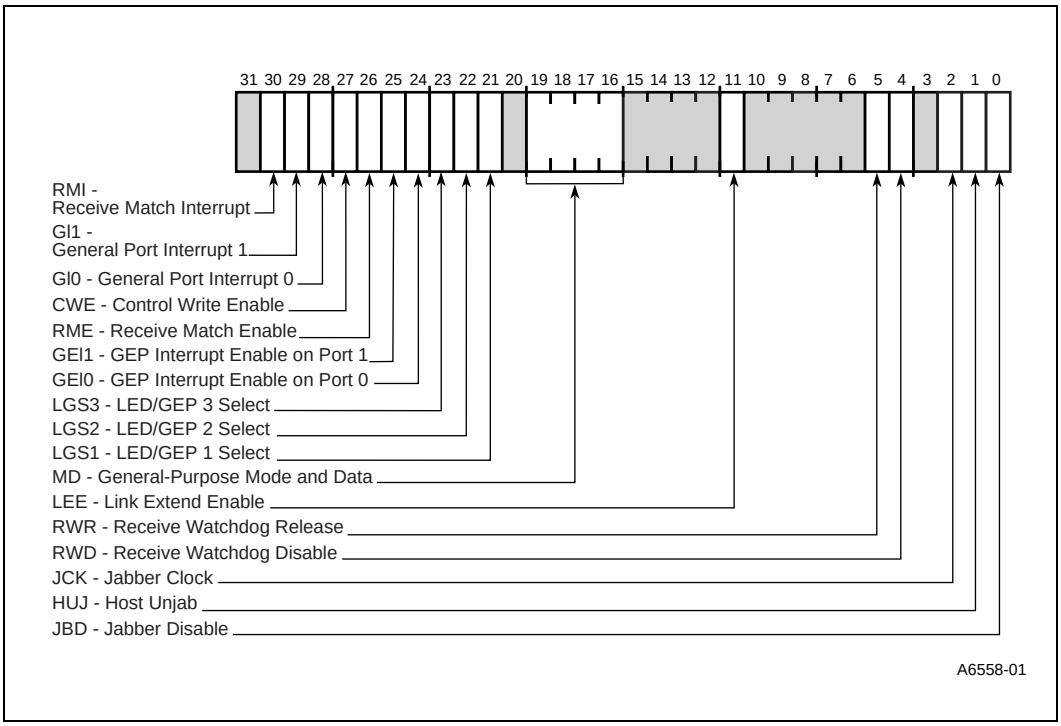


Table 8-84 describes the bit fields.

Table 8-84. CSR15 Register Bit Fields Description (Sheet 1 of 2)

Field	Description
30	RMI—Receive Match Interrupt Indicates that a packet has passed address filtering. When this bit is set and the receive match interrupt is enabled (CSR15<26>=1), the general-purpose port interrupt (CSR5<26>) is set. This bit is cleared when reading CSR15. This bit is not automatically cleared when general-purpose port interrupt (CSR5<26>) is cleared.
29	GI1—General Port Interrupt 1 Indicates that gep<1> has changed state. This bit is set only when gep<1> is programmed to be a general-purpose input port. When this bit is set and the general-purpose port interrupt is enabled (CSR15<24>=1), the general-purpose port interrupt (CSR5<26>) is set. This bit is cleared when reading CSR15. This bit is not automatically cleared when general-purpose port interrupt (CSR5<26>) is cleared.
28	GI0—General Port Interrupt 0 Indicates that gep<0> has changed state. This bit is set only when gep<0> is programmed to be a general-purpose input port. When this bit is set and the general-purpose port interrupt 0 is enabled (CSR15<24>=1), the general-purpose port interrupt (CSR5<26>) is set. This bit is cleared when reading CSR15. This bit is not automatically cleared when general-purpose port interrupt (CSR5<26>) is cleared.
27	CWE—Control Write Enable When CSR15 is written and CSR15<27> value is 1, the general-purpose control bits will be written. The general-purpose control bits include interrupt enables (CSR15<26:24>), LED/GEP selects (CSR15<23:20>), and general-purpose pin directions (CSR15<19:16>). When CSR15 is written and CSR15<27> value is 0, only general-purpose data (CSR15<19:16>) will be written.
26	RME—Receive Match Enable When this bit is set, receive match interrupt (CSR15<30>) is enabled. When this bit is reset, the interrupt is disabled. After a hardware or software reset, the interrupt is disabled.
25	GEI1—GEP Interrupt Enable on Port 1 When this bit is set, the interrupt from pin gep<1> (CSR15<29>) is enabled. When this bit is reset, the interrupt is disabled. After a hardware or software reset, the interrupt is disabled.
24	GEI0—GEP Interrupt Enable on Port 0 When this bit is set, the interrupt from gep<0> (CSR15<28>) is enabled. When this bit is reset, the interrupt is disabled. After a hardware or software reset, the interrupt is disabled.
23	LGS3—LED/GEP 3 Select This bit selects either the LED or gep<3> function for 21145 pin number 103. When this bit is set, the LED function is selected that, according to MiscHwOptions<0> (Gep3LedDefinition) bit in the serial ROM, provides an LED indicating either: –Network link integrity state for 10BASE-T or 100BASE-TX. –Both network activity and network link integrity state. When this bit is reset, the gep<3> function is selected. If the pin was designated to be an input pin, it functions as an input link status pin for OnNow support. If the pin was designated to be an output pin, it functions as a general-purpose port that performs output functions. After a hardware or software reset, the gep<3> function is selected.

Table 8-84. CSR15 Register Bit Fields Description (Sheet 2 of 2)

Field	Description
22	LGS2—LED/GEP 2 Select This bit selects either the rcv_match or gep<2> function for 21145 pin number 102. When this bit is set, the rcv_match function is selected, which provides a LED indicating the status of the address recognition (sets when a packet passes address recognition). When this bit is reset, the gep<2> function is selected. The gep<2> pin is a general-purpose port. After a hardware or software reset, the gep<2> function is selected.
21	LGS1—LED/GEP 1 Select This bit selects either the activ or gep<1> function for 21145 pin number 101. When this bit is set, the activ function is selected, which provides a LED indicating receive or transmit activity on the selected port (sets when there is receive or transmit activity on the selected port). When this bit is reset, the gep<1> function is selected. The gep<1> pin is a general-purpose port. After a hardware or software reset, the gep<1> function is selected.
19:16	MD—General-Purpose Mode and Data When CSR15<27> is set, the value that is written by the host to CSR15<19:16> directs pins gep<3:0> to act as input or output pins (CSR15<19> controls pin gep<3> and so on). A 1 directs the pin to be an output while a 0 directs the pin to be an input. The value that is driven by a gep pin that was directed to be an output is cleared when CSR15<27> is set. When CSR15<27> is reset, the values written to CSR15<19:16> are the values that will be driven on pins gep<3:0>, respectively. This is only true for the pins that are configured as output pins. After the 21145 is reset, all gep pins become input pins. If gep<1:0> pins are selected as input pins, an interrupt occurs when either of these bits change state from 1 to 0 or 0 to 1 (provided that the interrupt CSR15<25:24> is enabled). The application of the general-purpose pins in board design should be correlated with the way the port driver software is using it. Reading CSR15<19:16> returns the values of pins gep<3:0>.
11	LEE—Link Extend Enable When set, the 21145 reports link detection on its 100BASE-TX symbol port only if its sd pin (117) is asserted for at least 1.2 ms. When cleared, the 21145 reports link detection on its 100BASE-TX symbol port only if its sd pin (117) is asserted for at least 330 µs.
5	RWR—Receive Watchdog Release Defines the time interval from receive watchdog expiration until reenabling the receive channel (*no carrier)*. When set, the receive watchdog is released 40- to 48-bit-times from the last carrier deassertion. When reset, the receive watchdog is released 16- to 24-bit-times from the last carrier deassertion.
4	RWD—Receive Watchdog Disable When set, the receive watchdog counter is disabled. When cleared: If the 21145 is in Normal Power-Saving mode, receive carriers longer than 2560 bytes are guaranteed to cause the watchdog counter to timeout. Packets shorter than 2048 bytes are guaranteed to pass. If the 21145 is in Snooze mode, the counter will expire for receive carriers between 1792 and 2304 bytes and longer. The RWD bit must be set in HomePNA mode.
2	JCK—Jabber Clock When set, transmission is cut after 2048 bytes to 2560 bytes are transmitted. When clear, transmission is cut after 325000 byte times to 412500 byte times.
1	HUJ—Host Unjab Defines the time interval between transmit jabber expiration until reenabling of the transmit channel. When set, the transmit channel is released immediately after the jabber expiration. When reset, the transmit jabber is released 365 ms to 420 ms after jabber expiration at a 10 Mb/s line speed, 36.5 ms to 42.0 ms after jabber expiration at a 100 Mb/s line speed, and 148.2 ms to 194.7 ms for HomePNA.
0	JBD—Jabber Disable When set, the transmit jabber function is disabled.

Table 8-85 lists the access rules for the CSR15 register.

Table 8-85. CSR15 Register Access Rules

Category	Description
Value after reset	8FFX0000H
Read access rules	CSR15<27:20> are write-only bits.
Write access rules	—

8.3.2.19 SIA and MII Operating Modes

Table 8-86 through Table 8-90 list the programming of the different operating modes in the 21145 using CSR6, CSR13, CSR14, and CSR15. The states of operating mode CSR6<11:10>, full-duplex mode CSR6<9>, and port select CSR6<18> are also identified. Appendix C describes the port selection procedure.

Table 8-86 describes the programming of MII/SYM operating modes.

Table 8-86. Programming MII/SYM Operating Modes

Mode	CSR13<15:0>	CSR14<15:0>	CSR6<PS,FD>	CSR6<OM>
Half-duplex	0000	0000	1,0	00
Full-duplex	0000	0000	1,1	00
Internal loopback	0000	0000	1,0	01
External loopback	0000	0000	1,0	10

Table 8-87 describes the programming for the 10BASE-T and HomePNA operating mode with autosensing disabled and autonegotiation disabled.

Table 8-87. Programming 10BASE-T and HomePNA Operating Modes with Autosensing Disabled and Autonegotiation Disabled

Mode	CSR13<15:0>	CSR14<15:0>	CSR15<4:0>	CSR6<PS,FD>	CSR6<OM>
10BASE-T forced to half-duplex	0001	7F3F	0	0,0	00
10BASE-T forced to full-duplex	0001	7F3D	0	0,1	00
10BASE-T internal loopback	0001	7A3F	0	0,0	10
10BASE-T external loopback	0001	7B3D	0	0,0	10
HomePNA	0009	0505	10H	0,0	00
Internal loopback in MAC level	0009	0000	0	0,0	01

Table 8-88 describes the programming of 10BASE-T operating modes with autosensing disabled and autonegotiation enabled.

Table 8-88. Programming 10BASE-T Operating Modes with Autosensing Disabled and Autonegotiation Enabled

Mode	CSR13<15:0>	CSR14<15:0>	CSR15<2:0>	CSR6<PS,FD>	CSR6<OM>
10BASE-T advertising half- and full-duplex	0001	7FFF	0	0,1	00
10BASE-T advertising full-duplex	0001	7FBF	0	0,1	00
10BASE-T advertising half-duplex	0001	7FFF	0	0,0	00

Table 8-89 describes the programming of 10BASE-T and HomePNA operating modes with autosensing enabled and autonegotiation disabled.

Table 8-89. Programming 10BASE-T, and HomePNA Operating Modes with Autosensing Enabled and Autonegotiation Disabled

Mode	CSR13<15:0>	CSR14<15:0>	CSR6<PS,FD>	CSR6<OM>
10BASE-T forced to half-duplex	0001	FF3F	0,0	00
10BASE-T forced to full-duplex	0001	FF3D	0,1	00
HomePNA	0009	F73D	0,0	00

Table 8-90 describes the programming of 10BASE-T and HomePNA operating modes with autosensing enabled and autonegotiation enabled.

Table 8-90. Programming 10BASE-T and HomePNA Operating Modes with Autosensing Enabled and Autonegotiation Enabled

Mode	CSR13<15:0>	CSR14<15:0>	CSR15<2:0>	CSR6<PS,FD>	CSR6<OM>
10BASE-T advertising half- and full-duplex on TP	0001	FFFF	0	0,1	00
10BASE-T advertising only full-duplex on TP	0001	FFBF	0	0,1	00
10BASE-T advertising only half-duplex on TP	0001	FFFF	0	0,0	00
HomePNA advertising half- and full-duplex on TP	0009	F7FD	6	0,1	00
Home Run advertising only full-duplex on TP	0009	F7BD	6	0,1	00
HomePNA advertising only half-duplex on TP	0009	F7FD	6	0,0	00

8.4 Ethernet Function CardBus Status Changed Registers

The 21145 Ethernet Function implements four Status Changed registers. The Status Changed registers are accessed by the CardBus system software; they are typically not accessed by the 21145 Ethernet driver. These registers are mapped only to the memory address space and not to the I/O address space.

These registers affect the operation of the 21145 only if both:

- Func0_HwOptions<7> bit (RealSTSCHG) in the serial ROM is set.
- The FER or the FEMR were accessed with a write operation after a power-up reset.

Otherwise, these registers are not valid and do not affect the behavior of the 21145.

Note: Reserved bits are shaded and should be written with 0. Failing to do this could cause incompatibility problems with a future version of the 21145. Reserved bits are undefined on read access.

Table 8-91 lists the definitions and addresses for the CardBus Status Changed registers.

Table 8-91. Ethernet Function CardBus Status Changed Register Mapping

Register	Meaning	Offset from Ethernet CSR Base Address (CBIO and CBMA)
FER	Function event register	80H
FEMR	Function event mask register	84H
FPSR	Function present state register	88H
FFER	Function force event register	8CH

8.4.1 Function Event Register (FER–Offset 80H)

This register is the CardBus Status Changed function event register, which is used for reporting of interrupt pending and power-management event detection in a CardBus system.

Figure 8-40 shows the FER register bit fields and Table 8-92 describes the bit fields.

Figure 8-40. FER Register Bit Fields

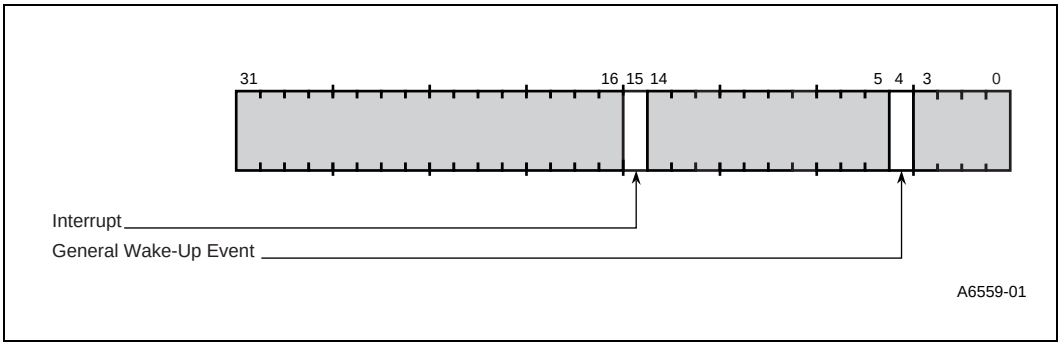


Table 8-92. FER Register Bit Fields Description

Field	Description
15	Interrupt This bit is set when there is an interrupt pending. This bit is cleared by write 1.
4	General Wake-Up Event This bit is set when the 21145 has detected a power management event. This bit is cleared upon power-up reset and by write 1. It is unaffected by either hardware or software reset. When the PME_Status bit in the Ethernet function PCI configuration is cleared, this bit is automatically cleared as well.

Table 8-93 lists the access rules for the FER register.

Table 8-93. FER Register Access Rules

Category	Description
Value after reset	Undefined for reserved bits; 0 for bits that are not reserved.
Read access rules	—
Write access rules	These register bits are cleared by writing 1; writing 0 has no effect.

8.4.2 Function Event Mask Register (FEMR–Offset 84H)

This register is the CardBus Status Changed function event mask register, which controls the assertion of the signals int_l and gep<2>/rcv_match/wake in a CardBus system.

Figure 8-41 shows the FEMR register bit fields and Table 8-94 describes the bit fields.

Figure 8-41. FEMR Register Bit Fields

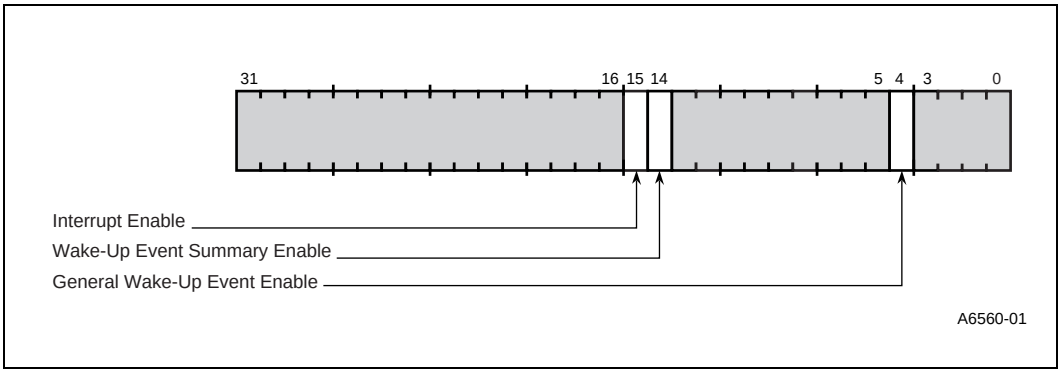


Table 8-94. FEMR Register Bit Fields Description

Field	Description
15	Interrupt Enable When set, enables the assertion of the interrupt pin (int_l).
14	Wake-Up Event Summary Enable When set together with the General Wake-Up Event Enable bit (FEMR<4>), enables the assertion of the gep<2>/rcv_match/wake pin. Note: To disable the assertion of the gep<2>/rcv_match/wake pin, the PME_Enable bit in the Ethernet function configuration register (CPMC<8>) must be cleared as well. This bit is cleared only upon a power-up reset.
4	General Wake-Up Event Enable When set together with the Wake-Up Event Summary Enable bit (FEMR<14>), enables the assertion of the gep<2>/rcv_match/wake pin. Note: To disable the assertion of the gep<2>/rcv_match/wake pin, the PME_Enable bit in the Ethernet function configuration register (CPMC<8>) must be cleared as well. This bit is cleared only upon a power-up reset.

Table 8-95 lists the access rules for the FEMR register.

Table 8-95. FEMR Register Access Rules

Category	Description
Value after reset	Undefined for reserved bits; 0 for bits that are not reserved.
Read access rules	—
Write access rules	These register bits are cleared by writing 1; writing 0 has no effect.

8.4.3 Function Present State Register (FPSR–Offset 88H)

This register is the CardBus Status Changed function present state register, which is used for reporting the present state of the int_l and the gep<2>/rcv_match/wake pins in a CardBus system.

Figure 8-42 shows the FPSR register bit fields and Table 8-96 describes the bit fields.

Figure 8-42. FPSR Register Bit Fields

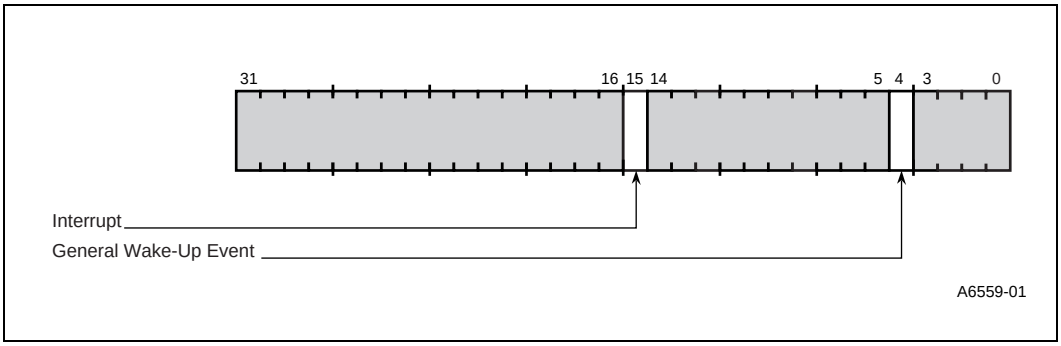


Table 8-96. FPSR Register Bit Fields Description

Field	Description
15	Interrupt This bit reflects the state of the interrupt line. It is set when all of the following conditions exist: –CSR5<15> is set or CSR5<16> is set. –The 21145 is in the D0 power state. –FEMR<15> is set or Func0_HwOptions<7> (RealSTSCHG) bit in the serial ROM is cleared.
4	General Wake-Up Event Reflects the current state of the wake-up event. This bit is cleared when either the General Wake-Up Event in the function event register is cleared, or when the PME_Status bit in the CPMC is cleared. This bit is cleared only upon a power-up reset.

Table 8-97 lists the access rules for the FPSR register.

Table 8-97. FPSR Register Access Rules

Category	Description
Value after reset	Undefined for reserved bits; 0 for bits that are not reserved.
Read access rules	—
Write access rules	This is a read-only register.

8.4.4 Function Force Event Register (FFER–Offset 8CH)

This register is the CardBus Status Changed function force event register, which is used to force the value of the interrupt and the general wake-up event bits in the function event register to a 1.

Figure 8-43 shows the FFER register bit fields and Table 8-98 describes the bit fields.

Figure 8-43. FFER Register Bit Fields

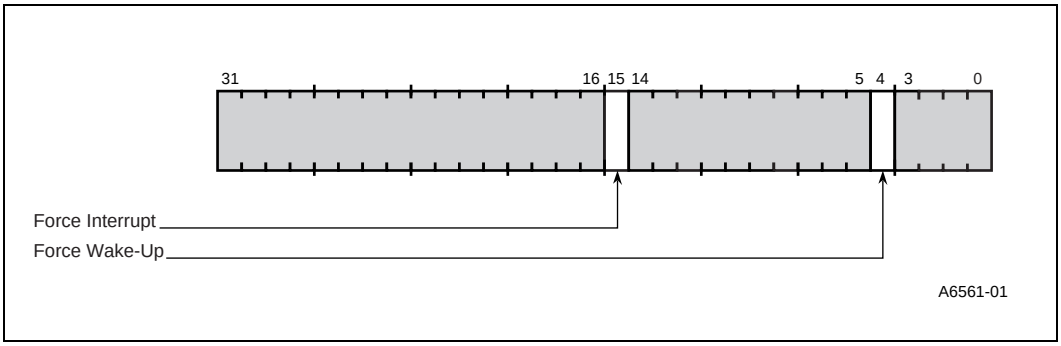


Table 8-98. FFER Register Bit Fields Description

Field	Description
15	Force Interrupt Writing 1 to this bit sets the Interrupt field in FER<15>, but not in FPSR<15>. If the interrupt is enabled, the 21145 also asserts the int_l pin. Writing 0 has no effect.
4	Force Wake-Up Writing 1 to this bit sets the wake-up event field in FER<4>, but not in FPSR<4>. If the wake-up event is enabled, the 21145 also asserts the gep<2>/rcv_match/wake pin. Writing 0 has no effect. This bit is cleared only upon a power-up reset.

Table 8-99 lists the access rules for the FFER register.

Table 8-99. FFER Register Access Rules

Category	Description
Value after reset	Undefined for reserved bits; 0 for bits that are not reserved.
Read access rules	This is a write-only register.
Write access rules	—

8.5 HomePNA PHY Internal Registers Interface

The interface is used for accessing the HomePNA PHY internal registers. It is equivalent to Tut Systems' SPI interface. This interface is controlled by four bits in CSR9, which are described in Table 8-71. For examples on how to use the interface, see Appendix G.

8.5.1 Principles of Operation

The interface contains an 8-bit instruction register. It is accessed via the SPI_DI input, with data being clocked in on the rising SPI_CLK. SPI_CS must remain high during the entire operation.

Table 8-100 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first. Data input is sampled on the first rising edge of SPI_CLK after SPI_CS goes high. SPI_CLK is static, allowing the user to stop the clock and then resume operations. The SET_WE (write enable) command must be issued before any write operations to the HomePNA PHY registers.

Table 8-100. SPI Interface Instruction Set

Instruction Name	Opcode[1]	Operation
SET_WE	0000 0110	Set the write latch (enable write).
CLEAR_WE	0000 0100	Clear the write latch (disable write) which is the default after reset.
READ	0000 0011	Read one data byte from PHY register, beginning at the selected address.
WRITE	0000 0010	Write one data byte to PHY register, beginning at the selected address.

NOTE:
1. Instructions are shown MSB in leftmost position. Opcodes are transferred MSB first.

8.5.2 Register Map

Table 8-101 lists each HomePNA PHY register name, meaning, and address offset.

Table 8-101. HomePNA PHY Register Map (Sheet 1 of 2)

Register	Meaning	I/O Address Offset
CONTROL	Control register	01H – 00H
STATUS	Status register	03H – 02H
IMASK (IMR)	Interrupt mask register	05H – 04H
ISTAT (ISR)	Interrupt status register	07H – 06H
TX_PCOM	Transmit PCOM register	0BH – 08H
RX_PCOM	Receive PCOM Register	0FH – 0CH
NOISE	Noise register	10H
PEAK	Peak level register	11H
NSE_FLOOR	Minimum noise level register	12H
NSE_CEILING	Maximum noise level register	13H

Table 8-101. HomePNA PHY Register Map (Sheet 2 of 2)

Register	Meaning	I/O Address Offset
NSE_ATTACK	Noise algorithm attack register	14H
NSE_EVENTS	Noise events register	15H
AID_ADDRESS	PHY AID collision detection register	19H
AID_INTERVAL	Access ID interval	1AH
AID_ISBI	AID inter symbol blanking interval	1BH
ISBI_SLOW	ISBI slow speed	1CH
ISBI_FAST	ISBI fast speed	1DH
TX_PULSE_WIDTH	Transmit pulse width	1EH
TX_PULSE_CYCLES	Transmit pulse cycle	1FH

8.5.3 HomePNA PHY Register Descriptions

The following sections describe the individual programmable registers.

8.5.3.1 Control Register (Address 01H – 00H)

The control register provides a common location for controlling the general operation of the HomePNA PHY. Figure 8-44 shows the control register bit fields and Table 8-103 describes the control register bit fields.

Figure 8-44. Control Register Bit Fields

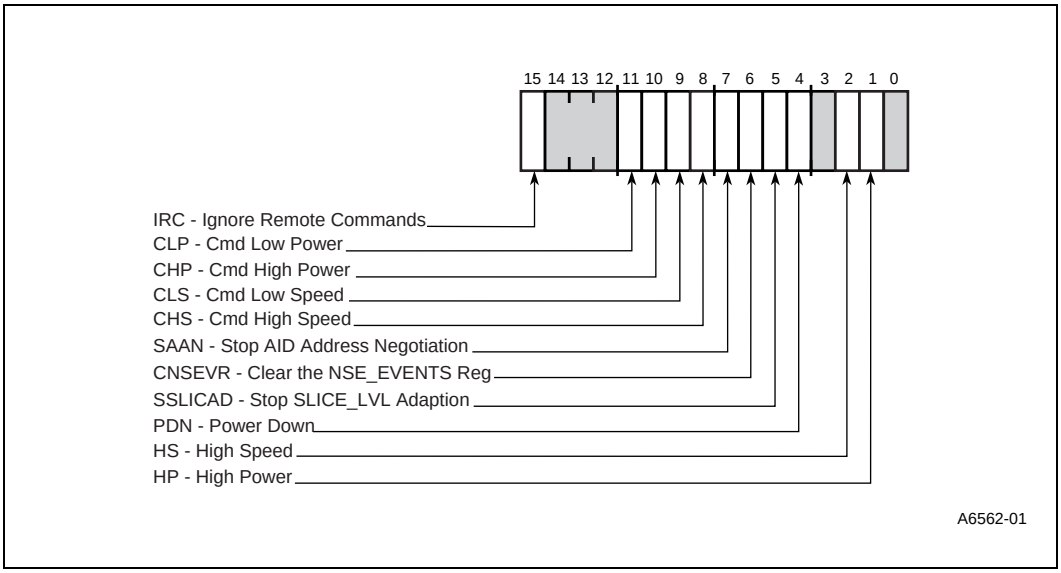


Table 8-102. Control Register Bit Field Description

Field	Description
15	IRC—Ignore Remote Commands When set, indicates that the HomePNA PHY will ignore incoming command from master HomePNA node to change the HomePNA speed or power operating mode.
11	CLP—Cmd Low Power When this bit is set, the 21145 will act as the master device and send a command to all other HomePNA network devices to move to a low power PHY operation. This bit is automatically cleared after the operation is completed.
10	CHD—Cmd High Power When this bit is set, the 21145 will act as the master device and send a command to all other HomePNA network devices to move to a high power PHY operation. This bit is automatically cleared after the operation is completed.
9	CMD—Cmd Low Speed When this bit is set, the 21145 will act as the master device and send a command to all other HomePNA network devices to move to a low speed PHY operation (0.7 Mb/s). This bit is automatically cleared after the operation is completed.
8	CHS—Cmd High Speed When this bit is set, the 21145 will act as the master device and send a command to all other HomePNA network devices to move to a high speed PHY operation (a 1 Mb/s data rate). This bit is automatically cleared after the operation is completed.
7	SAAN—Stop AID Address Negotiation When this bit is set, the 21145 will not change its Access ID value.
6	CNSEVR—Clear NSE_EVENTS register When set, clears the noise event register. This bit will be automatically cleared one cycle after writing a logic 1 into it.
5	SSLICAD—Stop SLICE_LVL Adaption When set, stops the adaption of the data and noise comparators according to the noise and peak signal levels.
4	PDN—Power Down When set, will power down the PHY logic. Note that this will not stop the PHY internal clocks.
2	HS—High Speed When set, will force the PHY to work at high speed operation. When reset, the PHY will work at low speed. Automatically set by Cmd High Speed and by a remote command.
1	HP—High Power When set, will force the PHY to work at high power mode of operation. When clear, the PHY will work at low power mode of operation. Automatically set by Cmd High Power and by a remote command.

Table 8-103 lists the access rules for the control register.

Table 8-103. Control Register Access Rules

Category	Description
Value after hardware reset	0005H
Read access rules	—
Write access rules	—

8.5.3.2 Status Register (Address 03H – 02H)

The status register provides information regarding the global aspects of the operation of the PHY. Figure 8-45 shows the status register bit fields and Table 8-104 describes the status register.

Figure 8-45. Status Register Bit Fields

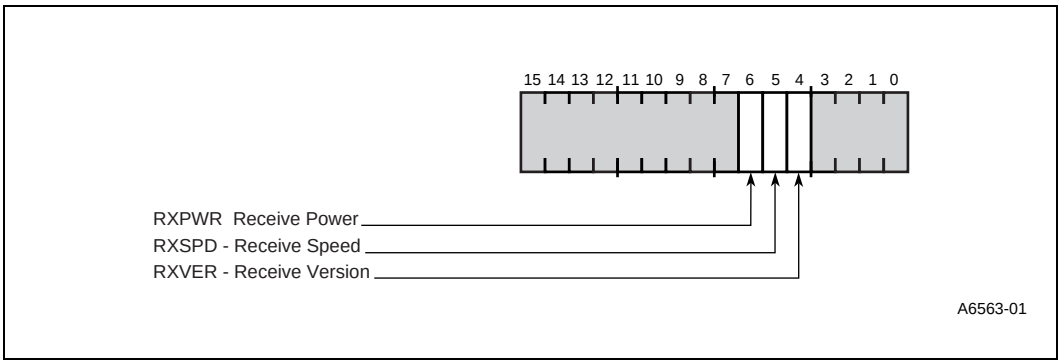


Table 8-104. Status Register Bit Fields

Field	Description
6	RXPWR—Receive Power The power of the last received packet. When set, indicates high power. When cleared, indicates low power.
5	RXSPD—Receive Speed The speed of the last received HomePNA packet. When set, indicates high speed. When reset, indicates low speed.
4	RXVER—Receive Version The technology version of the last received HomePNA packet.

Table 8-105 lists the access rules for the status register

Table 8-105. Status Register Access Rules

Category	Description
Value after hardware reset	0000H
Read access rules	—
Write access rules	R/O

8.5.3.3 Interrupt Mask (IMR) Register (Address 05H – 04H)

The interrupt mask register determines which HomePNA PHY interrupt sources will cause the HomePNA Interrupt bit (CSR5<28>) to be set. For the 21145 to generate an actual interrupt to the host, the HomePNA Interrupt Enable bit CSR7<28> must also be set. Figure 8-46 shows the interrupt mask register bit fields and Table 8-106 describes the bit fields. A logic 1 will enable the interrupt, while logic 0 will disable it. Each bit enables or disables the corresponding interrupt source in the PHY ISR register.

Figure 8-46. Interrupt Mask Register Bit Fields

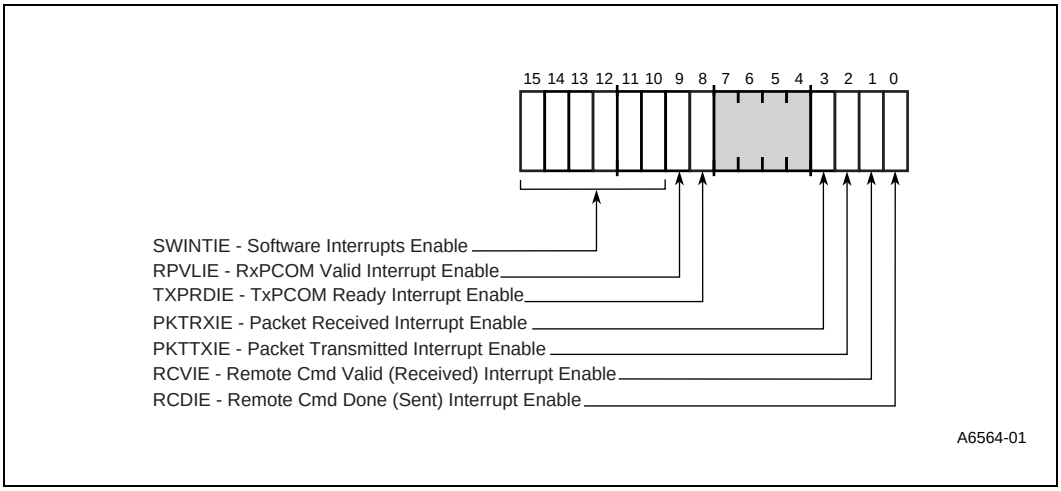


Table 8-106. Interrupt Mask Register Bit Fields Description

Field	Description
15:10	SWINTIE—Software Interrupts Enable Enables/disables the corresponding software interrupt bit in the ISR register.
9	RPVLIE—RxPCOM Valid Interrupt Enable Enables/disables the interrupt when a PCOM non-zero 32-bit field has been received.
8	TXPRDIE—TxPCOM Ready Interrupt Enable Enables/disables the interrupt when the TxPCOM has been transmitted and can be loaded again.
3	PKTRXIE—Packet Received Interrupt Enable Enables/disables the interrupt when a new packet has been received.
2	PKTTXIE—Packet Transmitted Interrupt Enable Enables/disables the interrupt when a new packet has been transmitted.
1	RCVIE—Remote Cmd Valid (Received) Interrupt Enable Enables/disables a remote command reception and execution interrupt.
0	RCDIE—Remote Cmd Done (Sent) Interrupt Enable Enables/disables a remote command completion of transmission interrupt.

Table 8-107 lists the access rules for the interrupt mask registers

Table 8-107. Interrupt Mask Register Access Rules

Category	Description
Value after hardware reset	0000H
Read access rules	—
Write access rules	—

8.5.3.4 Interrupt Status (ISR) Register (Address 07H – 06H)

The interrupt status register reports the state of each interrupt source, regardless of the state of the IMASK register. The interrupt sources are mapped into this register in an identical manner as the IMASK register. Furthermore, any bit may be written and so facilitate software-stimulated interrupt testing. The appropriate bits in this register must be cleared for the interrupt signal to the 21145 MAC to be cleared. Figure 8-47 shows the interrupt status register and Table 8-108 describes the bit fields.

Figure 8-47. Interrupt Status Register Bit Fields

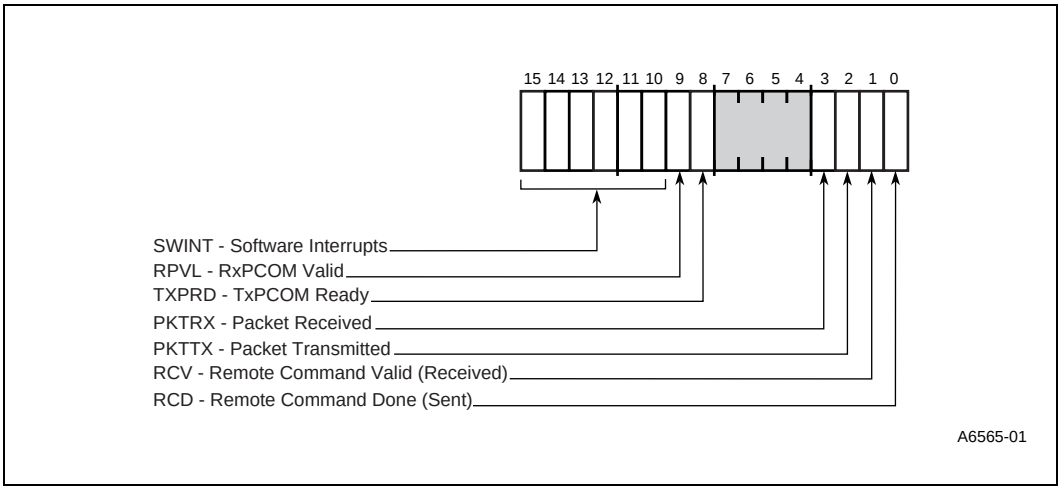


Table 8-108. Interrupt Status Register Bit Fields Description (Sheet 1 of 2)

Field	Description
15:10	SWINT—Software Interrupts Reserved for potential software interrupts.
9	RPVL—RxPCOM Valid When set, indicates that a non-zero 32-bit field of the PCOM has been received.
8	TXPRD—TxPCOM Ready When set, indicates that the transmitted PCOM has been transmitted and can be loaded again.
3	PKTRX—Packet Received When set, indicates that a new packet has been received.

Table 8-108. Interrupt Status Register Bit Fields Description (Sheet 2 of 2)

Field	Description
2	PKTTX—Packet Transmitted When set, indicates that a packet has been transmitted.
1	RCV—Remote Command Valid (Received) When set, indicates the reception and execution of a remote command (Cmd High Power, Cmd Low Power, Cmd High Speed, Cmd Low Speed.)
0	RCD—Remote Command Done (Sent) When set, indicates the completion of transmission of a remote command.

Table 8-109 lists the access rules for the interrupt status registers.

Table 8-109. Interrupt Status Register Access Rules

Category	Description
Value after hardware reset	0000H
Read access rules	—
Write access rules	—

8.5.3.5 Transmit PCOM (TX-PCOM) Register (Address 0BH – 08H)

The 32-bit transmitted data field to be used for out-of-band communication between PHY management entities. No protocol for out-of-band management is defined in this specification. Accessing any of the three low bytes causes the PHY to send all-0 PCOMs until the high byte has been accessed, the next transmitted packet will cause this register's contents to be shifted out in the PCOM field of the transmitted packet. Upon transmission, this register will read back as all -0's. A non-zero transmitted PCOM will set the TxPCOM ready bit in the ISTAT register. An access to any of the four TxPCOM bytes will clear the TxPCOM ready bit in the ISTAT register. Figure 8-48 shows the transmit PCOM register bit fields and Table 8-110 lists the access rules for the transmit PCOM register.

Figure 8-48. Transmit PCOM Register Bit Fields Description

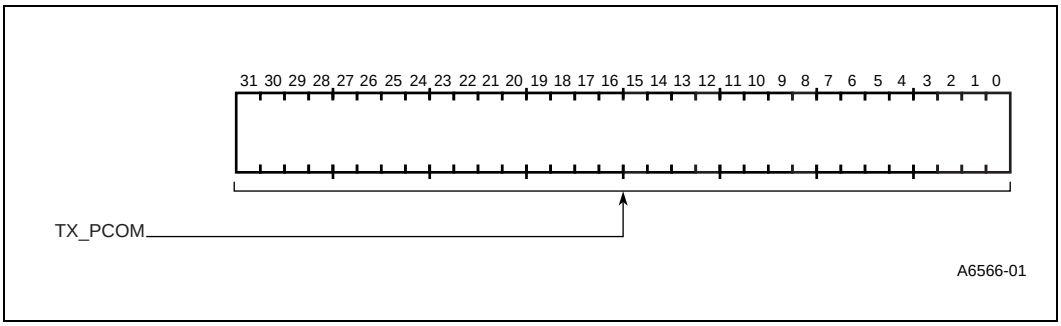


Table 8-110. Transmit PCOM Register Access Rules

Category	Description
Value after hardware reset	00000000H
Read access rules	—
Write access rules	—

8.5.3.6 Receive PCOM (RX-PCOM) Register (Address 0FH – 0CH)

The 32-bit received data field to be used for out-of-band communication between PHY management entities. No protocol for out-of-band management is defined in this specification. Accessing any of the three low bytes of this register is sufficient to ensure that subsequently received packets will not overwrite the register contents. A non-zero received PCOM will set the RxPCOM Valid bit of the ISTAT. Accessing the high byte of the register clears this bit and allows overwriting of the register by subsequent received packets. Figure 8-49 shows the receive PCOM register bit fields and Table 8-111 lists the access rules for the receive PCOM register.

Figure 8-49. Receive PCOM Register Bit Fields Description

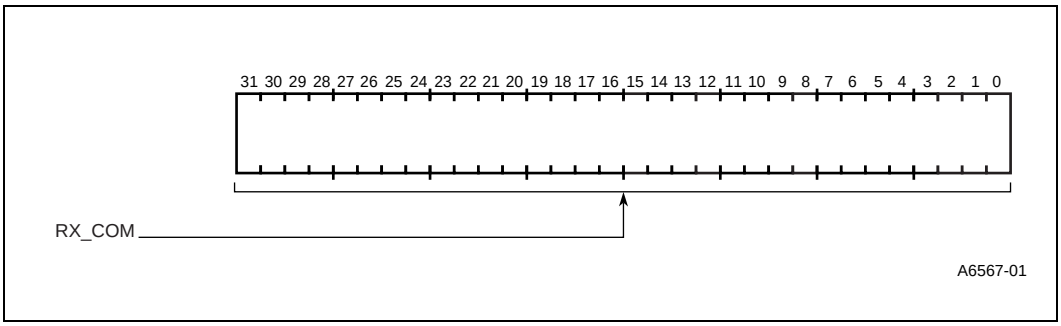


Table 8-111. Receive PCOM Register Access Rules

Category	Description
Value after hardware reset	00000000H
Read access rules	—
Write access rules	—

8.5.3.7 Noise Register (Address 10H)

This register reflects the maximum of the noise level on the wire and the NSE_FLOOR register. When auto-adaptation is enabled (bit 5 of the control register is clear), this register is updated with the current noise count every 50 ns. When adaptation is disabled, this register is writable and is used to generate the noise and data levels used by the PHY.

Figure 8-50 shows the Noise register bit fields and Table 8-112 lists the access rules for the Noise register.

Figure 8-50. Noise Register Bit Fields Description

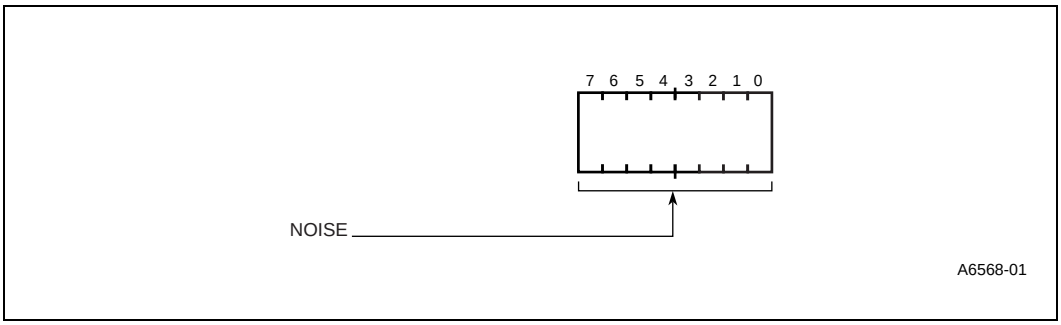


Table 8-112. Noise Register Access Rules

Category	Description
Value after hardware reset	Unknown
Read access rules	Bit 5 on the control register must be set to 1, otherwise value may change during the next cycle.
Write access rules	The noise register must be programmed with a value lower than the value in the peak register, otherwise it will reset to the NSE-floor value.

8.5.3.8 Peak Register (Address 11H)

This register contains the peak level of the last valid (non-collision) AID received.

Figure 8-51 shows the Peak register bit fields and Table 8-113 lists the access rules for the receive Peak register.

Figure 8-51. Peak Register Bit Fields Description

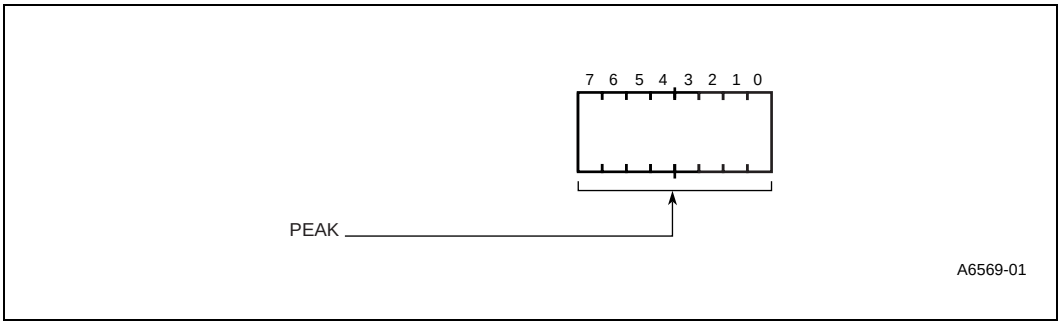


Table 8-113. Peak Register Access Rules

Category	Description
Value after hardware reset	Unknown
Read access rules	—
Write access rules	—

8.5.3.9 NSE_FLOOR Register (Address 12H)

This register determines the minimum value of the noise level.

Figure 8-52 shows the NSE_FLOOR register bit fields and Table 8-114 lists the access rules for the NSE_FLOOR register.

Figure 8-52. NSE_FLOOR Register Bit Fields Description

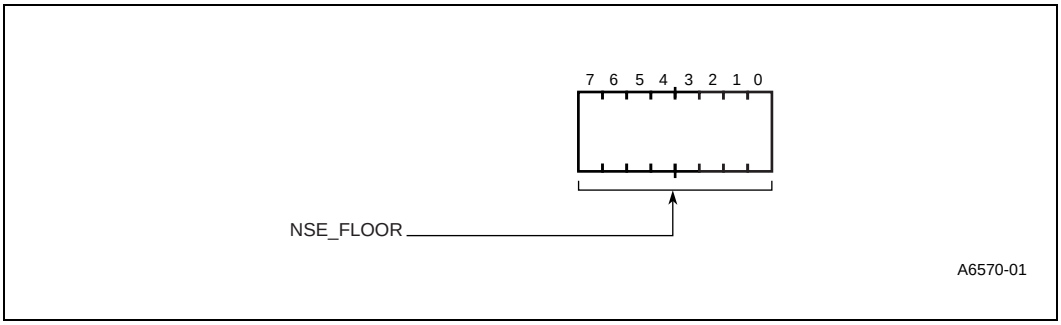


Table 8-114. NSE_FLOOR Register Access Rules

Category	Description
Value after hardware reset	04H
Read access rules	—
Write access rules	—

8.5.3.10 NSE_CEILING Register (Address 13H)

This register measures the maximum value of the noise level.

Figure 8-53 shows the NSE_CEILING register bit fields and Table 8-115 lists the access rules for the NSE_CEILING register.

Figure 8-53. NSE_CEILING Register Bit Fields Description

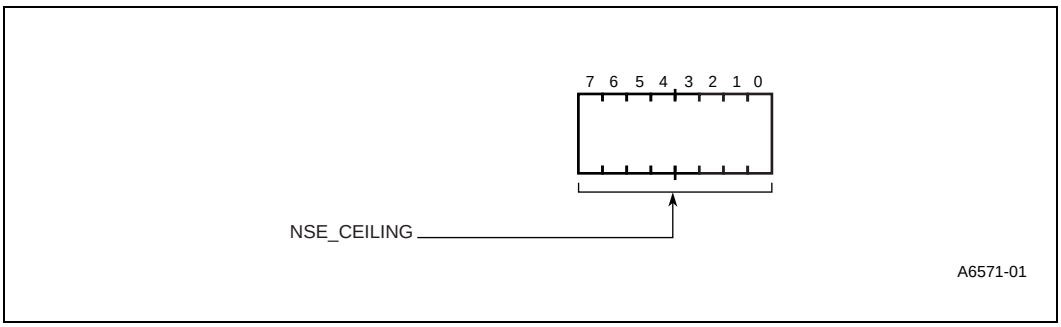


Table 8-115. NSE_CEILING Register Access Rules

Category	Description
Value after hardware reset	D0H
Read access rules	—
Write access rules	—

8.5.3.11 NSE_ATTACK Register (Address 14H)

This register sets the attack characteristics of the NOISE algorithm. Figure 8-54 and Table 8-116 show the NSE_ATTACK register bit fields and Table 8-117 lists the access rules for the NSE_ATTACK register.

Figure 8-54. NSE_ATTACK Register

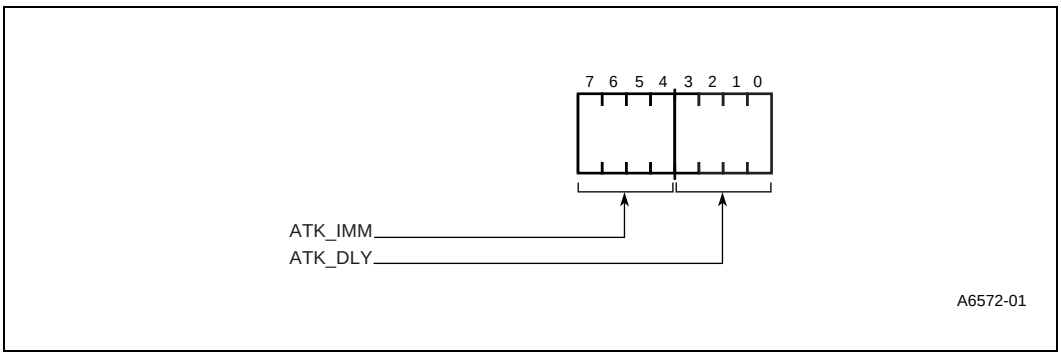


Table 8-116. NSE_ATTACK Register Bit Fields Description

Field	Description
7:4	ATK_IMM Number of noise events needed to raise the noise level immediately
3:0	ATK_DLY Number of noise events needed to raise the level at the end of an 870 ms period

Table 8-117. NSE_ATTACK Register Access Rules

Category	Description
Value after hardware reset	F4H
Read access rules	—
Write access rules	—

8.5.3.12 NSE_EVENTS Register (Address 15H)

An 8-bit counter that records the number of noise events detected. Overflows are held as FFH. Can be cleared by setting bit 6 of the PHY Control Register. Figure 8-55 shows the NSE_EVENTS register bit fields and Table 8-118 lists the access rules for the NSE_EVENTS register.

Figure 8-55. NSE_EVENTS Register Bit Fields Description

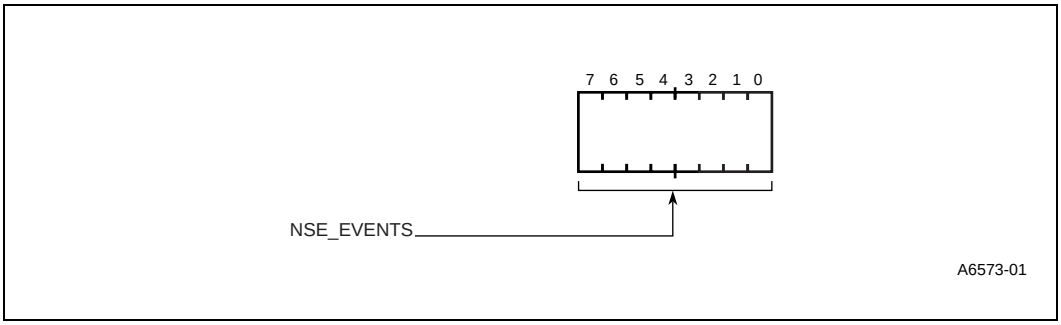


Table 8-118. NSE_EVENTS Register Access Rules

Category	Description
Value after hardware reset	Unknown
Read access rules	—
Write access rules	—

8.5.3.13 AID_ADDRESS Register (Address 19H)

The PHY's AID address is used for collision detection. Unless bit 7 of the PHY Control Register is set, the PHY is assured to select a Unique AID address. Addresses above 0EFH are reserved. Address FFH is defined to indicate a master station. Figure 8-56 shows the AID_ADDRESS register bit fields and Table 8-119 lists the access rules for the AID_ADDRESS register.

Figure 8-56. AID_ADDRESS Register Bit Fields Description

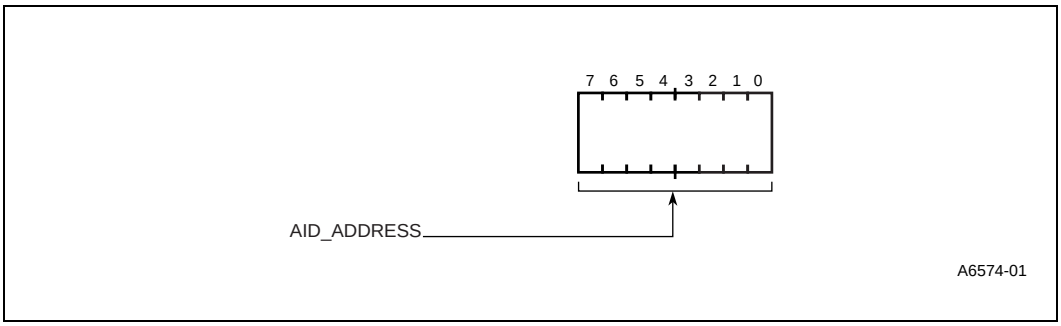


Table 8-119. AID_ADDRESS Register Access Rules

Category	Description
Value after hardware reset	00H
Read access rules	—
Write access rules	—

8.5.3.14 AID_INTERVAL Register (Address 1AH)

This value defines the number of TCLK's (116.7 ns) separating AID symbols. Figure 8-57 shows the AID_INTERVAL register bit fields and Table 8-120 lists the access rules for the AID_INTERVAL register.

Figure 8-57. AID_INTERVAL Register Bit Fields Description

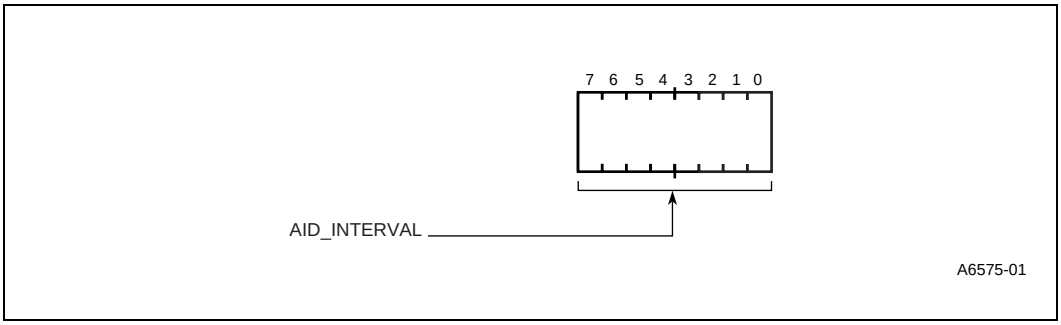


Table 8-120. AID_INTERVAL Register Access Rules

Category	Description
Value after hardware reset	14H
Read access rules	—
Write access rules	—

8.5.3.15 AID_ISBI Register (Address 1BH)

This value defines the number of TCLK's (116.7 ns) between AID pulses for symbol 0. Figure 8-58 shows the AID_ISBI register bit fields and Table 8-121 lists the access rules for the AID_ISBI register.

Figure 8-58. AID_ISBI Register Bit Fields Description

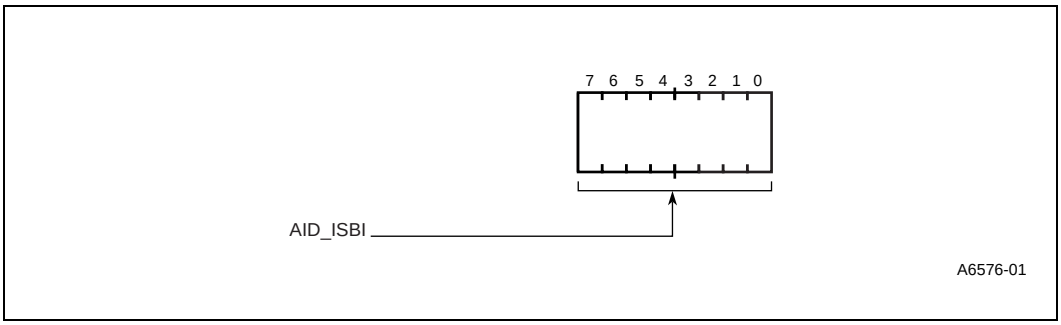


Table 8-121. AID_ISBI Register Access Rules

Category	Description
Value after hardware reset	40H
Read access rules	—
Write access rules	—

8.5.3.16 ISBI_SLOW Register (Address 1CH)

This value defines the number of TCLK's (116.7 ns) between DATA pulses for symbol 0 in low speed. Figure 8-59 shows the ISBI_SLOW register bit fields and Table 8-122 lists the access rules for the ISBI_SLOW register.

Figure 8-59. ISBI_SLOW Register Bit Fields Description

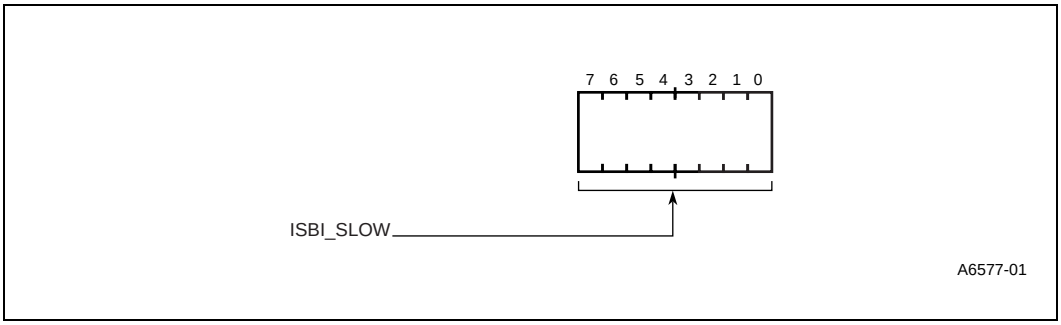


Table 8-122. ISBI_SLOW Register Access Rules

Category	Description
Value after hardware reset	2CH
Read access rules	—
Write access rules	—

8.5.3.17 ISBI_FAST Register (Address 1DH)

This value defines the number of TCLK's (116.7 ns) between DATA pulses for symbol 0 in high speed. Figure 8-60 shows the ISBI_FAST register bit fields and Table 8-123 lists the access rules for the ISBI_FAST register.

Figure 8-60. ISBI_FAST Register Bit Fields Description

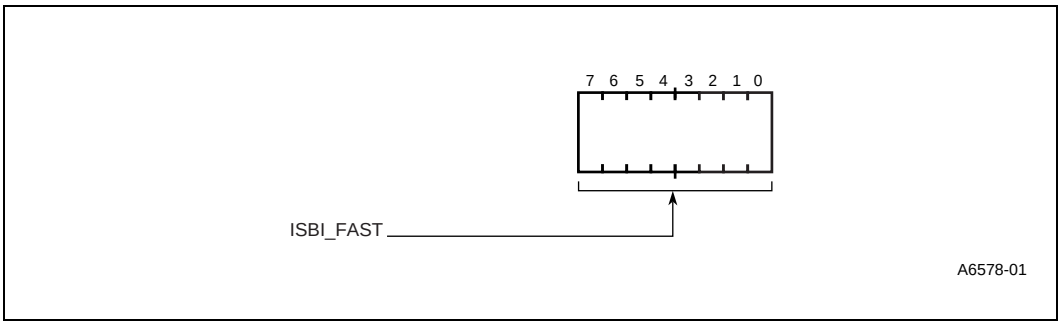


Table 8-123. ISBI_FAST Register Access Rules

Category	Description
Value after hardware reset	1CH
Read access rules	—
Write access rules	—

8.5.3.18 TX_PULSE_WIDTH Register (Address 1EH)

This value determines the length of the transmit pulse in 16.7 ns units. For proper HomePNA operation this register's value must be 04h. Figure 8-61 shows the TX_PULSE_WIDTH register bit fields and Table 8-124 lists the access rules for the TX_PULSE_WIDTH register.

Figure 8-61. TX_PULSE_WIDTH Register Bit Fields Description

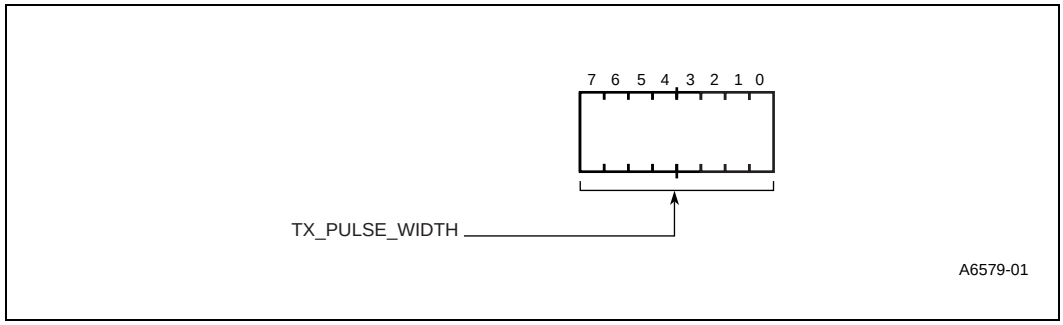


Table 8-124. TX_PULSE_WIDTH Register Access Rules

Category	Description
Value after hardware reset	04H
Read access rules	—
Write access rules	—

8.5.3.19 TX_PULSE_CYCLES Register (Address 1FH)

The low nibble of this register indicates the number of pulses on the TXN/TXNH pins, while the high nibble indicates the number of pulses on the TXP/TXPH pins. Figure 8-62 and Table 8-125 show the TX_PULSE_CYCLES register bit fields and Table 8-126 lists the access rules for the TX_PULSE_CYCLES register.

Figure 8-62. TX_PULSE_CYCLES Register

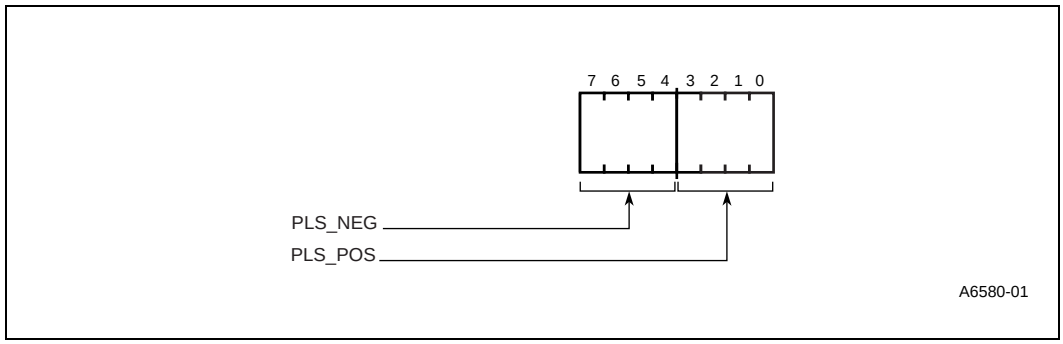


Table 8-125. TX_PULSE_CYCLES Register Bit Fields Description

Field	Description
7:4	PLS_NEG Indicates the number of pulses on the hr_txn/hr_txnh pins.
3:0	PLS_POS Indicates the number of pulses on the hr_txp/hr_txph pins.

Table 8-126. TX_PULSE_CYCLES Register Access Rules

Category	Description
Value after hardware reset	44H
Read access rules	—
Write access rules	—

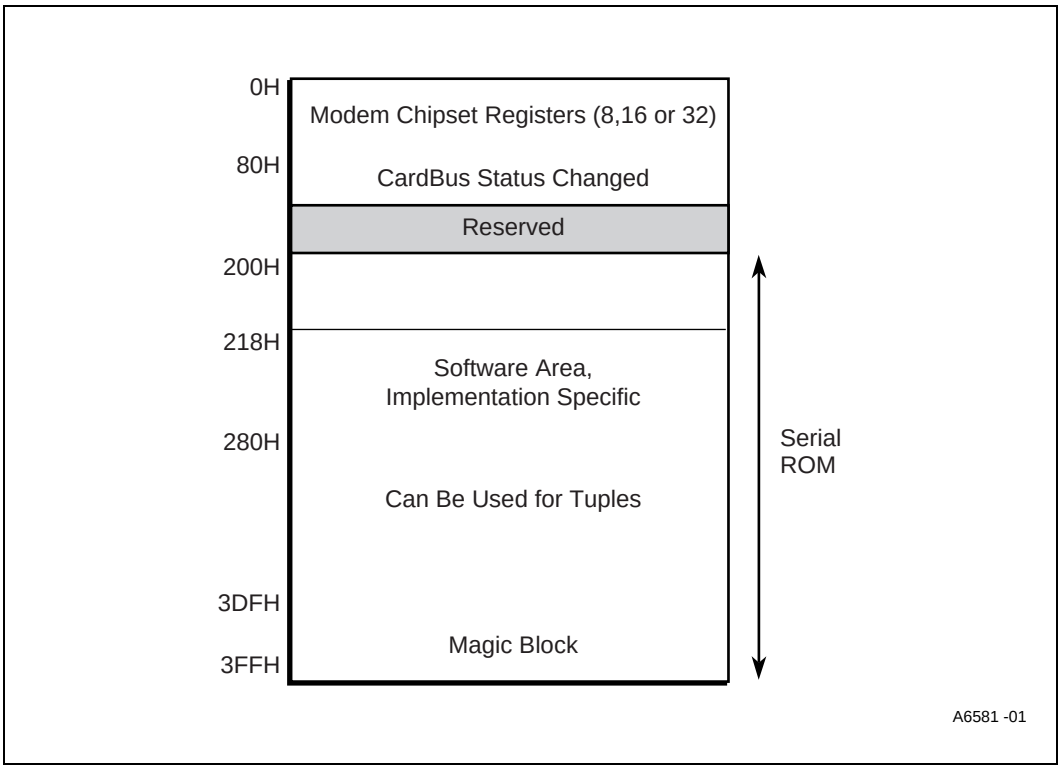
8.6 Modem Function Memory Map

Note: The 21145 Modem function supports the modem chipset's internal registers as 8, 16 or 32 byte-wide registers that can be mapped to either the I/O space through CBIO or to the memory space through CBMA. The number of registers is specified in the Func1_HwOptions<2:1> field in the Serial ROM; the locations between the number of modem registers specified in the Serial ROM and offset 80H are reserved, and accessing them will cause unpredictable results.

The Serial ROM is mapped to the memory space through the modem function's CBMA. In addition, the 21145's Modem function has four CardBus Status Changed Registers that can be mapped only to the memory space. Figure 8-63 shows a map of the 21145's Modem function memory map through CBMA.

Note: All shaded bits in the figures are reserved. All reserved fields within non-reserved locations must be written by software as 0, and must be masked off when read; reserved register and memory locations must not be written to.

Figure 8-63. Modem Function Memory Map



8.7 Modem Function PCI Configuration Registers

The 21145 implements 13 Modem Function PCI configuration registers. These registers, which are used for the initialization and the configuration of the 21145 Modem function, are described in the following subsections.

Note: If the Modem Function configuration registers are accessed by the host before the Func1_HwOptions<0> (ModemEnable) bit is loaded from the serial ROM, the 21145 responds with a retry termination on the PCI bus.

Table 8-127 lists the definitions and addresses of the modem configuration registers and Figure 8-64 shows the structure.

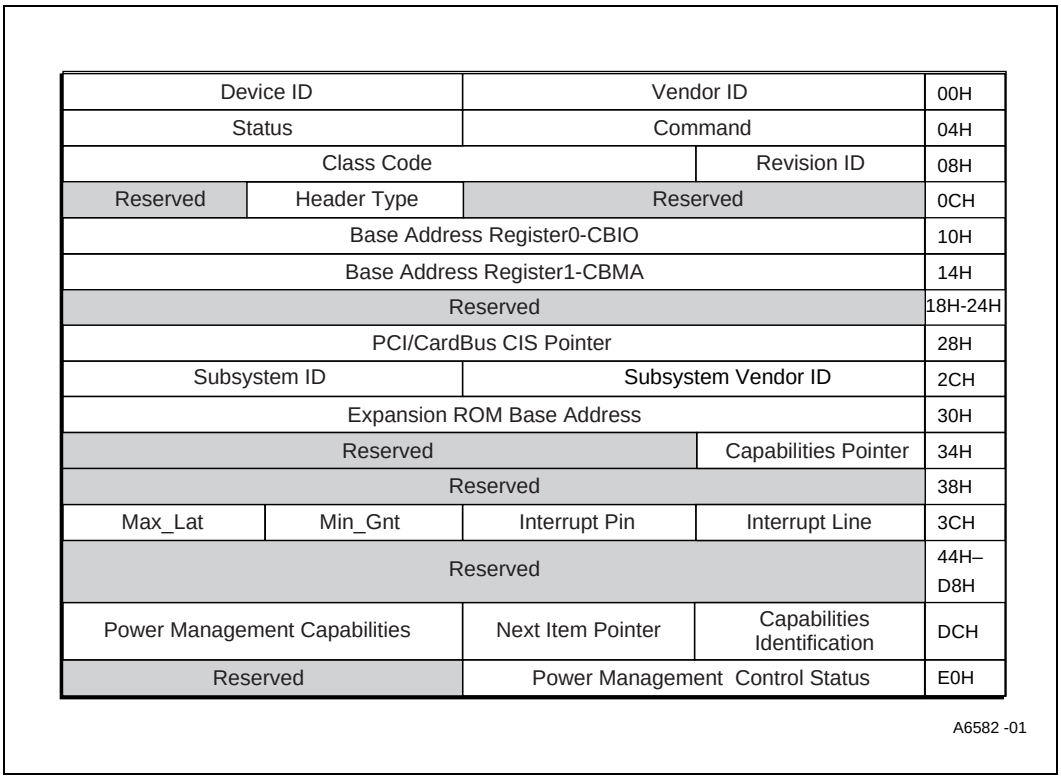
Table 8-127. Modem Function Configuration Registers Mapping (Sheet 1 of 2)

Configuration Register	Identifier	I/O Address Offset
Identification	CFID	00H
Command and status	CFCS	04H
Revision	CFRV	08H
Latency timer	CFHT	0CH
Base I/O address	CBIO	10H

Table 8-127. Modem Function Configuration Registers Mapping (Sheet 2 of 2)

Configuration Register	Identifier	I/O Address Offset
Base memory address	CBMA	14H
Reserved	—	18H–24H
Card information structure	CCIS	28H
Subsystem ID	CSID	2CH
Expansion ROM base address	CBER	30H
Capabilities Pointer	CCAP	34H
Reserved	—	38H
Interrupt	CFIT	3CH
Reserved	—	40H–D8H
Capabilities ID	CCID	0DCH
Power Management Control	CPMC	E0H

Figure 8-64. Modem Configuration Register Structure



8.7.1 Configuration ID Register (CFID–Offset 00H)

The CFID register identifies the 21145. Figure 8-65 shows the CFID register bit fields and Table 8-128 describes the bit fields.

Figure 8-65. CFID Register Bit Fields

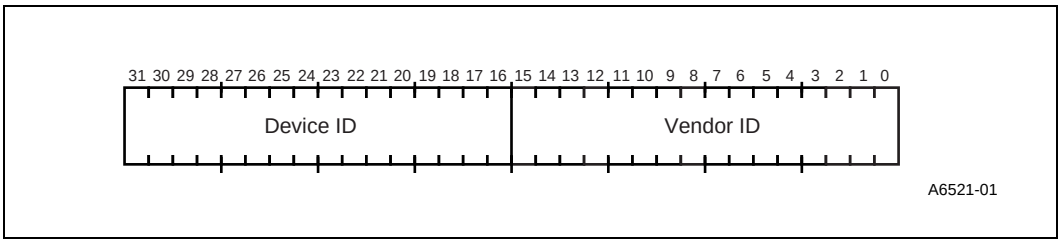


Table 8-128. CFID Register Bit Fields Description

Field	Description
31:16	Device ID Provides the unique 21145 Modem Function ID number (0034H).
15:0	Vendor ID Specifies the 21145 manufacturer ID (8086H)

Table 8-129 lists the access rules for the CFID register.

Table 8-129. CFID Register Access Rules

Category	Description
Value after hardware reset	00348086H
Read access rules	—
Write access rules	R/O

8.7.2 Command and Status Configuration Register (CFCS–Offset 04H)

The CFCS register is divided into two sections: a command register (CFCS<15:0>) and a status register (CFCS<31:16>).

The command register provides control of the 21145's Modem function ability to generate and respond to PCI cycles. When 0 is written to this register, the 21145 logically disconnects from the PCI bus for all accesses except configuration accesses.

The status register records status information for the PCI bus-related events. The CFCS status bits are not cleared when they are read. Writing 1 to these bits clears them; writing 0 has no effect. Figure 8-66 shows the CFCS register bit fields.

Figure 8-66. CFCS Register Bit Fields

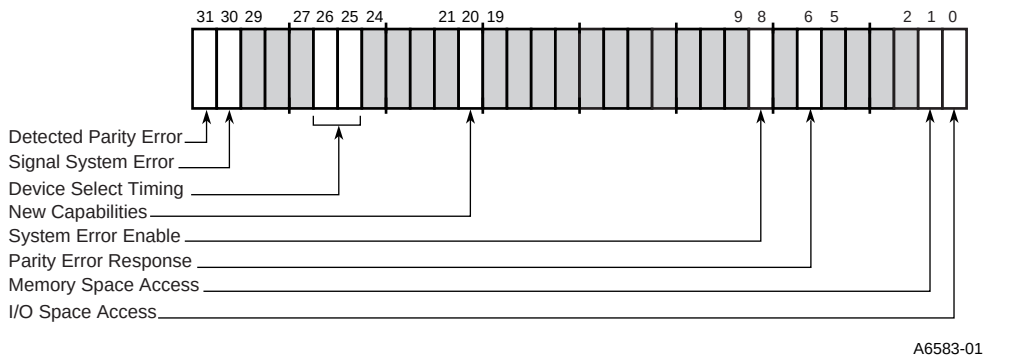


Table 8-130 describes the CFCS register bit fields.

Table 8-130. CFCS Register Bit Fields Description (Sheet 1 of 2)

Field	Bit Type	Description
31	Status	Detected Parity Error When set, indicates that the Modem function of the 21145 detected a parity error, even if parity error handling is disabled in parity error response (CFCS<6>).
30	Status	Signaled System Error When set, indicates that the modem function of the 21145 asserted the system error serr_l pin.
26:25	Status	Device Select Timing Indicates the timing of the assertion of device select (devsel_l). These bits are fixed at 01, which indicates a medium assertion of devsel_l.
20	Status	New Capabilities Indicates whether or not the 21145's Modem function implements a list of new capabilities. When set, this bit indicates the presence of New Capabilities. When cleared, New Capabilities are not implemented. The value of this bit is loaded from Func0_HwOptions<3> bit (PME_Enable) in the serial ROM.
8	Command	System Error Enable When set, the 21145's modem function asserts system error (serr_l) when it detects a parity error on the address phase.

Table 8-130. CFCS Register Bit Fields Description (Sheet 2 of 2)

Field	Bit Type	Description
6	Command	Parity Error Response When set, the 21145's Modem function asserts fatal bus error after it detects a parity error. When cleared, any detected parity error is ignored and the 21145's modem function continues normal operation.
1	Command	Memory Space Access When set, the 21145's Modem function responds to memory space accesses. When cleared, the 21145's Modem function does not respond to memory space accesses.
0	Command	I/O Space Access When set, the 21145's modem function responds to I/O space accesses. When cleared, the 21145's modem function does not respond to I/O space accesses.

Table 8-131 lists the access rules for the CFCS register.

Table 8-131. CFCS Register Access Rules

Category	Description
Value after hardware reset	29000000H[1]
Read access rules	—
Write access rules	—

1. According to Func0_HwOptions<3> in the serial ROM.

8.7.3 Configuration Revision Register (CFRV–Offset 08H)

The CFRV register contains the 21145 revision number. Figure 8-67 shows the CFRV register bit fields and Table 8-132 describes the bit fields.

Figure 8-67. CFRV Register Bit Fields

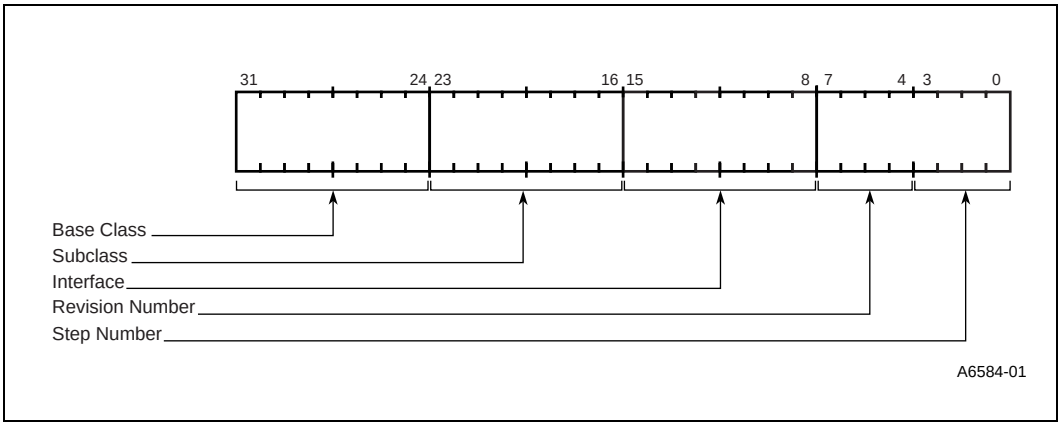


Table 8-132. CFRV Register Bit Fields Description

Field	Description
31:24	Base Class The value of this field is 07, indicating that this is a simple communication controller function.
23:16	Subclass The value of this field is loaded from the modem class code (sub-class) field in the serial ROM.
15:8	Interface The value of this field is loaded from the modem class code (interface) field in the serial ROM.
7:4	Revision Number Indicates the 21145 Modem function revision number.
3:0	Step Number Indicates the 21145 Modem function step number within the current revision.

Table 8-133 lists the revision and step numbers for each variant of the device.

Table 8-133. 21145 Modem Function Revision and Step Number

Device	Revision Number	Step Number
21145, 176-pin, B0 stepping (DC1116, order no. DE-NH978-AA)	1	1

Table 8-134 lists the access rules for the CFRV register

Table 8-134. CFRV Access Rules

Category	Description
Value after hardware reset	07XXYY11H[1]
Read access rules	—
Write access rules	R/O

1. XXYY are read from the “modem class code (interface/sub-code)” fields in the serial ROM.

8.7.4 Configuration Header Type Register (CFHT–Offset 0CH)

This register indicates to the system that the 21145 is a multi-function device. Figure 8-68 shows the CFLT bit field and Table 8-135 describes the CFLT bit field.

Figure 8-68. CFHT Configuration Header Type Register

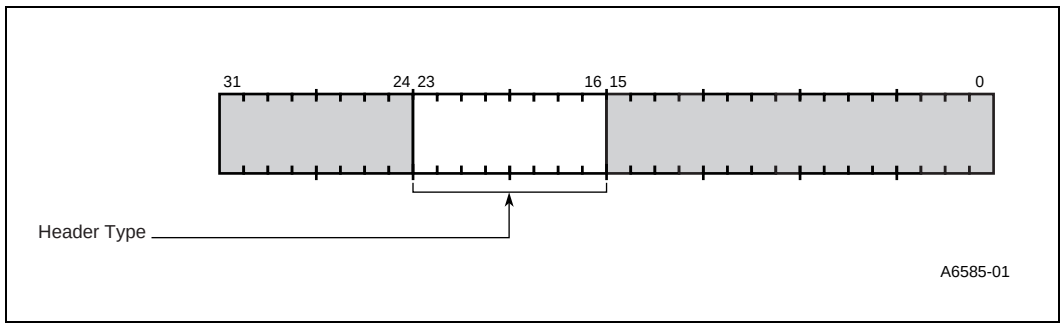


Table 8-135. CFHT Register Bit Fields Description

Field	Description
23:16	Header Type The value of this field is 80H, indicating that the 21145 is a multiple function device.

Table 8-136 lists the access rules for the CFHT register.

Table 8-136. CFHT Access Rules

Category	Description
Value after hardware reset	00800000H
Read access rules	—
Write access rules	R/O

8.7.5 Configuration Base I/O Address Register (CBIO–Offset 10H)

The CBIO register specifies the base I/O address for accessing the modem chipset registers. The CBIO register can map 8, 16, or 32 modem registers according to the serial ROM configuration.

This register must be initialized prior to accessing any modem register with I/O access.

Figure 8-69 shows the CBIO register bit fields and Table 8-137 describes the bit fields.

Figure 8-69. CBIO Register Bit Fields

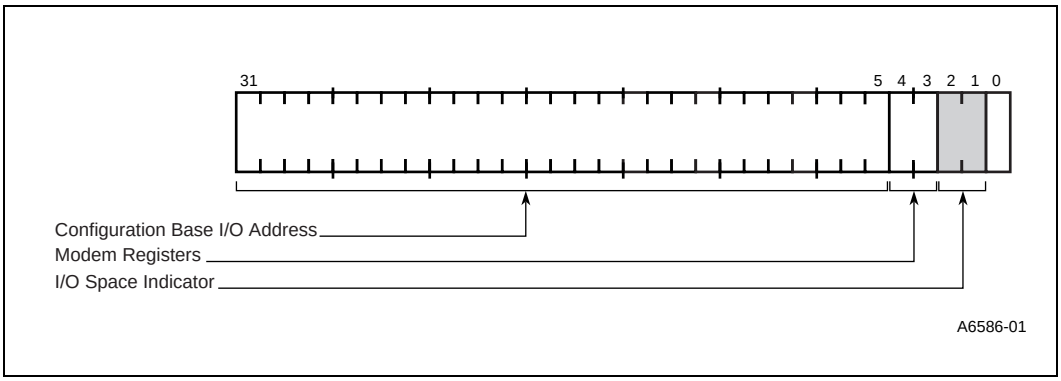


Table 8-137. CBIO Register Bit Fields Description

Field	Description
31:5	Configuration Base I/O Address Defines the base address assigned for mapping the modem chipset's CSRs.
4:3	Modem Registers The functionality of these bits is affected through serial ROM programming in Func1_HwOptions<2:1>. See Table 8-138 for possible values:
0	I/O Space Indicator Determines that the register maps into the I/O space. The value in this field is 1. This is a read-only field.

Table 8-138 lists the possible values for bit 4 and bit 3.

Table 8-138. Number of Internal Modem Registers

Number of Modem Registers	Bit 4	Bit 3	Serial ROM Code
8	read and write	read and write	00
16	read and write	0	01
32	0	0	10

Table 8-139 lists the access rules for the CBIO register.

Table 8-139. CBIO Register Access Rules

Category	Description
Value after hardware reset	Undefined
Read access rules	—
Write access rules	—

8.7.6 Configuration Base Memory Address Register (CBMA–Offset 14H)

The CBMA register specifies the base I/O address for accessing the modem chipset registers. The CBMA register can map 8, 16, or 32 modem registers, 4 CardBus Status Changed registers, and the serial ROM. This register must be initialized prior to accessing any modem function structures with memory access. Figure 8-70 shows the CBMA register bit fields and Table 8-140 describes the bit fields.

Figure 8-70. CBMA Register Bit Fields

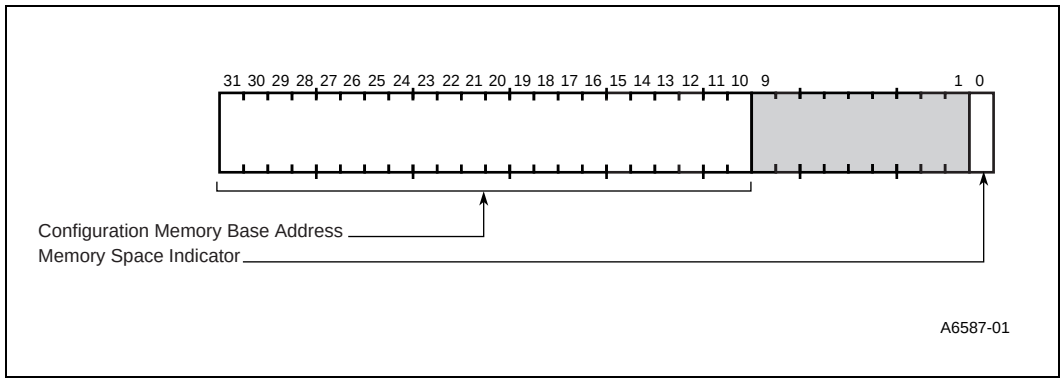


Table 8-140. CBMA Register Bit Fields Description

Field	Description
31:10	Configuration Base Memory Address Defines the base address assigned for mapping 8, 16 or 32 modem CSRs, 4 modem function PCI/CardBus Status Changed registers and 512 bytes of CIS in the serial ROM.
9:1	This field value is 0 when read.
0	Memory Space Indicator Indicates that this register maps Memory registers.

Table 8-141 lists the access rules for the CBMA register.

Table 8-141. CBMA Register Access Rules

Category	Description
Value after hardware reset	Undefined
Read access rules	—
Write access rules	—

8.7.7 Configuration Card Information Structure Register (CCIS–Offset 28H)

The CCIS register is a read-only 32-bit register. This register points to one of the possible address spaces where the card information structure (CIS) begins. The pointer is used in a PCI/CardBus PC card environment. The content of the CCIS is loaded from the serial ROM after a hardware reset. If the CCIS is accessed by the host before its content is loaded from the serial ROM, the 21145 responds with retry termination on the PCI bus. A value of 0 in this register indicates that CIS is not supported.

Figure 8-71 shows the CCIS register bit fields and Table 8-142 describes the bit fields.

Figure 8-71. CCIS Register Bit Fields

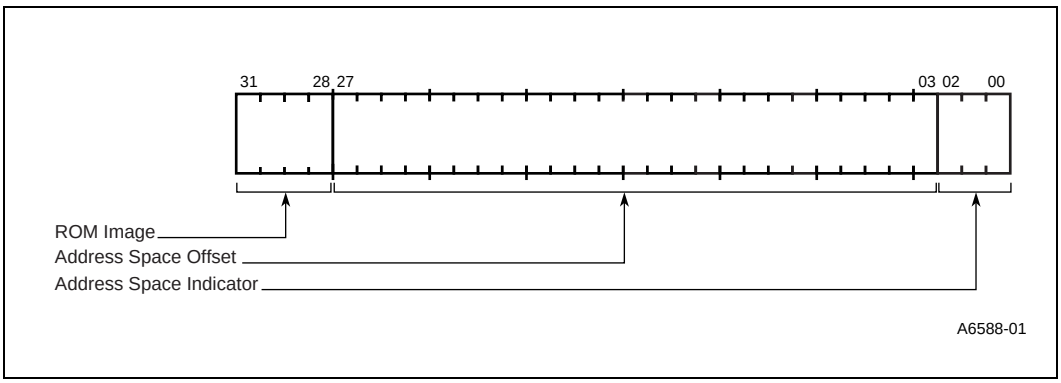


Table 8-142. CCIS Register Bit Fields Description

Field	Description
31:28	ROM Image The 4-bit ROM image field value when the CIS resides in an expansion ROM.
27:03	Address Space Offset. This field contains the address offset within the address space indicated by the address space indicator field (CCIS<2:0>).
2:0	Address Space Indicator This field indicates the location of the CIS base address. The 21145 supports the value of 2, indicating that the CIS is stored in the serial ROM, and 7, indicating that the CIS is stored in the expansion ROM. Any value other than 2 or 7 may lead to unpredictable behavior.

Table 8-143 lists the access rules for the CCIS register.

Table 8-143. CCIS Register Access Rules

Category	Description
Value after hardware reset	Read from serial ROM.
Read access rules	—
Write access rules	R/O

8.7.8 Subsystem ID Register (CSID–Offset 2CH)

The CSID register is a read-only 32-bit register. The content of the CSID is loaded from the serial ROM after a hardware reset. If the CSID is accessed by the host before its content is loaded from the serial ROM, the 21145 responds with retry termination on the PCI bus. The value is 0 if the serial ROM data integrity check fails.

Figure 8-72 shows the CSID register bit fields and Table 8-144 describes the bit fields.

Figure 8-72. CSID Register Bit Fields

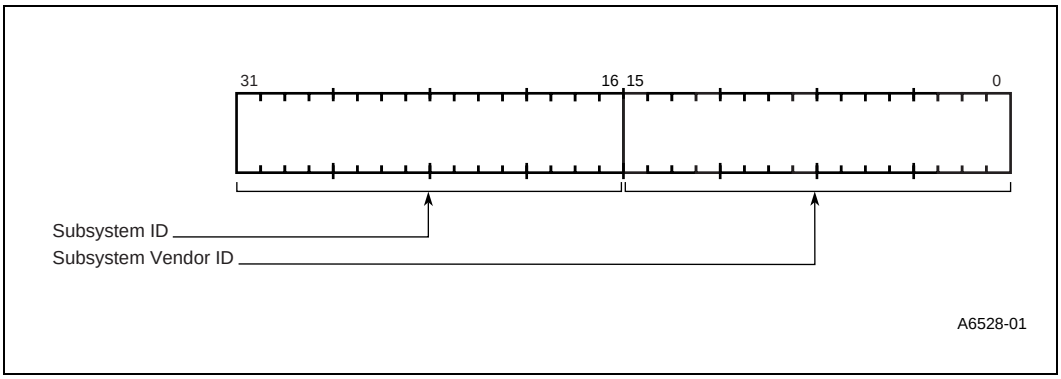


Table 8-144. CSID Register Bit Fields Description

Field	Description
31:16	Subsystem ID Indicates the subsystem ID. The value of this field is read from the serial ROM. Bits <31:24> are read from the subsystem ID - Ethernet <15:8> and bits <23:16> are read from the subsystem ID - modem field.
15:0	Subsystem Vendor ID Indicates the subsystem vendor ID. This field is read from the sub-system vendor ID - Ethernet and modem field in the serial ROM.

Table 8-145 lists the access rules for the CSID register.

Table 8-145. CSID Register Access Rules

Category	Description
Value after hardware reset	Read from serial ROM.
Read access rules	—
Write access rules	R/O

8.7.9 Expansion ROM Base Address Register (CBER–Offset 30H)

The CBER register specifies the base address and provides information about the expansion ROM size. This register must be initialized prior to accessing the expansion ROM with longword access.

Figure 8-73 shows the CBER register bit fields and Table 8-146 describes the bit fields.

Figure 8-73. CBER Register Bit Fields

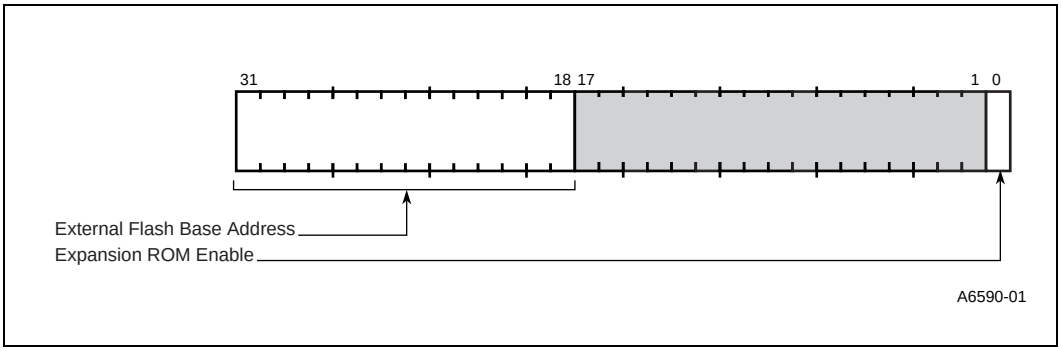


Table 8-146. CBER Register Bit Fields Description

Field	Description
31:18	External Flash Base Address Defines the base address assigned for mapping the expansion ROM.
17:1	This field value is 0 when read
0	Expansion ROM Enable Bit When set, enables the expansion ROM. The value of this bit is 0 after reset.

Table 8-147 lists the access rules for the CBER register.

Table 8-147. CBER Register Access Rules

Category	Description
Value after hardware reset	XXXX0000H
Read access rules	—
Write access rules	—

8.7.10 Capabilities Pointer (CCAP–Offset 34H)

The CCAP register has a pointer to the power management register block in the modem function PCI configuration space. This pointer is valid only if the new capabilities bit in CFCS is set.

Figure 8-74 shows the CCAP register bit fields and Table 8-148 describes the bit fields.

Figure 8-74. CCAP Register Bit Fields

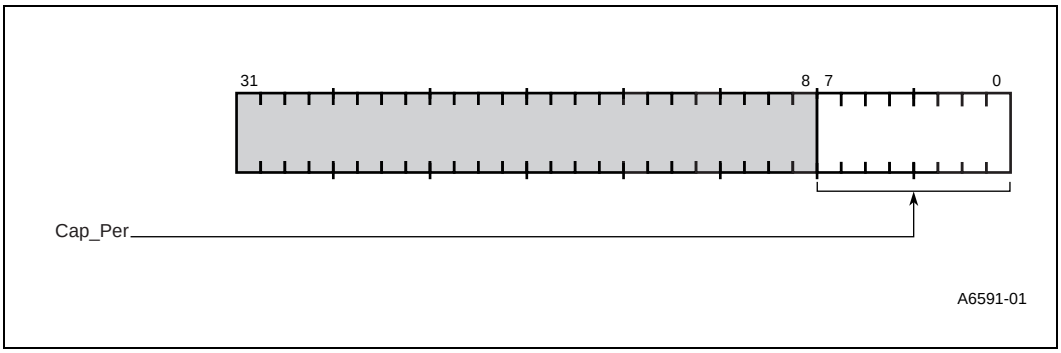


Table 8-148. CCAP Register Bit Fields Description

Field	Description
7:0	Capabilities pointer Points to the location of the power management register block in the modem function PCI Configuration Space. The value of this field is determined by Func0_HwOptions<3> bit (PME_Enable**)** in the serial ROM. If this bit is set, the value of this field is DCh, otherwise this bit is read as 00.

Table 8-149 lists the access rules for the CCAP register.

Table 8-149. CCAP Register Access Rules

Category	Description
Value after hardware reset	000000DC[1]H
Read access rules	—
Write access rules	—

1. According to the Func0_HwOptions<3> in the serial ROM.

8.7.11 Configuration Interrupt Register (CFIT–Offset 3CH)

The CFIT register is divided into two sections: the interrupt line and the interrupt pin. CFIT configures both the system's interrupt line and the 21145 interrupt pin connection. Figure 8-75 shows the CFIT register bit fields.

Figure 8-75. CFIT Register Bit Fields

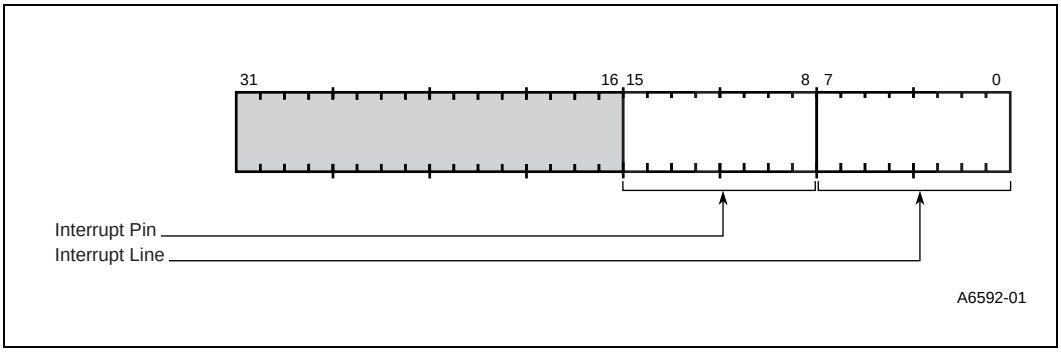


Table 8-150 describes the CFIT register bit fields

Table 8-150. CFIT Register Bit Fields Description

Field	Description
15:8	Interrupt Pin Indicates which interrupt pin the 21145 uses. The 21145 uses INTA and the read value is 01H.
7:0	Interrupt Line Provides interrupt line routing information. The basic input/output system (BIOS) writes the routing information into this field when it initializes and configures the system. The value in this field indicates which input of the system interrupt controller is connected to the 21145's interrupt pin. The driver can use this information to determine priority and vector information. Values in this field are system architecture specific.

Table 8-151 lists the access rules for the CFIT register.

Table 8-151. CFIT Register Access Rules

Category	Description
Value after hardware reset	000001XXH
Read access rules	—
Write access rules	—

8.7.12 Capability ID Register (CCID–Offset DCH)

The CCID register is a read-only register that provides information on the 21145 modem function power-management capabilities.

Figure 8-76 shows the CCID register.

Figure 8-76. CCID Register Bit Fields

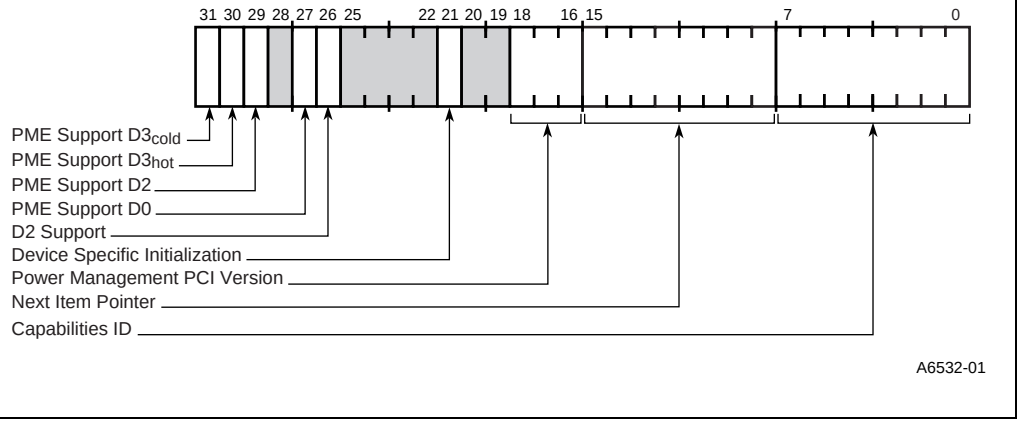


Table 8-152 describes the CCID register bit fields

Table 8-152. CCID Register Bit Fields Description (Sheet 1 of 2)

Field	Description
31	PME Support $D3_{cold}$ If this bit is set, the 21145 modem function may assert PME in D3cold power state. Otherwise, the 21145 modem function may not assert the gep<2>/rcv_match/wake pin in $D3_{cold}$. The value of this bit is loaded from Func0_HwOptions<6> bit in the serial ROM.
30	PME Support $D3_{hot}$ The value of this field is 1, indicating that the 21145 modem function may assert the gep<2>/ rcv_match/wake pin in the $D3_{hot}$ power state.
29	PME Support D2 The value of this field is 1, indicating that the 21145 modem function can assert the gep<2>/ rcv_match/wake pin in the D2 Power state.
27	PME Support D0 The value of this field is 0, indicating that the 21145 modem function does not assert the gep<2>/ rcv_match/wake pin in the D0 Power state.
26	D2 Support The value of this field is 1, indicating that the 21145 modem function supports the D2 Power state.
21	Device Specific Initialization The value of this field is 0, indicating that the 21145 modem function does not require a special initialization code sequence to be configured correctly.

Table 8-152. CCID Register Bit Fields Description (Sheet 2 of 2)

Field	Description
18:16	Power Management PCI Version The value of this field is 001b, indicating that the 21145 modem function complies with Rev 1.0 of the PCI Power Management Specifications.
15:8	Next Item Pointer Points to the location of the next block of the capability list in the modem function PCI Configuration Space. The value of this field is 00h, indicating that this is the last item of the Capability linked list.
7:0	Capabilities ID PCI Power Management Registers ID. The value of this field is 01h, indicating that this is the power management register block.

Table 8-153 contains the CCID register access rules

Table 8-153. CCID Register Access Rules

Category	Description
Value after reset	F6110001H[1]
Read access rules	—
Write access rules	

1. According to Func0_HwOptions<5> and FuncOptions<6> in the serial ROM.

8.7.13 Power Management Control Register (CPMC–Offset E0H)

The CPMC register is used to manage the device power state for the 21145 modem function, and to enable and monitor the power management events for the 21145 modem function.

Figure 8-77 shows the CPMC register.

Figure 8-77. CPMC Register Bit Fields

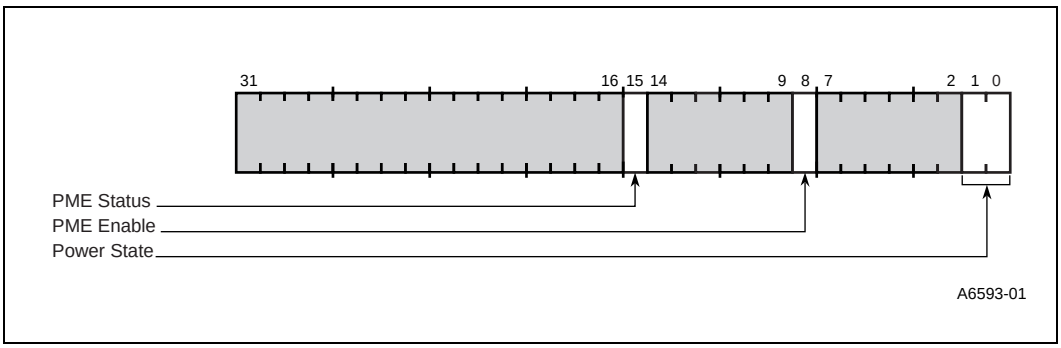


Table 8-154 describes the CPMC register bit fields.

Table 8-154. CPMC Register Bit Fields Description

Field	Description
15	PME Status This bit indicates that the 21145 Modem function has detected a power management event. If the PME_Enable bit is set, the 21145 also assert the gep<2>/rcv_match/wake pin. This bit may be cleared by writing 1 to it after the 21145 is placed in the D0 power state. When this bit is cleared, the 21145 deasserts the gep<2>/rcv_match/wake pin. Note: This bit is also affected by the General Enable bit of the Function Event Register (FER<4>); see. It is not modified by either hardware or software reset.
8	PME Enable If this bit is set, the 21145 Modem function can assert the gep<2>/rcv_match/wake pin. Otherwise, assertion of the gep<2>/rcv_match/wake pin by the 21145 modem function is disabled. This bit is cleared on power up reset only and is not modified by either hardware or software reset.
1:0	Power State This field is used to set the current power state of the 21145 Modem function and to determine its power state. The definition of the field values is: 0 - D0 1 - Reserved[1] 2 - D2 3 - $D3_{hot}$ This field hasa value of 0 after power up.

1. State D1 is not defined for communication devices.

Table 8-155 contains the CPMC register access rules

Table 8-155. CPMC Register Access Rules

Category	Description
Value after reset	00000000H
Read access rules	—
Write access rules	—

8.8 Modem Function CardBus Status Changed Registers

The 21145 Modem function implements four Status Changed registers. The Status Changed registers are accessed by the CardBus system software. These registers are mapped only to the memory address space and not to the I/O address space.

These registers affect the operation of the 21145 only if both:

- Func0_HwOptions<7> bit (RealSTSCHG) in the serial ROM is set.
- The FER or the FEMR were accessed with a write operation after a power-up reset.

Otherwise, these registers are not valid and do not affect the behavior of the 21145.

Note: Reserved bits are shaded and should be written with 0. Failing to do this could cause incompatibility problems with a future version of the 21145. Reserved bits are undefined on read access.

Table 8-156 lists the definitions and addresses for the CardBus Status Changed registers.

Table 8-156. Modem Function CardBus Status Changed Register Mapping

Register	Meaning	Offset from Modem Function Base Address (CBIO and CBMA)
FER	Function event register	80H
FEMR	Function event mask register	84H
FPSR	Function present state register	88H
FFER	Function force event register	8CH

8.8.1 Function Event Register (FER–Offset 80H)

This register is the CardBus Status Changed function event register, which is used for reporting of interrupt pending and power-management event detection in a CardBus system.

Figure 8-78 shows the FER register bit fields and Table 8-157 describes the bit fields.

Figure 8-78. FER Register Bit Fields

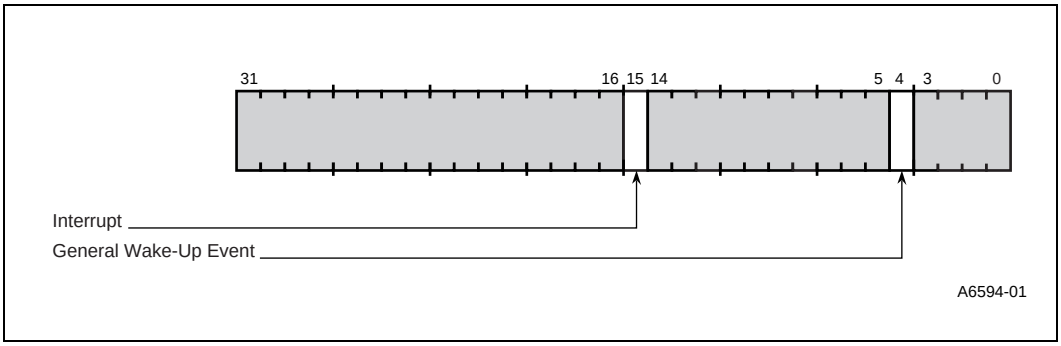


Table 8-157. FER Register Bit Fields Description

Field	Description
15	Interrupt This bit is set when there is an interrupt pending. This bit is cleared by write 1.
4	General Wake-Up Event This bit is set when the 21145 has detected a power management event. This bit is cleared upon power-up reset and by write 1. It is unaffected by either hardware or software reset. When the PME_Status bit in the modem function PCI configuration is cleared, this bit is automatically cleared as well.

Table 8-158 lists the access rules for the FER register.

Table 8-158. FER Register Access Rules

Category	Description
Value after reset	Undefined for reserved bits; 0 for bits that are not reserved.
Read access rules	—
Write access rules	—

8.8.2 Function Event Mask Register (FEMR–Offset 84H)

This register is the CardBus Status Changed function event mask register, which controls the assertion of the signals int_l, gep<2>/rcv_match/wake, and mdm_spkr_en in a CardBus system.

Figure 8-79 shows the FEMR register bit fields and Table 8-159 describes the bit fields.

Figure 8-79. FEMR Register Bit Fields

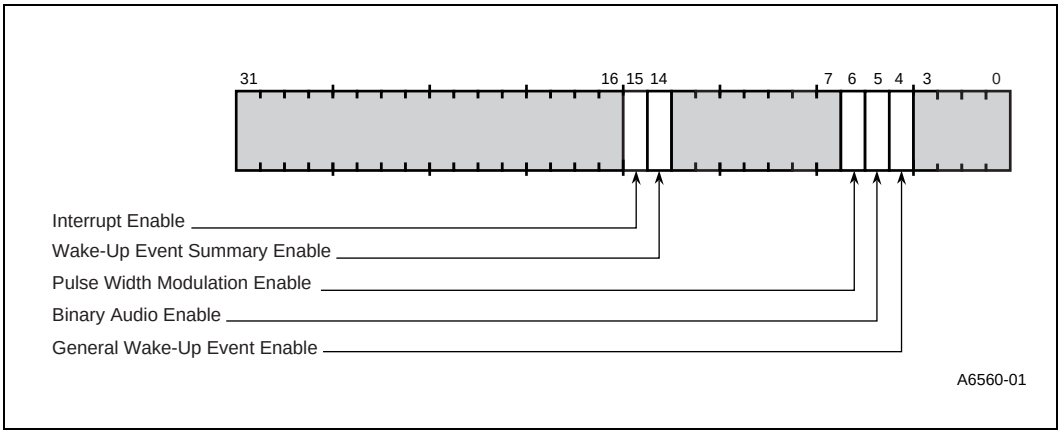


Table 8-159. FEMR Register Bit Fields Description

Field	Description
15	Interrupt Enable When set, enables an interrupt via assertion of the int_l pin.
14	Wake-Up Event Summary Enable When set together with the General Wake-Up Event Enable bit (FEMR<4>), enables the assertion of the gep<2>/rcv_match/wake pin. Note: To disable the assertion of the gep<2>/rcv_match/wake pin, the PME_Enable bit in the modem configuration register (CPMC<8>) must be cleared as well. This bit is cleared only upon a power-up reset.
6	Pulse Width Modulation Enable If func1_HwOptions<7> is cleared, the pulse width modulation enable bit is driven on the mdm_spkr_en pin. This bit cleared upon a hardware or software reset.
5	Binary Audio Enable If func1_HwOptions<7> is set, the binary audio enable bit is driven on the mdn_spkr_en pin. This bit is cleared upon a hardware or software reset.
4	General Wake-Up Event Enable When set together with the Wake-Up Event Summary Enable bit (FEMR<14>), enables the assertion of the gep<2>/rcv_match/wake pin. Note: To disable the assertion of the gep<2>/rcv_match/wake pin, the PME_Enable bit in the modem configuration register (CPMC<8>) must be cleared as well. This bit is cleared only upon a power-up reset.

Table 8-160 lists the access rules for the FEMR register.

Table 8-160. FEMR Register Access Rules

Category	Description
Value after reset	Undefined for reserved bits; 0 for bits that are not reserved.
Read access rules	—
Write access rules	—

8.8.3 Function Present State Register (FPSR–Offset 88H)

This register is the CardBus Status Changed function present state register, which is used for reporting the present state of the int_l and the gep<2>/rcv_match/wake pins in a CardBus system.

Figure 8-80 shows the FPSR register bit fields and Table 8-161 describes the bit fields.

Figure 8-80. FPSR Register Bit Fields

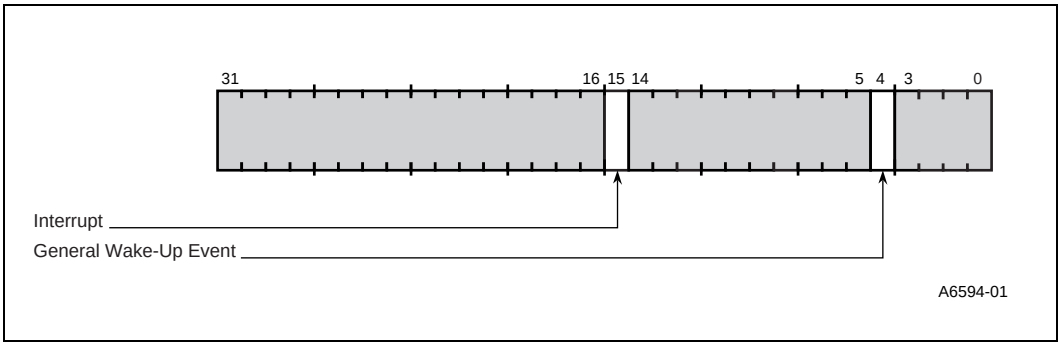


Table 8-161. FPSR Register Bit Fields Description

Field	Description
15	Interrupt This bit reflects the internal state of the Modem function interrupt line.
4	General Wake-Up Event Reflects the current state of the wake-up event. This bit is cleared when either the General Wake-Up Event in the function event register is cleared, or when the PME_Status bit in the CPMC is cleared. This bit is cleared only upon a power-up reset.

Table 8-162 lists the access rules for the FPSR register.

Table 8-162. FPSR Register Access Rules

Category	Description
Value after reset	Undefined for reserved bits; 0 for bits that are not reserved.
Read access rules	—
Write access rules	R/O

8.8.4 Function Force Event Register (FFER–Offset 8CH)

This register is the CardBus Status Changed function force event register, which is used to force the value of the interrupt and the general wake-up event bits in the function event register to a 1.

Figure 8-81 shows the FFER register bit fields and Table 8-163 describes the bit fields.

Figure 8-81. FFER Register Bit Fields

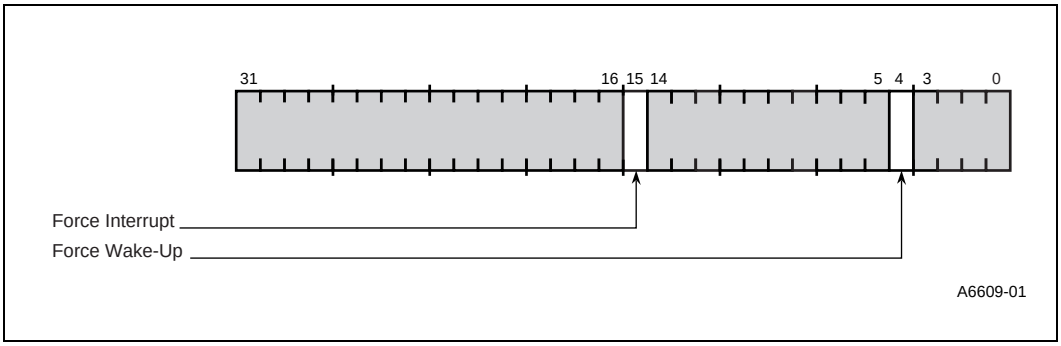


Table 8-163. FFER Register Bit Fields Description

Field	Description
15	Force Interrupt Writing 1 to this bit sets the Interrupt field in FER<15>, but not in FPSR<15>. If the interrupt is enabled, the 21145 also asserts the int_l pin. Writing 0 has no effect.
4	Force Wake-Up Writing 1 to this bit sets the wake-up event field in FER<4>, but not in FPSR<4>. If the wake-up event is enabled, the 21145 also asserts the gep<2>/rcv_match/wake pin. Writing 0 has no effect. This bit is cleared only upon a power-up reset.

Table 8-164 lists the access rules for the FFER register.

Table 8-164. FFER Register Access Rules

Category	Description
Value after reset	Undefined for reserved bits; 0 for bits that are not reserved.
Read access rules	W/O
Write access rules	—

DNA CSMA/CD Counters and Events Support A

This appendix describes the 21145 features that support the driver when implementing and reporting the specified counters and events[1]. CSMA/CD[2] specified events can be reported by the driver based on these features.

A.1 CSMA/CD Counters

Table A-1 lists the counters and features.

Table A-1. CSMA/CD Counters (Sheet 1 of 2)

Counter	21145 Feature
Time since creation counter	Supported by the host driver.
Bytes received	Driver must add the frame length (RDES0<29:16>) fields of all successfully received frames.
Bytes sent	Driver must add the buffer 1 size (TDES1<10:0>) and buffer 2 size (TDES1<21:11>) fields of all successfully transmitted buffers.
Frames received	Driver must count the successfully received frames in the receive descriptor list.
Frames sent	Driver must count the successfully transmitted frames in the transmit descriptor list.
Multicast bytes received	Driver must add the frame length (RDES0<29:16>) fields of all successfully received frames with multicast frame (RDES0<10>) set.
Multicast frames received	Driver must count the successfully received frames with multicast frame (RDES<10>) set.
Frames sent, initially deferred	Driver must count the successfully transmitted frames when deferred (TDES0<0>) is set.
Frames sent, single collision	Driver must count the successfully transmitted frames when the collision count (TDES0<6:3>) is equal to 1.
Frames sent, multiple collisions	Driver must count the successfully transmitted frames when the collision count (TDES0<6:3>) is greater than 1.
Send failure, excessive collisions	Driver must count the transmit descriptors when the excessive collisions (TDES0<8>) bit is set.
Send failure, carrier check failed	Driver must count the transmit descriptors when both late collision (TDES0<9>) and loss of carrier (TDES0<11>) are set.
Send failure, short circuit	There were two successive transmit descriptors when the no_carrier flag (TDES0<10>) is set. This indicates a short circuit.
Send failure, open circuit	There were two successive transmit descriptors when the excessive_collisions flag (TDES0<8>) is set. This indicates an open circuit.
Send failure, remote failure to defer	Flagged as a late collision (TDES0<9>) in the transmit descriptors.

1. As specified in the *DNA Maintenance Operations (MOP) Functional Specification*, Version T.4.0.0, 28 January 1988.
2. Carrier-sense multiple access with collision detection.

Table A-1. CSMA/CD Counters (Sheet 2 of 2)

Counter	21145 Feature
Receive failure, block check error	Driver must count the receive descriptors when CRC error (RDES0<1>) is set and dribbling bit (RDES0<2>) is cleared.
Receive failure, framing error	Driver must count the receive descriptors when both CRC error (RDES0<1>) and dribbling bit (RDES0<2>) are set.
Receive failure, frame too long	Driver must count the receive descriptors when frame too long (RDES0<7>) is set.
Unrecognized frame destination	Not applicable.
Data overrun	Driver must count the receive descriptors when (RDES0<0>) is set.
System buffer unavailable	Reported in the missed frame counter CSR8<15:0> (Section 8.3.2.11).
User buffer unavailable	Maintained by the driver.
Collision detect check failed	Driver must count the transmit descriptors when heartbeat fail (TDES0<7>) is set.

Hash C Routine B

This appendix provides examples of a C routine that generates the hash index for a given Ethernet address. The bit position in the hash table is taken from the CRC32 checksum derived from the first 6 bytes.

There are two C routines that follow: the first is for the little endian architecture and the second is for big endian architecture.

B.1 Little Endian Architecture Hash C Routine

```
#define CRC32_POLY   0xEDB88320UL   /* CRC-32 Poly -- Little Endian*/
#define HASH_BITS     9                      /* Number of bits in hash */

unsigned
crc32_mchash(
     unsigned char *mca)
{
    u_int idx, bit, data, crc = 0xFFFFFFFFUL;

    for (idx = 0; idx < 6; idx++)
        for (data = *mca++, bit = 0; bit < 8; bit++, data >>=1)
            crc = (crc >> 1) ^ (((crc ^ data) & 1) ? CRC32_POLY : 0);

    return crc & ((1 << HASH_BITS) - 1)  /* return low bits for hash */
}
```

B.2 Big Endian Architecture Hash C Routine

```
#include <stdio>
unsigned HashIndex (char *Address);

main (int argc, char *argv[]) {
   int Index;
   char m[6];
      if (argc < 2) {
      printf("usage: hash xx-xx-xx-xx-xx-xx\n");
      return;
   }
   sscanf(argv[1],"%2X-%2X-%2X-%2X-%2X-%2X",
     &m[0],&m[1],&m[2],
     &m[3],&m[4],&m[5]);

   Index = HashIndex(&m[0]);
```

```
    printf("hash_index = %d  byte: %d   bit: %d\n",
            Index,Index/8,Index%8);
}
unsigned HashIndex (char *Address) {

    unsigned Crc = 0xffffffff;
    unsigned const POLY  0x04c11db6
    unsigned Msb;
    int BytesLength = 6;

    unsigned char CurrentByte;
    unsigned Index;
    int Bit;
    int Shift;

    for (BytesLength=0; BytesLength<6; BytesLength++) {

      CurrentByte = Address[BytesLength];
      for (Bit=0; Bit<8 ; Bit++) {

         Msb = Crc >> 31;
         Crc  <<= 1;

         if ( Msb ^ (CurrentByte & 1)) {
             Crc ^= POLY;
             Crc |= 0x00000001;
         }
             CurrentByte >>= 1;
      }
     }

   /* the hash index is given by the upper 9 bits of the CRC
    * taken in decreasing order of significance
    * index<0> = crc<31>
    * index<1> = crc<30>
    * ...
    * index<9> = crc<23>
    */

    for (Index=0, Bit=23, Shift=8;
       Shift >= 0;
       Bit++, Shift--)  {
         Index |= (((Crc>>Bit) & 1) << Shift);

    }

    return Index;

}
```

Port Selection Procedure C

This appendix describes the port selection procedure for selecting one of the following 21145 ports:

MII
SYM
10BASE-T
HomePNA

These procedures provide the values to which the CSRs should be programmed, and also the order of programming. These procedures are for mode programming after reset, not for changing modes during operation. This appendix does not list all of the programming options. For additional options, refer to Table 8-86 through Table 8-90.

C.1 MII Port Selection

- Half-duplex mode
  CSR6<18> = 0
  CSR13<15:0> = 0000H
  CSR14<15:0> = 0000H
  CSR6<18> = 1
  CSR6<9> = 0
- Full-duplex mode
  CSR6<18> = 0
  CSR13<15:0> = 0000H
  CSR14<15:0> = 0000H
  CSR6<9> = 1, CSR6<18> = 1

C.2 SYM Port Selection

- Half-duplex mode
  CSR6<18> = 0
  CSR13<15:0> = 0000H
  CSR14<15:0> = 0000H
  CSR6<9> = 0, CSR6<18> = 1, CSR6<23> = 1, CSR6<24> = 1
- Full-duplex mode
  CSR6<18> = 0
  CSR13<15:0> = 0000H
  CSR14<15:0> = 0000H
  CSR6<9> = 1, CSR6<18> = 1, CSR6<23> = 1, CSR6<24> = 1

C.3 10BASE-T Port Selection

- Half-duplex mode
  CSR6<18> = 0
  CSR13<15:0> = 0000H
  CSR14<15:0> = 7F3FH
  CSR13<15:0> = 0001H
  CSR6<9> = 1
- Full-duplex mode
  CSR6<9> = 1, CSR6<18> = 0
  CSR13<15:0> = 0000H
  CSR14<15:0> = 7F3DH
  CSR13<15:0> = 0001H
- Auto-Negotiation advertising 10BASE-T and 100BASE-TX half-duplex and full-duplex ability
  CSR6<18> = 0
  CSR13<15:0> = 0000H
  CSR14<15:0> = 3FFFFH
  CSR13<15:0> = 0001H

C.4 HomePNA Port Selection

- HomePNA mode (assuming external envelope detector)
  CSR6<18> = 0, CSR6<19> = 1
  CSR13<31:0> = 00000000H
  CSR14<31:0> = 00000505H
  CSR15<4> = 1
  CSR13<31:0> = 30480009H

General-Purpose Port and LED Programming D

This appendix describes the procedure for programming the general-purpose port. The general-purpose port consists of the following pins:

Pin 100—gep<0>

Pin 101—gep<1>/activ

Pin 102—gep<2>/rcv_match/wake

Pin 103—gep<3>/link

The pins of the general-purpose port may be programmed for one of the following functions:

Input port with interrupt (gep<0> and gep<1> only)

Input port without interrupt

Output port

LED/Control (gep<1>, gep<2> and gep<3> only)

The procedures provide the CSR15 values for programming each of these functions. It uses 21145 pin 103 (gep<1>/activ) as an example. The CSR values provided in each line should be written in one CSR access.

D.1 Input Port Selection with Interrupt

To select the input port with the interrupt function, write the following values:

First write CSR15<27> = 1, CSR15<25> = 1, CSR15<21> = 0, CSR15<17> = 0

Then write CSR15<27> = 0.

D.2 Input Port Selection Without Interrupt

To select the input port without the interrupt function, write the following values:

First write CSR15<27> = 1, CSR15<25> = 0, CSR15<21> = 0, CSR15<17> = 0

Then write CSR15<27> = 0.

D.3 Output Port Selection

To select the output port function, write the following values:

First write CSR15<27> = 1, CSR15<21> = 0, CSR15<17> = 1

Then write CSR15<27> = 0.

D.4 LED/Control Selection

To select the LED/Control function, write the following values:

First write CSR15<27> = 1, CSR15<21> = 1

Then write CSR15<27> = 0.

Filtering Setup Frame Buffer Examples E

This appendix provides examples of perfect and imperfect filtering setup frame buffers.

Example E-1 shows a perfect filtering setup buffer (fragment).

Example E-1. Perfect Filtering Buffer

Ethernet addresses to be filtered:

A8-09-65-12-34-76 ①

09-BC-87-DE-03-15

.

.

.

Setup frame buffer fragment while in little endian

byte ordering:

xxxx09A8 ②

xxxx1265

xxxx7634

xxxxBC09

xxxxDE87

xxxx1503

.
.
.

Setup frame buffer fragment while in big endian byte ordering:

A809xxxx ③

6512xxxx

3476xxxx

09BCxxxx

87DExxxx

0315xxxx

.

.

.

1. Displays two Ethernet addresses written according to the Ethernet specification for address display.
2. Displays two addresses as they would appear in the buffer in little endian format.
3. Displays two addresses as they would appear in the buffer in big endian format.

Example E-2 shows an imperfect filtering setup frame buffer.

Example E-2. Imperfect Filtering Buffer

Ethernet addresses to be filtered:

25-00-25-00-27-00 ①

A3-C5-62-3F-25-87

D9-C2-C0-99-0B-82

7D-48-4D-FD-CC-0A

E7-C1-96-36-89-DD

61-CC-28-55-D3-C7

6B-46-0A-55-2D-7E

A8-12-34-35-76-08 ②

Setup frame buffer while in little endian byte ordering:

xxxx0000 ③

xxxx0000

xxxx0000

xxxx1000

xxxx0000

xxxx0000

xxxx0000

xxxx0000

xxxx0000

xxxx0000

xxxx0000

xxxx4000

xxxx0080

xxxx0000

xxxx0000

xxxx0010

xxxx0000

xxxx0000

xxxx0000

xxxx1000

xxxx0000

xxxx0000

xxxx0000

xxxx0000

xxxx0000

xxxx0000

xxxx0000

xxxx0001

xxxx0000

xxxx0000

xxxx0000

xxxx0040

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxx12A8 ④

xxxx3534

xxxx0876

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

Setup frame buffer while in big endian byte ordering:

0000xxxx ⑤

0000xxxx

0000xxxx

0010xxxx

0000xxxx

0000xxxx

0000xxxx

0000xxxx

0000xxxx

0000xxxx

0000xxxx

0040xxxx

8000xxxx

0000xxxx

0000xxxx

1000xxxx

0000xxxx

0000xxxx

0000xxxx

0010xxxx

0000xxxx

0000xxxx

0000xxxx

0000xxxx

0000xxxx

0000xxxx

0000xxxx

0100xxxx

0000xxxx

0000xxxx

0000xxxx

4000xxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

A812xxxx ⑥

3435xxxx

7608xxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

xxxxxxxx

1. Displays Ethernet multicast addresses written according to the Ethernet specification for address display.
2. Displays an Ethernet physical address.
3. Displays the first part of an imperfect filter setup frame buffer, in little endian byte ordering, with set bits for the multicast addresses as in 1.
4. Displays the second part of the buffer with the physical address as in 1, in little endian byte ordering.
5. Displays the first part of an imperfect filter setup frame buffer, in big endian byte ordering, with set bits for the multicast addresses as in 1.
6. Displays the second part of the buffer with the physical address as in 2, in big endian byte ordering.

Wake-Up Frame Filter Register Block Programming Examples F

This appendix provides examples of wake-up frame patterns and how the wake-up frame filter register block should be programmed.

Example F-1 describes the frame patterns for a wake-up with Unicast IP to node AB-00-04-01-D9-FA, Ethernet frame format only.

Example F-1. Wake-Up upon Unicast IP, Ethernet Frame Format

Wake-up pattern:

Offset (bytes)	Pattern (hex)	
00	AB 00 04 01 D9 FA	Destination MAC Address (Station Address)
12	08 00	Protocol Type (IP)

Frame data:

AB 00 04 01 D9 FA
XX XX XX XX XX XX
08 00

:

:

XX XX

Wake-up frame filter register's value:

Filter 0 Byte Mask	00000003	Pattern's bytes: 12, 13
Filter 0 Offset	0C	Offset = 12
Filter 0 Command	01	Unicast, Enable_filter
Filter 0 CRC16	7006	CRC16 (08, 00)

Filter 1, Filter 2, and Filter 3 are not being used.

Wake-up frame filter register block program sequence:

write CSR1-PM	00000003	(Filter 0 Byte Mask)
write CSR1-PM	00000000	(Filter 1 Byte Mask)
write CSR1-PM	00000000	(Filter 2 Byte Mask)
write CSR1-PM	00000000	(Filter 3 Byte Mask)
write CSR1-PM	00000001	(Filter 0-3 Command)
write CSR1-PM	0000000C	(Filter 0-3 Offset)
write CSR1-PM	00007006	(Filter 0-1 CRC16)
write CSR1-PM	00000000	(Filter 2-3 CRC16)

Note: The Destination MAC Address is detected by the 21145 address filtering mechanism and not by the frame filter. The address recognition RAM should be loaded with the AB-00-04-01-D9-FA address

(for information about the setting of the address recognition RAM, see Section 2.2.3 and Appendix G).

Example F-2 describes the filter formats for frames.

Example F-2. Filter Formats for Frames

Wake-up upon all various frames that are Unicast IPX to node AB-00-04-01-D9-FA. There are four possible formats for these frames:

- Ethernet frame with Ethernet type
- IEEE 802.3/802.2 SNAP frame
- IEEE 802.3/802.2 SAP frame
- IEEE 802.3/802.2 SAP frame with control

In order to wake up on each one of these formats, all four filters of the 21145 should be used (when each filter is programmed to detect one of these formats).

Ethernet frame with Ethernet type

Wake-up pattern:

Offset Pattern

(bytes) (hex)

00	AB 00 04 01 D9 FA	Destination MAC Address (Station Address)
12	81 37	Protocol Type (IPX)

Frame data:

AB 00 04 01 D9 FA
XX XX XX XX XX XX
81 37
:
:
XX XX

Wake-up frame filter register's value:

Filter 0 Byte Mask	00000003	Pattern's bytes: 12, 13
Filter 0 Offset	0C	Offset = 12
Filter 0 Command	01	Unicast, Enable_filter
Filter 0 CRC16	3620	CRC16 (81, 37)

IEEE 802.3/802.2 SNAP frame

Wake-up pattern:

Offset Pattern

(bytes) (hex)

00	AB 00 04 01 D9 FA	Destination MAC Address (Station Address)
14	AA AA 03 00 00 00 81 37	SAP + Protocol Type (IPX)

Frame data:

AB 00 04 01 D9 FA
XX XX XX XX XX XX
XX XX
AA AA 03 00 00 00
81 37
:
:
XX XX

Wake-up frame filter register's value:

Filter 1 Byte Mask 000000FF Pattern's bytes: 14..21
Filter 1 Offset 0E Offset = 14
Filter 1 Command 01 Unicast, Enable_filter
Filter 1 CRC16 B3E1 CRC16 (AA..37)
IEEE 802.3/802.2 SAP frame

Wake-up pattern:

Offset Pattern

(bytes) (hex)
00 AB 00 04 01 D9 FA Destination MAC Address (Station Address)
14 FF FF Protocol Type (IPX)

Frame data:

AB 00 04 01 D9 FA
XX XX XX XX XX XX
XX XX
FF FF
:
:
XX XX

Wake-up frame filter register's value:

Filter 2 Byte Mask 00000003 Pattern's bytes: 14, 15
Filter 2 Offset 0E Offset = 14
Filter 2 Command 01 Unicast, Enable_filter
Filter 2 CRC16 0000 CRC16 (FF, FF)
IEEE 802.3/802.2 SAP frame with control

Wake-up pattern:

Offset Pattern

(bytes) (hex)
00 AB 00 04 01 D9 FA Destination MAC Address (Station Address)

14 E0 E0 03 SAP + Control (IPX)

Frame data:

AB 00 04 01 D9 FA
XX XX XX XX XX XX
XX XX
E0 E0 03
:
:
XX XX

Wake-up frame filter register's value:

Filter 3 Byte Mask	00000007	Pattern's bytes: 14..16
Filter 3 Offset	0E	Offset = 14
Filter 3 Command	01	Unicast, Enable_filter
Filter 3 CRC16	F779	CRC16 (E0, E0, 03)

Wake-up frame filter register block program sequence:

write CSR1-PM	00000003	(Filter 0 Byte Mask)
write CSR1-PM	000000FF	(Filter 1 Byte Mask)
write CSR1-PM	00000003	(Filter 2 Byte Mask)
write CSR1-PM	00000007	(Filter 3 Byte Mask)
write CSR1-PM	01010101	(Filter 0-3 Command)
write CSR1-PM	0E0E0E0C	(Filter 0-3 Offset)
write CSR1-PM	B3E13620	(Filter 0-1 CRC16)
write CSR1-PM	F7790000	(Filter 2-3 CRC16)

Note: The Destination MAC Address is detected by the 21145 address filtering mechanism and not by the frame filter. The address recognition RAM should be loaded with the AB-00-04-01-D9-FA address (for information about the setting of the address recognition RAM, see Section 2.2.3 and Appendix G).

Example F-3 describes the filter formats for frames.

Example F-3. Filter Formats for Frames

Wake-up upon IPv6 neighbor solicitation to node 4037.0.0.0.1.800.200E.8C6C, Ethernet frame only.

The pattern of this frame contains 18 bytes, but they do not reside in 31 contiguous bytes. There are two possibilities to detect frames with this format:

- Use two of the 21145 filters with the add previous command for combining the two filters into one longer pattern matching.
- Use only one filter and check only a part of the pattern.

This example shows how the 21145 wake-up frame filter registers should be programmed for each of the two options.

Wake-up pattern:

Offset (bytes) (hex)	Pattern	
00	FF FF FF FF FF FF	Destination MAC Address (Broadcast)
12	08 00	Protocol Type (IP)
38	FF 02 00 00 00 00 00 00	IP Destination Address (target's
	00 00 00 01 20 0E 8C 6C	solicited-node multicast address)

Frame data:

FF FF FF FF FF FF
XX XX XX XX XX XX
08 00
XX XX XX XX XX XX
XX XX XX XX XX XX
XX XX XX XX XX XX
XX XX XX XX XX XX
FF 02 00 00 00 00 00 00
00 00 00 01 20 0E 8C 6C
:
:
XX XX

Full pattern matching with add previous:

Wake-up frame filter register's value:

Filter 0 Byte Mask	00000003	Pattern's bytes: 12, 13
Filter 0 Offset	0C	Offset = 12
Filter 0 Command	01	Unicast, Enable_filter
Filter 0 CRC16	7006	CRC16 (08, 00)
Filter 1 Byte Mask	0000FFFF	Pattern's bytes: 38..53

Filter 1 Offset	26	Offset = 38
Filter 1 Command	0D	Multicast, And_Previous, Enable_filter
Filter 1 CRC16	6F0E	CRC16 (FF, 02...8C, 6C)

Wake-up frame filter register block program sequence:

write CSR1-PM	00000003	(Filter 0 Byte Mask)
write CSR1-PM	0000FFFF	(Filter 1 Byte Mask)
write CSR1-PM	00000000	(Filter 2 Byte Mask)
write CSR1-PM	00000000	(Filter 3 Byte Mask)
write CSR1-PM	00000D01	(Filter 0-3 Command)
write CSR1-PM	0000260C	(Filter 0-3 Offset)
write CSR1-PM	6F0E7006	(Filter 0-1 CRC16)
write CSR1-PM	00000000	(Filter 2-3 CRC16)

Partial pattern matching with one filter:

Wake-up frame filter register's value:

Filter 0 Byte Mask	0000FFFF	Pattern's bytes: 38..53
Filter 0 Offset	26	Offset = 38
Filter 0 Command	09	Multicast, Enable_filter
Filter 0 CRC16	6F0E	CRC16 (FF, 02...8C, 6C)

Wake-up frame filter register block program sequence:

write CSR1-PM	0000FFFF	(Filter 0 Byte Mask)
write CSR1-PM	00000000	(Filter 1 Byte Mask)
write CSR1-PM	00000000	(Filter 2 Byte Mask)
write CSR1-PM	00000000	(Filter 3 Byte Mask)
write CSR1-PM	00000009	(Filter 0-3 Command)
write CSR1-PM	00000026	(Filter 0-3 Offset)
write CSR1-PM	00006F0E	(Filter 0-1 CRC16)
write CSR1-PM	00000000	(Filter 2-3 CRC16)

Note: The Destination MAC Address is detected by the 21145 address filtering mechanism and not by the frame filter. The 21145 should be programmed to receive broadcast frame.

The HomePNA PHY Register Interface G

This interface is used to access the HomePNA PHY's internal registers. This appendix describes the register access procedure through CSR9. For a description of the HomePNA PHY's commands and registers, see Section 8.5

This interface is controlled by writing and reading CSR9<23:20>. The following instructions illustrate how a write or read command should be issued utilizing CSR9. It should be noted that before any write operation to the HomePNA CSRs, the SET_WE (write enable) command should be issued.

SET WRITE ENABLE (SET_WE) COMMAND (COMMAND = 0000 0110)

1. Write CSR9 with CS=0, SCLK=0, SI=SO=don't care
2. Write CSR9 with CS=1, SCLK=0, SI=SO=don't care
3. Write CSR9 with CS=1, SCLK=0, SI= command bit<7>=0, SO=don't care
4. Write CSR9 with CS=1, SCLK=1, SI= command bit<7>=0, SO=don't care
5. Write CSR9 with CS=1, SCLK=0, SI= command bit<6>=0, SO=don't care
6. Write CSR9 with CS=1, SCLK=1, SI= command bit<6>=0, SO=don't care
7. Write CSR9 with CS=1, SCLK=0, SI= command bit<5>=0, SO=don't care
8. Write CSR9 with CS=1, SCLK=1, SI= command bit<5>=0, SO=don't care
9. Write CSR9 with CS=1, SCLK=0, SI= command bit<4>=0, SO=don't care
10. Write CSR9 with CS=1, SCLK=1, SI= command bit<4>=0, SO=don't care
11. Write CSR9 with CS=1, SCLK=0, SI= command bit<3>=0, SO=don't care
12. Write CSR9 with CS=1, SCLK=1, SI= command bit<3>=0, SO=don't care
13. Write CSR9 with CS=1, SCLK=0, SI= command bit<2>=1, SO=don't care
14. Write CSR9 with CS=1, SCLK=1, SI= command bit<2>=1, SO=don't care
15. Write CSR9 with CS=1, SCLK=0, SI= command bit<1>=1, SO=don't care
16. Write CSR9 with CS=1, SCLK=1, SI= command bit<1>=1, SO=don't care
17. Write CSR9 with CS=1, SCLK=0, SI= command bit<0>=0, SO=don't care
18. Write CSR9 with CS=1, SCLK=1, SI= command bit<0>=0, SO=don't care
19. Write CSR9 with CS=0, SCLK=0, SI=SO=don't care
20. Write CSR9 with CS=0, SCLK=1, SI=SO=don't care

BYTE WRITE OPERATION (COMMAND = 0000 0010)

1. Write CSR9 with CS=0, SCLK=0, SI=SO=don't care
2. Write CSR9 with CS=1, SCLK=0, SI=SO=don't care
3. Write CSR9 with CS=1, SCLK=0, SI= command bit<7>=0, SO=don't care
4. Write CSR9 with CS=1, SCLK=1, SI= command bit<7>=0, SO=don't care

And this goes on until the last command bit:

1. Write CSR9 with CS=1, SCLK=0, SI= command bit<0>=0, SO=don't care
2. Write CSR9 with CS=1, SCLK=1, SI= command bit<0>=0, SO=don't care
3. Write CSR9 with CS=1, SCLK=0, SI= byte-address-bit<7>, SO=don't care
4. Write CSR9 with CS=1, SCLK=1, SI= byte-address-bit<7>, SO=don't care
5. Write CSR9 with CS=1, SCLK=0, SI= byte-address-bit<6>, SO=don't care
6. Write CSR9 with CS=1, SCLK=1, SI= byte-address-bit<6>, SO=don't care

And this goes on until the last address bit (bit <0> of the address)

1. Write CSR9 with CS=1, SCLK=0, SI= byte-address-bit<0>, SO=don't care
2. Write CSR9 with CS=1, SCLK=1, SI= byte-address-bit<0>, SO=don't care
3. Write CSR9 with CS=1, SCLK=0, SI= data-byte-bit<7>, SO=don't care
4. Write CSR9 with CS=1, SCLK=1, SI= data-byte-bit<7>, SO=don't care

And this goes on until the last data byte:

1. Write CSR9 with CS=1, SCLK=0, SI= data-byte-bit<0>, SO=don't care
2. Write CSR9 with CS=1, SCLK=1, SI= data-byte-bit<0>, SO=don't care
3. Write CSR9 with CS=0, SCLK=0, SI=SO=don't care
4. Write CSR9 with CS=0, SCLK=1, SI=SO=don't care

BYTE READ OPERATION (COMMAND = 0000 0011)

1. Write CSR9 with CS=0, SCLK=0, SI=SO=don't care
2. Write CSR9 with CS=1, SCLK=0, SI=SO=don't care
3. Write CSR9 with CS=1, SCLK=0, SI= command bit<7>=0, SO=don't care
4. Write CSR9 with CS=1, SCLK=1, SI= command bit<7>=0, SO=don't care

And this goes on until the last command bit:

1. Write CSR9 with CS=1, SCLK=0, SI= command bit<0>=1, SO=don't care
2. Write CSR9 with CS=1, SCLK=1, SI= command bit<0>=1, SO=don't care
3. Write CSR9 with CS=1, SCLK=0, SI= byte-address-bit<7>, SO=don't care
4. Write CSR9 with CS=1, SCLK=1, SI= byte-address-bit<7>, SO=don't care
5. Write CSR9 with CS=1, SCLK=0, SI= byte-address-bit<6>, SO=don't care
6. Write CSR9 with CS=1, SCLK=1, SI= byte-address-bit<6>, SO=don't care

And this goes on until the last bit (bit <0> of the address)

1. Write CSR9 with CS=1, SCLK=0, SI= byte-address-bit<0>, SO=don't care
2. Write CSR9 with CS=1, SCLK=1, SI= byte-address-bit<0>, SO=don't care
3. Write CSR9 with CS=1, SCLK=0, SI=SO=don't care
4. Read CSR9: SO = data-bit<7>

5. Write CSR9 with CS=1, SCLK=1, SI=SO=don’t care
6. Write CSR9 with CS=1, SCLK=0, SI=SO=don’t care
7. Read CSR9: SO = data-bit<6>
8. Write CSR9 with CS=1, SCLK=1, SI=SO=don’t care
9. Write CSR9 with CS=1, SCLK=0, SI=SO=don’t care
10. Read CSR9: SO = data-bit<5>
11. Write CSR9 with CS=1, SCLK=1, SI=SO=don’t care

And this goes on until the last bit of the data:

1. Write CSR9 with CS=1, SCLK=0, SI=SO=don’t care
2. Read CSR9: SO = data-bit<0>
3. Write CSr9 with CS=1, SCLK=1, SI=SO=don’t care
4. Write CSR9 with CS=0, SCLK=0, SI=SO=don’t care
5. Write CSR9 with CS=0, SCLK=1, SI=SO=don’t care

HomePNA Telephone Line Interface H

This section details the 21145 HomePNA telephone line interface signals, as well as timing diagrams and specification.

H.1 Pin Description

Table H-1 describes the HomePNA pins.

Table H-1. HomePNA Telephone Line Pins

Signal	Type	Pin Number, 176-pin package	Pin Number, 144-pin package	Description
hr_rx_n	I	175	143	Negative differential receive input from the phone line.
hr_rx_p	I	174	142	Positive differential receive input from the phone line.
hr_txp	O	11	11	Positive differential transmit output with hr_txn.
hr_txn	O	12	12	Negative differential transmit output with hr_txp.
hr_txph	O	13	13	High-power positive differential transmit output with hr_txnh. Changes polarity at low HomePNA power levels.
hr_txnh	O	14	14	High power negative differential transmit output with hr_txph. Changes polarity at low HomePNA power levels.

H.2 HomePNA Transmit Output Pin Configuration

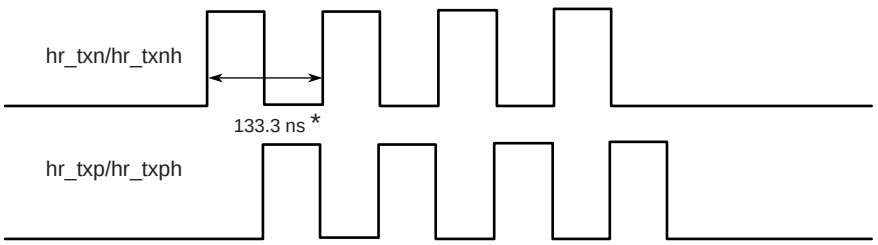
For the pin configuration, see Table H-2; for the transmit waveforms, see Figure H-1.

Table H-2. HomePNA Transmit Pin Configuration[1]

Power	Parameter	hr_txp	hr_txph	hr_txn	hr_txnh
High power	V_{oh}	1	1	0	0
High power	V_{ol}	0	0	1	1
Low power	V_{oh}	0	1	1	0
Low power	V_{ol}	1	0	0	1

1. When no pulse is being transmitted, all four pins drive 0.

Figure H-1. Transmit Output Waveform Mask, One Symbol. Without load. 500PPM



* The pulse width depends on the value written in the HomePNA PHY TX_PULSE_WIDTH register. 133.3 ns is the default value, which is also the recommended value.

A6440-01

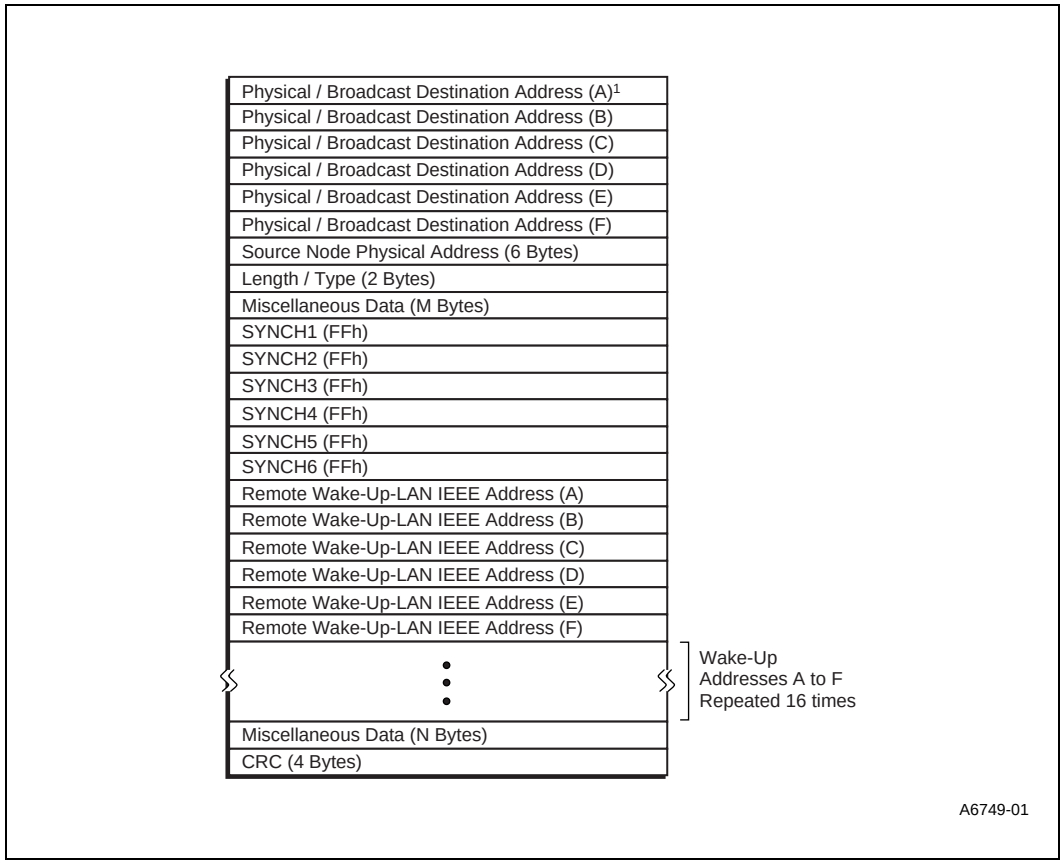
Magic Packet Format

I

This appendix describes the 21145 Magic Packet format.

Figure I-1 shows the structure of a Magic Packet used in the 21145

Figure I-1. Magic Packet Format for the 21145



Example I-1 shows the fields of a 21145 Magic Packet.

Example I-1. 21145 Magic Packet Fields

```
Physical Destination Address (A-B-C-D-E-F) 08-00-2B-11-22-33

Source Node Physical Address 08-00-2B-44-55-66

Length/Type 00-00

The Magic Packet for the 21145 would consist of the following data plus four bytes
of CRC (transmitted in byte order from left to right, and top to bottom):

(A——B——C——D——E——F)
08 00 2B 11 22 33(Remote Wake-Up-LAN IEEE Address A to F)
08 00 2B 44 55 66(Source Node Physical Address)
00 00(Length/Type Field)
FF FF FF FF FF FF(Synchronization Pattern)
08 00 2B 11 22 33(Remote Wake-Up-LAN IEEE Address A to F)
08 00 2B 11 22 33(Remote Address A to F Repeated 16 Times)
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
08 00 2B 11 22 33
00 00 00 00 00 00
```

Note: The match is performed byte by byte. If one address does not match, the 21145 scans the Magic Packet for another synchronization pattern and repeats the match process. The 21145 makes no assumption of the content of the source node physical address. For example, the source node physical address can start with consecutive FF or have FF at any place in the 6-byte address field.

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