Using the Intel 21143 with the Quality Semiconductor QS6611 Revision D4

Application Note

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Application Note

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1.0 Introduction

The Intel 21143 can be used with a number of 100-Mb/s physical layer transceivers. One of these transceivers is the Quality Semiconductor QS6611. Intel has developed a reference design and an evaluation board based upon the 21143 with the QS6611. This application note is intended to provide information to our 21143 customers about a possible problem that could occur in designs using the latest QS6611 revision, known as the D4 revision. The information in this note is expected to be applicable to future QS6611 revisions.

2.0 Problem Statement

The Quality Semiconductor QS6611 transceiver, revision D4, does not perform an internal reset upon power-up. This is unlike previous QS6611 revisions that did perform a power-up reset. To overcome this limitation, an external hardware reset must be issued to the QS6611 in order to guarantee correct operation. The hardware reset to the QS6611 can be generated by adding an additional reset chip, such as the Dallas Semiconductor* DS1233, or this reset can be issued by the 21143 with some software support.

3.0 Resetting the QS6611 Using the 21143

When the 21143 is used with the QS6611 in an application that does not make use of the 21143's Wake-up-LAN or ACPI features, the 21143's general-purpose port and its software driver can be used to perform this hardware reset. In a Wake-up-LAN or ACPI implementation using the 21143 with the QS6611, some external circuitry may be required to ensure that the QS6611 is properly initialized in all power modes. For PCCard CardBus* designs, in addition to assuring that the QS6611 is reset properly, it is necessary to also ensure that the QS6611 powers up in its low-power mode (PD* asserted).

To address these different design applications, this application note is organized into different design categories, as follows:

- Case 1: PCI Applications Without Wake-up-LAN or ACPI
- Case 2: PCI Applications Using Wake-up-LAN or ACPI
- Case 3: PCCard CardBus Applications

3.1 Case 1: PCI Applications Without Wake-up-LAN or ACPI

This section is intended to provide information to ensure that the QS6611 is reset for all PCI designs that do not make use of the 21143's Wake-up-LAN or ACPI features.

The 21143 has a four-pin general-purpose port (GEP) that is programmable via CSR15. Each of these pins can be configured to be either an input or an output. By accessing CSR15, the software driver can read values from the GEP input pins or write values to the GEP output pins.

One of the GEP pins may be used to provide a reset to the QS6611. To do this, one GEP pin can be directly connected to the RESET* pin of the QS6611. The software driver can then be used to setup the GEP pin as an output and toggle the state of this pin. This will issue a reset to the QS6611.

Note: This solution assumes that the PD* input of the QS6611 is not connected to a general-purpose pin of the 21143. If the PD* signal is connected to a different general-purpose pin, then refer to the solution described in Case 3. The PD* and RESET* signals should not be connected to the same general-purpose pin.

The drivers developed by Intel provide support for issuing a reset to the QS6611. The driver reads data about the GEP pins from the SROM and applies the data to the GEP pins through write operations to CSR15. The reset occurs as a secondary effect of programming the 21143's general-purpose port. To fully understand the method, it is recommended to refer to the *Intel 21x4 serial ROM format V3.03* or later, and the *21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual* (HRM). See "Support, Products, and Documentation" for information on these documents.

For developers of drivers outside of Intel, if the application involves a QS6611 PHY, it is necessary to ensure that this method of resetting the QS6611 is observed in the software, or that there is some other method to guarantee that the QS6611 has been reset.

3.1.1 Reset Technique

When the 21143 is used with a symbol-mode PHY such as the QS6611, the serial ROM media blocks that can be used are Type 2 and Type 4. The Type 2 block is used for 10-Mb/s media (10BASE-T, BNC, AUI, or 10BASE-T full duplex). The Type 4 block is used to specify the 100-Mb/s media (100BASE-TX, 100BASE-TX full duplex). A typical application of the 21143 with the QS6611 would have four media blocks: two Type 2 blocks (10BASE-T and 10BASE-T full duplex) and two Type 4 blocks (100BASE-TX and 100BASE-TX full duplex).

In each of the Type 2 and Type 4 block types there are two 16-bit fields titled Port Control and general-purpose Port Data. The 16 bits of each of these fields map directly to CSR15<31:16>. The values contained in the Control and Data fields are written as two consecutive writes to CSR15<31:16> every time the particular media is selected. The Control field determines which GEP pins will be set up as LEDs, general-purpose inputs, or general-purpose outputs. The Data field determines the output logic state to be used for the general-purpose output pins. See the *21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manua* for details about CSR15. The Control field is a write to CSR15<31:16> with bit 27 (Control Write Enable) set; the Data field is a write to CSR15<31:16> with bit 27 cleared.

In order to perform the software-controlled reset to the QS6611, the Control field should set the GEP pin that is connected to the QS6611 RESET* to be a general-purpose output. The Data field should set a data value of '1' on this pin (reset inactive). For example, if GEP1 is used to reset the PHY, and all other general-purpose pins are performing their LED functions, the Control field would be programmed to 08D2h and the Data field would be 0002h.

Each time that this sequence is executed (regardless of the media selected), the reset of the PHY will occur between the two successive writes to CSR15. (The first write was for the Control word; the second write, for the Data word.) The reset occurs because the initial value of a general-purpose output pin is always'0' (by design) following the write of any Control word. During the period of time between the two successive writes to CSR15, the general-purpose output pin will be driving a '0'. If the SROM programming guidelines are followed, the width of the reset pulse is longer than 100 ms in each of the drivers developed by Intel, and this meets the QS6611 reset specification. Though the reset occurs as a consequence of the general-purpose port programming, it is a reliable method to reset the QSI PHY.

3.2 Case 2: PCI Applications Using Wake-up-LAN or ACPI

When the 21143 is used in a Wake-up-LAN or ACPI application, some external circuitry may be required to properly reset the QS6611 during situations where the network controller is expected to be active without a driver ever having been loaded.

In Wake-up-LAN or ACPI mode of operation, the 21143 senses the system power status through the vdd_clamp pin. In a Wake-up-LAN application, when system power is off (vdd_clamp is low) and the 21143 is powered by an auxiliary power supply, the 21143 monitors the network for a wake-up packet. In an ACPI application, when system power is off (vdd_clamp is low), the 21143 is powered by an auxiliary power supply, AND the 21143 is operating in its D0 state, the 21143 monitors the network for a wake-up packet.

If both the main and auxiliary power have been off (that is, the system has been removed) and auxiliary power is restored without main power, the 21143 automatically enters a mode where it is monitoring the network for a wake-up packet. In this situation, it is necessary to ensure that external logic has forced a power-up reset to the QS6611.

This is required because the QS6611 must have been reset in order to guarantee that the 21143 can detect a wake-up packet. In this case, the additional logic must issue a reset pulse of at least 100 ms to the QS6611. This external logic may be used in addition to, or in place of, the GEP reset techniques discussed in the previous sections.

Note: GEP0 should not be used for resetting the PHY because it provides an AUI/BNC select function during Wake-up-LAN operation. GEP2 should not be used for resetting the PHY because this signal reports the wake-up event to the system after a wake-up packet has been received.

3.3 Case 3: PCCard CardBus Applications

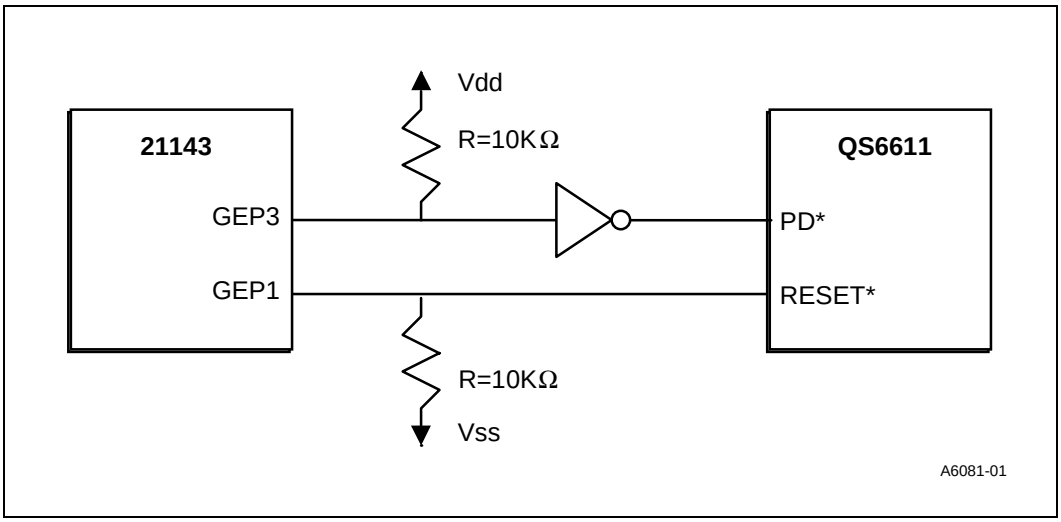
In PCCard CardBus applications where power consumption is critical, it is necessary to ensure that the QS6611's PD* input is low during power-up of the CardBus adapter. This assures that a CardBus adapter based on the 21143 and QS6611 can meet the 70-mA maximum current requirement at power-up. This section describes a recommended technique that meets this requirement, and also ensures that the QS6611 is properly reset using the 21143's general-purpose port.

The solution in this section is also applicable to PCI designs where the QS6611's PD* is connected to a different general-purpose pin than the QS6611's RESET* pin.

Figure 1 shows a suggested connection of the 21143's general-purpose port to the QS6611's RESET* and PD* signals. At power-up, the 21143's general-purpose port signals are all defined to be general-purpose inputs. For the circuit in Figure 1, when the board is initially powered up, the QS6611 will be powered down (by the external pull-up resistor and inverter). When the general-purpose port is written with a control word that defines both GEP3 and GEP1 as outputs, both GEP3 and GEP1 will drive a '0' value.

This initial value of '0' occurs by design any time that a control word is written. The '0' values will cause the QS6611 to be removed from its PowerDown state and issue a reset of the PHY. The reset can be cleared by writing a data word to the general-purpose register with a '1' value for GEP1 (and a '0' value for GEP3).

Figure 1. Power Down and Reset Connections



When the appropriate SROM programming is followed, the drivers developed by Intel can provide both the assertion of the reset pulse and deassertion of PD* to the QS6611. The technique is identical to the description in Case 1, with the additional requirement that the general-purpose pin connected to the QS6611's PD* is defined as an output, and is deasserted during normal operation.

3.3.1 Reset Technique

When the 21143 is used with a symbol-mode PHY such as the QS6611, the serial ROM media blocks that can be used are Type 2 and Type 4. The Type 2 block is used for 10-Mb/s media (10BASE-T, BNC, AUI, or 10BASE-T full duplex). The Type 4 block is used to specify the 100-Mb/s media (100BASE-TX, 100BASE-TX full duplex). A typical application of the 21143 with the QS6611 would have four media blocks: two Type 2 blocks (10BASE-T and 10BASE-T full duplex) and two Type 4 blocks (100BASE-TX and 100BASE-TX full duplex).

In each of the Type 2 and Type 4 block types there are two 16-bit fields titled General-Purpose Port Control and General-Purpose Port Data. The 16-bits of each of these fields map directly to CSR15<31:16>. The values contained in these two fields are written as two consecutive writes to CSR15<31:16> every time that this particular media is selected. The Control field determines which GEP pins will be setup as LEDs, general-purpose inputs or general-purpose outputs. The Data field determines the output logic state to be used for the general-purpose output pins. See Table 3-65 in the 21143 HRM for details about the bits of CSR15. The Control field is a write to CSR15<31:16> with bit 27 (Control Write Enable) set; the Data field is a write to CSR15<31:16> with bit 27 cleared.

In order to reset to the QS6611, the Control field should set so that the GEP pins connected to the QS6611 RESET* and PD* inputs are defined as general-purpose outputs. The Data field should set a data value of '1' on the RESET* pin (reset inactive) and a '0' on the PD* pin (this is inverted to make PowerDown inactive). For example, if GEP1 is used to reset the PHY and GEP3 is connected to PowerDown through an inverter (as shown in Figure 1), the Control field would be programmed to 085Ah and the Data field would be 0002h (GEP2 and GEP0 are defined as LEDs).

Each time that this sequence is executed (regardless of the media selected), PowerDown will be inactive, and a reset of the PHY will occur between the two successive writes to CSR15 (write #1 was for the Control word; write #2 for the Data word). The reset occurs because the initial value of

a general-purpose output pin is always ‘0’ following the write of any Control word. During the period of time between the two successive writes to CSR15, the general-purpose output pins will be driving a ‘0’. If the SROM programming guidelines are followed, the width of this reset pulse is longer than 100 ms in each of the drivers developed by Intel, and this meets the QS6611 reset specification. Though the reset occurs as a consequence of the general-purpose port programming, it is a reliable method to reset the QSI PHY.

Appendix A Verifying That the SROM Has Reset Information

This appendix describes how to review and/or modify the SROM template to assure that the reset will be issued to the QS6611 PHY.

On a DOS system, use SROMUTIL to examine the contents of the SROM:

1. SROMUTIL/ENGINEERING

   You may be prompted with several questions about entering subvendor ID blocks, Magic Packet*, or other information. All of these entries can be responded to with ‘No’ (or appropriate data can be provided).

2. From the SROM->Read Device menu, select the 21143 controller.
3. In the DS21143 Info window, all defined media types will be displayed.

   A typical application of the 21143 with the QS6611 will have four media types defined:

   a. TP (10BASET)

   b. TP Full Duplex (10BASET)

   c. SYM_SCR (100BASE-TX)

   d. SYM_SCR Full Duplex (100BASE-TX)

4. To use (or verify) the Reset Method:

   a. Select one of the defined media.

   b. In the Media Info window, there are fields for General-Purpose Port Control and General-Purpose Port Data. These are 4-bit hexadecimal fields that map directly to CSR15<31:16>.

      Ensure that the Control field sets the desired GEP pin to be an output and that the Data field sets the value on this GEP pin to ‘1’ (reset inactive). See Table 3-65 in the 21143 HRM for details about CSR15<31:16>.

   c. Repeat steps ‘a’ and ‘b’ for all defined media.

5. Backtrack through the menus until you get to the window titled SROM.
6. If changes were made to the SROM data, Select the File->Save Data menu and provide a filename (abcd.txt).
7. Reprogram the SROM using the SROMPROD utility:SROMPROD template=abcd.tx

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