21140-AF to 21143-xD Upgrade

Application Note

Revision 1.0

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Revision History

Revision Date	Revision	Description
June 1998	1.0	First version

1.0 Overview

The purpose of this document is to provide customers of the 21140-AF with information to upgrade to a new and more powerful Ethernet controller device, the 21143-xD.

This document describes how to upgrade your designs from the 21140-AF (order number 21140-AF) to the 21143-xD (order numbers 21143-PD and 21143-TD). It also describes register-level differences, and serves as a convenient reference for upgrading customer-developed 21140-AF drivers to work with the 21143-xD.

For detailed programming information and for register descriptions, consult the *DIGITAL Semiconductor 21140A PCI Fast Ethernet LAN Controller Hardware Reference Manual*, and the *DIGITAL Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual*.

2.0 Advantages of Upgrading to the 21143-xD

The 21143-xD offers the following features and performance enhancements:

- Fully integrates the SIA interface, including 10BASE-T and AUI capability, with full autonegotiation (NWAY) function support.
- Supports network device class OnNow* requirements for Microsoft's PC97 and PC98 specifications, including all wake-up events:
  - — Pattern matching
  - — Link change
  - — Magic Packet*
- Fully compliant with *Advanced Configuration and Power Interface (ACPI) specification, Revision 1.0*
- Fully compliant with *PCI Bus Power Management Interface specification, Revision 1.0*
- Supports CardBus* and has the following CardBus features:
  - — Supports storage of the CardBus Card Information Structure (CIS), also known as tuples, in the serial ROM or the external flash ROM.
  - — Supports automatic loading of the CIS pointer from the serial ROM.
  - — CardBus cstschg pin and Status Change registers.
- Supports PCI/CardBus clock control through clkrun.
- Supports interrupt mitigation on transmit and receive.
- Fully supports autodetection among three network ports: 10BASE-T (10 Mbp/s), AUI (10 Mbp/s), and MII/SYM (10/100 Mbp/s).
- Consumes less power through more efficient FIFOs and by defaulting to the sleep power mode after reset.
- Available in two package types:
  - — 21143-PD is in MQFP, ideal for Network Interface Card, LAN-On-Motherboard, or embedded systems.
  - — 21143-TD is in LQFP, a small, lower profile package, ideal for hand-held PC, laptop, CardBus, or any system where smaller IC packages are needed.

3.0 Cross Referencing Package Markings

Use the following table to cross-reference the 21140-AF and 21143-xD package markings with related documentation.

External Order Number	Device	Internal Part Number	Device Type and Revision	Hardware Reference Manual Number	Data Sheet Number
21140-AF	21140A	21-43864-04	DC1064C	EC-QN7NF-TE	EC-QN7PF-TE
21143-PD	21143	N/A	DC1096-B	EC-QWC4F-TE	EC-QWC3F-TE
21143-TD	21143	N/A	DC1096-B	EC-QWC4F-TE	EC-QWC3F-TE

4.0 Migrating Drivers

Software compatibility is retained for those customers utilizing Intel's DC21x4 drivers, allowing the same drivers and SROM format to be used with the 21143-xD that were used for the 21140-AF. For those customers who have developed their own drivers and require register information, see Section 6.0 in this upgrade document.

The following table lists the network and communications software available for the 21143-xD. For the latest driver and software information, see the Developer Area for Networking Components on the Intel World Wide Web at:
http://www.intel.com/design/network/new21/developers.htm

Drivers	Supports
NDIS2 Unified DC21x4 driver	NDIS2 MAC drivers for DOS, OS/2, Windows 3.1, Windows for Workgroups 3.11, and Windows 95
NDIS4 Unified DC21x4 driver	PC97 compliant and supports Windows NT 4.0, Windows 95, and Windows 98
NDIS5 Unified DC21x4 driver	PC97/PC98 compliant and supports ACPI/OnNow, Windows NT 5.0, and Windows 98
Novell Server Unified DC21x4 driver	32-bit ODI drivers for Versions 3.1x and 4.x Novell servers; Client32 drivers for DOS
Novell Client Unified DC21x4 driver	16-bit ODI drivers for DOS
SCO UNIX Unified DC21x4 driver	SCO UNIX LLI and MDI drivers
MOAB driver	Netware 5.0, and backward compatible with Netware 4.11
Support FIles	**Description**
SROM Specification for DC21x4 devices	EEPROM data and format requirements for interoperability with DC21x4 drivers
SROM programming toolkit	Serial ROM programming utilities
DVT Design Verification	Manufacturing test utility for verifying DC21x4 adapter functionality
PCITEST diagnostic	Utility to determine whether a PC is Revision 2.0 PCI compliant
EVBDebug diagnostic	Utility for low-level debug and analysis of Intel 21x4 evaluation boards (or similar)

Drivers	Supports
CardBus Enabler	Utility that maps CardBus slots into PCI configuration space for some CardBus laptops
BSDL	Boundary Scan Description Language files for Intel network chips
NDISDBG	Utility for low-level debug under Win 32 (Windows NT, Windows 95, and Windows 98) environment

5.0 Pinout Changes

The following sections detail pinout changes between the 21140-AF and the 21143-xD.

5.1 New Pinouts in the 21143-xD

The following table details pins that are new in the 21143-xD

Pin Name	Pin Description
aui_cd-	Attachment unit interface receive collision differential negative data.
aui_cd+	Attachment unit interface receive collision differential positive data.
aui_rd-	Attachment unit interface receive differential negative data.
aui_rd+	Attachment unit interface receive differential positive data.
aui_td-	Attachment unit interface transmit differential negative data.
aui_td+	Attachment unit interface transmit differential positive data.
cb_pads_l	This pin also determines the type of signals to use for the PCI/CardBus output pins, either PCI or CardBus. By default, this pin selects PCI signaling. To select CardBus signaling, this pin must be connected to a pull-down resistor.
clkrun_l	PCI/CardBus clock run indication. The host system asserts this signal to indicate normal operation of the clock. The host system deasserts clkrun_l when the clock is going to be stopped or slowed down to a non-operational frequency. If the clock is needed by the 21143, the 21143 asserts clkrun_l, requesting normal clock operation to be maintained or restored. Otherwise, the 21143 allows the system to stop the clock.
gep<0>/aui_bnc	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. This general-purpose pin can provide an interrupt when functioning as an input. • A control pin that provides an AUI (10BASE-5) or BNC (10BASE-2) select line. This control pin is mainly used to enable the external BNC transceiver in 10BASE-2 mode. When set, the 10BASE-5 mode is selected. When reset, the 10BASE-2 mode is selected.
gep<1>/activ	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. This general-purpose pin can • Provide an interrupt when functioning as an input. • A status pin that provides an LED that indicates either receive or transmit activity.

Pin Name	Pin Description
gep<2>/rcv_match/wake	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. • A status pin that provides an LED that indicates a receive packet has passed address recognition. This pin can also be controlled by PME_Enable bit (Func0_HwOptions<3>) in the serial ROM to be a wake-up event pin 1 that can be connected to pin pme# of the PCI connector or pin cstschg of the CardBus connector. When this pin is in a wake function, bit MiscHwOptions<1> in the serial ROM determines the polarity. The PME function takes precedence over the Magic Packet indication function. When the 21143 is in remote wake-up-LAN mode, this pin is used as an indicator that a Magic Packet has been successfully detected.
gep<3>/link	This pin can be configured by software to be: • A general-purpose pin that performs either input or output functions. • A status pin that provides an LED to indicate: — Network link integrity state for 10BASE-T or 100BASE-TX. — Both network activity and network link integrity state. For more information about LED indicators, refer to the 21143 Hardware Reference Manual.
iref	Current reference input for the analog phase-locked loop logic.
tp_rd–	Twisted-pair negative differential receive data from the twisted-pair lines.
tp_rd+	Twisted-pair positive differential receive data from the twisted-pair lines.
tp_td–	Twisted-pair negative differential transmit data from the twisted-pair lines.
tp_td– –	The positive and negative differential transmit data outputs are combined resistively outside the 21143 with equalization to compensate for intersymbol interference on the twisted-pair medium.
tp_td+	Twisted-pair positive differential transmit data from the twisted-pair lines.
tp_td+ +	The positive and negative differential transmit data outputs are combined resistively outside the 21143 with equalization to compensate for intersymbol interference on the twisted-pair medium.
vcap_h	Capacitor input for analog phase-locked loop logic.
vddac	Supplies +3.3-V input for analog phase-locked loop logic.
mii_rx_err/sel10_100	In MII PHY mode, this pin functions as receive error input. In SYM PHY mode, this pin functions as select 10/100 output. **Note:** This pin functions only as receive error input, mii_rx_err, in 21140.
mii_txen/sym_txd<4>	In MII PHY mode, this pin functions as transmit enable. In SYM PHY mod, this pin functions as transmit data. **Note:** This pin functions as transmit enable, mii_txen, in 21140.

5.2 Pinouts That Were in the 21140-AF But Are Not in the 21143-xD

The following table details the pinouts that were in the 21140-AF, but are not in the 21143-xD.

Pin Name	Pin Description
gep<7:0>	General-purpose pins can be used by software as either status pins or control pins. These pins can be configured by software to perform either input or output functions. **Note:** The 21143-xD uses only gep<3:0>. Refer to Section 5.1 for details.
nc	No connection.
srl_clsn	Collision detect signals a collision occurrence on the Ethernet cable to the 21140A. It may be asserted and deasserted asynchronously by the external ENDEC to the receive clock.
srl_rclk	Receive clock carries the recovered receive clock supplied by an external ENDEC. During idle periods, srl_rclk may be inactive.
srl_rxd	Receive data carries the input receive data from the external ENDEC. The incoming data should be synchronous with the srl_rclk signal.
srl_rxen	Receive enable signals activity on the Ethernet cable to the 21140A. It is asserted when receive data is present on the Ethernet cable and deasserted at the end of a frame. It may be asserted and deasserted asynchronously to the receive clock (srl_rclk) by the external ENDEC.
srl_tclk	Transmit clock carries the transmit clock supplied by an external ENDEC. This clock must always be active (even during reset).
srl_txd	Transmit data carries the serial output data from the 21140A. This data is synchronized to the srl_tclk signal.
srl_txen	Transmit enable signals an external ENDEC that the 21140A transmit is in progress.

5.3 Pins That Exist in Both the 21140-AF and 21143-xD

Even though the pin names below are implemented in both the 21140-AF and 21143-xD, most of the pinouts, corresponding to the pin names, are located differently in each device. Please, refer to the hardware reference manual or data sheet for details.

Pin Name	Pin Description
ad<31:0>	32-bit PCI address and data lines.
br_a<0>	Boot ROM address line bit 0. In a 256KB configuration, this pin also carries in two consecutive address cycles, boot ROM address bits 16 and 17.
br_a<1>	Boot ROM address line bit 1.This pin also latches the boot ROM address and control lines by the two external latches.
br_ad<7:0>	Boot ROM address and data multiplexed lines bits 7 through 0. In two consecutive address cycles, these lines contain the boot ROM address pins 7 through 2, oe_l and we_l in the first cycle; and these lines contain boot ROM address pins 15 through 8 in the second cycle. During the data cycle, bits 7 through 0 contain data.
br_ce_l	Boot ROM or external register chip enable.

Pin Name	Pin Description
c_be_l<3:0>	Bits 0 through 3 of the bus command and byte enable lines. Bus command and byte enable are multiplexed on the same PCI pins. During the address phase of the transaction, these 4 bits provide the bus command. During the data phase, these 4 bits provide the byte enable. The byte enable determines which byte lines carry valid data. For example, bit 0 applies to byte 0, and bit 3 applies to byte 3.
devsel_l	Device select is asserted by the target of the current bus access. When the 2114x is the initiator of the current bus access, it expects the target to assert devsel_l within 5 bus cycles, confirming the access. If the target does not assert devsel_l within the required bus cycles, the 2114x aborts the cycle. To meet the timing requirements, the 2114x asserts this signal in a medium speed (within 2 bus cycles).
frame_l	The frame_l signal is driven by the bus master to indicate the beginning and duration of an access. The frame_l signal asserts to indicate the beginning of a bus transaction. While frame_l is asserted, data transfers continue. The frame_l signal deasserts to indicate that the next data phase is the final data phase transaction.
gnt_l	Bus grant asserts to indicate to the 2114x that access to the bus is granted.
idsel	Initialization device select asserts to indicate that the host is issuing a configuration cycle to the 2114x.
int_l	Interrupt request asserts when one of the appropriate bits of CSR5 sets and causes an interrupt, provided that the corresponding mask bit in CSR7 is not asserted. Interrupt request deasserts by writing a 1 into the appropriate CSR5 bit. If more than one interrupt bit is asserted in CSR5 and the host does not clear all input bits, the 2114x deasserts int_l for one cycle to support edge-triggered systems.
irdy_l	Initiator ready indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of the clock when both irdy_l and target ready trdy_l are asserted. Wait cycles are inserted until both irdy_l and trdy_l are asserted together. When the 2114x is the bus master, it asserts irdy_l during write operations to indicate that valid data is present on the 32-bit ad lines. During read operations, the 2114x asserts irdy_l to indicate that it is ready to accept data.
par	Parity is calculated by the 2114x as an even parity bit for the 32-bit ad and 4-bit c_be_l lines. During address and data phases, parity is calculated on all the ad and c_be_l lines whether or not any of these lines carry meaningful information.
pci_clk	The clock provides the timing for the 2114x related PCI bus transactions. All the bus signals are sampled on the rising edge of pci_clk. The clock frequency range is between 20 MHz and 33 MHz.
perr_l	Parity error asserts when a data parity error is detected. When the 2114x is the bus master and a parity error is detected, the 2114x asserts both CSR5 bit 13 (fatal bus error) and CFCS bit 24 (data parity report). Next, it completes the current data burst transaction, then stops operation. After the host clears the system error, the 2114x continues its operation. The 2114x asserts perr_l when a data parity error is detected in either a master-read or a slave-write operation.
req_l	Bus request is asserted by the 2114x to indicate to the bus arbiter that it wants to use the bus.
rst_l	Resets the 2114x to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When in the reset state, all PCI output pins are put into tristate and all PCI O/D signals are floated.
serr_l	If an address parity error is detected and CFCS bit 8 (serr_l enable) is enabled, 2114x asserts both serr_l (system error) and CFCS bit 30 (signal system error). When an address parity error is detected, system error asserts two clocks after the failing address.

Pin Name	Pin Description
sr_ck	Serial ROM clock signal. This pin provides a serial clock output for the serial ROM.
sr_cs	Serial ROM chip-select signal. This pin provides a chip select for the serial ROM.
sr_di	Serial ROM data-in signal. This pin serially shifts the write data from the 21143 to the serial ROM device.
sr_do	Serial ROM data-out signal. This pin serially shifts the read data from the serial ROM device to the 2114x.
stop_l	Stop indicator indicates that the current target is requesting the bus master to stop the current transaction. The 2114x responds to the assertion of stop_l when it is the bus master, either to disconnect, retry, or abort.
tck	JTAG clock shifts state information and test data into and out of the 2114x during JTAG test operations. If the JTAG port is unused, this pin should be connected to vss.
tdi	JTAG data in is used to serially shift test data and instructions into the 2114x during JTAG test operations.
tdo	JTAG data out is used to serially shift test data and instructions out of the 21143 during JTAG test operations.
tms	JTAG test mode select controls the state operation of JTAG testing in the 2114x.
trdy_l	Target ready indicates the target agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both trdy_l and irdy_l are asserted. Wait cycles are inserted until both irdy_l and trdy_l are asserted together. When the 2114x is the bus master, target ready is asserted by the bus slave on the read operation, which indicates that valid data is present on the ad lines. During a write cycle, it indicates that the target is prepared to accept data.
vdd	3.3-V voltage supply input. These pins should be connected to the auxiliary power, if such power exists. Otherwise, these pins should be connected to the main power.
vdd_clamp	Supplies +5-V or +3.3-V reference for clamp logic.In the 21143-xD, This pin is also used to identify the lack of main power when the auxiliary power is on. This pin should be connected to the main power.In the 21140-AF, this pin is only for either +5V or +3.3V voltage reference.
vss	Ground pins.

5.4 MII/SYM Signal Pinout Implementation Differences

The MII/SYM signal pinouts are implemented differently in the 21140-AF and 21143-xD (pin number and function). Refer to the 21140A and 21143 Hardware Reference Manuals for comparison of these signal pinouts before attempting the PHY interconnection design.

6.0 Register Changes and Additions

The following sections detail the changes to registers that were present in the 21140-AF and list and describe the registers that have been added to the 21143-xD.

6.1 PCI Configuration Registers Changes

The following table lists the PCI Configuration Register changes between the 21140-AF and the 21143-xD.

New or Changed	Description	21140-AF	21143-xD
CFID<31:16>	Device ID.	Device ID, 0009H	Device ID, 0019H
CFRV<3:0>	Indicates the step number within the current revision.	The value of this field is set to 2.	The value of this field is set to 1.
CFRV<7:4>	Indicates the revision number.	The value of this field is set to 2.	The value of this field is set to 4.

6.2 PCI Configuration Registers Added to the 21143-xD

The following are the new registers and register bits available with the 21143-xD.

Configuration Register	Identifier	I/O Address Offset
Command and Status	CFCS<20>	04H
Card Information Structure	CCIS	28H
Capabilities Pointer	CCAP	34H
Configuration Wake-Up-LAN address 0 (D,C,B,A)	CWUA0	44H
Configuration Wake-Up-LAN address 0 (F, E)	CWUA1	48H
SecureON* Password (D,C,B,A)	SOP0	4CH
SecureON Password (F, E)	SOP1	50H
Configuration Wake-Up Command	CWUC	54H
Reserved	—	58H – D8H
Capabilities ID	CCID	DCH
Power Management Control Status	CMPC	E0H

6.3 Command and Status Configuration Register (CFCS - Offset 04H)

Previously reserved bit <20> is now defined to indicate whether the 21143-xD implements a list of new capabilities. The value of this bit is loaded from the Func0_HwOptions<3> bit (PME_Enable) in the serial ROM.

- When set, this bit indicates the presence of New Capabilities.
- When cleared, New Capabilities are not presented.

6.4 Configuration Card Information Structure Register (CCIS - Offset 28H)

This register points to one of the possible address spaces were the card information structure (CIS) begins. The pointer is used in a CardBus PC environment. The following table lists the fields.

Field	Description
CCIS<2:0>	Address Space Indicator. This field indicates the location of the CIS base address. • A value of 2, indicates that the CIS is stored in the serial ROM. • A value of 7, indicates that the CIS is stored in the expansion ROM or Boot ROM.
CCIS<27:3>	Address Space Offset. This field contains the address offset within the address space indicated by the address space indicator field, CCIS<2:0>.
CCIS<31:28>	ROM Image. The 4-bit ROM image field value when the CIS resides in an expansion ROM.

6.5 Capabilities Pointer (CCAP - Offset 34H)

This pointer has a pointer to the power-management register block in the PCI configuration space. It is valid only if the New Capabilities bit in CFCS is set. The following table lists the Capabilities Pointer register fields.

Field	Description
CCAP<7:0>	Points to the location of the power management register block in the PCI configuration space. The value of this field is determined by Func0_HwOptions<3> (PME_Enable) bit in the serial ROM. If this bit is set, the value of this field is DCH; otherwise, the value of this field is 00H.

6.6 Capability ID Register (CCID - Offset DCH)

This register provides information on the 21143-xD power-management capabilities. The following table lists the Capability ID register fields.

Field	Description
CCID<7:0>	PCI Power Management Register ID. The value of this field is 01H, indicating that this is the power management register block.
CCID<15:8>	Next Item Pointer. Points to the location of the next block of the capability list in the PCI Configuration Space. The value of this field is 00H, indicating that this is the last item of the Capability linked list.
CCID<18:16>	Power Management PCI Version. The value of this field is 001 binary, indicating that the 21143-xD complies with revision 1.0 of the *PCI Power Management specification*.
CCID<19>	Power Management Event Clock. The value of this field is 0, indicating that the 21143-xD does not rely on the presence of the CardBus clock in order to generate a PME.
CCID<21>	Device Specific Initialization. The value of this field is 0, indicating that the 21143-xD does not require a special initialization code sequence in order to be configured correctly.

Field	Description
CCID<25>	D1 Support. The value of this field is 1, indicating that the 21143-xD supports the D1 power state.
CCID<26>	D2 Support. The value of this field is 1, indicating that the 21143-xD supports the D2 power state.
CCID<27>	PME Support D0. The value of this field is 0, indicating that the 21143-xD does not assert PME# in D0 power state
CCID<28>	PME Support D1. The value is 1, meaning that the 21143-xD may assert PME# in D1 power state.
CCID<29>	PME Support D2. The value is 1, meaning that the 21143-xD may assert PME# in D2 power state.
CCID<30>	PME Support $D3_{hot}$. The value is 1, meaning that the 21143-xD may assert PME# in $D3_{hot}$.
CCID<31>	PME Support $D3_{cold}$. The value is 1, meaning that the 21143-xD may assert PME# in $D3_{cold}$.

6.7 Power-Management Control and Status Register (CMPC - Offset E0H)

This register is used to manage the 21143-xD device power state, and to enable and monitor the 21143-xD power-management events. The following table lists the Power-Management and Control Status register fields.

Field	Description
CPMC<1:0>	Power State. This field id used to set the current power state of the 21143-xD and to determine its power state. • 00 binary – D0 • 01 binary – D1 • 10 binary – D2 • 11 binary – D3(hot) This field gets a value of 00 binary after power up.
CPMC<8>	PME_Enable. If this bit is set, the 21143-xD assert the gep<2>/rcv_match/ wake pin upon a detection of the wake-up event. Otherwise, assertion of the gep<2>/rcv_match/wake pin by the 21143-xD is disabled.
CPMC<15>	PME_Status. This bit is set when the 21143-xD detects a wake-up event. If bit PME_Enable is set, the 21143-xD asserts the gep<2>/rcv_match/wake pin. This bit is cleared on power up reset or by write 1, and the 21143-xD deasserts the gep<2>/rcv_match/wake pin. It is not modified by either hardware or software reset. **Note:** This bit is also cleared if the General Enable bit of the (Function Event Register<4>) is cleared.

6.8 Remote Wake-Up-LAN Engineering Test Mode Registers

The following table lists the Remote Wake-Up-LAN Engineering Test Mode registers. Please refer to the 21143 Hardware Reference Manual for more detail.

Configuration Register	Identifier	I/O Address Offset
Configuration Wake-Up-LAN address 0 (D,C,B,A)	CWUA0	44H
Configuration Wake-Up-LAN address 0 (F, E)	CWUA1	48H
SecureON Password (D,C,B,A)	SOP0	4CH
SecureON Password (F, E)	SOP1	50H
Configuration Wake-Up Command	CWUC	54H

6.9 Command and Status Register Differences Between the 21140-AF and 21143-xD

The following table lists the Command and Status Register differences between the 21140-AF and the 21143-xD.

Change	21140-AF Registers	21143-xD Registers
CSR0<19:17> TAP - Transmit polling register	The polling values (in binary) ranges for: • SRL from 200 µs to 102.4 µs • 10 Mb/s MII from 800 µs to 409 µs • 100 Mb/s MII modes from 8 µs to 40.96 µs	The polling values (in binary) ranges for: • 10BASE-T/AUI from 200 µs to 89.6 µs • 10 Mb/s MII from 800 µs to 358.4 µs • 100 Mb/s MII/SYM from 80 µs to 35.84 µs
CSR5<15>	AIS–Abnormal Interrupt Summary. • CSR5<1>-Transmit Process stopped • CSR5<3>-Transmit jabber timeout • CSR5<5>-Transmit underflow • CSR5<7>-Receive buffer unavailable • CSR5<8>-Receive process stopped • CSR5<9>-Receive watchdog timeout • CSR5<10>-Early transmit interrupt • CSR5<13>-Fatal bus error interrupt	AIS–Abnormal Interrupt Summary. • CSR5<1>-Transmit Process stopped • CSR5<3>-Transmit jabber timeout • CSR5<4>-Link Pass or autonegotiation completed • CSR5<5>-Transmit underflow • CSR5<7>-Receive buffer unavailable • CSR5<8>-Receive process stopped • CSR5<9>-Receive watchdog timeout • CSR5<10>-Early transmit interrupt • CSR5<12>-Link Fail • CSR5<13>-Fatal bus error • CSR5<26>-General purpose interrupt • CSR5<27>-Link Changed

Change	21140-AF Registers	21143-xD Registers
CSR6<18>	PS–Port Select. When this bit is reset, the SRL port is selected. When it is set, the MII/SYM port is selected. Please refer to the 21140A Hardware Reference Manual for more details.	PS–Port Select. When this bit is reset, the 10BASE-T or AUI port is selected according to the CSR13<3> value. When it is set, the MII/SYM port is selected. Please refer to the 21140A Hardware Reference Manual for more details.
CSR6<9>	FD–Full Duplex Mode. When set the device operates in FD mode. Setting the 21140A to operate in full-duplex mode is allowed only if the transmit and receive processes are in the stopped state, and start/stop receive (CSR6<1>) and start/stop transmission commands (CSR6<13>) are both set to 0.	FD–Full Duplex Mode. When autonegotiation is disabled (CSR14<7>=0), this bit selects the 21143 half-duplex or full-duplex operation mode. A 0 selects HD operation while a 1 selects FD operation. When autonegotiation is enabled (CSR14<7>=1) and the 21143 is operating in 10BASE-T mode (CSR6<18>=0 and CSR13<3>=0), this bit controls the advertisement of the 10BASE-T FD capability (bit 6) in the transmitted code word. The 21143 will operate in 10BASE-T full-duplex capability mode only if both the link partners are advertising this bit set.
CSR7<15>	AIS–Abnormal Interrupt Summary Enable. • CSR5<1>-Transmit Process stopped • CSR5<3>-Transmit jabber timeout • CSR5<5>-Transmit underflow • CSR5<7>-Receive buffer unavailable • CSR5<8>-Receive process stopped • CSR5<9>-Receive watchdog timeout • CSR5<10>-Early transmit interrupt	AIS–Abnormal Interrupt Summary Enable. • CSR5<1>-Transmit Process stopped • CSR5<3>-Transmit jabber timeout • CSR5<4>-Link Pass or autonegotiation completed • CSR5<5>-Transmit underflow • CSR5<7>-Receive buffer unavailable • CSR5<8>-Receive process stopped • CSR5<9>-Receive watchdog timeout • CSR5<10>-Early transmit interrupt • CSR5<12>-Link Fail • CSR5<13>-Fatal bus error • SR5<26>-General purpose interrupt • CSR5<27>-Link Changed
CSR12	General Purpose Port Register	SIA Status Register. This register is completely redefined and is detailed in Section 6.18.

6.10 New Command and Status Registers Added to 21143-xD

The following is a list of new command and status registers and register bits added.

Register	Name	Offset from CSR Base Address (CBIO and CMBA)
CSR0<26>	Enable OnNow Registers	00H
CSR1-PM	Wake-Up frame filter control	08H
CSR2-PM	Wake-Up events control and status	10H
CRS5<4>	Link Pass or Autonegotiation Completed	28H
CSR5<12>	Link Fail	28H
CSR5<26>	General-Purpose Port Interrupt	28H
CSR5<27>	Link Changed	28H
CSR6<26>	Ignore Destination Address MSB	30H
CSR7<4>	LPE/ANE–Link Pass Enable or Autonegotiation completed	38H
CSR7<12>	LFE–Link Fail Enable	38H
CSR7<26>	GPE–General-Purpose Port Enable	38H
CSR7<27>	LCE–Link Changed Enabled	38H
CSR11<19:17>	Number of Receive Packets	58H
CSR11<23:20>	Receive Timer	58H
CSR11<26:24>	Number of Transmit Packets	58H
CSR11<30:27>	Transmit Timer	58H
CSR11<31>	Cycle Size	58H
CSR12	SIA Status Register	60H
CSR13	SIA Connectivity Register	68H
CSR14	SIA Transmit and Receive Register	70H
CSR15<30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19:16, 15, 14, 11, 3>	SIA and General-Purpose Port Register These register bits are added in CSR15 of the 21143-xD.	78H

6.11 Bus Mode Register (CSR0 - Offset 00H)

The following table lists the Bus Mode register fields.

Field	Description
26	Enable OnNow Register. When set, CSR1-PM and CSR2-PM are accessible. When this bit is cleared, writing to these registers is interpreted as writing to CSR1 and CSR2 (receive/transmit poll demand). This bit is cleared upon hardware and software register.

6.12 Wake-Up Frame Filter Register (CSR1-PM - Offset 08H)

This register is used for loading the wake-up frame filter register. In order to load the wake-up frame filter register, CSR0<26> must be set and CSR1-PM should be written eight times. The first value written to this register, after CSR1-PM<31:0> is set, is loaded by the 21143-xD to the first longword in the wake-up frame filter register, (filter_0_byte_mask). The second value written to this register is loaded to the second longword in the wake-up frame filter register and so on.

Filter 0 Byte Mask							
Filter 1 Byte Mask							
Filter 2 Byte Mask							
Filter 3 Byte Mask							
Reserved	Filter 3 Command	Reserved	Filter 2 Command	Reserved	Filter 1 Command	Reserved	Filter 0 Command
Filter 3 Offset		Filter 2 Offset		Filter 1 Offset		Filter 0 Offset	
Filter 1CRC-16				Filter 0 CRC-16			
Filter 3 CRC-16				Filter 2 CRC-16			

Filter i Byte Mask Bits Fields

This register defines which byte of the incoming frames are examined by the filter i in order to determine whether or not this is a wake-up frame.

Field	Description
30:0	Byte Mask. If bit number j of the byte mask is set, byte number pattern-offset + j of the incoming frame is processed by the CRC machine. Otherwise, byte pattern-offset + j is ignored. This field is not affected by either power-up, hardware, or software reset.
31	MBZ. This bit must be zero.

Filter i Command

This register controls the filter i operation.

Field	Description
3	Address Type. Defines the destination address type of the pattern. • If set, the pattern applies only to multicast frames. • If cleared, the pattern applies only to unicast frames.
2	Add Previous. When set, the 21143-xD perform a logical AND between the current filter matching signal and the matching signal of the previous filter. For the first filter, the 21143-xD chains the filter's matching signal with the result of the global unicast filter (CSR2-PM<9>).
1	Inverse Mode. When bit is set, the 21143-xD uses its match signal as rejection signal. A frame that does not match this filter causes the 21143-xD to generate a power-management event.
0	Enable Filter. When this bit is set, filter i is enabled, otherwise, filter is disabled.

Filter i Offset

This register defines the offset in the frame's destination address field from which the frames are examined by filter i.

Field	Description
7:0	Pattern Offset. The offset of the first byte in the frame that is examined by the 21143-xD in order to check if an incoming frames is a wake-up frame. Offset 0 is the first byte of the incoming frame's destination address. The minimum value allowed for this field is 12.

Filter i CRC-16

This register contains the CRC-16 result of a frame that should pass filter i.

Field	Description
15:0	Pattern CRC-16. This field contains the 16-bit CRC value calculated from the pattern and the byte mask programmed to the wake-up filter register block. The 21143-xD compares the result of its CRC machine to this value in order to determine whether the frame is a wake-up frame.

6.13 Wake-Up Event Control and Status Register (CSR2-PM - Offset 10H)

This register is used for programming the requested wake-up events and the VLAN parameters, and monitoring the wake-up events. In order to program the requested wake-up events and the VLAN parameters, CSR0<26> must be set. The following table lists the Wake-Up Event Control and Status register fields.

Field	Description
0	Link Change Enable. If set, enables generation of a power-management event due to link change.
1	Magic Packet Enable. If set, enables generation of a power-management event due to Magic-packet reception
2	Wake-Up Frame Enable. If set, enable generation of a power-management event due to reception of wake-up frame.
4	Link Change Detected. If set, indicates that a power-management event was generated due to link change. This bit is cleared by write 1, or upon power-up reset. It is unaffected by either hardware or software reset.
5	Magic Packet Received. If set, indicates that a power-management event was generated due to reception of a Magic Packet. This bit is cleared by write 1, or upon power-up reset. It is unaffected by either hardware or software reset.
6	Wake-up frame Received. If set, indicates that a power-management event was generated due to reception of a wake-up frame. This bit is cleared by write 1, or upon power-up reset. It is unaffected by either hardware or software reset.
8	MBZ. This bit must be zero.
9	Global Unicast. When set, enable any unicast packet filter by the 21143-xD address recognition to be a wake-up frame.

Field	Description
11	VLAN Enable. When set, enables the 21143-xD's VLAN support as described in the 21143 Hardware Reference Manual.
31:16	VLAN Type. If VLAN type Enable bit is set (CSR2-PM<11>), this field should be written with the VLAN type defined by the IEEE 802.1 standard.

6.14 Status Register (CSR5 - Offset 28H)

The status register (CSR5) contains all the status bits that the 21143 reports to the host. CSR5 bits are not cleared when read. Writing 1 to them clears them. The following table lists the Status register fields.

Field	Description
4	LNP/ANC–Link pass or Autonegotiation Completed. When autonegotiation is not enabled (CSR14<7> = 0), this bit indicates that the 10BASE-T Link Integrity Test has completed successfully, after the link was down. This bit is also set as a result of writing 0 to CSR14<12>, Link Test Enable. When autonegotiation is enable (CSR14<7> = 1), this bit indicates that the autonegotiation has completed (CSR12<14:12> = 5H). CSR12 should then be read for a link status report. This bit is valid only when port select (CSR6<18>) is reset, and receive squelch enable (CSR14<8>) is set. Link fail interrupt (CSR5<12>) automatically clears this bit.
12	LNF–Link Fail Indicates a transition to the link fail state is the twisted-pair port. See link fail status CSR12<2>. This bit is valid only when CSR6<18>, Port Select, is reset; CSR14<8>, Receive Squelch Enable, is set; and CSR13<3>, 10BaseT or AUI, is 0 (10BASE-T mode). Link pass CSR5<4> automatically clears this bit.
26	GPI–General Purpose Port Interrupt Indicates an interrupt from the general-purpose port. The value of this bit is the logical OR of: • CSR15<30>-Receive Match Interrupt • CSR15<29>-General-Purpose port interrupt 1 • CSR15<28>-General-Purpose port interrupt 0 Only unmasked bits affect the value of the general-purpose port CSR5<26> bit.
27	LC–Link Changed Indicates that the 10BASE-T link status has changes from the link pass to link fail or from link fail to link pass. The new status can be read from CSR12<1>, 100BASE-T link status.

6.15 Operating Mode Register (CSR6 - Offset 30H)

The Operating Mode register establishes the receive and transmit operating modes and commands. This should be the last CSR to be written as part of initialization. The following table lists the Operating Mode register fields.

Field	Description
26	Ignore Destination Address MSB. When set bit 47 of the destination address is ignored in the MAC's address filtering. This bit is meaningful only if the 21143 is programmed to do prefect address filtering. It is cleared upon hardware and software reset.

6.16 Interrupt Enable Register (CSR7 - Offset 38H)

This register enables the interrupts reported by CSR5. Setting a bit to 1 enables a corresponding interrupt. After hardware or software reset, all interrupts are disabled. The following table lists the Interrupt Enable register fields.

Field	Description
4	LPE/ANE–Link Pass Enable/Autonegotiation Completed Enable. When this bit and AIE (CSR7<15>) are set, the LPE/ANE completed interrupt (CSR5<4>) is enabled.
12	LFE–Link Fail Enable. When this bit and the abnormal interrupt summary enable bit (CSR7<15>) are set, the link fail interrupt (CSR5<12>) is enabled. When this bit is reset, the link fail interrupt (CSR5<12>) is disabled.
26	GPE–General Purpose Port Enable. When this bit and AIE (CSR7<15>) are set, the general-purpose port interrupt (CSR5<27>) is enabled.
27	LCE–Link Change Enable. When this bit and AIE (CSR7<15>) are set, the link changed interrupt (CSR5<27>) is enabled. When this bit is reset, the link changed interrupt (CSR5<27>) is disabled.

6.17 General-Purpose Timer and Interrupt Mitigation Control Register (CSR11 - Offset 58H)

The 21143 now supports interrupt mitigation. This mechanism allows the driver to reduce the number of receive and transmit interrupts, which reduces the CPU utilization for servicing a large number of interrupts. The following table lists the General-Purpose Timer and Interrupt Mitigation Control register fields.

Field	Description
19:17	Number of Receive Packets. Indicates the number of receive packets before issuing a receive interrupt.
23:20	Receive Timer. Indicates the time in units of “Cycles Size” before issuing a receive interrupt after packet reception.
26:24	Number of Transmit Packets. Indicates the number of transmit packets before issuing a transmit interrupt.
30:27	Transmit Timer. Indicates the time in units of “16 * Cycles Size” before issuing a transmit interrupt after packet transmission.
31	Cycle Size. This field controls the units for the transmit and receive timers. When set, the cycle size is: • 10BASE-T/AUI mode – 12.8 µs • MII/SYM 100 Mb/s mode – 5.12 µs • MII 10 Mb/s mode – 51.2 µs When cleared, the cycle size is • 10BASE-T/AUI mode – 204.8 µs • MII/SYM 100 Mb/s mode – 81.92 µs • MII 10 Mb/s mode – 819.2 µs

6.18 SIA Status Register (CSR12 - Offset 60H)

The SIA Status Register is a completely redefined register. The following table lists the SIA Status Register fields.

Field	Description
0	MRA–MII Receive Port Activity. This bit is set, when there is receive activity on the MII port and the MII port is selected. This bit is cleared by write 1.
1	LS100–100 Mb/s Link Status. This bit continuously reflects the 100BASE-TX link status. When set, the 100BASE-TX link test is in fail state. When reset, the 100BASE-TX link test is in pass state. This status is derived from the sd pin and is effective only when CSR6<23> (PCS function) is set. It is effective regardless of the status of CSR16<18> (Port Select) and CSR14<7> (Autonegotiation Enable). When CSR14<7> (Autonegotiation Enable) is set, the LS100 bit is effective only if autonegotiation arbitration state (CSR12<14:12>) is 101.
2	LS10–10 Mb/s Link Status. This bit continuously reflects the 10BASE-T link test status. When set, the 10BASE-T link test is in fail state. When reset, the 10BASE-T link test is in pass state. It is effective only in 10BASE-T mode and only when CSR14<8> is set. During link fail state the 21143 does not transmit any packet to the media and does not receive any packet from the media. When autonegotiation (CSR14<7>) is set, the LS10 bit is effective only if autonegotiation arbitration state (CSR12<14:12>) is 101.
3	APS–Autopolarity State. When set, the 10BASE-T polarity is positive. When reset, the 10BASE-T polarity is negative. The receiver inverts the received bit stream.
8	ARA–AUI Receive Port Activity. Sets when there is receive activity on the AUI port. This bit is valid only if port select CSR6<18> is reset. Writing 1 clears this bit.
9	TRA–10BASE-T Receive Port Activity. Sets when there is receive activity on the 10BASE-T port. This bit is valid only if port select CSR6<18> is reset. Writing 1 clears this bit.
10	NSN–Non-Stable NLP's Detected. When set, indicates that the 10BASE-T normal link pulse (NLP) is not stable. The Link Integrity Test passed for a while, but failed later during negotiation. This means that NLPs were recognized on the line, but were not stable enough to cause autonegotiation completion. This bit is cleared by read transaction. Effective only when CSR14<7> is set.
11	TRF–Transmit Remote Fault. When set, the 21143 sets bit 13 (remote fault bit) in the transmitted code words. This can be used to inform the link partner that some fault has occurred.

Field	Description
14:12	ANS–Autonegotiation Arbitration State. The CSR12<14:12> bits reflect the current autonegotiation arbitration state as follows: • 000 - Autonegotiation disable • 001 -Transition disable • 010 - Ability detect • 011 - Acknowledge detect • 100 - Complete acknowledge • 101 - FLP link good; autonegotiation complete • 110 - Link check When autonegotiation is completed, an ANC interrupt (CSR5<4>) is generated. These bits can also be used to restart the autonegotiation sequence. This is done by writing a pattern of 001 into this field, provided that autonegotiation enable (CSR14<7>) is set. Otherwise, these bits should be written as 0.
15	LP–Link Partner Negotiable. This bit is set when the link partner is recognized to be a device that implements the autonegotiation algorithm. Effective only when CSR14<7> is set.
31:16	LPC–Link Partner's Link Code Word. These bits contain the link partner's link code word, where bit 16 is S0 (selector field bit 0) and bit 3 is NP (Next page).

6.19 SIA Connectivity Register (CSR12 - Offset 68H)

This register contains the SIA connectivity bits that permit the interconnection of different sections within the SIA. The following table lists the SIA Connectivity register fields.

Field	Description
0	RST–SIA Reset. When reset, resets all the SIA functions and machines.
3	AUI–10BASE-T, or AUI. • When reset, forces the 21143 to select the 10BASE-T interface. • When set, forces the 21143 to select the AUI interface. The selection of AUI and 10BASE-2 (BNC) is done by CSR15<3>.

6.20 SIA Transmit and Receive Register (CSR14 - Offset 70H)

This register configures the SIA transmitter and receive operating modes. The following table lists The SIA Transmit and Receive register fields.

Field	Description
0	ECEN–Encode Enable. • When set the tranmsit data encode is enabled. • When reset thre transmit encoder is disabled.
1	LBK–Loopback Enable. Enabled loopback operation in the SIA. In AUI mode, this bit should be reset.
2	DREN–Driver Enable. • When set, the transmit SIA driver is enabled for AUI or 10BASE-T operation. • When reset, the transmit driver is disabled.

Field	Description
3	LSE–Link Pulse Send Enable. This bit is for 10BASE-T mode only. When set, the link pulse generator is enabled.
<5:4>	CPEN–Compensation Enable. These bits are valid only in 10BASE-T mode. See the 21143 Hardware Reference Manual for further details. • 00, 01 - Compensation disable mode • 10 - High power mode • 11 - Normal compensation mode
6	TH–10BASE-T Half Duplex Enable. This bit controls the value of bit 5 in the transmitted link code word. • When set, the ability to work with 10BASE-T Half-Duplex is advertised. • When clear, the ability to work with 10BASE-T Half-Duplex is not advertised. 10BASE-T full-duplex ability is advertisement (bit 6 in the transmitted link code word) is controlled by CSR6<9> Full Duplex Mode. This bit meaningful only if CSR14<7> is set.
7	ANE–Autonegotiation Enable. • When set, 21143 performs an autonegotiation with the link partner to determine the operation mode. It can be performed only when in 10BASE-T mode. • When reset, autonegotiation is disabled.
8	RSQ–Receive Squelch Enable. When set the AUI or 10BASE-T receivers are active in accordance with the selected mode. When the port autonegotiation is enabled, the AUI and 10BASE-T receivers are enabled simultaneously.
9	CSQ–Collision Squelch Enable. When set, AUI collision receivers are active.
10	CLD–Collision Detect Enable. When set, the collision detect logic is enabled.
11	SQE–Signal Quality (Heartbeat) Generate Enable. Controls the signal quality (SQE) generator ability to imitate external medium attachment unit (MAU) behavior. When set, a short heartbeat signal is generated after the conclusion of a transmitted packet. In 10BASE-T mode, SQE (CSR14<11>) should be set; otherwise, a heartbeat fail (TDES0<7>) is set. In AUI mode, SQE (CSR14<11>) should be reset.
12	LTE–Link Test Enable. This bit is meaningful only for 10BASE-T port. When set, the link test function logic is enabled. Resetting this bit forces the link test function to link pass rate.
13	APE–Autopolarity Enable. When set and link test enable (CSR14<12>) is also set, the autopolarity function logic is enabled. When reset, the polarity is determined by set polarity plus (CSR14<14>). When link test enable (CSR14<12>) is reset, this bit should be also reset. This bit is valid only in 10BASE-T mode.
14	SPP–Set Polarity Plus. When reset and autopolarity enable (CSR14<13> is reset, the polarity on the incoming data is switched. This feature can be used by driver to reverse polarity on the incoming packets; otherwise this bit should be set. It is valid only in 10BASE-T mode.
15	TAS–10BASE-T/AUI Autosensing Enable • When set, the 10BASE-T and AUI ports are monitored. The selected port operation is not affected. • When cleared, only the port that is selected for operation, AUI or 10BASE-T is monitored as per CSR13<3>.

Field	Description
16	TXH–100BASE-TX Half-Duplex. This bit controls the value of bit 7 in the transmitted link code word. • When set, the ability to work with 100BASE-TX Half-Duplex is advertised. • When clear, the ability to work with 100BASE-TX Half-Duplex is not advertised. This bit meaningful only if CSR14<7> is set.
17	TXF–100BASE-TX Full-Duplex. This bit controls the value of bit 8 in the transmitted link code word. • When set, the ability to work with 100BASE-TX Full-Duplex is advertised. • When clear, the ability to work with 100BASE-TX Full-Duplex is not advertised. This bit meaningful only if CSR14<7> is set.
18	T4–100BASE-T4. This bit controls the value of bit 9 in the transmitted link code work. • When set, the ability to work with 100BASE-T4 is advertised. • When clear, the ability to work with 100BASE-T4 is not advertised. This bit is meaningful only if CSR14<7> is set.

6.21 SIA and General Purpose Port Register (CSR15 - Offset 78H)

This register is divided in to two section: the SIA register (CSR15<15:0>) and the General Purpose Port register (CSR15<31:16>). The following table lists the SIA and General Purpose Port register fields.

Field	Description
3	ABM–AUI/BNC Mode. This bit is used by the driver to select either AUI or BNC mode. • When set, AUI (10Base5) is selected. • When clear BNC is selected.
11	LEE–Link Extend Enable. • When set, the 21143 reports link detection on this 100BASE-TX symbol port only if its sd pin is asserted for at least 1.2 ms. • When cleared the 21143 reports link detection on this 100BASE-TX symbol port only if its sd pin is asserted for at least 330 µs.
14	RMP–Received Magic Packet. When set, indicates that a Magic Packet has been received. Writing a 1 to this bit will clear it. It is unaffected by reset.
15	HCKR–Hacker. When set, indicates that 16 packets have been received with a matching remote wake-up-LAN format, including a good CRC but with a non-matching password.

Field	Description
19:16	MD–General-Purpose Mode and Data. When CSR15<27> is set, the value that is written by the host to CSR15<19:16> directs pins gep<3:0> to act as input or output pins (CSR15<19> controls pin gep<3> and so on). A 1 directs the pin to be an output pin and vise versa. The value that is driven by a gep pin that was directed to be an output is cleared when CSR15<27> is set. When set CSR15<27> is reset, the values written to CSR15<19:16> are the values that will be driven on pin gep<3:0>, respectively. This is only true for the pins that are configured as output pins. After reset, all gep pins become input pins.If gep<1:0> pin are selected as input pins, an interrupt occurs when either of these bits change state (provided that CSR15<25:24> is enabled).
20	LGS0–LED/GEP 0 Select. This bit selects either aui_bnc or gep<0> function for 21143 pin 100. • When set the aui_bnc function is selected, which provides a control line to select either 10Base5 (AUI) or 10Base2 (BNC) as programmed by CSR15<3>. • When reset the gep<0> function is selected. The gep<0> is a general-purpose port. After a hardware or software rest, the gep<0> function is selected.
21	LGS1–LED/GEP 1 Select. This bit selects either activ or gep<1> function for 21143 pin 101. • When set the activ function is selected, which provides a LED indicating receive or transmit activity on the selected port. • When reset the gep<1> function is selected. The gep<1> is a general-purpose port. After a hardware or software rest, the gep<1> function is selected.
22	LGS2–LED/GEP 2 Select. This bit select either the rcv_match or gep<2> function for 21143 pin 102. • When set, the rcv_match function is selected, which provides a LED indicating the status of address recognition (sets when a packet passes address recognition. • When reset, the gep<2> function is selected. The gep<2> is a general-purpose port. After a hardware or software rest, the gep<2> function is selected.
23	LGS3–LED/GEP 3 Select. This bit selects either the LED or gep<3> function for the 21143 pin 103. • When this bit is set. The LED function is selected that, according to MiscHwOptions<0> (Gep3LedDefinition) bit in the serial ROM, provides an LED indicating either: (a) Network link integrity state for 10BASE-T or 100BASE-TX (b) both network activity and network link integrity state. • When this bit is reset, the gep<3> function is selected. If the pin was designated to be an input pin, it functions as an input link status pin for OnNow support. If the pin was designated to be an output pin, it functions as a general-purpose pin that performs output functions. After a hardware or software rest, the gep<3> function is selected.
24	GEI0–GEP Interrupt Enable or Port 0. • When set, the interrupt from gep<0> (CSR15<28>) is enabled. • When reset, the interrupt is disabled. After hardware or software reset the interrupt is disabled.
25	GEI1–GEP Interrupt Enable or Port 1. • When set, the interrupt from gep<1> (CSR15<29>) is enabled. • When reset, the interrupt is disabled. After hardware or software reset the interrupt is disabled.

Field	Description
26	RME–Receive Match Enable. • When set, receive match interrupt (CSR15<30>) is enabled. • When reset, the interrupt is disabled. After hardware or software reset the interrupt is disabled.
27	CWE–Control Write Enable. When CSR15 is written and SR15<27> value is 1, the general-purpose control bits will be written. These control bits include, interrupt enables. When CSR15 is written and CSR15<27> value is 0, only the general-purpose data (CSR15<19:16>) will be written.
28	GI0–General Purpose Interrupt. Indicates the gep<0> has changed state. This bit is set only when gep<0> is programmed to be a general-purpose input port. When this bit is set and the general-purpose port interrupt is enable (CSR15<24>=1), the general-purpose port interrupt (CSR5<26>) is set. This bit is cleared when reading CSR15 and is not automatically cleared when general-purpose port interrupt (CSR5<26>) is cleared.
29	GI1–General Purpose Interrupt. Indicates the gep<1> has changed state. This bit is set only when gep<1> is programmed to be a general-purpose input port. When bit is set and general-purpose port interrupt is enable (CSR15<24>=1), the general-purpose port interrupt (CSR5<26>) is set. This bit is cleared when reading CSR15 and is not automatically cleared when general-purpose port interrupt (CSR5<26>) is cleared.
30	RMI–Receive Match Interrupt. Indicates that a packet has passed address filtering. When this bit is set and receive match interrupt is enabled (CSR15<26>=1), the general-purpose port interrupt (CSR5<26>) is set. This bit is cleared when reading CSR15 and is NOT automatically cleared when reading general-purpose port interrupt CSR<26> is cleared.

7.0 Highlights on Migration to the 21143-xD

The following sections contain important information about migration issues.

7.1 21143-xD Applications Without PME/ACPI

For those customers who are migrating to the 21143-xD from the 21140-AF and are not intending to implement the Wake-Up-LAN and ACPI feature, the following PCI Configuration Registers and Command and Status Registers (CSRs), are not applicable.

Name	Description
CFCS<20>	New Capabilities bit
CCAP<7:0>	Capabilities Pointer
CCID	Capabilities ID register
CMPC	Power Management Control and Status register
CWUA0	Configuration Wake-Up-LAN IEEE Address registers
CWUA1	Configuration Wake-Up-LAN IEEE Address registers
SOP0	SecureON Password registers
SOP1	SecureON Password registers
CWUC	Configuration Wake-Up Command register
CSR1-PM	Wake-Up Frame Filter register
CSR2-PM	Wake-Up Events Control and Status register
CSR15<14>	RMP-Receive Magic Packet
CSR15<15>	HCKR-Hacker

7.2 Non-CardBus Applications

The following PCI Configuration Registers and CardBus Status Changed Registers are not applicable for non-CardBus applications:

Name	Description
CCIS	Card Information Structure
FER	Function Event register
FEMR	Function Event Mask register
FPSR	Function Present State register
FFER	Function Force Event register

7.3 SIA interface

A Manchester Encoder and Decoder (ENDEC) is fully integrated in the 21143-xD SIA interface. Therefore, an external ENDEC is not required.

7.4 Other External Component Requirements

The following are external component connections for the 21143-xD:

- Unused JTAG port requirements.
  - — Leave pin tms (pin 12), tdi (pin 13), and tdo (pin 14) open.
  - — Pull down pin tck (pin 11) through 4.75 Kohm resistor to ground.
- Current Reference and capacitor input.
  - — Pull down iref (pin 108) through a 2.4 Kohm resistor to ground.
  - — Pull down vcap_h (pin 110) through a 0.022 µF capacitor to ground.
- Crystal or Crystal Oscillator Connection.

  The 21143-xD requires a 20 MHz clock input to xtal1 (pin 106). Note that, if the 10BASE-T and AUI port are not used, the xtal1 (pin 106) can be provided with any clock source. There are two ways to provide sources for this connection method:
  - — An external 20MHz crystal connects to xtal1, pin 106. Please refer to the *DIGITAL Semiconductor 21143 Connection to the Network Using Physical Layer Devices: An Application Note,* for details on how to connect an external crystal to xtal1 and xtal2, pin 106 and 105.
  - — A 20 MHz clock source from SYM PHY or txclk signal from MII PHY can be directly connected to xtal1, pin 106, of the 21143-xD. Pin xtal2, pin 105, of the 21143-xD can be left open.

7.5 Serial ROM Programming

The 21143-xD supports two sizes of serial ROM, 1 Kb and 4 Kb. The serial ROM has three types of information:

- The ID and Magic block. These two information blocks are where the 21143-xD reads from without software driver involvement. The ID block is read upon a hardware reset or when the 21143-xD transitions from the D3 power state to the D0 power state. The Magic block is read when the 21143-xD transitions from D0 power state to any other lower power state, D1, D2, or D3, or when the 21143-xD enters the Wake-Up-LAN (Magic Packet) mode.
- Network Media Connection information. This information is where the driver accesses to read what media connection types that the network adapter supports.
- CardBus Card Information Structure, CIS, data.

The 21143-xD supports only extended info serial ROM blocks. Please, refer to Intel's latest *Serial ROM Programming Utilities* and *Serial ROM Specification for DC21x4 devices*, version 4.05, for details on new fields added in the ID block, Magic block, and CIS. It can be downloaded from http://www.intel.com/design/network/new21/download/dsc-software-nc.htm

For SIA media connection, the 21143 has on-chip integrated 10BASE-T and AUI capability as opposed to the 21140. Please refer to Block Type 2 used for the 21142. For details refer to the *Serial ROM Specification Format*, version 4.05.

For MII PHY media connection, please refer to Block Type 3 used for the 21142. For details refer to the *Serial ROM Specification Format*, version 4.05.

For SYM PHY media connection, the 21143 fully implements Autonegotiation (NWAY) capability as opposed to the 21140, please refer to Block Type 4 used for the 21143-xD. For details refer to the *Serial ROM Specification Format*, version 4.05.

8.0 Hardware Characteristics

The following table compares the temperature and power characteristics of the 21140-AF with the 21143-xD.

Characteristics	21140-AF	21143-xD
Storage temperature range	–55°C to +125°C (–67°F to +257°F)	–55°C to +125°C (–67°F to +257°F)
Operating temperature range	0°C to 70°C (32°F to 158°F)	0°C to 70°C (32°F to 158°F)
Package	144-pin PQFP	144-pin MQFP, 144-pin LQFP[1]
Power supply	Vdd = 3.3 V, Vdd_clamp = 5 V or 3.3 V	Vdd = 3.3 V, Vdd_clamp = 5 V or 3.3 V
Power dissapation @ Vdd = 3.3 V	413 mW maximum	560 mW maximum
Frequency = 33 MHz PCI clock		
Sleep mode	198 mW maximum	110 mW maximum
Snooze mode	248 mW maximum	225 mW maximum

1. For the 21143-xD, the PQFP package type has been reidentified as the MQFP, and the TQFP package type has been reidentified as the LQFP. This was done to conform to industry standard. The physical characteristics are the same for both package identifiers.

9.0 Ordering Intel Products

To order the 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller or evaluation boards, contact your local distributor. The following table lists some of the products available.

Product	Order number
21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (MQFP)	21143–PD
21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (LQFP)	21143–TD
21143 PCI Evaluation Board Kit	21A43–04
21143 CardBus Evaluation Card Kit	21A43–02

For more information about the 21143, visit the Intel World Wide Web Internet site at: http://developer.intel.com/design/network/index.htm

The Intel Massachusetts Customer Technology Center continues to service your Network Product technical inquiries. The Customer Technology Center can be contacted at:

1-978-568-7474 (International & Domestic)

1-978-568-6698 (FAX)

Techsup@intel.com (EMAIL)