Power Management in Intel's 21143-xD Ethernet Controllers

Application Note

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1.0 Overview

This document provides design guidelines for applications that take advantage of the power management support included in the 21143-xD (21143-PD and 21143-TD) PCI/CardBus 10/100 Mb/s Ethernet LAN Controller.

Note: Throughout this application note, the 21143-xD is also referred to as the controller or the Ethernet controller.

This document explains power management design considerations and guidelines to be used while designing a power-management-aware system or a network interface card (NIC) based on the 21143-xD.

Appendix A provides references to additional power management information that appears in the *21143 PCI/CardBus 10/100 Mb/s Ethernet LAN Controller Hardware Reference Manual* and the *21X4 Serial ROM Format,* Version 4.04.

The Ethernet controllers comply with revision 1.0 of the *Advanced Configuration and Power Interface (ACPI) Specification* and the *Device Class Power Management Reference Specification: Network Device Class* under the OnNow* architecture for PC97 and PC98.

This application note describes only the power management aspects of the controllers and refers only to the new power management features; specifically, support for the *PCI Bus Power Management Interface Specification*, the *Advanced Configuration and Power Interface (ACPI) Specification*, the *Device Class Power Management Reference Specification: Network Device Class* and the *Device Class Power Management Reference Specification: Communications Device Class* under the OnNow architecture for PC97 and PC98.

For a description of sleep, snooze, clkrun, and remote wake-up-LAN modes, refer to the *21143 PCI/CardBus 10/100 Mb/s Ethernet LAN Controller Hardware Reference Manual.*

1.1 Power Management Events

A power management event (PME) is a mechanism that a device uses to report events that might change the system's power state. The response to a PME might be to move the entire system, or specific devices, to the fully operational power state or to a lower power state, depending upon the event and the current power state.

The following three PME events, for the 21143-xD, are defined in revision 1.0 of the *Device Class Power Management Reference Specification: Network Device Class.*

link change

Magic Packet

wake-up frame

1.2 Power Management Event Notification

The controllers notify the system of a power management event by asserting the wake signal (gep<2>/rcv_match/wake).

Table 1 describes the register and serial ROM bits that control the wake signal.

Table 1. Wake Signal Control Bits

Bit	Location	Description
CPMC<8>	PCI configuration space	PME_Enable — Enables the assertion of the wake signal when a PME occurs.
CPMC<15>	PCI configuration space	PME_Status (deassert wake) — Indicates that a PME has occurred. When this bit is cleared, the wake signal is deasserted.
CFCS<20>	PCI configuration space	New Capabilities —The value of this bit determines whether the controller implements a list of new capabilities. The value of this bit is loaded from the Func0_HwOptions<3> bit (PME_Enable) in the serial ROM.
CCID<31>	PCI configuration space	PME_Support $D3_{cold}$ —If this bit is set, the controller asserts PME when in the $D3_{cold}$ power state. If this bit is not set, the controller does not assert PME when in the $D3_{cold}$ power state. This bit is loaded from the Func0_HwOptions<6> bit (OnNowD3ColdCap) in the serial ROM.
MiscHwOptions<1>	Serial ROMs	PME_STSCHG —Sets wake signal polarity.

Note: Fields in the CardBus* status-changed registers also enable the wake signal and check its status.

The wake signal is not asserted by either function when that function is in the D0 power state because D0 is the fully awake power state.

The wake signal provides an active output only when the controllers assert the output; otherwise, the output is tri-stated. For example, when the wake signal is programmed to be active low and it is asserted, it drives the output to ground. When it is not asserted, it floats the output.

The wake signal is the source for reporting a PME in either the PCI or CardBus system. In the PCI system, a PME is reported on the PME# line; in the CardBus system, it is reported on the CSTSCHG line. These signal pins are described in Sections 1.2.1 and 1.2.2.

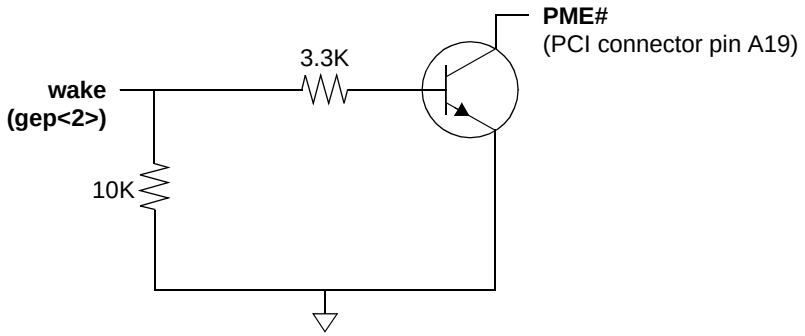
If the Ethernet function generates the PME, the specific status bits can be read to determine whether the PME was generated by a link change, Magic Packet, or wake-up frame.

1.2.1 PME#

The *PCI Bus Power Management Interface Specification*, Revision 1.0, specifies that the PME# signal is used to notify the system of a PME. The PME# signal is an open drain output signal assigned to PCI connector pin A19. This signal should be driven low to report a PME to the system. When this circuit is used, MiscHwOptions<1> should be set.

Figure 1 shows an example circuit that is designed to isolate the PME# signal when power is removed in the $D3_{cold}$ state. This circuit can be used in order to comply with the *PCI Bus Power Management Interface Specification.*

Figure 1. Open Drain PME# from wake



Note: This circuit applies only to applications that do not guarantee auxiliary power to the controllers in the $D3_{cold}$ power state (typically, add-in cards). When using this circuit, MiscHwOptions<1> should be set.

1.2.2 CSTSCHG

CardBus devices use the CSTSCHG signal, which is specific to the CardBus, to generate PMEs. The wake pin can be connected directly to the CSTSCHG pin of the CardBus connector. The CardBus defines the CSTSCHG signal to be active high; consequently, the wake signal polarity must be programmed by setting the wake polarity bit (serial ROM MiscHwOptions<1> = 1).

2.0 Implementations

This section describes several design examples of power management implementations with the 21143-xD.

2.1 Motherboard Design

Figure 2 shows an example of a motherboard design to support the $D3_{cold}$ power state.

Figure 2. Motherboard Design

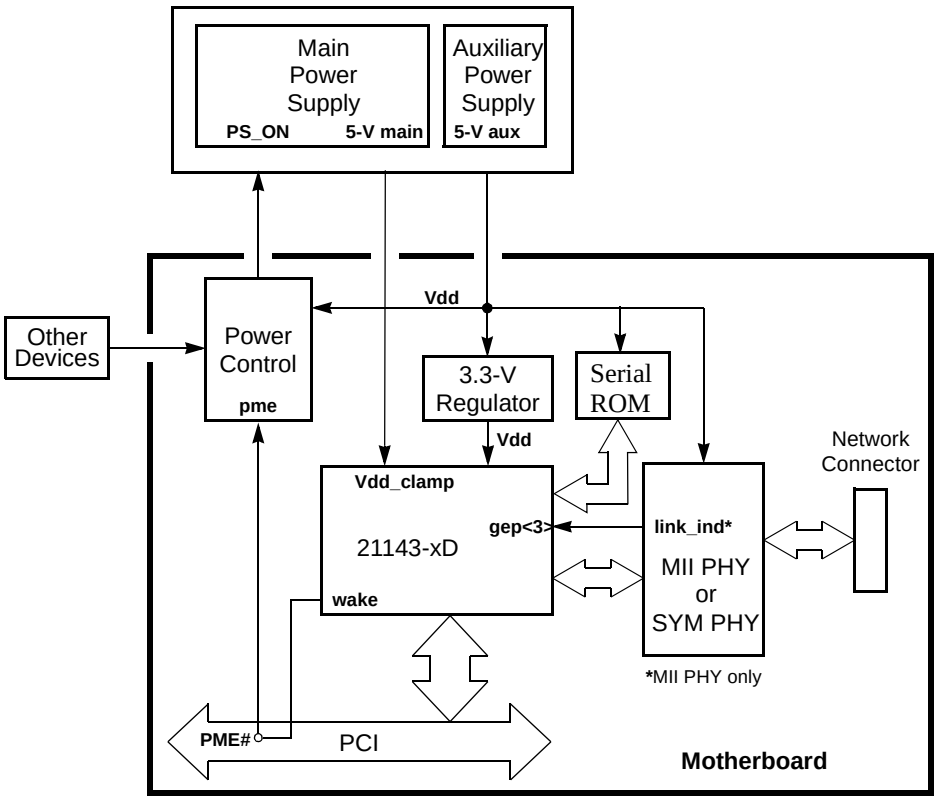


Table 2 lists the serial ROM settings for the design in Figure 2.

Table 2. Serial ROM Settings for a Motherboard Design

Bit	State	Description
MiscHwOptions<1>	0	**wake** signal polarity = active low.
Func0_HwOptions<3>	1	**wake** signal is enabled.
Func0_HwOptions<6>	1	PME is supported in the $D3_{cold}$ power state.

The Ethernet controller, serial ROM, and PHY are powered by the auxiliary 5 V power supply. The Ethernet controller operates at 3.3 V and requires a 3.3 V voltage regulator. These devices remain powered on when the main power is turned off. The main 5 V power supply is connected to Ethernet controller pin Vdd_clamp. The controller monitors Vdd_clamp to sense whether the main power is on.

The motherboard power-control circuit turns the main power supply on and off. This circuit always remains powered on by the auxiliary power supply and is responsible for turning on the main power supply based on a wake-up event. A wake-up event can be a PME# signal or inputs from other devices, such as the keyboard, mouse, or front panel on/off switch.

The wake signal generates a PME. Because wake is connected to PME# in the example circuit (Figure 2), wake must be active low. To program wake polarity as active low, the wake pin polarity bit is cleared (serial ROM MiscHwOptions<1> = 0). When wake is asserted, it drives the output to ground; when it is not asserted, the output floats.

When the Ethernet controller is not powered on, wake provides a path to ground. The PCI specification requires PME# sources to be isolated when power is removed from the controller while the system is in the $D3_{cold}$ state. The motherboard design described in this implementation assumes that the controller is permanently powered whenever power is applied to the motherboard. At no time is the auxiliary power off unless the whole system is off. Therefore, wake can be tied directly to the PCI bus PME# signal line and the circuit shown in Figure 2 is not needed.

If the Ethernet controller is not powered on and other parts of the system are powered on (for example, another device in the system is responsible for the wake-up and the auxiliary power to the Ethernet controller is turned off), then the circuit shown in Figure 2 should be added for the wake line connection to the PME# line and MiscHwOptions<1> should be set.

Some system designs power the controllers using the main power, and use the auxiliary power when the main power is off. These systems should have a switching circuit between the auxiliary and main power supply outputs and the devices on the motherboard.

OnNow requires that a link change is recognized as a PME. The Ethernet controller can detect link state changes when it is using its internal 10BASE-T port or an external, symbol-interface 100BASE-TX PHY device without any special connections to the PHY. In order to detect link state changes while connected to an MII PHY, a link indication signal from the PHY to the Ethernet controller is required. The Ethernet controller is designed to receive the link indication signal on the gep<3> pin and automatically generate a PME. This requires that the GEP be programmed as an input. The Ethernet controller assumes the input is in the link-pass state when the gep<3> pin is asserted high.

Note: When working with a non-MII PHY, gep<3> should not be programmed as an input in a power-management-aware system.

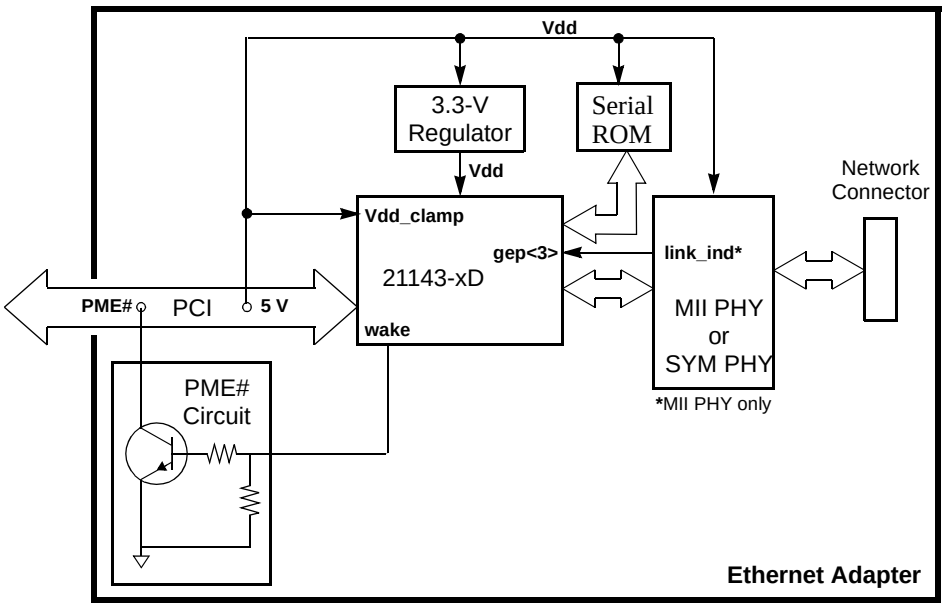
2.2 Add-In Card Design

Add-in cards can be installed into systems with the following configurations:

- Auxiliary power is not provided.
- Auxiliary power is provided to the motherboard but not to the add-in card.

Figure 3 shows an example of an add-in card design.

Figure 3. Add-In Card Design



Power is provided by the main power supply through the PCI Vdd. The PME transistor circuit is required to ensure that PME# is isolated from the PCI bus when auxiliary power is available to the system but not to the controller. The *PCI Bus Power Management Interface Specification*, Revision 1.0, does not define a line in the PCI connector through which auxiliary power can be passed. Therefore, this configuration does not support the $D3_{cold}$ power state because the Ethernet controller is powered down when the main PCI Vdd power supply is powered down.

Table 3 shows the serial ROM settings for this design.

Table 3. Serial ROM Settings for a Design Without Auxiliary Power

Bit	State	Description
MiscHwOptions<1>	1	wake signal polarity = active high.
Func0_HwOptions<3>	1	wake signal is enabled.
Func0_HwOptions<6>	0	PME is not supported in $D3_{cold}$ power state.

2.3 CardBus Design

Figure 4 shows an example of a CardBus design. The wake signal is connected directly to the CardBus CSTSCHG pin. Similar to the add-in card design, this configuration does not support the $D3_{cold}$ power state because there is no auxiliary power line in the CardBus connector.

Figure 4. CardBus Design

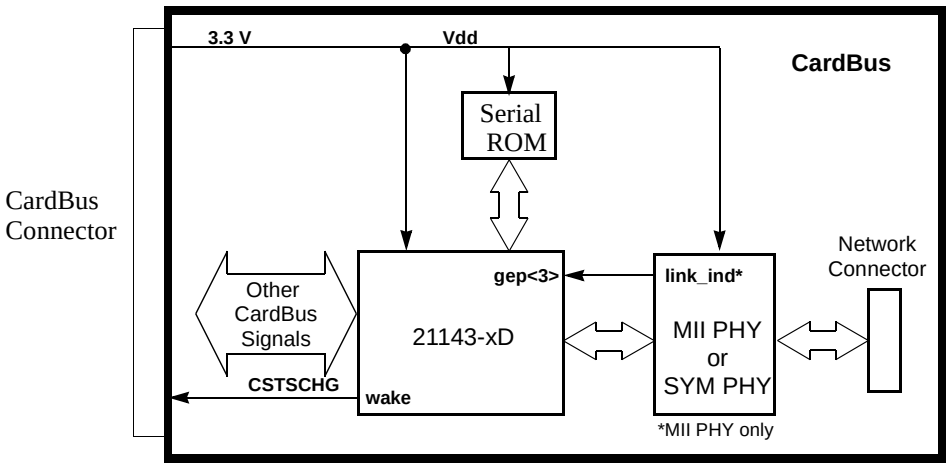


Table 4 shows the serial ROM settings for this design.

Table 4. Serial ROM Settings for a CardBus Design

Bit	State	Description
MiscHwOption <1>	1	wake signal polarity = active high.
Func0_HwOptions<3>	1	wake signal is enabled.
Func0_HwOptions<6>	0	PME is not supported in $D3_{cold}$ power state.

Appendix A Power Management References Locations

This appendix provides references to power management related information that appears in the *21143 PCI/CardBus 10/100 Mb/s Ethernet LAN Controller Hardware Reference Manual* and the *21X4 Serial ROM Format*, Version 4.04.

A.1 Registers

Tables 5 and 6 list sections in the *21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual* that describe power management registers.

Table 5. Configuration Space Register References

Register	Section
CFCS<20>	3.1.2.2
CCAP	3.1.2.10
CCID	3.1.2.12
CPMC	3.1.2.13

Table 6. Command and Status Register References

Register	Section
CSR0<26>	3.2.2.1
CSR1-PM	3.2.2.3
Wake-up frame filter block	3.2.2.4
CSR2-PM	3.2.2.6
FER	3.3.1
FEMR	3.3.2
FPSR	3.3.3
FFER	3.3.4

A.2 Pins

The following pins are related to power management:

Vdd
Vdd_clamp
gep<2>/rcv_match/wake
gep<3>/link

For a description of these pins, refer to Section 2.2 of the *21143 PCI/CardBus 10/100 Mb/s Ethernet LAN Controller Hardware Reference Manual.*

A.3 Serial ROM Fields

Table 7 lists references to power management information in the *21X4 Serial ROM Format*, Version 4.04.

Table 7. 21143-xD Serial ROM Fields References

Field/Bits	Section
MiscHwOptions	6.2
Func0_HwOptions bits <3,6:7>	6.3
Func1_HwOptions bits <4:5>	6.1

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