A Cirrus Logic Company

4/22/97

Performance Summary: CS8920 Datasheet Change

ISA Plug-and-Play Ethernet Controller (DS174PP1 MAR '96)

Corrections to The CS8920 Data Sheet

Page	Correction
7	Figure 1.3. Typical Connection Diagram: the label for pin 115 "HWSLEEP" should be changed to "SLEEP".
7	Figure 1.3. Typical Connection Diagram: the label for pin 116 "TESTSEL" should be changed to "TEST".
10	Table 2.2, Symbol MEMR should have an overscore indicating it is an active-low signal.
10	Table 2.2, Symbol MEMW should have an overscore indicating it is an active-low signal.
10	Table 2.2, Symbol MCS16 should have an overscore indicating it is an active-low signal.
10	Table 2.2, Symbol REFRESH should have an overscore indicating it is an active-low signal.
10	Table 2.2, Symbol IOR should have an overscore indicating it is an active-low signal.
10	Table 2.2, Symbol IOW should have an overscore indicating it is an active-low signal.
11	Table 2.2, Symbol IOCS16 should have an overscore indicating it is an active-low signal.
11	Table 2.2, Symbol SBHE should have an overscore indicating it is an active-low signal.
11	In table 2.2, add the following to description of /SBHE, "After a hardware or a software reset, provide a HIGH to LOW and then LOW to HIGH transition on /SBHE signal before any IO or memory access is done to the CS8920."
11	Table 2.2, Symbol DACK5, DACK6 and DACK7 should have overscores indicating active-low signals.
11	Table 2.2, Symbol CSOUT should have an overscore indicating it is an active-low signal.
13	Table 2.2, Symbol SLEEP should have an overscore indicating it is an active-low signal.
13	Table 2.2, Symbol LINKLED should have an overscore indicating it is an active-low signal.
13	Table 2.2, Symbol HC0 should have an overscore indicating it is an active-low signal.
13	Table 2.2, Symbol BSTATUS should have an overscore indicating it is an active-low signal.
13	Table 2.2, Symbol HC1 should have an overscore indicating it is an active-low signal.
13	Table 2.2, Symbol LANLED should have an overscore indicating it is an active-low signal.
13	Table 2.2, Symbol FDXLED should have an overscore indicating it is an active-low signal.
13	Table 2.2, Symbol TEST should have an overscore indicating it is an active-low signal.
21	Second column, paragraph 2, the first sentence should read, "Bits 9 through 0 of the Group Header specify a 10-bit PacketPage Address."
21	Second column, paragraph 2, the third line sentence should read, "Bits B and A of the Group Header are forced to 0, restricting the destination address range to the first 1024 bytes of PacketPage memory.
21	Figure 3.1. Group Header, the right bracket should be larged to include bit 9 and "9-bit PacketPage Address" should be changed to, "10-bit PacketPage address"
22	Paragraph ***Determining EEPROM Size,*** delete "(sequential error)" and "(non-sequential EEPROM)."

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Page	Correction
23	Paragraph ***EEPROM Readout Completion***, the first line should read, "Once all the configuration data are transferred to the appropriate PacketPage registers, the CS8920 adds the sum of the data bytes it read to the 2's complement checksum at the end of the configuration data to verify the Reset Configuration Block's data are valid."
25	**Table 3.8. Low-Power Mode Operation**: The SLEEP pin is defined as being pin 77. It should read "pin 116".
34	In the paragraph, *Auto-Select*:, the first sentence should read "In Auto-Select mode, the CS8920 automatically selects the 10BASE-T interface and powers down the AUI if valid packets or link pulses are detected by the 10BASE-T receiver."
37	**Figure 3.12 AUI**: The collision signal pins should be labeled as CI+ and CI- instead of CL+ and CL-.
40	**Table 4.1. PacketPage Memory Address Map**: the base address value "002c" should read "002Ch".
45	Section 4.4 **Status and Control Registers**, the first line should read, "The Status and Control registers are the primary registers used to control and check the status of the CS8920."
48	**Figure 4.2. Status and Control Register Summary**: the first occurrence of the row value "Not Applicable and Reserved, E-11" should be replaced with "Not Applicable and Reserved, F"
48	**Figure 4.2. Status and Control Register Summary**: the second occurrence of the row value "Not Applicable and Reserved, E-11" should be replaced with "Not Applicable and Reserved, 11"
48	**Figure 4.2. Status and Control Register Summary**: third row from the bottom, "Not Applicable and Reserved, 1B-1F" should be replaced with "Not Applicable and Reserved, 1B".
51	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 000011, where the LSB corresponds to Bit 0".
52	Add the following at the end of description for ***Register 4: Receiver Event (RxEvent, Read-only),*** "Value in RxEvent register is undefined when RxDMAOnly bit (Bit9, Register 3, RxCFG) is set."
53	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 000101, where the LSB corresponds to Bit 0".
54	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 000111, where the LSB corresponds to Bit 0".
57	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 001011, where the LSB corresponds to Bit 0".
58	Description for BIT F, RxDestiE, add the following after the last line, "If RxDestiE is set, the BufEvent could be RxDest or Rx128. After 128 bytes are received, the BufEvent changes from RxDest to Rx128."
60	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 001011, where the LSB corresponds to Bit 0".
62	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 010011, where the LSB corresponds to Bit 0".
63	Description for BIT C, PolarityOK, the third line should read, "If PolarityDis (Register 13, LineCTL, Bit C) is clear, the polarity is automatically corrected, if needed.
64	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 010101, where the LSB corresponds to Bit 0".
66	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 010111, where the LSB corresponds to Bit 0".
68	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 011001, where the LSB corresponds to Bit 0".
70	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 011101, where the LSB corresponds to Bit 0".

Page	Correction
71	***Register 1E: ISA Bus State***: the description for bit 8, FlpLink, should read "Set when the CS8920 has seen at least one FLP burst..."
74	Description for Individual Address, for Address 0015Dh replace "High-order byte of IA" with "octet 5 of IA".
74	Description for Individual Address, for Address 00158h replace "Low-order byte of IA" with "octet 0 of IA".
74	Description for Individual Address, delete the entire table.
75	***Plug and Play Activation Register***, Description: the second line of the description should read "and DMA accesses. When set, the CS8920 will respond to modes that are enabled."
75	***Plug and Play Activation Register***, last sentence of description should read "All other bits in this register are read as 0 after reset."
78	**Interrupt Number Register**: "Address 0371h" should be changed to "Address 0370h".
88	First column, the last line of text, the word "buffing" should be replaced with "buffering".
89	**Table 5.1. Physical Interface Configuration**: operation description of bit 8, AUIonly, delete the sentence "When clear, 10BASE-T selected."
89	**Table 5.1. Physical Interface Configuration**: operation description of bit 9, AutoAUI/10BT, add the sentence "When both bits 8 and 9 are clear, 10BASE-T selected."
93	First column, third paragraph, the sentence "A received frame is freed from commitment by any one of the following conditions:" should be replaced with "A received frame is freed from commitment by either of the following conditions:".
93	Top of second column, delete the first line "Or:" and entire item "3. The host reads part of the frame and then reads the...".
95	Second column, paragraph ***Broadcast Frames***:, the first sentence should read "Broadcast frames have a DA equal to FFFF FFFF FFFFh."
99	***5.5.4 Receive-DMA-Only Operation***, add the following as a new paragraph after the first paragraph, "The CS8920's DMA request pin remains active (HIGH), until all but one word is transferred. The DMA request pin goes inactive just before transfer of the last word. For an ISA bus, the DMA request signal is latched during a DMA cycle. Therefore a DMA controller will generate one more cycle after the CS8920's DMA request pin goes inactive. The CS8920 expects this additional DMA cycle after its DMA request pin goes inactive".
120	Table 6.1, second column, change the heading from FDXforce to FDX.
130	**SWITCHING CHARACTERISTICS**, for ***DMA READ***, change t_{DMAR2} MAX = 80 nS.
130	**SWITCHING CHARACTERISTICS**, for ***DMA READ***, for the parameter t_{DMAR2}, the start of measurement should be at the rising edge of the /IOR and not the falling edge of the /IOR as it is indicated in the timing diagram.