A Cirrus Logic Company

4/22/97

Performance Summary: CS8900 Datasheet Change

Highly-Integrated ISA Ethernet Controller (DS150PP2 DEC '95)

Corrections to the CS8900 Data Sheet

Page	Correction
7	**Figure 1.3. Typical Connection Diagram**: pin labeled "HWSLEEP" should be labeled with a pin number of "77".
7	**Figure 1.3. Typical Connection Diagram**: pin labeled "TESTSEL" should be labeled with a pin number of "76".
7	**Figure 1.3. Typical Connection Diagram**: pin labeled "HWSLEEP" should be labeled "SLEEP".
7	**Figure 1.3. Typical Connection Diagram**: pin labeled "TESTSEL" should be labeled "TEST".
8	**2.1 Pin Diagram**: The label for pin 77 "HWSLEEP" should read "SLEEP".
8	**2.1 Pin Diagram**: The label for pin 76 "TESTSEL" should read "TEST". All additional occurances of "TESTSEL" in the document should read "TEST"
9	In the table 2.2, add the following to description of AEN, "AEN should be inactive when performing an IO or memory access and it should be active during a DMA cycle."
9	Table 2.2, Symbol MEMR should have an overscore indicating it is an active-low signal.
9	Table 2.2, Symbol MEMW should have an overscore indicating it is an active-low signal.
9	Table 2.2, Symbol MEMCS16 should have an overscore indicating it is an active-low signal.
9	Table 2.2, Symbol REFRESH should have an overscore indicating it is an active-low signal.
9	Table 2.2, Symbol IOR should have an overscore indicating it is an active-low signal.
9	Table 2.2, Symbol IOW should have an overscore indicating it is an active-low signal.
9	Table 2.2, Symbol IOCS16 should have an overscore indicating it is an active-low signal.
10	Table 2.2, Symbol SBHE should have an overscore indicating it is an active-low signal.
10	In table 2.2, add the following to description of /SBHE, "After a hardware or a software reset, provide a HIGH to LOW and then LOW to HIGH transition on /SBHE signal before any IO or memory access is done to the CS8900."
10	Table 2.2, Symbol DMACK0 should have an overscore indicating it is an active-low signal.
10	Table 2.2, add the following to description of CHIPSEL, "The CHIPSEL is ignored for IO and DMA mode of the CS8900."
10	Table 2.2, Symbol ELCS should have an overscore indicating it is an active-low signal.
10	Table 2.2, Symbol CSOUT should have an overscore indicating it is an active-low signal.
12	Table 2.2, Symbol SLEEP should have an overscore indicating it is an active-low signal.
12	Table 2.2, Symbol LINKLED should have an overscore indicating it is an active-low signal.
12	Table 2.2, Symbol BSTATUS should have an overscore indicating it is an active-low signal.
12	Table 2.2, Symbol LANLED should have an overscore indicating it is an active-low signal.
14	Section 3.2, in paragraph ***Memory Mode operation***, the second line should read," the CS8900's internal registers and frame buffers are mapped into a".

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16	Section 3.3.3, in paragraph ***Bus Reset Considerations***, the second sentence should read, "The 3000h value can be used as part of the CS8900 signature when the system scans for the CS8900.
18	Table 3.6, description for Word Address 0Dh should read, "Individual Address Octet 0 and 1"
18	Table 3.6, description for Word Address 0Eh should read, "Individual Address Octet 2 and 3"
18	Table 3.6, description for Word Address 0Fh should read, "Individual Address Octet 4 and 5"
18	Table 3.6, description for Word Address 10h, the "hexadecimal sum of the bytes is D7h" should read, "hexadecimal sum of the bytes is D8h".
19	In the paragraph, ***Reset Configuration Block Checksum***, the last sentence should read, "Since the checksum is calculated as the 2's complement of the sum of all preceding bytes in the Reset Configuration Block, a total of 0 should result when the checksum value is added to the sum of the previous bytes.
20	Section 3.5, in paragraph ***EEPROM Command Execution***, the first line should read, "During the execution of a command, the two Opcode bits, followed by the six bits of address (for a 'C46 or 'CS46) or eight bits of address (for a 'C56, 'CS56, 'C66, or 'CS66), are shifted out of the CS8900, into the EEPROM.
31	In the paragraph, *Auto-Select*:, the first sentence should read "In Auto-Select mode, the CS8900 automatically selects the 10BASE-T interface and powers down the AUI if valid packets or link pulses are detected by the 10BASE-T receiver."
37	Table 4.1, # of bytes for PacketPage Address 0404h should be " -".
37	Table 4.1, # of bytes for PacketPage Address 0A00h should be "-".
37	Table 4.1, Type for PacketPage Address 0A00h should read "Write Only".
38	Section 4.3, ***Bus Interface Registers***, the ***I/O Base Address*** register: byte address 0020h and 0021h should be reversed.
39	DMA Channel Number Register, Address 0024h, the last line of the DMA channel assignment table should read, "0000 0011b = All DMRQ pins high impedance"
39	The last paragraph should read "After reset, if no EEPROM is found by the CS8900, then the register has the following initial state which corresponds to setting all DMRQ pins to high impedance."
44	Section 4.4 **Status and Control Registers**, the first line should read, "The Status and Control registers are the primary registers used to control and check the status of the CS8900."
48	Description for ISQ, 5th line in the paragraph should read, "BufEvent (Register C). The other two registers are counter-overflow reports: RxMISS (Register 10) and TxCOL".
49	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 000011, where the LSB corresponds to Bit 0".
49	Description for BIT 8, RxOKiE, add the following line at the end, "RxOK interrupt is not generated when DMA mode is used for frame reception."
50	Add the following at the end of description for ***Register 4: Receiver Event (RxEvent, Read-only),*** "Value in RxEvent register is undefined when RxDMAOnly bit (Bit9, Register 3, RxCFG) is set."
50	Description for BIT 6, IAHash, second line delete, "RxOK (Bit 8) is set,".
51	Description for BIT 5-0, first paragraph, delete the last line, "To write to this register, these bits must be 000101, where the LSB corresponds to Bit 0".
52	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 000111, where the LSB corresponds to Bit 0".
55	Description for BIT 5-0, delete the last line, "To write to this register, these bits must be 001011, where the LSB corresponds to Bit 0".
56	Description for BIT F, RxDestiE, add the following after the last line, "If RxDestiE is set, the BufEvent could be RxDest or Rx128. After 128 bytes are received, the BufEvent changes from RxDest to Rx128."

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58	Description for bit 5-0, change “identify this as the Bus Status Register,” to “identify this as the Receiver Miss Counter.”
59	Description for bit 5-0, change “identify this as the Bus Status Register,” to “identify this as the Transmit Collision Counter.”
60	Description for BIT 5-0, delete the last line, “To write to this register, these bits must be 010011, where the LSB corresponds to Bit 0”.
61	Description for BIT C, PolarityOK, the third sentence should read, “If PolarityDis (Register 13, LineCTL, Bit C) is clear, the polarity is automatically corrected, if needed.
62	Description for BIT 5-0, delete the last line, “To write to this register, these bits must be 010101, where the LSB corresponds to Bit 0”.
64	Description for BIT 5-0, delete the last line, “To write to this register, these bits must be 010111, where the LSB corresponds to Bit 0”.
64	Description for BIT 9, the first line should read, “When set, the /MEMCS16 pin goes low whenever the address on ISA bus [12..19]”.
66	Description for BIT 5-0, delete the last line, “To write to this register, these bits must be 011001, where the LSB corresponds to Bit 0”.
70	Description for Individual Address, for Address 0015Dh replace “High-order byte of IA” with “octet 5 of IA”.
70	Description for Individual Address, for Address 00158h replace “Low-order byte of IA” with “octet 0 of IA”.
70	Description for Individual Address, delete the entire table.
73	Second column, seventh paragraph, replace “on;y” with “only.”
74	**Section 4.10 I/O Space Operation**, the last line of the first paragraph, the colon at the end of the line should be changed to a period.
75	**Figure 4.4**, bits E-C are defined as 000b. They should be defined as 011b.
75	***I/O Mode Operation***, delete the last sentence “For these applications, the /ELCS pin is tied low.”
77	First column, first paragraph, last sentence, a closing parenthesis is needed at the end of the sentence.
77	Second column, third paragraph, the last sentence, “see Section 4.3.” should be changed to “See Section 4.3.”
79	First column, the last line of text, the word “buffing” should be replaced with “buffering”.
80	**Table 5.1. Physical Interface Configuration**: operation description of bit 8, AUIonly, delete the sentence “When clear, 10BASE-T selected.”
80	**Table 5.1. Physical Interface Configuration**: operation description of bit 9, AutoAUI/10BT, add the sentence “When both bits 8 and 9 are clear, 10BASE-T selected.”
81	Bottom first column, top of second column, items 1, 2, and 3, the semicolons should be replaced with commas.
81	**Early Interrupt Generation**: The first line of the paragraph should read “The CS8900 supports”.
84	First column, third paragraph, the sentence “A received frame is freed from commitment by any one of the following conditions:” should be replaced with “A received frame is freed from commitment by either of the following conditions:”.
84	First column, last line: remove the last line “Or:”.
84	Top of second column, delete entire item “3. The host reads part of the frame and then...”.
86	First column, item 1 starting, “At the start of the frame...”, delete the bar from over the word “*even*”.
86	Second column, paragraph ***Broadcast Frames***:, the first sentence should read “Broadcast frames have a DA equal to FFFF FFFF FFFFh.”

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90	***5.4.4 Receive-DMA-Only Operation***, add the following as a new paragraph after the first paragraph, "The CS8900's DMA request pin remains active (HIGH), until all but one word is transferred. The DMA request pin goes inactive just before the transfer of the last word. For an ISA bus, the DMA request signal is latched during a DMA cycle. Therefore a DMA controller will generate one more cycle after the CS8900's DMA request pin goes inactive. The CS8900 expects this additional DMA cycle after its DMA request pin goes inactive".
91	Caption for Table 5.9. should read "Table 5.9. RxDMAFrame Bit".
101	First column, last line, delete "as follows:" and place a period after the word "Space".
107	Table 6.1, second column, change the heading from FDXforce to FDX.
115	**SWITCHING CHARACTERISTICS**, for ***16-BIT I/O READ, IOCHRDY NOT USED***, change t_{IOR2} (Min) to 10 nS.
115	**SWITCHING CHARACTERISTICS**, for ***16-BIT I/O READ, IOCHRDY NOT USED***, change t_{IOR4} (Min) to 0 nS.
115	**SWITCHING CHARACTERISTICS**, for ***16-BIT I/O READ, IOCHRDY NOT USED***, change t_{IOR5} (Min) to 35 nS.
116	**SWITCHING CHARACTERISTICS**, for ***16-BIT MEMORY READ, IOCHRDY NOT USED***, change t_{MEMR2} (Min) to 10 nS.
116	**SWITCHING CHARACTERISTICS**, for ***16-BIT MEMORY READ, IOCHRDY NOT USED***, change t_{MEMR6} (Min) to 35 nS.
117	**SWITCHING CHARACTERISTICS**, for ***DMA READ***, change t_{DMAR1} to 10 nS.
117	**SWITCHING CHARACTERISTICS**, for ***DMA READ***, change t_{DMAR3} to 145 nS.
117	**SWITCHING CHARACTERISTICS**, for ***16 BIT I/O WRITE***, change t_{IOW2} to 20 nS.
117	**SWITCHING CHARACTERISTICS**, for ***16 BIT I/O WRITE***, change t_{IOW4} to 0 nS.
117	**SWITCHING CHARACTERISTICS**, for ***16 BIT I/O WRITE***, change t_{IOW6} to 35 nS.
118	**SWITCHING CHARACTERISTICS**, for ***16 BIT MEMORY WRITE***, change t_{MEMW2} to 20 nS.
118	**SWITCHING CHARACTERISTICS**, for ***16 BIT MEMORY WRITE***, change t_{MEMW3} to 110 nS.
118	**SWITCHING CHARACTERISTICS**, for ***16 BIT MEMORY WRITE***, change t_{MEMW5} to 0 nS.
118	**SWITCHING CHARACTERISTICS**, for ***16 BIT MEMORY WRITE***, change t_{MEMW7} to 35 nS.
119	**SWITCHING CHARACTERISTICS,** for ***10BASE-T RECEIVE,*** change t_{TRX5} MAX = 320 ns
121	**SWITCHING CHARACTERISTICS,** for ***AUI RECEIVE,*** change t_{ARX3} MIN = 50 ns
121	**SWITCHING CHARACTERISTICS,** for ***AUI RECEIVE,*** change t_{ARX3} MAX = 150 ns
121	**SWITCHING CHARACTERISTICS,** for ***AUI RECEIVE,*** change t_{ARX5} MIN = 150 ns
121	**SWITCHING CHARACTERISTICS,** for ***AUI RECEIVE,*** delete value for t_{ARX5} TYP
121	**SWITCHING CHARACTERISTICS,** for ***AUI RECEIVE,*** change t_{ARX5} MAX = 250 ns
121	**SWITCHING CHARACTERISTICS,** for ***AUI COLLISION,*** change t_{ACL4} MIN = 50 ns
121	**SWITCHING CHARACTERISTICS,** for ***AUI COLLISION,*** change t_{ACL4} MAX = 200 ns
121	**SWITCHING CHARACTERISTICS,** for ***AUI COLLISION,*** change t_{ACL5} MIN = 150 ns
121	**SWITCHING CHARACTERISTICS,** for ***AUI COLLISION,*** delete value for t_{ACL5} TYP
121	**SWITCHING CHARACTERISTICS,** for ***AUI COLLISION,*** change t_{ACL5} MAX = 300 ns
125	**14.0 PHYSICAL DIMENSIONS** table values parameter e should read as per the following: Millimeters: MIN = 0.375, NOM = 0.5, MAX = 0.625 INCHES: MIN = 0.015, NOM = 0.020, MAX = 0.025