CSR65: Next Transmit Buffer Address Upper

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	NXBAU	Contains the upper 16 bits of the next transmit buffer address from which the Am79C972 controller will transmit an outgoing frame. Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.

CSR66: Next Transmit Byte Count

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-12	RES	Reserved locations. Read and written as zeros.
11-0	NXBC	Next Transmit Byte Count. This field is a copy of the BCNT field of TMD1 of the next transmit descriptor. Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.

CSR67: Next Transmit Status

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	NXST	Next Transmit Status. This field is a copy of bits 31-16 of TMD1 of the next transmit descriptor. Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.
7-0	RES	Reserved locations. Read and written as zeros. Accessible only when either the STOP or the SPND bit is set.

CSR72: Receive Ring Counter

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	RCVRC	Receive Ring Counter location. Contains a two's complement binary number used to number the current receive descriptor. This counter interprets the value in CSR76 as pointing to the first descriptor. A counter value of zero corresponds to the last descriptor in the ring. Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.

CSR74: Transmit Ring Counter

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	XMTRC	Transmit Ring Counter location. Contains a two's complement binary number used to number the current transmit descriptor. This counter interprets the value in CSR78 as pointing to the first descriptor. A counter value of zero corresponds to the last descriptor in the ring. Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.

CSR76: Receive Ring Length

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	RCVRL	Receive Ring Length. Contains the two's complement of the receive descriptor ring length. This register is initialized during the Am79C972 controller initialization routine based on the value in the RLEN field of the initialization block. However, this register can

be manually altered. The actual receive ring length is defined by the current value in this register. The ring length can be defined as any value from 1 to 65535.

Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.

CSR78: Transmit Ring Length

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	XMTRL	Transmit Ring Length. Contains the two's complement of the transmit descriptor ring length. This register is initialized during the Am79C972 controller initialization routine based on the value in the TLEN field of the initialization block. However, this register can be manually altered. The actual transmit ring length is defined by the current value in this register. The ring length can be defined as any value from 1 to 65535. Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.

CSR80: DMA Transfer Counter and FIFO Threshold Control

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-14	RES	Reserved locations. Written as zeros and read as undefined.
13-12	RCVFW[1:0]	Receive FIFO Watermark. RCVFW controls the point at which receive DMA is requested in relation to the number of received bytes in the Receive FIFO. RCVFW specifies the number of bytes which must be present (once the frame has been verified as a non-runt) before receive DMA is requested. Note however that, if the network interface is operating in half-duplex mode, in order for receive DMA to be performed for a new frame, at least 64 bytes must have been received. This effectively avoids having to react to receive frames which are runts or suffer a collision during the slot time (512 bit times). If the Runt Packet Accept feature is enabled or if the network interface is operating in full-duplex mode, receive DMA will be requested as soon as either the RCVFW threshold is reached, or a complete valid receive frame is detected (regardless of length). When the FDRPAD (BCR9, bit 2) is set and the Am79C972 controller is in full-duplex mode, in order for receive DMA to be performed for a new frame, at least 64 bytes must have been received. This effectively disables the runt packet accept feature in full duplex. When operating in the NO-SRAM mode (no SRAM enabled), the Bus Receive FIFO and the MAC Receive operate like a single FIFO and the watermark value selected by RCVFW[1:0] sets the number of bytes that must be present in the FIFO before receive DMA is requested. When operating with the SRAM, the Bus Receive FIFO, and the MAC Receive FIFO operate independently on the bus side and MAC side of the SRAM, respectively. In this case, the watermark value set by RCVFW[1:0] sets the number of bytes that must be present in the Bus Receive FIFO only. See Table 23.

Table 23. Receive Watermark Programming

RCVFW[1:0]	Bytes Received
00	16
01	64
10	112
11	Reserved

Read/Write accessible only when either the STOP or the SPND bit is set. RCVFW[1:0] is set to a value of 01b (64 bytes) after H_RESET or S_RESET and is unaffected by STOP.

11-10 XMTSP[1:0] Transmit Start Point. XMTSP controls the point at which preamble transmission attempts to commence in relation to the number of bytes written to the MAC Transmit FIFO for the current transmit frame. When the entire frame is in the MAC Transmit FIFO, transmission will start regardless of the value in XMTSP. If the network interface is operating in half-duplex mode, regardless of XMTSP, the FIFO will not internally overwrite its data until at least 64 bytes (or the entire frame if shorter than 64 bytes) have been transmitted onto the network. This ensures that for collisions within the slot time window, transmit data need not be rewritten to the Transmit FIFO, and retries will be handled autonomously by the MAC. If the Disable Retry feature is enabled, or if the network is operating in full-duplex mode, the Am79C972 controller can overwrite the beginning of the frame as soon as the data is transmitted, because no collision handling is required in these modes.

Note that when the SRAM is being used, if the NOUFLO bit (BCR18, bit 11) is set to 1, there is the additional restriction that the complete transmit frame must be DMA'd into the Am79C972 controller and reside within a combination of the Bus Transmit FIFO, the SRAM, and the MAC Transmit FIFO.

When the SRAM is used, SRAM_SIZE > 0, there is a restriction that the number of bytes written is a combination of bytes written into the Bus Transmit FIFO and the MAC Transmit FIFO. The Am79C972 controller supports a mode that will wait until a full packet is available before commencing with the transmission of preamble. This mode is useful in a system where high latencies cannot be avoided. See Table 24.

Read/Write accessible only when either the STOP or the SPND bit is set. XMTSP is set to a value of 01b (64 bytes) after H_RESET or S_RESET and is unaffected by STOP.

Table 24. Transmit Start Point Programming

XMTSP[1:0]	SRAM_SIZE	Bytes Written
00	0	20
01	0	64
10	0	128
11	0	220 max
00	>0	36 (NOUFLO = 0)
01	>0	64 (NOUFLO = 0)
10	>0	128 (NOUFLO = 0)
11	>0	Full Packet when NOUFLO bit is set

9-8 XMTFW[1:0] Transmit FIFO Watermark. XMTFW specifies the point at which transmit DMA is requested, based upon the number of bytes that could be written to the Transmit FIFO without FIFO overflow. Transmit DMA is requested at any time when the number of bytes specified by XMTFW could be written to the FIFO without causing Transmit FIFO overflow, and the internal microcode engine has reached a point where the Transmit FIFO is checked to determine if DMA servicing is required.

When operating in the NO-SRAM mode (no SRAM enabled), SRAM_SIZE set to 0, the Bus Transmit FIFO and the MAC

Transmit FIFO operate like a single FIFO and the watermark value selected by XMTFW[1:0] sets the number of FIFO byte locations that must be available in the FIFO before receive DMA is requested.

When operating with the SRAM, the Bus Transmit FIFO and the MAC Transmit FIFO operate independently on the bus side and MAC side of the SRAM, respectively. In this case, the watermark value set by XMTFW[1:0] sets the number of FIFO byte locations that must be available in the Bus Transmit FIFO. See Table 25.

Table 25. Transmit Watermark Programming

XMTFW[1:0]	Bytes Available
00	16
01	64
10	108
11	Reserved

Read/Write accessible only when either the STOP or the SPND bit is set. XMTFW is set to a value of 00b (16 bytes) after H_RESET or S_RESET and is unaffected by STOP.

7-0 DMATC[7:0] DMA Transfer Counter. Writing and reading to this field has no effect. Use MAX_LAT and MIN_GNT in the PCI configuration space.

CSR82: Transmit Descriptor Address Pointer Lower

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	TXDAPL	Contains the lower 16 bits of the transmit descriptor address corresponding to the last buffer of the previous transmit frame. If the previous transmit frame did not use buffer chaining, then TXDAPL contains the lower 16 bits of the previous frame's transmit descriptor address. When both the STOP or SPND bits are cleared, this register is updated by Am79C972 controller immediately before a transmit descriptor write. Read accessible always. Write accessible through the PXDAL bits (CSR60) when the STOP or SPND bit is set. TXDAPL is set to 0 by H_RESET and are unaffected by S_RESET or STOP.

CSR84: DMA Address Register Lower

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	DMABAL	This register contains the lower 16 bits of the address of system memory for the current DMA cycle. The Bus Interface Unit controls the Address Register by issuing increment commands to increment the memory address for sequential operations. The DMABAL register is undefined until the first Am79C972 controller DMA operation. Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.

CSR85: DMA Address Register Upper

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	DMABAU	This register contains the upper 16 bits of the address of system memory for the current DMA cycle. The Bus Interface Unit controls the Address Register by issuing increment commands to increment the memory address for sequential operations. The DMABAU register is undefined until the first Am79C972 controller DMA operation.

		Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.

CSR86: Buffer Byte Counter

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-12	RES	Reserved. Read and written with ones.
11-0	DMABC	DMA Byte Count Register. Contains the two's complement of the current size of the remaining transmit or receive buffer in bytes. This register is incremented by the Bus Interface Unit. The DMABC register is undefined until written. Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.

CSR88: Chip ID Register Lower

Bit	Name	Description
31-28	VER	Version. This 4-bit pattern is silicon-revision dependent. Read accessible only when either the STOP or the SPND bit is set. VER is read only. Write operations are ignored.
27-12	PARTID	Part number. The 16-bit code for the Am79C972 controller is 0010 0110 0010 0100 (2624h). This register is exactly the same as the Device ID register in the JTAG description. However, this part number is different from that stored in the Device ID register in the PCI configuration space. Read accessible only when either the STOP or the SPND bit is set. PARTID is read only. Write operations are ignored.
11-1	MANFID	Manufacturer ID. The 11-bit manufacturer code for AMD is 00000000001b. This code is per the JEDEC Publication 106-A. Note that this code is not the same as the Vendor ID in the PCI configuration space. Read accessible only when either the STOP or the SPND bit is set. VER is read only. MANFID is read only. Write operations are ignored.
0	ONE	Always a logic 1. Read accessible only when either the STOP or the SPND bit is set. VER is read only. ONE is read only. Write operations are ignored.

CSR89: Chip ID Register Upper

Bit	Name	Description
31-16	RES	Reserved locations. Read as undefined.
15-12	VER	Version. This 4-bit pattern is silicon-revision dependent. Read accessible only when either the STOP or the SPND bit is set. VER is read only. VER is read only. Write operations are ignored.
11-0	PARTIDU	Upper 12 bits of the Am79C972 controller part number, i.e., 0010 0110 0010b (262h). Read accessible only when either the STOP or the SPND bit is set. VER is read only. PARTIDU is read only. Write operations are ignored.

CSR92: Ring Length Conversion

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	RCON	Ring Length Conversion Register. This register performs a ring length conversion from an encoded value as found in the initialization block to a two's complement

value used for internal counting. By writing bits 15-12 with an encoded ring length, a two's complemented value is read. The RCON register is undefined until written.

Read/Write accessible only when either the STOP or the SPND bit is set. These bits are unaffected by H_RESET, S_RESET, or STOP.

CSR100: Bus Timeout

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	MERRTO	This register contains the value of the longest allowable bus latency (interval between assertion of $\overline{REQ}$ and assertion of $\overline{GNT}$) that a system may insert into an Am79C972 controller master transfer. If this value of bus latency is exceeded, then a MERR will be indicated in CSR0, bit 11, and an interrupt may be generated, depending upon the setting of the MERRM bit (CSR3, bit 11) and the IENA bit (CSR0, bit 6). The value in this register is interpreted as the unsigned number of bus clock periods divided by two, (i.e., the value in this register is given in 0.1 µs increments.) For example, the value 0600h (1536 decimal) will cause a MERR to be indicated after 153.6 µs of bus latency. A value of 0 will allow an infinitely long bus latency, i.e., bus timeout error will never occur. Read/Write accessible only when either the STOP or the SPND bit is set. This register is set to 0600h by H_RESET or S_RESET and is unaffected by STOP.

CSR112: Missed Frame Count

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	MFC	Missed Frame Count. Indicates the number of missed frames. MFC will roll over to a count of 0 from the value 65535. The MFCO bit of CSR4 (bit 8) will be set each time that this occurs. Read accessible always. MFC is read only, write operations are ignored. MFC is cleared by H_RESET or S_RESET or by setting the STOP bit.

CSR114: Receive Collision Count

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	RCC	Receive Collision Count. Indicates the total number of collisions encountered by the receiver since the last reset of the counter. RCC will roll over to a count of 0 from the value 65535. The RCVCCO bit of CSR4 (bit 5) will be set each time that this occurs. Read accessible always. RCC is read only, write operations are ignored. RCC is cleared by H_RESET or S_RESET, or by setting the STOP bit.

CSR116: OnNow Power Mode Register

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-11	RES	Reserved locations. Written as zeros and read as undefined.
10	PME_EN_OVR	PME_EN Overwrite. When this bit is set and the MPMAT or LCDET bit is set, the $\overline{PME}$ pin will always be asserted regardless of the state of PME_EN bit.

Read/Write accessible only when either the STOP bit or the SPND bit is set. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

9 LCDET — Link Change Detected. This bit is set when the MII auto-polling logic detects a change in link status and the LCMODE bit is set.

LCDET is cleared when power is initially applied (POR).

Read/Write accessible only when either the STOP bit or the SPND bit is set. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

8 LCMODE — Link Change Wake-up Mode. When this bit is set to 1, the LCDET bit gets set when the MII auto polling logic detects a Link Change.

Read/Write accessible only when either the STOP bit or the SPND bit is set. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

7 PMAT — Pattern Matched. This bit is set when the PMMODE bit is set and an OnNow pattern match occurs.

PMAT is cleared when power is initially applied (POR).

Read/Write accessible only when either the STOP bit or the SPND bit is set. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

6 EMPPLBA — Magic Packet Physical Logical Broadcast Accept. If both EMPPLBA and MPPLBA (CSR5, bit 5) are at their default value of 0, the Am79C972 controller will only detect a Magic Packet frame if the destination address of the packet matches the content of the physical address register (PADR). If either EMPPLBA or MPPLBA is set to 1, the destination address of the Magic Packet frame can be unicast, multicast, or broadcast. Note that the setting of EMPPLBA and MPPLBA only affects the address detection of the Magic Packet frame. The Magic Packet frame's data sequence must be made up of 16 consecutive physical addresses (PADR[47:0]) regardless of what kind of destination address it has.

Read/Write accessible always. EMPPLBA is set to 0 by H_RESET or S_RESET and is not affected by setting the STOP bit.

5 MPMAT — Magic Packet Match. This bit is set when PCnet-FAST+ detects a Magic Packet while it is in the Magic Packet mode.

MPMAT is cleared when power is initially applied (POR).

Read/Write accessible only when either the STOP bit or the SPND bit is set. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

4 MPPEN — Magic Packet Pin Enable. When this bit is set, the device enters the Magic Packet mode when the PG input goes LOW or MPEN bit (CSR5, bit 2) gets set to 1. This bit is OR'ed with MPEN bit (CSR5, bit 2).

Read/Write accessible only when either the STOP bit or the SPND bit is set. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

3 RWU_DRIVER — RWU Driver Type. If this bit is set to 1, RWU is a totem pole driver; otherwise RWU is an open drain output.

Read/Write accessible only when either the STOP bit or the SPND bit is set. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

2 RWU_GATE — RWU Gate Control. If this bit is set, RWU is forced to the high Impedance State when PG is LOW, regardless of the state of the MPMAT and LCDET bits.

		Read/Write accessible only when either the STOP bit or the SPND bit is set. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
1	RWU_POL	RWU Pin Polarity. If RWU_POL is set to 1, the RWU pin is normally HIGH and asserts LOW; otherwise RWU is normally LOW and asserts HIGH. Read/Write accessible only when either the STOP bit or the SPND bit is set. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
0	RST_POL	PHY_RST Pin Polarity. If the PHY_POL is set to 1, the PHY_RST pin is active LOW; otherwise PHY_RST is active HIGH. Read/Write accessible only when either the STOP bit or the SPND bit is set. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

CSR122: Advanced Feature Control

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-1	RES	Reserved locations. Written as zeros and read as undefined.
0	RCVALGN	Receive Packet Align. When set, this bit forces the data field of ISO 8802-3 (IEEE/ANSI 802.3) packets to align to 0 MOD 4 address boundaries (i.e., DWord aligned addresses). It is important to note that this feature will only function correctly if all receive buffer boundaries are DWord aligned and all receive buffers have 0 MOD 4 lengths. In order to accomplish the data alignment, the Am79C972 controller simply inserts two bytes of random data at the beginning of the receive packet (i.e., before the ISO 8802-3 (IEEE/ANSI 802.3) destination address field). The MCNT field reported to the receive descriptor will not include the extra two bytes. Read/Write accessible always. RCVALGN is cleared by H_RESET or S_RESET and is not affected by STOP.

CSR124: Test Register 1

This register is used to place the Am79C972 controller into various test modes. The Runt Packet Accept is the only user accessible test mode. All other test modes are for AMD internal use only.

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-4	RES	Reserved locations. Written as zeros and read as undefined.
3	RPA	Runt Packet Accept. This bit forces the Am79C972 controller to accept runt packets (packets shorter than 64 bytes). Read accessible always; write accessible only when STOP is set to 1. RPA is cleared by H_RESET or S_RESET and is not affected by STOP.
2-0	RES	Reserved locations. Written as zeros and read as undefined.

CSR125: MAC Enhanced Configuration Control

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-8	IPG	Inter Packet Gap. Changing IPG allows the user to program the Am79C972 controller for aggressiveness on a network. By changing the default value of 96 bit times (60h) the user can adjust the fairness or aggressiveness of the Am79C972 MAC on the network. By programming a lower number of bit times other then the ISO/IEC 8802-3 standard requires, the Am79C972 MAC will become more aggressive on the network. This aggressive nature will give rise to the Am79C972 controller possibly “capturing the network” at times by forcing other

less aggressive nodes to defer. By programming a larger number of bit times, the Am79C972 MAC will become less aggressive on the network and may defer more often than normal. The performance of the Am79C972 controller may decrease as the IPG value is increased from the default value.

***Note**: Programming of the IPG should be done in nibble intervals instead of absolute bit times. The decimal and hex values do not match due to delays in the part used to make up the final IPG. Changes should be added or subtracted from the provided hex value on a one-for-one basis.*

CAUTION: Use this parameter with care. By lowering the IPG below the ISO/IEC 8802-3 standard 96 bit times, the Am79C972 controller can interrupt normal network behavior.

Read accessible always. Write accessible when the STOP bit is set to 1. IPG is set to 60h (96 Bit times) by H_RESET or S_RESET and is not affected by STOP.

7-0 IFS1

InterFrameSpacingPart1. Changing IFS1 allows the user to program the value of the InterFrameSpacePart1 timing. The Am79C972 controller sets the default value at 60 bit times (3ch). See the subsection on *Medium Allocation* in the section *Media Access Management* for more details. The equation for setting IFS1 when IPG ≥ 96 bit times is:

IFS1 = IPG - 36 bit times

***Note**: Programming of the IPG should be done in nibble intervals instead of absolute bit times due to the MII. The decimal and hex values do not match due to delays in the part used to make up the final IPG. Changes should be added or subtracted from the provided hex value on a one-for-one basis. Due to changes in synchronization delays internally through different network ports, the IFS1 can be off by as much as +12 bit times.*

Read accessible always. Write accessible only when the SPND bit or the STOP bit is set to 1. IFS1 is set to 3ch (60 bit times) by H_RESET or S_RESET and is not affected by STOP.

Bus Configuration Registers

The Bus Configuration Registers (BCR) are used to program the configuration of the bus interface and other special features of the Am79C972 controller that are not related to the IEEE 8802-3 MAC functions. The BCRs are accessed by first setting the appropriate RAP value and then by performing a slave access to the BDP. See Table 26.

All BCR registers are 16 bits in width in Word I/O mode (DWIO = 0, BCR18, bit 7) and 32 bits in width in DWord I/O mode (DWIO = 1). The upper 16 bits of all BCR registers is undefined when in DWord I/O mode. These bits should be written as zeros and should be treated as undefined when read. The default value given for any BCR is the value in the register after H_RESET. Some of these values may be changed shortly after H_RESET when the contents of the external EEPROM is automatically read in. None of the BCR register values are affected by the assertion of the STOP bit or S_RESET.

Note that several registers have no default value. BCR0, BCR1, BCR3, BCR8, BCR10-17, and BCR21 are reserved and have undefined values. BCR2 and BCR34 are not observable without first being programmed through the EEPROM read operation or a user register write operation.

BCR0, BCR1, BCR16, BCR17, and BCR21 are registers that are used by other devices in the PCnet family. Writing to these registers have no effect on the operation of the Am79C972 controller.

Writes to those registers marked as “Reserved” will have no effect. Reads from these locations will produce undefined values.

Table 26. BCR Registers

RAP	Mnemonic	Default	Name	Programmability	
				User	EEPROM
0	MSRDA	0005h	Reserved	No	No
1	MSWRA	0005h	Reserved	No	No
2	MC	0002h	Miscellaneous Configuration	Yes	Yes
3	Reserved	N/A	Reserved	No	No
4	LED0	00C0h	LED0 Status	Yes	Yes
5	LED1	0084h	LED1 Status	Yes	Yes
6	LED2	0088h	LED2 Status	Yes	Yes
7	LED3	0090h	LED3 Status	Yes	Yes
8	Reserved	N/A	Reserved	No	No
9	FDC	0000h	Full-Duplex Control	Yes	Yes
10-15	Reserved	N/A	Reserved	No	No
16	IOBASEL	N/A	Reserved	No	No
17	IOBASEU	N/A	Reserved	No	No
18	BSBC	9001h	Burst and Bus Control	Yes	Yes
19	EECAS	0002h	EEPROM Control and Status	Yes	No
20	SWS	0000h	Software Style	Yes	No
21	INTCON	N/A	Reserved	No	No
22	PCILAT	FF06h	PCI Latency	Yes	Yes
23	PCISID	0000h	PCI Subsystem ID	No	Yes
24	PCISVID	0000h	PCI Subsystem Vendor ID	No	Yes
25	SRAMSIZ	0000h	SRAM Size	Yes	Yes
26	SRAMB	0000h	SRAM Boundary	Yes	Yes
27	SRAMIC	0000h	SRAM Interface Control	Yes	Yes
28	EBADDRL	N/A	Expansion Bus Address Lower	Yes	No
29	EBADDRU	N/A	Expansion Bus Address Upper	Yes	No
30	EBD	N/A	Expansion Bus Data Port	Yes	No
31	STVAL	FFFFh	Software Timer Value	Yes	No
32	MIICAS	0000h	MII Control and Status	Yes	Yes
33	MIIADDR	0000h	MII Address	Yes	Yes
34	MIIMDR	N/A	MII Management Data	Yes	No
35	PCIVID	1022h	PCI Vendor ID	No	Yes
36	PMC_A	C811h	PCI Power Management Capabilities (PMC) Alias Register	No	Yes
37	DATA0	0000h	PCI DATA Register Zero Alias Register	No	Yes
38	DATA1	0000h	PCI DATA Register One Alias Register	No	Yes
39	DATA2	0000h	PCI DATA Register Two Alias Register	No	Yes
40	DATA3	0000h	PCI DATA Register Three Alias Register	No	Yes
41	DATA4	0000h	PCI DATA Register Four Alias Register	No	Yes
42	DATA5	0000h	PCI DATA Register Five Alias Register	No	Yes
43	DATA6	0000h	PCI DATA Register Six Alias Register	No	Yes
44	DATA7	0000h	PCI DATA Register Seven Alias Register	No	Yes
45	PMR1	N/A	Pattern Matching Register 1	Yes	No
46	PMR2	N/A	Pattern Matching Register 2	Yes	No
47	PMR3	N/A	Pattern Matching Register 3	Yes	No

BCR0: Master Mode Read Active

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	MSRDA	Reserved locations. After H_RESET, the value in this register will be 0005h. The setting of this register has no effect on any Am79C972 controller function. It is only included for software compatibility with other PCnet family devices.

Read always. MSRDA is read only. Write operations have no effect.

BCR1: Master Mode Write Active

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	MSWRA	Reserved locations. After H_RESET, the value in this register will be 0005h. The setting of this register has no effect on any Am79C972 controller function. It is only included for software compatibility with other PCnet family devices. Read always. MSWRA is read only. Write operations have no effect.

BCR2: Miscellaneous Configuration

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-13	RES	Reserved locations. Written and read as zeros.
12	LEDPE	LED Program Enable. When LEDPE is set to 1, programming of the LED0 (BCR4), LED1 (BCR5), LED2 (BCR6), and LED3 (BCR7) registers is enabled. When LEDPE is cleared to 0, programming of LED0 (BCR4), LED1 (BCR5), LED2 (BCR6), and LED3 (BCR7) registers is disabled. Writes to those registers will be ignored. Read/Write accessible always. LEDPE is cleared to 0 by H_RESET and is unaffected by S_RESET or by setting the STOP bit.
11-9	RES	Reserved locations. Written and read as zeros.
8	APROMWE	Address PROM Write Enable. The Am79C972 controller contains a shadow RAM on board for storage of the first 16 bytes loaded from the serial EEPROM. Accesses to Address PROM I/O Resources will be directed toward this RAM. When APROMWE is set to 1, then write access to the shadow RAM will be enabled. Read/Write accessible always. APROMWE is cleared to 0 by H_RESET and is unaffected by S_RESET or by setting the STOP bit.
7	INTLEVEL	Interrupt Level. This bit allows the interrupt output signals to be programmed for level or edge-sensitive applications. When INTLEVEL is cleared to 0, the $\overline{\text{INTA}}$ pin is configured for level-sensitive applications. In this mode, an interrupt request is signaled by a low level driven on the $\overline{\text{INTA}}$ pin by the Am79C972 controller. When the interrupt is cleared, the $\overline{\text{INTA}}$ pin is tri-stated by the Am79C972 controller and allowed to be pulled to a high level by an external pullup device. This mode is intended for systems which allow the interrupt signal to be shared by multiple devices. When INTLEVEL is set to 1, the $\overline{\text{INTA}}$ pin is configured for edge-sensitive applications. In this mode, an interrupt request is signaled by a high level driven on the $\overline{\text{INTA}}$ pin by the Am79C972 controller. When the interrupt is cleared, the $\overline{\text{INTA}}$ pin is driven to a low level by the Am79C972

controller. This mode is intended for systems that do not allow interrupt channels to be shared by multiple devices.

INTLEVEL should not be set to 1 when the Am79C972 controller is used in a PCI bus application.

Read/Write accessible always. INTLEVEL is cleared to 0 by H_RESET and is unaffected by S_RESET or by setting the STOP bit.

6-4 RES — Reserved locations. Written as zeros and read as undefined.

3 EADISEL — EADI Select. When set to 1, this bit enables the three EADI interface pins that are multiplexed with other functions. EESK/$\overline{\text{LED1}}$ becomes SFBD, EEDO/$\overline{\text{LED3}}$ becomes SRD, and $\overline{\text{LED2}}$ becomes SRDCLK. See the section on *External Address Detection* for more details.

Read/Write accessible always. EADISEL is cleared by H_RESET and is unaffected by S_RESET or by setting the STOP bit.

2 RES — Reserved location. Written and read as zeros.

1 ASEL — Auto Select. When set, the Am79C972 controller will automatically select the operating media interface port. If ASEL has been set to a 1, then when the MIIPD bit (BCR32, bit 14) is 1, the MII port is selected. In addition, if DANAS bit (BCR32, bit 7) is 0, the Am79C972 controller will automatically configure the external PHY connected to the MII port.

If ASEL is set to 0, port selection is controlled by the PORTSEL[1:0] bits, and the Network Port Manager will not automatically configure the external PHY.

The PORTSEL[1:0] bits do not reflect the selected network port when ASEL is 1. Read/Write accessible always. ASEL is set to 1 by H_RESET and is unaffected by S_RESET or STOP. See Table 27.

0 RES — Reserved location. Written and read as zeros.

Table 27. Network Port Configuration

PORTSEL[1:0]	ASEL (BCR2[1])	MII Status (BCR32[14])	Network Port
XX	1	1	MII
10	0	Don't Care	GPSI
11	0	Don't Care	MII

BCR4: LED 0 Status

BCR4 controls the function(s) that the $\overline{\text{LED0}}$ pin displays. Multiple functions can be simultaneously enabled on this LED pin. The LED display will indicate the logical OR of the enabled functions. BCR4 defaults to Link Status (LNKST) with pulse stretcher enabled (PSE = 1) and is fully programmable.

Note: *When LEDPE (BCR2, bit 12) is set to 1, programming of the LED0 Status register is enabled. When LEDPE is cleared to 0, programming of the LED0 register is disabled. Writes to those registers will be ignored.*

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15	LEDOUT	This bit indicates the current (non-stretched) value of the LED output pin. A value of 1 in this bit indicates that the OR of the enabled signals is true. The logical value of the LEDOUT status signal is determined by the settings of the individual Status Enable bits of the LED register (bits 8 and 6-0). Read accessible always. This bit is read only; writes have no effect. LEDOUT is unaffected by H_RESET, S_RESET, or STOP.
14	LEDPOL	LED Polarity. When this bit has the value 0, then the LED pin will be driven to a LOW level whenever the OR of the enabled signals

is true, and the LED pin will be disabled and allowed to float high whenever the OR of the enabled signals is false (i.e., the LED output will be an Open Drain output and the output value will be the inverse of the LEDOUT status bit).

When this bit has the value 1, then the LED pin will be driven to a HIGH level whenever the OR of the enabled signals is true, and the LED pin will be driven to a LOW level whenever the OR of the enabled signals is false (i.e., the LED output will be a Totem Pole output and the output value will be the same polarity as the LEDOUT status bit.).

The setting of this bit will not effect the polarity of the LEDOUT bit for this register.

Read/Write accessible always. LEDPOL is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

13 LEDDIS — LED Disable. This bit is used to disable the LED output. When LEDDIS has the value 1, then the LED output will always be disabled. When LEDDIS has the value 0, then the LED output value will be governed by the LEDOUT and LEDPOL values.

Read/Write accessible always. LEDDIS is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

12 100E — 100 Mbps Enable. When this bit is set to 1, a value of 1 is passed to the LEDOUT bit in this register when the Am79C972 controller is operating at 100 Mbps mode.

Read/Write accessible always. 100E is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

11-10 RES — Reserved locations. Written and read as zeros.

9 MPSE — Magic Packet Status Enable. When this bit is set to 1, a value of 1 is passed to the LEDOUT bit in this register when Magic Packet frame mode is enabled and a Magic Packet frame is detected on the network.

Read/Write accessible always. MPSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

8 FDLSE — Full-Duplex Link Status Enable. Indicates the Full-Duplex Link Test Status. When this bit is set, a value of 1 is passed to the LEDOUT signal when the Am79C972 controller is functioning in a Link Pass state and full-duplex operation is enabled. When the Am79C972 controller is not functioning in a Link Pass state with full-duplex operation being enabled, a value of 0 is passed to the LEDOUT signal.

Read/Write accessible always. FDLSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

7 PSE — Pulse Stretcher Enable. When this bit is set, the LED illumination time is extended for each new occurrence of the enabled function for this LED output. A value of 0 disables the pulse stretcher.

Read/Write accessible always. PSE is set to 1 by H_RESET and is not affected by S_RESET or setting the STOP bit.

6 LNKSE — Link Status Enable. When this bit is set, a value of 1 will be passed to the LEDOUT bit in this register when in Link Pass state.

Read/Write accessible always. LNKSE is set to 1 by H_RESET and is not affected by S_RESET or setting the STOP bit.

5 RCVME — Receive Match Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is receive activity on the network that has

		passed the address match function for this node. All address matching modes are included: physical, logical filtering, broadcast and promiscuous. Read/Write accessible always. RCVME is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
4	XMTE	Transmit Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is transmit activity on the network. Read/Write accessible always. XMTE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
3	RES	Reserved location. Written and read as zeros.
2	RCVE	Receive Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is receive activity on the network. Read/Write accessible always. RCVE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
1	RES	Reserved location. Written and read as zeros.
0	COLE	Collision Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is collision activity on the network. Read/Write accessible always. COLE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

BCR5: LED1 Status

BCR5 controls the function(s) that the $\overline{\text{LED1}}$ pin displays. Multiple functions can be simultaneously enabled on this LED pin. The LED display will indicate the logical OR of the enabled functions. BCR5 defaults to Receive Status (RCV) with pulse stretcher enabled (PSE = 1) and is fully programmable.

Note: *When LEDPE (BCR2, bit 12) is set to 1, programming of the LED1 Status register is enabled. When LEDPE is cleared to 0, programming of the LED1 register is disabled. Writes to those registers will be ignored.*

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15	LEDOUT	This bit indicates the current (non-stretched) value of the LED output pin. A value of 1 in this bit indicates that the OR of the enabled signals is true. The logical value of the LEDOUT status signal is determined by the settings of the individual Status Enable bits of the LED register (bits 8 and 6-0). Read accessible always. This bit is read only, writes have no effect. LEDOUT is unaffected by H_RESET, S_RESET, or STOP.
14	LEDPOL	LED Polarity. When this bit has the value 0, then the LED pin will be driven to a LOW level whenever the OR of the enabled signals is true, and the LED pin will be disabled and allowed to float high whenever the OR of the enabled signals is false (i.e., the LED output will be an Open Drain output and the output value will be the inverse of the LEDOUT status bit). When this bit has the value 1, then the LED pin will be driven to a HIGH level whenever the OR of the enabled signals is true, and the LED pin will be driven to a LOW level whenever the OR of the enabled signals is false (i.e., the LED output will be a Totem Pole output and the output value will be the same polarity as the LEDOUT status bit). The setting of this bit will not effect the polarity of the LEDOUT bit for this register.

Read/Write accessible always. LEDPOL is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

13 LEDDIS — LED Disable. This bit is used to disable the LED output. When LEDDIS has the value 1, then the LED output will always be disabled. When LEDDIS has the value 0, then the LED output value will be governed by the LEDOUT and LEDPOL values.

Read/Write accessible always. LEDDIS is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

12 100E — 100 Mbps Enable. When this bit is set to 1, a value of 1 is passed to the LEDOUT bit in this register when the Am79C972 controller is operating at 100 Mbps mode.

Read/Write accessible always. 100E is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

11-10 RES — Reserved locations. Written and read as zeros.

9 MPSE — Magic Packet Status Enable. When this bit is set to 1, a value of 1 is passed to the LEDOUT bit in this register when Magic Packet mode is enabled and a Magic Packet frame is detected on the network.

Read/Write accessible always. MPSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

8 FDLSE — Full-Duplex Link Status Enable. Indicates the Full-Duplex Link Test Status. When this bit is set, a value of 1 is passed to the LEDOUT signal when the Am79C972 controller is functioning in a Link Pass state and full-duplex operation is enabled. When the Am79C972 controller is not functioning in a Link Pass state with full-duplex operation being enabled, a value of 0 is passed to the LEDOUT signal.

Read/Write accessible always. FDLSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

7 PSE — Pulse Stretcher Enable. When this bit is set, the LED illumination time is extended for each new occurrence of the enabled function for this LED output. A value of 0 disables the pulse stretcher.

Read/Write accessible always. PSE is set to 1 by H_RESET and is not affected by S_RESET or setting the STOP bit.

6 LNKSE — Link Status Enable. When this bit is set, a value of 1 will be passed to the LEDOUT bit in this register in Link Pass state.

Read/Write accessible always. LNKSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

5 RCVME — Receive Match Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is receive activity on the network that has passed the address match function for this node. All address matching modes are included: physical, logical filtering, broadcast, and promiscuous.

Read/Write accessible always. RCVME is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

4 XMTE — Transmit Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is transmit activity on the network.

Read/Write accessible always. XMTE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

3 RES — Reserved location. Written and read as zeros.

2 RCVE — Receive Status Enable. When this bit is set, a value of 1 is

		passed to the LEDOUT bit in this register when there is receive activity on the network. Read/Write accessible always. RCVE is set to 1 by H_RESET and is not affected by S_RESET or setting the STOP bit.
1	RES	Reserved location. Written and read as zeros.
0	COLE	Collision Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is collision activity on the network. Read/Write accessible always. COLE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

BCR6: LED2 Status

BCR6 controls the function(s) that the $\overline{\text{LED2}}$ pin displays. Multiple functions can be simultaneously enabled on this LED pin. The LED display will indicate the logical OR of the enabled functions.

Note: *When LEDPE (BCR2, bit 12) is set to 1, programming of the LED2 Status register is enabled. When LEDPE is cleared to 0, programming of the LED2 register is disabled. Writes to those registers will be ignored.*

Note: *Bits 15-0 in this register are programmable through the EEPROM PREAD operation.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15	LEDOUT	This bit indicates the current (non-stretched) value of the LED output pin. A value of 1 in this bit indicates that the OR of the enabled signals is true. The logical value of the LEDOUT status signal is determined by the settings of the individual Status Enable bits of the LED register (bits 8 and 6-0). Read accessible always. This bit is read only; writes have no effect. LEDOUT is unaffected by H_RESET, S_RESET, or STOP.
14	LEDPOL	LED Polarity. When this bit has the value 0, then the LED pin will be driven to a LOW level whenever the OR of the enabled signals is true, and the LED pin will be disabled and allowed to float high whenever the OR of the enabled signals is false (i.e., the LED output will be an Open Drain output and the output value will be the inverse of the LEDOUT status bit). When this bit has the value 1, then the LED pin will be driven to a HIGH level whenever the OR of the enabled signals is true, and the LED pin will be driven to a LOW level whenever the OR of the enabled signals is false (i.e., the LED output will be a Totem Pole output and the output value will be the same polarity as the LEDOUT status bit). The setting of this bit will not effect the polarity of the LEDOUT bit for this register. Read/Write accessible always. LEDPOL is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
13	LEDDIS	LED Disable. This bit is used to disable the LED output. When LEDDIS has the value 1, then the LED output will always be disabled. When LEDDIS has the value 0, then the LED output value will be governed by the LEDOUT and LEDPOL values. Read/Write accessible always. LEDDIS is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
12	100E	100 Mbps Enable. When this bit is set to 1, a value of 1 is passed to the LEDOUT bit in this register when the Am79C972 controller is operating at 100 Mbps mode. Read/Write accessible always. 100E is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

11-10	RES	Reserved locations. Written and read as zeros.
9	MPSE	Magic Packet Status Enable. When this bit is set to 1, a value of 1 is passed to the LEDOUT bit in this register when Magic Packet frame mode is enabled and a Magic Packet frame is detected on the network. Read/Write accessible always. MPSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
8	FDLSE	Full-Duplex Link Status Enable. Indicates the Full-Duplex Link Test Status. When this bit is set, a value of 1 is passed to the LEDOUT signal when the Am79C972 controller is functioning in a Link Pass state and full-duplex operation is enabled. When the Am79C972 controller is not functioning in a Link Pass state with full-duplex operation being enabled, a value of 0 is passed to the LEDOUT signal. Read/Write accessible always. FDLSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
7	PSE	Pulse Stretcher Enable. When this bit is set, the LED illumination time is extended for each new occurrence of the enabled function for this LED output. A value of 0 disables the pulse stretcher. Read/Write accessible always. PSE is set to 1 by H_RESET and is not affected by S_RESET or setting the STOP bit.
6	LNKSE	Link Status Enable. When this bit is set, a value of 1 will be passed to the LEDOUT bit in this register in Link Pass state. Read/Write accessible always. LNKSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
5	RCVME	Receive Match Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is receive activity on the network that has passed the address match function for this node. All address matching modes are included: physical, logical filtering, broadcast, and promiscuous. Read/Write accessible always. RCVME is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
4	XMTE	Transmit Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is transmit activity on the network. Read/Write accessible always. XMTE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
3	RES	Reserved location. Written and read as zeros.
2	RCVE	Receive Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is receive activity on the network. Read/Write accessible always. RCVE is set to 1 by H_RESET and is not affected by S_RESET or setting the STOP bit.
1	RES	Reserved location. Written and read as zeros.
0	COLE	Collision Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is collision activity on the network. Read/Write accessible always. COLE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

BCR7: LED3 Status

BCR7 controls the function(s) that the $\overline{\text{LED3}}$ pin displays. Multiple functions can be simultaneously enabled on this LED pin. The LED display will indicate the logical OR of the enabled functions. BCR7 defaults to Transmit Status (XMT) with pulse stretcher enabled (PSE = 1) and is fully programmable.

Note: *When LEDPE (BCR2, bit 12) is set to 1, programming of the LED3 Status register is enabled. When LEDPE is cleared to 0, programming of the LED3 register is disabled. Writes to those registers will be ignored.*

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15	LEDOUT	This bit indicates the current (non-stretched) value of the LED output pin. A value of 1 in this bit indicates that the OR of the enabled signals is true. The logical value of the LEDOUT status signal is determined by the settings of the individual Status Enable bits of the LED register (bits 8 and 6-0). Read accessible always. This bit is read only; writes have no effect. LEDOUT is unaffected by H_RESET, S_RESET, or STOP.
14	LEDPOL	LED Polarity. When this bit has the value 0, then the LED pin will be driven to a LOW level whenever the OR of the enabled signals is true, and the LED pin will be disabled and allowed to float high whenever the OR of the enabled signals is false (i.e., the LED output will be an Open Drain output and the output value will be the inverse of the LEDOUT status bit.). When this bit has the value 1, then the LED pin will be driven to a HIGH level whenever the OR of the enabled signals is true, and the LED pin will be driven to a LOW level whenever the OR of the enabled signals is false (i.e., the LED output will be a Totem Pole output and the output value will be the same polarity as the LEDOUT status bit). The setting of this bit will not effect the polarity of the LEDOUT bit for this register. Read/Write accessible always. LEDPOL is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
13	LEDDIS	LED Disable. This bit is used to disable the LED output. When LEDDIS has the value 1, then the LED output will always be disabled. When LEDDIS has the value 0, then the LED output value will be governed by the LEDOUT and LEDPOL values. Read/Write accessible always. LEDDIS is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
12	100E	100 Mbps Enable. When this bit is set to 1, a value of 1 is passed to the LEDOUT bit in this register when the Am79C972 controller is operating at 100 Mbps mode. Read/Write accessible always. 100E is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
11-10	RES	Reserved locations. Written and read as zeros.
9	MPSE	Magic Packet Status Enable. When this bit is set to 1, a value of 1 is passed to the LEDOUT bit in this register when magic frame mode is enabled and a magic frame is detected on the network. Read/Write accessible always. MPSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
8	FDLSE	Full-Duplex Link Status Enable. Indicates the Full-Duplex Link Test Status. When this bit is set, a value of 1 is passed to the LEDOUT signal when the Am79C972 controller is functioning in a Link

		Pass state and full-duplex operation is enabled. When the Am79C972 controller is not functioning in a Link Pass state with full-duplex operation being enabled, a value of 0 is passed to the LEDOUT signal. Read/Write accessible always. FDLSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
7	PSE	Pulse Stretcher Enable. When this bit is set, the LED illumination time is extended for each new occurrence of the enabled function for this LED output. A value of 0 disables the pulse stretcher. Read/Write accessible always. PSE is set to 1 by H_RESET and is not affected by S_RESET or setting the STOP bit.
6	LNKSE	Link Status Enable. When this bit is set, a value of 1 will be passed to the LEDOUT bit in this register in Link Pass state. Read/Write accessible always. LNKSE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
5	RCVME	Receive Match Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is receive activity on the network that has passed the address match function for this node. All address matching modes are included: physical, logical filtering, broadcast, and promiscuous. Read/Write accessible always. RCVME is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
4	XMTE	Transmit Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is transmit activity on the network. Read/Write accessible always. XMTE is set to 1 by H_RESET and is not affected by S_RESET or setting the STOP bit.
3	RES	Reserved location. Written and read as zeros.
2	RCVE	Receive Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is receive activity on the network. Read/Write accessible always. RCVE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
1	RES	Reserved location. Written and read as zeros.
0	COLE	Collision Status Enable. When this bit is set, a value of 1 is passed to the LEDOUT bit in this register when there is collision activity on the network. Read/Write accessible always. COLE is cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

BCR9: Full-Duplex Control

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-3	RES	Reserved locations. Written as zeros and read as undefined.
2	FDRPAD	Full-Duplex Runt Packet Accept Disable. When FDRPAD is set to 1 and full-duplex mode is enabled, the Am79C972 controller will only receive frames that meet the minimum Ethernet frame length of 64 bytes. Receive DMA will not start until at least 64 bytes or a complete frame have been received. By default, FDRPAD is cleared to 0. The Am79C972 controller will accept any length frame and receive DMA will start according to the programming of the receive FIFO watermark. Note that there should not be any

runt packets in a full-duplex network, since the main cause for runt packets is a network collision and there are no collisions in a full-duplex network. This bit needs to be set if in full-duplex mode and external address rejection ($\overline{EAR}$ (BCR9, bit 2)) functionality is desired.

Read/Write accessible always. FDRPAD is cleared by H_RESET and is not affected by S_RESET or by setting the STOP bit.

1 RES — Reserved locations. Written as zeros and read as undefined.

0 FDEN — Full-Duplex Enable. FDEN controls whether full-duplex operation is enabled. When FDEN is cleared and the Auto-Negotiation is disabled, full-duplex operation is not enabled and the Am79C972 controller will always operate in the half-duplex mode. When FDEN is set, the Am79C972 controller will operate in full-duplex mode when the MII port is enabled. ***Do not set this bit when Auto-Negotiation is enabled***.

Read/Write accessible always. FDEN is reset to 0 by H_RESET, and is unaffected by S_RESET and the STOP bit.

BCR16: I/O Base Address Lower

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-5	IOBASEL	Reserved locations. After H_RESET, the value of these bits will be undefined. The settings of these bits will have no effect on any Am79C972 controller function. It is only included for software compatibility with other PCnet family devices. Read/Write accessible always. IOBASEL is not affected by S_RESET or STOP.
4-0	RES	Reserved locations. Written as zeros, read as undefined.

BCR17: I/O Base Address Upper

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	IOBASEU	Reserved locations. After H_RESET, the value in this register will be undefined. The settings of this register will have no effect on any Am79C972 controller function. It is only included for software compatibility with other PCnet family devices. Read/Write accessible always. IOBASEU is not affected by S_RESET or STOP.

BCR18: Burst and Bus Control Register

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-12	ROMTMG	Expansion ROM Timing. The value of ROMTMG is used to tune the timing for all EBDATA (BCR30) accesses to Flash/EPROM as well as all Expansion ROM accesses to Flash/EPROM. ROMTMG, during read operations, defines the time from when the Am79C972 controller drives the lower 8 or 16 bits of the Expansion Bus Address bus to when the Am79C972 controller latches in the data on the 8 or 16 bits of the Expansion Bus Data inputs. ROMTMG, during write operations, defines the time from when the Am79C972 controller drives the lower 8 or 16 bits of the Expansion Bus Data to when the $\overline{EBWE}$ and $\overline{EROMCS}$ deassert. The register value specifies the time in number of clock cycles +1 according to Table 28

.

Table 28. ROMTNG Programming Values

ROMTMG (bits 15-12)	No. of Expansion Bus Cycles
1h<=n <=Fh	n+1

***Note**: Programming ROMTNG with a value of 0 is not permitted.*

The access time for the Expansion ROM or the EBDATA (BCR30) device (tACC) during read operations can be calculated by subtracting the clock to output delay for the EBUA_EBA[7:0] outputs (tv_A_D) and by subtracting the input to clock setup time for the EBD[7:0] inputs (ts_D) from the time defined by ROMTMG:

tACC = ROMTMG * CLK period *CLK_FAC - (tv_A_D) - (ts_D)

The access time for the Expansion ROM or for the EBDATA (BCR30) device (tACC) during write operations can be calculated by subtracting the clock to output delay for the EBUA EBA[7:0] outputs (tv_A_D) and by adding the input to clock setup time for Flash/EPRO inputs (ts_D) from the time defined by ROMTMG.

tACC = ROMTMG * CLK period * CLK_FAC - (tv_A_D) - (ts_D)

For an adapter card application, the value used for clock period should be 30 ns to guarantee correct interface timing at the maximum clock frequency of 33 MHz.

Read accessible always; write accessible only when the STOP bit is set. ROMTMG is set to the value of 1001b by H_RESET and is not affected by S_RESET or STOP. The default value allows using an Expansion ROM with an access time of 250 ns in a system with a maximum clock frequency of 33 MHz.

11 NOUFLO — No Underflow on Transmit. When the NOUFLO bit is set to 1, the Am79C972 controller will not start transmitting the preamble for a packet until the Transmit Start Point (CSR80, bits 10-11) requirement (except when XMTSP = 3h, Full Packet has no meaning when NOUFLO is set to 1) has been met *and* the complete packet has been DMA'd into the Am79C972 controller. The complete packet may reside in any combination of the Bus Transmit FIFO, the SRAM, and the MAC Transmit FIFO, as long as enough of the packet is in the MAC Transmit FIFO to meet the Transmit Start Point requirement. When the NOUFLO bit is cleared to 0, the Transmit Start Point is the only restriction on when preamble transmission begins for transmit packets.

Setting the NOUFLO bit guarantees that the Am79C972 controller will never suffer transmit underflows, because the arbiter that controls transfers to and from the SRAM guarantees a worst case latency on transfers to and from the MAC and Bus Transmit FIFOs such that it will never underflow if the complete packet has been DMA'd into the Am79C972 controller before packet transmission begins.

The NOUFLO bit has no effect when the Am79C972 controller is operating in the NO-SRAM mode.

Read/Write accessible only when either the STOP or the SPND bit is set. NOUFLO is cleared to 0 after H_RESET or S_RESET and is unaffected by STOP.

10 RES — Reserved location. Written as zeros and read as undefined.

9 MEMCMD — Memory Command used for burst read accesses to the transmit buffer. When MEMCMD is set to 0, all burst read accesses to the transmit buffer are of the PCI command type Memory Read Line (type 14). When MEMCMD is set to 1, all burst read accesses to the transmit buffer are of the PCI command type Memory Read Multiple (type 12).

Read accessible always; write accessible only when either the STOP or the SPND bit is set. MEMCMD is cleared by H_RESET and is not affected by S_RESET or STOP.

8 EXTREQ Extended Request. This bit controls the deassertion of $\overline{REQ}$ for a burst transaction. If EXTREQ is set to 0, $\overline{REQ}$ is deasserted at the beginning of a burst transaction. (The Am79C972 controller never performs more than one burst transaction within a single bus mastership period.) In this mode, the Am79C972 controller relies on the PCI latency timer to get enough bus bandwidth, in case the system arbiter also removes $\overline{GNT}$ at the beginning of the burst transaction. If EXTREQ is set to 1, $\overline{REQ}$ stays asserted until the last but one data phase of the burst transaction is done. This mode is useful for systems that implement an arbitration scheme without preemption and require that $\overline{REQ}$ stays asserted throughout the transaction.

EXTREQ should not be set to 1 when the Am79C972 controller is used in a PCI bus application.

Read accessible always, write accessible only when either the STOP or the SPND bit is set. EXTREQ is cleared by H_RESET and is not affected by S_RESET or STOP.

7 DWIO Double Word I/O. When set, this bit indicates that the Am79C972 controller is programmed for DWord I/O (DWIO) mode. When cleared, this bit indicates that the Am79C972 controller is programmed for Word I/O (WIO) mode. This bit affects the I/O Resource Offset map and it affects the defined width of the Am79C972 controllers I/O resources. See the DWIO and WIO sections for more details.

The initial value of the DWIO bit is determined by the programming of the EEPROM.

The value of DWIO can be altered automatically by the Am79C972 controller. Specifically, the Am79C972 controller will set DWIO if it detects a DWord write access to offset 10h from the Am79C972 controller I/O base address (corresponding to the RDP resource).

Once the DWIO bit has been set to a 1, only a H_RESET or an EEPROM read can reset it to a 0. (Note that the EEPROM read operation will only set DWIO to a 0 if the appropriate bit inside of the EEPROM is set to 0.)

Read accessible always. DWIO is read only, write operations have no effect. DWIO is cleared by H_RESET and is not affected S_RESET or by setting the STOP bit.

6 BREADE Burst Read Enable. When set, this bit enables burst mode during memory read accesses. When cleared, this bit prevents the device from performing bursting during read accesses. The Am79C972 controller can perform burst transfers when reading the initialization block, the descriptor ring entries (when SWSTYLE = 3) and the buffer memory.

BREADE should be set to 1 when the Am79C972 controller is used in a PCI bus application to guarantee maximum performance.

Read accessible always; write accessible only when either the STOP or the SPND bit is set. BREADE is cleared by H_RESET and is not affected by S_RESET or STOP.

5 BWRITE Burst Write Enable. When set, this bit enables burst mode during memory write accesses. When cleared, this bit prevents the device from performing bursting during write accesses. The Am79C972 controller can perform burst transfers when writing the descriptor ring entries (when

		SWSTYLE = 3) and the buffer memory. BWRITE should be set to 1 when the Am79C972 controller is used in a PCI bus application to guarantee maximum performance. Read accessible always, write accessible only when either the STOP or the SPND bit is set. BWRITE is cleared by H_RESET and is not affected by S_RESET or STOP.
4-3	TSTSHDW	Reserved locations. Written an read as zeros.
2-0	LINBC	Reserved locations. Read accessible always; write accessible only when either the STOP or the SPND bit is set. After H_RESET, the value in these bits will be 001b. The setting of these bits have no effect on any Am79C972 controller function. LINBC is not affected by S_RESET or STOP.

BCR19: EEPROM Control and Status

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15	PVALID	EEPROM Valid status bit. Read accessible only. PVALID is read only; write operations have no effect. A value of 1 in this bit indicates that a PREAD operation has occurred, and that (1) there is an EEPROM connected to the Am79C972 controller interface pins and (2) the contents read from the EEPROM have passed the checksum verification operation. A value of 0 in this bit indicates a failure in reading the EEPROM. The checksum for the entire 68 bytes of EEPROM is incorrect or no EEPROM is connected to the interface pins. PVALID is set to 0 during H_RESET and is unaffected by S_RESET or the STOP bit. However, following the H_RESET operation, an automatic read of the EEPROM will be performed. Just as is true for the normal PREAD command, at the end of this automatic read operation, the PVALID bit may be set to 1. Therefore, H_RESET will set the PVALID bit to 0 at first, but the automatic EEPROM read operation may later set PVALID to a 1. If PVALID becomes 0 following an EEPROM read operation (either automatically generated after H_RESET, or requested through PREAD), then all EEPROM-programmable BCR locations will be reset to their H_RESET values. The content of the Address PROM locations, however, will not be cleared. If no EEPROM is present at the EESK, EEDI, and EEDO pins, then all attempted PREAD commands will terminate early and PVALID will *not* be set. This applies to the automatic read of the EEPROM after H_RESET, as well as to host-initiated PREAD commands.
14	PREAD	EEPROM Read command bit. When this bit is set to a 1 by the host, the PVALID bit (BCR19, bit 15) will immediately be reset to a 0, and then the Am79C972 controller will perform a read operation of 68 bytes from the EEPROM through the interface. The EEPROM data that is fetched during the read will be stored in the appropriate internal registers on board the Am79C972 controller. Upon completion of the EEPROM read operation, the Am79C972 controller will assert the PVALID bit. EEPROM contents will be indirectly accessible to the host through read accesses to the Address PROM (offsets 0h through Fh) and through read accesses to other EEPROM programmable registers. Note that read accesses from these locations will not actually access the EEPROM itself, but instead will access the Am79C972 controllers internal

copy of the EEPROM contents. Write accesses to these locations may change the Am79C972 controller register contents, but the EEPROM locations will not be affected. EEPROM locations may be accessed directly through BCR19.

At the end of the read operation, the PREAD bit will automatically be reset to a 0 by the Am79C972 controller and PVALID will be set, provided that an EEPROM existed on the interface pins and that the checksum for the entire 68 bytes of EEPROM was correct.

Note that when PREAD is set to a 1, then the Am79C972 controller will no longer respond to any accesses directed toward it, until the PREAD operation has completed successfully. The Am79C972 controller will terminate these accesses with the assertion of $\overline{\text{DEVSEL}}$ and $\overline{\text{STOP}}$ while $\overline{\text{TRDY}}$ is not asserted, signaling to the initiator to disconnect and retry the access at a later time.

If a PREAD command is given to the Am79C972 controller but no EEPROM is attached to the interface pins, the PREAD bit will be cleared to a 0, and the PVALID bit will remain reset with a value of 0. This applies to the automatic read of the EEPROM after H_RESET as well as to host initiated PREAD commands. EEPROM programmable locations on board the Am79C972 controller will be set to their default values by such an aborted PREAD operation. For example, if the aborted PREAD operation immediately followed the H_RESET operation, then the final state of the EEPROM programmable locations will be equal to the H_RESET programming for those locations.

If a PREAD command is given to the Am79C972 controller and the auto-detection pin (EESK/$\overline{\text{LED1}}$/SFBD) indicates that no EEPROM is present, then the EEPROM read operation will still be attempted.

Note that at the end of the H_RESET operation, a read of the EEPROM will be performed automatically. This H_RESET-generated EEPROM read function will not proceed if the auto-detection pin (EESK/$\overline{\text{LED1}}$/SFBD) indicates that no EEPROM is present.

Read accessible always; write accessible only when either the STOP or the SPND bit is set. PREAD is set to 0 during H_RESET and is unaffected by S_RESET or the STOP bit.

13 EEDET

EEPROM Detect. This bit indicates the sampled value of the EESK/$\overline{\text{LED1}}$/SFBD pin at the end of H_RESET. This value indicates whether or not an EEPROM is present at the EEPROM interface. If this bit is a 1, it indicates that an EEPROM is present. If this bit is a 0, it indicates that an EEPROM is not present.

Read accessible only. EEDET is read only; write operations have no effect. The value of this bit is determined at the end of the H_RESET operation. It is unaffected by S_RESET or the STOP bit.

Table 29 indicates the possible combinations of EEDET and the existence of an EEPROM and the resulting operations that are possible on the EEPROM interface.

12-5 RES

Reserved locations. Written as zeros; read as undefined.

4 EEN

EEPROM Port Enable. When this bit is set to a 1, it causes the values of ECS, ESK, and EDI to be driven onto the EECS, EESK, and EEDI pins, respectively. If EEN = 0 and no EEPROM read function is currently active, then EECS will be driven LOW. When

EEN = 0 and no EEPROM read function is currently active, EESK and EEDI pins will be driven by the LED registers BCR5 and BCR4, respectively. See Table 30.

Read accessible always, write accessible only when either the STOP or the SPND bit is set. EEN is set to 0 by H_RESET and is unaffected by the S_RESET or STOP bit.

3 RES — Reserved location. Written as zero and read as undefined.

2 ECS — EEPROM Chip Select. This bit is used to control the value of the EECS pin of the interface when the EEN bit is set to 1 and the PREAD bit is set to 0. If EEN = 1 and PREAD = 0 and ECS is set to a 1, then the EECS pin will be forced to a HIGH level at the rising edge of the next clock following bit programming.

Table 29. EEDET Setting

EEDET Value (BCR19[13])	EEPROM Connected?	Result if PREAD is Set to 1	Result of Automatic EEPROM Read Operation Following H_RESET
0	No	EEPROM read operation is attempted. Entire read sequence will occur, checksum failure will result, PVALID is reset to 0.	First two EESK clock cycles are generated, then EEPROM read operation is aborted and PVALID is reset to 0.
0	Yes	EEPROM read operation is attempted. Entire read sequence will occur, checksum operation will pass, PVALID is set to 1.	First two EESK clock cycles are generated, then EEPROM read operation is aborted and PVALID is reset to 0.
1	No	EEPROM read operation is attempted. Entire read sequence will occur, checksum failure will result, PVALID is reset to 0.	EEPROM read operation is attempted. Entire read sequence will occur, checksum failure will result, PVALID is reset to 0.
1	Yes	EEPROM read operation is attempted. Entire read sequence will occur, checksum operation will pass, PVALID is set to 1.	EEPROM read operation is attempted. Entire read sequence will occur, checksum operation will pass, PVALID is set to 1.

Table 30. Interface Pin Assignment

$\overline{\text{RST}}$ Pin	PREAD or Auto Read in Progress	EEN	EECS	EESK	EEDI
Low	X	X	0	Tri-State	Tri-State
High	1	X	Active	Active	Active
High	0	1	From ECS Bit of BCR19	From ESK Bit of BCR19	From EEDI Bit of BCR19
High	0	0	0	LED1	LED0

If EEN = 1 and PREAD = 0 and ECS is set to a 0, then the EECS pin will be forced to a LOW level at the rising edge of the next clock following bit programming. ECS has no effect on the output value of the EECS pin unless the PREAD bit is set to 0 and the EEN bit is set to 1.

Read accessible always, write accessible only when either the STOP or the SPND bit is set. ECS is set to 0 by H_RESET and is not affected by S_RESET or STOP.

1 ESK — EEPROM Serial Clock. This bit and the EDI/EDO bit are used to control host access to the EEPROM. Values programmed to this bit are placed onto the EESK pin at the rising edge of the next clock following bit programming, except when the PREAD bit is set to 1 or the EEN bit is set to 0. If both the ESK bit and the EDI/EDO bit values are changed during one BCR19 write operation, while EEN = 1, then setup and hold times of the EEDI pin value with respect to the EESK signal edge are not guaranteed.

ESK has no effect on the EESK pin unless the PREAD bit is set to 0 and the EEN bit is set to 1.

Read accessible always, write accessible only when either the STOP or the SPND bit is set. ESK is reset to 1 by H_RESET and is not affected by S_RESET or STOP.

0 EDI/EDO — EEPROM Data In/EEPROM Data Out. Data that is written to this bit will appear on the EEDI output of the interface, except when the PREAD bit is set to 1 or the EEN bit is set to 0. Data that is read from this bit reflects the value of the EEDO input of the interface.

EDI/EDO has no effect on the EEDI pin unless the PREAD bit is set to 0 and the EEN bit is set to 1.

Read accessible always; write accessible only when either the STOP or the SPND bit is set. EDI/EDO is reset to 0 by H_RESET and is not affected by S_RESET or STOP.

BCR20: Software Style

This register is an alias of the location CSR58. Accesses to and from this register are equivalent to accesses to CSR58.

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-11	RES	Reserved locations. Written as zeros and read as undefined.
10	APERREN	Advanced Parity Error Handling Enable. When APERREN is set to 1, the BPE bits (RMD1 and TMD1, bit 23) start having a meaning. BPE will be set in the descriptor associated with the buffer that was accessed when a data parity error occurred. Note that since the advanced parity error handling uses an additional bit in the descriptor, SWSTYLE (bits 7-0 of this register) must be set to 2 or 3 to program the Am79C972 controller to use 32-bit software structures. APERREN does not affect the reporting of address parity errors or data parity errors that occur when the Am79C972 controller is the target of the transfer. Read anytime; write accessible only when either the STOP or the SPND bit is set. APERREN is cleared by H_RESET and is not affected by S_RESET or STOP.
9	RES	Reserved locations. Written as zeros; read as undefined.
8	SSIZE32	Software Size 32 bits. When set, this bit indicates that the Am79C972 controller utilizes 32-bit software structures for the initialization block and the transmit and receive descriptor entries. When cleared, this bit indicates that the Am79C972 controller utilizes 16-bit software structures for the initialization block and the transmit and receive descriptor entries. In this mode, the Am79C972 controller is backwards compatible with the Am7990 LANCE and Am79C960 PCnet-ISA controllers. The value of SSIZE32 is determined by the Am79C972 controller according to the setting of the Software Style (SWSTYLE, bits 7-0 of this register). Read accessible always. SSIZE32 is read only; write operations will be ignored. SSIZE32 will be cleared after H_RESET (since SWSTYLE defaults to 0) and is not affected by S_RESET or STOP. If SSIZE32 is reset, then bits IADR[31:24] of CSR2 will be used to generate values for the upper 8 bits of the 32-bit address bus during master accesses initiated by the Am79C972 controller. This action is required, since the 16-bit software structures specified by the SSIZE32 = 0 setting

will yield only 24 bits of address for Am79C972 controller bus master accesses.

If SSIZE32 is set, then the software structures that are common to the Am79C972 controller and the host system will supply a full 32 bits for each address pointer that is needed by the Am79C972 controller for performing master accesses.

The value of the SSIZE32 bit has no effect on the drive of the upper 8 address bits. The upper 8 address pins are always driven, regardless of the state of the SSIZE32 bit.

Note that the setting of the SSIZE32 bit has no effect on the defined width for I/O resources. I/O resource width is determined by the state of the DWIO bit (BCR18, bit 7).

Bit	Name	Description
7-0	SWSTYLE	Software Style register. The value in this register determines the style of register and memory resources that shall be used by the Am79C972 controller. The Software Style selection will affect the interpretation of a few bits within the CSR space, the order of the descriptor entries and the width of the descriptors and initialization block entries. All Am79C972 controller CSR bits and all descriptor, buffer, and initialization block entries not cited in the Table 31 are unaffected by the Software Style selection and are, therefore, always fully functional as specified in the CSR and BCR sections. Read/Write accessible only when either the STOP or the SPND bit is set. The SWSTYLE register will contain the value 00h following H_RESET and will be unaffected by S_RESET or STOP.

Table 31. Software Styles

SWSTYLE [7:0]	Style Name	SSIZE32	Initialization Block Entries	Descriptor Ring Entries
00h	LANCE/ PCnet-ISA controller	0	16-bit software structures, non-burst or burst access	16-bit software structures, non-burst access only
01h	RES	1	RES	RES
02h	PCnet-PCI controller	1	32-bit software structures, non-burst or burst access	32-bit software structures, non-burst access only
03h	PCnet-PCI controller	1	32-bit software structures, non-burst or burst access	32-bit software structures, non-burst or burst access
All Other	Reserved	Undefined	Undefined	Undefined

BCR22: PCI Latency Register

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-8	MAX_LAT	Maximum Latency. Specifies the maximum arbitration latency the Am79C972 controller can sustain without causing problems to the network activity. The register value specifies the time in units of 1/4 microseconds. MAX_LAT is aliased to the PCI configuration space register MAX_LAT (offset 3Fh). The host will use the value in the register to determine the setting of the Am79C972 Latency Timer register. Read accessible always; write accessible only when either the STOP or the SPND bit is set. MAX_LAT is set to the value of FFh by H_RESET which results in a default maximum latency of 63.75 microseconds. It is recommended to program the value of

		18H via EEPROM. MAX_LAT is not affected by S_RESET or STOP.
7-0	MIN_GNT	Minimum Grant. Specifies the minimum length of a burst period the Am79C972 controller needs to keep up with the network activity. The length of the burst period is calculated assuming a clock rate of 33 MHz. The register value specifies the time in units of 1/4 µs. MIN_GNT is aliased to the PCI configuration space register MIN_GNT (offset 3Eh). The host will use the value in the register to determine the setting of the Am79C972 Latency Timer register. Read accessible always; write accessible only when either the STOP or the SPND bit is set. MIN_GNT is set to the value of 06h by H_RESET which results in a default minimum grant of 1.5 µs, which is the time it takes the Am79C972 controller to read/write half of the FIFO. (16 DWord transfers in burst mode with one extra wait state per data phase inserted by the target.) Note that the default is only a typical value. It also does not take into account any descriptor accesses. It is recommended to program the value of 18H via EEPROM. MIN_GNT is not affected by S_RESET or STOP.

BCR23: PCI Subsystem Vendor ID Register

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-0	RES	Reserved locations. Written as zeros and read as undefined.
15-0	SVID	Subsystem Vendor ID. SVID is used together with SID (BCR24, bits 15-0) to uniquely identify the add-in board or subsystem the Am79C972 controller is used in. Subsystem Vendor IDs can be obtained from the PCI SIG. A value of 0 (the default) indicates that the Am79C972 controller does not support subsystem identification. SVID is aliased to the PCI configuration space register Subsystem Vendor ID (offset 2Ch). Read accessible always. SVID is read only. Write operations are ignored. SVID is cleared to 0 by H_RESET and is not affected by S_RESET or by setting the STOP bit.

BCR24: PCI Subsystem ID Register

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	SID	Subsystem ID. SID is used together with SVID (BCR23, bits 15-0) to uniquely identify the add-in board or subsystem the Am79C972 controller is used in. The value of SID is up to the system vendor. A value of 0 (the default) indicates that the Am79C972 controller does not support subsystem identification. SID is aliased to the PCI configuration space register Subsystem ID (offset 2Eh). Read accessible always. SID is read only. Write operations are ignored. SID is cleared to 0 by H_RESET and is not affected by S_RESET or by setting the STOP bit.

BCR25: SRAM Size Register

Bit	Name	Description

Note: *Bits 7-0 in this register are programmable through the EEPROM.*

31-8 RES — Reserved locations. Written as zeros and read as undefined.

7-0 SRAM_SIZE — SRAM Size. Specifies the upper 8 bits of the 16-bit total size of the SRAM buffer. Each bit in SRAM_SIZE accounts for a 512-byte page. The starting address for the lower 8 bits is assumed to be 00h and the ending address for the lower is assumed to be FFh. Therefore, the maximum address range is the starting address of 0000h to ending address of ((SRAM_SIZE +1) * 256 words) or 17FFh. An SRAM_SIZE value of all zeros specifies that no SRAM will be used and the internal FIFOs will be joined into a contiguous FIFO similar to the PCnet-PCI II controller.

Note*: The minimum allowed number of pages is eight for normal network operation. The Am79C972 controller will not operate correctly with less than the eight pages of memory. When the minimum number of pages is used, these pages must be allocated four each for transmit and receive.*

CAUTION: Programming SRAM_BND and SRAM_SIZE to the same value will cause data corruption except in the case where SRAM_SIZE is 0.

Read accessible always; write accessible only when the STOP bit is set. SRAM_SIZE is set to 000000b during H_RESET and is unaffected by S_RESET or STOP.

BCR26: SRAM Boundary Register

Bit	Name	Description

Note: Bits 7-0 in this register are programmable through the EEPROM.

31-8 RES — Reserved locations. Written as zeros and read as undefined.

7-0 SRAM_BND — SRAM Boundary. Specifies the upper 8 bits of the 16-bit address boundary where the receive buffer begins in the SRAM. The transmit buffer in the SRAM begins at address 0 and ends at the address located just before the address specified by SRAM_BND. Therefore, the receive buffer always begins on a 512 byte boundary. The lower bits are assumed to be zeros. SRAM_BND has no effect in the Low Latency Receive mode.

Note*: The minimum allowed number of pages is four. The Am79C972 controller will not operate correctly with less than four pages of memory per queue. See Table 32 for SRAM_BND programming details.*

Table 32. SRAM_BND Programming

SRAM Addresses	SRAM_BND [7:0]
Minimum SRAM_BND Address	04h
Maximum SRAM_BND Address	13h

CAUTION: Programming SRAM_BND and SRAM_SIZE to the same value will cause data corruption except in the case where SRAM SIZE is 0.

Read accessible always; write accessible only when the STOP bit is set. SRAM_BND is set to 00000000b during H_RESET and is unaffected by S_RESET or STOP.

BCR27: SRAM Interface Control Register

Bit	Name	Description

31-16 RES — Reserved locations. Written as zeros and read as undefined.

15 PTR TST Reserved. Reserved for manufacturing tests. Written as zero and read as undefined.

***Note**: Use of this bit will cause data corruption and erroneous operation.*

Read/Write accessible always. PTR_TST is set to 0 by H_RESET and is unaffected by S_RESET and the STOP bit.

14 LOLATRX Low Latency Receive. When the LOLATRX bit is set to 1, the Am79C972 controller will switch to an architecture applicable to cut-through switches. The Am79C972 controller will assert a receive frame DMA after only 16 bytes of the current receive frame has been received regardless of where the RCVFW (CSR80, bits 13-12) are set. The watermark is a fixed value and cannot be changed. The receive FIFOs will be in NO_SRAM mode while all transmit traffic is buffered through the SRAM. This bit is only valid and the low latency receive only enabled when the SRAM_SIZE (BCR25, bits 7-0) bits are non-zero. SRAM_BND (BCR26, bits 7-0) has no meaning when the Am79C972 controller is in the Low Latency mode. See the section on *SRAM Configuration* for more details.

When the LOLATRX bit is set to 0, the Am79C972 controller will return to a normal receive configuration. The runt packet accept bit (RPA, CSR124, bit 3) must be set when LOLATRX is set.

CAUTION: To provide data integrity when switching into and out of the low latency mode, DO NOT SET the FASTSPNDE (CSR7, bit 15) bit when setting the SPND bit. Receive frames WILL be overwritten and the Am79C972 controller may give erratic behavior when it is enable again. The minimum allowed number of pages is four. The Am79C972 controller will not operate correctly in the LOLATRX mode with less than four pages of memory.

Read/Write accessible only when the STOP bit is set. LOLATRX is cleared to 0 after H_RESET or S_RESET and is unaffected by STOP.

13-6 RES Reserved locations. Written as zeros and read as undefined.

5-3 EBCS Expansion Bus Clock Source. These bits are used to select the source of the fundamental clock to drive the SRAM and Expansion ROM access cycles. Table 33 shows the selected clock source for the various values of EBCS. Note that the actual frequency that the Expansion Bus access cycles run at is a function of both the EBCS and CLK_FAC (BCR27, bits 2-0) bit field settings. When EBCS is set to either the PCI clock or the Time Base clock, no external clock source is required as the clocks are routed internally and the EBCLK pin should be pulled to VDD through a resistor.

Table 33. EBCS Values

EBCS	Expansion Bus Clock Source
000	CLK pin (PCI Clock)
001	Time Base Clock
010	EBCLK pin
011	Reserved
1XX	Reserved

Read accessible always; write accessible only when the STOP bit is set. EBCS is set to 000b (PCI clock selected) during H_RESET and is unaffected by S_RESET or the STOP bit.

***Note**: The clock frequency driving the Expansion Bus access cycles that results from the settings of the EBCS and CLK FAC bits must not exceed 33 MHz at any time. When EBCS is set to either the PCI clock or the Time Base clock, no external clock source is required because the clocks are*

routed internally and the EBCLK pin should be pulled to VDD through a resistor.

CAUTION: Care should be exercised when choosing the PCI clock pin because of the nature of the PCI clock signal. The PCI specification states that the PCI clock can be stopped. If that can occur while it is being used for the Expansion Bus clock data, corruption will result.

CAUTION: The Time Base Clock will not support 100 Mbit operation and should only be selected in 10 Mbit only configurations.

CAUTION: The external clock source used to drive the EBCLK pin must be a continuous clock source at all times.

2-0 CLK_FAC Clock Factor. These bits are used to select whether the clock selected by EBCS is used directly or if it is divided down to give a slower clock for running the Expansion Bus access cycles. The possible factors are given in Table 34.

Table 34. CLK_FAC Values

CLK_FAC	Clock Factor
000	1
001	1/2 (divide by 2)
010	Reserved
011	1/4 (divide by 4)
1XX	Reserved

Read accessible always; write accessible only when the STOP bit is set. CLK_FAC is set to 000b during H_RESET and is unaffected by S_RESET or STOP.

BCR28: Expansion Bus Port Address Lower (Used for Flash/EPROM and SRAM Accesses)

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	EPADDRL	Expansion Port Address Lower. This address is used to provide addresses for the Flash and SRAM port accesses. SRAM accesses are started when a read or write is performed on BCR30 and the FLASH (BCR 29, bit 15) is set to 0. During SRAM accesses only bits in the EPADDRL are valid. Since all SRAM accesses are word oriented only, EPADDRL[0] is the least significant word address bit. On any byte write accesses to the SRAM, the user will have to follow the read-modify-write scheme. On any byte read accesses to the SRAM, the user will have to chose which byte is needed from the complete word returned in BCR30. Flash accesses are started when a read or write is performed on BCR30 and the FLASH (BCR 29, bit 15) is set to 1. During Flash accesses all bits in EPADDR are valid. Read accessible always; write accessible only when the STOP is set or when SRAM SIZE (BCR25, bits 7-0) is 0. EPADDRL is undefined after H_RESET and is unaffected by S_RESET or STOP.

BCR29: Expansion Port Address Upper (Used for Flash/EPROM Accesses)

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15	FLASH	Flash Access. When the FLASH bit is set to 1, the Expansion Bus access will be a Flash cycle. When FLASH is set to 0, the Expansion Bus access will be a SRAM cycle. For a complete description, see the section on *Expansion Bus Accesses*. This bit is only applicable to reads or writes to EBDATA (BCR30). It does not affect Expansion ROM accesses from the PCI system bus.

		Read accessible always; write accessible only when the STOP bit is set. FLASH is 0 after H_RESET and is unaffected by S_RESET or the STOP bit.
14	LAAINC	Lower Address Auto Increment. When the LAAINC bit is set to 1, the Expansion Port Lower Address will automatically increment by one after a read or write access to EBDATA (BCR30). When EBADDRL reaches FFFFh and LAAINC is set to 1, the Expansion Port Lower Address (EPADDRL) will roll over to 0000h. When the LAAINC bit is set to 0, the Expansion Port Lower Address will not be affected in any way after an access to EBDATA (BCR30) and must be programmed. Read accessible always; write accessible only when the STOP bit is set. LAINC is 0 after H_RESET and is unaffected by S_RESET or the STOP bit.
13-4	RES	Reserved locations. Written as zeros and read as undefined.
3-0	EPADDRU	Expansion Port Address Upper. This upper portion of the Expansion Bus address is used to provide addresses for Flash/EPROM port accesses. Read accessible always; write accessible only when the STOP bit is set or when SRAM SIZE (BCR25, bits 7-0) is 0. EPADDRU is undefined after H_RESET and is unaffected by S_RESET or the STOP bit.

BCR30: Expansion Bus Data Port Register

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	EBDATA	Expansion Bus Data Port. EBDATA is the data port for operations on the Expansion Port accesses involving SRAM and Flash accesses. The type of access is set by the FLASH bit (BCR 29, bit 15). When the FLASH bit is set to 1, the Expansion Bus access will follow the Flash access timing. When the FLASH bit is set to 0, the Expansion Bus access will follow the SRAM access timing. ***Note:*** *It is important to set the FLASH bit and load Expansion Port Address EPADDR (BCR28, BCR29) with the required address before attempting read or write to the Expansion Bus data port. The Flash and SRAM accesses use different address phases. Incorrect configuration will result in a possible corruption of data.* Flash read cycles are performed when BCR30 is read and the FLASH bit (BCR29, bit 15) is set to 1. Upon completion of the read cycle, the 8-bit result for Flash access is stored in EBDATA[7:0], EBDATA[15:8] is undefined. Flash write cycles are performed when BCR30 is written and the FLASH bit (BCR29, bit 15) is set to 1. EBDATA[7:0] only is valid for write cycles. SRAM read cycles are performed when BCR30 is read and the FLASH bit (BCR29, bit 15) is set to 0. Upon completion of the read cycle, the 16-bit result for SRAM access is stored in EBDATA. Write cycles to the SRAM are invoked when BCR30 is written and the FLASH bit (BCR29, bit 15) is set to 0. Byte writes to the SRAM must use a read-modify-write scheme since the word is always valid for SRAM write or read accesses. Read and write accessible only when the STOP is set or when SRAM SIZE (BCR25, bits 7-0) is 0. EBDATA is undefined after H_RESET, and is unaffected by S_RESET and the STOP bit.

BCR31: Software Timer Register

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	STVAL	Software Timer Value. STVAL controls the maximum time for the Software Timer to count before generating the STINT (CSR7, bit 11) interrupt. The Software Timer is a free-running timer that is started upon the first write to STVAL. After the first write, the Software Timer will continually count and set the STINT interrupt at the STVAL period. The STVAL value is interpreted as an unsigned number with a resolution of 256 Time Base Clock periods. For instance, a value of 122 ms would be programmed with a value of 9531 (253Bh) if the Time Base Clock is running at 20 MHz. A value of 0 is undefined and will result in erratic behavior. Read and write accessible always. STVAL is set to FFFFh after H_RESET and is unaffected by S_RESET and the STOP bit.

BCR32: MII Control and Status Register

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15	ANTST	Reserved for manufacturing tests. Written as 0 and read as undefined. ***Note****: Use of this bit will cause data corruption and erroneous operation.* Read/Write accessible always. ANTST is set to 0 by H_RESET and is unaffected by S_RESET and the STOP bit.
14	MIIPD	MII PHY Detect. MIIPD reflects the quiescent state of the MDIO pin. MIIPD is continuously updated whenever there is no management operation in progress on the MII interface. When a management operation begins on the interface, the state of MIIPD is preserved until the operation ends, when the quiescent state is again monitored and continuously updates the MIIPD bit. When the MDIO pin is at a quiescent LOW state, MIIPD is cleared to 0. When the MDIO pin is at a quiescent HIGH state, MIIPD is set to 1. MIIPD is used by the automatic port selection logic to select the MII port. When the Auto Select bit (ASEL, BCR2, bit 1) is a 1 and the MIIPD bit is a 1, the MII port is selected. Any transition on the MIIPD bit will set the MIIPDINT bit in CSR7, bit 1. Read accessible always. MIIPD is read only. Write operations are ignored.
13-12	FMDC	Fast Management Data Clock. When FMDC is set to 2h the MII Management Data Clock will run at 10 MHz max. The Management Data Clock will no longer be IEEE 802.3u-compliant and setting this bit should be used with care. The accompanying external PHY must also be able to accept management frames at the new clock rate. When FMDC is set to 1h, the MII Management Data Clock will run at 5 MHz max. The Management Data Clock will no longer be IEEE 802.3u-compliant and setting this bit should be used with care. The accompanying external PHY must also be able to accept management frames at the new clock rate. When FMDC is set to 0h, the MII Management Data Clock will run at 2.5 MHz max and will be fully compliant to IEEE 802.3u standards. See Table 35.

Table 35. FMDC Values

FMDC	Fast Management Data Clock
00	2.5 MHz max
01	5 MHz max
10	10 MHz max
11	Reserved

Read/Write accessible always. FMDC is set to 0 during H_RESET, and is unaffected by S_RESET and the STOP bit

11 APEP MII Auto-Poll External PHY. APEP when set to 1 the Am79C972 controller will poll the MII status register in the external PHY. This feature allows the software driver or upper layers to see any changes in the status of the external PHY. An interrupt when enabled is generated when the contents of the new status is different from the previous status.

Read/Write accessible always. APEP is set to 0 during H_RESET and is unaffected by S_RESET and the STOP bit.

10-8 APDW MII Auto-Poll Dwell Time. APDW determines the dwell time between MII Management Frames accesses when Auto-Poll is turned on. See Table 36.

Table 36. APDW Values

APDW	Auto-Poll™ Dwell Time
000	Continuous (26µs @ 2.5 MHz)
001	Every 128 MDC cycles (103µs @ 2.5 MHz)
010	Every 256 MDC cycles (206µs @ 2.5 MHz)
011	Every 512 MDC cycles (410 µs @ 2.5 MHz)
100	Every 1024 MDC cycles (819 µs @ 2.5 MHz)
101	Every 2048 MDC cycles (1640 µs @ 2.5 MHz)
110-111	Reserved

Read/Write accessible always. APDW is set to 100h after H_RESET and is unaffected by S_RESET and the STOP bit.

7 DANAS Disable Auto-Negotiation Auto Setup. When DANAS is set, the Am79C972 controller after a H_RESET or S_RESET will remain dormant and not automatically startup the Auto-Negotiation section or the enhanced automatic port selection section. Instead, the Am79C972 controller will wait for the software driver to setup the Auto-Negotiation portions of the device. The MII programming in BCR33 and BCR34 is still valid. The Am79C972 controller will not generate any management frames unless Auto-Poll is enabled.

Read/write accessible always. DANAS is set to 0 by H_RESET and is unaffected by S_RESET and the STOP bit.

6 XPHYRST External PHY Reset. When XPHYRST is set, the Am79C972 controller after an H_RESET or S_RESET will issue an MII management frames that will reset the external PHY. This bit is needed when there is no way to guarantee the state of the external PHY. This bit must be reprogrammed after every H_RESET.

Read/Write accessible always. XPHYRST is set to 0 by H_RESET and is unaffected by S_RESET and the STOP bit. XPHYRST is only valid when the internal Network Port Manager is scanning for a network port.

5 XPHYANE External PHY Auto-Negotiation Enable. This bit will force the external PHY into enabling Auto-Negotiation. When set to 0 the Am79C972 controller will send a MII management frame disabling Auto-Negotiation.

Read/Write accessible always. XPHYANE is set to 0 by H_RESET and is unaffected by S_RESET and the STOP bit. XPHYANE is only valid when the internal Network Port Manager is scanning for a network port.

4	XPHYFD	External PHY Full Duplex. When set, this bit will force the external PHY into full duplex when Auto-Negotiation is not enabled. Read/Write accessible always. XPHYFD is set to 0 by H_RESET, and is unaffected by S_RESET and the STOP bit. XPHYFD is only valid when the internal Network Port Manager is scanning for a network port.
3	XPHYSP	External PHY Speed. When set, this bit will force the external PHY into 100 Mbps mode when Auto-Negotiation is not enabled. Read/Write accessible always. XPHYSP is set to 0 by H_RESET, and is unaffected by S_RESET and the STOP bit. XPHYSP is only valid when the internal Network Port Manager is scanning for a network port.
2	RES	Reserved location. Written as zeros and read as undefined.
1	MIIILP	Media Independent Interface Internal Loopback. When set, this bit will cause the internal portion of the MII data port to loopback on itself. The interface is mapped in the following way. The TXD[3:0] nibble data path is looped back onto the RXD[3:0] nibble data path. TX_CLK is looped back as RX_CLK. TX_EN is looped back as RX_DV. CRS is correctly OR'd with TX_EN and RX_DV and always encompasses the transmit frame. TX_ER is looped back as RX_ER. However, TX_ER will not get asserted by the Am79C972 controller to signal an error. The TX_ER function is reserved for future use. Read/Write accessible always. MIIILP is set to 0 by H_RESET and is unaffected by S_RESET and the STOP bit.
0	RES	Reserved location. Written as zeros and read as undefined.

BCR33: MII Address Register

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-10	RES	Reserved locations. Written as zeros and read as undefined.
9-5	PHYAD	MII Management Frame PHY Address. PHYAD contains the 5-bit PHY Address field that is used in the management frame that gets clocked out via the MII management port pins (MDC and MDIO) whenever a read or write transaction occurs to BCR34. The PHY address 1Fh is not valid. The Network Port Manager copies the PHYAD after the Am79C972 controller reads the EEPROM and uses it to communicate with the external PHY. The PHY address must be programmed into the EEPROM prior to starting the Am79C972 controller. Read/Write accessible always. PHYAD is undefined after H_RESET and is unaffected by S_RESET and the STOP bit.
4-0	REGAD	MII Management Frame Register Address. REGAD contains the 5-bit Register Address field that is used in the management frame that gets clocked out via the MII management port pins (MDC and MDIO) whenever a read or write transaction occurs to BCR34. Read/Write accessible always. REGAD is undefined after H_RESET and is unaffected by S_RESET and the STOP bit.

BCR34: MII Management Data Register

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	MIIMD	MII Management Data. MIIMD is the data port for operations on the MII management interface (MDIO and MDC). The Am79C972 de-

vice builds management frames using the PHYAD and REGAD values from BCR33. The operation code used in each frame is based upon whether a read or write operation has been performed to BCR34. Read cycles on the MII management interface are invoked when BCR34 is read. Upon completion of the read cycle, the 16-bit result of the read operation is stored in MIIMD. Write cycles on the MII management interface are invoked when BCR34 is written. The value written to MIIMD is the value used in the data field of the management write frame.

Read/Write accessible always. MIIMD is undefined after H_RESET and is unaffected by S_RESET and the STOP bit.

BCR35: PCI Vendor ID Register

Note: *Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-0	VID	Vendor ID. The PCI Vendor ID register is a 16-bit register that identifies the manufacturer of the Am79C972 controller. AMD's Vendor ID is 1022h. Note that this Vendor ID is not the same as the Manufacturer ID in CSR88 and CSR89. The Vendor ID is assigned by the PCI Special Interest Group. The Vendor ID is not normally programmable, but the Am79C972 controller allows this due to legacy operating systems that do not look at the PCI Subsystem Vendor ID and the Vendor ID to uniquely identify the add-in board or subsystem that the Am79C972 controller is used in. ***Note: If the operating system or the network operating system supports PCI Subsystem Vendor ID and Subsystem ID, use those to identify the add-in board or subsystem and program the VID with the default value of 1022h***. VID is aliased to the PCI configuration space register Vendor ID (offset 00h). Read accessible always. VID is read only. Write operations are ignored. VID is set to 1022h by H_RESET and is not affected by S_RESET or by setting the STOP bit.

BCR36: PCI Power Management Capabilities (PMC) Alias Register

Note: *This register is an alias of the PMC register located at offset 42h of the PCI Configuration Space. Since PMC register is read only, BCR36 provides a means of programming it through the EEPROM. The contents of this register are copied into the PMC register. For the definition of the bits in this register, refer to the PMC register definition. Bits 15-0 in this register are programmable through the EEPROM. Read accessible always. Read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.*

BCR37: PCI DATA Register Zero (DATA0) Alias Register

Note: *This register is an alias of the DATA register and also of the DATA_SCALE field of the PMCSR register. Since these two are read only, BCR37 provides a means of programming them indirectly. The contents of this register are copied into the corresponding fields pointed with the DATA_SEL field set to zero. Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
15-10	RES	Reserved locations. Written as zeros and read as undefined.
9-8	D0_SCALE	These bits correspond to the DATA_SCALE field of the PMCSR (offset Register 44 of the PCI configuration space, bits 14-13). Refer to the description of DATA_SCALE for the meaning of this field. Read accessible always. D0_SCALE is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

7-0	DATA0	These bits correspond to the PCI DATA register (offset Register 47 of the PCI configuration space, bits 7-0). Refer to the description of DATA register for the meaning of this field. Read accessible always. DATA0 is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit

BCR38: PCI DATA Register One (DATA1) Alias Register

Note: *This register is an alias of the DATA register and also of the DATA_SCALE field of the PMCSR register. Since these two are read only, BCR38 provides a means of programming them through the EEPROM. The contents of this register are copied into the corresponding fields pointed with the DATA_SEL field set to one. Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
15-10	RES	Reserved locations. Written as zeros and read as undefined.
9-8	D1_SCALE	These bits correspond to the DATA_SCALE field of the PMCSR (offset Register 44 of the PCI configuration space, bits 14-13). Refer to the description of DATA_SCALE for the meaning of this field. Read accessible always. D1_SCALE is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
7-0	DATA1	These bits correspond to the PCI DATA register (offset Register 47 of the PCI configuration space, bits 7-0). Refer to the description of DATA register for the meaning of this field. Read accessible always. DATA1 is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

BCR39: PCI DATA Register Two (DATA2) Alias Register

Note: *This register is an alias of the DATA register and also of the DATA_SCALE field of the PMCSR register. Since these two are read only, BCR39 provides a means of programming them through the EEPROM. The contents of this register are copied into the corresponding fields pointed with the DATA_SEL field set to two. Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
15-10	RES	Reserved locations. Written as zeros and read as undefined.
9-8	D2_SCALE	These bits correspond to the DATA_SCALE field of the PMCSR (offset Register 44 of the PCI configuration space, bits 14-13). Refer to the description of DATA_SCALE for the meaning of this field. Read accessible always. D2_SCALE is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
7-0	DATA2	These bits correspond to the PCI DATA register (offset Register 47 of the PCI configuration space, bits 7-0). Refer to the description of DATA register for the meaning of this field. Read accessible always. DATA2 is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit

BCR40: PCI DATA Register Three (DATA3) Alias Register

Note: *This register is an alias of the DATA register and also of the DATA_SCALE field of the PMCSR register. Since these two are read only, BCR40 provides a means of programming them through the EEPROM. The contents of this register are copied into the corresponding fields pointed with the DATA_SEL field set to three. Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
15-10	RES	Reserved locations. Written as zeros and read as undefined.

9-8	D3_SCALE	These bits correspond to the DATA_SCALE field of the PMCSR (offset Register 44 of the PCI configuration space, bits 14-13). Refer to the description of DATA_SCALE for the meaning of this field. Read accessible always. D3_SCALE is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
7-0	DATA3	These bits correspond to the PCI DATA register (offset Register 47 of the PCI configuration space, bits 7-0). Refer to the description of DATA register for the meaning of this field. Read accessible always. DATA3 is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

BCR41: PCI DATA Register Four (DATA4) Alias Register

Note: *This register is an alias of the DATA register and also of the DATA_SCALE field of the PMCSR register. Since these two are read only, BCR41 provides a means of programming them through the EEPROM. The contents of this register are copied into the corresponding fields pointed with the DATA_SEL field set to four. Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
15-10	RES	Reserved locations. Written as zeros and read as undefined.
9-8	D4_SCALE	These bits correspond to the DATA_SCALE field of the PMCSR (offset register 44 of the PCI configuration space, bits 14-13). Refer to the description of DATA_SCALE for the meaning of this field. Read accessible always. D4_SCALE is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit
7-0	DATA4	These bits correspond to the PCI DATA register (offset Register 47 of the PCI configuration space, bits 7-0). Refer to the description of DATA register for the meaning of this field. Read accessible always. DATA4 is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

BCR42: PCI DATA Register Five (DATA5) Alias Register

Note: *This register is an alias of the DATA register and also of the DATA_SCALE field of the PMCSR register. Since these two are read only, BCR42 provides a means of programming them through the EEPROM. The contents of this register are copied into the corresponding fields pointed with the DATA_SEL field set to five. Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
15-10	RES	Reserved locations. Written as zeros and read as undefined.
9-8	D5_SCALE	These bits correspond to the DATA_SCALE field of the PMCSR (offset Register 44 of the PCI configuration space, bits 14-13). Refer to the description of DATA_SCALE for the meaning of this field. Read accessible always. D5_SCALE is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit
7-0	DATA5	These bits correspond to the PCI DATA register (offset Register 47 of the PCI configuration space, bits 7-0). Refer to the description of DATA register for the meaning of this field. Read accessible always. DATA5 is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

BCR43: PCI DATA Register Six (DATA6) Alias Register

Note: *This register is an alias of the DATA register and also of the DATA_SCALE field of the PMCSR register. Since these two are read only, BCR43 provides a means of programming them through the EEPROM. The contents of this register are copied into the corresponding fields pointed with the DATA_SEL field set to six. Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
15-10	RES	Reserved locations. Written as zeros and read as undefined.
9-8	D6_SCALE	These bits correspond to the DATA_SCALE field of the PMC-SR (offset Register 44 of the PCI configuration space, bits 14-13). Refer to the description of DATA_SCALE for the meaning of this field. Read accessible always. D6_SCALE is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit
7-0	DATA6	These bits correspond to the PCI DATA register (offset Register 47 of the PCI configuration space, bits 7-0). Refer to the description of DATA register for the meaning of this field. Read accessible always. DATA6 is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

BCR44: PCI DATA Register Seven (DATA7) Alias Register

Note: *This register is an alias of the DATA register and also of the DATA_SCALE field of the PMCSR register. Since these two are read only, BCR44 provides a means of programming them through the EEPROM. The contents of this register are copied into the corresponding fields pointed with the DATA_SEL field set to seven. Bits 15-0 in this register are programmable through the EEPROM.*

Bit	Name	Description
15-10	RES	Reserved locations. Written as zeros and read as undefined.
9-8	D7_SCALE	These bits correspond to the DATA_SCALE field of the PMC-SR (offset Register 44 of the PCI configuration space, bits 14-13). Refer to the description of DATA_SCALE for the meaning of this field. Read accessible always. D7_SCALE is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.
7-0	DATA7	These bits correspond to the PCI DATA register (offset register 47 of the PCI configuration space, bits 7-0). Refer to the description of DATA register for the meaning of this field. Read accessible always. DATA7 is read only. Cleared by H_RESET and is not affected by S_RESET or setting the STOP bit.

BCR45: OnNow Pattern Matching Register 1

Note: *This register is used to control and indirectly access the Pattern Match RAM (PMR). When BCR45 is written and the PMAT_MODE bit (bit 7) is 1, Pattern Match logic is enabled. No bus accesses into PMR are possible, and BCR46, BCR47, and all other bits in BCR45 are ignored. When PMAT_MODE is set, a read of BCR45, BCR46, or BCR47 returns all undefined bits except for PMAT_MODE.*

When BCR45 is written and the PMAT_MODE bit is 0, the Pattern Match logic is disabled and accesses to the PMR are possible. Bits 6-0 of BCR45 specify the address of the PMR word to be accessed. Following the write to BCR45, the PMR word may be read by reading BCR45, BCR46 and BCR47 in any order. To write to PMR word, the write to BCR45 must be followed by a write to BCR46 and a write to BCR47 in that order to complete the operation. The RAM will not actually be written until the write to BCR47 is complete. The write to BCR47 causes all 5 bytes (four bytes of BCR46-47 and the upper byte of the BCR45) to be written to whatever PMR word is addressed by bits 6:0 of BCR45.

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-8	PMR_B0	Pattern Match RAM Byte 0. This byte is written into or read from Byte 0 of the Pattern Match RAM

Read and write accessible always. PMR_B0 is undefined after H_RESET, and is unaffected by S_RESET and the STOP bit.

7 PMAT_MODE Pattern Match Mode. Writing a 1 to this bit will enable Pattern Match Mode and should only be done after the Pattern Match RAM has been programmed.

Read and write accessible always. PMAT_MODE is reset to 0 after H_RESET, and is unaffected by S_RESET and the STOP bit.

6-0 PMR_ADDR Pattern Match Ram Address. These bits are the Pattern Match Ram address to be written to or read from.

Read and write accessible always. PMR_ADDR is reset to 0 after H_RESET, and is unaffected by S_RESET and the STOP bit.

BCR46: OnNow Pattern Matching Register 2

Note: *This register is used to control and indirectly access the Pattern Match RAM (PMR). When BCR45 is written and the PMAT_MODE bit (bit 7) is 1, Pattern Match logic is enabled. No bus accesses into PMR are possible, and BCR46, BCR47, and all other bits in BCR45 are ignored. When PMAT_MODE is set, a read of BCR45, BCR46, or BCR47 returns all undefined bits except for PMAT_MODE.*

When BCR45 is written and the PMAT_MODE bit is 0, the Pattern Match logic is disabled and accesses to the PMR are possible. Bits 6-0 of BCR45 specify the address of the PMR word to be accessed. Following the write to BCR45, the PMR word may be read by reading BCR45, BCR46 and BCR47 in any order. To write to PMR word, the write to BCR45 must be followed by a write to BCR46 and a write to BCR47 in that order to complete the operation. The RAM will not actually be written until the write to BCR47 is complete. The write to BCR47 causes all 5 bytes (four bytes of BCR46-47 and the upper byte of the BCR45) to be written to whatever PMR word is addressed by bits 6:0 of BCR45.

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-8	PMR_B2	Pattern Match RAM Byte 2. This byte is written into or read from Byte 2 of the Pattern Match RAM. Read and write accessible always. PMR_B2 is undefined after H_RESET, and is unaffected by S_RESET and the STOP bit.
7-0	PMR_B1	Pattern Match RAM Byte 1. This byte is written into or read from Byte 1 of Pattern Match RAM. Read and write accessible always. PMR_B1 is undefined after H_RESET, and is unaffected by S_RESET and the STOP bit.

BCR47: OnNow Pattern Matching Register 3

Note: *This register is used to control and indirectly access the Pattern Match RAM (PMR). When BCR45 is written and the PMAT_MODE bit (bit 7) is 1, Pattern Match logic is enabled. No bus accesses into PMR are possible, and BCR46, BCR47, and all other bits in BCR45 are ignored. When PMAT_MODE is set, a read of BCR45, BCR46, or BCR47 returns all undefined bits except for PMAT_MODE.*

When BCR45 is written and the PMAT_MODE bit is 0, the Pattern Match logic is disabled and accesses to the PMR are possible. Bits 6-0 of BCR45 specify the address of the PMR word to be accessed. Following the write to BCR45, the PMR word may be read by reading BCR45, BCR46 and BCR47 in any order. To write to PMR word, the write to BCR45 must be followed by a write to BCR46 and a write to BCR47 in that order to complete the operation. The RAM will not actually be written until the write to BCR47 is complete. The write to BCR47 causes all 5 bytes (four bytes of BCR46-47 and the upper byte of the BCR45) to be written to whatever PMR word is addressed by bits 6:0 of BCR45.

When PMAT_MODE is 0, the contents of the word addressed by bits 6:0 of BCR45 can be read by reading BCR45-47 in any order.

Bit	Name	Description
31-16	RES	Reserved locations. Written as zeros and read as undefined.
15-8	PMR_B4	Pattern Match RAM Byte 4. This byte is written into or read from Byte 4 of Pattern Match RAM. Read and write accessible always. PMR_B4 is undefined after H_RESET, and is unaffected by S_RESET and the STOP bit.

7-0	PMR_B3	Pattern Match RAM Byte 3. This byte is written into or read from Byte 3 of Pattern Match RAM. Read and write accessible always. PMR_B3 is undefined after H_RESET, and is unaffected by S_RESET and the STOP bit.

Initialization Block

Note: When SSIZE32 (BCR20, bit 8) is set to 0, the software structures are defined to be 16 bits wide. The base address of the initialization block must be aligned to a DWord boundary, i.e., CSR1, bit 1 and 0 must be cleared to 0. When SSIZE32 is set to 0, the initialization block looks like Table 37.

Note: *The Am79C972 controller performs DWord accesses to read the initialization block. This statement is always true, regardless of the setting of the SSIZE32 bit.*

When SSIZE32 (BCR20, bit 8) is set to 1, the software structures are defined to be 32 bits wide. The base address of the initialization block must be aligned to a DWord boundary, i.e., CSR1, bits 1 and 0 must be cleared to 0. When SSIZE32 is set to 1, the initialization block looks like Table 38.

Table 37. Initialization Block (SSIZE32 = 0)

Address	Bits 15-13	Bit 12	Bits 11-8	Bits 7-4	Bits 3-0
IADR+00h	MODE 15-00				
IADR+02h	PADR 15-00				
IADR+04h	PADR 31-16				
IADR+06h	PADR 47-32				
IADR+08h	LADRF 15-00				
IADR+0Ah	LADRF 31-16				
IADR+0Ch	LADRF 47-32				
IADR+0Eh	LADRF 63-48				
IADR+10h	RDRA 15-00				
IADR+12h	RLEN	0	RES	RDRA 23-16	
IADR+14h	TDRA 15-00				
IADR+16h	TLEN	0	RES	TDRA 23-16	

Table 38. Initialization Block (SSIZE32 = 1)

Address	Bits 31-28	Bits 27-24	Bits 23-20	Bits 19-16	Bits 15-12	Bits 11-8	Bits 7-4	Bits 3-0
IADR+00h	TLEN	RES	RLEN	RES	MODE			
IADR+04h	PADR 31-00							
IADR+08h	RES				PADR 47-32			
IADR+0Ch	LADRF 31-00							
IADR+10h	LADRF 63-32							
IADR+14h	RDRA 31-00							
IADR+18h	TDRA 31-00							

RLEN and TLEN

When SSIZE32 (BCR20, bit 8) is set to 0, the software structures are defined to be 16 bits wide, and the RLEN and TLEN fields in the initialization block are each three bits wide. The values in these fields determine the number of transmit and receive Descriptor Ring Entries (DRE) which are used in the descriptor rings. Their meaning is shown in Table 39. If a value other than those listed in Table 39 is desired, CSR76 and CSR78 can be written after initialization is complete.

When SSIZE32 (BCR20, bit 8) is set to 1, the software structures are defined to be 32 bits wide, and the RLEN and TLEN fields in the initialization block are each 4 bits wide. The values in these fields determine the number

of transmit and receive Descriptor Ring Entries (DRE) which are used in the descriptor rings. Their meaning is shown in Table 40.

If a value other than those listed in Table 40 is desired, CSR76 and CSR78 can be written after initialization is complete.

Table 39. R/TLEN Decoding (SSIZE32 = 0)

R/TLEN	Number of DREs
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

RDRA and TDRA

RDRA and TDRA indicate where the transmit and receive descriptor rings begin. Each DRE must be located at a 16-byte address boundary when SSIZE32 is set to 1 (BCR20, bit 8). Each DRE must be located at an 8-byte address boundary when SSIZE32 is set to 0 (BCR20, bit 8).

Table 40. R/TLEN Decoding (SSIZE32 = 1)

R/TLEN	Number of DREs
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
11XX	512
1X1X	512

LADRF

The Logical Address Filter (LADRF) is a 64-bit mask that is used to accept incoming Logical Addresses. If the first bit in the incoming address (as transmitted on the wire) is a 1, it indicates a logical address. If the first bit is a 0, it is a physical address and is compared against the physical address that was loaded through the initialization block.

A logical address is passed through the CRC generator, producing a 32-bit result. The high order 6 bits of the CRC is used to select one of the 64 bit positions in the Logical Address Filter. If the selected filter bit is set, the address is accepted and the frame is placed into memory.

The Logical Address Filter is used in multicast addressing schemes. The acceptance of the incoming frame based on the filter value indicates that the message may be intended for the node. It is the node's responsibility to determine if the message is actually intended for the node by comparing the destination address of the stored message with a list of acceptable logical addresses.

If the Logical Address Filter is loaded with all zeros and promiscuous mode is disabled, all incoming logical addresses except broadcast will be rejected. If the DRCVBC bit (CSR15, bit 14) is set as well, the broadcast packets will be rejected. See Figure 52.

PADR

This 48-bit value represents the unique node address assigned by the ISO 8802-3 (IEEE/ANSI 802.3) and used for internal address comparison. PADR[0] is compared with the first bit in the destination address of the incoming frame. It must be 0 since only the destination address of a unicast frames is compared to PADR. The six hex-digit nomenclature used by the ISO 8802-3 (IEEE/ANSI 802.3) maps to the Am79C972 PADR register as follows: the first byte is compared with PADR[7:0], with PADR[0] being the least significant bit of the byte. The second ISO 8802-3 (IEEE/ANSI 802.3) byte is compared with PADR[15:8], again from the least significant bit to the most significant bit, and so on. The sixth byte is compared with PADR[47:40], the least significant bit being PADR[40].

Mode

The mode register field of the initialization block is copied into CSR15 and interpreted according to the description of CSR15.

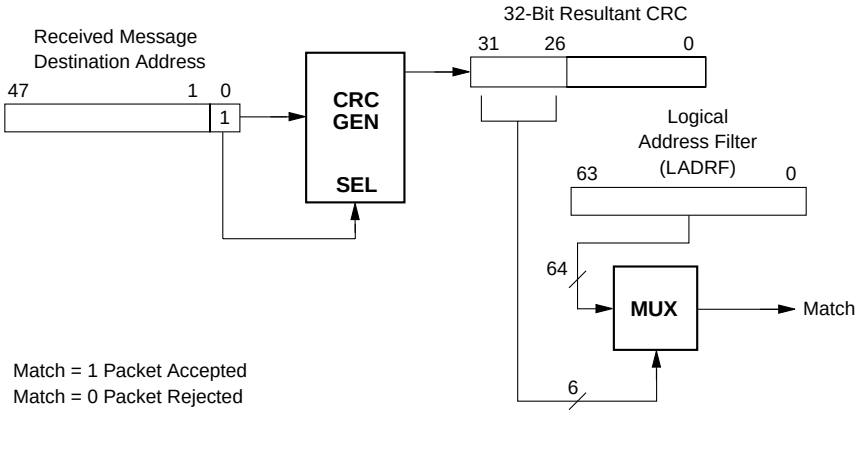

Figure 52. Address Match Logic

Receive Descriptors

When SWSTYLE (BCR20, bits 7-0) is set to 0, then the software structures are defined to be 16 bits wide, and receive descriptors look like Table 41 (CRDA = Current Receive Descriptor Address).

When SWSTYLE (BCR 20, bits 7-0) is set to 2, then the software structures are defined to be 32 bits wide, and receive descriptors look like Table 42 (CRDA = Current Receive Descriptor Address).

When SWSTYLE (BCR 20, bits 7-0) is set to 3, then the software structures are defined to be 32 bits wide, and receive descriptors look like Table 43 (CRDA = Current Receive Descriptor Address).

Table 41. Receive Descriptor (SWSTYLE = 0)

Address	15	14	13	12	11	10	9	8	7-0
CRDA+00h	RBADR[15:0]								
CRDA+02h	OWN	ERR	FRAM	OFLO	CRC	BUFF	STP	ENP	RBADR[23:16]
CRDA+04h	1	1	1	1	BCNT				
CRDA+06h	0	0	0	0	MCNT				

Table 42. Receive Descriptor (SWSTYLE = 2)

Address	31	30	29	28	27	26	25	24	23	22	21	20	19-16	15-12	11-0
CRDA+00h	RBADR[31:0]														
CRDA+04h	OWN	ERR	FRAM	OFLO	CRC	BUFF	STP	ENP	BPE	PAM	LAFM	BAM	RES	1111	BCNT
CRDA+08h	RES	RFRTAG[14:0]												0000	MCNT
CRDA+0Ch	USER SPACE														

Table 43. Receive Descriptor (SWSTYLE = 3)

Address	31	30	29	28	27	26	25	24	23	22	21	20	19-16	15-12	11-0
CRDA+00h	RES	RFRTAG[14:0]												0000	MCNT
CRDA+04h	OWN	ERR	FRAM	OFLO	CRC	BUFF	STP	ENP	BPE	PAM	LAFM	BAM	RES	1111	BCNT
CRDA+08h	RBADR[31:0]														
CRDA+0Ch	USER SPACE														

RMD0

Bit	Name	Description
31-0	RBADR	Receive Buffer address. This field contains the address of the receive buffer that is associated with this descriptor.

RMD1

Bit	Name	Description
31	OWN	This bit indicates whether the descriptor entry is owned by the host (OWN = 0) or by the Am79C972 controller (OWN = 1). The Am79C972 controller clears the OWN bit after filling the buffer that the descriptor points to. The host sets the OWN bit after emptying the buffer. Once the Am79C972 controller or host has relinquished ownership of a buffer, it must not change any field in the descriptor entry.
30	ERR	ERR is the OR of FRAM, OFLO, CRC, BUFF, or BPE. ERR is set by the Am79C972 controller and cleared by the host.
29	FRAM	Framing error indicates that the incoming frame contains a non-integer multiple of eight bits and there was an FCS error. If there was no FCS error on the incoming frame, then FRAM will not be set even if there was a non-integer multiple of eight bits in the frame. FRAM is not valid in internal loopback mode. FRAM is valid only when ENP is set and OFLO is not. FRAM is set by the Am79C972 controller and cleared by the host.
28	OFLO	Overflow error indicates that the receiver has lost all or part of the incoming frame, due to an inability to move data from the receive FIFO into a memory buffer before the internal FIFO overflowed. OFLO is set by the Am79C972 controller and cleared by the host.
27	CRC	CRC indicates that the receiver has detected a CRC (FCS) error on the incoming frame. CRC is valid only when ENP is set and OFLO is not. CRC is set by the Am79C972 controller and cleared by the host. CRC will also be set when Am79C972 receives an RX_ER indication from the external PHY through the MII.
26	BUFF	Buffer error is set any time the Am79C972 controller does not own the next buffer while data chaining a received frame. This can occur in either of two ways: 1. The OWN bit of the next buffer is 0. 2. FIFO overflow occurred before the Am79C972 controller was able to read the OWN bit of the next descriptor. If a Buffer Error occurs, an Overflow Error may also occur internally in the FIFO, but will not be reported in the descriptor status entry unless both BUFF and OFLO errors occur at the same time. BUFF is set by the Am79C972 controller and cleared by the host.
25	STP	Start of Packet indicates that this is the first buffer used by the Am79C972 controller for this frame. If STP and ENP are both set to 1, the frame fits into a single buffer. Otherwise, the frame is spread over more than one buffer. When LAPPEN (CSR3, bit 5) is cleared to 0, STP is set by the Am79C972 controller and cleared by the host. When LAPPEN is set to 1, STP must be set by the host.
24	ENP	End of Packet indicates that this is the last buffer used by the Am79C972 controller for this frame. It is used for data chaining buffers. If both STP and ENP are set, the frame fits into one buffer and there is no data chaining. ENP is set by the Am79C972 controller and cleared by the host.

23	BPE	Bus Parity Error is set by the Am79C972 controller when a parity error occurred on the bus interface during data transfers to a receive buffer. BPE is valid only when ENP, OFLO, or BUFF are set. The Am79C972 controller will only set BPE when the advanced parity error handling is enabled by setting APERREN (BCR20, bit 10) to 1. BPE is set by the Am79C972 controller and cleared by the host. This bit does not exist when the Am79C972 controller is programmed to use 16-bit software structures for the descriptor ring entries (BCR20, bits 7-0, SWSTYLE is cleared to 0).
22	PAM	Physical Address Match is set by the Am79C972 controller when it accepts the received frame due to a match of the frame's destination address with the content of the physical address register. PAM is valid only when ENP is set. PAM is set by the Am79C972 controller and cleared by the host. This bit does not exist when the Am79C972 controller is programmed to use 16-bit software structures for the descriptor ring entries (BCR20, bits 7-0, SWSTYLE is cleared to 0).
21	LAFM	Logical Address Filter Match is set by the Am79C972 controller when it accepts the received frame based on the value in the logical address filter register. LAFM is valid only when ENP is set. LAFM is set by the Am79C972 controller and cleared by the host. Note that if DRCVBC (CSR15, bit 14) is cleared to 0, only BAM, but not LAFM will be set when a Broadcast frame is received, even if the Logical Address Filter is programmed in such a way that a Broadcast frame would pass the hash filter. If DRCVBC is set to 1 and the Logical Address Filter is programmed in such a way that a Broadcast frame would pass the hash filter, LAFM will be set on the reception of a Broadcast frame. This bit does not exist when the Am79C972 controller is programmed to use 16-bit software structures for the descriptor ring entries (BCR20, bits 7-0, SWSTYLE is cleared to 0).
20	BAM	Broadcast Address Match is set by the Am79C972 controller when it accepts the received frame, because the frame's destination address is of the type 'Broadcast.' BAM is valid only when ENP is set. BAM is set by the Am79C972 controller and cleared by the host. This bit does not exist when the Am79C972 controller is programmed to use 16-bit software structures for the descriptor ring entries (BCR20, bits 7-0, SWSTYLE is cleared to 0).
19-16	RES	Reserved locations. These locations should be read and written as zeros.
15-12	ONES	These four bits must be written as ones. They are written by the host and unchanged by the Am79C972 controller.
11-0	BCNT	Buffer Byte Count is the length of the buffer pointed to by this descriptor, expressed as the two's complement of the length of the buffer. This field is written by the host and unchanged by the Am79C972 controller.

RMD2

Bit	Name	Description
31	ZERO	This field is reserved. The Am79C972 controller will write a zero to this location.

30-16 RFRTAG — Receive Frame Tag. Indicates the Receive Frame Tag applied from the EADI interface. This field is user defined and has a default value of all zeros. When RX-FRTG (CSR7, bit 14) is set to 0, RFRTAG will be read as all zeros. See the section on *Receive Frame Tagging* for details.

15-12 ZEROS — This field is reserved. Am79C972 controller will write zeros to these locations.

11-0 MCNT — Message Byte Count is the length in bytes of the received message, expressed as an unsigned binary integer. MCNT is valid only when ERR is clear and ENP is set. MCNT is written by the Am79C972 controller and cleared by the host. ***Note***: *This is a 13-bit internal counter.*

RMD3

Bit	Name	Description
31-0	US	User Space. Reserved for user defined space.

Transmit Descriptors

When SWSTYLE (BCR20, bits 7-0) is set to 0, the software structures are defined to be 16 bits wide, and transmit descriptors look like Table 44 (CXDA = Current Transmit Descriptor Address).

When SWSTYLE (BCR 20, bits 7-0) is set to 2, the software structures are defined to be 32 bits wide, and transmit descriptors look like Table 45 (CXDA = Current Transmit Descriptor Address).

When SWSTYLE (BCR 20, bits 7-0) is set to 3, then the software structures are defined to be 32 bits wide, and transmit descriptors look like Table 46 (CXDA = Current Transmit Descriptor Address).

Table 44. Transmit Descriptor (SWSTYLE = 0)

Address	15	14	13	12	11	10	9	8	7-0
CXDA+00h	TBADR[15:0]								
CXDA+02h	OWN	ERR	ADD_ FCS	MORE/ LTINT	ONE	DEF	STP	ENP	TBADR[23:16]
CXDA+04h	1	1	1	1	BCNT				
CXDA+06h	BUFF	UFLO	EX DEF	LCOL	LCAR	RTRY	TDR		

Table 45. Transmit Descriptor (SWSTYLE = 2)

Address	31	30	29	28	27	26	25	24	23	22-16	15-12	11-4	3-0
CXDA+00h	TBADR[31:0]												
CXDA+04h	OWN	ERR	ADD_ FCS	MORE/ LTINT	ONE	DEF	STP	ENP	BPE	RES	1111	BCNT	
CXDA+08h	BUFF	UFLO	EX DEF	LCOL	LCAR	RTRY	RES	RES	RES	RES	RES	RES	TRC
CXDA+0Ch	USER SPACE												

Table 46. Transmit Descriptor (SWSTYLE = 3)

Address	31	30	29	28	27	26	25	24	23	22-16	15-12	11-4	3-0
CXDA+00h	BUFF	UFLO	EX DEF	LCOL	LCAR	RTRY	RES					RES	TRC
CXDA+04h	OWN	ERR	ADD_ FCS	MORE/ LTINT	ONE	DEF	STP	ENP	BPE	RES	1111	BCNT	
CXDA+08h	TBADR[31:0]												
CXDA+0Ch	USER SPACE												

TMD0

Bit	Name	Description
31-0	TBADR	Transmit Buffer address. This field contains the address of the transmit buffer that is associated with this descriptor.

TMD1

Bit	Name	Description
31	OWN	This bit indicates whether the descriptor entry is owned by the host (OWN = 0) or by the Am79C972 controller (OWN = 1). The host sets the OWN bit after filling the buffer pointed to by the descriptor entry. The Am79C972 controller clears the OWN bit after transmitting the contents of the buffer. Both the Am79C972 controller and the host must not alter a descriptor entry after it has relinquished ownership.
30	ERR	ERR is the OR of UFLO, LCOL, LCAR, RTRY or BPE. ERR is set by the Am79C972 controller and cleared by the host. This bit is set in the current descriptor when the error occurs and, therefore, may be set in any descriptor of a chained buffer transmission.
29	ADD_FCS	ADD_FCS dynamically controls the generation of FCS on a frame by frame basis. This bit should be set with the ENP bit. However, for backward compatibility, it is recommended that this bit be set for every descriptor of the intended frame. When ADD_FCS is set, the state of DXMTFCS is ignored and transmitter FCS generation is activated. When ADD_FCS is cleared to 0, FCS generation is controlled by DXMTFCS. When APAD_XMT (CSR4, bit 11) is set to 1, the setting of ADD_FCS has no effect on frames shorter than 64 bytes. ADD_FCS is set by the host, and is not changed by the Am79C972 controller. This is a reserved bit in the C-LANCE (Am79C90) controller.
28	MORE/LTINT	Bit 28 always functions as MORE. The value of MORE is written by the Am79C972 controller and is read by the host. When LTINTEN is cleared to 0 (CSR5, bit 14), the Am79C972 controller will never look at the contents of bit 28, write operations by the host have no effect. When LTINTEN is set to 1 bit 28 changes its function to LTINT on host write operations and on Am79C972 controller read operations.
	MORE	MORE indicates that more than one retry was needed to transmit a frame. The value of MORE is written by the Am79C972 controller. This bit has meaning only if the ENP bit is set.
	LTINT	LTINT is used to suppress interrupts after successful transmission on selected frames. When LTINT is cleared to 0 and ENP is set to 1, the Am79C972 controller will not set TINT (CSR0, bit 9) after a successful transmission. TINT will only be set when the last descriptor of a frame has both LTINT and ENP set to 1. When LTINT is cleared to 0, it will only cause the suppression of interrupts for successful transmission. TINT will always be set if the transmission has an error. The LTINTEN overrides the function of TOKINTD (CSR5, bit 15).
27	ONE	ONE indicates that exactly one retry was needed to transmit a frame. ONE flag is not valid when LCOL is set. The value of the ONE bit is written by the Am79C972 controller. This bit has meaning only if the ENP bit is set.
26	DEF	Deferred indicates that the Am79C972 controller had to defer while trying to transmit a frame. This condition occurs if the channel is busy when the Am79C972 controller is ready to transmit. DEF is set by the Am79C972 controller and cleared by the host.
25	STP	Start of Packet indicates that this is the first buffer to be used by the Am79C972 controller for this

		frame. It is used for data chaining buffers. The STP bit must be set in the first buffer of the frame, or the Am79C972 controller will skip over the descriptor and poll the next descriptor(s) until the OWN and STP bits are set. STP is set by the host and is not changed by the Am79C972 controller.
24	ENP	End of Packet indicates that this is the last buffer to be used by the Am79C972 controller for this frame. It is used for data chaining buffers. If both STP and ENP are set, the frame fits into one buffer and there is no data chaining. ENP is set by the host and is not changed by the Am79C972 controller.
23	BPE	Bus Parity Error is set by the Am79C972 controller when a parity error occurred on the bus interface during a data transfers from the transmit buffer associated with this descriptor. The Am79C972 controller will only set BPE when the advanced parity error handling is enabled by setting APERREN (BCR20, bit 10) to 1. BPE is set by the Am79C972 controller and cleared by the host. This bit does not exist, when the Am79C972 controller is programmed to use 16-bit software structures for the descriptor ring entries (BCR20, bits 7-0, SWSTYLE is cleared to 0).
22-16	RES	Reserved locations.
15-12	ONES	These four bits must be written as ones. This field is written by the host and unchanged by the Am79C972 controller.
11-00	BCNT	Buffer Byte Count is the usable length of the buffer pointed to by this descriptor, expressed as the two's complement of the length of the buffer. This is the number of bytes from this buffer that will be transmitted by the Am79C972 controller. This field is written by the host and is not changed by the Am79C972 controller. There are no minimum buffer size restrictions.

TMD2

Bit	Name	Description
31	BUFF	Buffer error is set by the Am79C972 controller during transmission when the Am79C972 controller does not find the ENP flag in the current descriptor and does not own the next descriptor. This can occur in either of two ways: 1. The OWN bit of the next buffer is 0. 2. FIFO underflow occurred before the Am79C972 controller obtained the STATUS byte (TMD1[31:24]) of the next descriptor. BUFF is set by the Am79C972 controller and cleared by the host. If a Buffer Error occurs, an Underflow Error will also occur. BUFF is set by the Am79C972 controller and cleared by the host.
30	UFLO	Underflow error indicates that the transmitter has truncated a message because it could not read data from memory fast enough. UFLO indicates that the FIFO has emptied before the end of the frame was reached. When DXSUFLO (CSR3, bit 6) is cleared to 0, the transmitter is turned off when an UFLO error occurs (CSR0, TXON = 0). When DXSUFLO is set to 1, the Am79C972 controller gracefully recovers from an UFLO error. It scans the transmit descriptor ring until it finds the start of a new frame and starts a new transmission. UFLO is set by the Am79C972 controller and cleared by the host.

29	EXDEF	Excessive Deferral. Indicates that the transmitter has experienced Excessive Deferral on this transmit frame, where Excessive Deferral is defined in the ISO 8802-3 (IEEE/ANSI 802.3) standard. Excessive Deferral will also set the interrupt bit EXDINT (CSR5, bit 7).
28	LCOL	Late Collision indicates that a collision has occurred after the first channel slot time has elapsed. The Am79C972 controller does not retry on late collisions. LCOL is set by the Am79C972 controller and cleared by the host.
27	LCAR	Loss of Carrier is set when the carrier is lost during an Am79C972 controller initiated transmission when in GPSI mode and the device is operating in half-duplex mode. The Am79C972 controller does not retry upon loss of carrier. It will continue to transmit the whole frame until done. LCAR will not be set when the device is operating in full-duplex mode and the GPSI port is active. LCAR is not valid in Internal Loopback Mode. LCAR is set by the Am79C972 controller and cleared by the host. In MII mode, LCAR will be set when the PHY is in Link Fail state during transmission.
26	RTRY	Retry error indicates that the transmitter has failed after 16 attempts to successfully transmit a message, due to repeated collisions on the medium. If DRTY is set to 1 in the MODE register, RTRY will set after one failed transmission attempt. RTRY is set by the Am79C972 controller and cleared by the host.
25-4	RES	Reserved locations.
3-0	TRC	Transmit Retry Count. Indicates the number of transmit retries of the associated packet. The maximum count is 15. However, if a RETRY error occurs, the count will roll over to 0. In this case only, the Transmit Retry Count value of 0 should be interpreted as meaning 16. TRC is written by the Am79C972 controller into the last transmit descriptor of a frame, or when an error terminates a frame. Valid only when OWN is cleared to 0.

TMD3

Bit	Name	Description
31-0	US	User Space. Reserved for user defined space.

REGISTER SUMMARY

PCI Configuration Registers

Offset	Name	Width in Bit	Access Mode	Default Value
00h	PCI Vendor ID	16	RO	1022h
02h	PCI Device ID	16	RO	2000h
04h	PCI Command	16	RW	0000h
06h	PCI Status	16	RW	0290h
08h	PCI Revision ID	8	RO	3xh
09h	PCI Programming IF	8	RO	00h
0Ah	PCI Sub-Class	8	RO	00h
0Bh	PCI Base-Class	8	RO	02h
0Ch	Reserved	8	RO	00h
0Dh	PCI Latency Timer	8	RW	00h
0Eh	PCI Header Type	8	RO	00h
0Fh	Reserved	8	RO	00h
10h	PCI I/O Base Address	32	RW	0000 0001h
14h	PCI Memory Mapped I/O Base Address	32	RW	0000 0000h
18h - 2Bh	Reserved	8	RO	00h
2Ch	PCI Subsystem Vendor ID	16	RO	00h
2Eh	PCI Subsystem ID	16	RO	00h
30h	PCI Expansion ROM Base Address	32	RW	0000 0000h
34h	Capabilities Pointer	8	RO	40h
31h - 3Bh	Reserved	8	RO	00h
3Ch	PCI Interrupt Line	8	RW	00h
3Dh	PCI Interrupt Pin	8	RO	01h
3Eh	PCI MIN_GNT	8	RO	06h
3Fh	PCI MAX_LAT	8	RO	FFh
40h	PCI Capability Identifier	8	RO	01h
41h	PCI Next Item Pointer	8	RO	00h
42h	PCI Power Management Capabilities	16	RO	00h
44h	PCI Power Management Control/Status	8	RO	00h
46h	PCI PMCSR Bridge Support Extensions	8	RO	00h
47h	PCI Data	8	RO	00h
48h - FFh	Reserved	8	RO	00h

***Note**: RO = read only, RW = read/write, x = revision dependent*

Control and Status Registers

RAP Addr	Symbol	Default Value	Comments	Use
00	CSR0	uuuu 0004	Am79C972 Controller Status Register	R
01	CSR1	uuuu uuuu	Lower IADR: maps to location 16	S
02	CSR2	uuuu uuuu	Upper IADR: maps to location 17	S
03	CSR3	uuuu 0000	Interrupt Masks and Deferral Control	S
04	CSR4	uuuu 0115	Test and Features Control	R
05	CSR5	uuuu 0000	Extended Control and Interrupt 1	R
06	CSR6	uuuu uuuu	RXTX: RX/TX Encoded Ring Lengths	S
07	CSR7	0uuu 0000	Extended Control and Interrupt 1	R
08	CSR8	uuuu uuuu	LADRF0: Logical Address Filter — LADRF[15:0]	S
09	CSR9	uuuu uuuu	LADRF1: Logical Address Filter — LADRF[31:16]	S
10	CSR10	uuuu uuuu	LADRF2: Logical Address Filter — LADRF[47:32]	S
11	CSR11	uuuu uuuu	LADRF3: Logical Address Filter — LADRF[63:48]	S
12	CSR12	uuuu uuuu	PADR0: Physical Address Register — PADR[15:0][	S
13	CSR13	uuuu uuuu	PADR1: Physical Address Register — PADR[31:16]	S
14	CSR14	uuuu uuuu	PADR2: Physical Address Register — PADR[47:32]	S
15	CSR15	see register description	MODE: Mode Register	S
16	CSR16	uuuu uuuu	IADRL: Base Address of INIT Block Lower (Copy)	T
17	CSR17	uuuu uuuu	IADRH: Base Address of INIT Block Upper (Copy)	T
18	CSR18	uuuu uuuu	CRBAL: Current RCV Buffer Address Lower	T
19	CSR22	uuuu uuuu	CRBAU: Current RCV Buffer Address Upper	T
20	CSR20	uuuu uuuu	CXBAL: Current XMT Buffer Address Lower	T
21	CSR21	uuuu uuuu	CXBAU: Current XMT Buffer Address Upper	T
22	CSR22	uuuu uuuu	NRBAL: Next RCV Buffer Address Lower	T
23	CSR23	uuuu uuuu	NRBAU: Next RCV Buffer Address Upper	T
24	CSR24	uuuu uuuu	BADRL: Base Address of RCV Ring Lower	S
25	CSR25	uuuu uuuu	BADRU: Base Address of RCV Ring Upper	S
26	CSR26	uuuu uuuu	NRDAL: Next RCV Descriptor Address Lower	T
27	CSR27	uuuu uuuu	NRDAU: Next RCV Descriptor Address Upper	T
28	CSR28	uuuu uuuu	CRDAL: Current RCV Descriptor Address Lower	T
29	CSR29	uuuu uuuu	CRDAU: Current RCV Descriptor Address Upper	T
30	CSR30	uuuu uuuu	BADXL: Base Address of XMT Ring Lower	S
31	CSR31	uuuu uuuu	BADXU: Base Address of XMT Ring Upper	S
32	CSR32	uuuu uuuu	NXDAL: Next XMT Descriptor Address Lower	T
33	CSR33	uuuu uuuu	NXDAU: Next XMT Descriptor Address Upper	T

Note:

u = undefined value, R = Running register, S = Setup register, T = Test register; all default values are in hexadecimal format.

Control and Status Registers (Continued)

RAP Addr	Symbol	Default Value After H_RESET	Comments	Use
34	CSR34	uuuu uuuu	CXDAL: Current XMT Descriptor Address Lower	T
35	CSR35	uuuu uuuu	CXDAU: Current XMT Descriptor Address Upper	T
36	CSR36	uuuu uuuu	NNRDAL: Next Next Receive Descriptor Address Lower	T
37	CSR37	uuuu uuuu	NNRDAU: Next Next Receive Descriptor Address Upper	T
38	CSR38	uuuu uuuu	NNXDAL: Next Next Transmit Descriptor Address Lower	T
39	CSR39	uuuu uuuu	NNXDAU: Next Next Transmit Descriptor Address Upper	T
40	CSR40	uuuu uuuu	CRBC: Current Receive Byte Count	T
41	CSR41	uuuu uuuu	CRST: Current Receive Status	T
42	CSR42	uuuu uuuu	CXBC: Current Transmit Byte	T
43	CSR43	uuuu uuuu	CXST: Current Transmit Status	T
44	CSR44	uuuu uuuu	NRBC: Next RCV Byte Count	T
45	CSR45	uuuu uuuu	NRST: Next RCV Status	T
46	CSR46	uuuu uuuu	TXPOLL: Transmit Poll Time Counter	T
47	CSR47	uuuu uuuu	TXPI: Transmit Polling Interval	S
48	CSR48	uuuu uuuu	RXPOLL: Receive Poll Time Counter	T
49	CSR49	uuuu uuuu	RXPI: Receive Polling Interval	S
50	CSR50	uuuu uuuu	Reserved	
51	CSR51	uuuu uuuu	Reserved	
52	CSR52	uuuu uuuu	Reserved	
53	CSR53	uuuu uuuu	Reserved	
54	CSR54	uuuu uuuu	Reserved	
55	CSR55	uuuu uuuu	Reserved	
56	CSR56	uuuu uuuu	Reserved	
57	CSR57	uuuu uuuu	Reserved	
58	CSR58	see register description	SWS: Software Style	S
59	CSR59	uuuu uuuu	Reserved	T
60	CSR60	uuuu uuuu	PXDAL: Previous XMT Descriptor Address Lower	T
61	CSR61	uuuu uuuu	PXDAU: Previous XMT Descriptor Address Upper	T
62	CSR62	uuuu uuuu	PXBC: Previous Transmit Byte Count	T
63	CSR63	uuuu uuuu	PXST: Previous Transmit Status	T
64	CSR64	uuuu uuuu	NXBAL: Next XMT Buffer Address Lower	T
65	CSR65	uuuu uuuu	NXBAU: Next XMT Buffer Address Upper	T
66	CSR66	uuuu uuuu	NXBC: Next Transmit Byte Count	T
67	CSR67	uuuu uuuu	NXST: Next Transmit Status	T
68	CSR68	uuuu uuuu	Reserved	
69	CSR69	uuuu uuuu	Reserved	
70	CSR70	uuuu uuuu	Reserved	

Control and Status Registers (Continued)

RAP Addr	Symbol	Default Value After H_RESET	Comments	Use
71	CSR71	uuuu uuuu	Reserved	
72	CSR72	uuuu uuuu	RCVRC: RCV Ring Counter	T
73	CSR73	uuuu uuuu	Reserved	
74	CSR74	uuuu uuuu	XMTRC: XMT Ring Counter	T
75	CSR75	uuuu uuuu	Reserved	
76	CSR76	uuuu uuuu	RCVRL: RCV Ring Length	S
77	CSR77	uuuu uuuu	Reserved	
78	CSR78	uuuu uuuu	XMTRL: XMT Ring Length	S
79	CSR79	uuuu uuuu	Reserved	
80	CSR80	uuuu 1410	DMATCFW: DMA Transfer Counter and FIFO Threshold	S
81	CSR81	uuuu uuuu	Reserved	
82	CSR82	uuuu uuuu	Transmit Descriptor Pointer Address Lower	S
83	CSR83	uuuu uuuu	Reserved	
84	CSR84	uuuu uuuu	DMABA: Address Register Lower	T
85	CSR85	uuuu uuuu	DMABA: Address Register Upper	T
86	CSR86	uuuu uuuu	DMABC: Buffer Byte Counter	T
87	CSR87	uuuu uuuu	Reserved	
88	CSR88	x262 4003	Chip ID Register Lower	T
89	CSR89	uuuu x262	Chip ID Register Upper	T
90	CSR90	uuuu uuuu	Reserved	
91	CSR91	uuuu uuuu	Reserved	T
92	CSR92	uuuu uuuu	RCON: Ring Length Conversion	T
93	CSR93	uuuu uuuu	Reserved	
94	CSR94	uuuu uuuu	Reserved	
95	CSR95	uuuu uuuu	Reserved	
96	CSR96	uuuu uuuu	Reserved	
97	CSR97	uuuu uuuu	Reserved	
98	CSR98	uuuu uuuu	Reserved	
99	CSR99	uuuu uuuu	Reserved	
100	CSR100	uuuu 0200	Bus Timeout	S
101	CSR101	uuuu uuuu	Reserved	
102	CSR102	uuuu uuuu	Reserved	
103	CSR103	uuuu 0105	Reserved	
104	CSR104	uuuu uuuu	Reserved	
105	CSR105	uuuu uuuu	Reserved	
106	CSR106	uuuu uuuu	Reserved	
107	CSR107	uuuu uuuu	Reserved	

Control and Status Registers (Concluded)

RAP Addr	Symbol	Default Value After H_RESET	Comments	Use
108	CSR108	uuuu uuuu	Reserved	
109	CSR109	uuuu uuuu	Reserved	
110	CSR110	uuuu uuuu	Reserved	
111	CSR111	uuuu uuuu	Reserved	
112	CSR112	uuuu uuuu	Missed Frame Count	**R**
113	CSR113	uuuu uuuu	Reserved	
114	CSR114	uuuu uuuu	Received Collision Count	**R**
115	CSR115	uuuu uuuu	Reserved	
116	CSR116	0000 0000	OnNow Miscellaneous	**S**
117	CSR117	uuuu uuuu	Reserved	
118	CSR118	uuuu uuuu	Reserved	
119	CSR119	uuuu 0105	Reserved	
120	CSR120	uuuu uuuu	Reserved	
121	CSR121	uuuu uuuu	Reserved	
122	CSR226	uuuu 0000	Receive Frame Alignment Control	**S**
123	CSR237	uuuu uuuu	Reserved	
124	CSR248	uuuu 0000	Test Register 1	**T**
125	CSR125	003c 0060	MAC Enhanced Configuration Control	**T**
126	CSR126	uuuu uuuu	Reserved	
127	CSR127	uuuu uuuu	Reserved	

Bus Configuration Registers

Writes to those registers marked as “Reserved” will have no effect. Reads from these locations will produce undefined values.

RAP	Mnemonic	Default	Name	Programmability	
				User	EEPROM
0	MSRDA	0005h	Reserved	No	No
1	MSWRA	0005h	Reserved	No	No
2	MC	0002h	Miscellaneous Configuration	Yes	Yes
3	Reserved	N/A	Reserved	No	No
4	LED0	00C0h	LED0 Status	Yes	Yes
5	LED1	0084h	LED1 Status	Yes	Yes
6	LED2	0088h	LED2 Status	Yes	Yes
7	LED3	0090h	LED3 Status	Yes	Yes
8	Reserved	N/A	Reserved	No	No
9	FDC	0000h	Full-Duplex Control	Yes	Yes
10-15	Reserved	N/A	Reserved	No	No
16	IOBASEL	N/A	Reserved	No	No
17	IOBASEU	N/A	Reserved	No	No
18	BSBC	9001h	Burst and Bus Control	Yes	Yes
19	EECAS	0002h	EEPROM Control and Status	Yes	No
20	SWS	0200h	Software Style	Yes	No
22	PCILAT	FF06h	PCI Latency	Yes	Yes
23	PCISID	0000h	PCI Subsystem ID	No	Yes
24	PCISVID	0000h	PCI Subsystem Vendor ID	No	Yes
25	SRAMSIZ	0000h	SRAM Size	Yes	Yes
26	SRAMB	0000h	SRAM Boundary	Yes	Yes
27	SRAMIC	0000h	SRAM Interface Control	Yes	Yes
28	EBADDRL	N/A	Expansion Bus Address Lower	Yes	No
29	EBADDRU	N/A	Expansion Bus Address Upper	Yes	No
30	EBDR	N/A	Expansion Bus Data Port	Yes	No
31	STVAL	FFFFh	Software Timer Value	Yes	No
32	MIICAS	0000h	MII Control and Status	Yes	Yes
33	MIIADDR	N/A	MII Address	Yes	Yes
34	MIIMDR	N/A	MII Management Data	Yes	No
35	PCIVID	1022h	PCI Vendor ID	No	Yes
36	PMC_A	C811h	PCI Power Management Capabilities (PMC) Alias Register	No	Yes
37	DATA0	0000h	PCI DATA Register Zero Alias Register	No	Yes
38	DATA1	0000h	PCI DATA Register One Alias Register	No	Yes
39	DATA2	0000h	PCI DATA Register Two Alias Register	No	Yes
40	DATA3	0000h	PCI DATA Register Three Alias Register	No	Yes
41	DATA4	0000h	PCI DATA Register Four Alias Register	No	Yes
42	DATA5	0000h	PCI DATA Register Five Alias Register	No	Yes
43	DATA6	0000h	PCI DATA Register Six Alias Register	No	Yes
44	DATA7	0000h	PCI DATA Register Seven Alias Register	No	Yes
45	PMR1	N/A	Pattern Matching Register 1	Yes	No
46	PMR2	N/A	Pattern Matching Register 2	Yes	No
47	PMR3	N/A	Pattern Matching Register 3	Yes	No

REGISTER PROGRAMMING SUMMARY

Am79C972 Programmable Registers

Am79C972 Control and Status Registers

Register	Contents			
CSR0	Status and control bits: (DEFAULT = 0004)			
	8000 ERR 4000 -- 2000 CERR 1000 MISS	0800 MERR 0400 RINT 0200 TINT 0100I IDON	0080 INTR 0040 IENA 0020 RXON 0010 TXON	0008 TDMD 0004 STOP 0002 STRT 0001 INIT
CSR1	Lower IADR (Maps to CSR 16)			
CSR2	Upper IADR (Maps to CSR 17)			
CSR3	Interrupt masks and Deferral Control: (DEFAULT = 0)			
	8000 -- 4000 -- 2000 -- 1000 MISSM	0800 MERRM 0400 RINTM 0200 TINTM 0100 IDONM	0080 -- 0040 DXSUFLO 0020 LAPPEN 0010 DXMT2PD	0008 EMBA 0004 BSWP 0002 -- 0001 --
CSR4	Interrupt masks, configuration and status bits: (DEFAULT = 0115)			
	8000 -- 4000 DMAPLUS 2000 -- 1000 TXDPOLL	0800 APAD_XMT 0400 ASTRP_RCV 0200 MFCO 0100 MFCOM	0080 UNITCMD 0040 UNIT 0020 RCVCCO 0010 RCVCCOM	0008 TXSTRT 0004 TXSTRTM 0002 -- 0001 --
CSR5	Extended Interrupt masks, configuration and status bits: (DEFAULT = 0XXX)			
	8000 TOKINTD 4000 LTINTEN 2000 -- 1000 --	0800 SINT 0400 SINTE 0200 -- 0100 --	0080 EXDINT 0040 EXDINTE 0020 MPPLBA 0010 MPINT	0008 MPINTE 0004 MPEN 0002 MPMODE 0001 SPND
CSR7	Extended Interrupt masks, configuration and status bits: (DEFAULT = 0000)			
	8000 FASTSPND 4000 RXFRMTG 2000 RDMD 1000 RXDPOLL	0800 STINT 0400 STINTE 0200 MREINT 0100 MREINTE	0080 MAPINT 0040 MAPINTE 0020 MCCINT 0010 MCCINTE	0008 MCCIINT 0004 MCCIINTE 0002 MIIPDTINT 0001 MIIPDTNTE
CSR8 - CSR11	Logical Address Filter			
CSR12 - CSR14	Physical Address Register			
CSR15	MODE: (DEFAULT = 0) bits [8:7] = PORTSEL, Port Selection 10 GPSI port 11 Media Independent Interface			
	8000 PROM 4000 DRCVBC 2000 DRCVPA 1000 --	0800 -- 0400 -- 0200 -- 0100 PORTSEL1	0080 PORTSEL0 0040 INTL 0020 DRTY 0010 FCOLL	0008 DXMTFCS 0004 LOOP 0002 DTX 0001 DRX
CSR47	TXPOLLINT: Transmit Polling Interval			
CSR49	RXPOLLINT: Receive Polling Interval			
CSR58	Software Style (mapped to BCR20) bits [7:0] = SWSTYLE, Software Style Register. 0000 LANCE/PCnet-ISA 0002 PCnet-32			
	8000 -- 4000 -- 2000 -- 1000 --	0800 -- 0400 APERREN 0200 -- 0100 SSIZE32	0080 -- 0040 -- 0020 -- 0010 --	0008 SWSTYLE3 0004 SWSTYLE2 0002 -- 0001 SWSTYLE0

Am79C972 Control and Status Registers (Concluded)

Register	Contents
CSR76	RCVRL: RCV Descriptor Ring length
CSR78	XMTRL: XMT Descriptor Ring length
CSR80	FIFO threshold and DMA burst control (DEFAULT = 2810)
	8000 Reserved 4000 Reserved bits [13:12] = RCVFW, Receive FIFO Watermark 0000 Request DMA when 16 bytes are present 1000 Request DMA when 64 bytes are present 2000 Request DMA when 112 bytes are present 3000 Reserved bits [11:10] = XMTSP, Transmit Start Point 0000 Start transmission after 20/36 (No SRAM/SRAM) bytes have been written 0400 Start transmission after 64 bytes have been written 0800 Start transmission after 128 bytes have been written 0C00 Start transmission after 220 max/Full Packet (No SRAM/SRAM with UFLO bit set) bytes have been written bits [9:8] = XMTFW, Transmit FIFO Watermark 0000 Start DMA when 16 write cycles can be made 0100 Start DMA when 32 write cycles can be made 0200 Start DMA when 64 write cycles can be made 0300 Start DMA when 128 write cycles can be made bits [7:0] = DMA Burst Register
CSR88~89	Chip ID (Contents = v2624003; v = Version Number)
CSR112	Missed Frame Count
CSR114	Receive Collision Count
CSR116	OnNow Miscellaneous
	8000 -- 0800 -- 0080 PMAT 0008 RWU_DRIVER 4000 -- 0400 -- 0040 EMPPLBA 0004 RWU_GATE 2000 -- 0200 PME_EN_OVR 0020 MPMAT 0002 RWU_POL 1000 -- 0100 LCDET 0010 MPPEN 0001 RST_POL
CSR122	Receive Frame Alignment Control
	8000 -- 0800 -- 0080 -- 0008 -- 4000 -- 0400 -- 0040 -- 0004 -- 2000 -- 0200 -- 0020 -- 0002 -- 1000 -- 0100 -- 0010 -- 0001 RCVALGN
CSR124	BMU Test Register (DEFAULT = 0000)
	8000 -- 0800 -- 0080 -- 0008 -- 4000 -- 0400 -- 0040 -- 0004 RPA 2000 -- 0200 -- 0020 -- 0002 -- 1000 -- 0100 -- 0010 -- 0001 --
CSR125	MAC Enhanced Configuration Control (DEFAULT = 603c bits [15:8] = IPG, InterPacket Gap (Default=60xx, 96 bit times) bits [8:0] = IFS1, InterFrame Space Part 1 (Default=xx3c, 60 bit times)

Am79C972 Bus Configuration Registers

RAP Addr	Register	Contents							
0	MSRDA	Programs width of DMA read signal (DEFAULT = 5)							
1	MSWRA	Programs width of DMA write signal (DEFAULT = 5)							
2	MC	Miscellaneous Configuration bits: (DEFAULT = 2)							
		8000	--	0800	--	0080	INITLEVEL	0008	EADISEL
		4000	--	0400	--	0040	--	0004	--
		2000	--	0200	--	0020	--	0002	ASEL
		1000	--	0100	APROMWE	0010	--	0001	--
4	LED0	Programs the function and width of the LED0 signal. (DEFAULT = 00C0)							
		8000	LEDOUT	0800	--	0080	PSE	0008	--
		4000	LEDPOL	0400	--	0040	LNKSE	0004	RCVE
		2000	LEDDIS	0200	MPSE	0020	RCVME	0002	--
		1000	100E	0100	FDLSE	0010	XMTE	0001	COLE
5	LED1	Programs the function and width of the LED1 signal. (DEFAULT = 0084)							
		8000	LEDOUT	0800	--	0080	PSE	0008	--
		4000	LEDPOL	0400	--	0040	LNKSE	0004	RCVE
		2000	LEDDIS	0200	MPSE	0020	RCVME	0002	--
		1000	100E	0100	FDLSE	0010	XMTE	0001	COLE
6	LED2	Programs the function and width of the LED2 signal. (DEFAULT = 0088)							
		8000	LEDOUT	0800	--	0080	PSE	0008	--
		4000	LEDPOL	0400	--	0040	LNKSE	0004	RCVE
		2000	LEDDIS	0200	MPSE	0020	RCVME	0002	--
		1000	100E	0100	FDLSE	0010	XMTE	0001	COLE
7	LED3	Programs the function and width of the LED3 signal. (DEFAULT = 0090)							
		8000	LEDOUT	0800	--	0080	PSE	0008	--
		4000	LEDPOL	0400	--	0040	LNKSE	0004	RCVE
		2000	LEDDIS	0200	MPSE	0020	RCVME	0002	--
		1000	100E	0100	FDLSE	0010	XMTE	0001	COLE
9	FDC	Full-Duplex Control. (DEFAULT= 0000)							
		8000	--	0800	--	0080	--	0008	--
		4000	--	0400	--	0040	--	0004	FDRPAD
		2000	--	0200	--	0020	--	0002	--
		1000	--	0100	--	0010	--	0001	FDEN
16	IOBASEL	I/O Base Address Lower							
17	IOBASEU	I/O Base Address Upper							
18	BSBC	Burst Size and Bus Control (DEFAULT = 2101)							
		8000	ROMTMG3	0800	NOUFLO	0080	DWIO	0008	--
		4000	ROMTMG2	0400	--	0040	BREADE	0004	--
		2000	ROMTMG1	0200	MEMCMD	0020	BWRITE	0002	--
		1000	ROMTMG0	0100	EXTREQ	0010	--	0001	--
19	EECAS	EEPROM Control and Status (DEFAULT = 0002)							
		8000	PVALID	0800	--	0080	--	0008	--
		4000	PREAD	0400	--	0040	--	0004	ECS
		2000	EEDET	0200	--	0020	--	0002	ESK
		1000	--	0100	--	0010	EEN	0001	EDI/EDO
20	SWSTYLE	Software Style (DEFAULT = 0000, maps to CSR 58)							

Am79C972 Bus Configuration Registers (Concluded)

RAP Addr	Register	Contents
22	PCILAT	PCI Latency (DEFAULT = FF06)
		bits [15:8] = MAX_LAT bits [7:0] = MIN_GNT
25	SRAMSIZE	SRAM Size (DEFAULT = 0000)
		bits [7:0] = SRAM_SIZE
26	SRAMBND	SRAM Boundary (DEFAULT = 0000)
		bits [7:0] = SRAM_BND
27	SRAMIC	SRAM Interface Control (Default = 0000)
		8000 PTR TST 4000 LOLATRX bits [5:3] = EBCS, Expansion Bus Clock Source 0000 CLK pin, PCI clock 0008 Time Base Clock 0010 EBCLK pin, Expansion Bus Clock bits [2:0] = CLK_FAC, Expansion Bus Clock Factor 0000 1/1 clock factor 0001 1/2 clock factor 0002 -- 0003 --
28	EPADDRL	Expansion Port Address Lower (Default = 0000)
29	EPADDRU	Expansion Port Address Upper (Default = 0000)
		8000 FLASH, 4000 LAINC, 2000 --, 1000 -- 0800 --, 0400 --, 0200 --, 0100 -- 0080 --, 0040 --, 0020 --, 0010 -- 0008 EPADDRU3, 0004 EPADDRU2, 0002 EPADDRU1, 0001 EPADDRU0
30	EBDATA	Expansion Bus Data Port
31	STVAL	Software Timer Interrupt Value (DEFAULT = FFFF)
32	MIICAS	MII Status and Control (DEFAULT = 0000)
		8000 *ANTST*, 4000 MIIPD, 2000 FMDC1, 1000 FMDC0 0800 APEP, 0400 APDW2, 0200 APDW1, 0100 APDW0 0080 DANAS, 0040 XPHYRST, 0020 XPHYANE, 0010 XPHYFD 0008 XPHYSP, 0004 --, 0002 MIILP, 0001 --
33	MIIADDR	MII Address (DEFAULT = 0000)
		bits [9:5] = PHYAD, Physical Layer Device Address bits [4:0] = REGAD, MII/Auto-Negotiation Register Address
34	MIIMDR	MII Data Port
35	PCI Vendor ID	PCI Vendor ID Register (DEFAULT = 1022h)
36	PMC Alias	PCI Power Management Capabilities (DEFAULT = 0000)
37	DATA 0	PCI Data Register Zero Alias Register (DEFAULT = 0000)
38	DATA 1	PCI Data Register One Alias Register (DEFAULT = 0000)
39	DATA 2	PCI Data Register Two Alias Register (DEFAULT = 0000)
40	DATA 3	PCI Data Register Three Alias Register (DEFAULT = 0000)
41	DATA 4	PCI Data Register Four Alias Register (DEFAULT = 0000)
42	DATA 5	PCI Data Register Five Alias Register (DEFAULT = 0000)
43	DATA 6	PCI Data Register Six Alias Register (DEFAULT = 0000)
44	DATA 7	PCI Data Register Seven Alias Register (DEFAULT = 0000)
45	PMR 1	OnNow Pattern Matching Register 1
46	PMR 2	OnNow Pattern Matching Register 2
47	PMR 3	OnNow Pattern Matching Register 3

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature ..... -65°C to +70°C

Supply voltage
with respect to V_{SSB}, V_{SS} ..... –0.3 V to 3.63 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (TA) ..... 0°C to +70°C

Industrial (I) Devices

Temperature (TA) ..... -40°C to +85°C

Supply Voltages (VDD, VDDB, V_{DD_PCI}) ..+3.3 V ±10%

All inputs within the range:

V_{SS} - 0.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Units
Digital I/O (Non-PCI Pins)					
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
V_{OL}	Output LOW Voltage	I_{OL1} = 4 mA I_{OL2} = 6 mA I_{OL3} = 12 mA (Note 1)		0.4	V
V_{OH}	Output HIGH Voltage (Notes 2, 3)	I_{OH1}= -4 mA I_{OH2}= -2 mA (Note 3)	2.4		V
I_{OZ}	Output Leakage Current (Note 4)	0 V <V_{OUT} <V_{DD}	-10	10	µA
I_{IX}	Input Leakage Current (Note 5)	0 V <V_{IN} <V_{DD}	-10	10	µA
I_{IL}	Input LOW Current (Note 6)	V_{IN} = 0 V; V_{DD} = 3.6 V	-200	-10	µA
I_{IH}	Input HIGH Current (Note 6)	V_{IN} = 2.7 V; V_{DD} = 3.6 V	-50	10	µA
PCI Bus Interface - 5 V Signaling					
V_{IH}	Input HIGH Voltage		2.0	5.5	V
V_{IL}	Input LOW Voltage		-0.5	0.8	V
I_{OZ}	Output Leakage Current (Note 4)	0 V <V_{IN} < V_{DD_PCI}	-10	10	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V	--	-70	µA
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V	--	70	µA
I_{IX_PME}	Input Leakage Current (Note 7)	0 V = < V_{IN} < 5.5 V	-1	1	µA
V_{OH}	Output HIGH Voltage (Note 2)	I_{OH} = -2 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL}4 = 3 mA I_{OL}2 = 6 mA (Note 1)		0.55	V
PCI Bus Interface - 3.3 V Signaling					
V_{IH}	Input HIGH Voltage		0.5 V_{DD_PCI}	V_{DD_PCI} + 0.5	V
V_{IL}	Input LOW Voltage		-0.5	0.3 V_{DD_PCI}	V
I_{OZ}	Output Leakage Current (Note 4)	0 V < V_{OUT} < V_{DD_PCI}	-10	10	µA
I_{IL}	Input HIGH Current	0 V < V_{IN} < V_{DD_PCI}	-10	10	µA
I_{IX_PME}	Input Leakage Current (Note 7)	0 V = < V_{IN} < 5.5 V	-1	1	µA
V_{OH}	Output HIGH Voltage (Note 2)	I_{OH} = -500 µA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 1500 µA		0.1 V_{DD_PCI}	V

DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES unless otherwise specified (Concluded)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Units
Pin Capacitance					
C_{IN}	Pin Capacitance	F_C = 1 MHz (Note 8)		10	pF
C_{CLK}	CLK Pin Capacitance	F_C = 1 MHz (Notes 8,9)	5	12	pF
C_{IDSEL}	IDSEL Pin Capacitance	Fc = 1 MHz (Notes 8, 10		8	pF
LPIN	Pin Inductance	Fc = 1 MHz (Note 8)		20	nH
Power Supply Current					
I_{DD}	Dynamic Current	PCI CLK at 33 MHz, MII Interface at 25 MHz, Full-Duplex operation		120	mA
I_{DD_WU1}	Wake-up current when the device is in the D1, D2, or D3 state and the PCI bus is in the B0 or B1 state.	PCI CLK at 33 MHz, MII Interface at 25 MHz, Device at Magic Packet or OnNow mode, receiving non-matching packets		65	mA
I_{DD_WU2}	Wake-up current when the device is in the D2 or D3 state and the PCI bus is in the B2 or B3 state.	PCI CLK LOW, MII Interface at 25 MHz, PG LOW, Device at Magic Packet or OnNow mode, receiving non-matching packets		25	mA
I_{DD_S}	Static I_{DD}	PCI CLK, RST, and MII pins LOW and TBC_EN pin HIGH.		1	mA

Notes:

1. *I_{OL1} applies to TXD[3:0], TX_EN,TX_ER,MDC, and MDIO pins.*
   I_{OL2} applies to $\overline{DEVSEL}$, $\overline{FRAME}$, $\overline{INTA}$, $\overline{IRDY}$, $\overline{PERR}$, $\overline{SERR}$, $\overline{STOP}$, $\overline{TRDY}$, EECS, EEDI, EBUA_EBA[7:0], EBDA[15:8], EBD[7:0], $\overline{EROMCS}$, AS_$\overline{EBOE}$, $\overline{EBWE}$, and PHY_RST.
   I_{OL3} applies to LED0, LED1, LED2, LED3, and WUMI.
   I_{OL4} applies to AD[31:0], C/$\overline{BE}$[3:0], PAR, and $\overline{REQ}$ pins in a 5 V signalling environment.
2. *V_{OH} does not apply to open-drain output pins.*
3. *I_{OH1} applies to TXD[3:0], TX_EN,TX_ER,MDC, and MDIO pins.*
   I_{OH2} applies to all other outputs.
4. *I_{OZ} applies to all output and bidirectional pins, except the $\overline{PME}$ pin. Tests are performed at V_{IN} = 0 V and at V_{DD} only.*
5. *I_{IX} applies to all input pins except $\overline{PME}$, TDI, TCLK, and TMS pins.*
6. *I_{IL} and I_{IH} apply to the TDI, TCLK, and TMS pins.*
7. *I_{IX_PME} applies to the $\overline{PME}$ pin only. Tests are performed at V_{IN} = 0 V and 5.5 V only.*
8. *Parameter not tested. Value determined by characterization.*
9. *C_{CLK} applies only to the CLK pin.*
10. *C_{IDSEL} applies only to the IDSEL, TX_CLK, COL, CRS, RX_CLK, RXD[3:0], RX_DV, and RX_ER pins.*

SWITCHING CHARACTERISTICS: BUS INTERFACE unless otherwise noted, parametric values are applicable to Commercial and Industrial devices

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
Clock Timing					
F_{CLK}	CLK Frequency		0	33	MHz
t_{CYC}	CLK Period	@ 1.5 V for 5 V signaling @ 0.4 V_{DD} for 3.3 V signaling	30	–	ns
t_{HIGH}	CLK High Time	@ 2.0 V for 5 V signaling @ 0.4 V_{DD} for 3.3 signaling	12		ns
t_{LOW}	CLK Low Time	@ 0.8 V for 5 V signaling @ 0.3 V_{DD} for 3.3 V signaling	12		ns
t_{FALL}	CLK Fall Time	over 2 V p-p for 5 V signaling over 0.4 V_{DD} for 3.3 V signaling (Note 1)	1	4	V/ns
t_{RISE}	CLK Rise Time	over 2 V p-p for 5 V signaling over 0.4 V_{DD} for 3.3 V signaling (Note 1)	1	4	V/ns
Output and Float Delay Timing					
t_{VAL}	AD[31:00], C/BE[3:0], PAR, FRAME, IRDY, TRDY, STOP, DEVSEL, PERR, SERR Valid Delay		2	11	ns
t_{VAL} ($\overline{REQ}$)	$\overline{REQ}$ Valid Delay		2	12	ns
t_{ON}	AD[31:00], C/BE[3:0], PAR, FRAME, IRDY, TRDY, STOP, DEVSEL Active Delay		2		ns
t_{OFF}	AD[31:00], C/BE[3:0], PAR, FRAME, IRDY, TRDY, STOP, DEVSEL Float Delay			28	ns
Setup and Hold Timing					
t_{SU}	AD[31:00], C/BE[3:0], PAR, FRAME, IRDY, TRDY, STOP, DEVSEL, IDSEL Setup Time		7		ns
t_{H}	AD[31:00], C/BE[3:0], PAR, FRAME, IRDY, TRDY, STOP, DEVSEL, IDSEL Hold Time		0		ns
t_{SU} ($\overline{GNT}$)	$\overline{GNT}$ Setup Time		10		ns
t_{H} (GNT)	GNT Hold Time		0		ns

SWITCHING CHARACTERISTICS: BUS INTERFACE unless otherwise noted, parametric values are applicable to Commercial and Industrial devices (Concluded)

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
EEPROM Timing					
f_{EESK}	EESK Frequency	(Note 2)		650	kHz
t_{HIGH} (EESK)	EESK High Time		780		ns
t_{LOW} (EESK)	EESK Low Time		780		ns
t_{VAL} (EEDI)	EEDI Valid Output Delay from EESK	(Note 2)	-15	15	ns
t_{VAL} (EECS)	EECS Valid Output Delay from EESK	(Note 2)	-15	15	ns
t_{LOW} (EECS)	EECS Low Time		1550		ns
t_{SU} (EEDO)	EEDO Setup Time to EESK	(Note 2)	50		ns
t_{H} (EEDO)	EEDO Hold Time from EESK	(Note 2)	0		ns
JTAG (IEEE 1149.1) Test Signal Timing					
t_{J1}	TCK Frequency			10	MHz
t_{J2}	TCK Period		100		ns
t_{J3}	TCK High Time	@ 2.0 V	45		ns
t_{J4}	TCK Low Time	@ 0.8 V	45		ns
t_{J5}	TCK Rise Time			4	ns
t_{J6}	TCK Fall Time			4	ns
t_{J7}	TDI, TMS Setup Time		8		ns
t_{J8}	TDI, TMS Hold Time		10		ns
t_{J9}	TDO Valid Delay		3	30	ns
t_{J10}	TDO Float Delay			50	ns
t_{J11}	All Outputs (Non-Test) Valid Delay		3	25	ns
t_{J12}	All Outputs (Non-Test) Float Delay			36	ns
t_{J13}	All Inputs (Non-Test)) Setup Time		8		ns
t_{J14}	All Inputs (Non-Test) Hold Time		7		ns

Notes:

1. *Not tested; parameter guaranteed by design characterization.*
2. *Parameter value is given for automatic EEPROM read operation. When EEPROM port (BCR19) is used to access the EEPROM, software is responsible for meeting EEPROM timing requirements.*

SWITCHING CHARACTERISTICS: MEDIA INDEPENDENT INTERFACE unless otherwise noted, parametric values are applicable to Commercial and Industrial devices

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
Transmit Timing					
t_{TVAL}	TX_EN, TX_ER, TXD valid from ↑ TX_CLK	measured from V_{ilmax} = 0.8 V or measured from V_{ihmin} = 2.0V (Note 1)	0	25	ns
Receive Timing					
t_{RSU}	RX_DV, RX_ER, RXD setup to ↑ RX_CLK	measured from V_{ilmax} = 0.8 V or measured from V_{ihmin} = 2.0V (Note 1)	10		ns
t_{RH}	RX_DV, RX_ER, RXD hold to ↑ RX_CLK	measured from V_{ilmax} = 0.8 V or measured from V_{ihmin} = 2.0V (Note 1)	10		ns
Management Cycle Timing					
t_{MHIGH}	MDC Pulse Width HIGH Time	C_{LOAD} = 390 pf	160		ns
t_{MLOW}	MDC Pulse Width LOW Time	C_{LOAD} = 390 pf	160		ns
t_{MCYC}	MDC Cycle Period	C_{LOAD} = 390 pf	400		ns
t_{MSU} (Input Parameter)	MDIO setup to ↑ MDC	C_{LOAD} = 470 pf, measured from V_{ilmax} = 0.8 V or measured from V_{ihmin} = 2.0V (Note 1)	25		ns
t_{MH} (Input Parameter)	MDIO hold to ↑ MDC	C_{LOAD} = 470 pf, measured from V_{ilmax} = 0.8 V or measured from V_{ihmin} = 2.0V (Note 1)	10		ns
t_{MVAL} (Input Parameter)	MDIO valid from ↑ MDC	C_{LOAD} = 470 pf, measured from V_{ilmax} = 0.8 V or measured from V_{ihmin} = 2.0V, (Note 1)	t_{MCYC} - t_{MSU}		ns

Notes:

1. *MDIO valid measured at the exposed mechanical Media Independent Interface.*
2. *TXCLK and RXCLK frequency and timing parameters are defined for the external physical layer transceiver as defined in the IEEE 802.3u standard. They are not replicated here.*

SWITCHING CHARACTERISTICS: GENERAL-PURPOSE SERIAL INTERFACE unless otherwise noted, parametric values are applicable to Commercial and Industrial devices

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
Transmit Timing					
t_{GPT1}	TXCLK Period (802.3 compliant)	@ 1.5 V	99.99	100.01	ns
t_{GPT2}	TXCLK HIGH Time	@ 2.0 V	40	60	ns
t_{GPT3}	TXDAT and TXEN Delay from ↑ TXCLK	@ 1.5 V	0	70	ns
t_{GPT4}	RXEN Setup before ↑ TXCLK (Last Bit)	@ 1.5 V	210		ns
t_{GPT5}	RXEN Hold after ↓ TXEN	@ 1.5 V	0		ns
t_{GPT6}	CLSN Active Time to Trigger Collision	@ 1.5 V (Note 1)	410		ns
t_{GPT7}	CLSN Active to ↓ RXEN to Prevent LCAR Assertion	@ 1.5 V	0		ns
t_{GPT8}	CLSN Active to ↓ RXEN for SQE Heartbeat window	@ 1.5 V	0	4.0	µs
t_{GPT9}	CLSN Active to ↑ RXEN for Normal Collision	@ 1.5 V	0	51.2	µs
Receive Timing					
t_{GPR1}	RXCLK Period	@ 1.5 V (Note 2)	80	120	ns
t_{GPR2}	RXCLK HIGH Time	@ 2.0 V (Note 2)	30	80	ns
t_{GPR3}	RXCLK LOW Time	@ 0.8 V (Note 2)	30	80	ns
t_{GPR4}	RXDAT and RXEN Setup to ↑ RXCLK	@ 1.5 V	15		ns
t_{GPR5}	RXDAT Hold after ↑ RXCLK	@ 1.5 V	15		ns
t_{GPR6}	RXEN Hold after ↓ RXCLK	@ 1.5 V	0		ns
t_{GPR7}	CLSN Active to First ↑ RXCLK (Collision Recognition)	@ 1.5 V	0		ns
t_{GPR8}	CLSN Active to ↑ RXCLK for Address Type Designation Bit	@ 1.5 V (Note 3)	51.2		µs
t_{GPR9}	CLSN Setup to Last ↑ RXCLK for Collision Recognition	@ 1.5 V	210		ns
t_{GPR10}	CLSN Active	@ 1.5 V	410		ns
t_{GPR11}	CLSN Inactive Setup to First ↑ RXCLK	@ 1.5 V	300		ns
t_{GPR12}	CLSN Inactive Hold to Last ↑ RXCLK	@ 1.5 V	300		ns

***Notes**:*

1. *CLSN must be asserted for a continuous period of 110 ns or more. Assertion for less than 110 ns period may or may not result in CLSN recognition.*
2. *RXCLK should meet jitter requirements of IEEE 802.3 specification.*
3. *CLSN assertion before 51.2 µs will be indicated as a normal collision. CLSN assertion after 51.2 µs will be considered as a Late Receive Collision.*

SWITCHING CHARACTERISTICS: EXTERNAL ADDRESS DETECTION INTERFACE unless otherwise noted, parametric values are applicable to Commercial and Industrial devices

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
External Address Detection Interface: Internal PHY					
t_{EAD1}	SRD setup to ↑ SRDCLK		40		ns
t_{EAD2}	SRD hold to ↑ SRDCLK		40		ns
t_{EAD3}	SFBD# change to ↓ SRDCLK		-15	+15	ns
t_{EAD4}	EAR deassertion to ↑ SRDCLK (first rising edge)		50		ns
t_{EAD5}	EAR assertion after SFD event (frame rejection)		0	51,090	ns
t_{EAD6}	EAR assertion width		110		ns
External Address Detection Interface: External PHY - MII @ 25 MHz					
t_{EAD7}	SFBD change to ↓ RX_CLK		0	20 (Note 1)	ns
tEAD8	EAR deassertion to ↑ RX_CLK (first rising edge)		40		ns
t_{EAD9}	EAR assertion after SFD event (frame rejection)		0	5,080	ns
t_{EAD10}	EAR assertion width		50		ns
External Address Detection Interface: External PHY - MII @ 2.5 MHz					
t_{EAD11}	$\overline{EAR}$ deassertion to ↑ RX_CLK (first rising edge)		400		ns
t_{EAD12}	$\overline{EAR}$ assertion after SFD event (frame rejection)		0	50,800	ns
t_{EAD13}	$\overline{EAR}$ assertion width		500		ns
Receive Frame Tag Timing with Media Independent Interface					
t_{EAD14}	RXFRTGE assertion to ↑SF/BD (first rising edge)		0		ns
t_{EAD15}	RXFRTGE, RXFRTGD setup to ↑ RX_CLK		10		ns
t_{EAD16}	RXFRTGE, RXFRTGD hold to ↑ RX_CLK		10		ns
t_{EAD17}	RXFRTGE deassertion to ↓ RX_DV	RX_CLK @25 MHz RX_CLK @2.5 MHz	40 400		ns ns

Note:

1. May need to delay RX_CLK to capture Start Frame Byte Delimiter (SFBD) at 100 Mbps operation.

SWITCHING WAVEFORMS

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUITS

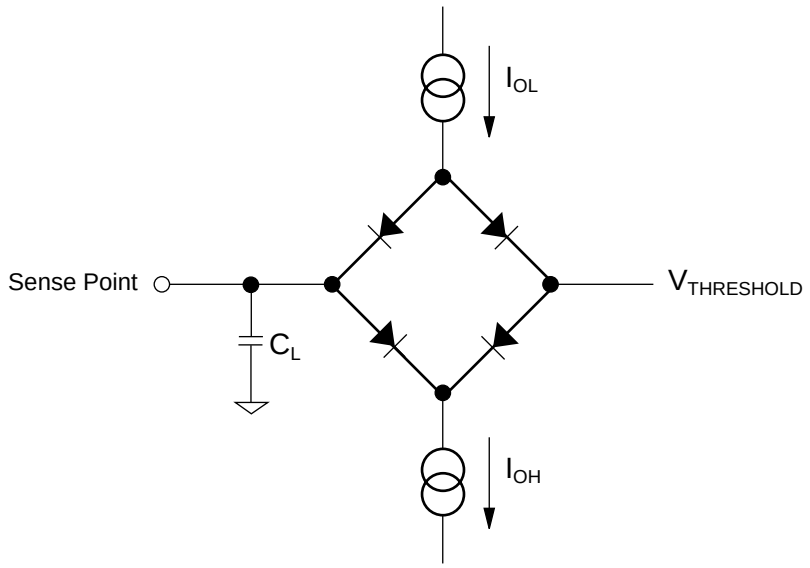

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Figure 53. Normal and Tri-State Outputs

SWITCHING WAVEFORMS: SYSTEM BUS INTERFACE

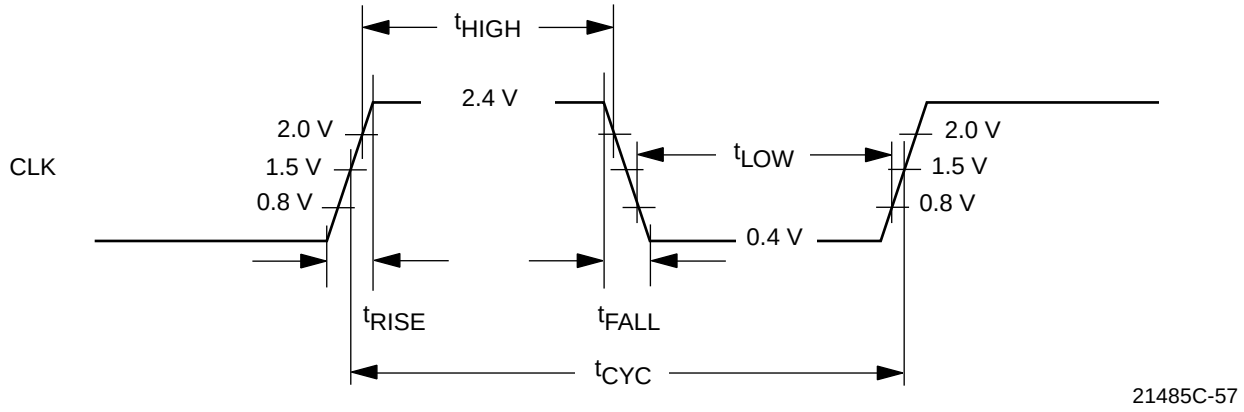

Figure 54. CLK Waveform for 5 V Signaling

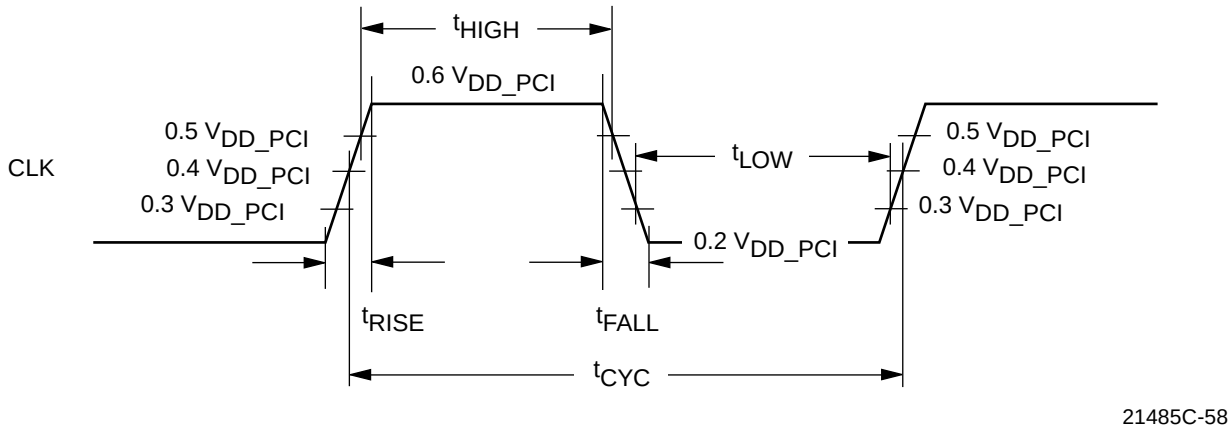

Figure 55. CLK Waveform for 3.3 V Signaling

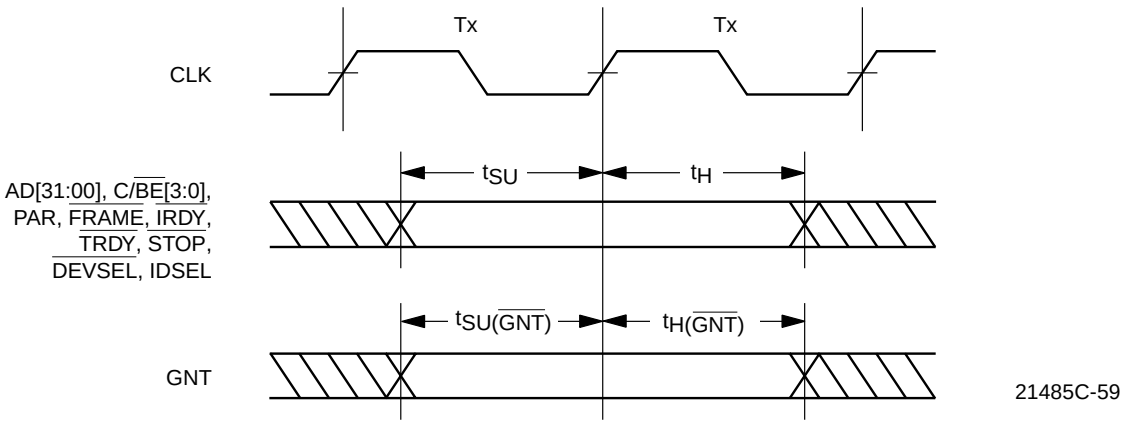

Figure 56. Input Setup and Hold Timing

SWITCHING WAVEFORMS: SYSTEM BUS INTERFACE (Continued)

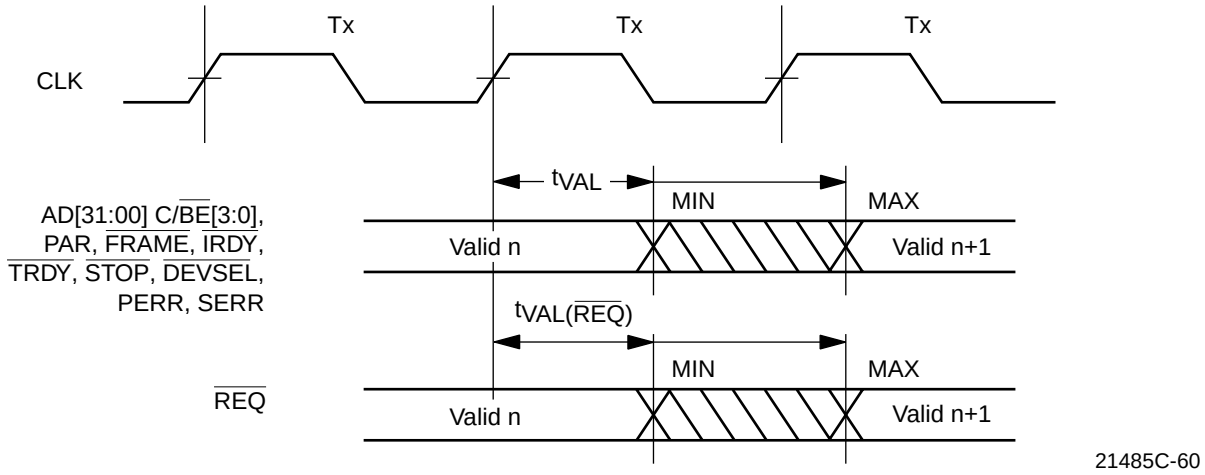

Figure 57. Output Valid Delay Timing

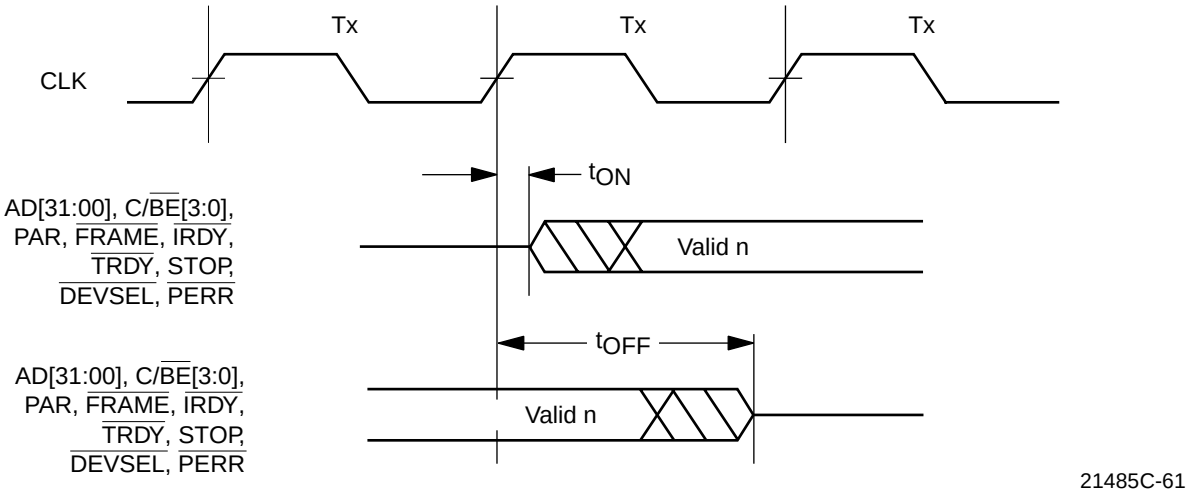

Figure 58. Output Tri-state Delay Timing

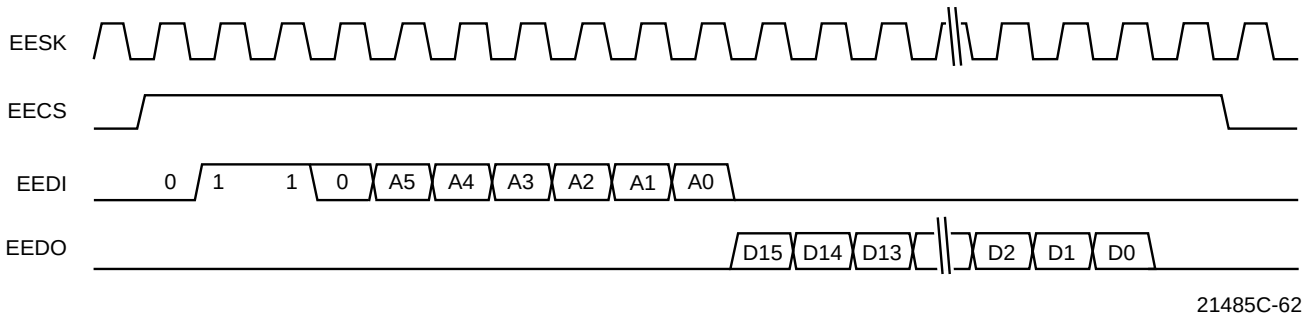

Figure 59. EEPROM Read Functional Timing

SWITCHING WAVEFORMS: SYSTEM BUS INTERFACE (Continued)

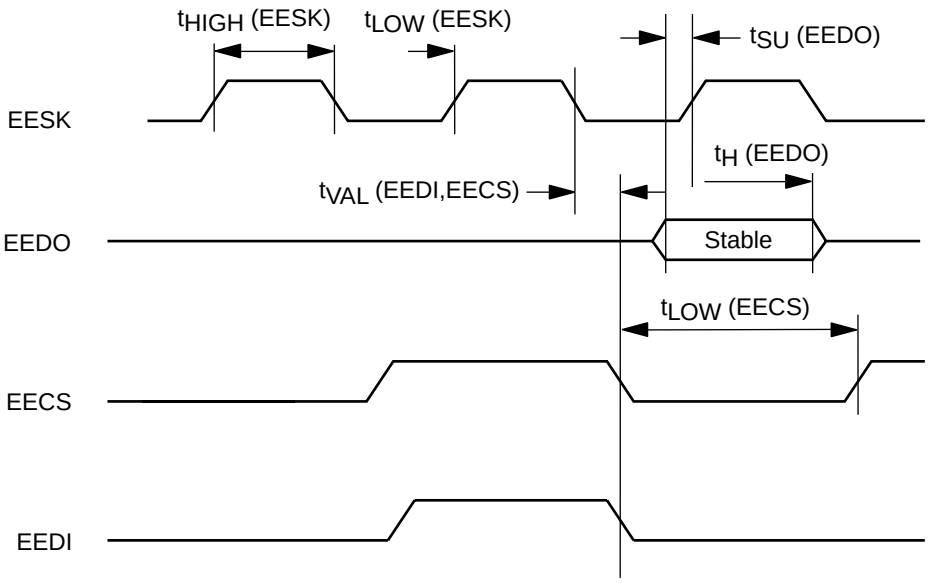

Figure 60. Automatic PREAD EEPROM Timing

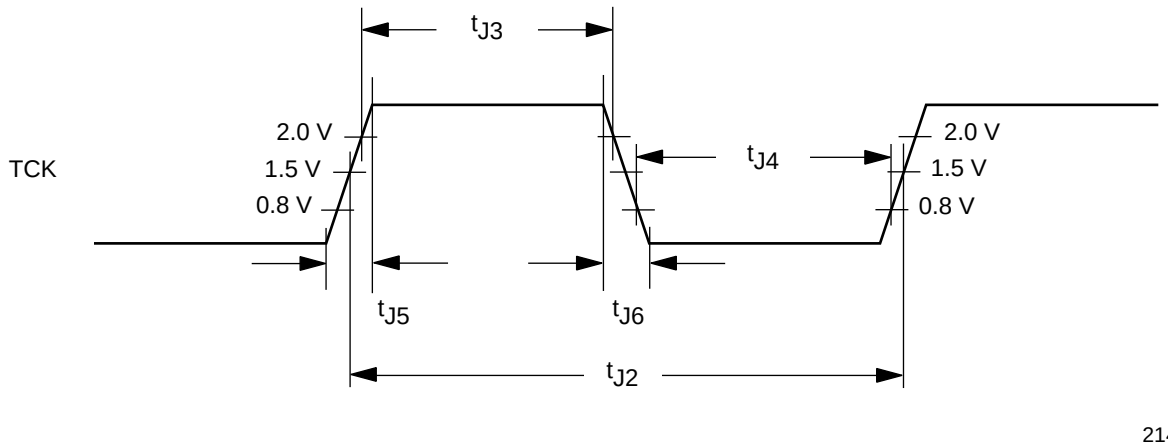

Figure 61. JTAG (IEEE 1149.1) TCK Waveform for 5 V Signaling

SWITCHING WAVEFORMS: SYSTEM BUS INTERFACE (Concluded)

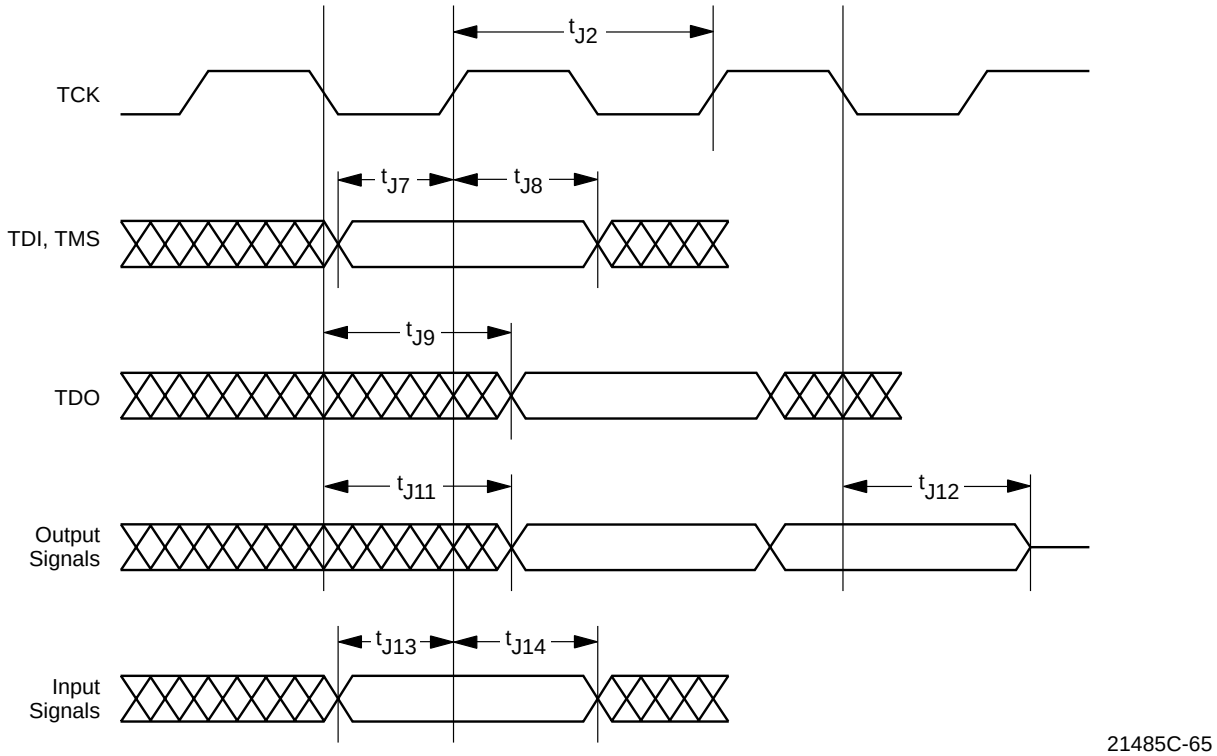

Figure 62. JTAG (IEEE 1149.1) Test Signal Timing

SWITCHING WAVEFORMS: EXPANSION BUS INTERFACE

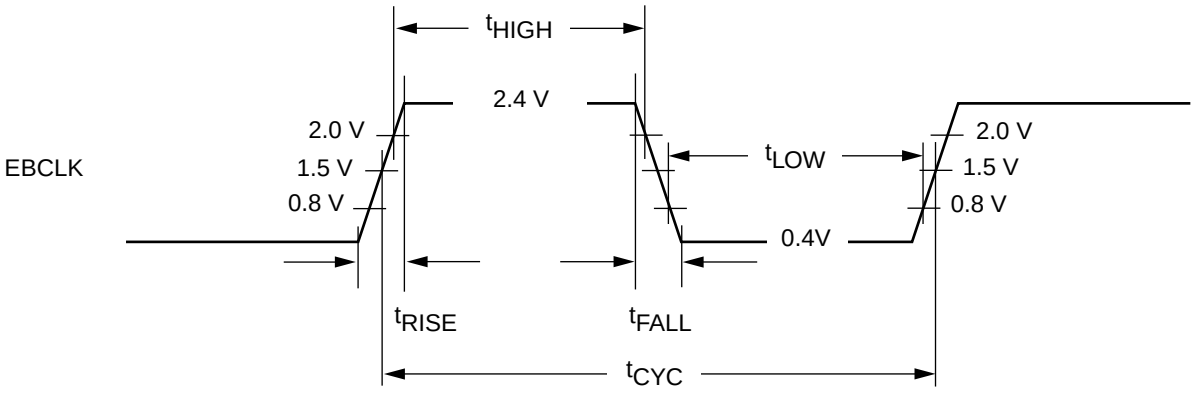

Figure 63. EBCLK Waveform

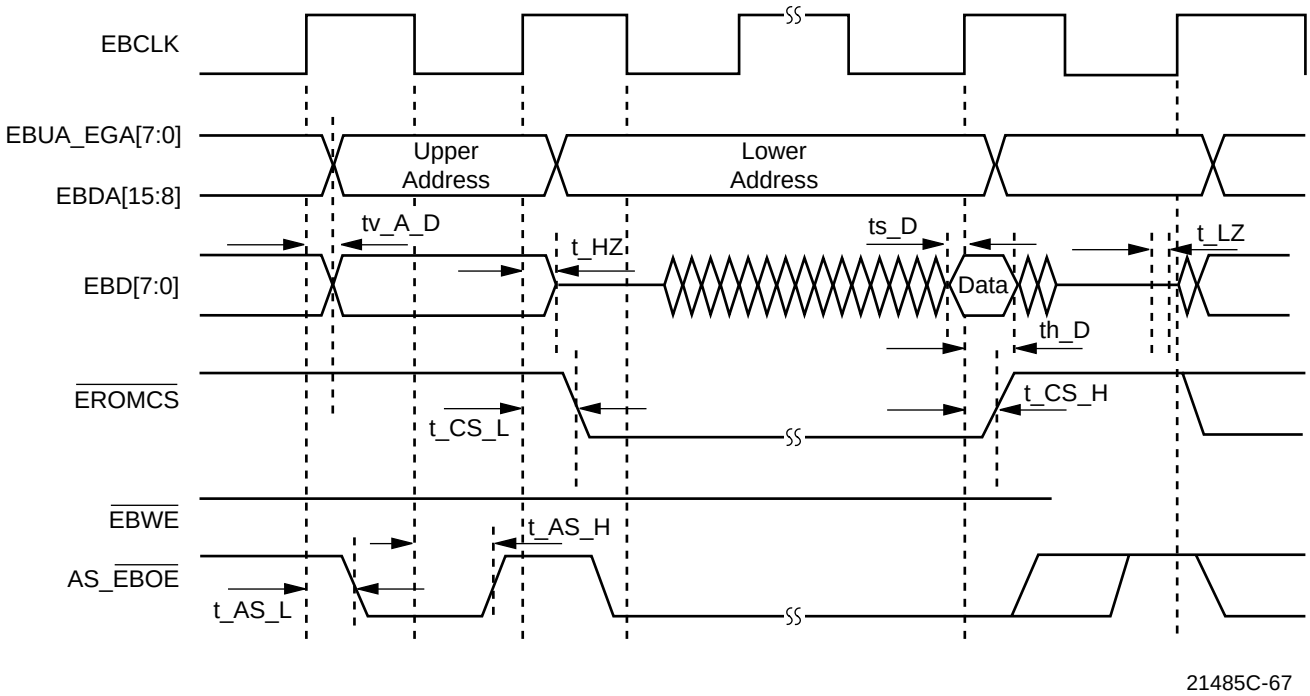

Figure 64. Expansion Bus Read Timing

SWITCHING WAVEFORMS: EXPANSION BUS INTERFACE (Concluded)

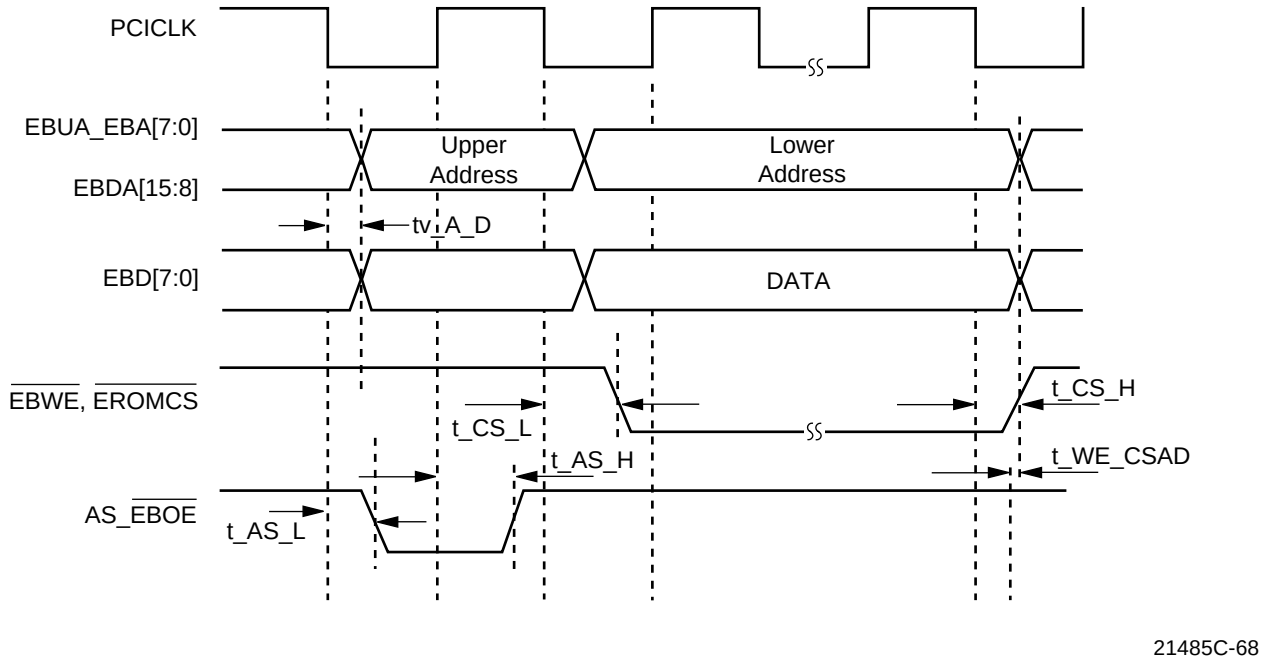

Figure 65. Expansion Bus Write Timing

SWITCHING WAVEFORMS: MEDIA INDEPENDENT INTERFACE

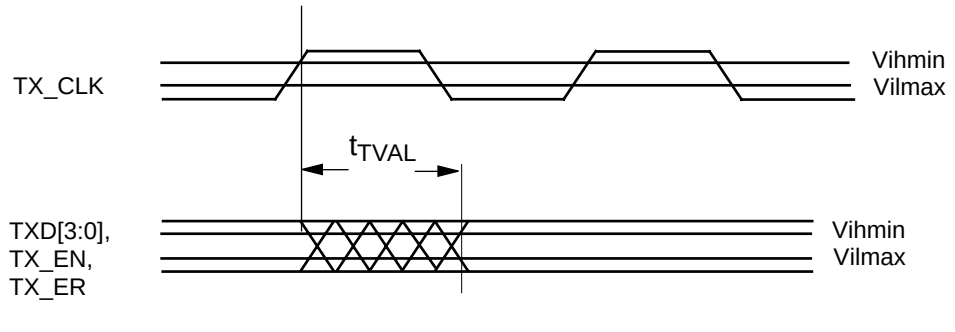

Figure 66. Transmit Timing

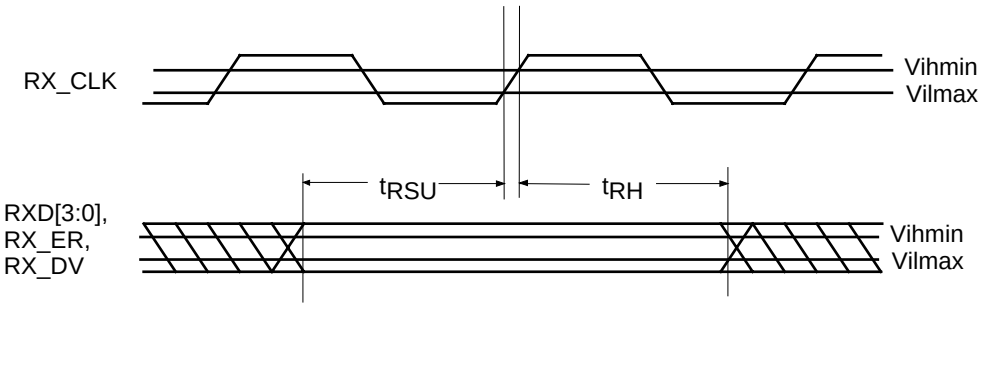

Figure 67. Receive Timing

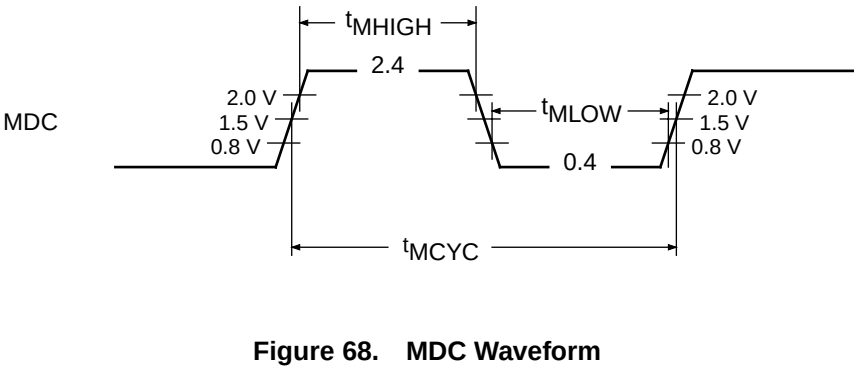

Figure 68. MDC Waveform

SWITCHING WAVEFORMS: MEDIA INDEPENDENT INTERFACE (Concluded)

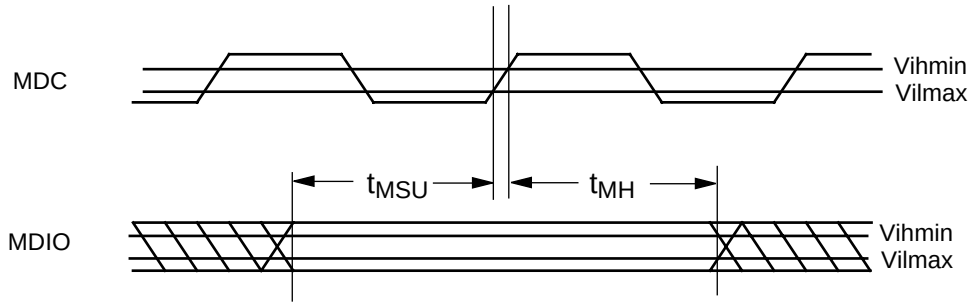

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Figure 69. Management Data Setup and Hold Timing

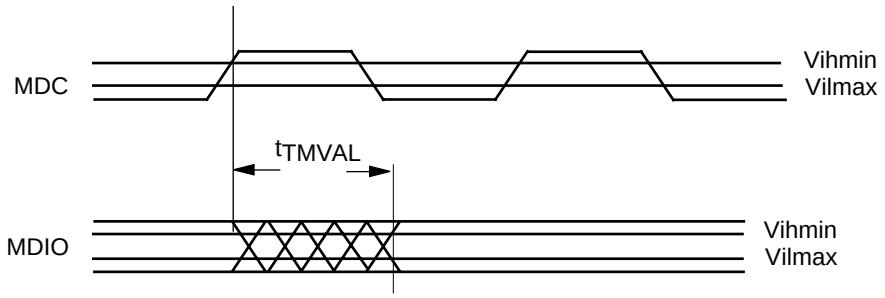

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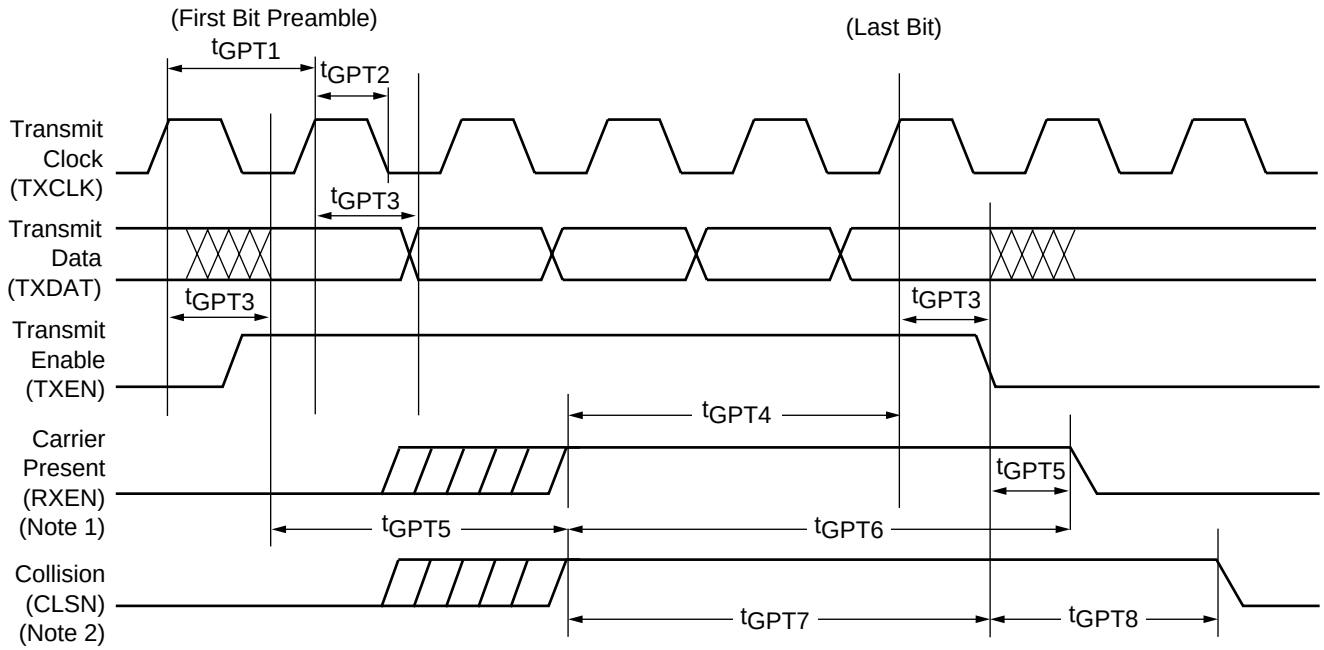
Figure 70. Management Data Output Valid Delay Timing

SWITCHING WAVEFORMS: GENERAL-PURPOSE SERIAL INTERFACE



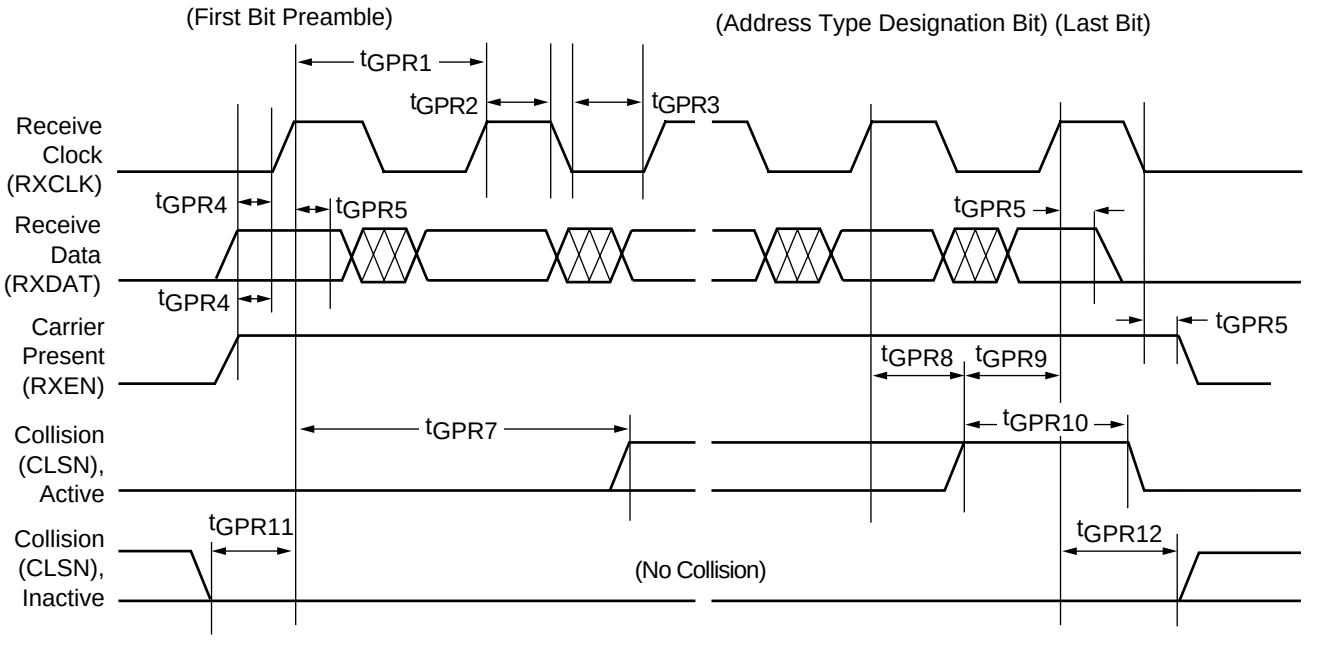
Notes:

1. If RXCRS is not present during transmission, LCAR bit in TMD2 will be set.

2. If CLSN is not present during or shortly after transmission, CERR in CSR0 will be set.

21485C-74

Figure 71. Transmit Timing



21485C-75

Figure 72. Receive Timing

SWITCHING WAVEFORMS: EXTERNAL ADDRESS DETECTION INTERFACE

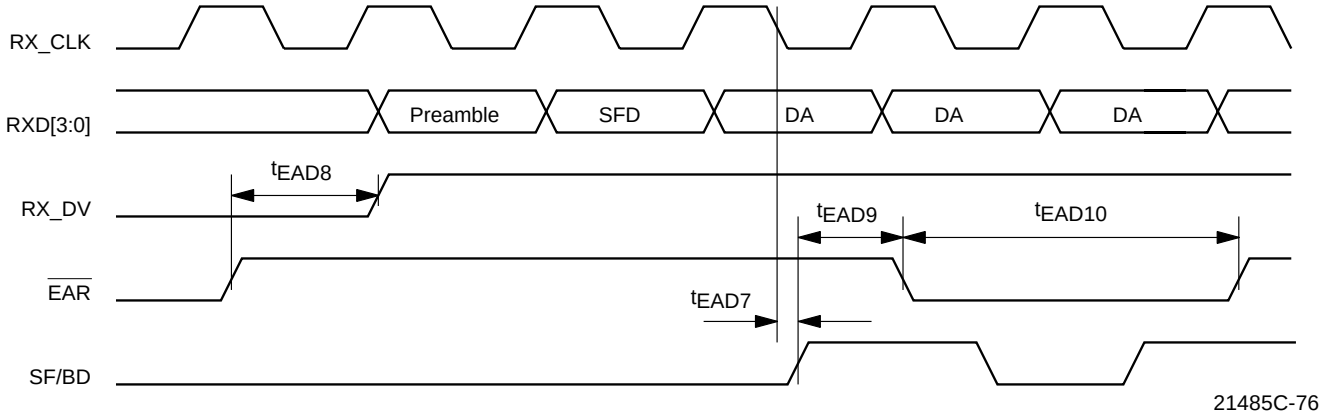


Figure 73. Reject Timing - External PHY MII @ 25 MHz

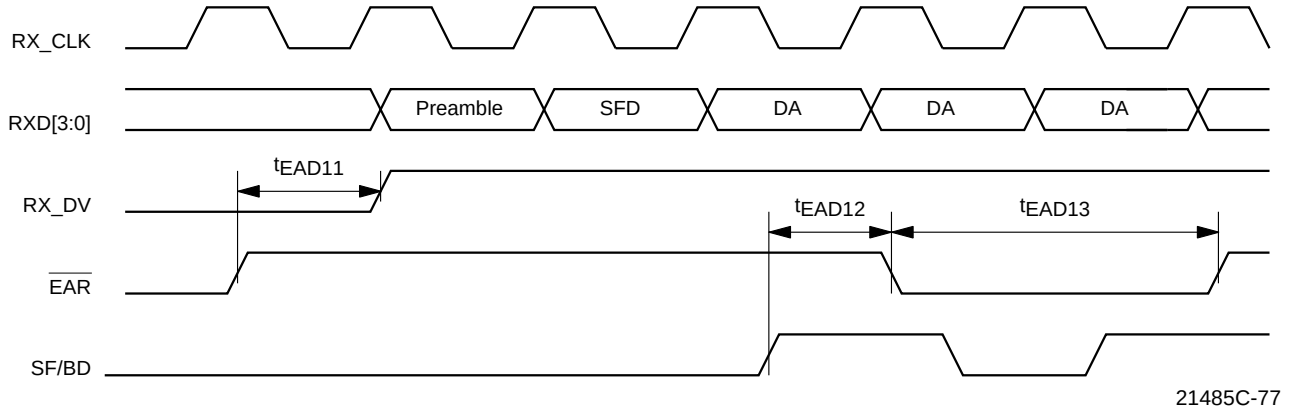


Figure 74. Reject Timing - External PHY MII @ 2.5 MHz

SWITCHING WAVEFORMS: RECEIVE FRAME TAG

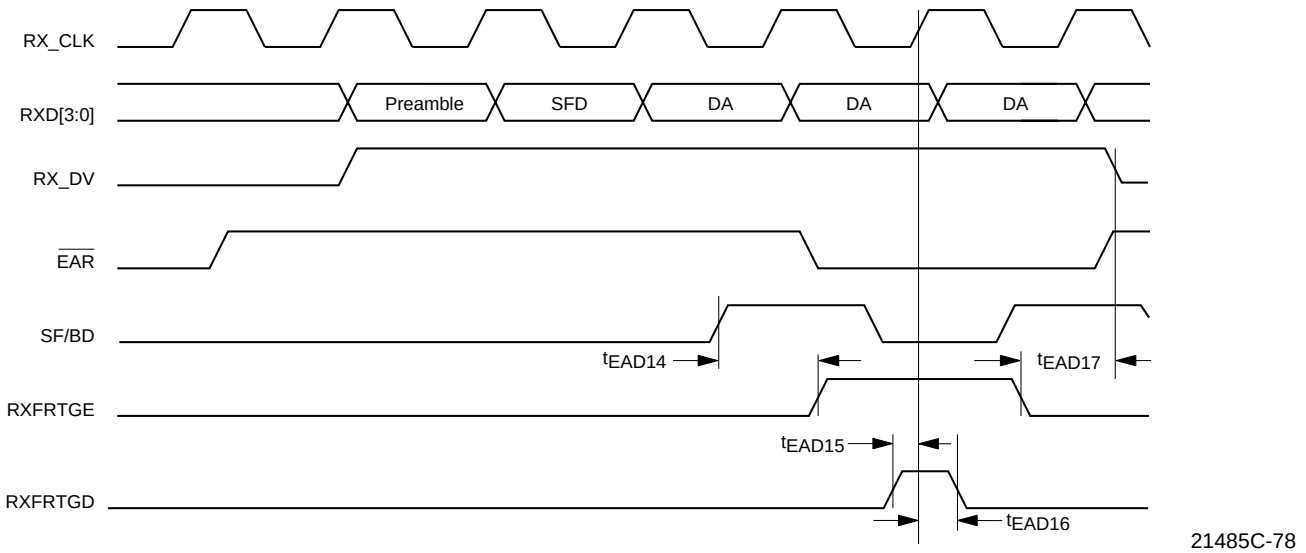
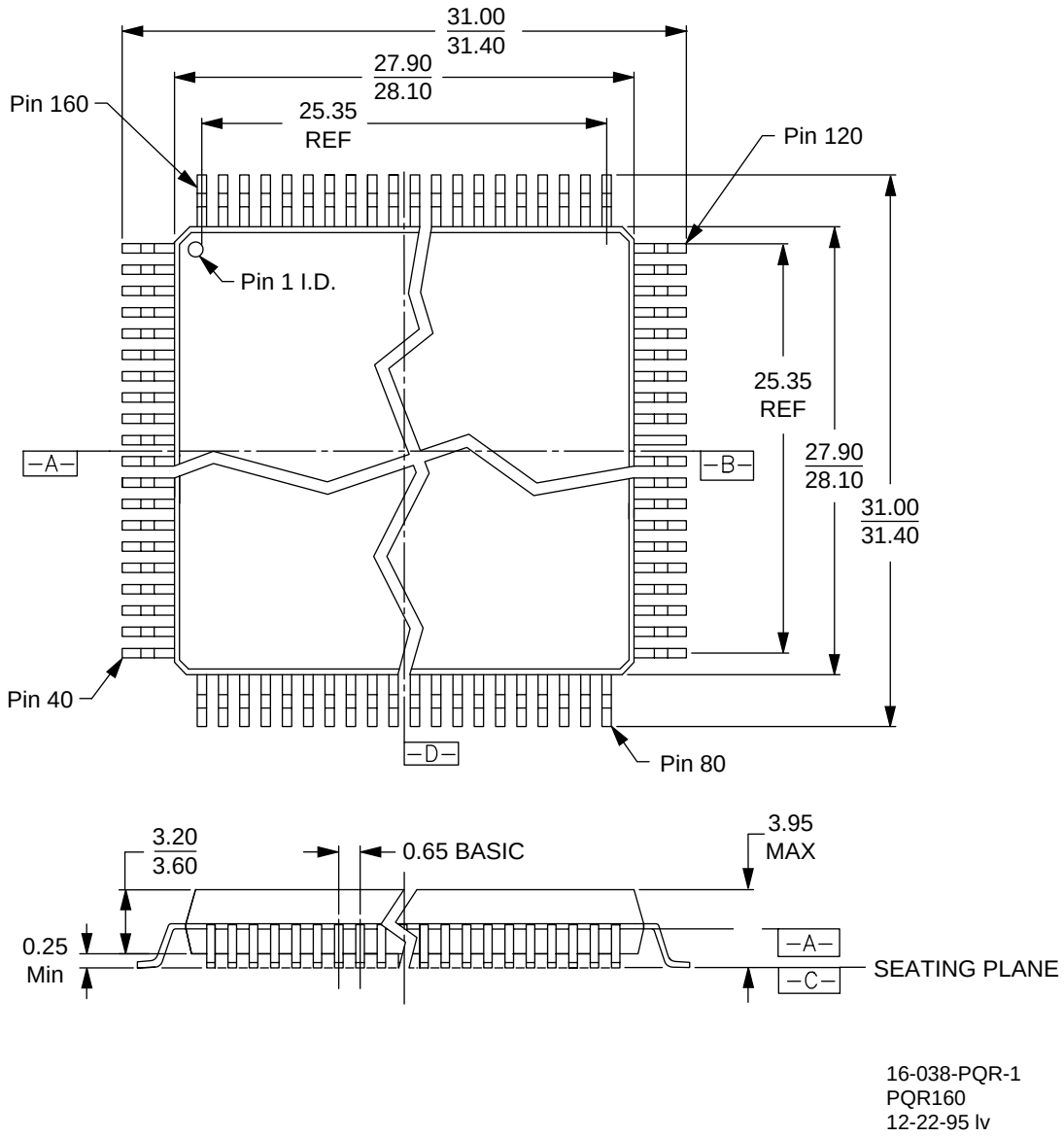


Figure 75. Receive Frame Tag Timing with Media Independent Interface

PHYSICAL DIMENSIONS*

PQR160

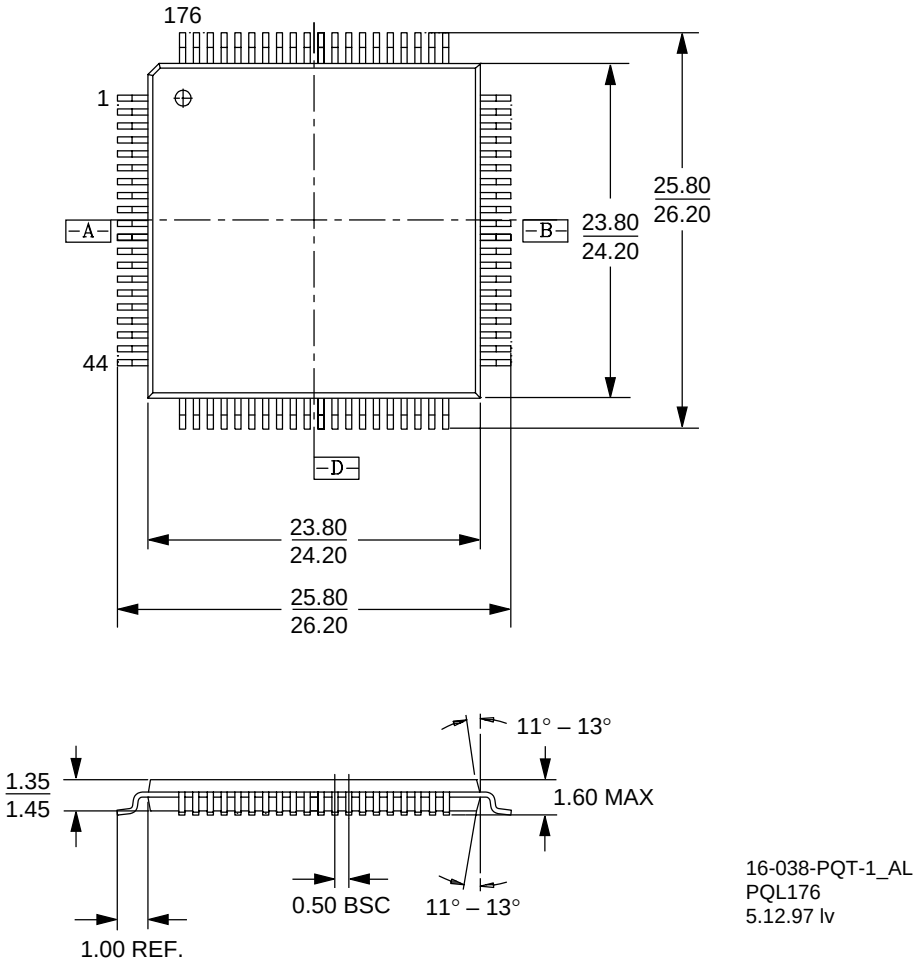
Plastic Quad Flat Pack (measured in millimeters)



16-038-PQR-1
PQR160
12-22-95 lv

**For reference only. BSC is an ANSI standard for Basic Space Centering.*

PQL176
Thin Quad Flat Pack (measured in millimeters)



16-038-PQT-1_AL
PQL176
5.12.97 lv

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APPENDIX A

Alternative Method for Initialization

The Am79C972 controller may be initialized by performing I/O writes only. That is, data can be written directly to the appropriate control and status registers (CSR instead of reading from the initialization block in memory). The registers that must be written are shown in Table A-47. These register writes are followed by writing the START bit in CSR0.

Table A-47. Registers for Alternative Initialization Method (Note 1)

Control and Status Register	Comment
CSR2	IADR[31:16] (Note 2)
CSR8	LADRF[15:0]
CSR9	LADRF[31:16]
CSR10	LADRF[47:32]
CSR11	LADRF[63:48]
CSR12	PADR[15:0] (Note 3)
CSR13	PADR[31:16] (Note 3)
CSR14	PADR[47:32] (Note 3)
CSR15	Mode
CSR24-25	BADR
CSR30-31	BADX
CSR47	TXPOLLINT
CSR49	RXPOLLINT
CSR76	RCVRL
CSR78	XMTRL

Note:

1. The INIT bit must not be set or the initialization block will be accessed instead.

2. Needed only if SSIZE32 =0.

3. Needed only if the physical address is different from the one stored in EEPROM or if there is no EEPROM present.

Look-Ahead Packet Processing (LAPP) Concept

INTRODUCTION

A driver for the Am79C972 controller would normally require that the CPU copy receive frame data from the controllers buffer space to the applications buffer space after the entire frame has been received by the controller. For applications that use a ping-pong windowing style, the traffic on the network will be halted until the current frame has been completely processed by the entire application stack. This means that the time between last byte of a receive frame arriving at the client's Ethernet controller and the client's transmission of the first byte of the next outgoing frame will be separated by:

1. The time that it takes the client's CPU interrupt procedure to pass software control from the current task to the driver,
2. Plus the time that it takes the client driver to pass the header data to the application and request an application buffer,
3. Plus the time that it takes the application to generate the buffer pointer and then return the buffer pointer to the driver,
4. Plus the time that it takes the client driver to transfer all of the frame data from the controller's buffer space into the application's buffer space and then call the application again to process the complete frame,
5. Plus the time that it takes the application to process the frame and generate the next outgoing frame, and
6. Plus the time that it takes the client driver to set up the descriptor for the controller and then write a TDMD bit to CSR0.

The sum of these times can often be about the same as the time taken to actually transmit the frames on the wire, thereby, yielding a network utilization rate of less than 50 percent.

An important thing to note is that the Am79C972 controller's data transfers to its buffer space are such that the system bus is needed by the Am79C972 controller for approximately 4 percent of the time. This leaves 96 percent of the system bus bandwidth for the CPU to perform some of the interframe operations in advance of the completion of network receive activity, if possible.

The question then becomes: how much of the tasks that need to be performed between reception of a frame and transmission of the next frame can be performed before the reception of the frame actually ends at the network, and how can the CPU be instructed to perform these tasks during the network reception time?

The answer depends upon exactly what is happening in the driver and application code, but the steps that can be performed at the same time as the receive data are arriving include as much as the first three steps and part of the fourth step shown in the sequence above. By performing these steps before the entire frame has arrived, the frame throughput can be substantially increased.

A good increase in performance can be expected when the first three steps are performed before the end of the network receive operation. A much more significant performance increase could be realized if the Am79C972 controller could place the frame data directly into the application's buffer space; (i.e., eliminate the need for step 4.) In order to make this work, it is necessary that the application buffer pointer be determined before the frame has completely arrived, then the buffer pointer in the next descriptor for the receive frame would need to be modified in order to direct the Am79C972 controller to write directly to the application buffer. More details on this operation will be given later.

An alternative modification to the existing system can gain a smaller but still significant improvement in performance. This alternative leaves step 4 unchanged in that the CPU is still required to perform the copy operation, but is allows a large portion of the copy operation to be done before the frame has been completely received by the controller, i.e., the CPU can perform the copy operation of the receive data from the Am79C972 controller's buffer space into the application buffer space before the frame data has completely arrived from the network. This allows the copy operation of step 4 to be performed concurrently with the arrival of network data, rather than sequentially, following the end of network receive activity.

Outline of LAPP Flow

This section gives a suggested outline for a driver that utilizes the LAPP feature of the Am79C972 controller.

Note: *The labels in the following text are used as references in the timeline diagram that follows (Figure B-1).*

Setup

The driver should set up descriptors in groups of three, with the OWN and STP bits of each set of three descriptors to read as follows: 11b, 10b, 00b.

An option bit (LAPPEN) exists in CSR3, bit position 5; the software should set this bit. When set, the LAPPEN bit directs the Am79C972 controller to generate an INTERRUPT when STP has been written to a receive descriptor by the Am79C972 controller.

Flow

The Am79C972 controller polls the current receive descriptor at some point in time before a message arrives. The Am79C972 controller determines that this receive buffer is OWNed by the Am79C972 controller and it stores the descriptor information to be used when a message does arrive.

N0 Frame preamble appears on the wire, followed by SFD and destination address.

N1 The 64th byte of frame data arrives from the wire. This causes the Am79C972 controller to begin frame data DMA operations to the first buffer.

C0 When the 64th byte of the message arrives, the Am79C972 controller performs a lookahead operation to the next receive descriptor. This descriptor should be owned by the Am79C972 controller.

C1 The Am79C972 controller intermittently requests the bus to transfer frame data to the first buffer as it arrives on the wire.

S1 The driver remains idle.

C2 When the Am79C972 controller has completely filled the first buffer, it writes status to the first descriptor.

C3 When the first descriptor for the frame has been written, changing ownership from the Am79C972 controller to the CPU, the Am79C972 controller will generate an SRP INTERRUPT. (This interrupt appears as a RINT interrupt in CSR0).

S1 The SRP INTERRUPT causes the CPU to switch tasks to allow the Am79C972 controller's driver to run.

C4 During the CPU interrupt-generated task switching, the Am79C972 controller is performing a lookahead operation to the third descriptor. At this point in time, the third descriptor is owned by the CPU.

Note: *Even though the third buffer is not owned by the Am79C972 controller, existing AMD Ethernet controllers will continue to perform data DMA into the buffer space that the controller already owns (i.e., buffer number 2). The controller does not know if buffer space in buffer number 2 will be sufficient or not for this frame, but it has no way to tell except by trying to move the entire message into that space. Only when the message does not fit will it signal a buffer error condition--there is no need to panic at this point that it discovers that it does not yet own descriptor number 3.*

S2 The first task of the drivers interrupt service routing is to collect the header information from the Am79C972 controller's first buffer and pass it to the application.

S3 The application will return an application buffer pointer to the driver. The driver will add an offset to the application data buffer pointer, since the Am79C972 controller will be placing the first portion of the message into the first and second buffers. (the modified application data buffer pointer will only be directly used by the Am79C972 controller when it reaches the third buffer.) The driver will place the modified data buffer pointer into the final descriptor of the group (#3) and will grant ownership of this descriptor to the Am79C972 controller.

C5 Interleaved with S2, S3, and S4 driver activity, the Am79C972 controller will write frame data to buffer number 2.

S4 The driver will next proceed to copy the contents of the Am79C972 controller's first buffer to the beginning of the application space. This copy will be to the exact (unmodified) buffer pointer that was passed by the application.

S5 After copying all of the data from the first buffer into the beginning of the application data buffer, the driver will begin to poll the ownership bit of the second descriptor. The driver is waiting for the Am79C972 controller to finish filling the second buffer.

C6 At this point, knowing that it had not previously owned the third descriptor and knowing that the current message has not ended (there is more data in the FIFO), the Am79C972 controller will make a last ditch lookahead to the final (third) descriptor. This time the ownership will be TRUE (i.e., the descriptor belongs tot he controller), because the driver wrote the application pointer into this descriptor and then changed the ownership to give the descriptor to the Am79C972 controller back at S3. Note that if steps S1, S2, and S3 have not completed at this time, a BUFF error will result.

C7 After filling the second buffer and performing the last chance lookahead to the next descriptor, the Am79C972 controller will write the status and change the ownership bit of descriptor number 2.

S6 After the ownership of descriptor number 2 has been changed by the Am79C972 controller, the next driver poll of the second descriptor will show ownership granted to the CPU. The driver now copies the data from buffer number 2 into the middle section of the application buffer space. This operation is interleaved with the C7 and C8 operations.

C8 The Am79C972 controller will perform data DMA to the last buffer, whose pointer is pointing to application space. Data entering the least buffer will not need the infamous double copy that is required by existing drivers, since it is being placed directly into the application buffer space.

N2 The message on the wire ends.

S7 When the driver completes the copy of buffer number 2 data to the application buffer space, it begins polling descriptor number 3.

C9 When the Am79C972 controller has finished all data DMA operations, it writes status and changes ownership of descriptor number 3.

S8 The driver sees that the ownership of descriptor number 3 has changed, and it calls the application to tell the application that a frame has arrived.

S9 The application processes the received frame and generates the next TX frame, placing it into a TX buffer.

S10 The driver sets up the TX descriptor for the Am79C972 controller.

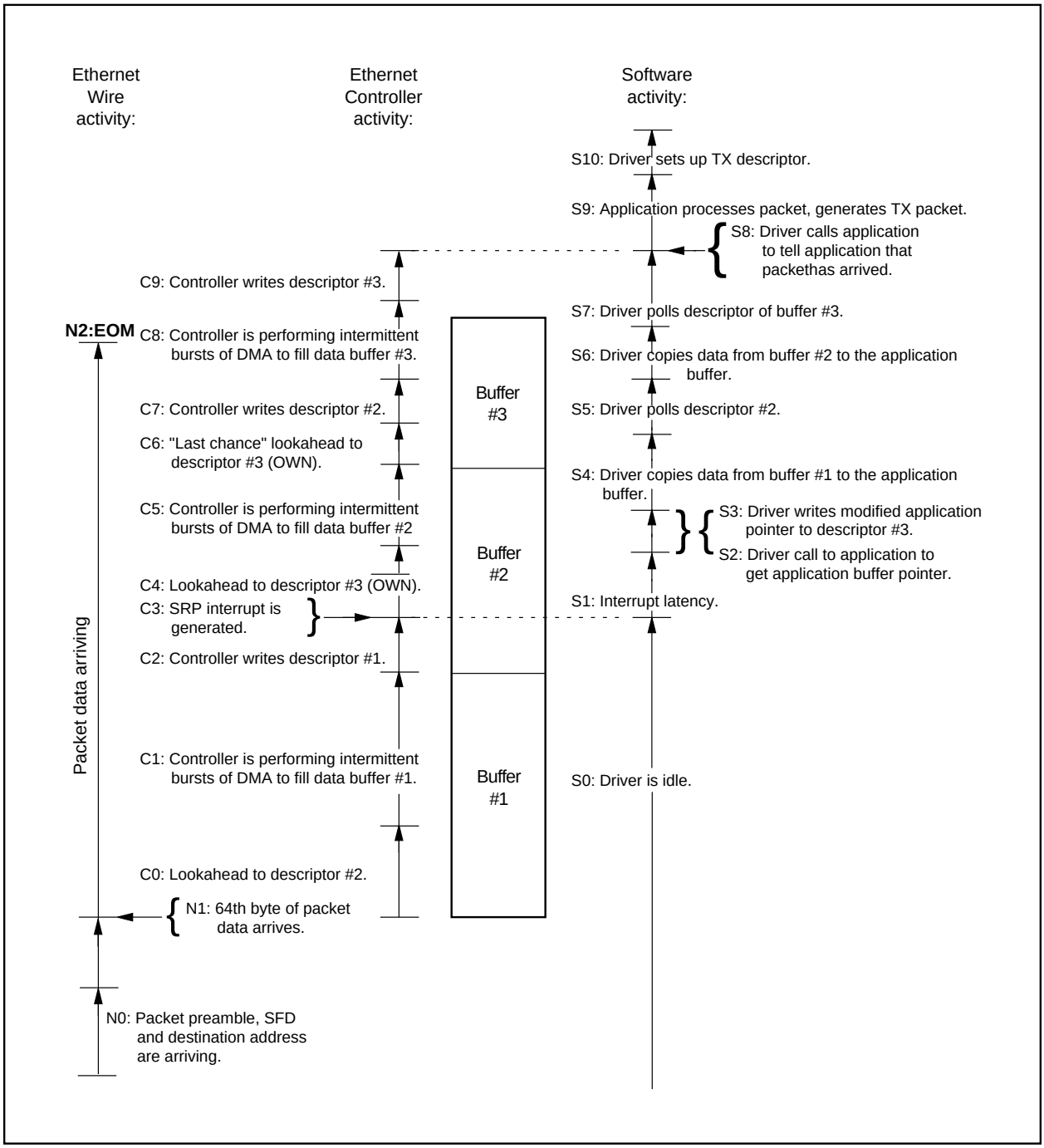

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Figure B-1. LAPP Timeline

LAPP Software Requirements

Software needs to set up a receive ring with descriptors formed into groups of three. The first descriptor of each group should have OWN = 1 and STP = 1, the second descriptor of each group should have OWN = 1 and STP = 0. The third descriptor of each group should have OWN = 0 and STP = 0. The size of the first buffer (as indicated in the first descriptor) should be at least equal to the largest expected header size; however, for maximum efficiency of CPU utilization, the first buffer size should be larger than the header size. It should be equal to the expected number of message bytes, minus the time needed for interrupt latency and minus the application call latency, minus the time needed for the driver to write to the third descriptor, minus the time needed for the drive to copy data from buffer number 2 to the application buffer space. Note that the time needed for the copies performed by the driver depends upon the sizes of the second and third buffers, and that the sizes of the second and third buffers need to be set according to the time needed for the data copy operations. This means that an iterative self-adjusting mechanism needs to be placed into the software to determine the correct buffer sizing for optimal operation. Fixed values for buffer sizes may be used; in such a case, the LAPP method will still provide a significant performance increase, but the performance increase will not be maximized.

Figure B-2 illustrates this setup for a receive ring size of 9.

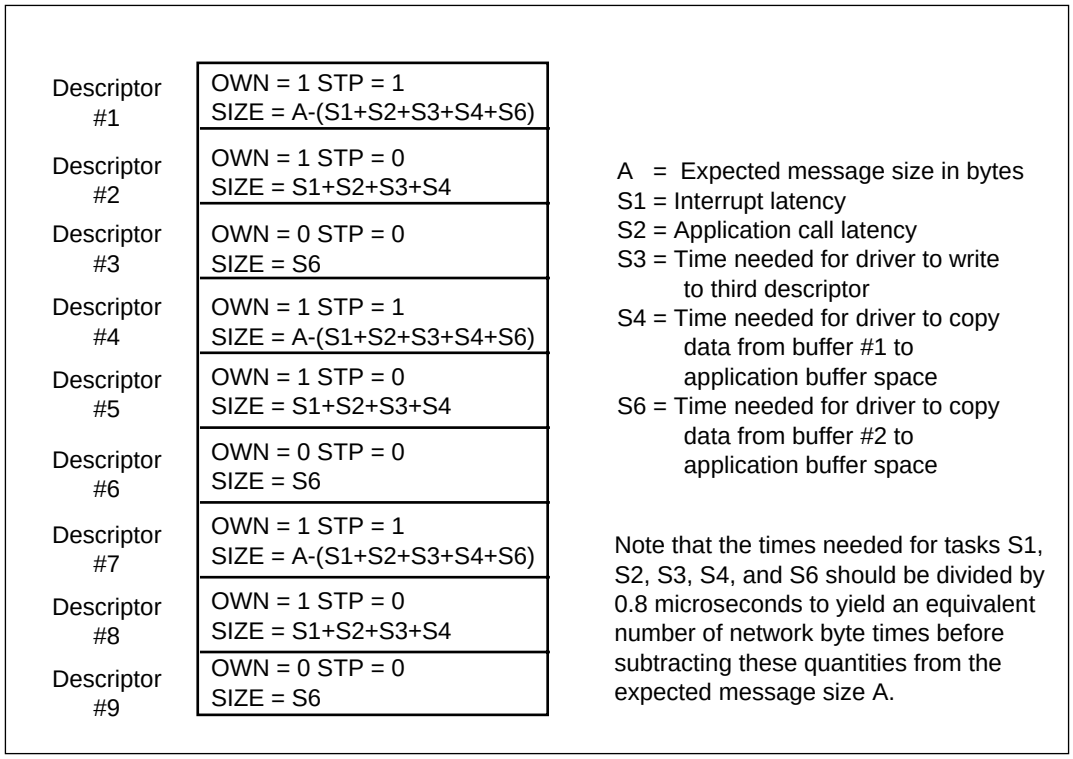

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Figure B-2. LAPP 3 Buffer Grouping

LAPP Rules for Parsing Descriptors

When using the LAPP method, software must use a modified form of descriptor *parsing* as follows:

- Software will examine OWN and STP to determine where an RCV frame begins. RCV frames will only begin in buffers that have OWN = 0 and STP = 1.
- Software shall assume that a frame continues until it finds either ENP = 1 or ERR = 1.
- Software must discard all descriptors with OWN = 0 and STP = 0 and move to the next descriptor when searching for the beginning of a new frame; ENP and ERR should be ignored by software during this search.
- Software cannot change an STP value in the receive descriptor ring after the initial setup of the ring is complete, even if software has ownership of the STP

descriptor, unless the previous STP descriptor in the ring is also OWNED by the software.

When LAPPEN = 1, then hardware will use a modified form of descriptor *parsing* as follows:

- The controller will examine OWN and STP to determine where to begin placing an RCV frame. A new RCV frame will only begin in a buffer that has OWN = 1 and STP =1.
- The controller will always obey the OWN bit for determining whether or not it may use the next buffer for a chain.
- The controller will always mark the end of a frame with either ENP = 1 or ERR = 1.

The controller will discard all descriptors with OWN = 1 and STP = 0 and move to the next descriptor when searching for a place to begin a new frame. It discards these descriptors by simply changing the ownership bit from OWN = 1 to OWN = 0. Such a descriptor is unused for receive purposes by the controller, and the driver must recognize this. (The driver will recognize this if it follows the software rules.)

The controller will ignore all descriptors with OWN = 0 and STP = 0 and move to the next descriptor when searching for a place to begin a new frame. In other words, the controller is allowed to skip entries in the ring that it does not own, but only when it is looking for a place to begin a new frame.

Some Examples of LAPP Descriptor Interaction

Choose an expected frame size of 1060 bytes. Choose buffer sizes of 800, 200, and 200 bytes.

- **Example 1**: Assume that a 1060 byte frame arrives correctly, and that the timing of the early interrupt and the software is smooth. The descriptors will have changed from:

Descriptor Number	Before the Frame Arrives			After the Frame Arrives			Comments (After Frame Arrival)
	OWN	STP	ENP[a]	OWN	STP	ENP[b]	
1	1	1	x	0	1	0	Bytes 1-800
2	1	0	X	0	0	0	Bytes 801-1000
3	0	0	X	0	0	1	Bytes 1001-1060
4	1	1	X	1	1	X	Controller's current location
5	1	0	X	1	0	X	Not yet used
6	0	0	X	0	0	X	Not yet used
etc.	1	1	X	1	1	X	Net yet used

a. *& b. ENP or ERR.*

- **Example 2**: Assume that instead of the expected 1060 byte frame, a 900 byte frame arrives, either because there was an error in the network, or because this is the last frame in a file transmission sequence

Descriptor Number	Before the Frame Arrives			After the Frame Arrives			Comments (After Frame Arrival)
	OWN	STP	ENP[a]	OWN	STP	ENP[b]	
1	1	1	x	0	1	0	Bytes 1-800
2	1	0	X	0	0	0	Bytes 801-1000
3	0	0	X	0	0	?*	Discarded buffer
4	1	1	X	1	1	X	Controller's current location
5	1	0	X	1	0	X	Not yet used
6	0	0	X	0	0	X	Not yet used
etc.	1	1	X	1	1	X	Net yet used

a. *& b. ENP or ERR.*

Note: *The Am79C972 controller might write a ZERO to ENP location in the third descriptor. Here are the two possibilities:*

1. If the controller finishes the data transfers into buffer number 2 after the driver writes the application modified buffer pointer into the third descriptor, then the controller will write a ZERO to ENP for this buffer and will write a ZERO to OWN and STP.
2. If the controller finishes the data transfers into buffer number 2 before the driver writes the applications

modified buffer point into the third descriptor, then the controller will complete the frame in buffer number 2 and then skip the then unowned third buffer. In this case, the Am79C972 controller will not have had the opportunity to RESET the ENP bit in this descriptor, and it is possible that the software left this bit as ENP = 1 from the last time through the ring. Therefore, the software must treat the location as a *don't care.* The rule is, after finding ENP = 1 (or ERR = 1) in descriptor number 2, the software must ignore ENP bits until it finds the next STP = 1.

- **Example 3**: Assume that instead of the expected 1060 byte frame, a 100 byte frame arrives, because there was an error in the network, or because this is the last frame in a file transmission sequence, or perhaps because it is an acknowledge frame.

**Same as note in example 2 above, except that in this case, it is very unlikely that the driver can respond to the interrupt and get the pointer from the application before the Am79C972 controller has completed its poll of the next descriptors. This means that for almost all occurrences of this case, the Am79C972 controller will not find the OWN bit set for this descriptor and, therefore, the ENP bit will almost always contain the old value, since the Am79C972 controller will not have had an opportunity to modify it.*

***Note that even though the Am79C972 controller will write a ZERO to this ENP location, the software should treat the location as a don't care, since after finding the ENP = 1 in descriptor number 2, the software should ignore ENP bits until it finds the next STP = 1.*

Descriptor Number	Before the Frame Arrives			After the Frame Arrives			Comments (After Frame Arrival)
	OWN	STP	ENP[a]	OWN	STP	ENP[b]	
1	1	1	x	0	1	0	Bytes 1-800
2	1	0	X	0	0	0**	Discarded buffer
3	0	0	X	0	0	?	Discarded buffer
4	1	1	X	1	1	X	Controller's current location
5	1	0	X	1	0	X	Not yet used
6	0	0	X	0	0	X	Not yet used
etc.	1	1	X	1	1	X	Net yet used

a. *& b.ENP or ERR*.

Buffer Size Tuning

For maximum performance, buffer sizes should be adjusted depending upon the expected frame size and the values of the interrupt latency and application call latency. The best driver code will minimize the CPU utilization while also minimizing the latency from frame end on the network to the frame sent to application from driver (frame latency). These objectives are aimed at increasing throughput on the network while decreasing CPU utilization.

Note: *The buffer sizes in the ring may be altered at any time that the CPU has ownership of the corresponding descriptor. The best choice for buffer sizes will maximize the time that the driver is swapped out, while minimizing the time from the last byte written by the Am79C972 controller to the time that the data is passed from the driver to the application. In the diagram, this corresponds to maximizing S0, while minimizing the time between C9 and S8. (the timeline happens to show a minimal time from C9 to S8.)*

Note: *By increasing the size of buffer number 1, we increase the value of S0. However, when we increase the size of buffer number 1, we also increase the value of S4. If the size of buffer number 1 is too large, then the driver will not have enough time to perform tasks S2, S3, S4, S5, and S6. The result is that there will be delay from the execution of task C9 until the execution of task S8. A perfectly timed system will have the values for S5 and S7 at a minimum.*

An average increase in performance can be achieved, if the general guidelines of buffer sizes in Figure 2 is followed. However, as was noted earlier, the correct sizing for buffers will depend upon the expected message size. There are two problems with relating expected message size with the correct buffer sizing:

1. Message sizes cannot always be accurately predicted, since a single application may expect different message sizes at different times. Therefore, the buffer sizes chosen will not always maximize throughput.
2. Within a single application, message sizes might be somewhat predictable, but when the same driver is to be shared with multiple applications, there may not be a common predictable message size.

Additional problems occur when trying to define the correct sizing because the correct size also depends upon the interrupt latency, which may vary from system to system, depending upon both the hardware and the software installed in each system.

In order to deal with the unpredictable nature of the message size, the driver can implement a self-tuning mechanism that examines the amount of time spent in tasks S5 and S7. As such, while the driver is polling for each descriptor, it could count the number of poll operations performed and then adjust the number 1 buffer size to a larger value, by adding “t” bytes to the buffer count, if the number of poll operations was greater than ”x.” If fewer than “x” poll operations were needed for each of S5 and S7, then software should adjust the buffer size to a smaller value by subtracting “y” bytes from the buffer count. Experiments with such a tuning mechanism must be performed to determine the best values for “x” and “y.”

Note: *Whenever the size of buffer number 1 is adjusted, buffer sizes for buffer number 2 and buffer number 3 should also be adjusted.*

In some systems, the typical mix of receive frames on a network for a client application consists mostly of large data frames, with very few small frames. In this case, for maximum efficiency of buffer sizing, when a frame arrives under a certain size limit, the driver should not adjust the buffer sizes in response to the short frame.

An Alternative LAPP Flow: Two-Interrupt Method

An alternative to the above suggested flow is to use two interrupts, one at the start of the receive frame and the other at the end of the receive frame, instead of just looking for the SRP interrupt as described above. This alternative attempts to reduce the amount of time that the software wastes while polling for descriptor own bits. This time would then be available for other CPU tasks. It also minimizes the amount of time the CPU needs for data copying. This savings can be applied to other CPU tasks.

The time from the end of frame arrival on the wire to delivery of the frame to the application is labeled as frame latency. For the one-interrupt method, frame latency is minimized, while CPU utilization increases. For the two-interrupt method, frame latency becomes greater, while CPU utilization decreases. See Figure B-3.

Note: *Some of the CPU time that can be applied to non-Ethernet tasks is used for task switching in the CPU. One task switch is required to swap a non-Ethernet task into the CPU (after S7A) and a second task switch is needed to swap the Ethernet driver back in again (at S8A). If the time needed to perform these task switches exceeds the time saved by not polling descriptors, then there is a net loss in performance with this method. Therefore, the LAPP method implemented should be carefully chosen.*

Figure B-4 shows the buffer sizing for the two-interrupt method. Note that the second buffer size will be about the same for each method.

There is another alternative which is a marriage of the two previous methods. This third possibility would use the buffer sizes set by the two-interrupt method, but would use the polling method of determining frame end. This will give good frame latency but at the price of very high CPU utilization. And still, there are even more compromise positions that use various fixed buffer sizes and, effectively, the flow of the one-interrupt method. All of these compromises will reduce the complexity of the one-interrupt method by removing the heuristic buffer sizing code, but they all become less efficient than heuristic code would allow.

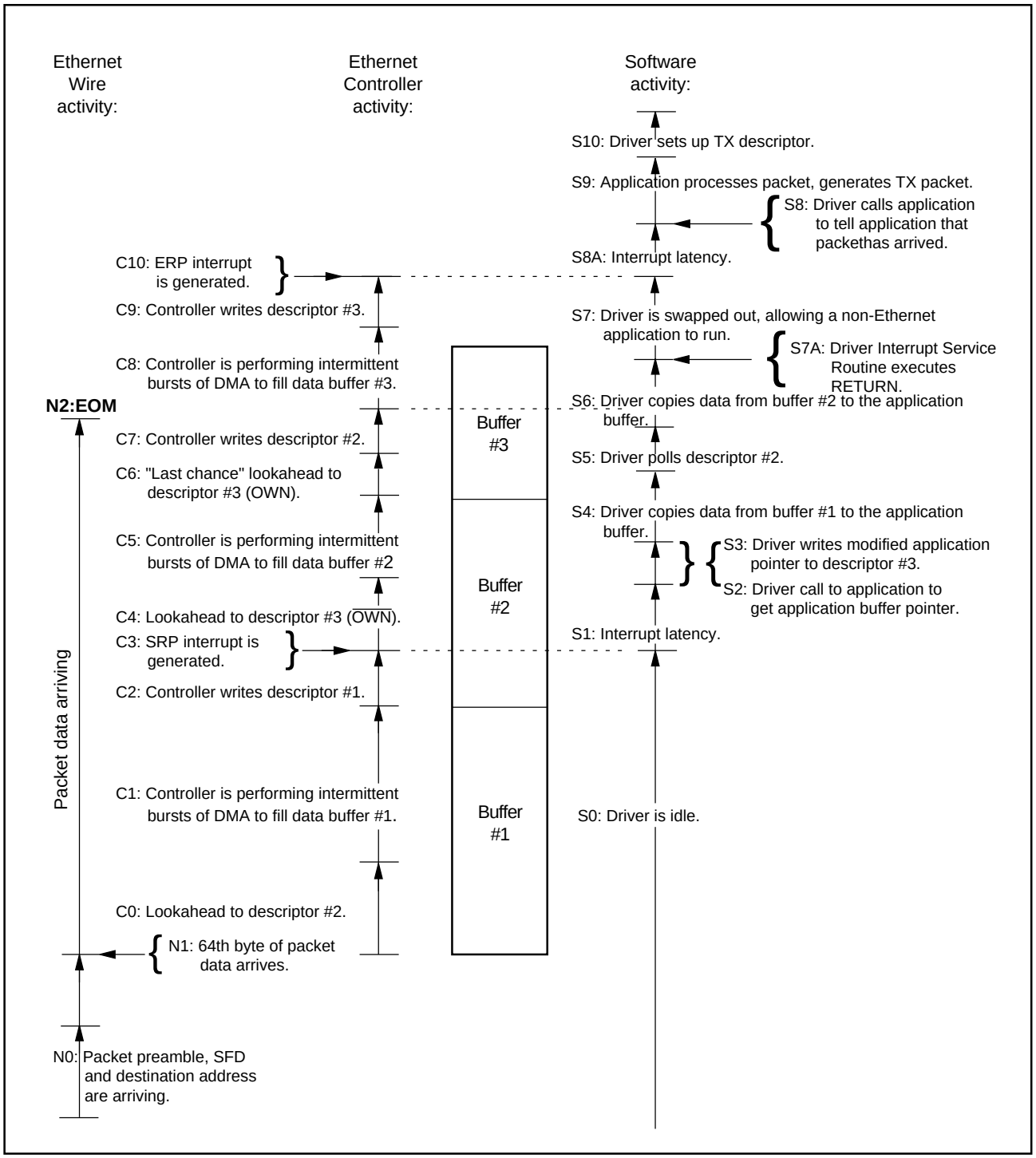

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Figure B-3. LAPP Timeline for Two-Interrupt Method

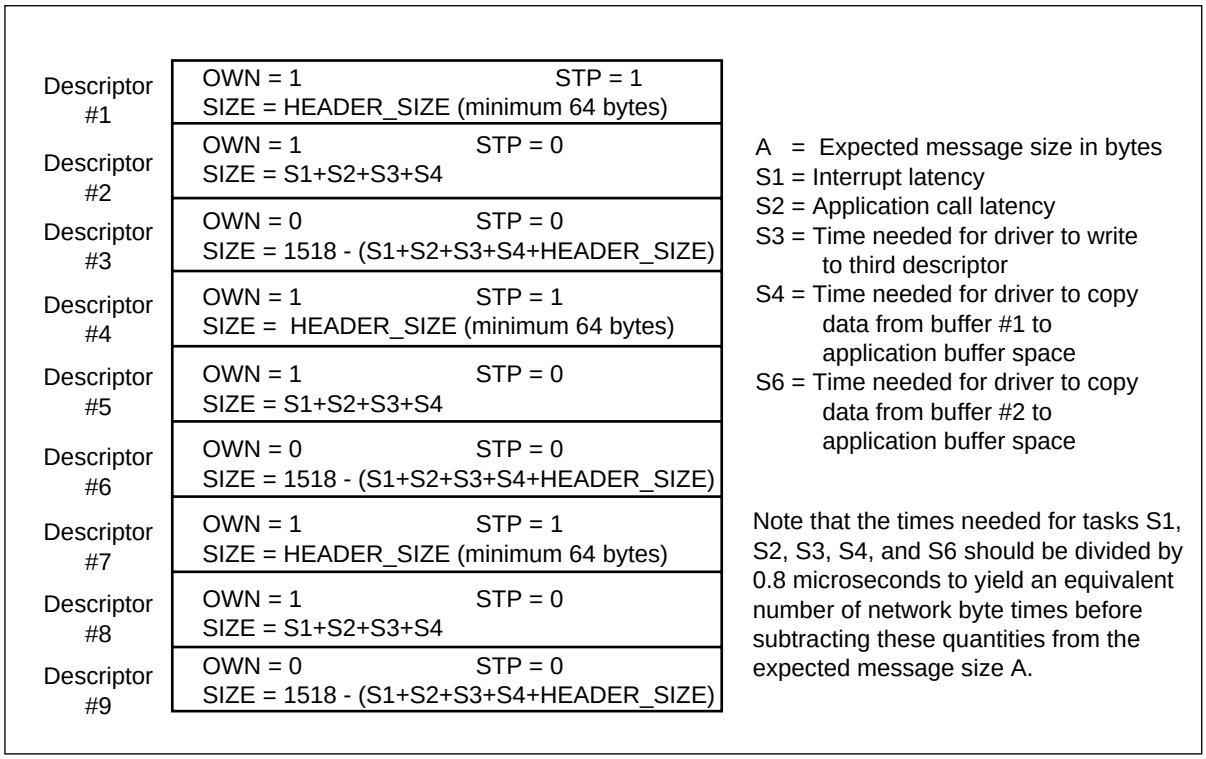

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Figure B-4. LAPP 3 Buffer Grouping for Two-interrupt Method

MII Management Registers

As specified in the IEEE standard, the basic register set consists of the Control Register (Register 0) and the Status Register (Register 1). The extended register set consists of Registers 2 to 31 (decimal). All PHYs that provide an MII shall incorporate the basic register set. Both sets of registers are accessible through the MII Management Interface.

Table C-48 lists the most interesting registers.

Control Register (Register 0)

Table C-49 shows the MII Management Control Register (Register 0).

Table C-48. MII Management Register Set

Register Address	Register Name	Basic/ Extended
0	MII Control	B
1	MII Status	B
2-3	PHY Identifier	E
4	Auto-Negotiation Advertisement	E
5	Auto-Negotiation Link Partner Ability	E

Table C-49. MII Management Control Register (Register 0)

Bits	Name	Description	Read/Write (Note 1)
15	Soft Reset	When write: 1 = PHY software reset 0 = normal operation. When read: 1 = reset in process 0 = reset done.	R/W, SC
14	Loopback	1 = enables Loopback mode 0 = disables Loopback mode	R/W
13	Speed Selection	1 = 100 Mbps 0 = 10 Mbps	R/W
12	Auto-Negotiation Enable	1 = enable Auto-Negotiation 0 = disable Auto-Negotiation	R/W
11	Power Down	1 = power down, 0 = normal operation	R/W
10	Isolate	1 = electrically isolate PHY from MII 0 = normal operation	R/W
9	Restart Auto-Negotiation	1 = restart Auto-Negotiation 0 = normal operation	R/W, SC
8	Duplex Mode	1 = full duplex 0 = half duplex	R/W
7	Collision Test	1 = enable COL signal test 0 = disable COL signal test	R/W
6-0	Reserved	Write as 0, ignore on read	RO

Note:

1. R/W = Read/Write, SC = Self Clearing, RO = Read only.

Status Register (Register 1)

The MII Management Status Register identifies the physical and auto-negotiation capabilities of the PHY. This register is read only; a write will have no effect. See Table C-50.

Table C-50. MII Management Status Register (Register 1)

Bits	Name	Description	Read/Write (Note 1)
15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO
14	100BASE-X Full Duplex	1 = PHY able to perform full-duplex 100BASE-X 0 = PHY not able to perform full-duplex 100BASE-X	RO
13	100BASE-X Half Duplex	1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X	RO
12	10 Mbps Full Duplex	1 = PHY able to operate at 10 Mbps full-duplex mode 0 = PHY not able to operate at 10 Mbps full-duplex mode	RO
11	10 Mbps Half Duplex	1 = PHY able to operate at 10 Mbps half-duplex mode 0 = PHY not able to operate at 10 Mbps half-duplex mode	RO
10-7	Reserved	Ignore when read	RO
6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed 0 = PHY not able to accept management frames with preamble suppressed	RO
5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
4	Remote Fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO, LH
3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
2	Link Status	1 = link is up 0 = link is down	RO, LL
1	Jabber Detect	1 = jabber condition detected, 0 = no jabber condition detected	RO
0	Extended Capability	1 = extended register capabilities, 0 = basic register set capabilities only	RO

Note:

1. RO = Read Only, LH = Latching High, LL = Latching Low.

Auto-Negotiation Advertisement Register (Register 4)

The purpose of this register is to advertise the technology ability to the link partner device. See Table C-51.

When this register is modified, Restart Auto-Negotiation (Register 0, bit 9) must be enabled to guarantee the change is implemented.

Table C-51. Auto-Negotiation Advertisement Register (Register 4)

Bit(s)	Name	Description	Read/ Write
15	Next Page	When set, the device wishes to engage in next page exchange. If clear, the device does not wish to engage in next page exchange.	R/W
14	Reserved		RO
13	Remote Fault	When set, a remote fault bit is inserted into the base link code word during the Auto Negotiation process. When cleared, the base link code word will have the bit position for remote fault as cleared.	R/W
12:5	Technology Ability	Link partner technology ability field.	RO
4:0	Selector Field	Link partner selector field.	RO

Technology Ability Field Bit Assignments

The technology bit field consists of bits A0-A8 in the IEEE 802.3 Selector Base Page. Table C-52 summarizes the bit assignments.

Table C-52. Technology Ability Field Bit Assignments

Bit	Technology
A0	10BASE-T
A1	10BASE-T Full Duplex
A2	100BASE-TX
A3	100BASE-TX Full Duplex
A4	100BASE-T4
A5	Reserved for future technology
A6	Reserved for future technology
A7	Reserved for future technology

Auto-Negotiation Link Partner Ability Register (Register 5)

The Auto-Negotiation Link Partner Ability Register is Read Only. The register contains the advertised ability of the link partner. The bit definitions represent the received link code word. This register contains either the base page or the link partner's next pages. See Table C-53.

Table C-53. Auto-Negotiation Link Partner Ability Register (Register 5) - Base Page Format

Bit(s)	Name	Description	Read/ Write
15	Next Page	Link partner next page request.	RO
14	Acknowledge	Link partner acknowledgment	RO
13	Remote Fault	Link partner remote fault request	RO
12:5	Technology Ability	Link partner technology ability field	RO
4:0	Selector Field	Link partner selector field.	RO

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